

# ELECTRICALLY RECONFIGURABLE LOGIC ARRAY

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## ABSTRACT

The VLSI technology has been exploited to build more complication and special purpose devices. Some of these devices tailored to certain complex algorithm, systolic array processors, combinational logic, programmable logic array and graphic display. The use of microcircuit is due to its leverage in high integration and uniformity for mass production of simple logic or circuit elements in the algorithm.

How does one compose the complicated systems using algorithmically specialized logic circuits or processors. One solution is to perform relational computations such as union, division and intersection directly on hardware. These relations can be poplined efficiently on network of processor having array configuration. These processors can be designed and implemented with few simple cells.

In order to determine the state-of-the-art in Electrically Reconfigurable Logic Array (ERLA), a survey of the available programmable logic array (PLA) and the logic circuit elements used in such arrays was conducted. Based on this survey some recommendations are made for ERLA devices.

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## INTRODUCTION

For the last 20 to 25 years, the semiconductor industry has been in the turmoil of innovative changes and has been the prime example of innovative excellence in the U.S.A. Similar innovation going in the NASA programs as well as in the electronic laboratory of the Marshall Space Flight Center. With the innovation of integrated circuit and now with very large integrated logic array (circuit in the range 100,000 to 1,000,000 on a single chip), new approaches have to be invented as how to interconnect such logic array. In the order to keep the manufacturing cost have the logic arrays are fabricated with the standard logic circuits. Using the computer aided mask design. These arrays can be connected to the desired configuration. With the invention of Programmable logic array, it is deasible to see if these logic arrays can be reprogrammed or its configuration changed electrical signed in the field. The first objective of this investigation is to find on-going work in the areas of electrically reconfigurable logic arrays (ERLA). Also study different circuit configurations and fabrication microelectronic techniques with are presently used in programmable logic arrays, and investigate if any of the current fabrication technique may be suitable for 'ERLA' design.

## CONCLUSIONS AND RECOMMENDATIONS

The Electronically Reconfigurable Logic Arrays (ERLA) is a processed array of microelectronic devices whose configuration (and/or connection) can be changed by external stimuli. There are two approaches to the design of such a system. System one where the system is partitioned into number of small processor elements (PE) also known as bit slice microprocessors whose word length could vary by external stimuli. These PE's (or MPU's) connects through microprocessor control units (MUC) as shown in fig. 1.

The other approach is the Arrays Logic MACROS. The type of logic array considered is the dual or folded array configuration where first one array is made up of programmable decoders whose putput selects words in the second array. The programmable decode array which performs the product function known as AND array, the second array which performs the sum function called OR array, as shown in figure 2.

It seems simple to use any of these two approaches to make ERLA but in practice designs engineer is faced with numbers of basis problems. One of the two main problems are how to interconnect each cross point cell in the associative (AND) logic array and the second problem is having to change the basic function of 0, 2, do't care condition at the cross points as shown in figure 2. The following is the summary of what is available in terms of reprogrammable logic array or ERLA and also which logic circuit configuration and fabrication technique is candidates for ERLA at the present time.

The Restructurable VLSI is another name given to ERLA. The Lincoln Laboratory of Massachusetts Institute of Technology has been working on RVLSI. The Lincoln Laboratory is using dynamic bonding in the Multi Project Chip (MPC) Style of fabricating experimental NMOS integrated circuits. Many unrelated designs are placed on a single die, having each with its own I/O pads. The MPC implementation technique tends to minimize mask and wafer fabrication cost per design but not without some disadvantages. A scheme for the dynamic bonding of experimental NMOS test projects has been implemented by Lincoln Laboratory as shown in fig. 3 in this scheme, all projects of a multi project die are interfaced to the same set of physical I/O pads. The power is turned on for the selected project only. Dynamic bonding would make it feasible to test projects at the wafer level, simplify the packaging procedure, and allow all projects on a die to be tested after packaging.

Redundancy is necessary in very large integrated circuits since processing these circuits are not perfect and some of the circuitry will not function. The Lincoln Laboratory is using an approach to partition the total circuit into pieces which can be individually tested after fabrication. These pieces are interconnected using X-Y grid of conductors and primary interest centers on the device placed at crossing. The Lincoln Laboratory is using lasers zappable links. The zappable links built at Lincoln Laboratory use metal-metal structures. Data gathered at the laboratory showed that these failure modes involving metal-poly and metal-substrate shorts in various test structures. The possibility are that these mechanisms could be exploited to form useful links in MOSIS. Attempts were made to use laser zapping the links but it appeared that three times the amount of beam intensity was required to cut through poly as through metal, indicating that it is possible to make a metal-poly link without shorting through to the substrate.

Some of the future VLSI systems will rely on the use of Programmable Building Blocks. Each building block consists of a set of cell design together with rules for combining the cells into larger circuits, thus using these circuits in larger systems. In the programmable logic array, programmable building blocks are frequently used to implement logic design. These building blocks can be made to change these logical functional output using electrical stimuli. These building blocks can be personalized to obtain various functions. Forter and Kung introduces a new programmable building block for recognition of regular languages. The building block can be programmed for any regular expression using a syntax directed construction method which also allows easy and mechanical verification of circuit properties. The recognizers made using these building blocks are efficient pipeline circuits that have constant response time and avoid broadcast. The Programmable recognizes array (PRA) provide compact reconfigurable layouts, requiring only  $n \log n$  area for the regular expression of length  $n$ . (5)

Another candidate for ERLA is parallel computer. One such computer architecture research is going on at Purdue University called the Configurable, Highly Parallel (Chip) computers. A Chip computer is composed of a set of homogeneous micro-processor elements connected at regular intervals to the switches connected by data paths to each other or to the PE's. The switch lattice is a regular structure formed from programmable switches connected by data paths. The PE's are connected to the switch lattice at regular intervals rather than being directly connected to each other. External storage devices connects to the lattice at the perimeter switches. (7) Figure 4 shows examples of switch lattices. The PE's are shown as squares, the switches as circles and the data path as lines. The switches are circuits rather than packet switches. Each switch contains sufficient local memory to store several interconnecting configuration settings. A particular setting enables the switch to establish a direct, static connection between two or more of its incident data paths. The design of the PE's determines the degrees to which Chip computer is a general purpose computer, hence influenced by the intended applications. A parallel program is considered as the composition of several parallel algorithms each with its own processor interconnection pattern. (7)

A programmable logic array has been recognized as an AND plane forming product terms, followed by an OR plane combining product terms to give required output. In other words these devices realize combinational and sequential logic. In order to make this reconfigurable logic array, AND and OR planes must have the

programming links at each cross point replaced by a link controlled from the memory element or any other external stimuli. The memory element at the crosspoint of each AND and OR grid must also have a means of altering their information content according to some external input.<sup>(8)</sup> Figure 5(a) and 5(b) shows diagram of a general rewritable-programmable logic array (R-PLA, another name for ERLA) using conventional current mode logic (CML) memory element as proposed by Tanka, Ozawa and Mori.<sup>(9)</sup> The ERLA can be constructed by splitting a conventional random access memory into two sections. Hence each cell structure of the ERLA (R-PLA) is thought as the conventional RAM, differing from the complicated cell structure is proposed in (10). Figure 5(a) and 5(b) shows logically as well as electrically that Search and Read parts of R-PLA can perform logic-in-memory without the use of special AND gates in each cell in the Read mode and can enter a Write data from a word direction in the Write mode. In this R-PLA, bit personalities can be easily loaded and dynamically changed word by word to achieve specific logic function during processing.

As mentioned earlier, there is not much thought given to electrically Reconfigurable Logic Arrays, but an extensive literature is available in Alterable or Rewritable Read-Only-Memories (ROM) or electrically reprogrammable ROM (REPROM). The semiconductor fabricated technique most promises for REPROM or ERLA is MNOS. The devices consists of N-channel or P-channel memory transistors with floating (buried) gate, non-volatile memory transistor, which enables reprogramming operation as proposed in (11). The memory is programmed by electron injection by junction avalanche. An internal voltage multiplication scheme using varactor boot strapping is used. Erasure takes place by modified Poole-Frenkel conduction in a  $\text{Si}_3\text{N}_4$  of 700-Å thickness which overlays the buried (floating) gate. In this example, standard silicon gate P-MOS processing is used (12). Bit retention is very good even at 150°C.

The buried gate memory element, as explained in (12), after writing consists of an "ON" P-MOS transistor with a conducting channel. After erasing, the floating gate holds practically no negative charge, leaving the transistor in the "OFF" state. A single transistor and an erase gate is shown in figure 6<sup>(12)</sup> in its simplest form. The floating gate is charged after the write pulse, resulting in an output voltage. An erase pulse at terminal E reduces the storage charge on the floating gate below the transistor threshold voltage. Fig. 7 shows a better form of buried-gate cell involves the addition of a boot strap variable capacitor which is inserted between the access transistor and the floating gate. This provide lower writing voltage by multiplying the voltage of the internal mode.

Fig. 8 shows a 1024 bit erasable buried gate ROM chip. To write, a bit is selected by coincident addressing with  $V_{DD}$  and P-terminal at -23V. Reading is done by addressing the same way as writing except that  $V_{DD}$  and E-terminal are at -15V. It appears at this time that the techniques presented represents a reasonable approach to construct Electronically Reconfigurable logic array. The buried (floating) gate transistor have highest promise for Electrically Reconfigurable logic array. The transistor memory cell can be used in an AND, OR plane. The logic functions can be changed by altering cross point storage in the matrix AND plane as shown in Fig.1. Same type logic or (memory) cell can be used in PE's for the modulator approach in ERLA.

It is recommended that future work should be directed toward MNOS buried (floating) gate transistor element. Also the use of cellular logic in designing specific logic function should be implemented. The buried (floating) gate (shown in fig. 7) can be used as an element for AND and OR plane of macro logic array. (Shown in fig. 1). It only need five metal lines (two for x and y input. one for erase, one to write and one to read) to interconnect entire AND plane. The read output of the buried gate has to be connected as wired 'OR' on the AND plane before it connects to OR plane. Further study is needed to implement buried MNOS gate in the Programmable Logic Array (PLA) macro so that the PLA can be programmed electrically in the field or run as parallel computers. It is further recommended that an experimental ERLA system should be designed, built and tested as a feasibility study.

## REFERENCES

1. Scott, M.A., and Smith, K.C., "A Dynamically Reconfigurable Microprocessor Architecture" IEEE Trans. on Computer, Vol. 5.
2. Jones, J.W., "Array Logic Macros" IBM J. Res. Development, March 1975, pp. 120-126.
3. Anderson, Alen H. "Restructurable VLSI Program Semi-annual Summary Report, Lincoln Laboratory, Mass. Inst. of Tech. April 1979-March 1980, ADA09075.
4. Anderson, Alen H., "Restructurable VLSI Program" Semi-annual Tech, Summary Report, Lincoln Laboratory MIT, April-September 1981 issue Jan. 1982.
5. Forter, J.J., and Kung, H.T., "Recognize Regular Languages with Programmable Building Blocks" Interim Report Dept. of Computer Science, Carnegie-Mellon University, June 19, 1981-AD-A104874
6. Snyder, Lawrence, "Overview of the CHIP Computer "VLSI 81-Book, Edited by John P. Gray, Academic Press, pp. 237-246.
7. Snyder, Lawrence, "Programming Processor Interconnection Structures" Dept. of Computer Science, Purdue University, Oct 1981, AD-A109294.
8. Kinniment, D.J., "Regular Programmable Control Structures "VLSI 1981, edited by John P. Gray, Academic Press. pp.191-202.
9. Tanaka, Mamoru; Ozawa, Shinju, and Mori, Shinsaku, "Rewritable Programmable Logic Array of Current Mode Logic IEEE Trans. on computers Vol. C-30 No. 3 March 1981 pp. 229-234.
10. Fleisher, J., and Maissel, L.I. "An Introduction to Array Logic" IBM J. of Res & Dev. March 1975, pp. 98-109.
11. WADA, Toshi, "Electrically Reprogrammable ROM Using N-channel Memory Transistors with Floating Gate" Solid State Electronics, Vol. 20 1977 pp. 623-627.
12. Newgebauer, Constantine A.; Burgess, James G. and Stein, L "Electrically Erasable Buried-Gate Nonvolatile Read-only Memory" IEEE Trans. on Elec. Devices. Vol. ED-24 No. 5 May 1977 pp. 612-618.
13. Rossler, Bernard, "Electrically Erasable and Reprogrammable Read only Memory using the N-channel SIMOS one-transistor cell "IEEE Trans on Elec. Devices, ED-24 No. 5 May 1977, pp. 606-613.
14. Brewer, Joe E., "MNOS Density Parameters" IEEE Trans. on Elec. Devices, ED-24 No. 5 May 1977, pp. 618-625.
15. Wagner, Richard H. A. "The Gated-Access MNOS Memory Transistor" IEEE Trans. on Elec. Devices. Vol. ED-27, No. 1 Jan. 1980, pp. 226-276.
16. Lonky, M.L.; Fagan J.L.; & Victorey J.P. "VINRAM-AN MDS/MNOS RAM" NAECON 1977, pp. 628-632.

17. LODI, Robert J. Browvicka, M.B.; Kosicki, B.B.; Pogemiller, T.A.; and Eklund, M.V. "MNOS BORAM Memory Characteristics" IEEE Journal of Solid State Circuits Vol. SC-11 No. 5, Oct. 1976, pp. 622-630.
18. Sakural, Junji, "An Experimental Study of the BO-Mos Dynamic RAM Cell" IEEE Trans. of Electron Devices, Vol. ED-28, No. 10, Oct. 1981.
19. Greenwood, Ed, "VLSI Array Processor" R&D Status Report, Jan. 11, 1982, AD-A 111986.
20. Wood, Roy A., "A High Density Programmable Logic Array Chip" IEEE Trans. on Computers, Vol. C-28, No. 9, Sept. 1979, pp. 602-607.
21. Smith, Kent F.; Carter, Tony M. and Hunt, Charles E. "Structured Logic Design of Integrated Circuits Using the Storage/Logic Array (SLA)", IEEE J. of Solid State Circuits, Vol. SC-17, No. 2, April 1982. pp. 395-406.
22. Logue, J.C.; Brickman, N.F.; Howley, F.; Jones, J.W. and Wu, W.W. "Hardware Implementation of a Small System in Programmable Logic Array" IBM J. of Res. and Development, March 1975, pp. 110-119.
23. Patil, Suhas S. and Welch, Terry A. "A Programmable Logic Approach for VLSI" IEEE Trans. on Computer, Vol. C-28, No. 9 Sept. 1979, pp. 594-601.
24. Mukhopadhyay, Amar "Hardware Algorithms for String Processing: IEEE. Trans of Computer, May 1980, pp. 508-511.
25. Kambayashi, Yahuko "logic Design of Programmable Logic Arrays." IEEE Trans of Computers. Vol. 28, No. 9, Sept. 1979, pp. 609-617.
26. Golden, R.L.; Latus, P.A.; and Lowy, P. "Design Automation and Programmable Logic Array Macro". IBM J. Res. Development, Vol. 24 No.1, Jan. 1980 pp. 23-31
27. Mudge, Craig, J. "VLSI Chip Design at the Crossroads." VLSI 81, Academic Press. John P. Gray, editor pp. 205-215.
28. Marques, Alves J. "MOSAIC: A Modular Architecture for VLSI System Circuits" VLSI 81, Academic Press, John P. Gray, editor, pp. 53-61.
29. Kautz, William H., "Programmable Cellur Logic" Recent Developments in Switchup Theory, Book-Amar Murkhopadhyay, editor, Academic Press, 1971. Chapter IX, pp. 369-421.
30. Goates, Gary B.; Waldron, Harvey M.; Patil, Suhar S.; Smith, Kent F. and Tatman, Joseph A., "Storage/Logic Arrays for VHSIC." Proceedings of Semi-Custom Integrated Circuit Technology Symposium, May 26-27, 1981 Glen W. Preston, editor, pp. 191-207.
31. Siskind, Jeffery Mark; Southerland, Jay Roger and Gouch, Kenneth Walter "Generating Custom High Performance VLSI Designs from Succint Algorithmic Descriptions" MIT Lincoln Laboratory, Lexington, MA, Dec. 1981.
32. Brewer, J.E., "MNDS-BORAM Manufacturing Methods and Technology Project" Research and Development Technical Report, DELET-TR-80-0259, Jan. 1982 Westinghouse Electric Corp. Baltimore, MD.

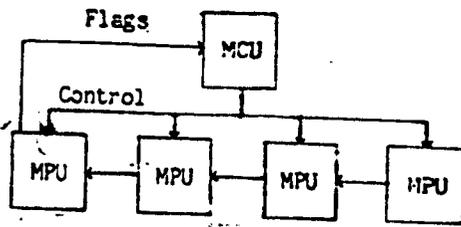


Fig. 1

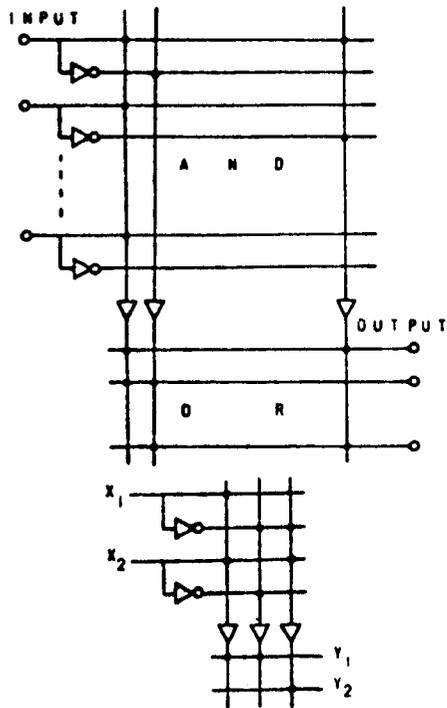


Fig. 2

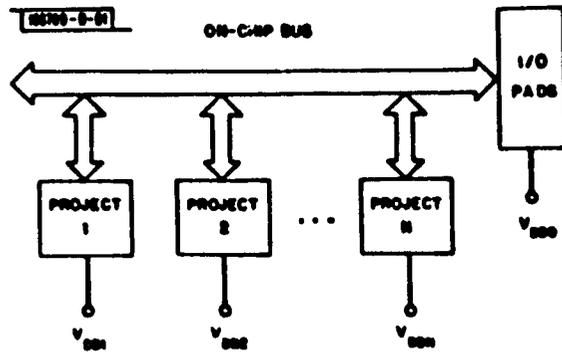


Fig. 3

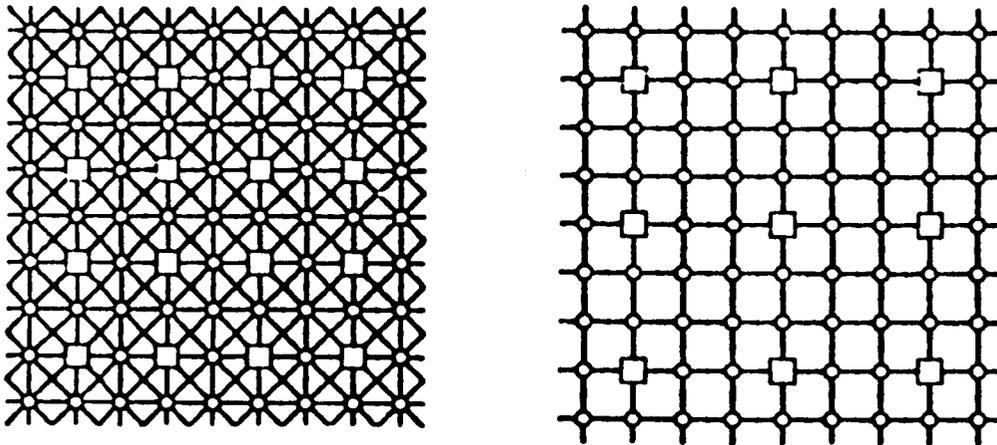


Fig. 4

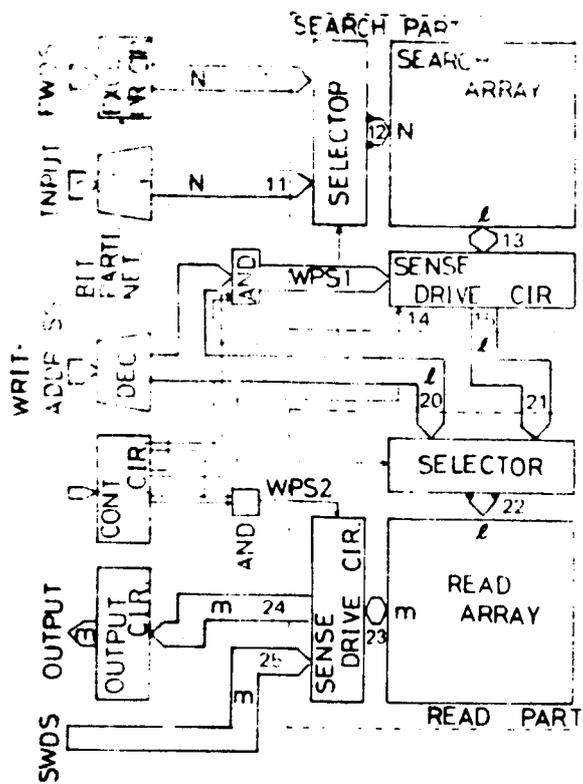


Fig. 5(a)

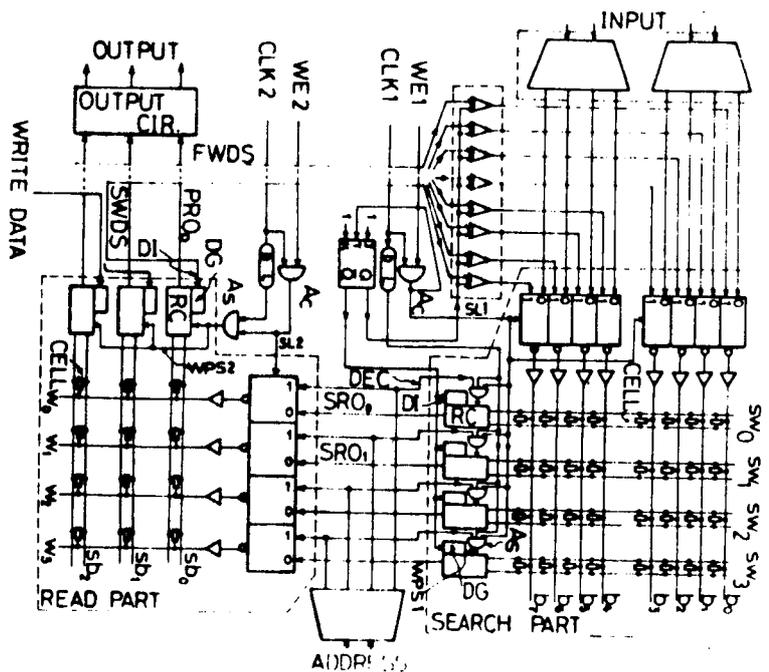


Fig. 5(b)

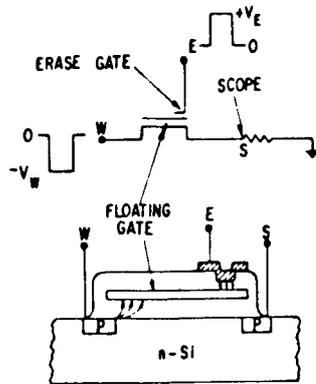


Fig. 6

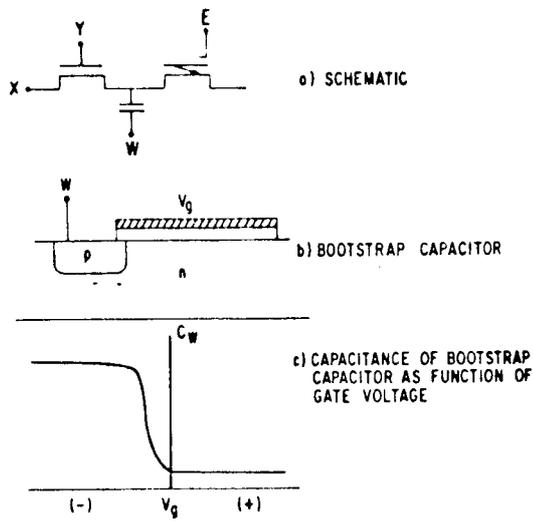


Fig. 7

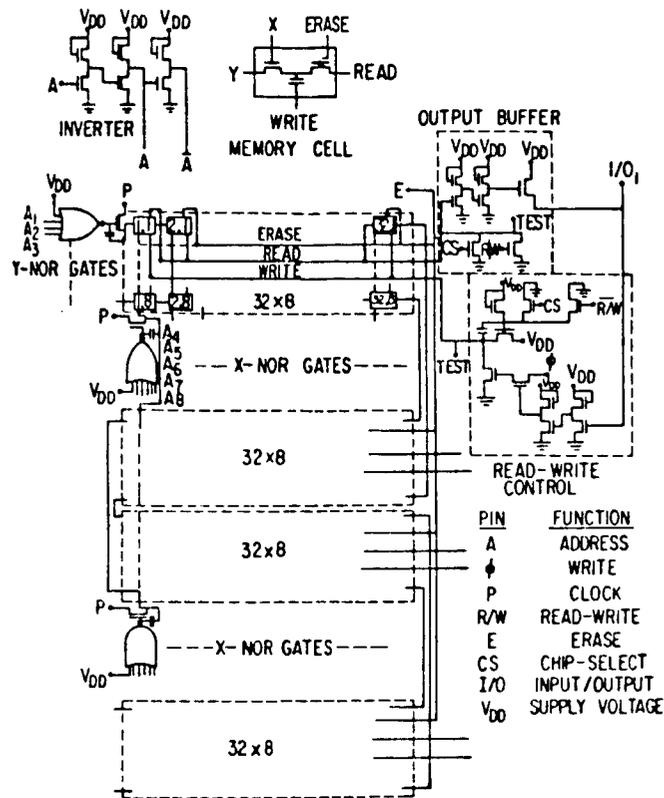


Fig. 8