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RS-232 COMMUNICATIONS ANALYZER MODULE FOR HP-1602A LOGIC ANALYZER

An ASCII analyzer has been designed and built as a plug-in module for a Hewlett-Packard 1602A logic state analyzer. The ASCII analyzer simultaneously examines the transmit and receive serial data lines. When a valid ASCII character is found on either data line, it is converted to a parallel format using a UAR/T. The parallel data is then made available to the logic state analyzer for display. The unit is self-contained and it interfaces directly with the data probe of the HP-1602A. Common baud rates are selectable from 300 to 9600 bits per second.

by

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I. INTRODUCTION

Most microcomputer-based systems utilize some sort of serial data communication for input/output (I/O) purposes. The most commonly encountered serial communication format is the American Standard Code for Information Interchange (ASCII). The need for an ASCII analyzer has surfaced during the debugging of serial interfaces on microcomputer systems.

This paper describes the design and construction of a simple ASCII analyzer. It has been built to interface directly to a Hewlett-Packard 1602A logic state analyzer but the circuitry could easily be configured to operate with any logic analyzer (refer to figures 1, 2, and 3). The design of the ASCII analyzer allows the use of all the trace and delay functions for the HP-1602A.

The ASCII analyzer circuit utilizes two Universal Asynchronous Receiver/Transmitters (UAR/Ts) to simultaneously examine both the transmit and receive serial data lines. Baud rates from 300 to 9600 bits per second are selectable with the externally mounted DIP switch. The unit requires no external power supply connection and all of the integrated circuits are CMOS for low power consumption. (Refer to figures 4 and 5.)

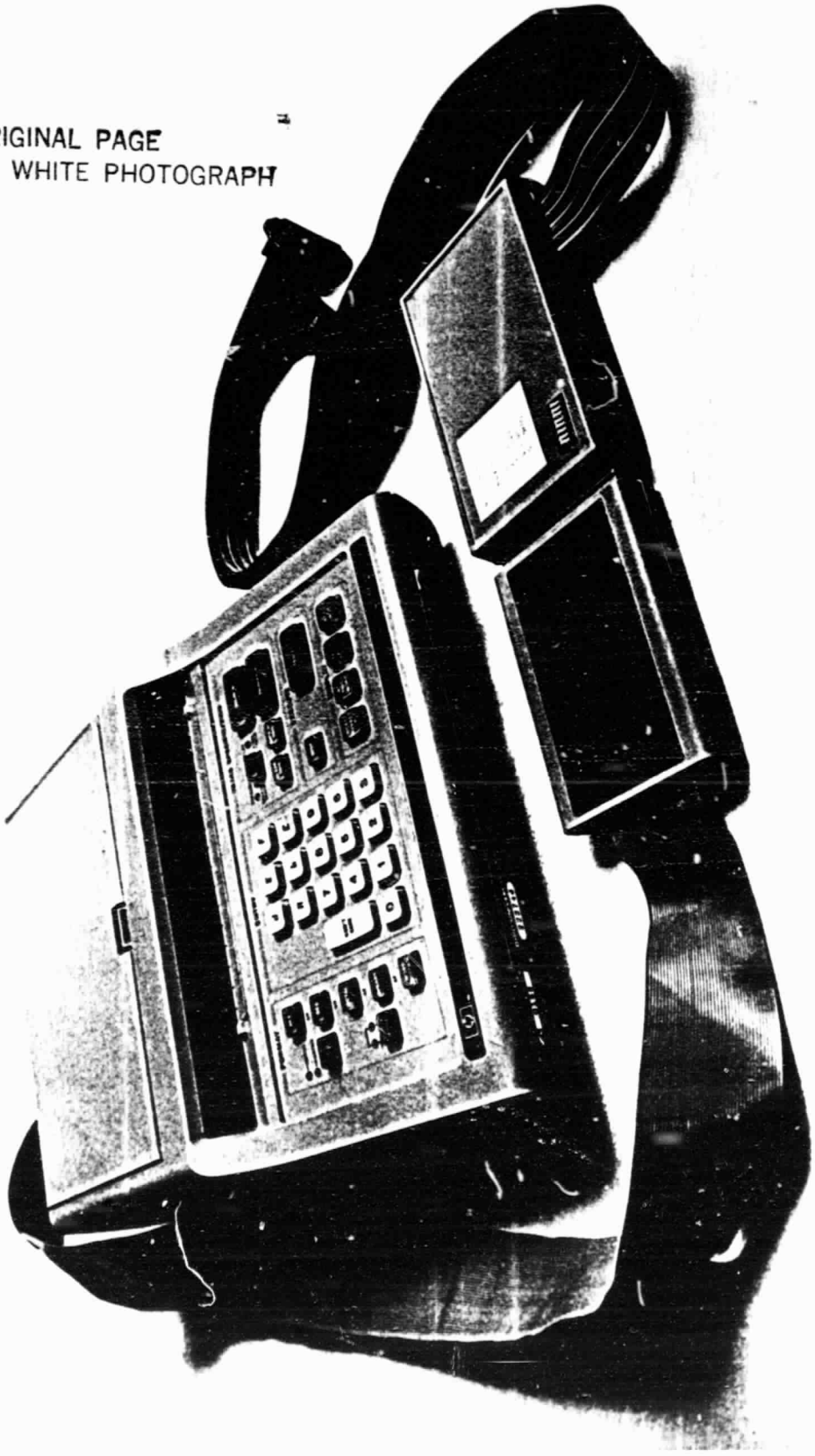


Figure 1. HP-1602A with ASCII Analyzer Module.

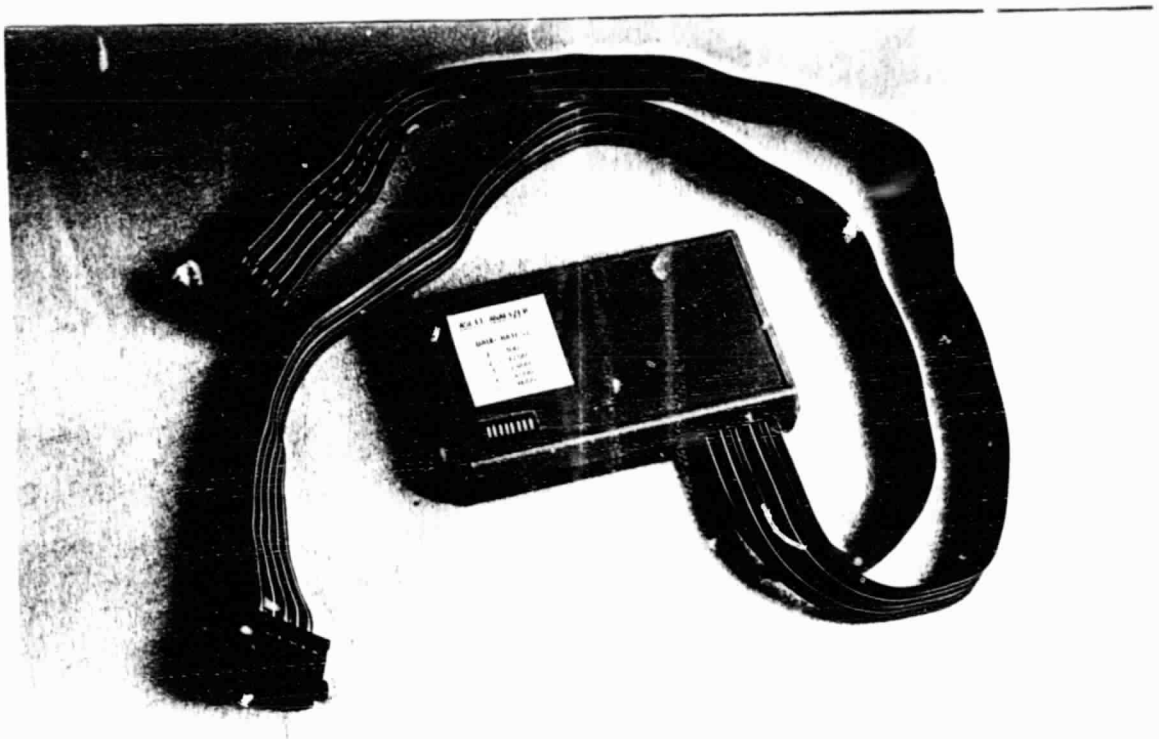


Figure 2. ASCII Analyzer Module.

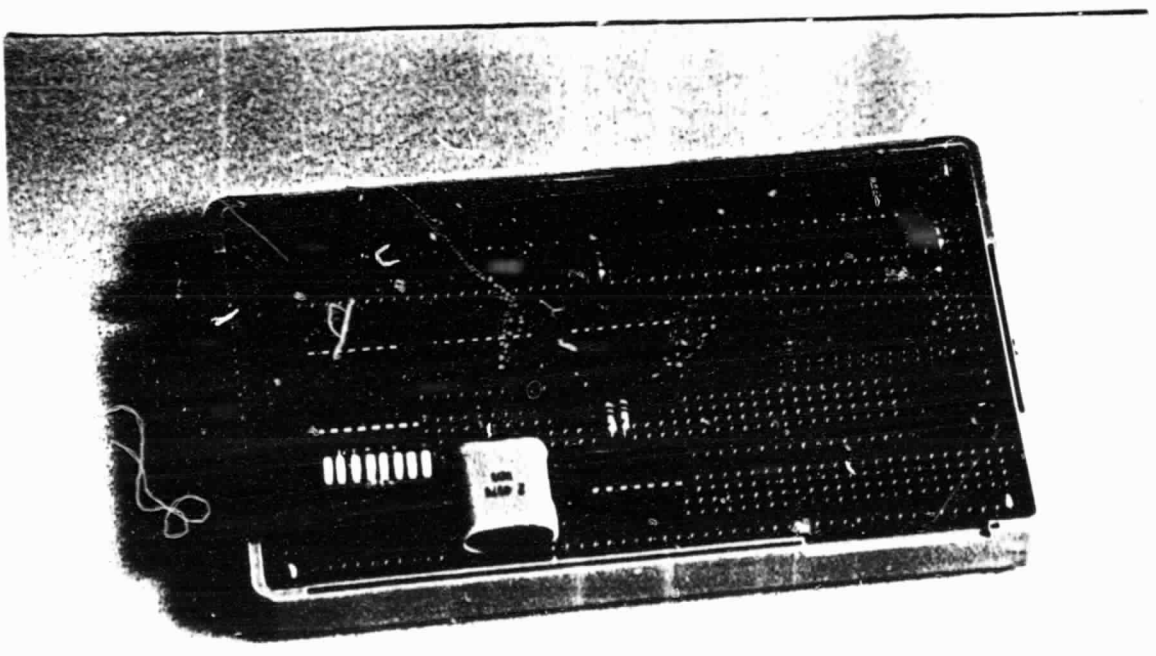


Figure 3. ASCII Analyzer Circuit Board.

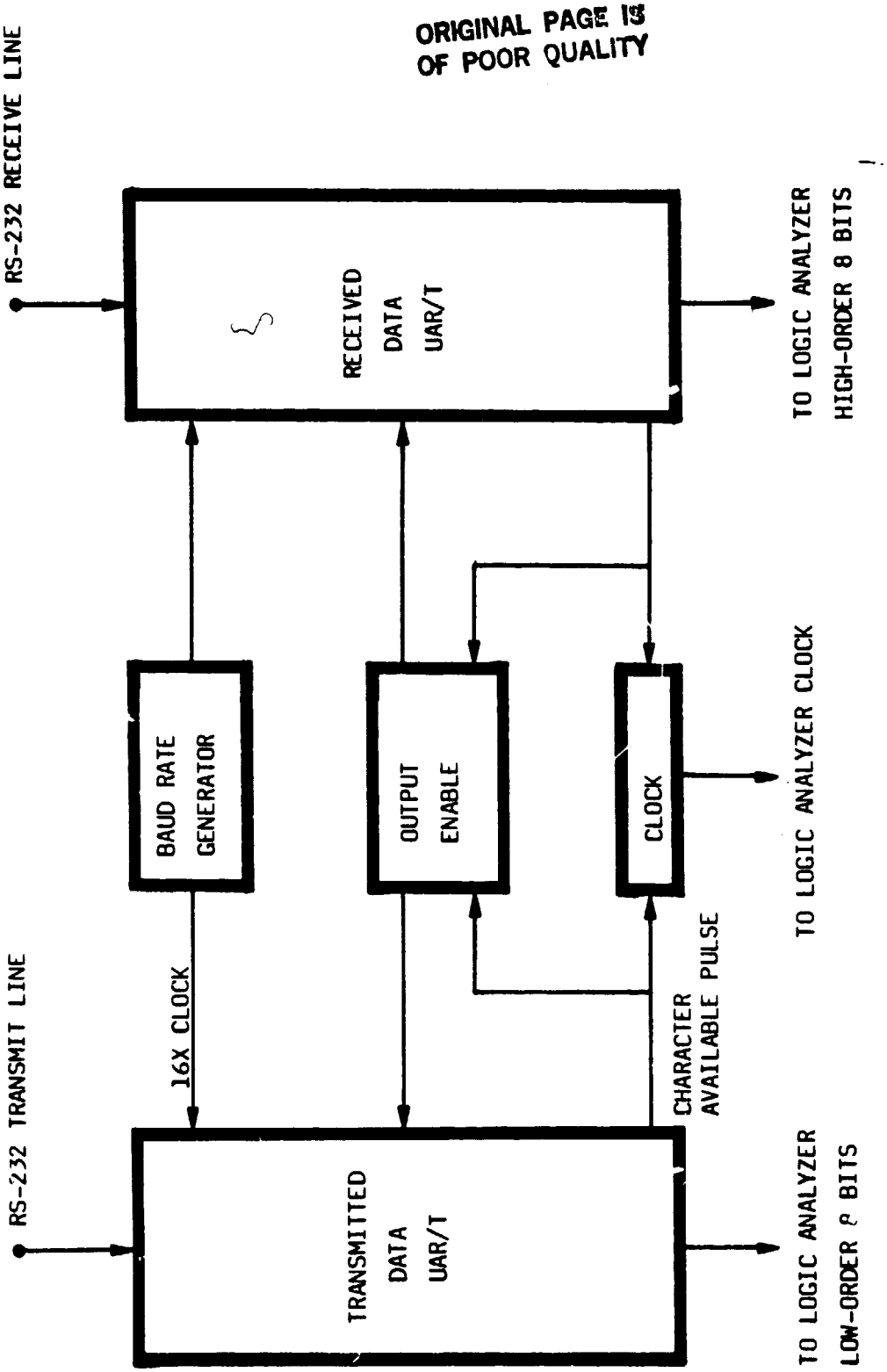


Figure 4. Functional Block Diagram.

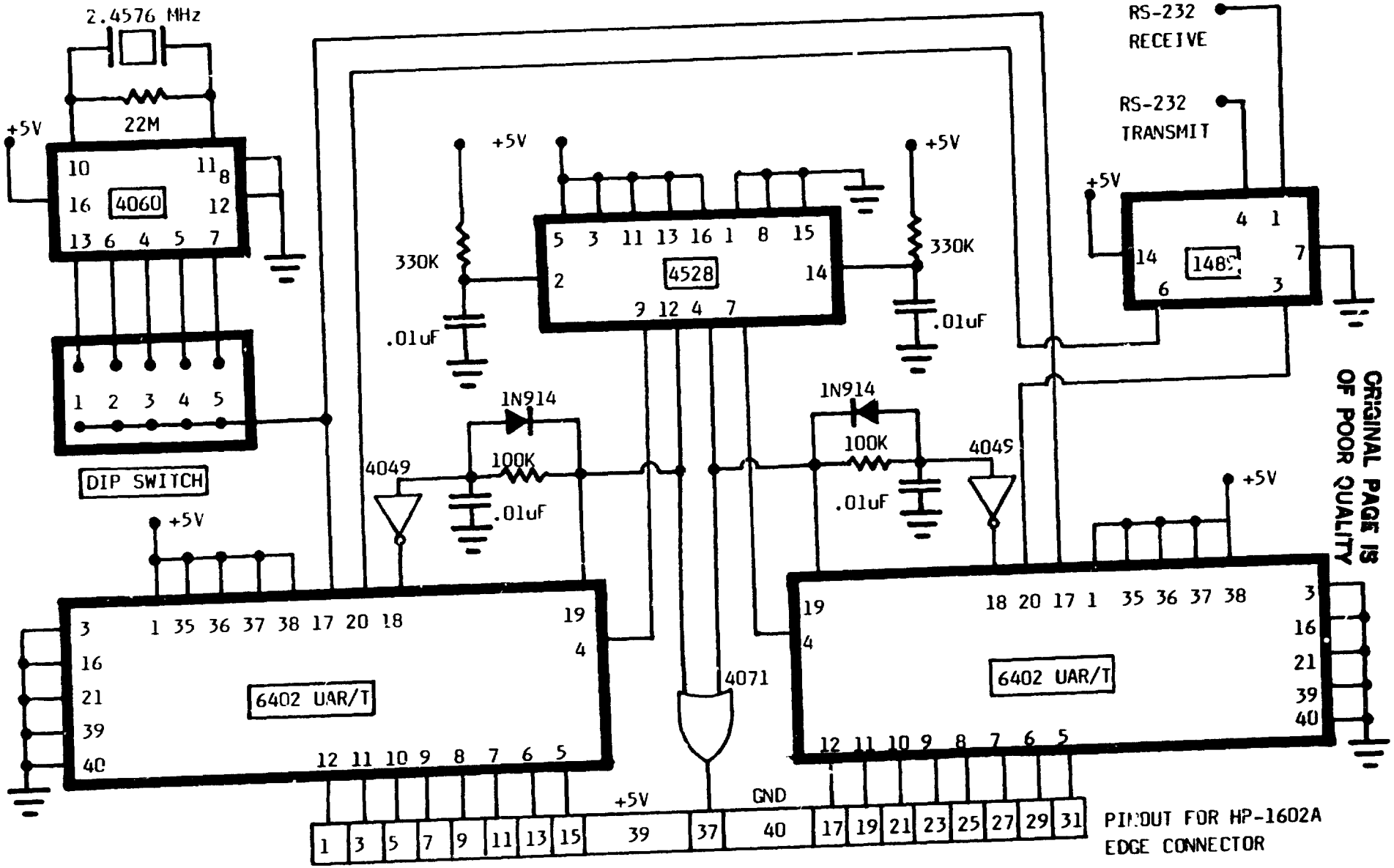


Figure 5. Circuit Diagram.

II. CIRCUIT DESIGN

1. Baud Rate Generator

Both of the UAR/Ts require a 16 times baud rate clock frequency. To supply the frequencies for the desired baud rates, a simple circuit was implemented using a crystal oscillator and a 4060 binary counter. A DIP switch is provided to select the proper frequency. The available baud rates are: 300, 1200, 2400, 4800, and 9600 bits per second.

2. UAR/T Configuration

The 6402 UAR/Ts are both configured as serial receivers, with parallel data output to the logic analyzer (refer to figure 6). Voltage level translation from RS-232 to TTL levels is accomplished with a 1489 line receiver. The received data UAR/T is connected to the RS-232 receive line (pin 3, data transmission device), while the transmitted data UAR/T is connected to the RS-232 send line (pin 2, data transmission device). The UAR/Ts are configured to receive an eight-bit serial data group. This allows the display of the seven ASCII data bits plus the parity bit. (The high order bit is for parity.) The diode circuit obtained from [1] enables the UAR/T to receive the next serial character as soon as the current character is sent to the logic analyzer. The transmitter portion of the UAR/Ts (parallel to serial conversion) is not used.

3. Output Enabling

In order to utilize the trace function of the HP-1602A, the tri-state outputs of the UAR/Ts must be disabled when a character is not being sent. The outputs on the UAR/Ts are enabled by a 4528 dual monostable which is triggered by the data available pulse on the UAR/T (refer to figure 7). When triggered, the monostable enables the UAR/T outputs for one millisecond. This enabling time allows the transmit and receive ASCII characters to appear in the same word of the logic analyzer if they appear at approximately the same time. (This situation is encountered in full duplex serial operation.) The 4528 was configured as suggested in [2].

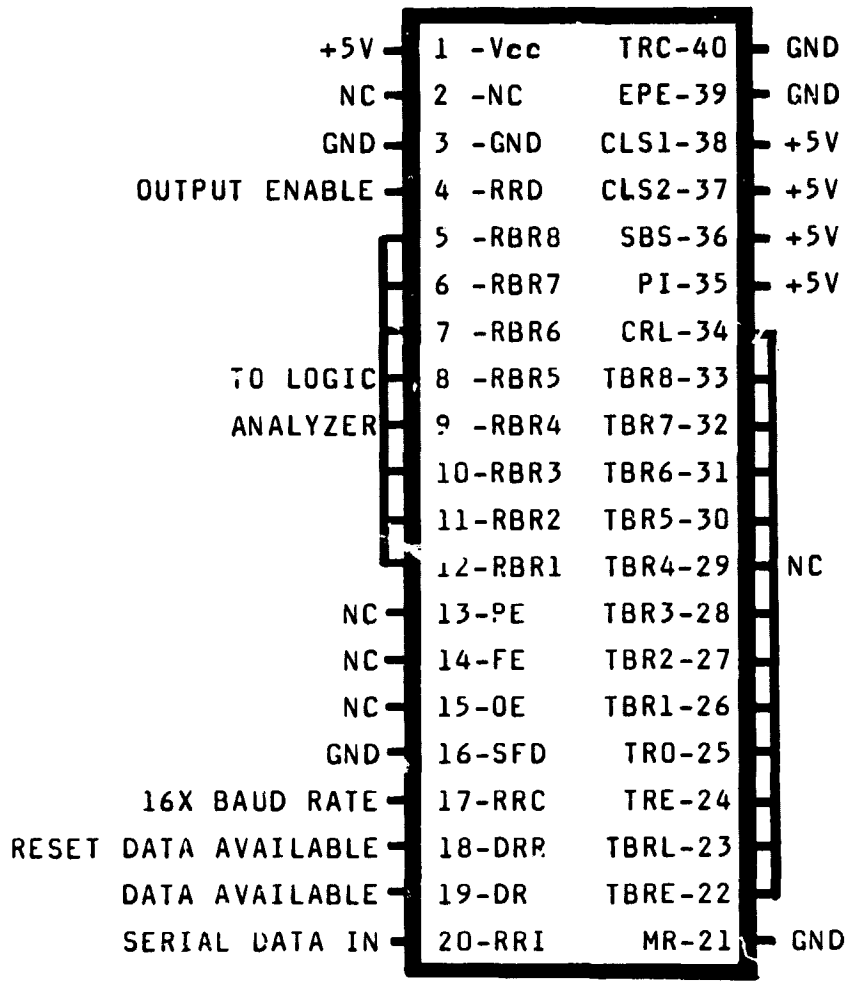
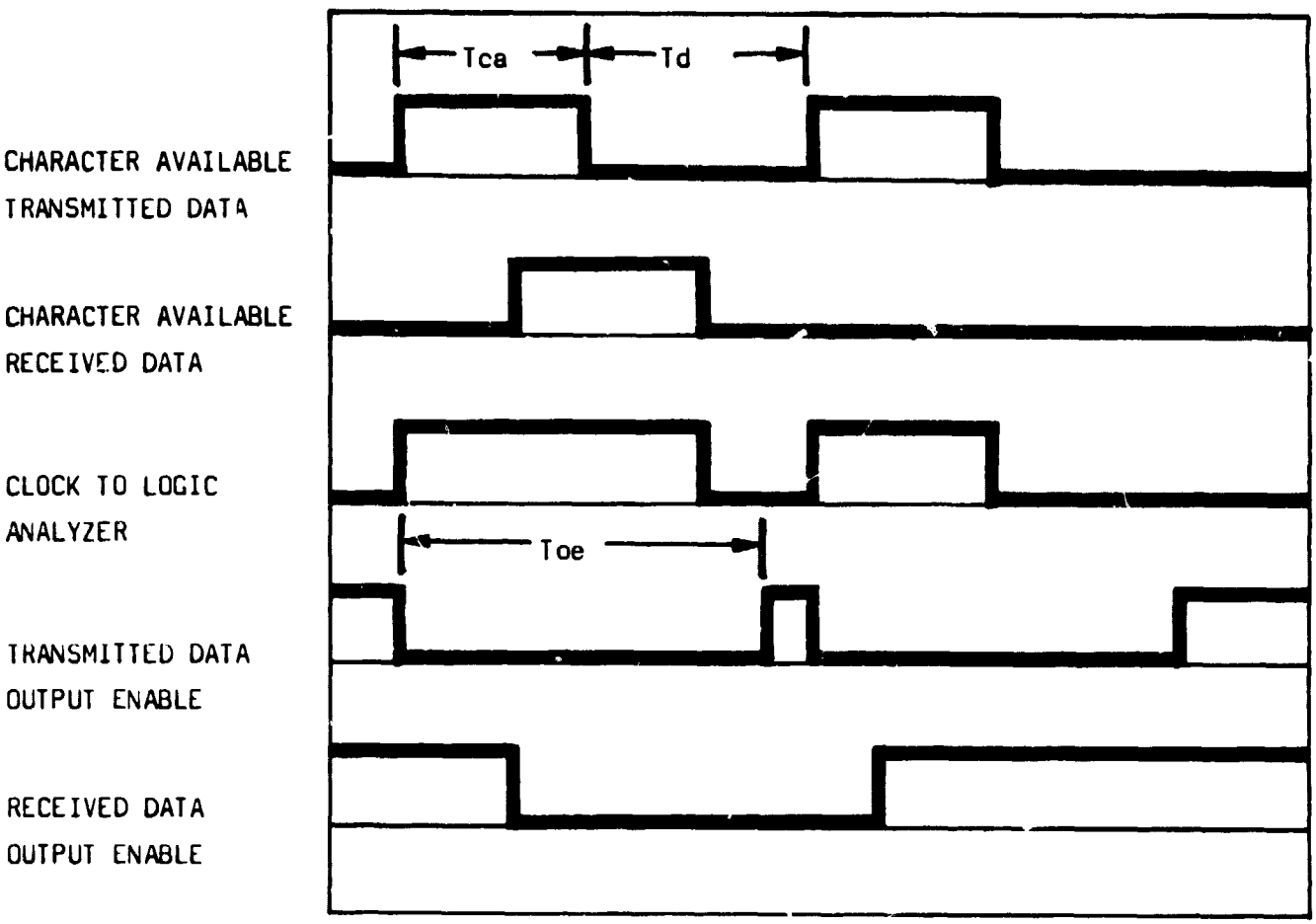


Figure 6. Intersil 6402 UAR/T Pinouts and Connections.



Tca = 0.5 ms. Length of character available pulse.
Td = 0.6 ms. Minimum delay time between characters at 9600 baud.
Toe = 1.0 ms. Duration of tri-state output enable.

Logic analyzer triggers on negative edge of clock pulse.

Figure 7. Timing Diagram.

III. OPERATING THE ASCII ANALYZER

1. Theory of Operation

To use the ASCII analyzer, the HP-1602A must be configured for positive logic, negative edge clock pulse trigger, and 16-bit word length. The data available pulse from either or both UAR/Ts serves as the clock for the logic analyzer. Whenever a character is received by a UAR/T, the data available pulse goes high and the tri-state outputs are enabled. When the data available pulse goes low after 0.5 milliseconds, the character is received by the logic analyzer (negative edge trigger), and the UAR/T is ready for another character.

2. Usage Example

The ASCII analyzer is connected directly into the RS-232 data lines with the cables and connectors provided. The set-up is complete when the HP-1602A has been configured as outlined above and the correct baud rate is selected with the DIP switch. The logic analyzer can trace in a "don't care" condition where the first 64 characters will be stored or one can trace for a specific character. The RS-232 transmit line characters will appear as the low-order eight bits of the sixteen-bit logic analyzer word. The high-order eight bits are the RS-232 receive characters. The following are some logic analyzer displays and their meaning:

10 FF31 FF35
These are the tenth and eleventh stored words. Only RS-232 transmit characters are displayed. (ASCII 1 and 5)

0 FF38 30FF
The trigger word was FF38. Notice that the second word is a RS-232 receive character.

62 3520 372F
These are the last two words in the logic analyzer storage. This is a full duplex condition, both lines are active at the same time.

Many times when an irregular source of serial data is used, the logic analyzer will indicate a "no clock" error. This is because the data available pulses are not occurring at regular intervals. Even if the logic analyzer indicates a clock error, the data is still being stored properly.

IV. CONCLUSION

The ASCII analyzer described in this paper has been designed and built to aid in the debugging of serial I/O devices present in many microprocessor systems. The unit has been tested in various serial transmission modes and with different baud rates. The ASCII analyzer has been designed to interface directly to the HP-1602A logic state analyzer. The simple design would be easy to convert for use with other logic analyzers. All of the integrated circuits used in this design are inexpensive and easily obtainable. The appendix lists the components used to build the ASCII analyzer.

V. REFERENCES

[1] Lancaster, Don, "TV Typewriter Cookbook", Howard W. Sams & Co., Indianapolis, Ind., 1976.

[2] Lancaster, Don, "CMOS Cookbook", Howard W. Sams & Co., Indianapolis, Ind., 1977.

[3] Hewlett-Packard Co., "Model 1602A Logic State Analyzer", Operating and Service Manual, Colorado Springs, Col., 1978.

VI. APPENDIX

ASCII ANALYZER COMPONENT LIST

2	Intersil 6402 UAR/Ts
1	1489 quad line receiver
1	4049 CMOS inverting hex buffer
1	4528 CMOS dual monostable
1	4071 CMOS quad OR gate
1	4060 CMOS binary counter
1	2.4576 MHz crystal oscillator
4	.01 microfarad capacitors
2	100K ohm resistors
2	330K ohm resistors
2	1N914 diodes
1	8 position DIP switch
1	RS-232 ribbon cable
1	Plastic case
1	Circuit board
	appropriate sockets and mounting hardware