NASA CR 168041
WESDL-82-07E

Kilovolt DC Solid State Remote Power Controller Development

FINAL REPORT
OCTOBER 1982

PREPARED BY:

J. T. MITCHELL

PREPARED FOR:

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
NASA-LEWIS RESEARCH CENTER
CLEVELAND, OHIO 44135
CONTRACT NAS3-22646

WESTINGHOUSE ELECTRIC CORPORATION
ELECTRICAL SYSTEMS DIVISION
LIMA, OHIO 45802

FOREWORD

The work described in this report was performed by the Electrical Systems Division of Westinghouse Electric Corporation in Lima, Ohio. The work was performed under Contract Number NAS3-22646 with the National Aeronautics and Space Administration (NASA). The project was managed by Mr. John Sturman of the Electric Propulsion and Space Experiments Branch, NASA-Lewis Research Center in Cleveland, Ohio.

The bipolar development was done by Mr. J. Marshall; power MOSFET development was conducted by the author with the assistance of Mr. K. Jones of Westinghouse ESD. Mr. P. Hower of the Westinghouse R&D Center in Pittsburgh, Pennsylvania furnished the high voltage bipolar switching transistors.

I, II

TABLE OF CONTENTS

TABLE OF CONTENTS

(Continued)

TABLE OF CONTENTS

(Continued)

LIST OF FIGURES

LIST OF FIGURES

(Continued)

LIST OF FIGURES

(Continued)

LIST OF TABLES

SECTION I

SUMMARY

1.1 Project Synopsis

This report summarizes the experience gained in developing and applying solid state power controller (SSPC) technology at high voltage DC (HVDC) potentials and power levels of up to 25 kilowatts. This program extended from September, 1980 through April, 1982 under the direction of NASA-Lewis Research Center on Contract Number NAS3-22646, as amended on April 21, 1981. This program compliments the work conducted on Contract Number NAS3-21755 by adding high voltage power MOSFET switching development. The program consisted of seven tasks which are summarized as follows.

Task I: Preliminary analysis focused on the HVDC switching devices, power switching concepts, drive circuits, and very fast acting overcurrent protection circuits. The best available HV bipolar switching transistors were chosen and fast acting tripping circuits were considered.

Task II: RPC breadboard design and fabrication resulted in the design and building of a 25A bipolar breadboard with the Darlington connected switching transistors having $V_{CEO(SUS)}$ = 1,000 volts.

Task III: Testing and evaluation of breadboard included fault testing at 900 volts. Fault testing consisted of turning on into a short circuit and carrying rated current immediately before the short circuit.

1.1 Project Synopsis (Continued)

Task IV: Development of a bipolar transistor packaged breadboard design included schematic, parts list, drawings, specification, and instructions. A cost estimate was included as part of this task.

Task V: Design of power MOSFET RPC was accomplished and a breadboard fabricated. The 25A breadboard included banks of MOSFETS operated in series. Each bank consisted of ten 500V MOSFETS connected in parallel to give a R_{DS-on} of .06 ohm. The 20 TO-3 transistors gave three volts drop at 25 amperes. Testing included turning on into a short circuit with 500V source and carrying rated current immediately before the short circuit. The current reached 2.5 PU and 2 PU, respectively.

Task VI: Delivery and final presentation has been partially completed. The bipolar and MOSFET breadboards have been shipped as well as the packaged breadboard design package under Task V.

Task VII: Reporting requirements will be complete with the issuance of this report.

1.2 Accomplishments

The following is a list of significant program accomplishments.

1. Circuit technology has been developed and demonstrated that establishes the technical feasibility of HVDC bipolar transistor and MOSFET SSPCs rated 25 amperes for applications up to 1,000 volts.
2. Fast switching bipolar circuit has been developed that will clear a fault within three microseconds.

1.2 Accomplishments (Continued)

3. A fast switching MOSFET circuit has been developed that will clear a fault within 1.5 microseconds. The peak "let-through" current can be controlled to a very safe value. It is suitable for hybrid fabrication for minimum weight and size.
4. Two innovations have been developed for improved operation of the overcurrent protection circuit. A front end that is responsive to rapidly rising (e.g., fault) current and the sensitivity threshold set by the steady state current allow for very fast fault clearing. This is a major advancement of the technology.
5. Gate drive circuits for series connected banks of power MOSFETS - these were trimmed to obtain tracking of the two banks during switching within less than 20 nanoseconds. This is absolutely necessary if fast switching is required. They must be matched within 5% of the switch speed to prevent one bank causing undue voltage stress on the other.
6. Excellent operating efficiency in excess of 99.66% can be obtained when higher voltage devices are available.
7. The developed circuits are compatible with higher voltage transistors being developed.

SECTION II

INTRODUCTION

2.1 Background

Large power systems needed on future space stations will need high voltage DC switchgear in the multi-kilowatt range. Steady progress has been made over the last few years in the development of solid state power controllers. More recent developments include a 200-400 VDC, 50A SSPC with parallel transistors for the switching element and a 1,000 VDC, 25A device using a SCR for the switching element (NASA CR-165413). Additionally, AC SSPCs have been developed for 440 volts and 100 amperes. Hybrid techniques have been utilized to package 28 VDC at 20 amperes, 120 VDC at 30 amperes, (NASA CR-135216) and both 115 volts and 230 VAC at 400 Hz with various current ratings.

In addition to load switching, overload protection, status indication, and remotely controllable and resettable SSPCs possess the following advantages.

1. No contact bounce or wear and no arcing.
2. Precise open and close times.
3. Controlled current transients.
4. Consistent, repeatable overload protection over the temperature range.
5. High vibration and shock immunity.

These advantages allow SSPCs to be used in a wide range of applications. In space applications where weight and volume are very important, the ability to be packaged by hybrid methods can become a very important advantage.

2.2 Objectives

The objectives of this program are to determine the feasibility of KVDC switchgear capable of controlling 25 kilowatts of electrical power and having the potential of being fabricated into a minimum weight and volume. Analytical study, experimental analysis, and breadboard evaluation were to be used to develop and demonstrate switchgear concepts feasibility. Very fast switching circuits are to be used. The peak let-through current is to be kept to a minimum during a fault.

Eight months after the start of this program, power MOSFETS became available with a 500 V_{DS} rating and 0.6 R_{DS-on}. Since these are much easier to package by hybrid techniques than bipolar power transistors, the program was modified to include one breadboard with a bipolar power switch and one with a MOSFET power switch. Siemens list a 1,000V power MOSFET in their catalogue, but they are not yet available in this country. It is expected that 1,000V power MOSFETS will be available from multiple US sources by 1985. It is practical to parallel 20 power chips. Both breadboards are to be designed such that the new transistors can be substituted directly for the lower voltage devices with only minor circuit changes.

2.3 Outline of Tasks

To accomplish the technical objectives, the program was divided into five tasks. Tasks IV and V were modified to delete building of packaged breadboards and add the power MOSFET breadboard.

- Task I - Preliminary Analysis
- Task II - RPC Breadboard Design and Fabrication
- Task III - Testing and Evaluation of Breadboard
- Task IV - Development of Bipolar Transistor Packaged Breadboard Design
- Task V - Design of Power MOSFET RPC

2.4 Specification for HVDC Switchgear

• Rated Operating Voltage	400 to 1,000 VDC
• Maximum Surge Voltage	1,100 VDC
• Rated Output Current	25 Amps
• Load Current, Minimum	0 at Rated Voltage
• Control Power Source	28 ± 7 VDC
• Control Voltage	T^2L Compatible
• ON State Control Signal	Logic 1 (High)
• Overload Trip Indication	T^2L Signal - High after trip, resetting when input is commanded OFF.
• Status Indication	T^2L Signal - High while switch is closed.
• Turn-On and Turn-Off Times	.01 to 1.0 Millisecond
• Rise and Fall Times	10 Microseconds Minimum
• Voltage Drop at Rated Load, Maximum	2.0 VDC
• Power Dissipation Off, Maximum	5 Watts
• Efficiency at 20 to 100% Rated Load Current	Equal to or Greater Than 99.5% (Including Control Power)

SECTION III

PRELIMINARY ANALYSIS

(TASK I)

3.1 Task Objectives

1. Investigate and analyze approaches in power switching technology for one KVDC SSPC. The design selected should be such that transistors meeting the full voltage specification could be substituted in the RPC when they become available with, ideally, no circuit changes.
2. Assume power sources for analysis and circuit simulation will be a "hard" DC bus with a current capability of at least ten times the continuous rated switch current. Control of the transient currents when the RPC output is short circuited is a major goal.
3. Conduct survey of available high voltage power transistors and their characteristics to identify the most suitable single device or parallel combination of devices for use as the main switching element in the RPC.
4. Choose circuitry that has the potential of being fabricated into a minimum weight and volume RPC using .07 pound per watt for the trade-off factor. Techniques adaptable to hybrid circuit applications shall be given primary emphasis.

3.2 Survey of HV Bipolar Transistors

Much of the work in the preliminary analysis centers on consideration of the transistor chosen for the power switch element. Inquiries made into existence or availability of 1,000V transistors provided no positive results. A thorough transistor study was conducted by Westinghouse engineers as a part of switchgear design analysis for high voltage DC switchgear development for NASA-Lewis, Contract Number NAS3-21755. This study was used as a starting point in investigating the high voltage transistor market. Manufacturers listed in the report were contacted and indicated substantially no change in voltage ratings although some reported higher voltage rating in individual production runs. For example, in the case of the Power Tech PT3526 with a V_{CEO} of 600V, some transistors test out at 700V.

Even though no 1,000V rating transistors were found, manufacturers are slowly pushing the ratings upward. Motorola expects to offer a 20A, 850V device and Toshiba expects to release a 100A, 900V unit. Within the next five years, there should be several bipolar transistors on the market in the one kilovolt range.

Westinghouse Research and Development Laboratories at Pittsburgh, Pennsylvania is developing high voltage/high current NPN transistors under a NASA contract. These appear to be by far the best choice for this application since the $V_{CEO(SUS)}$ is approximately 1,000 volts and the V_{CBO} is greater than 1,500 volts. A single device (with a Darlington driver) is adequate for current and gain.

3.3 Discussion of Switching Speed

It is well known that in opening an inductive circuit, a high Ldi/dt voltage appears across the switch. The same thing occurs across a solid state switch and it can easily destroy the switching device from voltage breakdown. The higher the current is allowed to go before opening the circuit, the higher this voltage will become (assuming the same switch speed). There are three basic ways of handling this problem. The most obvious way is to add enough inductance in the power controller to slow the rate of rise of current and use slow switch speeds. This method works, but the inductors get much too large for airborne or space applications. A second method is to select switches and drive circuits so that the switching device will only pass so much current and then saturate, in the case of a MOSFET; of pullout of saturation, in the case of a bipolar switch. This method was used on the 400V, 50A breadboard on a previous contract. The third approach is to use an extremely fast switch and begin the trip-off as close as possible to one per unit current. All methods have advantages and disadvantages. No one method is clearly the best in all cases. The third method was chosen for this project since it had not previously been explored because slow response of previous circuits made it impractical.

3.4 Circuit Discussion (Figures 3-1, 3-2)

Previous development took the approach of slow turn-on and turn-off by limiting the base drive current so the power transistor will pull out of saturation and control the maximum load current. For example, during turning on into a short circuit, it took 40 microseconds to reach 2.6 PU current, and more than 20 microseconds for the current to be returned to substantially zero. This slow operation requires a very high safe operating area (SOA) on the power switching transistor. For this investigation, the opposite approach was taken - very fast operating circuits were to be developed to expand the technology. To obtain fast turn-off, two basic circuits are needed: (1) a fast acting base drive circuit, and (2) a fast acting overcurrent protection circuit.

The fast acting base drive circuit chosen is shown in figure 3-1. During normal operation, C106 becomes charged because of the few volts drop across CR111, CR112, CR113, and R114. For a fast turn-off, SCR2 is fired which allows C106 to discharge down through SCR2, R116, and R115. This applies a reverse potential across Q101 and Q102 emitter-base junctions which clears the junction of carriers for a fast turn-off. The three diodes are included in series with R114 in order to obtain a minimum voltage of three diode drops to work against the drop in SCR2 and have sufficient voltage left to clear the carriers in Q101 and Q102.

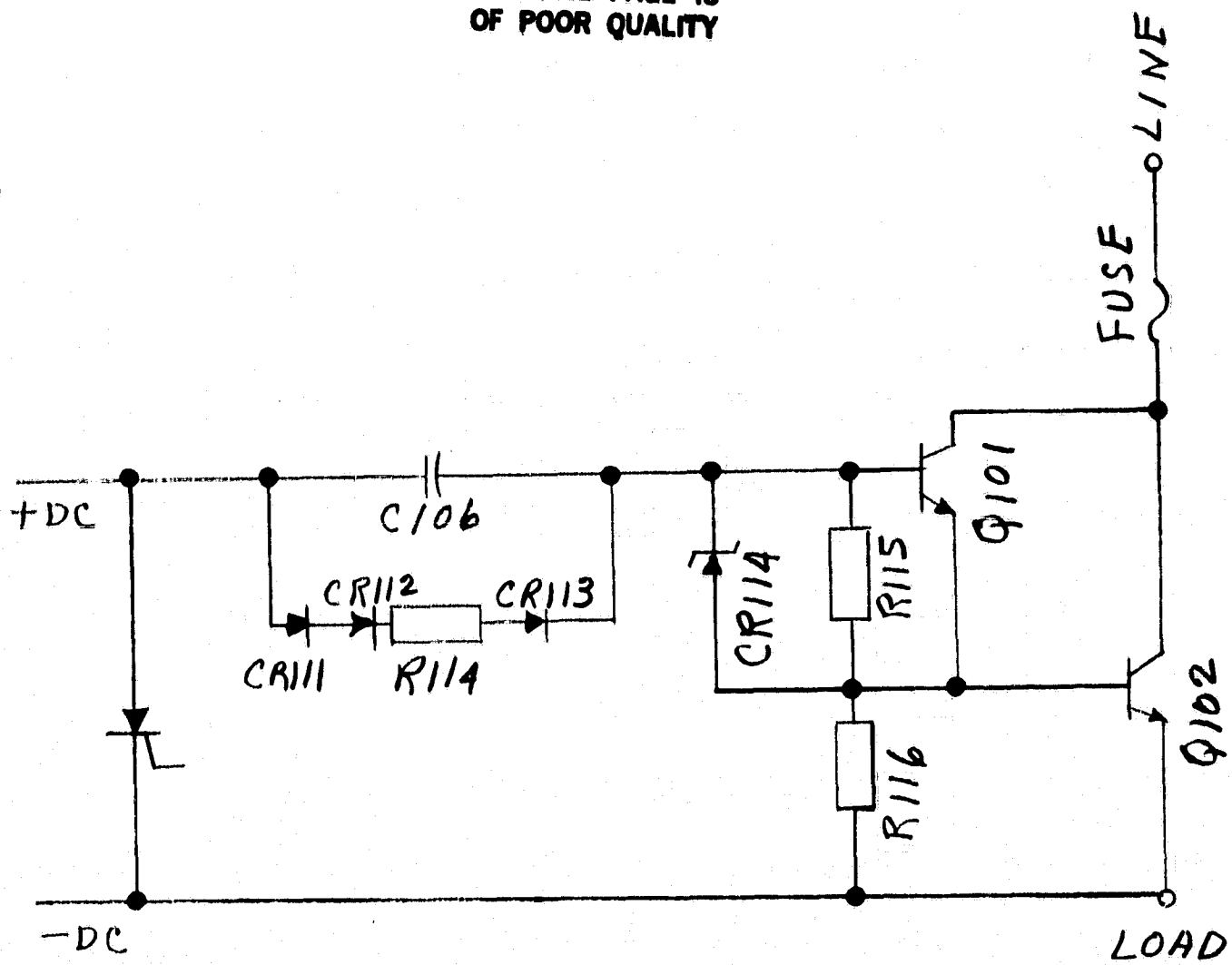


Figure 3-1 - Fast Acting Base Drive Circuit

3.4 Circuit Discussion (Figures 3-1, 3-2) (Continued)

A fast acting overcurrent protection circuit is shown in figure 3-2. Z101 and Z102 are connected in a normal inverting threshold/integrator trip circuit. CR110 is a 1.22V precision reference which along with R110 and R112 sets the threshold at which Z101 responds and causes the output at pin 6 to go high which in turn charges capacitors C105 through R109. When the voltage at pin 6 of Z101 is greater than CR110 reference voltage, Z102 comparator output at pin 2 goes positive which fires SCR1 through CR105. This causes a "slow" trip response from the base drive circuit since C106 must discharge through CR106 in addition to SCR1. This gives less reverse voltage across the emitter-base junctions of Q101 and Q102.

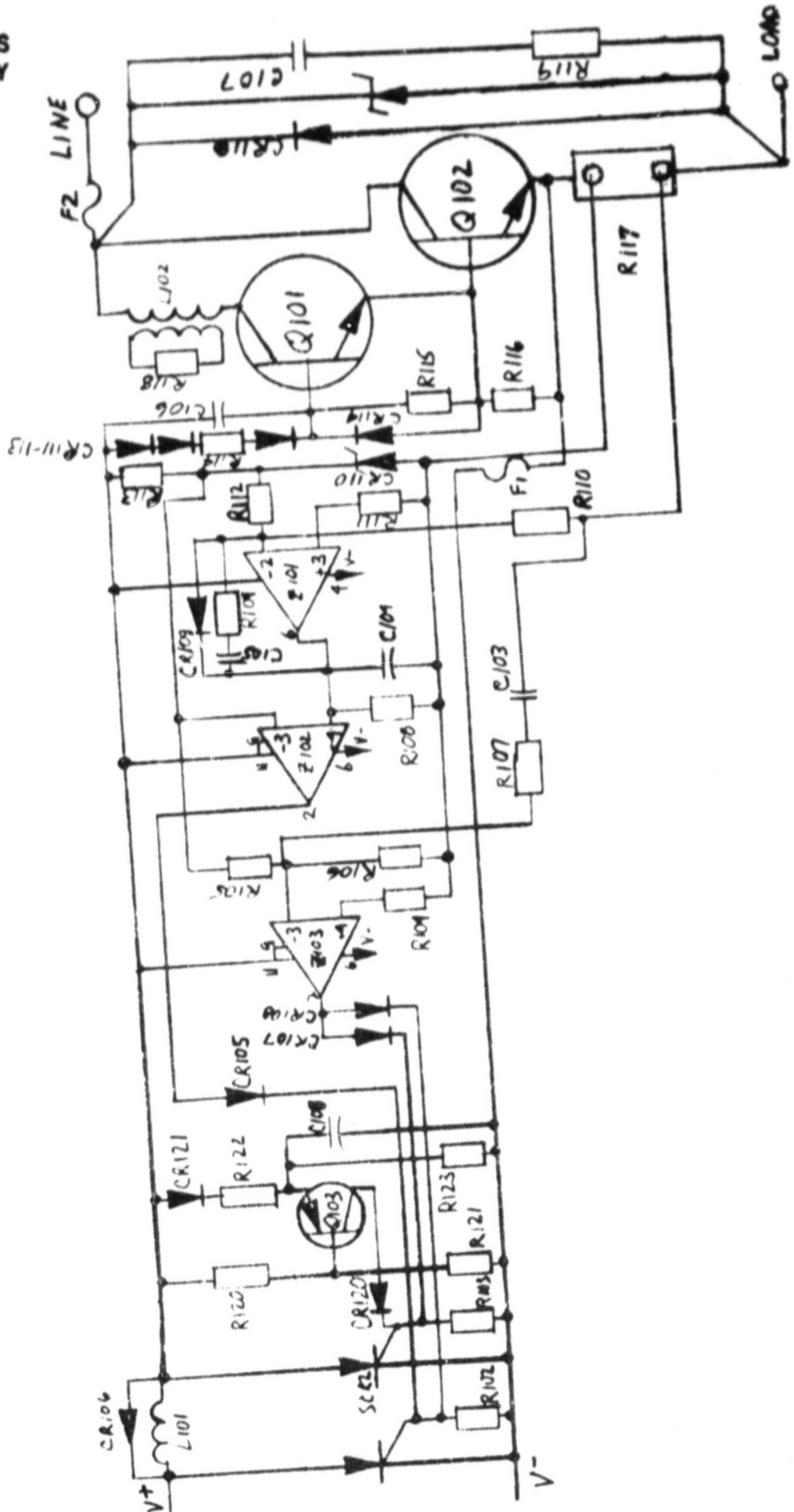


Figure 3-2 - Fast Acting Overcurrent Protection Circuit

3.4 Circuit Discussion (Figures 3-1, 3-2) (Continued)

Pin 6 of Z101 can reach the reference voltage of 1.22 volts by allowing C105 to charge to that voltage (integrating the current) which results in an inverse current/time relationship. If the load current reached 3 PU, there would tend to be a highly negative voltage at pin 2 of Z101 and its output would be driven suddenly positive and the resulting voltage drop would appear across R109 since C105 would be a short circuit. This would allow pin 6 to go above 1.22 volts without waiting for capacitor C105 to charge. An "instant" trip condition could result. R109 is chosen for this to occur at 3 PU. Z101 and Z102 are relatively slow devices and this instant trip would take several microseconds before the output of Z101 went positive. If this occurred as the result of a short circuit, the current could well be above 5 PU before a trip was initiated. No action would begin until the current reached 3 PU and in the few microseconds response time of Z101 and Z102, the current could be much higher. Therefore, this circuit is not adequate for short circuit protection without current limiting. It is adequate for light overloads.

The current sensing shunt R117 gives 50 millivolts drop at 25A (1 PU) load. This voltage does not normally appear at pin 3 of Z103 because of capacitor C103. However, with a rapidly rising current (e.g., a steep front of current from a short circuit), C103 appears as an effective short circuit, and half of the negative shunt voltage appears at pin 3 of Z103 (R106 and R107 are equal and divide the shunt voltage). Pin 3 of Z103 is normally held at +55 millivolts.

3.4 Circuit Discussion (Figures 3-1, 3-2) (Continued)

Therefore, when a steep front of load current reached 2.2 per unit, the net voltage at pin 3 of Z103 would be zero since the shunt voltage of -110 millivolts is divided and exactly neutralizes the +55 millivolts at the inverting terminal. As the steep front increased beyond 2.2 PU, the output of Z103 would go positive and fire SCR1 and SCR2. This would give a "fast" tripping action as previously described. A very fast operational amplifier is chosen for Z103. Tripping action takes less than one microsecond.

The remainder of the circuit consists mainly of power supply and logic follows from the previous development work on Contract Number NAS3-21755.

SECTION IV

RPC BREADBOARD DESIGN AND FABRICATION

(TASK II)

4.1 Task Objectives

1. Based on the results of task I, design a RPC meeting all specifications.
2. Build breadboard.

The circuit of figure 4-1 has the potential of meeting the objectives of the RPC. Based on previous power controller experience and recent precontract research, no major problems are anticipated in such areas as power switch capabilities, overcurrent protection, and efficiency.

4.2 Circuit Description (Figure 4-1)

The circuit shown in figure 4-1 is the final circuit. Certain changes were made during development testing. These changes are indicated in section V. The more important changes include the addition of the reset lockout, speedup of normal turn-off (addition of Q103), and improvements in the snubber circuit. A brief description of operation of each circuit function follows.

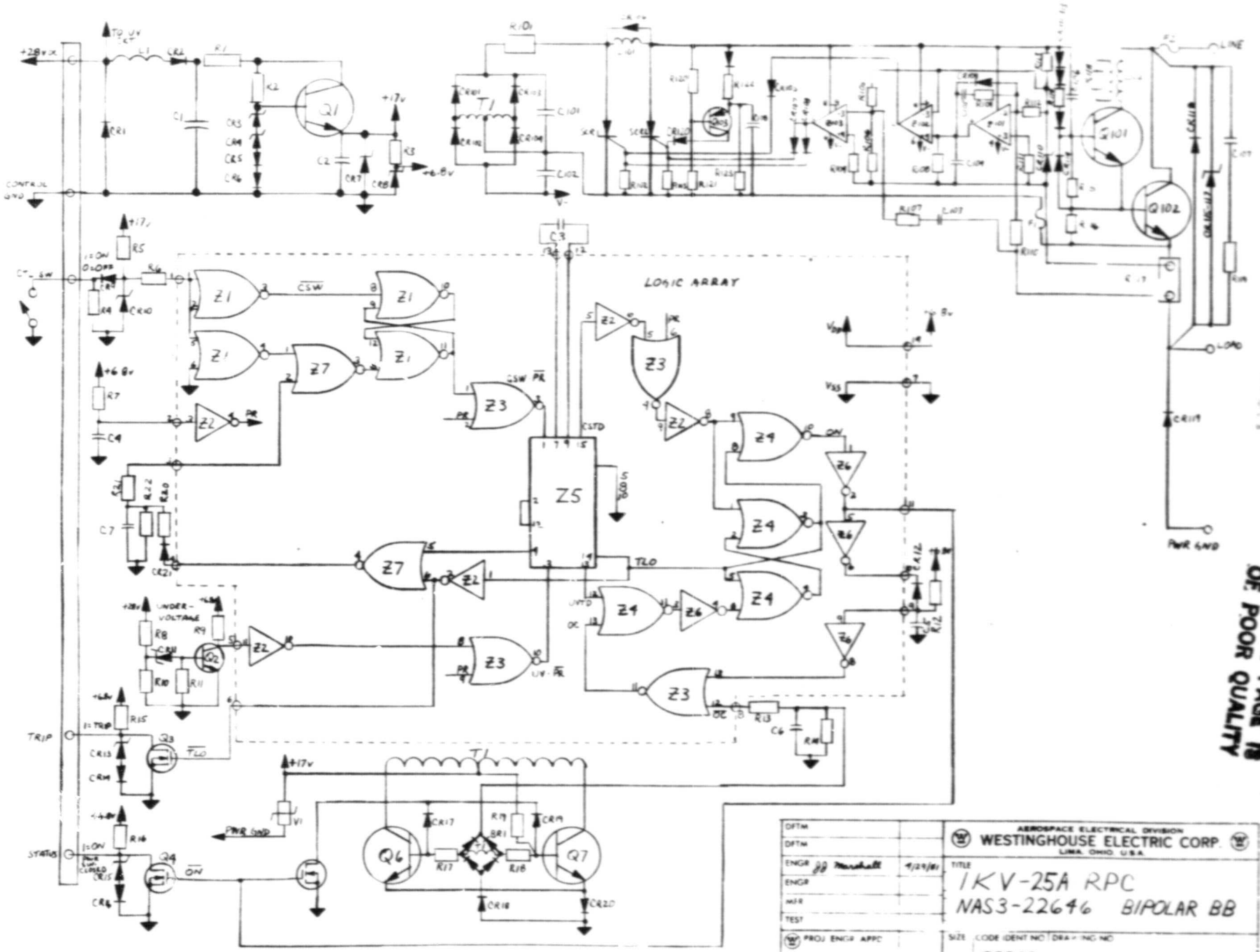


Figure 4-1 - 1 KV Bipolar SSPC Diagram

Table 4-1

1 KV/25A Bipolar SSPC Parts List

Logic Section

BR1	Bridge FSA2705M
C1-A, B, C	Capacitor 86 MFD Tantalum
C2	Capacitor 2.2 MFD Tantalum
C3	Capacitor 4700 PF Tantalum
C4, 5	Capacitor .068 MFD Ceramic
C6	Capacitor 680 PF Ceramic
CR1, 2	Diode IN4002
CR3, 4, 11	Zener Diode 8.2V
CR5, 6, 9, 12, 14, 16, 17, 18, 19	Diode IN4148
CR7	Zener Diode 22V
CR8	Zener Diode 6.8V
CR10	Zener Diode 5.6V
CR13, 15	Zener Diode 4.7V
CR20	Diode IN5416
L1*	Inductor 2.4 μH
Q1	Transistor 2N3773
Q2	Transistor 2N2219A
Q3, 4, 5	FET 2N6660
Q6, 7	Transistor SDT4905
R1	Resistor 5 Ohm
R2	Resistor 1K
R3, 5	Resistor 2K
R4, 15, 16	Resistor 5.1K

Table 4-1

1 KV/25A Bipolar SSPC Parts List

(Continued)

Logic Section

R6	Resistor 49.9K Metal Film
R7	Resistor 499K Metal Film
R8, 10	Resistor 20K Metal Film
R9, 11	Resistor 47K
R12, 13, 14	Resistor 51K
R17, 18	Resistor 125 Ohm PTC
R19	Resistor 24K
T1*	Transformer PR1 60T Bifilar, SEC 34T, SEC 34T Bifilar
V1	Varistor V24ZA4
Z1, 3, 4	Quad 2 Input NOR MC14001
Z2, 6	Hex Inverter MC14069
Z5	Hex Bounce Eliminator MC14490
C101, 106	Capacitor 10 MFD Tantalum
C102, 105	Capacitor 1 MFD Tantalum
C103	Capacitor 6800 PF Ceramic
C104	Capacitor .1 MFD Tantalum
CR101, 102, 103, 104, 105, 107, 108	Diode VSK130
CR106, 114	Diode IN5416
CR109	Diode IN4148
CR110	Zener Diode Reference 1.23V
CR111, 112, 113	Diode IN4001

Table 4-1

1 KV/25A Bipolar SSPC Parts List

(Continued)

Logic Section

CR115	Zener Diode 200V
CR116, 117	Zener Diode 400V
CR118	A177PE
CR119	A170RPE
F1	Fuse 2A
F2	Fuse 35A
L101*	Inductor .35 Millihenry
L102*	Inductor 50 μH
Q101, 102	Transistor Westinghouse R&D HV Development
R101	Resistor 1 Ohm
R102, 103	Resistor 510 Ohm
R104, 106, 107	Resistor 4.99K Metal Film
R105, 109	Resistor 105K Metal Film
R108	Resistor 910K
R110	Resistor 12.7K Metal Film
R111	Resistor 12K
R112	Resistor 255K Metal Film
R113	Resistor 6.2K
R114	Resistor 6 Ohm
R115	Resistor 30 Ohm
R116	Resistor 3 Ohm

Table 4-1

1 KV/25A Bipolar SSPC Parts List

(Continued)

Logic Section

R117	Shunt 50 MV/25A
SCR1, 2	Silicon Controller Rectifier
Z101	OP Amp CA3160
Z102, 103	Comparator LM111

* L1, C1 relationship should have the relationship:

$$L1 = \frac{6.33 \times 10^{-7}}{C1} \text{ with C1} \quad 50 \text{ MFD}$$

L1 carries approximately .6A.

T1 core is Magnetics, Inc. 50176-2A.

PR1 60T bifilar #28 wire.

Section #1 34T #28 wire.

Dipped and baked twice (varnish).

Taped with Kapton tape.

Section #2 34T bifilar #26 Teflon insulated wire.

L101 inductor T/T 19146 .35 millihenry.

L102 inductor core HF-106125-2. (Arnold)

18 turns #18 Teflon insulated wire 50 μH.

4.2.1 Power Supply (Figure 4-2)

The purpose of the power supply is to provide regulated DC voltages for the SSPC circuits. The 28 VDC supply voltage is regulated down to about 17 VDC by the CR3-4-5-6 string and Q1, and is maintained for 28 VDC supply variations (±7V). The CR3-4-5-6 diode string provides temperature stability for the regulated voltage. The 6.8V regulated voltage is provided for the CMOS logic devices. CR7 provides protection against a component failure that could cause abnormally high regulated voltages (e.g., Q1 short, T1 secondary-primary short or CR3-4-5-6 open). Filtering is provided by C1 and L1. Reverse voltage protection is provided by CR1.

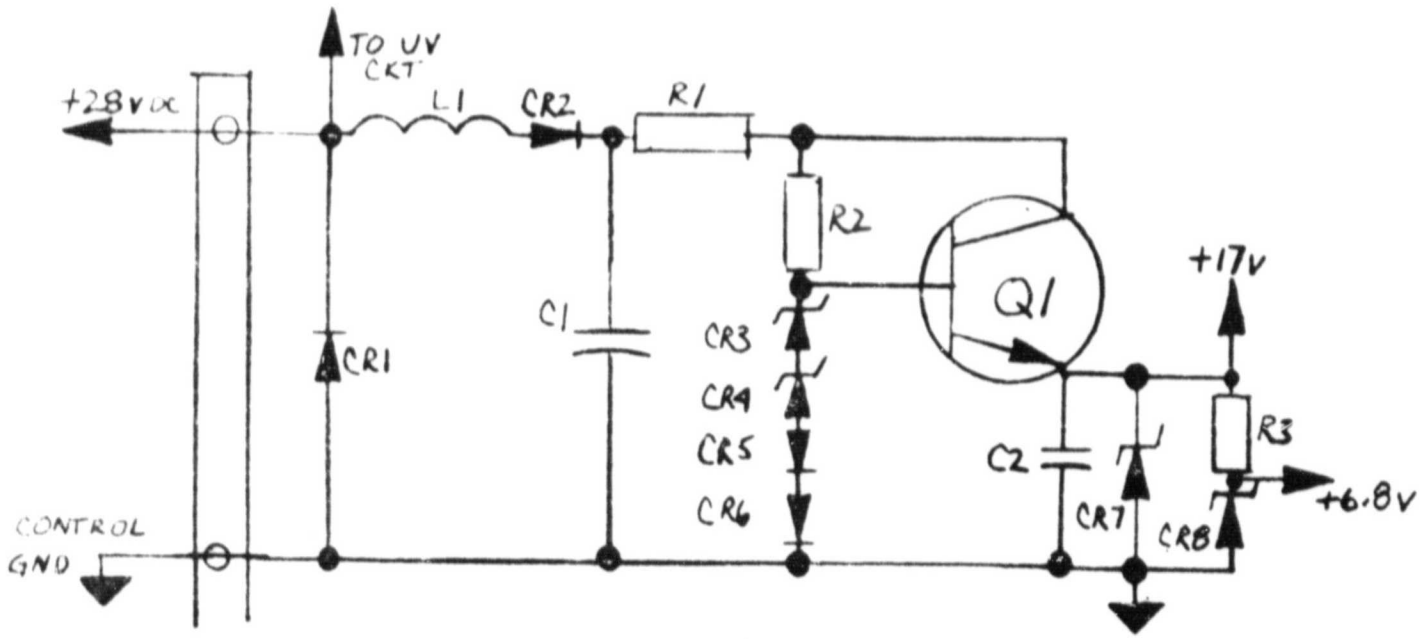


Figure 4-2 - Power Supply Circuit

4.2.2 Power Ready (Figure 4-3)

The purpose of the power ready (PR) function is to initialize the SSPC logic circuitry when 28 VDC power is applied. This is accomplished in the PR circuit by a R-C time delay (R7-C4-Z2) circuit which generates a pulse persisting for about 30 milliseconds when 28 VDC power is applied. This PR signal is utilized to lock out the undervoltage and control switch circuits and reset the control switch time delay and trip lockout circuits.

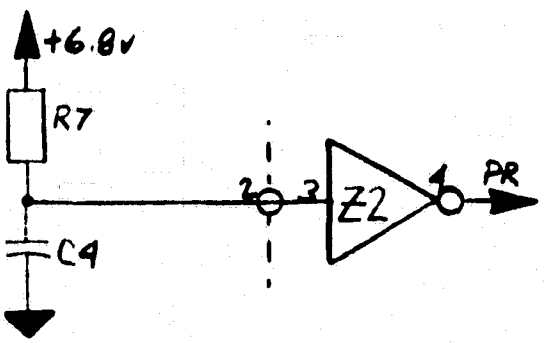


Figure 4-3 - Power Ready Circuit

4.2.3 28 VDC Undervoltage Protection Circuit (Figure 4-4)

The purpose of this circuit is to protect the SSPC in the event the 28 VDC supply voltage becomes excessively low. This protection is necessary because the 28 VDC supply is used to power the drive circuit and when the 28 VDC supply drops below its 21V lower limit, drive to the power switch will be reduced, thereby risking excessive switch voltage drop and power dissipation.

The input to the 28 VDC undervoltage (UV) circuit is the 28 VDC supply voltage, which is applied via R8 and CR11 to the Q2 base. When the 28 VDC supply voltage is above 21 volts, CR11 is broken down so that a base signal is applied to Q2 and Q2 is in the conducting state and its collector voltage is at a low potential. Whenever the 28 VDC drops below the 21V level, depending upon the actual CR11 breakdown voltage, there will be a level below which CR11 and subsequently, Q2, will become nonconductive. When this occurs, the high Q2 collector voltage signal applied to CMOS gates Z2 and Z3 results in the UV trip signal at the output of Z3. The UV trip signal is inhibited at the time 28 VDC power is applied to the SSPC by the power ready signal to preclude UV trip signals at turn-on.

The UV trip signal results in the setting of the trip lockout (TLO) circuit, so that the SSPC will require resetting in order to return to the ON state even though the 28 VDC supply voltage has returned to normal operating limits. This retentive lockout will preclude load cycling in event of a fluctuating 28 VDC supply voltage.

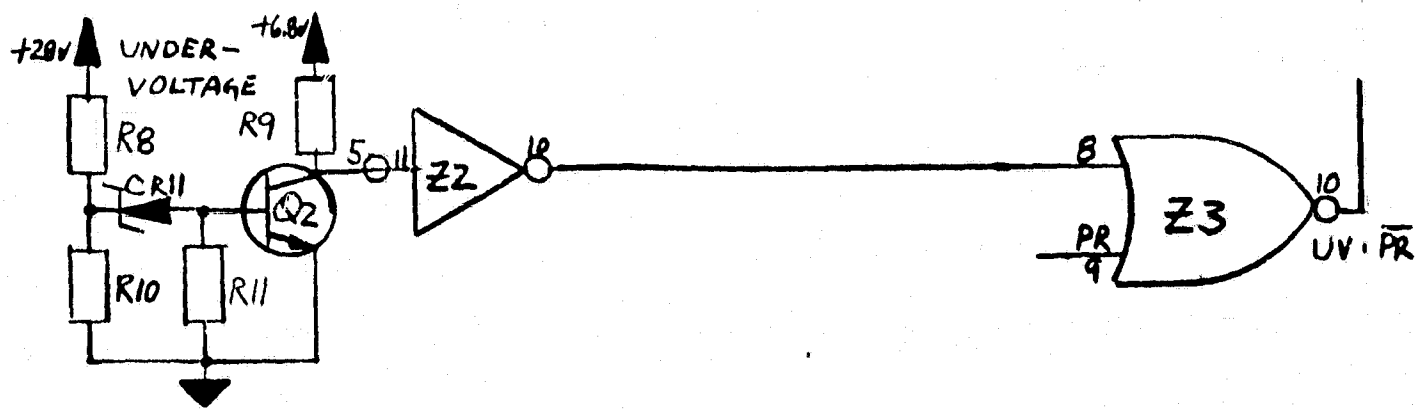


Figure 4-4 - Undervoltage Protection Circuit

4.2.4 Control Switch Logic and Time Delay (Figure 4-5)

The purposes of this circuit are to:

1. interface between the external SSPC OFF/ON control switch or signal; and
2. provide voltage hysteresis and time delay for operation stability.

As shown in the circuit diagram, the external control switch is a grounding device which when closed results in an "0" level signal at the control input and when opened results in a "1" level signal. The circuit is designed to operate with a TTL device in place of the switch. The control input voltage is applied to gates Z1A and Z1B which operate as threshold detectors and to RLOTD (reset lockout time delay) Z1C and Z1D which complete a toggle circuit when RLO = 0. The circuit is designed to operate with a small amount of hysteresis (established by the Z1A and Z1B input connections) and provide a digital logic signal in response to the input voltage level (CSW_{in}) at the control switch terminal. The output signal of Z1D, $\overline{CS}$, is high when the CSW_{in} level is low and low when the CSW_{in} level is high. The $\overline{CS}$ signal is gated with the power ready signal so that the $\overline{CS}$ signal only operates the control switch time delay (CSTD) when the PR signal is absent. The CSTD function is provided by Z5, a CMOS IC which is a digital time delay device of the contact bounce eliminator type. The CSTD period is on the order of seven milliseconds, is a function of C5, and is provided for both turn-on and turn-off.

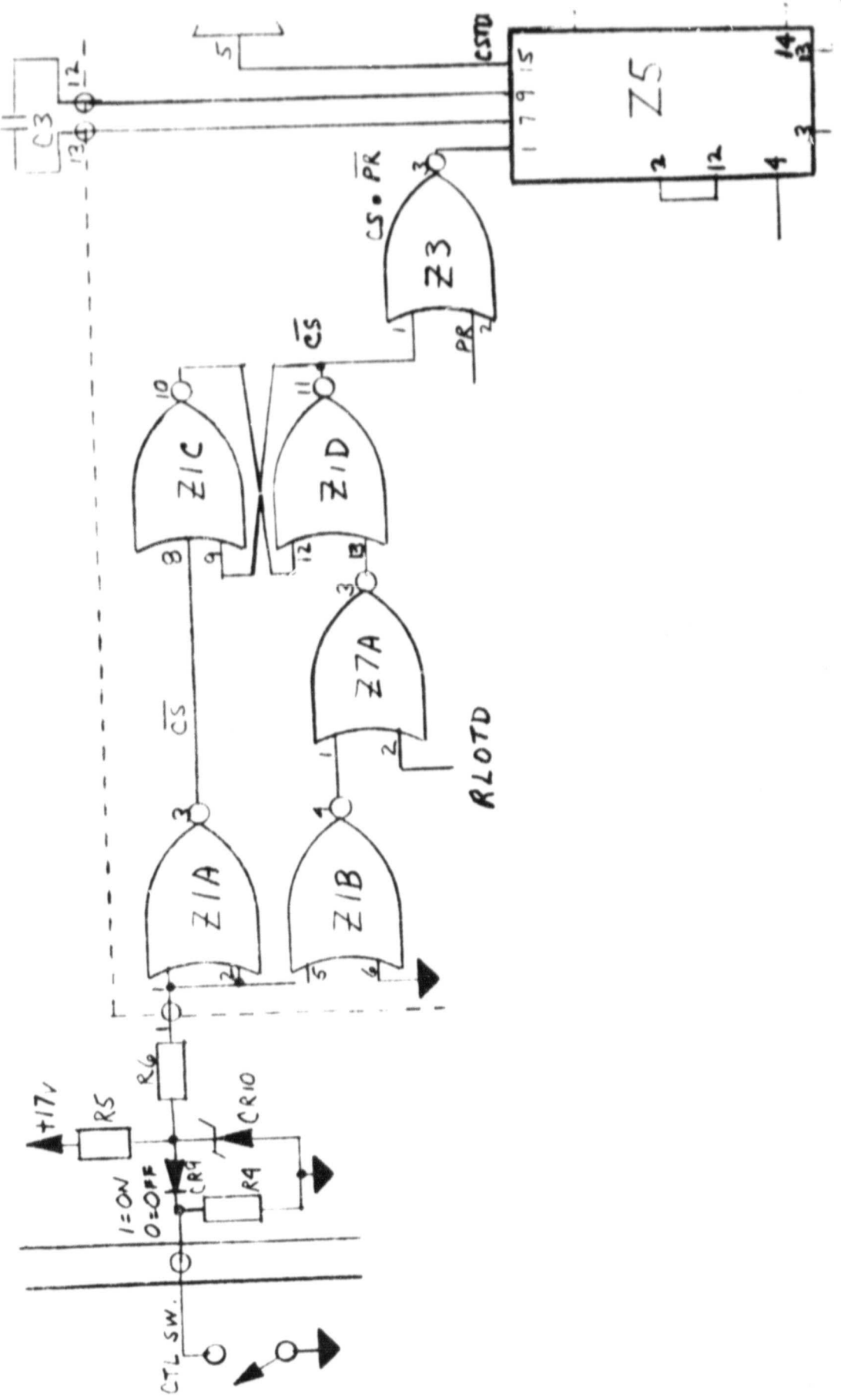


Figure 4-5 - Control Switch Logic and Time Delay

4.2.5 Drive Circuit (Figure 4-6)

The purpose of the drive circuit is to provide amplification and electrical isolation for the logical ON signal which becomes the input drive signal to the power switch. The ON signal occurs when the CSTD signal is present and the PR and TLO signals are absent. The ON signal is amplified by field effect transistor Q5. Operation of the Royer oscillator is controlled by FET Q5. When in the conducting state, this transistor effectively clamps the bases of Q6 and Q7 switching transistors to the control ground to divert base drive current from the transistors. This prevents conduction and prevents the oscillator from functioning. To turn the oscillator on, the gate of Q5 is clamped to control ground by Z6A. This turns Q5 off and allows base drive starting current to flow through R19 and through Q7 emitter-base. This small amount of current causes Q7 to turn on and allow current to flow from the center tap through the right side of the winding and through Q7 collector emitter to control ground. This change in current induces a voltage in all windings of the transformer including the Royer drive winding (shown inside the BR1 bridge rectifier). The induced voltage turns on Q6 and turns Q7 off. Oscillations build up until equilibrium is reached at approximately 3.5 KHz (frequency is proportional to voltage).

The secondary of T1 is full-wave rectified and filtered to give a positive voltage with respect to common and a negative voltage with respect to common. These provide base drive to the power switch and energize the overcurrent protection circuit.

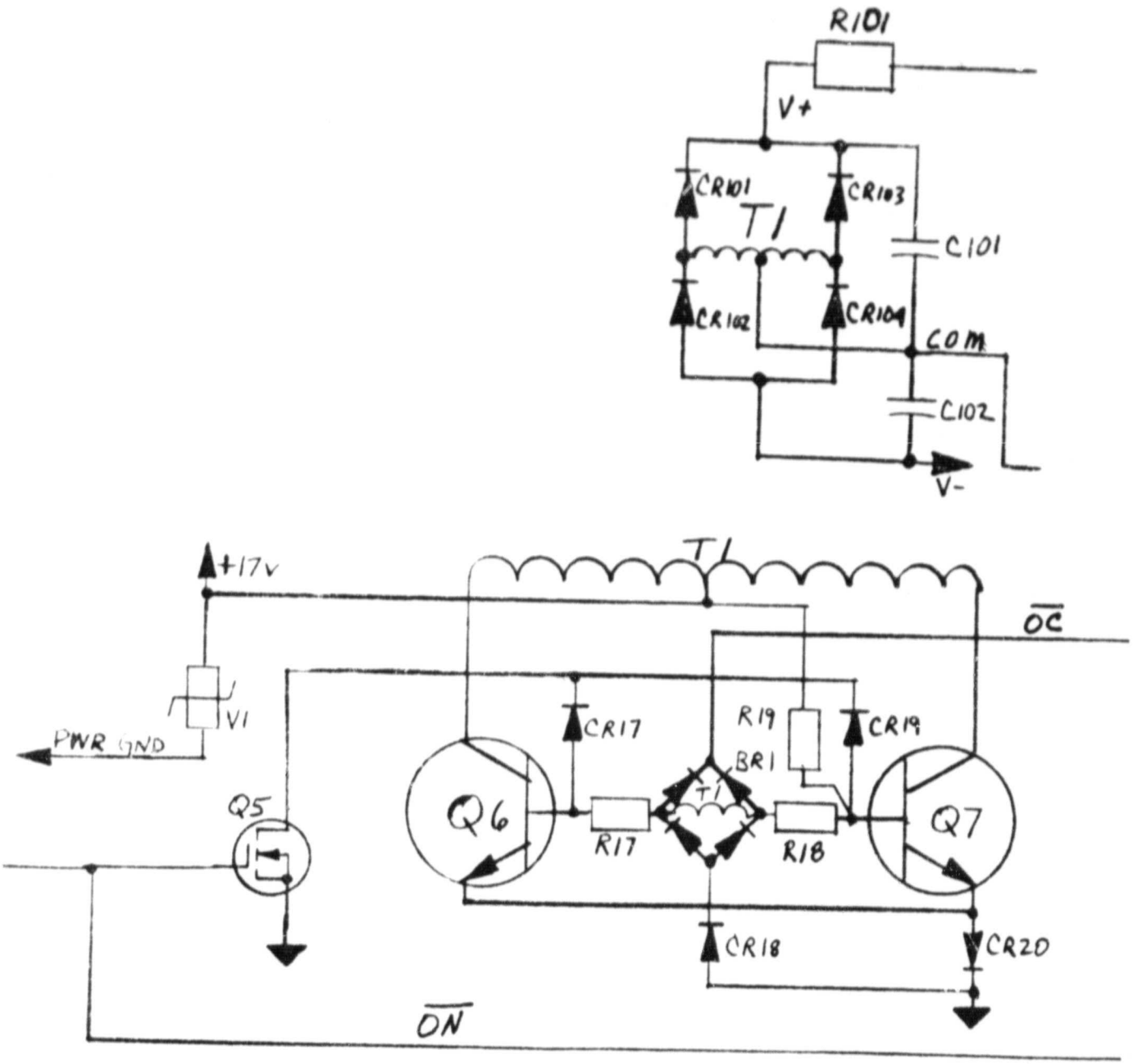


Figure 4-6 - Drive Circuit

4.2.6.2 Trip Lockout and Trip Indication (Figure 4-7)

The trip lockout function is utilized to provide trip-free operation for the prevention of SSPC OFF/ON cycling in the event of an overcurrent (OC) or undervoltage trip-off. The TLO retention is provided by CMOS gates Z4A and Z4B which are connected to form a NOR flip-flop circuit. This flip-flop is reset to the $\overline{\text{TLO}}$ state via gates Z3B and Z2D at initial SSPC energization by the PR signal and after an overcurrent trip-off by changing the control switch from a logical 1 to a logic 0 and back to a logic 1 to interrupt and reapply the $\overline{\text{CSTD}}$ signal via Z2C. The flip-flop is set to the TLO state via gates Z4D and Z6B by the occurrence of either an undervoltage time delay (UVTD) signal or an OC signal. The occurrence of an OC condition is detected by the Z3D NOR gate whose input is the rectified and filtered drive transformer signal, $\overline{\text{OC}}$, that quickly disappears when an OC condition is sensed by the OC protection circuit. The other Z3D input signal is an OFF or $\overline{\text{ON}}$ signal that is time delayed, disappearing at SSPC turn-on to allow for the C6-R14 voltage buildup time.

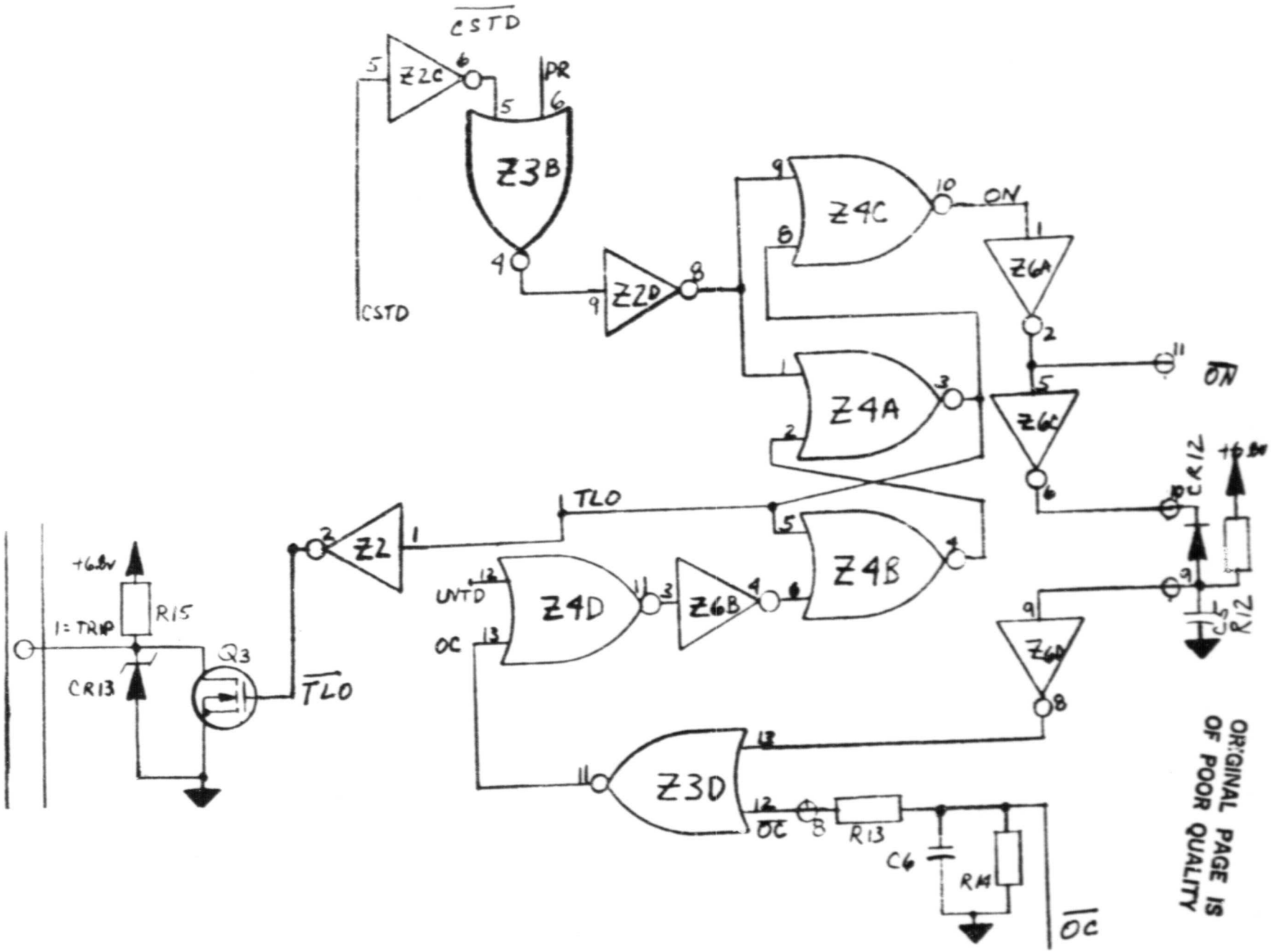


Figure 4-7 - Trip Lockout and Trip Indication

4.2.6 Trip Lockout and Trip Indication (Figure 4-7) (Continued)

The TLO output signals are used to inhibit the power switch drive circuit via gates Z4C and Z6A and to provide a drive signal for the trip lockout indication output transistor, Q3. The trip output signal is TTL compatible with about a five volt active pull-up output (1) signal in the SSPC tripped state due to an overcurrent condition on the HV line or to an undervoltage condition on the 28V bus. It also provides a clamped output (0) signal in the SSPC ON and OFF states. CR13 also provides reversed voltage protection. In conclusion, it should be noted that the TLO circuit can be reset after a fault condition by two means:

1. closing and reopening the control switch with the appropriate waiting time, or
2. removing and reapplying the +28 VDC control power with the appropriate waiting time.

4.2.7 Reset Lockout (Figure 4-8)

The reset lockout function provides thermal protection for the power switch by precluding reclosure after an overcurrent trip-off until an adequate cooling off period has elapsed. For this application, a ten to 20 second period was considered adequate and is provided by this circuit. Whenever an overcurrent trip-off occurs, the occurrence of the TLO signal causes a pulse at the output of Z7B that persists until the time delayed TLO signal appears from the digital time delay device Z5 about 14 milliseconds later. This pulse charges up C7 through CR21 and R20 at a rather fast rate so that C7 reaches virtually the 6.8V supply voltage level. The discharge time of C7 is determined by R21 and R22 and is selected to be relatively long - ten to 20 seconds in this case. While the C7 voltage level remains above the buffer gate Z6E threshold, the reset lockout time signal from gate Z6F will persist. This signal is provided for the control switch logic circuit for the purpose of inhibiting SSPC reclosure as long as the RLOTD persists.

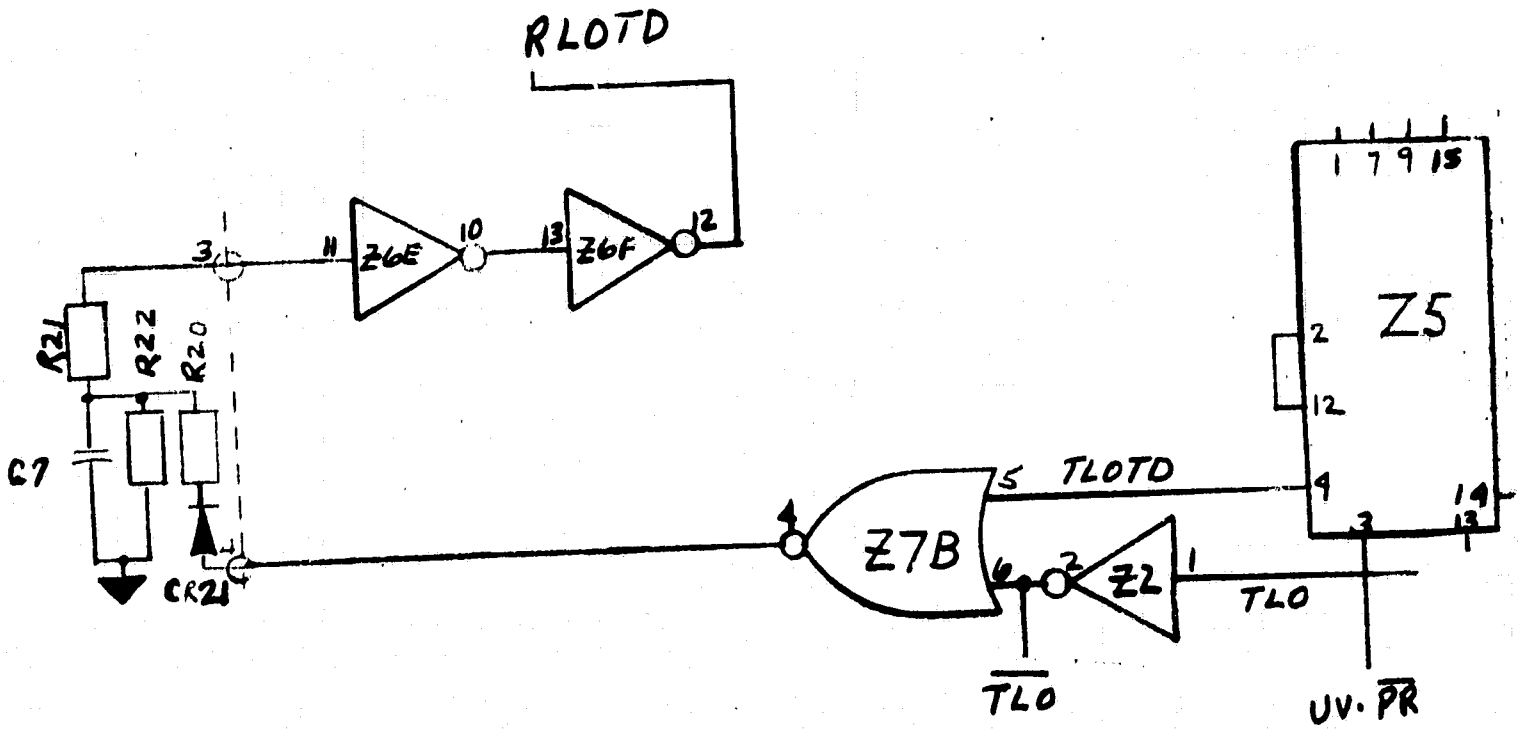


Figure 4-8 - Reset Lockout

4.2.8 Status Indication (Figure 4-9)

The status indication circuit consists of Q4 and associated components. Q4 provides a clamping ground path to give a logic low when the RPC is in the OFF state. This occurs after an overcurrent or undervoltage (on the 28V bus) trip as well as when turned off by the control switch. When the RPC is on, Q4 is not conducting and the voltage at the status terminal rises to the limit of CR15 (4.7 volts) to give a logic high. Reverse voltage protection is provided by CR15.

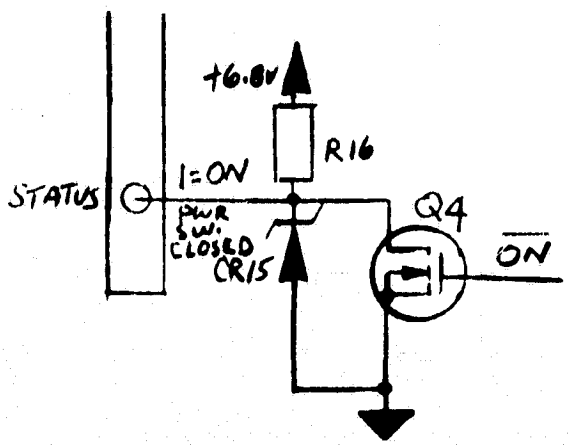
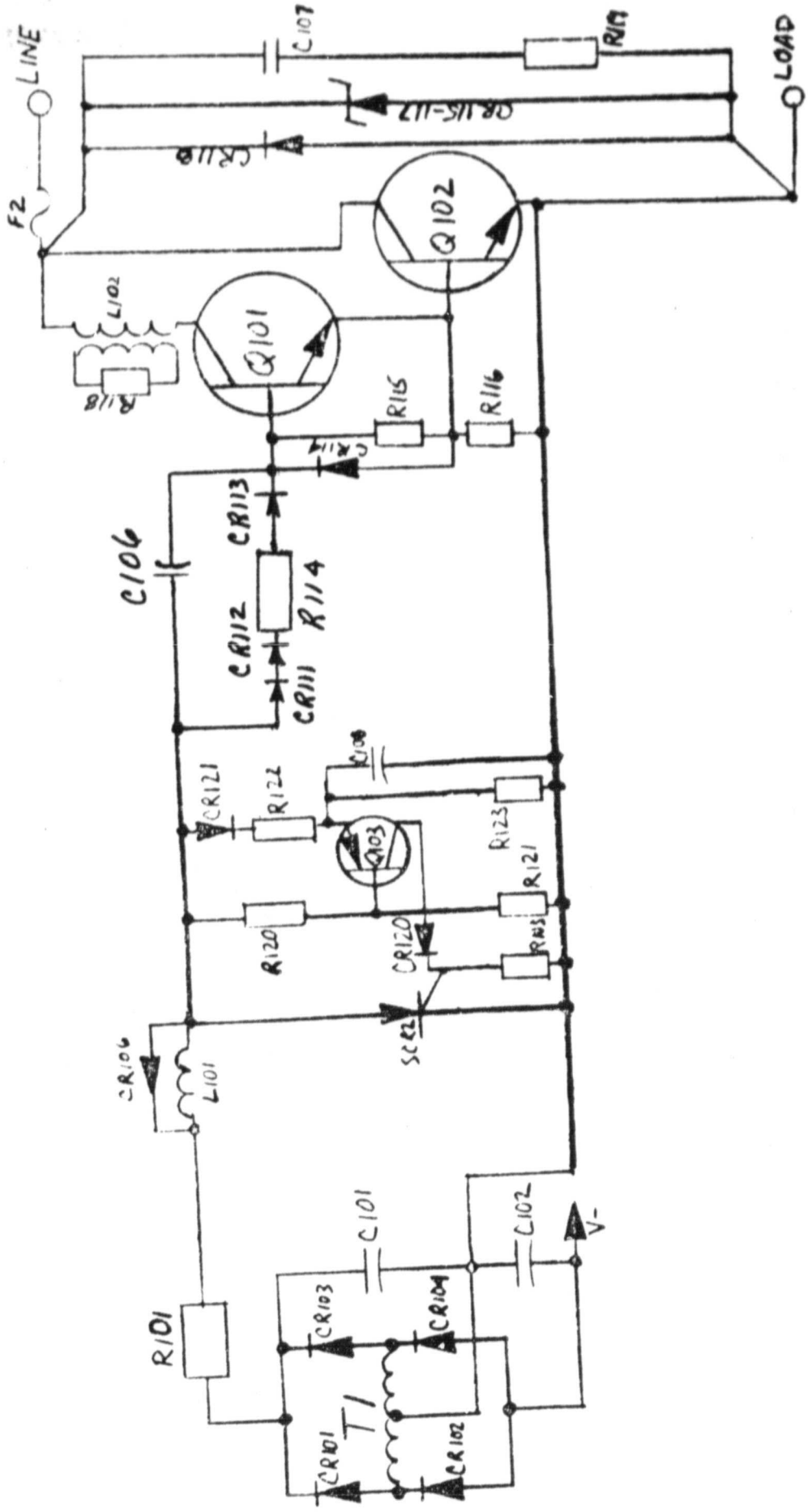


Figure 4-9 - Status Indication

4.2.9 Power Switch and Base Drive (Figures 4-10 Through 4-12)

The power switch consists of Q102 with Q101 as its Darlington driver. It is Zener and snubber protected against voltage peaks and the driver is protected against current surges. A low impedance emitter-base resistor enhances voltage blocking capability. On turn-on, the normal oscillator starting time is sufficiently fast to maintain the power switch Q102 in its safe operating area since the voltage falls before the load current is fully established. During normal operation, C106 becomes charged because of the few volts drop across CR111, CR112, CR113, and R114. For a fast turn-off, SCR2 is fired which allows C106 to discharge down through SCR2, R116, and R115-CR114. This applies a reverse potential across Q101 and Q102 emitter-base junctions which clears the junctions of carriers. These diodes are included in series with R114 to obtain a minimum voltage on C106 equal to three diode drops.

On turn-off, the switch voltage rises before the load current has dropped significantly, presenting the danger of excessive power dissipation. In order to prevent this occurrence, two drive decay detectors centered around Q103 senses the fall of the filtered drive voltage on turn-off and triggers SCR2, applying the voltage on C106 in reverse direction across the power switch. This is a momentary voltage to sweep the carriers and is not intended to be a highly negative voltage during turn-off. This could cause negative bias secondary breakdown. Typical operating times are given in figures 4-11 and 4-12.



ORIGINAL PAGE IS
OF POOR QUALITY

Figure 4-10 - Power Switch and Base Drive

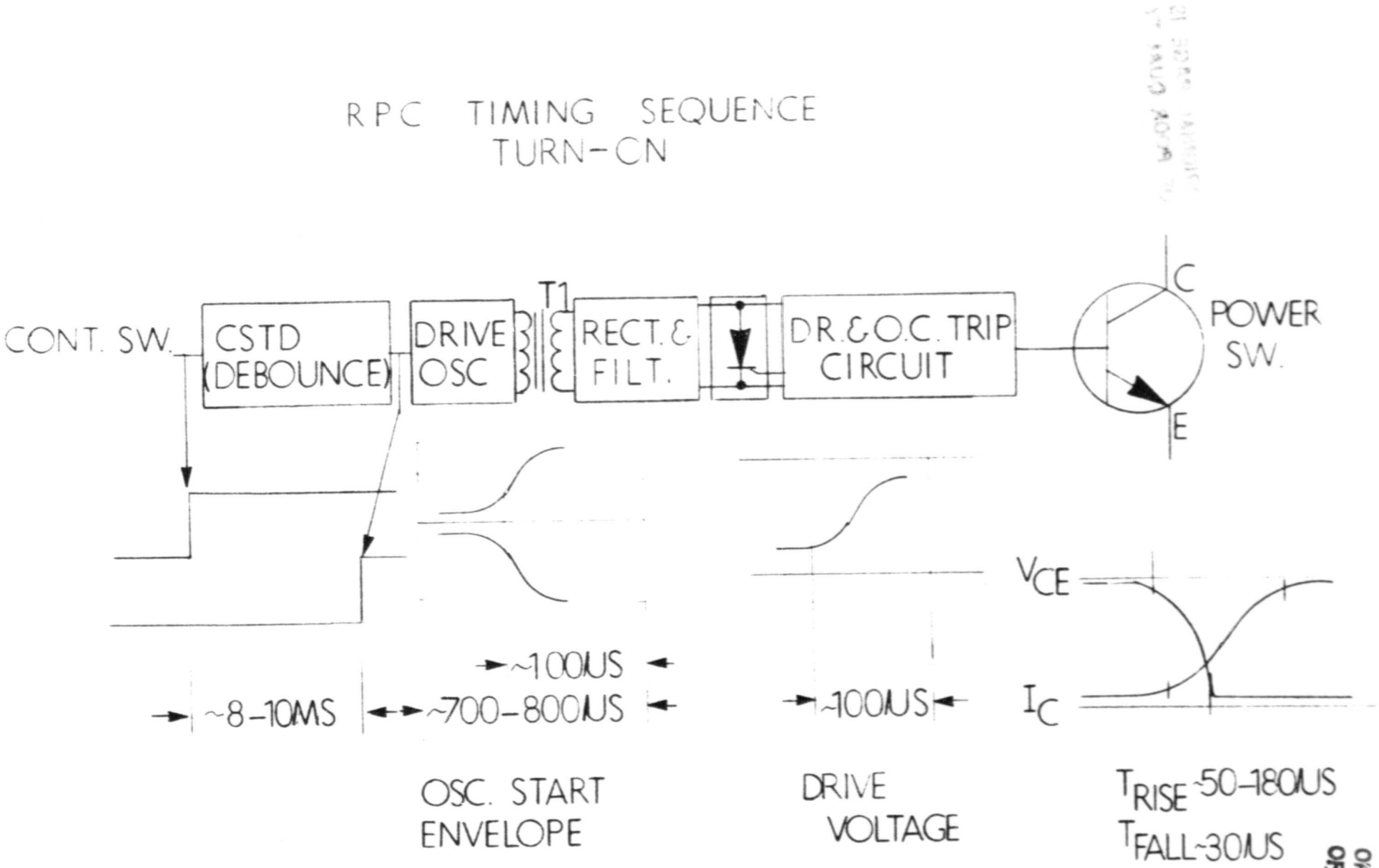


Figure 4-11 - RPC Timing Sequence - Turn-On

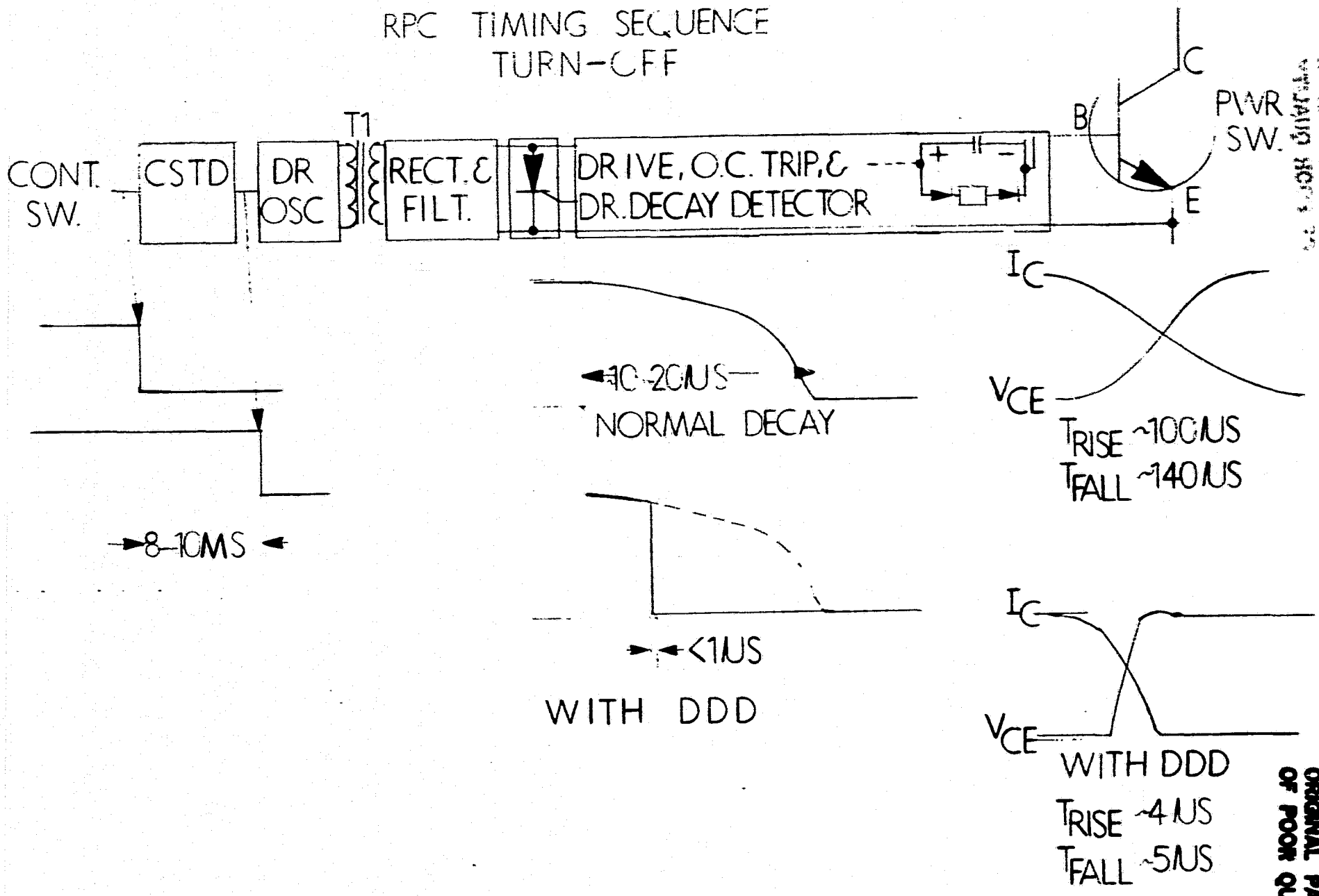


Figure 4-12 - RPC Timing Sequence - Turn-Off

4.2.10 Overcurrent Protection (Figures 4-13, 4-14)

The overcurrent protection circuit consists of current shunt R117; operational amplifiers Z101, Z102, and Z103; transistors Q103, SCR1, SCR2; and associated diodes, resistors, and capacitors. Its purpose is to monitor load current and to provide a trip signal whenever the current level exceeds the minimum overcurrent threshold level, nominally about 1.25 PU (31.25 amperes). The tripping time is inversely related to the level of overcurrent; that is, the greater the current, the shorter the tripping time. The overcurrent circuit functions in the following manner.

A fast acting overcurrent protection circuit is shown in figure 3-2. Z101 and Z102 are connected in a normal inverting threshold/integrator trip circuit. CR110 is a 1.22V precision reference which along with R110 and R112 sets the threshold at which Z101 responds and causes the output at pin 6 to go high which in turn charges capacitors C105 through R109. When the voltage at pin 6 of Z101 is greater than CR110 reference voltage, Z102 comparator output at pin 2 goes positive which fires SCR1 through CR105. This causes a slow trip response from the base drive circuit since C106 must discharge through CR106 in addition to SCR1. This gives less reverse voltage across the emitter-base junctions of Q101 and Q102.

4.2.10 Overcurrent Protection (Figures 4-13, 4-14) (Continued)

Pin 6 of Z101 can reach the reference voltage of 1.22 volts by allowing C105 to charge to that voltage (integrating the current) which results in an inverse current/time relationship. If the load current reached 3 PU, there would tend to be a highly negative voltage at pin 2 of Z101 and its output would be driven suddenly positive and the resulting voltage drop would appear across R109 since C105 would be a short circuit. This would allow pin 6 to go above 1.22 volts without waiting for capacitor C105 to charge. An instant trip condition could result. R109 is chosen for this to occur at 3 PU. Z101 and Z102 are relatively slow devices and this instant trip would take several microseconds before the output of Z102 went positive. If this occurred as the result of a short circuit, the current could well be above 5 PU before a trip was initiated. No action would begin until the current reached 3 PU and in the few microseconds response time of Z101 and Z102, the current could rise much higher. Therefore, this circuit is not adequate for short circuit protection without current limiting. It is adequate for light overloads.

4.2.10 Overcurrent Protection (Figures 4-13, 4-14) (Continued)

The current sensing shunt R117 gives 50 millivolts drop at 25A (1 PU) load. This voltage does not normally appear at pin 3 of Z103 because of capacitor C103. However, with a rapidly rising current (e.g., a steep front of current from a short circuit), C103 appears as an effective short circuit, and half of the negative shunt voltage appears at pin 3 of Z103 (R106 and R107 are equal and divide the shunt voltage). Pin 3 of Z103 is normally held at +55 millivolts. Therefore, when a steep front of load current reached 2.2 per unit, the net voltage at pin 3 of Z103 would be zero since the shunt voltage of -110 millivolts is divided and exactly neutralizes the +55 millivolts at the inverting terminal. As the steep front increased beyond 2.2 PU, the output of Z103 would go positive and fire SCR1 and SCR2. This would give a fast tripping action as previously described. A very fast operational amplifier is chosen for Z103. Tripping action takes less than one microsecond. The normal current/time trip curve is shown in figure 4-14.

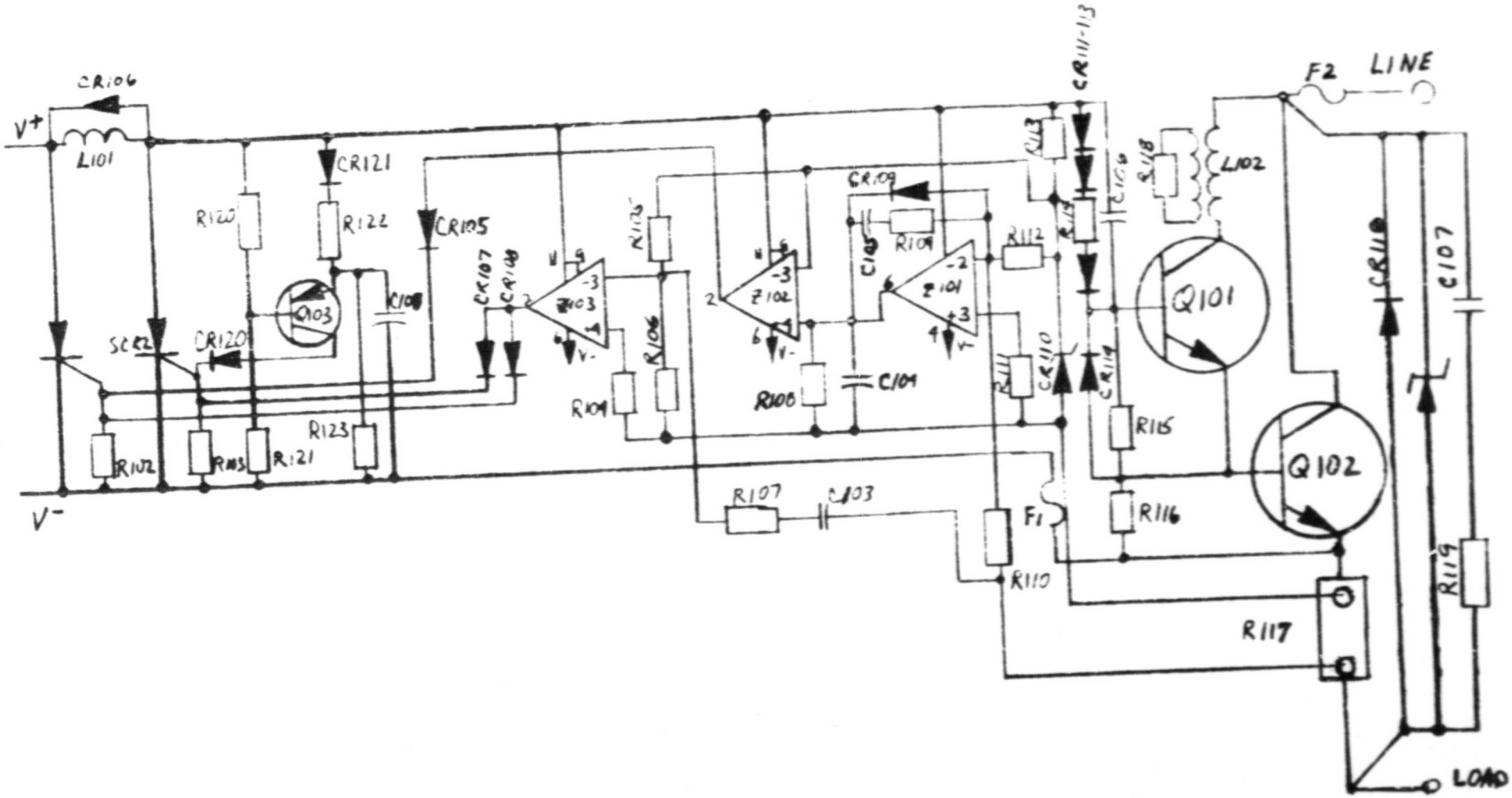


Figure 4-13 - Overcurrent Protection Circuit

Figure 4-14 - Overcurrent Protection Curve

4.3 General Comments, Packaging

The isolation interfaces in this RPC provide overcurrent protection without discrete isolator components or hard electrical connections from the high voltage line to the low voltage logic circuit. All drive power is provided by the 28V control voltage; therefore, absence of control voltage prevents switch turn-on, except of course, in a shorted failure mode. The limiting factors for isolation are the power switch, the output diode, and the Royer transformer isolation. The latter two can be quite high - the diode on the order of 1,400-1,500 volts and the transformer 2,000-3,000 volts, leaving the power switch as the weak link.

Protection from HVDC, by Royer transformer breakdown of the control logic and equipment connected to it through the 28V power supply and the status circuits, can be achieved by using an appropriately sized varistor as shown in figure 4-1. It is not known if the HVDC ground and the control ground will be common in the RPC application. If they are common or if the control ground is floating at ten volts or less below power ground, the varistor and associated interrupting fuse F2 would provide adequate protection. However, if the grounds are more widely separated, additional protection should be considered such as employing individual varistors at the control, 28V, and status terminals.

4.3 General Comments, Packaging (Continued)

Probable production packaging based on component size and isolation requirements would be a combination of three modules. One module would contain the control, logic, status indication, trip indication, and the low level components of the power supply and primary side of the Royer. A second module would contain the base drive circuit including the bridge rectifiers and filters on the secondary side of the Royer. The third module would house the overcurrent protection circuit.

The additional components such as the Royer transformer, commutation diodes, fuse, and power transistors would be external to the modules because of size and isolation considerations. Because of the one kilovolt potential involved, care must be exercised in packaging to make certain components and/or modules operating at different voltage levels are separated by suitable dielectric material. For the breadboard, mechanical spacing will be relied on. On a flight worthy unit, there should be solid insulation used for isolation and close attention paid to its selection and installation. A minimum of 2,200 VAC dielectric breakdown should be provided in the range of four to six torr ambient pressure.

4.4 Preliminary Tests (Figures 4-15 Through 4-23)

Since one kilovolt transistors were not available when this project reached the design stage, lower voltage transistors (Westinghouse D60T) were used for preliminary development test and the high voltage D70T transistors from Westinghouse R&D Center were later substituted. Since the HV power subcircuit has only magnetic coupling to the low voltage subcircuit, no changes were made in the circuit for low voltage testing. The only inherent limitations to the operating voltage of the power circuit are the breakdown voltages of the HV power switch transistors, commutating diode, and the coupling transformer. Circuit limitations are the inductance of the source line and capacitance of the load.

Tests conducted on a preliminary circuit at reduced voltage and current indicate that very fast trip action can be achieved. Figure 4-15 shows a fast trip of what would have been a ten per unit overload using a line voltage of 125 volts and one per unit of five amperes. The fast trip pickup level was set at 1.25 PU showing response time on the order of a microsecond.

Figures 4-16 and 4-17 show one per unit current turn-on and turn-off, again with a line voltage of 125 volts and one per unit of five amperes.

4.4 Preliminary Tests (Figures 4-15 Through 4-23) (Continued)

Figures 4-18, 4-19, 4-20, and 4-21 show the action of the trip circuit turning on into various loads. The fast trip action picks up in figure 4-21, which shows a trip which would have resulted in a 3.5 PU load current had not the fast trip acted on the rising current slope. The expanded time scale of figure 4-22 shows turn-on into a short circuit. Figure 4-23 shows a short circuit with a one per unit preload.

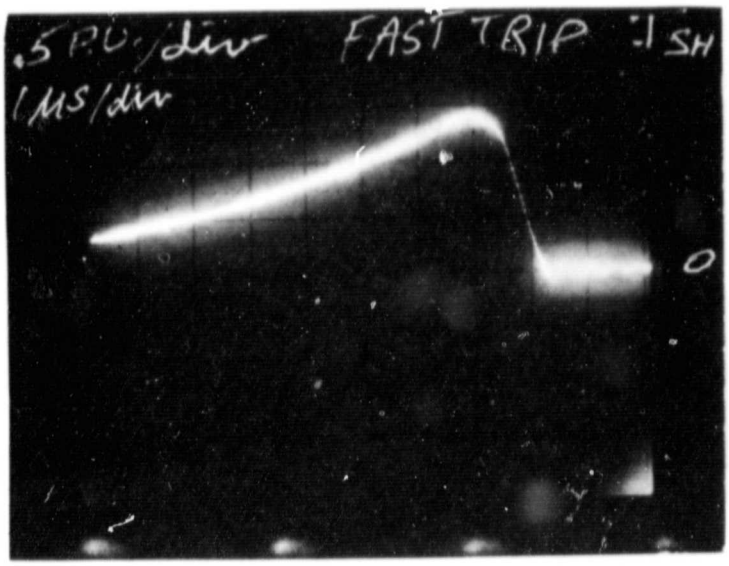


Figure 4-15 - Shunt Current
1 PU = 5A
Line Voltage = 125V
10 PU Fault

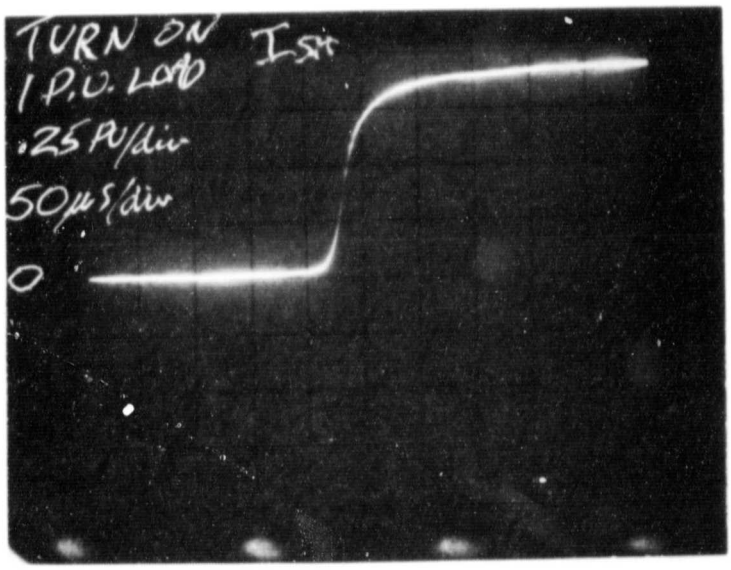


Figure 4-16 - Shunt Current
1 PU = 5A
Line Voltage = 125V
1 PU Turn-On

ORIGINAL PAGE
BLACK AND WHITE PHOTOGRAPH

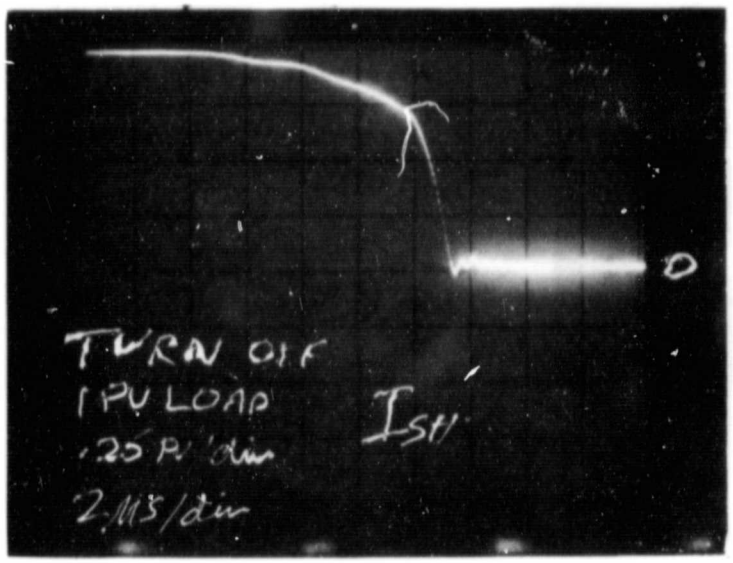


Figure 4-17 - Shunt Current
1 PU = 5A
Line Voltage = 125V
1 PU Turn-Off

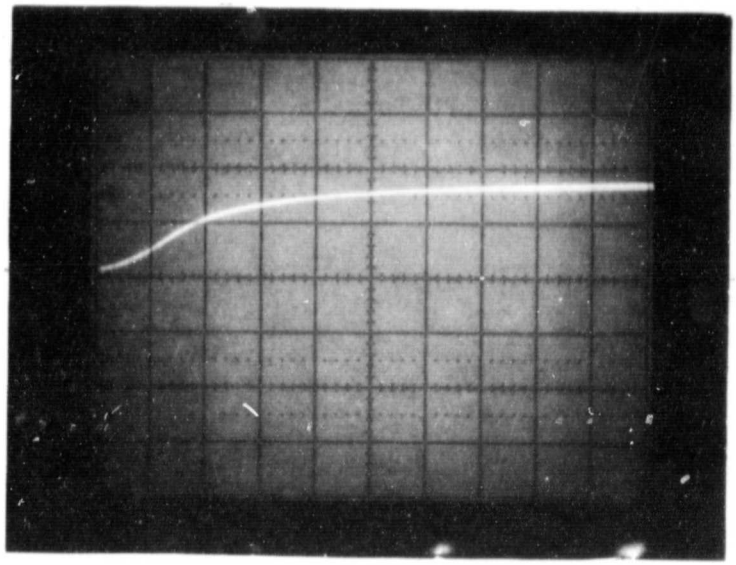


Figure 4-18 - Load Current
Turn-On into 2 PU Load
Line Voltage = 200V
1 PU = 5A
1 PU/Division
10 Microseconds/Division
Eventual Trip at 200
Milliseconds

ORIGINAL PAGE
BLACK AND WHITE PHOTOGRAPH

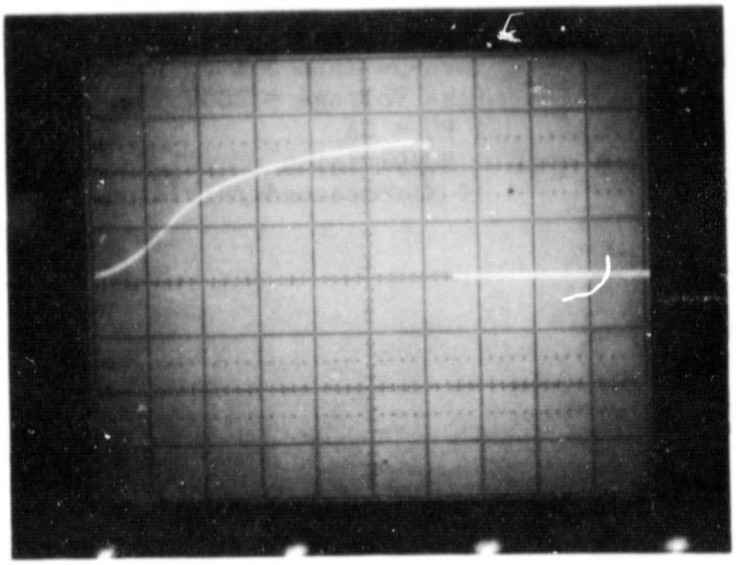


Figure 4-19 - Load Current
Turn-On into 2.5 PU Load
Line Voltage = 200V
1 PU = 5A
1 PU/Division
10 Microseconds/Division

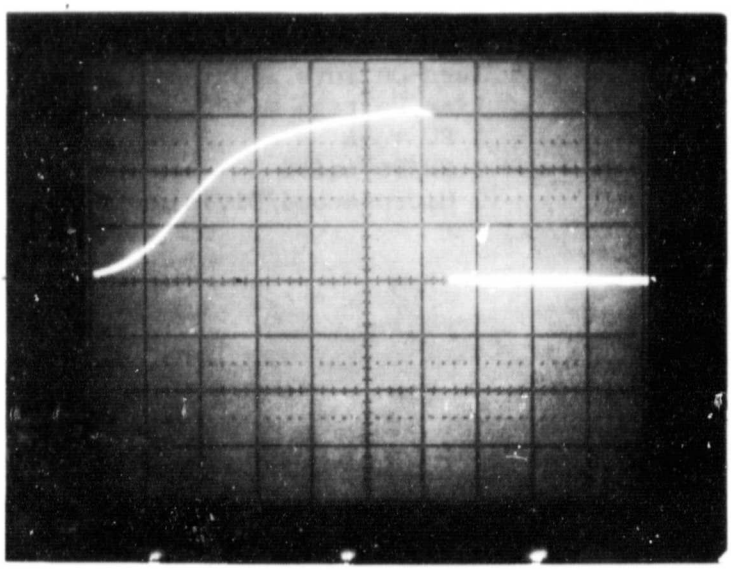


Figure 4-20 - Load Current
Turn-On into 3 PU Load
Line Voltage = 200V
1 PU = 5A
1 PU/Division
10 Microseconds/Division

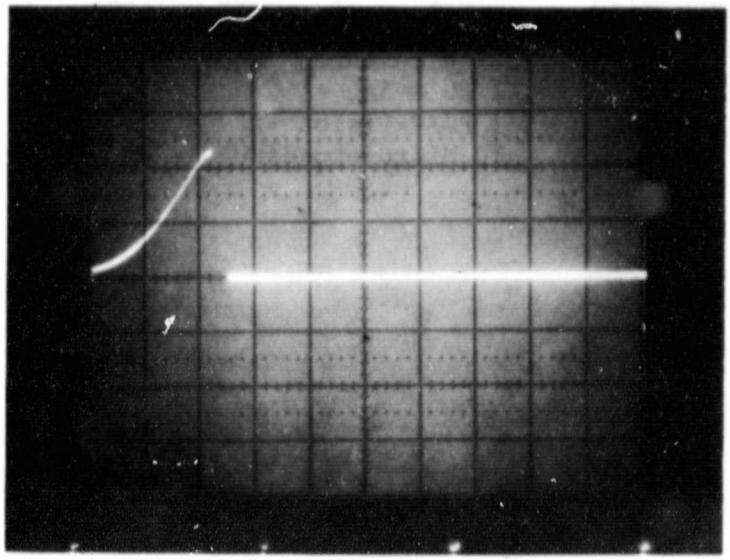


Figure 4-21 - Load Current
Turn-On into 3.5 PU Load
Line Voltage = 200V
1 PU = 5A
1 PU/Division
10 Microseconds/Division

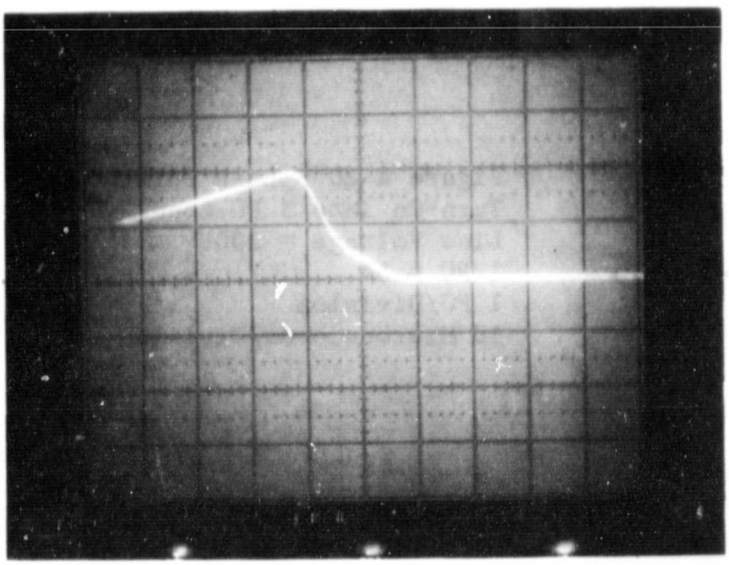


Figure 4-22 - Load Current
Turn-On into Short Circuit
Line Voltage = 200V
1 PU = 5A
1 PU/Division
1 Microsecond/Division

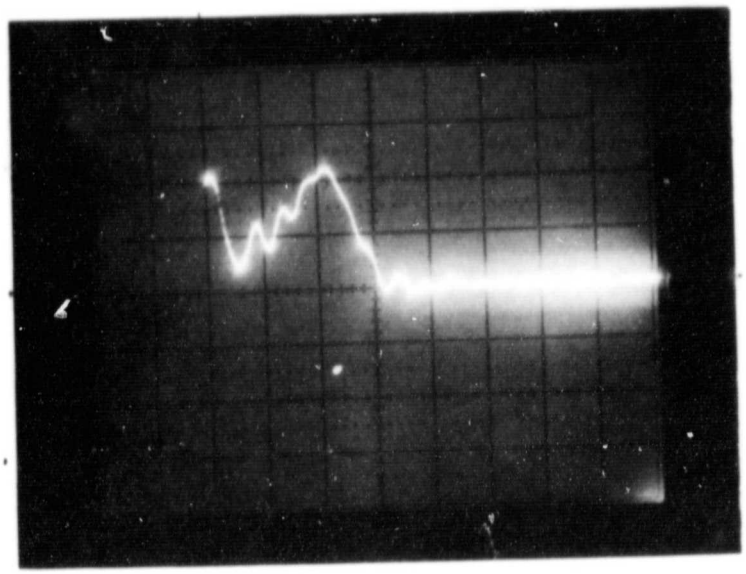


Figure 4-23 - Load Current
Short Circuit with 1 PU
Preload
Line Voltage = 200V
1 PU = 5A
1 PU/Division
1 Microsecond/Division

SECTION V

TESTING AND EVALUATION OF BREADBOARDS

(TASK III)

5.1 Task Objectives

1. Prepare a test plan.
2. Design and assemble the necessary test circuits, instrumentation, power sources, and loads.
3. Perform tests to demonstrate compliance with the specification.
4. Prepare and interpret test data.

5.2 Test Plan

The test plan is shown in appendix A.

5.3 Test Circuit (Figure 5-1)

The test circuit is shown in figure 5-1. Two 600V, 50A DC power supplies were connected in series. They are Electrical Measurements, Model 600-50. A coaxial current shunt was used for the oscilloscope current pickup.

Initially, the characteristics of the power supply were investigated. Voltage overshoot was observed on turn-off and on overcurrent trips. Capacitance was added at the wall mounted control box to minimize the effect of line inductance back to the power supply (which is located outside the laboratory), leaving only the line inductance from the control box over to the RPC on the bench. Additionally, a snubber was used across the power switch to further reduce overshoot.

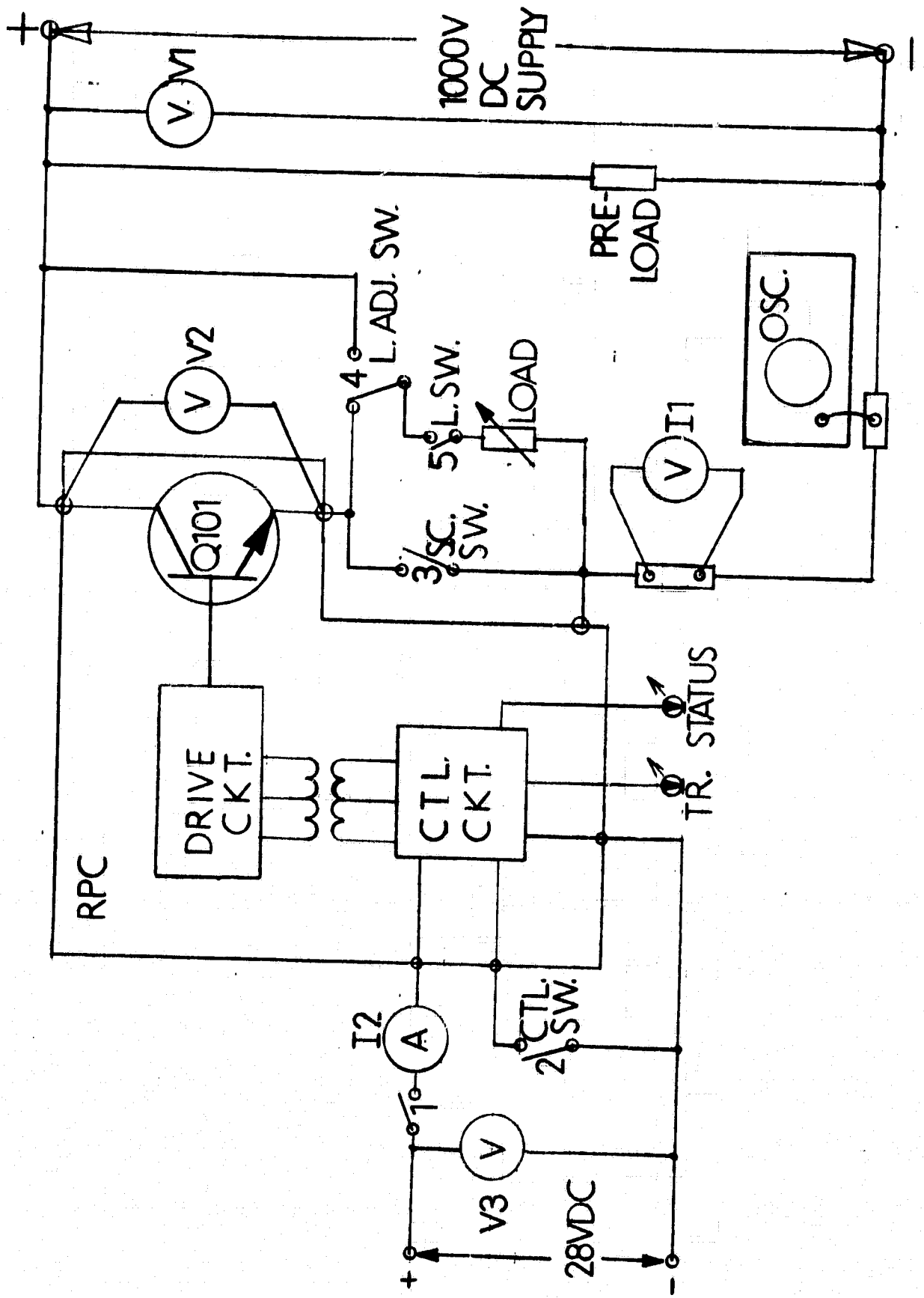


Figure 5-1 - Test Circuit

5.4 Development Tests and Results (Figures 5-2 Through 5-11)

Testing of the RPC began with spot checks at various loads and voltages. The RPC successfully switched 25 amps at 900 volts and cleared light overcurrent conditions. The RPC was also turned on into a short circuit at 900 volts with a resultant 35A current peak falling in about three microseconds (figure 5-2). Switch drop data was taken at five, ten, 15, 20, and 25 amps and at control voltages of 21, 28, and 35 volts, while observing control current in the ON, OFF, and TRIPPED states. The control current remained stable in these three states at each control voltage level regardless of load current (see tables).

At this point, a data run was begun intending to include 400, 700, and 900 volts line voltage, switch drops and control voltage, and current data for 20 through 100% rated load. During this data run, the switch failed shorted at 700 volts line voltage and about 19 amps load current. The driver transistor was unharmed. It was decided that after replacing the switching transistor, testing would be confined to the 600V level with more extensive data taken.

Several days later during some lower voltage short circuit tests, another failure occurred which as in the case of the first may have been due to extraordinary stresses not expected in normal operation.

The shorted transistors were examined at the Westinghouse R&D Center in Pittsburgh. They were found to have burned spots indicating failure as a result of too rapid ON/OFF cycling. This probably was done in testing without a sensitivity toward what was happening to the junctions. Consultation with R&D scientists also indicated their concern over the speed of a normal turn-off in the RPC application.

5.4 Development Tests and Results (Figures 5-2 Through 5-11) (Continued)

Two circuit changes were made to improve the transistor survival rate. First, after an overcurrent trip (excessive current has passed through the RPC causing greater dissipation at the junction of the transistor), the cycling of the control switch is inhibited for ten to 20 seconds allowing junction temperatures to equalize. This delay is also in force even if an attempt to recycle is made by removing and reapplying the control voltage. Second, on normal turn-off, the drive to the switch element is shut off more rapidly. Instead of allowing the drive to decay normally, a SCR is fired after the drive voltage is applied to the junction with only slightly less impact than an overcurrent trip. This substantially reduces turn-off time, sparing the transistor from excessive heating.

Turn-on and turn-off rise and fall times are shown in figures 5-3 and 5-4. At turn-on, the switch voltage fall time (90 to 10%) is approximately 30 microseconds while current rise time is in the 180-200 microsecond range (figure 5-3). At turn-off, the voltage rises in about 100 microseconds while the current falls in about 140 microseconds (figure 5-4).

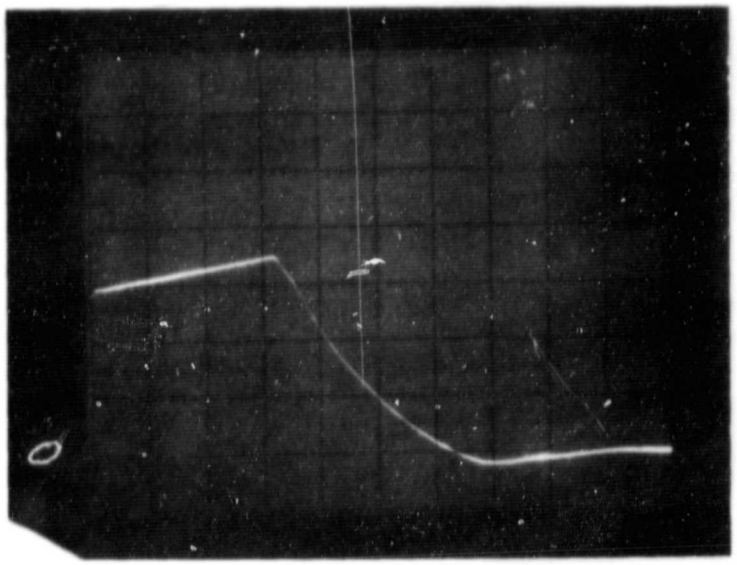


Figure 5-2 - Load Current
Turn-On into Short Circuit
Line Voltage = 900V
10A/Division
1 Microsecond/Division

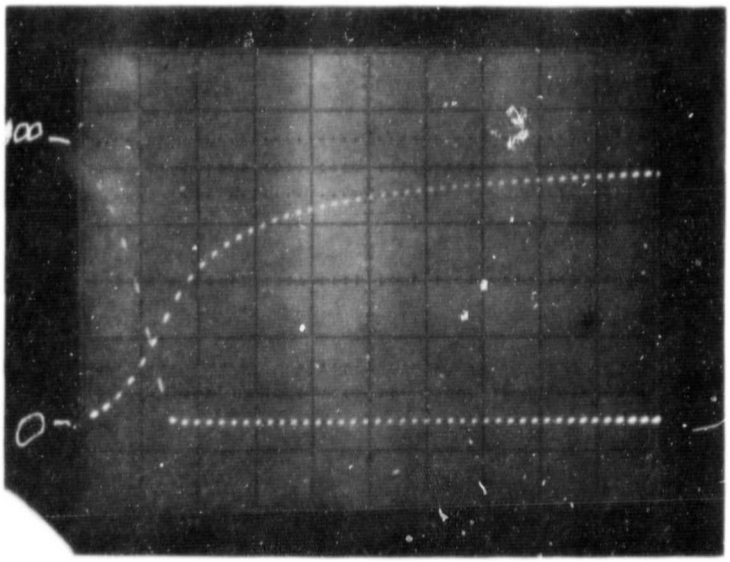


Figure 5-3 - Turn-On Switch
Voltage
600V = 100%
Switch Current 25A = 100%
20 Microseconds/Division

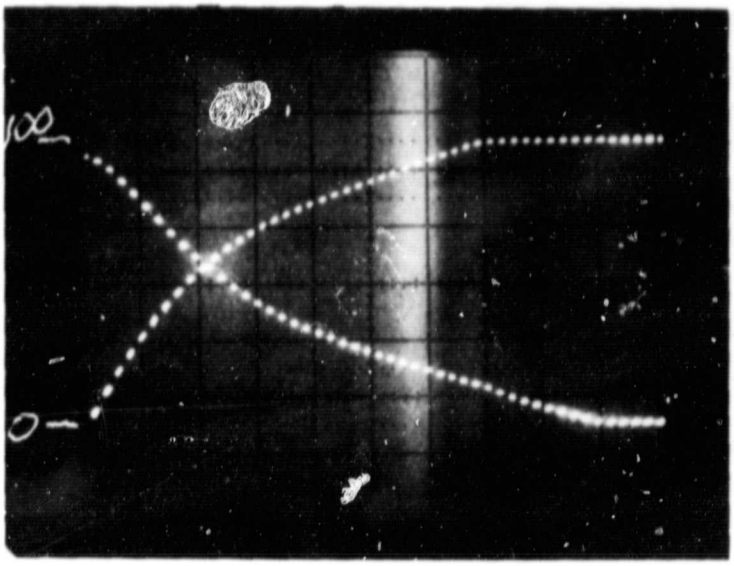


Figure 5-4 - Turn-Off Switch Voltage
600V = 100%
Switch Current 25A = 100%
20 Microseconds/Division

5.4 Development Tests and Results (Figures 5-2 Through 5-11) (Continued)

Actual turn-on time from control switch to load current is compiled as follows: the control switch action passes through an eight to ten millisecond debounce time delay and then sends an ON signal to the Royer oscillator. The Royer comes to full voltage in about .8 millisecond. During the first 700 microseconds or so, the voltage rises slowly to about 2.5 to 3.5 volts and then rises rapidly to its full seven volt level. The switch begins to turn on at the start of this steeper rise as diode thresholds are exceeded. This time relationship is shown in figure 5-5.

The control undervoltage protection was activated as control voltage dropped to 17.30 volts and returned to normal operation as control voltage rose to 17.35 volts.

Because the RPC has a normal turn-off that is relatively fast, it was found that adding a damping coil to the inductor which is in series with the driver collector prevented voltage spikes on turn-off while still maintaining the desired current limiting action in the driver during ON state faults. Additionally, it was found that voltage spikes caused by line inductance could be minimized by adding a small capacitance across the supply near the RPC terminals. A summary of test data is given in the tables and curves.

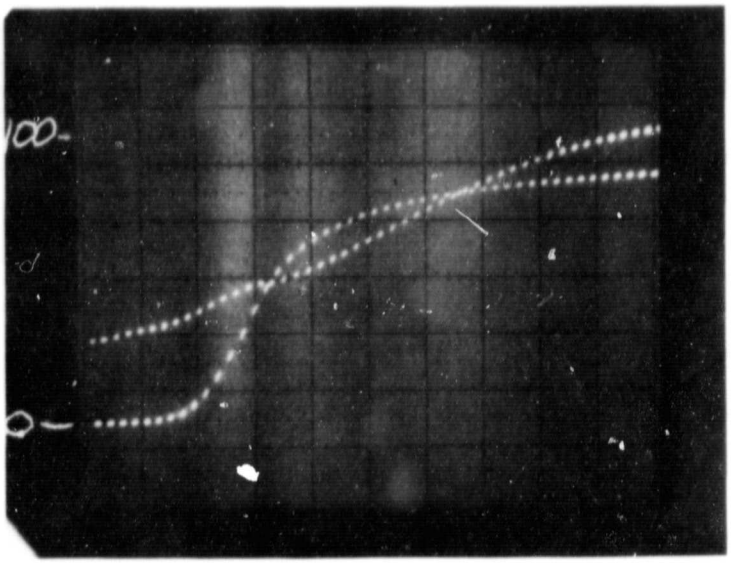
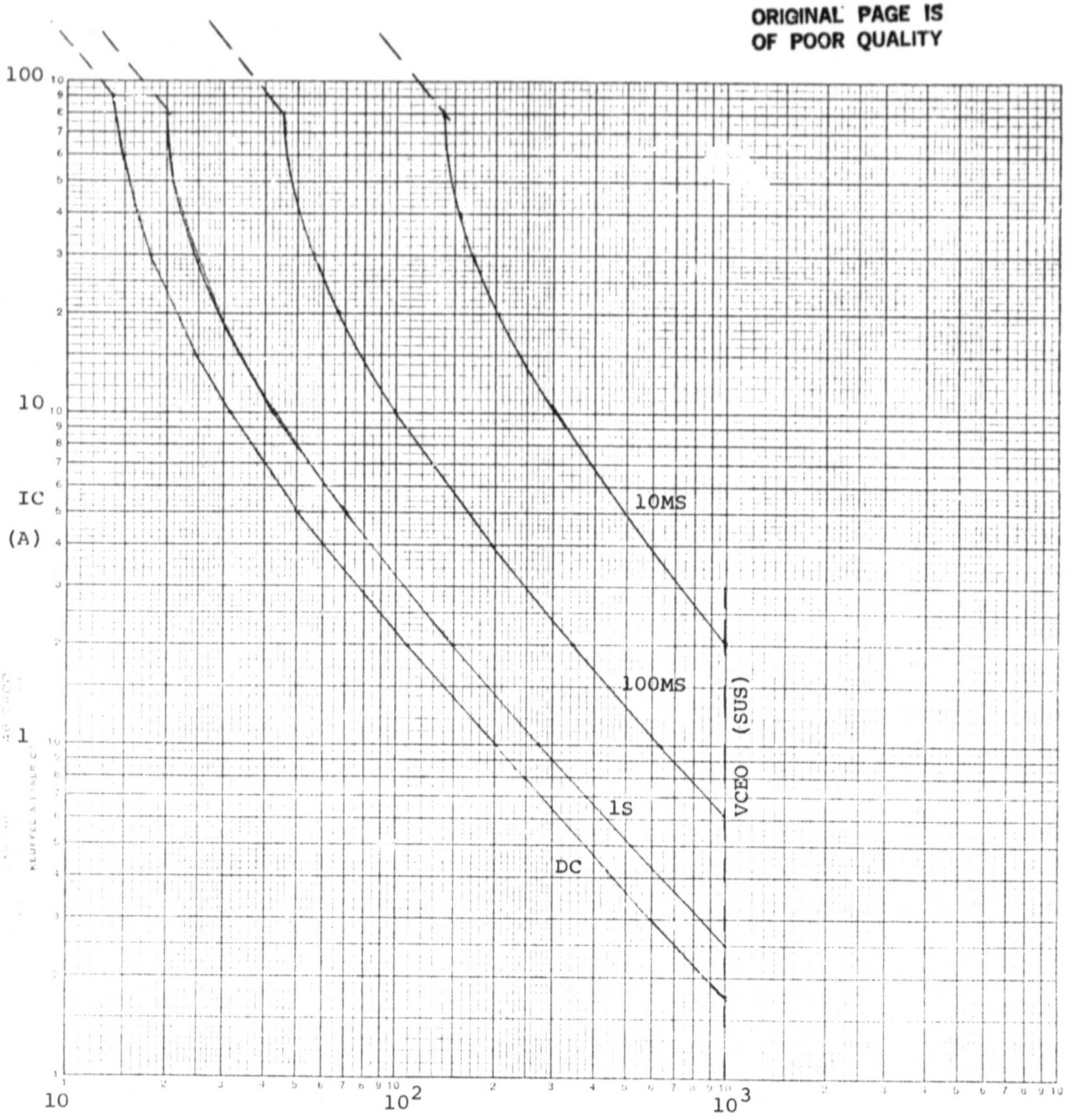


Figure 5-5 - Turn-On Drive Voltage
7V = 100%
Shunt Current 25A = 100%



Calculated Forward SOA for D70 Stud
RθJC = 0.085°C (DC)
RE = 1.1 MΩ

Figure 5-6 - SOA of D70T Stud Mounted Transistor

Table 5-1

Bipolar Performance Data

Item	Load Current 5-25A	Specification	Units
On Dissipation	13.27 to 33.27	15.1 to 75.4*	Watts
On Efficiency	99.56 to 99.78	99.5	%
Off Dissipation	.672	5	Watts
Turn-On Time	8 to 10	.01 to 1.0	Milliseconds
Rise Time	50 to 180	10 Minimum	Microseconds
Turn-Off Time	8 to 10	.01 to 1.0	Milliseconds
Fall Time	5	10 Minimum	Microseconds
Control Undervoltage Protection Dropout/Pickup	17.30/17.35	-----	Volts
Projected at 1,000V, 25A on Dissipation	33.27	125.6	Watts
Efficiency 20 to 100% Load	99.74 to 99.87	99.5	%

Undervoltage Time Delay = 9 MS
Reset Time = 9 MS
Trip Lockout Time Delay = 12.7 Seconds

* Based on efficiency of 99.5 at 20 to 100% load (5 to 25A) at 600 volts.

Table 5-2

Switch Drop (Volts) Versus Load Current (Amps) at Control Voltage 21, 28.35V

Switch Drop CTL Voltage	Load Current				
	5	10	15	20	25
21	.75	.8	.85	.95	1.05
28	.75	.8	.85	.92	.95
35	.7	.78	.82	.85	.95

Table 5-3

Power Losses (Watts) and Efficiency (%) Versus Load Current (Amps)

600 VDC at CTL Voltage 21, 28, 35V

CTL Volts		Load Current				
		5	10	15	20	25
21	P_{Loss}	9	13.25	18	24.25	31.5
	EFF	99.7	99.78	99.8	99.8	99.79
28	P_{Loss}	13.27	17.52	22.57	27.92	33.27
	EFF	99.56	99.71	99.75	99.77	99.78
35	P_{Loss}	16.1	20.4	24.9	29.6	36.35
	EFF	99.45	99.66	99.72	99.75	99.76

Table 5-4

Efficiency (%) Versus Bus Voltage at CTL Voltage 21, 28, 35V

Load Current 25 ADC

	120	240	360	480	600
21	98.96	99.48	99.65	99.74	99.79
28	98.9	99.45	99.63	99.72	99.78
35	98.8	99.48	99.6	99.7	99.76

Table 5-5

Control Current (MA) Versus Control Voltage (Volts) ON, OFF, TRIPPED States

	21V	28V	35V
ON	250	340	360
OFF	16	24	31
TRIPPED	14	21	29

Table 5-6

Maximum Capacitance (μF) into Which RPC may be Turned on Without Tripping

Parallel Resistive Load Current (Amps) Versus Bus Voltage (Volts)

Parallel Load Current	Bus Voltage		
	120	300	600
5A	.6	.25	.11
10A	4.1	.28	.14
20A	4.3	.47	.20
25A	3.6	.60	.21

ORIGINAL PAGE IS
OF POOR QUALITY

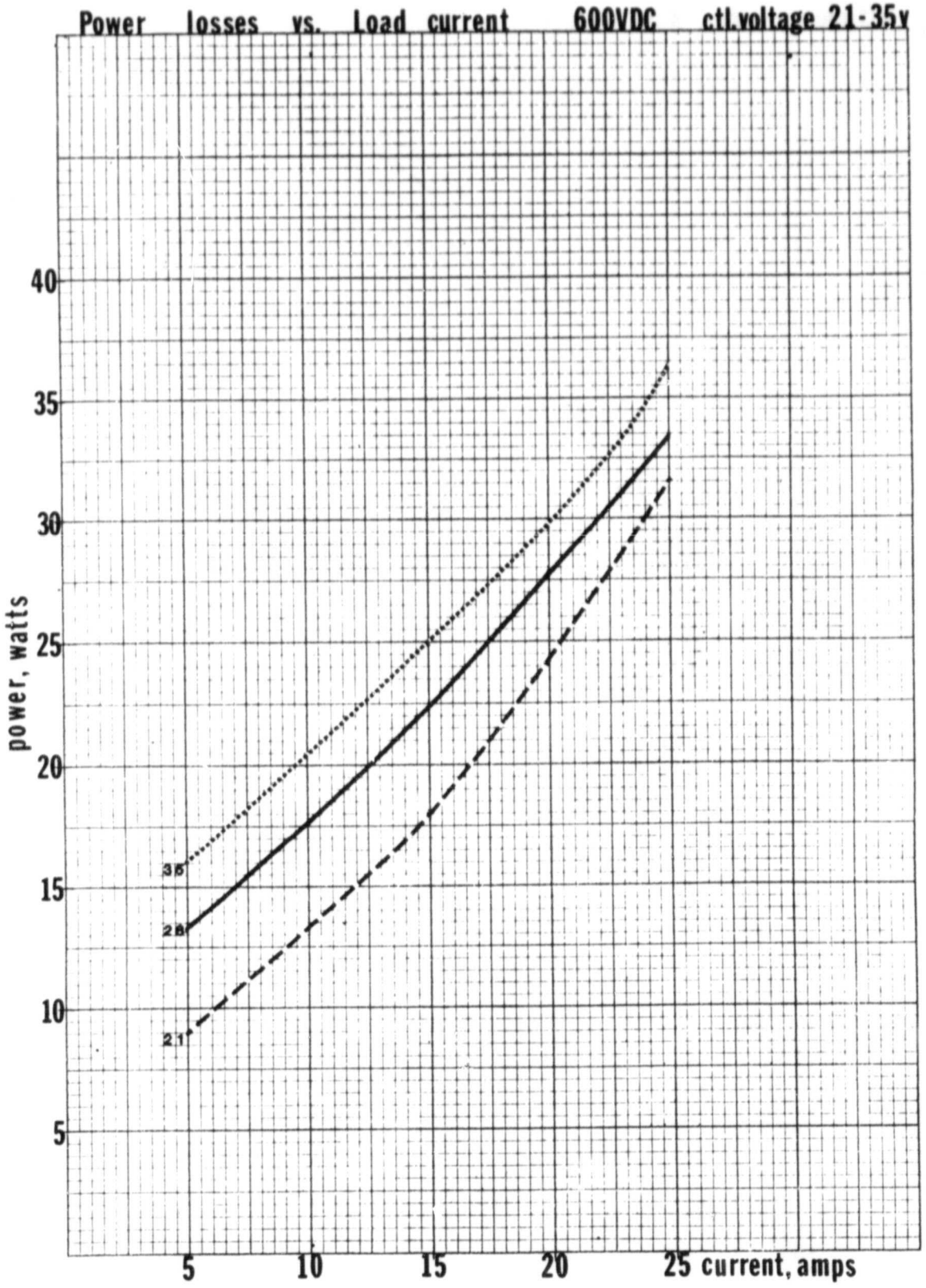


Figure 5-7 - Losses Versus Load Current

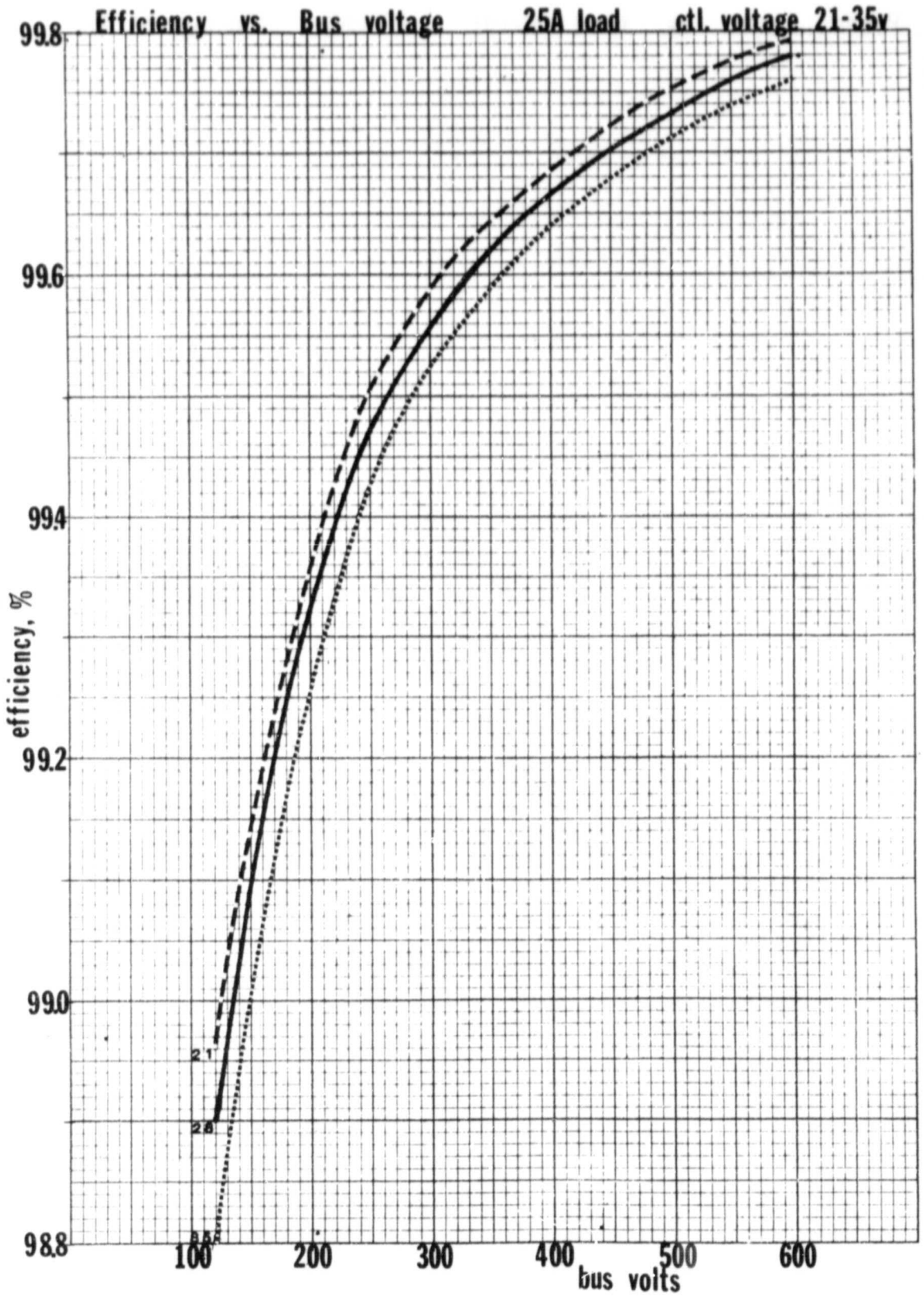


Figure 5-8 - Efficiency Versus Bus Voltage

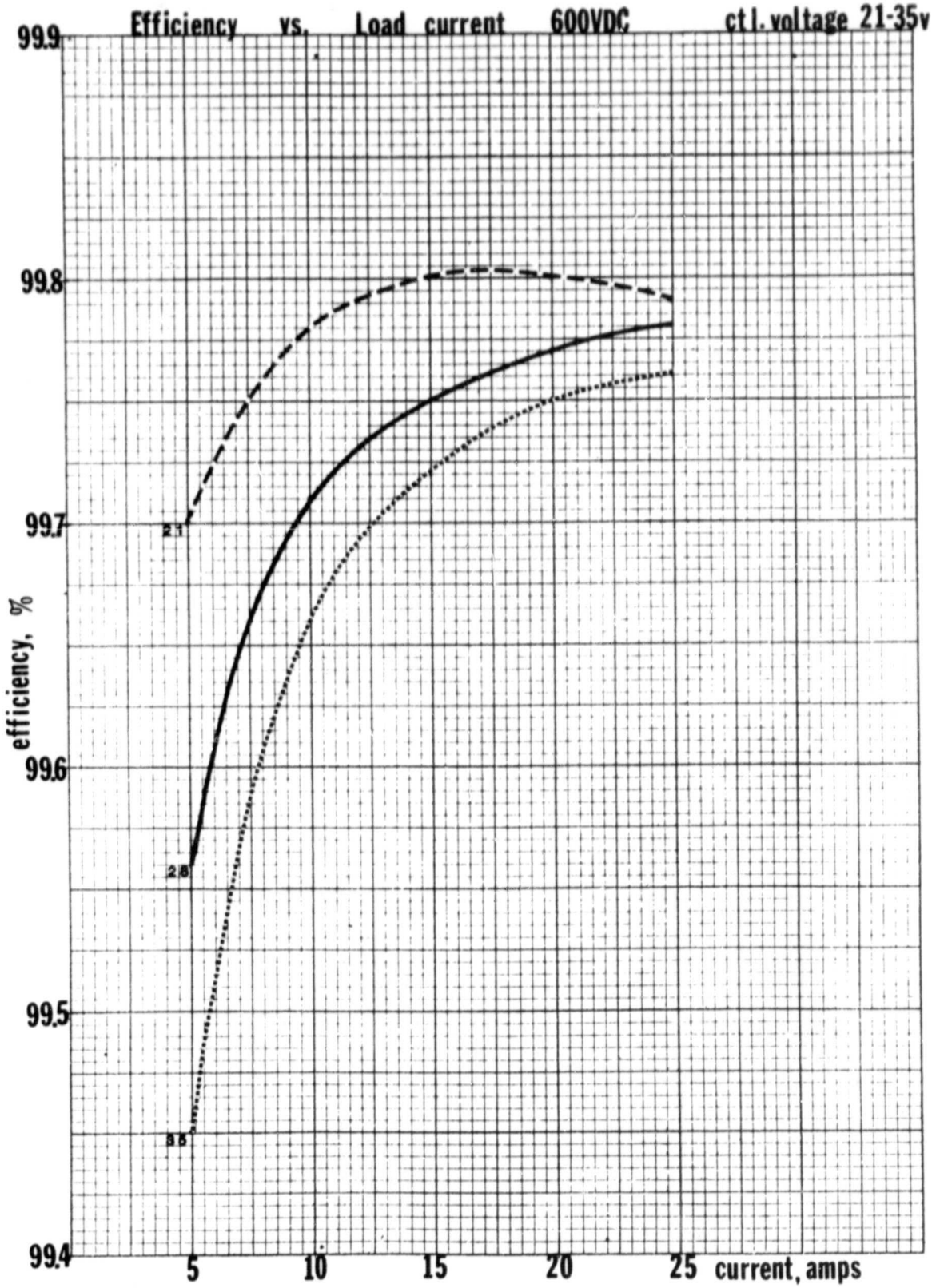


Figure 5-9 - Efficiency Versus Load Current

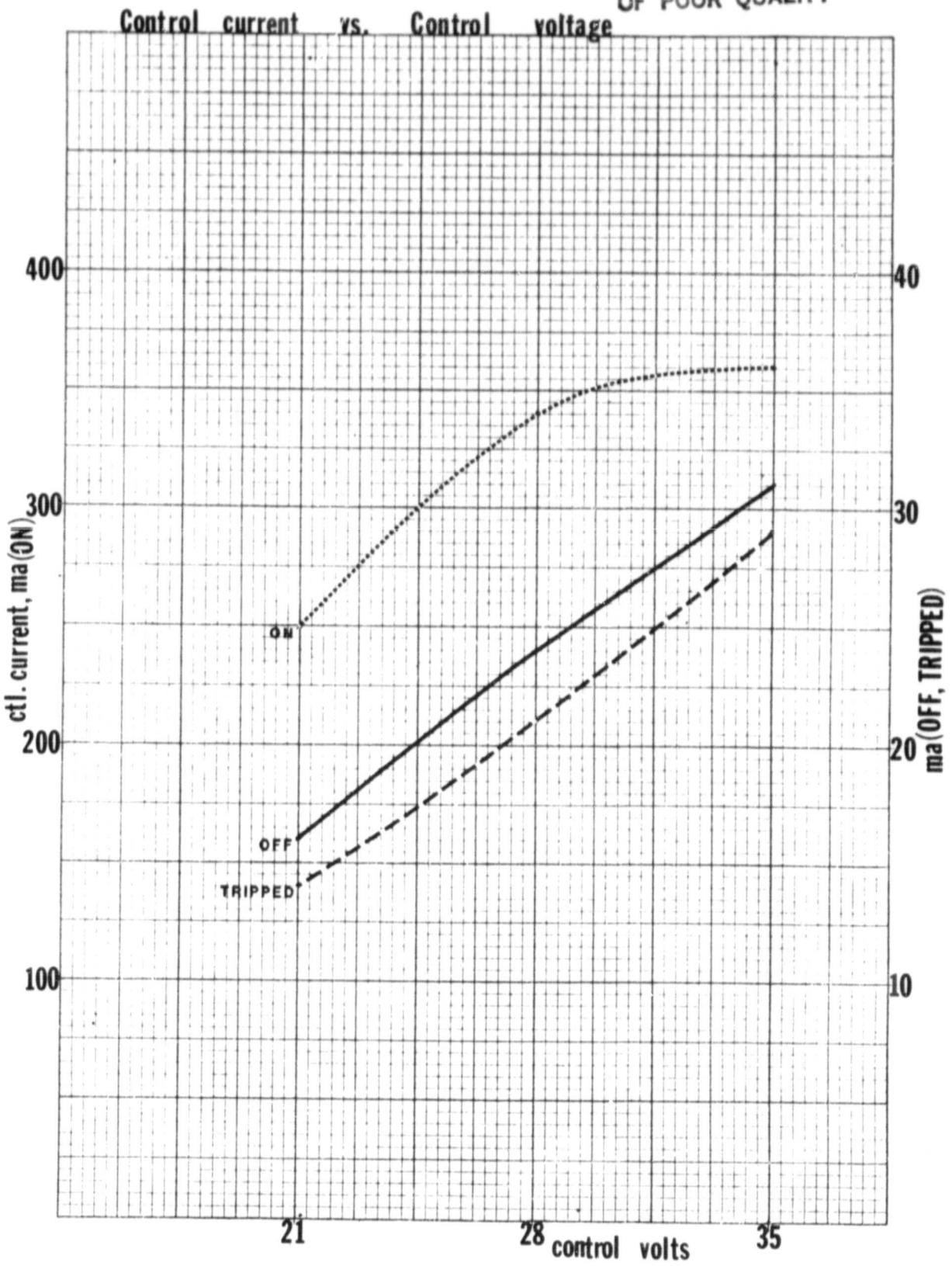


Figure 5-10 - Control Current Versus Control Voltage

ORIGINAL PAGE IS
OF POOR QUALITY

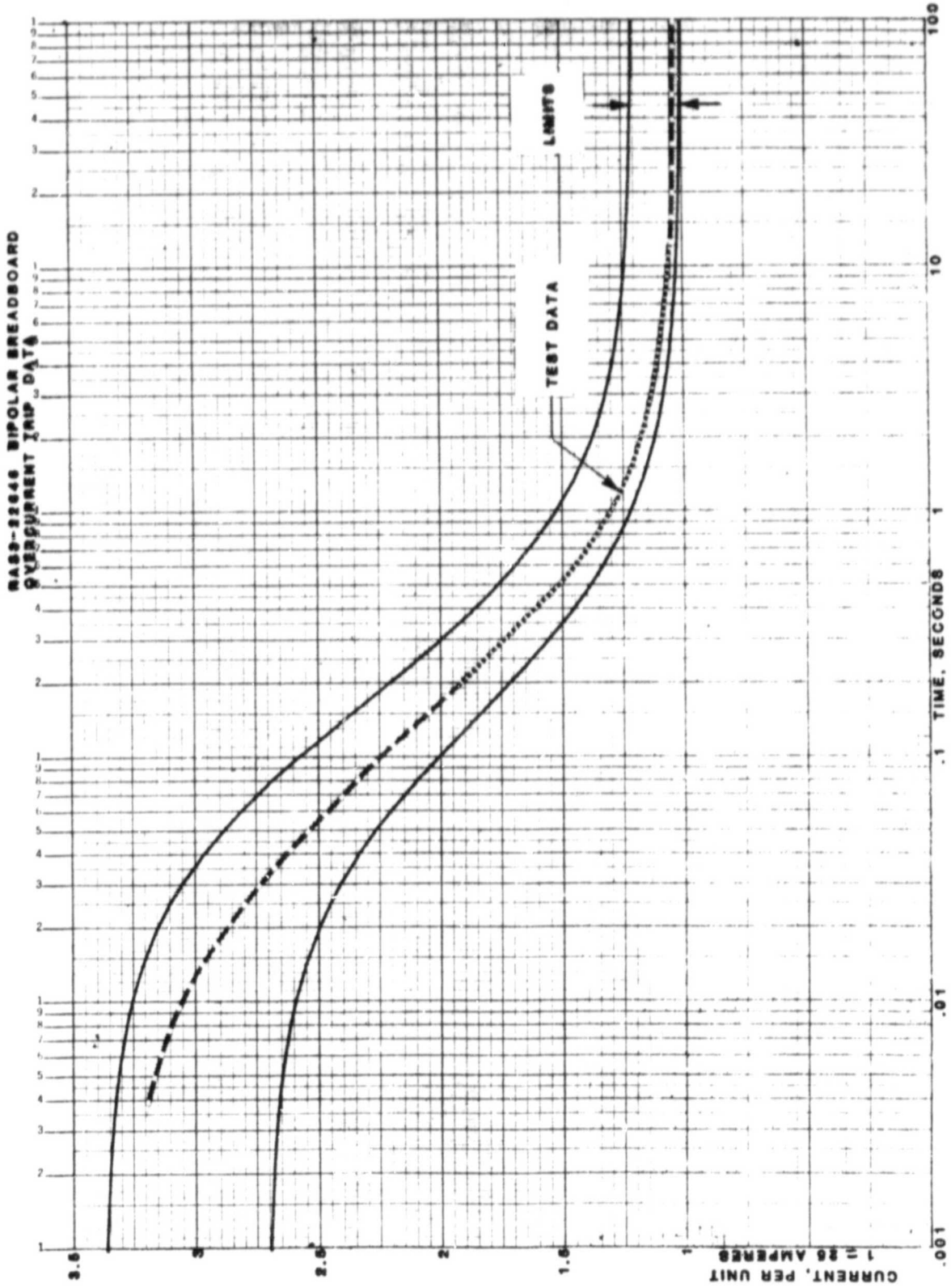


Figure 5-11 - Overcurrent Protection Curve

5.4 Development Tests and Results (Figures 5-2 Through 5-11) (Continued)

Data from figures 5-3 and 5-4 are summarized below.

At 600V, 25A	Turn-On	Turn-Off
Voltage	30 Microseconds FT	100 Microseconds RT
Current	180 Microseconds RT	140 Microseconds FT

As testing on the bipolar breadboard neared completion, the switch transistors were shorted as a result of a protection circuit having been inadvertently disconnected. Additional transistors from Westinghouse R&D Center were received and installed. These latest transistors possess slightly different characteristics than the previous ones. At a sacrifice of about 100 volts of V_{CEO}, sustaining the gain has increased from between three and seven to between 13 and 16 at a collector current of 40 amps. This will insure a low switch drop at the 25A rating.

Turn-on into capacitive load was conducted on the breadboard using bipolar transistors as the power switch. This essentially completes the testing of the bipolar breadboard. The breadboard was tested at voltages up to 900 volts including turning on into current overloads and into a short circuit at that level. However, most of the partial load testing was done at the 600V level. The test plan submitted early in the program was not followed to the letter because of the lower voltages used in testing. Nevertheless, sufficient data was obtained to adequately evaluate the design.

SECTION VI

DEVELOPMENT OF A BIPOLAR TRANSISTOR PACKAGED BREADBOARD DESIGN

(TASK IV)

6.1 Task Objectives

The original objective was to build two packaged breadboards. The task was redefined to furnish the design and cost of a packaged breadboard.

6.2 Drawings

Drawing and information for a packaged breadboard were furnished to NASA-Lewis under separate cover.

SECTION VII

DESIGN OF A POWER MOSFET RPC

(TASK V)

7.1 Task Objectives

The objectives of this task were changed to the following:

1. Using the previously completed analysis, and supplementing it where necessary, design and develop a RPC with the same specifications as the bipolar transistor breadboard of task II, using MOSFETS instead of bipolar transistors as the main power switch.
2. Use at least two MOSFETS in series and as many in parallel as required.
3. Follow same test procedure as for the bipolar breadboard.

7.2 Breadboard Design and Test (Figure 7-1)

A breadboard using international rectifier IRF 350 power MOSFETS was designed and evaluated. These transistors are rated 400 volts and the $R_{DS\text{-}on}$ is typically .3 ohm. Two banks were connected in series with four transistors in parallel in each bank. Twenty-five Siemens BUZ54 1,000V devices with $R_{DS\text{-}on}$ of two ohms were placed on order. With 12 transistors in parallel, the voltage drop would be eight volts at 25 amperes. This is somewhat higher than desired, but the combined voltages of the two banks would be 2,000 volts. Fault testing could be done with little danger of damaging the transistors. Some testing could be done with 25 transistors in parallel to make a 1,000V bank. The full load voltage drop would be two volts. This is quite acceptable.

7.2 Breadboard Design and Test (Figure 7-1) (Continued)

Initial testing was done with the IRF 350 and the results of this investigation will be reported first. The schematic is shown in figure 7-1. Much of the circuit is the same as for the bipolar unit. However, the power switch drive and power switch operate entirely differently. These will be explained below.

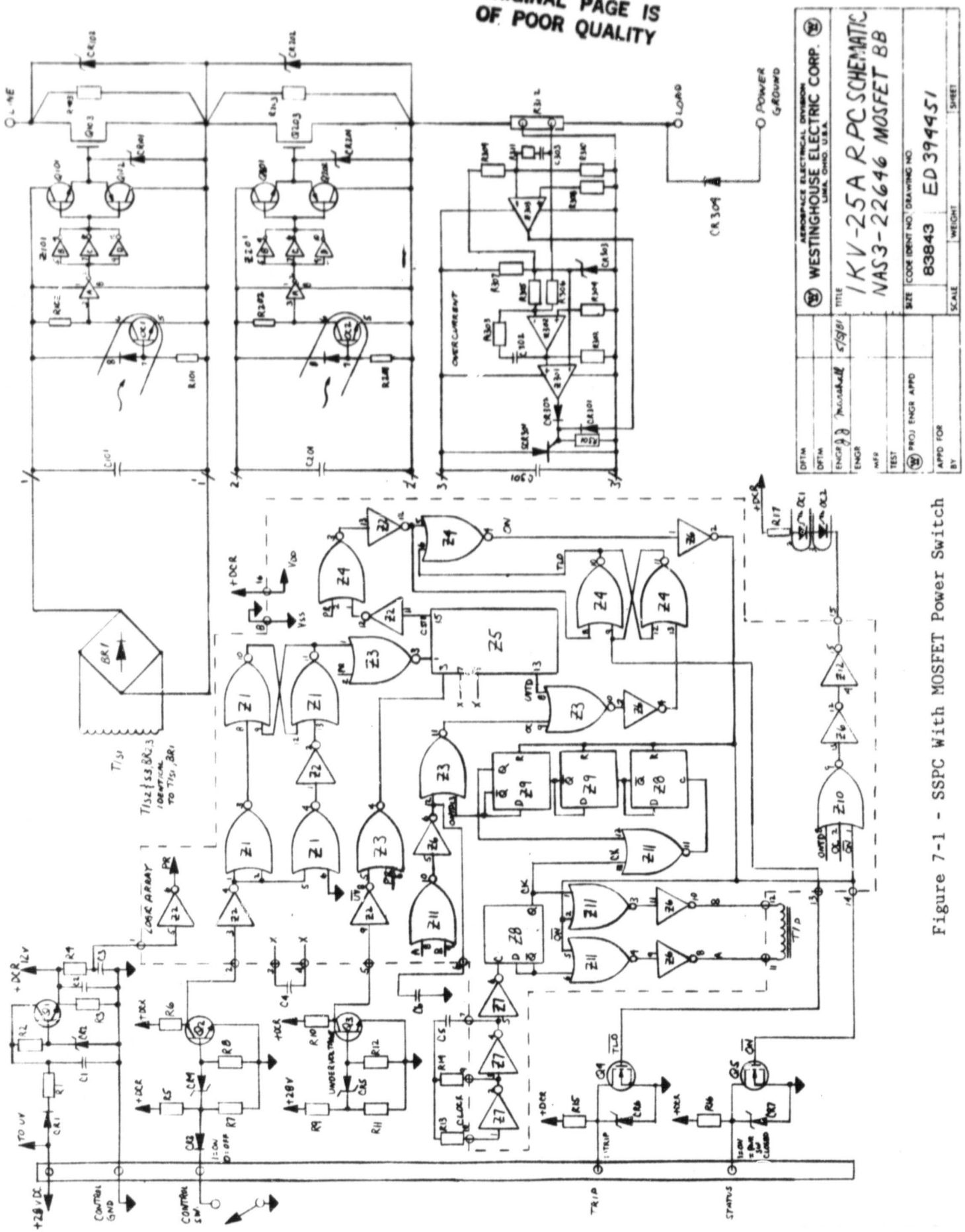


Figure 7-1 - SSPC With MOSFET Power Switch

Table 7-1

MOSFET Breadboard NAS3-22646 Logic Circuit Parts List

CR1	Diode IN4001
CR2	Zener Diode 13V
CR3	Diode IN4148
CR4, 6, 7	Zener Diode 5.1V
CR5	Zener Diode 8.2V
C1	Capacitor 8.2 µF Tantalum
C2	Capacitor .47 µF
C3	Capacitor .068 µF Ceramic
C4	Capacitor 4700 PF Tantalum
C5	Capacitor 47 PF Ceramic
C6	Capacitor 82 PF Ceramic
OC1, 2	Optocoupler HP 6N136
Q1	Transistor 2N3700
Q2, 3	Transistor 2N2222A
Q4, 5	Transistor 2N6660
R1	Resistor 20 Ohm
R2, 7	Resistor 3K
R3, 15, 16	Resistor 10K
R4	Resistor 15K
R5	Resistor 1.5K
R6, 10	Resistor 82K
R8, 12	Resistor 47K
R9, 11	Resistor 20K
R13	Resistor 100K

Table 7-1

MOSFET Breadboard NAS3-22646 Parts List Logic Circuit

(Continued)

R14	Resistor 180K
R17	Resistor 470 Ohm
T1	Transformer: Core 80613-½F, 160 Turns, #36 Wire, Quadfilar
Z1, 3, 4, 11	Quad 2 Input NOR
Z2, 6, 7, 12	Hex Inverter
Z5	Hex Bounce Eliminator
Z8, 9	Dual "D" Flip-Flop
Z10	Dual 3 Input NOR

Table 7-2

Drive and Power Circuit Parts List

BR1, 2, 3	Full-Wave Bridge FSA2705
CR101, 201	Zener Diode 12V
CR102, 202	Zener Diode, Combination 1,100V
CR301, 302	Diode, VSK 130
CR303	Zener Diode, 1.22V Reference
CR304	Diode, Freewheeling
C101, 201, 301	Capacitor .068 µF Ceramic
C302	Capacitor 1.0 µF Tantalum
C303	Capacitor 6800 PF Ceramic
Q101, 201	Transistor NPN 2N2219
Q102, 202	Transistor PNP 2N2904
Q103, Q203	Power MOSFET
R101, 103, 201, 203, 302	Resistor 1 Megohm
R102, 202	Resistor 47K
R301	Resistor 510 Ohm
R303	Resistor 105K
R304	Resistor 12K
R305	Resistor 255K
R306	Resistor 12.7K
R307	Resistor 10K
R308, 310, 311	Resistor 4.99K
R312	Shunt 50 MV
SCR301	Silicon Controlled Rectifier GB200
Z101, 201	Hex Inverter MC14049

Table 7-2

Drive and Power Circuit Parts List

(Continued)

Z301, 303	Comparator LM111
Z302	Operation Amplifier CA3130

7.2.1 Power Switch Drive

The power switch drive consists of a CMOS oscillator operating at one half the frequency (approximately 44 KHz) of the clock which consists of Z7, R13, R14, and C5.

The oscillator drive T1 isolates the logic from the power switch. At turn-on, the Z6A output goes low allowing the oscillator to start up by unlocking Z11A and Z11B. Actual turn-on is inhibited however by the ON time delay consisting of a string of three "D" flip-flops. During this time OC1 and OC2 are conducting, clamping the power switch gate drive off. After the time delay is complete the optocouplers are shut off allowing drive voltage to be applied to the power switch gate. On turn-off, the optocouplers are turned on and the gate of the power switch discharged through Q102, 202.

7.2.2 Power Switch

The power switch consists of Q103A-D and Q203A-D in a "four in parallel, two in series" combination. R103 and R203 force voltage sharing between the two sections in the OFF state. Zener diode strings CR102A-D insure that the transistor's breakdown voltages are not exceeded. At turn-on, Q101, 201 are turned on applying drive voltage to the gates through R104, 204 and R106A-D. Turn-on time is determined by the RC time constant of this resistance and the gate capacitances of the power switch transistors. At turn-off, PNP transistors Q102, 202 turn on clamping the power switch gates to the source, removing drive and shutting the RPC off.

7.2.3 Discussion of Results

Because a series combination of transistors is being pursued, turn-on and turn-off tracking is a concern. It is also important that the individual drain/source voltage ratings not be exceeded. Because faults must be cleared rapidly, a drive circuit was developed that operates at under half a microsecond at turn-off. This is accomplished by providing a low impedance path through Q102 to discharge the MOSFET gate capacitance. A similar low impedance charging path through Q101 is available for rapid turn-on. By using optocouplers in the logic, the turn-on and turn-off functions are performed independently of the rise and fall of the drive oscillator. The ON time delay (Z9), used to prevent overcurrent trips while the oscillator is turning on, is also used to trigger the gate drive optocoupler to turn on the MOSFET after full drive voltage is reached, rather than allowing the gate voltage to ramp up with the drive voltage. Because the overcurrent sensing circuit is separated from the drive circuits, the same optocouplers are used to transfer the trip information to the drive circuits, bypassing the slow decay of the drive supply. The oscillator transformer can be shorted by SCR301 very rapidly and that information sensed by Z11 at points on the logic side A and B, but capacitors C101 and C201 are not rapidly discharged by this action; hence, the optocouplers are used to provide timely trip information.

Other gate drive designs were evaluated in an effort to simplify the circuit and reduce the number of parts required. Consideration is given to the adaptability of the design to hybrid packaging.

7.2.3 Discussion of Results (Continued)

Because it is understood that the series gating technology development is the primary thrust of the MOSFET design, attempts to achieve the specified current and voltage levels will be made after that development is essentially complete. Current, voltage, and switch drop will be considered and trade-offs evaluated.

The MOSFET design was built and low voltage testing was begun. Oscillation of the gate voltage on turn-off probably due to coupling through the MOSFET inherent gate-to-drain and gate-to-source capacitance was attacked by trying to provide a drive circuit with a low output resistance. The drive circuit is powered through a CMOS oscillator because of the lower power requirements for gating MOSFETS. However, as parallel switches are added, the drive load may increase sufficiently so as to require a transistor oscillator similar to the Royer oscillator used in other RPC designs.

7.2.3 Discussion of Results (Continued)

As it is desirable to provide a fast turn-on and turn-off, Q101, Q201 and Q102, 202 are used to insure a low impedance charging path. Since the MOSFET gate input capacitance is fixed, the turn-on time can be reduced by reducing the impedance in the charging path (RC time constant). It was observed that by applying the drive supply directly to the gate through Q101, the resultant surge of current depressed the drive supply primary sufficiently so as to cause an overcurrent trip to be sensed in the logic circuit. Consequently, a current limiting resistor was inserted in series with the Q101 collector to prevent this false tripping. Additionally, resistors were added in series with each gate as recommended by the semiconductor manufacturer in order to prevent possible oscillations. These measures lengthened turn-on time somewhat, but not to the point of causing problems with the safe operating area of the MOSFETS.

Because the devices used exhibit a 400V drain-to-source breakdown voltage, the practical operating voltage for the RPC would be somewhere under 800 volts. With four in parallel and two in series, the observed on resistance was about .125 ohm allowing a 15A unit for a switch drop of under two volts. The RPC was tested at 400 volts and five amps with some testing at 600 volts.

7.2.3 Discussion of Results (Continued)

As more MOSFETS are added in parallel to achieve higher currents while maintaining a low switch drop, the gate drive requirements increase, triggering a series of interlocking trade-off considerations. First, the turn-on current requirements for a parallel string may strain the capability of the CMOS oscillator. Additionally, the drive current limiting resistors previously mentioned cannot be made very large because to do so would make the turn-on unacceptably slow. While the CMOS oscillator may still have sufficient driving capability, the overcurrent trip circuit detection scheme used may cause problems. To avoid a nuisance trip during turn on, the circuit must distinguish between a normal turn-on transient and an overcurrent trip. Both conditions overload the CMOS oscillator. Since the turn-on transient is only a momentary overload, the trip lockout circuit could be inhibited for sufficient time to allow the CMOS oscillator to recover from the turn-on transient. The "inhibit time" used to allow a normal turn-on is now a delay time in operation of the overcurrent protection circuit. This would probably be satisfactory for all conditions except for a short circuit occurring during the on state.

A possible solution would be to use a transistor driven oscillator to provide additional capacity. This would increase circuit size and weight which is undesirable from a hybrid packaging viewpoint. The simplicity of a CMOS drive oscillator is attractive for a lightweight space application.

7.2.3 Discussion of Results (Continued)

Another solution to the problem of false overcurrent trips on turn-on would be to convey trip information for turn-off directly to the drive circuit to shut off the switch while still allowing the drive oscillator to be shut off by the slower detection of the shorted transformer as before. This method would add complexity and require additional voltage isolation devices such as optocouplers.

Given the fixed input capacitance of a power MOSFET, there is a limit on the number of devices that may be operated in parallel with a relatively low power drive circuit. Beyond that limit a higher power drive is necessary. Because the drain to gate capacitance interacts with the drive voltage, higher drain to source voltages also increase drive requirements. Although the actual steady state drive power needed is very low, the momentary turn-on capability must be present in order to turn on the switch rapidly and safely.

In the overall analysis as compared with a single switch element, the series connection requires synchronization of the drive circuits so that each device is protected from unbalanced and potentially harmful conditions. Furthermore, the synchronization must not depend heavily on matched circuit components that may vary with temperature. Overcurrent trip circuits must act on both switch elements and because the voltage references on each element are different, isolation must be provided.

7.3 New Breadboard Design, Discussion

Because of the problems occurring with the input capacitance of the power MOSFETS, it became clear that the gate drive circuits would never be satisfactory for the transistors in parallel switching a high bus voltage. A low impedance power supply/gate drive circuit was needed. Siemens informed Westinghouse that the 1,000V devices were not available as yet and recommended the BUZ-45, a 500V device for immediate delivery. A new circuit was designed to have the following improvements.

1. Low impedance gate drive circuit.
2. Controlled ramp gate voltage for turn-on.
3. Gate drive circuits to be individually trimmable to get simultaneous switching within a few nanoseconds during both turn-on and turn-off.
4. Faster acting overcurrent trips.
5. Overcurrent protection circuit to have steady state load current biasing of the fast trip section. This would result in faster response to sudden short circuits occurring while in the ON state.

To accomplish the first of these objectives, the low voltage side of the bipolar circuit was followed with only very few changes. Since it was important that the power supply/logic/Royer work the first time and the exact requirements were not known, no effort was made to miniaturize the power supply, transformer, and Royer switching transistors. This resulted in a power source much larger and having much lower impedance than necessary.

7.3 New Breadboard Design, Discussion (Continued)

Improvements #2 and #3 were obtained by changing the CMOS gate (Z101, Z201) and bipolar transistors (Q101, Q102, A201, Q202) of figure 7-1 to operational amplifiers driving MOSFETS. This allows a controlled ramp for turn-on (adjustable with a capacitor) and a sudden turn-off. The emitter-base resistors of the optocouplers can be selected to get simultaneous turn-on. The fast acting turn-off operational amplifiers can be "compensated" with a few picofarads to slow the faster one and obtain simultaneous turn-off.

Improvement #4 was obtained by adding an optocoupler between the overcurrent protection circuit and the logic circuit. "Tripping" is accomplished by a signal directly into the logic which shuts off both drive circuits simultaneously. Subsequent to the procurement of the BUZ-45 devices, IRC listed their IRF 450. They should be a 50% improvement over the BUZ-45 since they are rated at 500 volts and have $R_{DS\text{-}on}$ = .4 ohm (BUZ-45, $R_{DS\text{-}on}$ = 0.6). All testing was done with the BUZ-45, but the IRF 450 should be a direct substitution with a lower forward voltage drop. To accomplish Improvement #5, another operational amplifier was added in the front end of the overcurrent protection circuit. The reference voltage on the inverting input of Z303 is reduced directly proportional to load current from no load to full load. A detailed description of operation and results are given below.

7.4 New MOSFET Breadboard Description and Test Results (Figure 7-2)

Refer to the logic/drive circuit shown in figure 7-2. Note that circuit designators may be different than corresponding components on previous circuits.

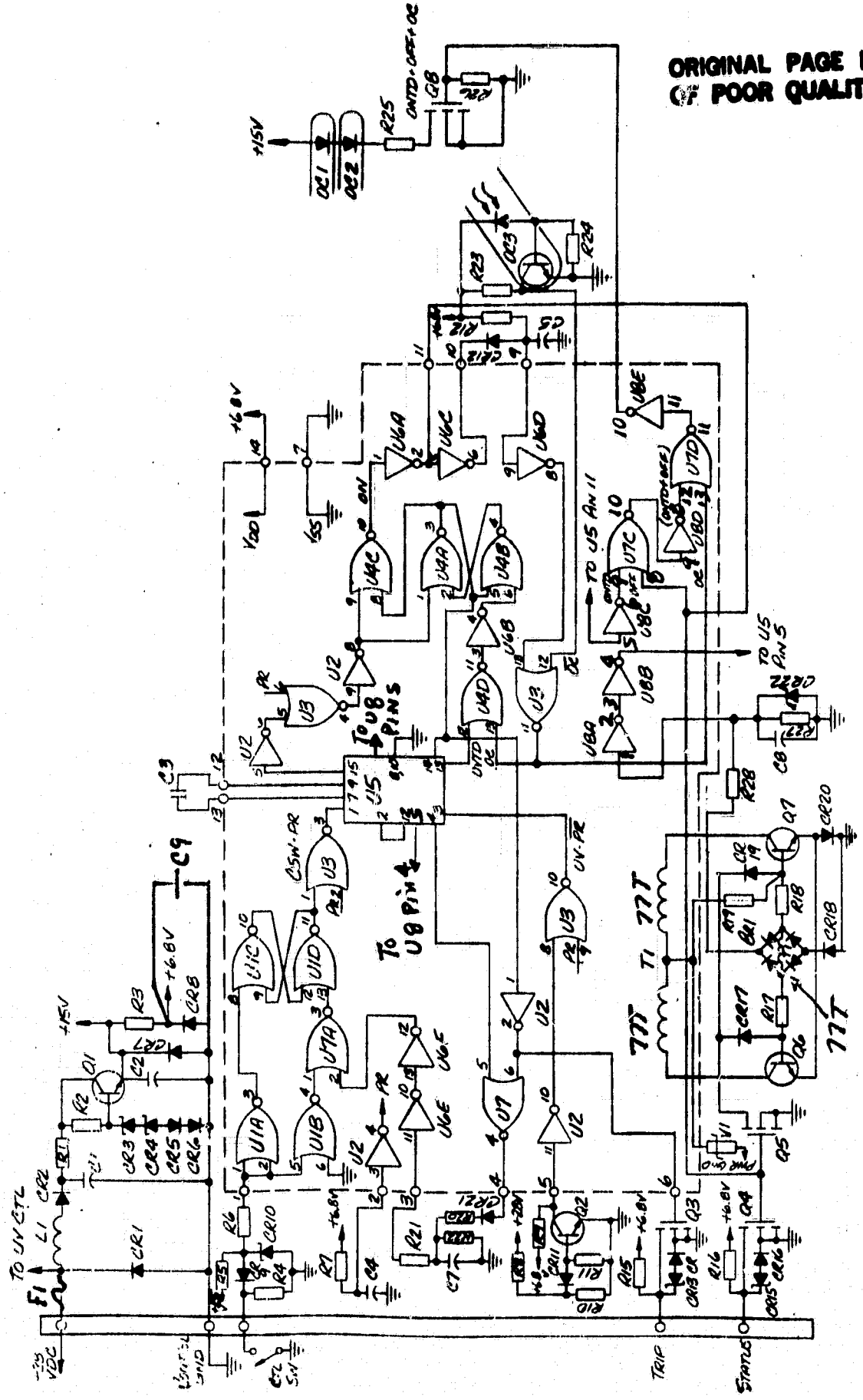


Figure 7-2 - Logic/Drive Circuit

Table 7-3

New Logic/Power Supply Parts List

C1	22 µF/100V Tantalum
C2	2.2 µF/35V Tantalum
C3	4700 PF Ceramic
C4	.068 µF Ceramic
C5	.068 µF Ceramic
C7	2.2 µF Tantalum
C8	.068 µF Ceramic
C9	3.3 µF Tantalum
F1	½A Picofuse
BR1	4-IN4148
CR1	IN4007
CR2	IN4007
CR3	8.2V/400 MW
CR4	5.6V/400 MW
CR5	IN4148
CR6	IN4148
CR7	18V/400 MW
CR8	6.8V/400 MW
CR9	IN4863
CR10	5.6V/400 MW
CR11	8.2V/400 MW
CR12	IN4148
CR13	LED, Red
CR15	LED, Green

Table 7-3

New Logic/Power Supply Parts List

(Continued)

CR17	IN4148
CR18	IN4148
CR19	IN4148
CR20	IN5416
CR21	IN4148
CR22	5.6V/500 MW
L1	2.4 µH
OC1	6N136 Optocoupler
OC2	6N136 Optocoupler
OC3	6N136 Optocoupler
Q1	2N3773
Q2	2N2219A
Q3	2N6660
Q4	2N6660
Q5	2N6660
Q6	SDT4925
Q7	SDT4925
Q8	2N6660
R1	5Ω CC 1W
R2	470Ω CC ½W
R3	820Ω CC
R4	4.7K CC
R5	2K CC
R6	49.9K MF

Table 7-3

New Logic/Power Supply Parts List

(Continued)

R7	432K MF
R8	24.9K MF
R9	47K MF
R10	24.9K MF
R11	4.7K CC
R12	47K CC
R15	910Ω CC ½W
R16	910Ω CC ½W
R17	820Ω CC ½W
R18	820Ω CC ½W
R19	24K CC
R20	2K CC
R21	10 Megohm CC
R22	10 Megohm CC
R23	47K CC
R24	220K CC
R25	510μ CC
R26	47K CC
R27	220K CC
R28	220K CC
T1	50063-2A (Magnetics, Inc.)

Table 7-3

New Logic/Power Supply Parts List

(Continued)

U1	MC14001BAL
U2	MC14069BAL
U4	MC14001BAL
U5	MC14490
U6	MC14069BAL
U7	MC14001BAL
U8	MC14069BAL

7.4 New MOSFET Breadboard Description and Test Results (Figures 7-2 Through 7-24) (Continued)

A 28 VDC supply (0.25A maximum) is to be connected between the +28 VDC and control ground terminals. This voltage can vary from 18 volts to more than 35 volts. Capacitor C1 does some filtering to prevent current spikes from causing problems on the line. Regulated voltage supplies of 15 and 6.8 are provided. The 6.8V supply is used for all logic gates and low level functions. The 15V supply is applied to the center tap of the Royer oscillator transformer and to power the optoisolators OC1 and OC2. Normal turn-on and turn-off are accomplished by the control switch. U5 is a CMOS IC which is a digital time delay of the contact bounce eliminator type. The control switch time delay, on the order of seven milliseconds, is a function of C3 and is provided for both turn-on and turn-off.

7.4 New MOSFET Breadboard Description and Test Results (Figures 7-2 Through 7-24) (Continued)

Operation of the Royer oscillator is controlled by FET Q5. When in the conducting state, this transistor effectively clamps the bases of Q6 and Q7 switching transistors to the control ground to divert base drive current from the transistors to the control ground. This prevents conduction and prevents the oscillator from functioning. To turn the oscillator on, the gate of Q5 is clamped to control ground by U6A. This turns Q5 off and allows base drive starting current to flow through R19 and through Q7 emitter-base. This small amount of current causes Q7 to turn on and allow current to flow from the center tap through the right side of the winding and through Q7 emitter collector to control ground. This change in current induces a voltage in all windings of the transformer including the Royer drive winding (shown inside the BR1 bridge rectifier). The induced voltage turns on Q6 and turns Q7 off. Oscillations build up until equilibrium is reached at approximately 3.5 KHz (frequency is proportional to voltage).

7.4 New MOSFET Breadboard Description and Test Results (Figures 7-2 Through 7-24) (Continued)

During oscillator buildup, the gate of Q8 is held high by U8E. This allows Q8 to conduct and OC1 and OC2 are turned on. Two identical banks of FETs are operated in series to double their voltage rating. Refer to the bank drive schematic (figure 7-3). The Royer oscillator is functioning and OC1 is ON. This clamps the collector (pin 6) to the emitter (pin 5). This clamps pin 2 of U102 and pin 3 of U101 to the negative rail. These actions keep Q101 turned off and Q102A-D conducting. Therefore, the power switch Q104A-J is open. The purpose of this delay is to allow sufficient time for the power supply voltage (+12 volts) to build up sufficiently to accomplish two purposes. First, operational amplifiers U101 and U102 must have sufficient voltage for proper operation when the power switch turns on, and second, the voltage should be greater than five volts when Q101 is turned on and Q102 is turned off. In approximately 25 milliseconds, C8, R27, R28, U8A-D and U5 allow invert gate U8E to go low which turns off Q8 and removes the clamping at pin 6 of OC1. Pin 2 of U102 is driven high and Q102A-D releases the gate circuit of Q104A-J. In addition, pin 3 of U101 goes high and turns on the operational amplifier. C101 applies feedback to U101 which causes the gate drive bus voltage (junction of R108, Q101, and Q102) to rise in a controlled ramp. The rate of rise is controlled by C101. C103 furnishes a small amount of "compensation" to reduce oscillations. The controlled turn-on condition is shown in figure 7-4. V_{Bank} is the gate drive bus voltage for Q104A-J at point A.

7.4 New MOSFET Breadboard Description and Test Results (Figures 7-2 Through 7-24) (Continued)

The gates of each power transistor are connected to this bus through a 20 ohm resistor. Figure 7-5 shows the drain/source voltage switching has been completed in less than 30 microseconds, but the load current is only up to 80% of its equilibrium value in 65 microseconds. Figure 7-6 shows the turn-on condition at 400 volts.

The normal turn-off and turn-off during a fault use the same switching on the breadboard. A slower turn-off could be used for a commanded OFF condition. This would involve the addition of a few more parts to each bank drive. During operation, pin 11 of U3 (figure 7-16) is clamped low and pin 11 of U7D is high with pin 10 of U8E low. OC1 and OC2 are not conducting. When the control switch is opened, pins 1 and 2 of U1A and pin 5 of U1B go high and after a delay of approximately seven milliseconds, pin 11 of U7D goes low. This caused changes in the bank drives which are the reverse of turn-on. When the collector (pin 6) of OC1 (figure 7-3) is clamped to the -3V rail, operational amplifier U102 is suddenly driven positive (pin 6) and Q102A-D clamps the gate drive bus point A to the common terminal which causes the gates of Q104A-J (ten parallel FETs) to discharge and the drain/source voltage to rise. This entire sequence of events takes place within one half microsecond after the turn-off signal reaches U7D. Figure 7-7 shows a normal turn-off from 200 volts. U102 is a high speed operational amplifier (RCA3130BS) and is uncompensated. Q102-A-D consists of four 2N6661 FETs in parallel to lower the drain/source on resistance and clamp point A solidly to common during the turn-off transient.

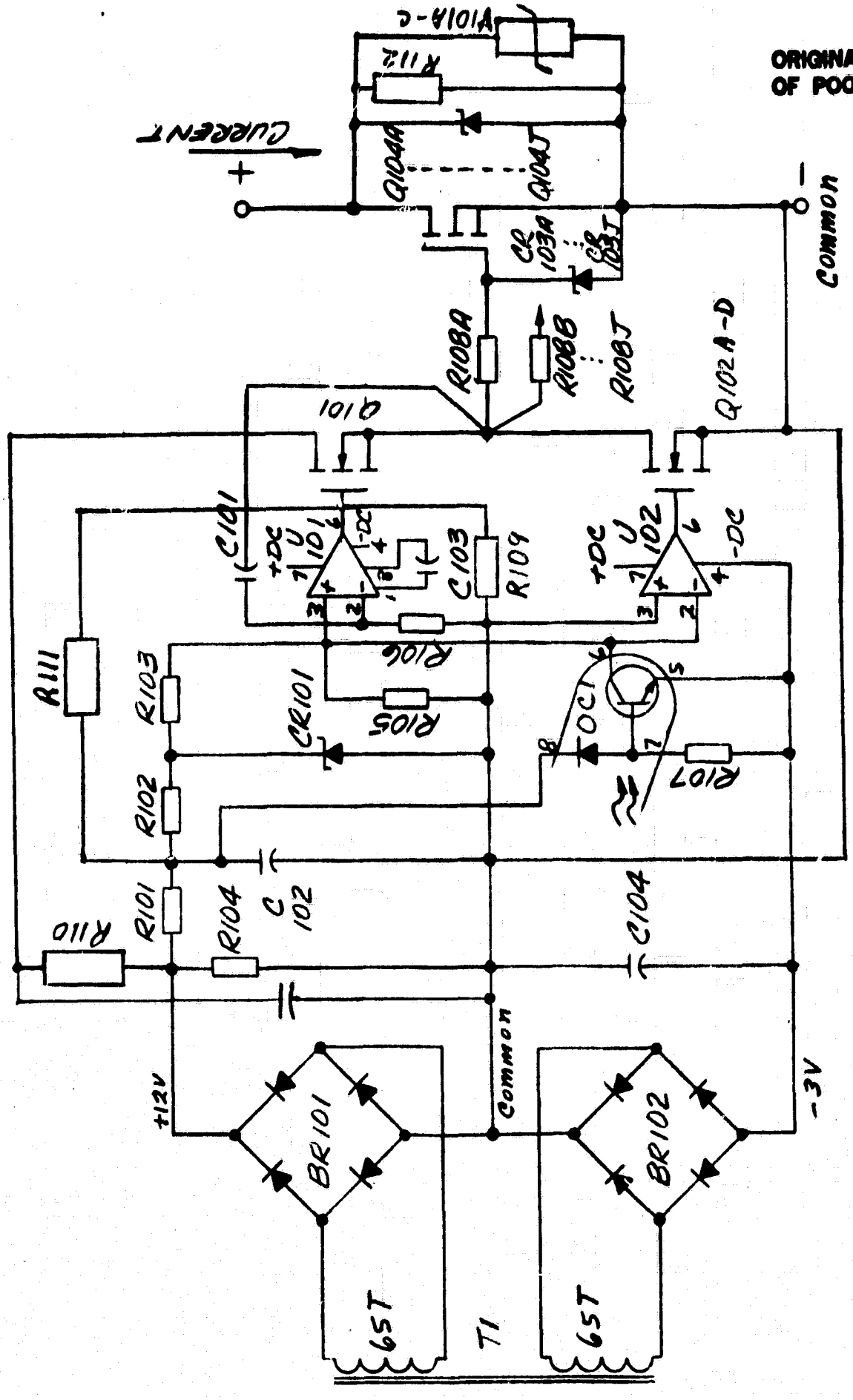


Figure 7-3 - Bank Drive

Table 7-4

Bank Drive Parts List

Designator	Description
BR101	4 - IN4007
BR102	4 - IN4007
C101	.01 µF/50V Ceramic
C102	1 µF/50V Ceramic
C103	10 PF/50V Ceramic
C104	12 µF Tantalum
C105	3.3 µF Tantalum
CR101	ICL8069 1.22V Reference
CR103A-J	10V/400 MW
CR104-A-G	56V/3 Watt
OC1	6N136 Optocoupler
Q101	2N6661
Q102A-D	2N6661
Q104A-J	BUZ45, Siemens
R101	100Ω CC
R102	20K CC
R103	26.7K MF
R104	10K CC
R105	10K MF
R106	1K MF
R107	121K MF (301K) on Bottom Bank
R108	20Ω CC
R109	2.4K CC

Table 7-4

Bank Drive Parts List

(Continued)

Designator	Description
R110	220Ω CC
R111	3K CC
R112	91K CC ¼ Watt
U101	CA3130BS, RCA
U102	CA3130BS, RCA
V101A-C	Varistor V150CA10A (GE)

ORIGINAL PAGE
BLACK AND WHITE PHOTOGRAPH

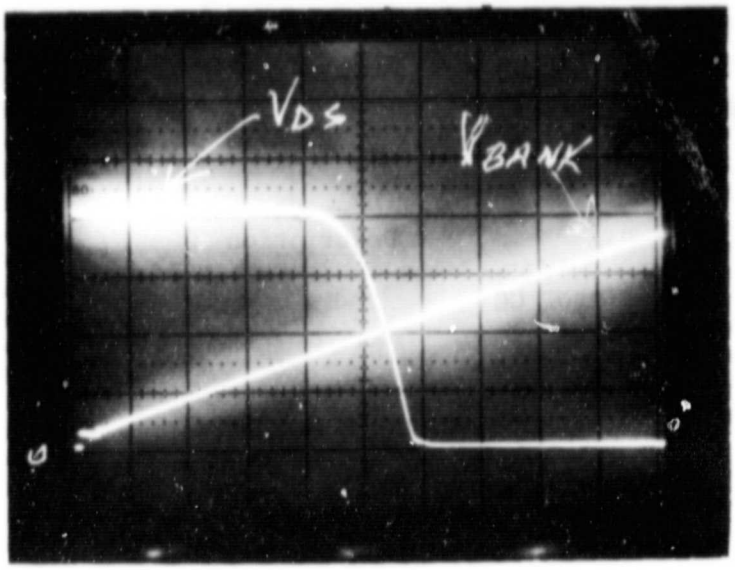


Figure 7-4 - Turn-On
V_{DS} = 200 at 25V/Division
I_{Load} = 25A
V_{Bank} = 2V/Division
Horizontal 20 µS/Division

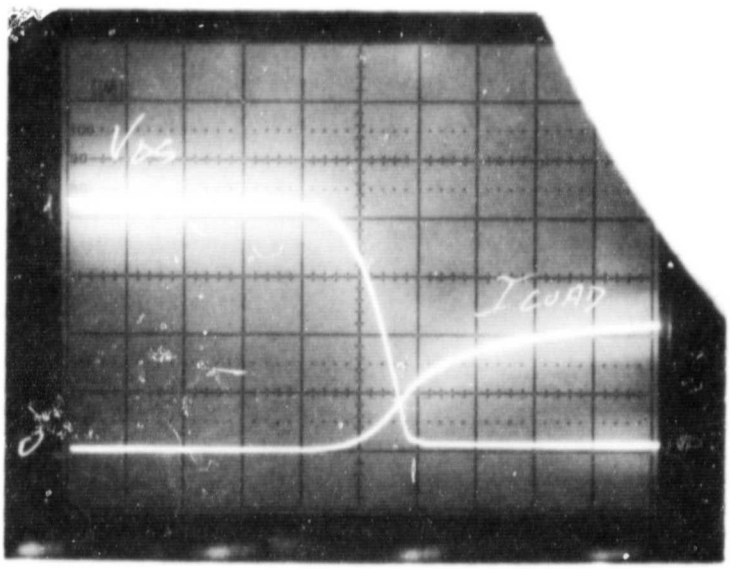


Figure 7-5 - Turn-On
V_{DS} = 200 at 25V/Division
I_{Load} = 25A at 10A/Division
Horizontal 20 µS/Division

ORIGINAL PAGE
BLACK AND WHITE PHOTOGRAPH

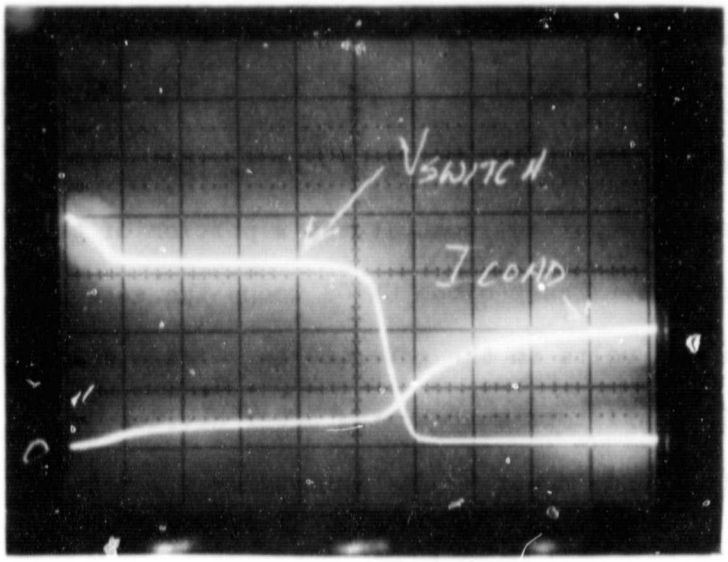


Figure 7-6 - Turn-On
$V_{Switch} = V_{DS} = 400V$ at 100V/Division
$I_{Load} = 25A$ at 10A/Division
Horizontal 20 μS/Division

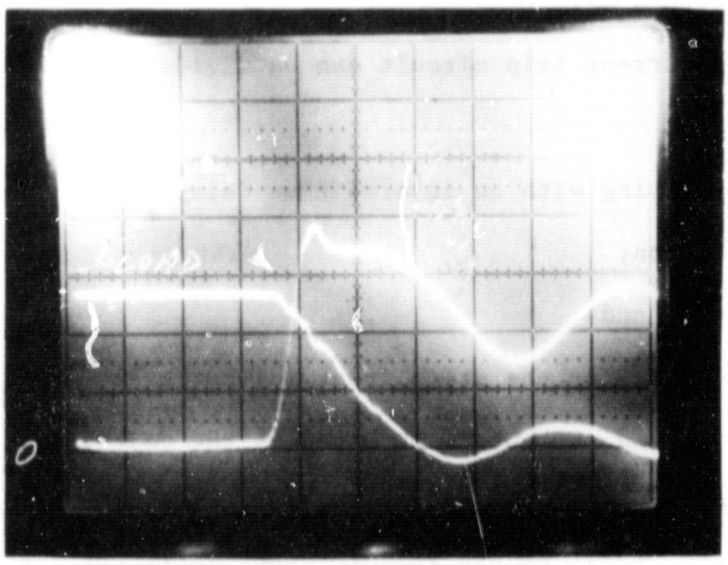


Figure 7-7 - Turn-Off
$V_{DS} = 200V$ at 100V/Division
$I_{Load} = 25A$ at 10A/Division
Horizontal 200NS/Division

7.4 New MOSFET Breadboard Description and Test Results (Figures 7-2 Through 7-24) (Continued)

The rise in drain voltage requires a charging current in the drain/gate capacitance and this current constitutes a portion of the current through R108 to common. Zener diode CR103 keeps the gate current from rising above ten volts so the gate/source voltage stays within safe limits. Q102 transistors must be the newer devices without protective gate to source Zener diodes internally. A direct path would result through the Zener to the output (pin 6) of U102 and on to the -3 volt rail during the off state. It must be appreciated that point A is clamped to common before U101 has acted. Thus, Q101 is momentarily shorted through R110 during turn-off. The compensation and voltage swing of U101 slow down its operation more than can be tolerated during a turn-off. For this reason, point A is clamped to common before Q101 has turned off.

Operation of the overcurrent trip circuit can be divided into four basic functions:

1. normal overcurrent tripping with an inverse time delay;
2. actual tripping operation;
3. steep front of current; and
4. modification of threshold for the steep front instant trip.

A voltage proportional to load current is obtained as the voltage across RSH. This current shunt is chosen for 50 millivolts with full load current (25 amperes). Refer to the circuit shown in figure 7-8. Normal overcurrent tripping with an inverse time delay uses operational amplifiers U303A and B and associated components.

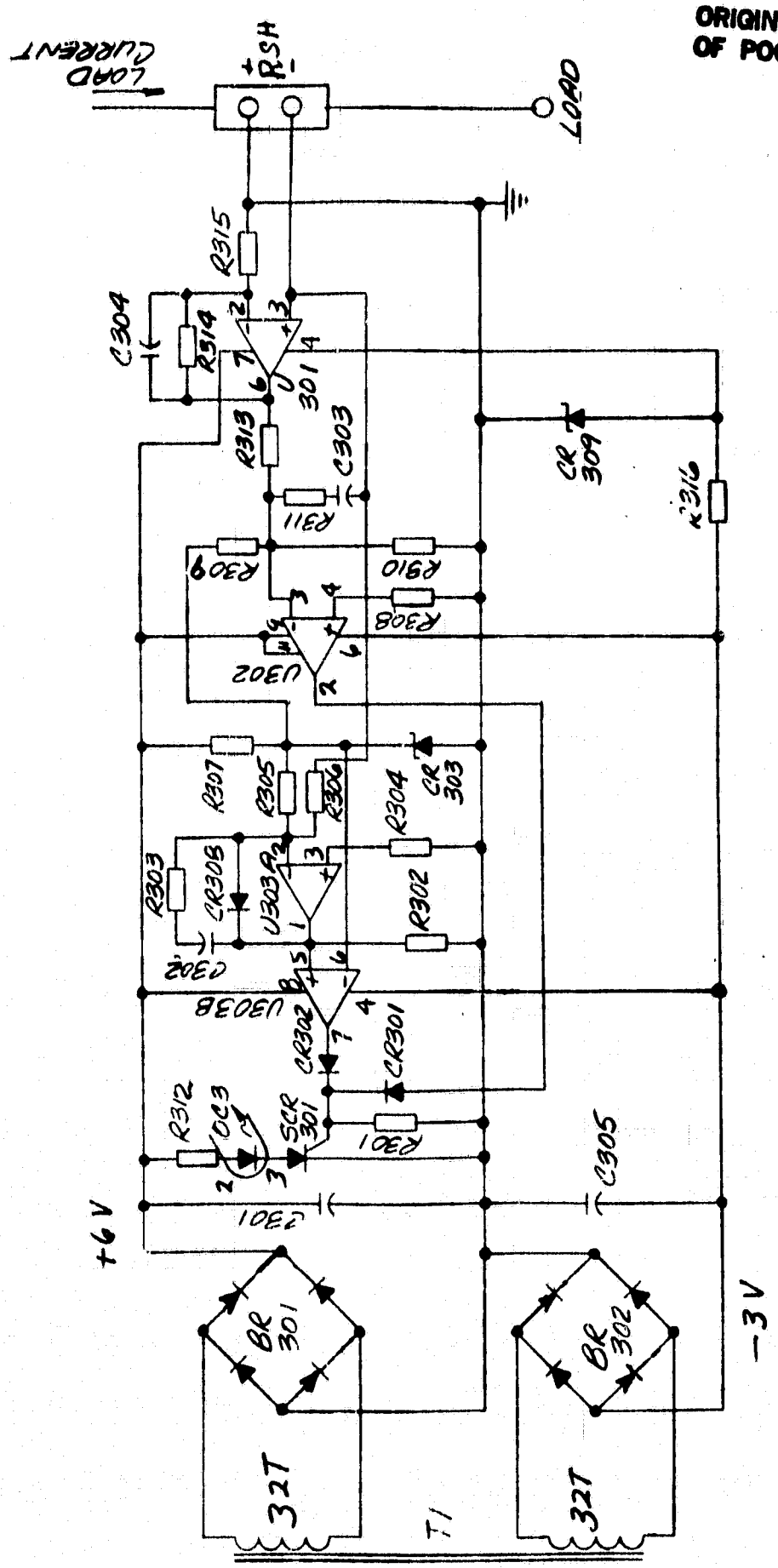


Figure 7-8 - Overcurrent Trip Circuit

7.4 New MOSFET Breadboard Description and Test Results (Figures 7-2 Through 7-24) (Continued)

CR303 is a 1.22V precision voltage reference which provides a bias current that subtracts from the load current signal from RSH and R306 at the non-inverting input of pin 2 of V303A. For load current the R305 bias current exceeds the R306 load current signal and the U303A output voltatge pin 1 will be at a low level. At high values of load current, current (microamps) will flow out of pin 1 of U303A to charge C302 through resistor R303. The capacitor gives a time integration of the input current above 1.2 PU and pin 1 voltage of U303A continues to rise until the voltage at pins of the U303B comparator reaches the CR303 reference voltage level at pin 6. Thus, when the output voltage of the integrator (pin 1 of U303A) exceeds 1.22 volts, pin 7 of U303B goes high, firing SCR301 causing conduction of OC3. When the phototransistor collector of OC3 (figure 7-2) is clamped to control common, pin 12 of NOR gate U3 goes low causing the OC trip signal at pin 11 to go high (since input pin 13 is low). The OC trip signal causes the output signal at pin 11 of U7D to go low and the output of U8E high providing gate drive to Q8 thereby turning on OC1 and OC2. Turn-off proceeds the same as described before. R303 is included in the integrating circuit to lower the trip time at higher currents since the integrating current causes a voltage drop in R303. Thus, the voltage on pin 1 of U303A could rise rapidly since some of the voltage would appear across R303. R303 is chosen to give instant tripping if the current exceeds three per unit. Actual operation of this circuit takes several microseconds which is too slow for fault protection. If the power controller turns on into a short circuit, the current rises very rapidly.

7.4 New MOSFET Breadboard Description and Test Results (Figures 7-2 Through 7-24) (Continued)

The rate of rise of this steep front of current is limited by the circuit inductance, switching speed of the power controller, and the voltage/current characteristics of the source. If the inductance of the circuit is in the order of 20 microhenries, the rate of rise of current could reach in the order of 40 amperes per microsecond on an 800V system. The normal sequence of events would be for U303A, C302, and R303 to begin the integration process as the current passed approximately 30 amperes. Within two microseconds, the current would have passed 3 PU and pin 1 of U303A would have risen to 1.23 volts with most of it appearing across R303. A few microseconds later, pin 7 of U303B would be high enough to fire SCR301. By this time, the power switch, and perhaps components in the load circuits, would have been damaged.

There are two severe conditions that a SSPC must handle without degradation. The first of these is turning on into a short circuited load. This results in a rapidly rising current which is limited only by the switch voltage and inductance in the circuit. It is for this condition that U302 was added to initiate an "immediate" trip. U303 is much too slow to respond to steep fronts of current and would allow the current to reach 3 PU before it would go into the instant trip mode. Instant trip for U303 would still require several mircoseconds and the peak let-through current could be well above 3 PU unless some sort of current limiting is used. Current limiting was used on SSPCs developed on Contract Number NAS3-21755 by allowing the switching bipolar transistor to pull out of saturation.

7.4 New MOSFET Breadboard Description and Test Results (Figures 7-2 Through 7-24) (Continued)

If the current reaches a high peak, the turn-off must be slowed to reduce the peak voltages developed across the power switch by the decay of line current, e = -L(di/dt). The approach taken here is to sense these rapidly rising currents and use a high speed circuit to trip-off before the current reached 3 PU. The circuit should not be so sensitive as to give nuisance trips with normal fluctuations of current.

An explanation of the fast tripping overcurrent protection circuit can be simplified by drawing an equivalent circuit of the portion containing U302. Refer to figure 7-9. This portion of the circuit responds only to steep fronts of current by sensing the resulting high dv/dt developed across the current shunt. C303 can be considered a short circuit for these rapidly changing currents which allows V_{sh} to appear across R310 and R311 in series. Since these resistors are equal, one half of V_{sh} appears at U302. The polarity of this voltage is negative and, since it is applied to the inverting input of U302, the output of U302 (E_{02}) will be driven positive and fire SCR301 which turns on OC3. Since response to small changes is not desired, a positive voltage is established at pin 3 of U301 by CR303, R309, and R310. This positive reference voltage must be overcome by the negative V_{sh} voltage in order to drive pin 3 of U302 negative. By controlling this positive reference voltage on pin 3 of U302, the circuit can be made to respond to transient currents of any magnitude. It was decided that the trip should be initiated when the rapidly rising current reached 2 PU.

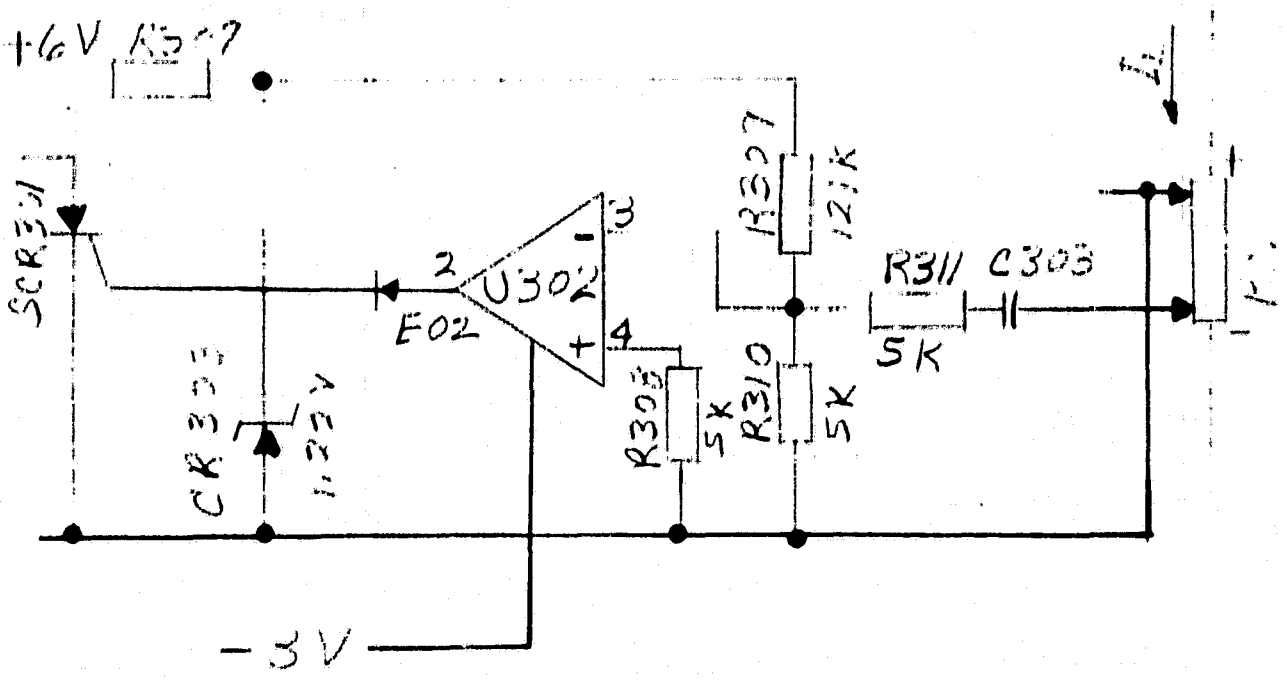


Figure 7-9 - Fast Trip Circuit

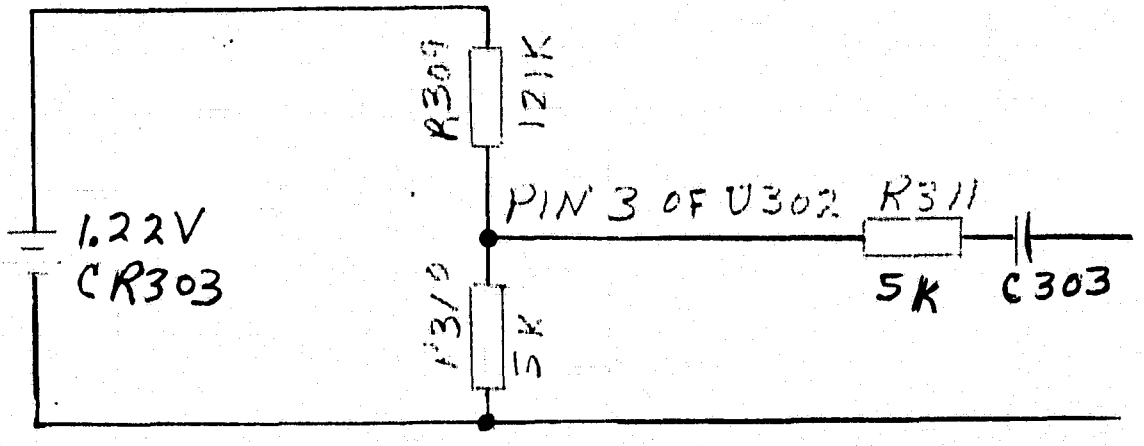


Figure 7-10 - Equivalent of Fast Trip Circuit

7.4 New MOSFET Breadboard Description and Test Results (Figures 7-2 Through 7-24) (Continued)

R309 and R310 were selected to give 48 millivolts (positive polarity) at pin 3 of U302. Since the current shunt R_{sh} is chosen to give 50 millivolts drop at rated current and this voltage is divided by R310 and R311, the voltage at pin 3 of U302 would be driven slightly negative (-2MV) when the current reached 2 PU. Figure 7-10 shows the equivalent circuit.

$$\frac{5K \times 1.22V}{121K + 5K} - \frac{5K \times 50\ MV \times 2\ PU}{10K} = -2\ MV$$

This is true only when the rate of rise of current is such that C303 is effectively a short circuit. The bipolar breadboard was made using this circuit.

Since U302 is a high speed (LM111, DIP) comparator, operation is very rapid. Figure 7-11 shows the load current and drain/source voltage as the power controller closes 200 volts into a short circuit. Note the smooth ramp-up of current to peak at 60 amperes (2.4 PU). If the rate of rise of load current was such that C303 was not an effective short circuit, pin 3 of U302 would see less than half of the shunt voltage and operation would be delayed until the voltage at pin 3 reached 50 millivolts. If the current rose more slowly, it would also rise less after the tripping voltage was reached and before the actual trip occurred. The limiting case is for a current rising so slowly that U302 does not respond at all and the protection is provided by U303. In this case, the current can reach 3 PU before a trip is initiated.

ORIGINAL PAGE
BLACK AND WHITE PHOTOGRAPH

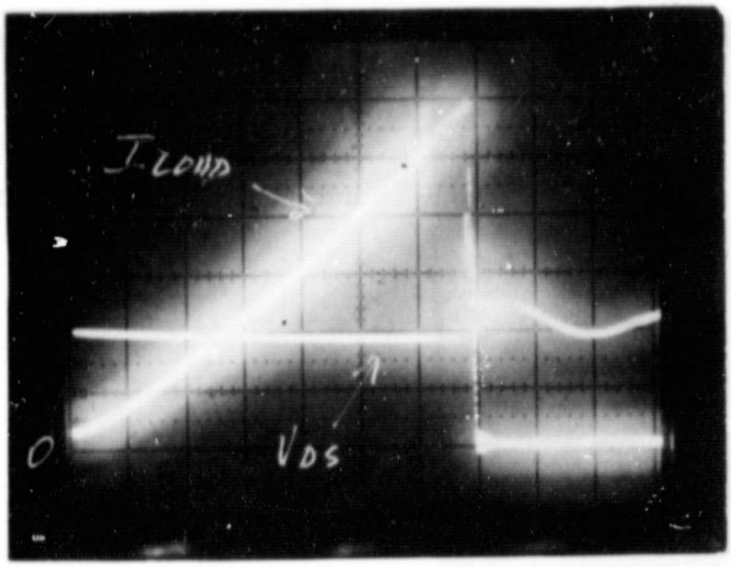


Figure 7-11 - Turn-On into Short Circuit
V_{DS} = 100V/Division
I_{Load} = 10A/Division
V_{Source} = 200V
Horizontal 10 µS/Division

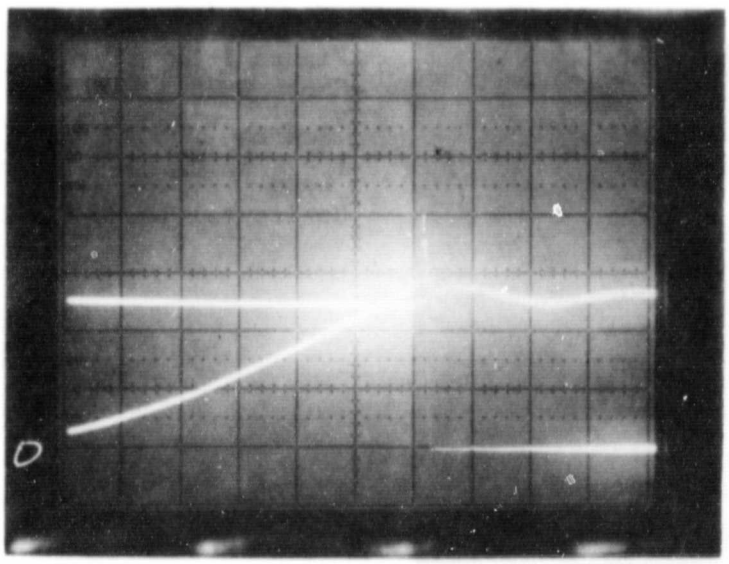


Figure 7-12 - Turn-On into Short Circuit
V_{Source} = 500 VDC at 200/Division
I_{Load} = 20A/Division
V_{Switch} = V_{DS} = 200V/Division
Horizontal 10 µS/Division

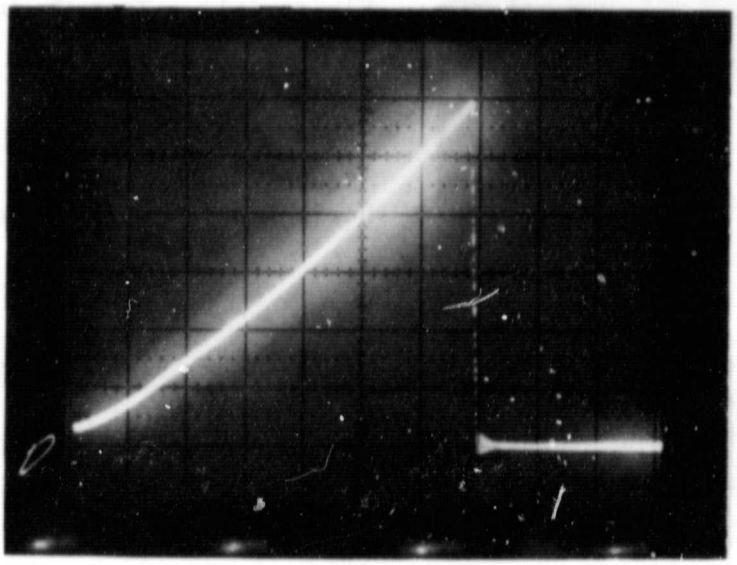


Figure 7-13 - Turn-On into Short Circuit
V_{Source} = 200V
I_{Load} = 10A/Division
Horizontal 10 µS/Division

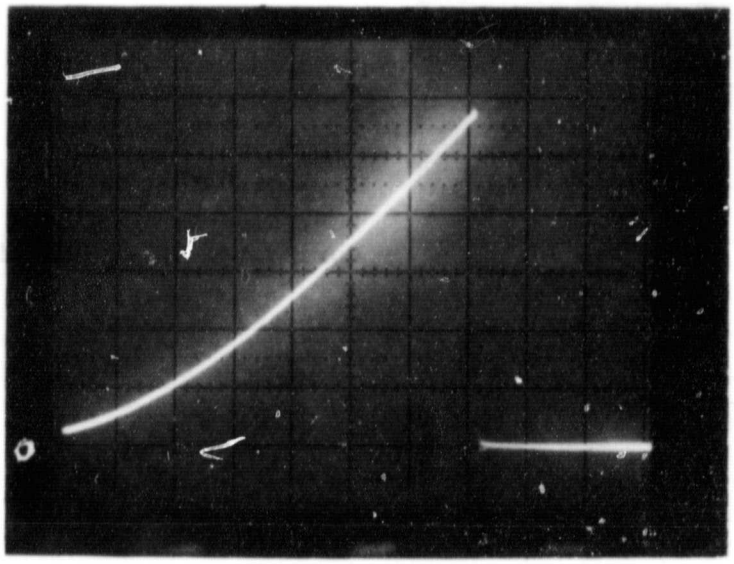


Figure 7-14 - Turn-On into Short Circuit
V_{Source} = 500 VDC
I_{Load} = 10A/Division
Horizontal 10 µS/Division

ORIGINAL PAGE
BLACK AND WHITE PHOTOGRAPH

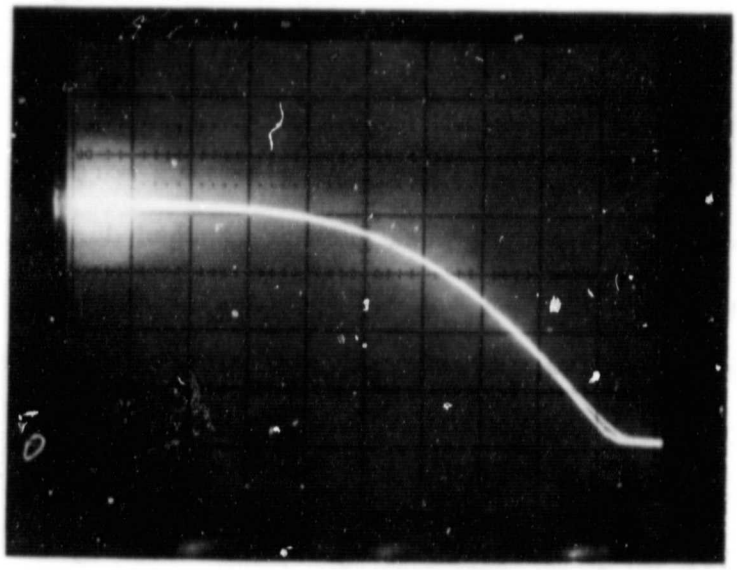


Figure 7-15 - Turn-On V_{DS} of Both Banks Superimposed
Vertical 50V/Division
I_{Load} = 25A
Horizontal 5 µS/Division

7.4 New MOSFET Breadboard Description and Test Results (Figures 7-2 Through 7-24) (Continued)

However, a current wave rising this slowly will not rise much more during the tripping operation. Thus, the peak current reached during turning on into a fault would be between 2.4 and perhaps 3.2 PU. Figure 7-12 shows the current and switch voltage while closing 500 VDC into a short circuit. A coaxial current shunt was used to obtain the sense voltage for the oscilloscope. Note the operation is almost identical to the 200V case, except for the voltage spike caused by Ldi/dt. Figures 7-13 and 7-14 show the current on the same scale and a direct comparison can be made. Operation is almost identical. Figure 7-15 shows the drain/source voltages of both banks superimposed during a normal turn-on into a 25A load. The release of OC1 clamp of pin 6 to the negative rail is used as a trigger for time zero.

The ability to turn on into a fault without damage to the line, load or switching device is a very important capability. However, it is not the most difficult task. The more difficult function is to clear a fault which occurs while the switch is in the ON condition. This could occur during normal operation and a sudden short circuit occurring at the terminals from "battle damage." In this case the load current could be at 1 PU before the short circuit and the rate of rise could be very rapid. An instant before the fault, the overcurrent protection is in a standby state with voltage at U303, pin 2 20% below the threshold and no current through R311-C303. As stated before, U303 cannot respond fast enough to protect against faults so the task falls to U302, but the current is at 1 PU before the fault and U302 cannot respond until the steep front voltage caused by a sudden change in current reaches 2 PU.

7.4 New MOSFET Breadboard Description and Test Results (Figures 7-2 Through 7-24) (Continued)

The change in current must be 2 PU because the shunt voltage is equally divided by R310 and R311 and the threshold at pin 3 of U302 is equivalent to 1 PU. Therefore, the current must reach 3 PU before U302 responds. This is assuming a 1 PU preload before the short circuit. The current could easily reach 5 PU before the actual trip-off occurred. This creates some serious problems. First of all, it creates more stress on the power switch during the switching operation. An alternative is to change the positive threshold voltage at pin 3 of U302 with load. If it were reduced to .0125 volt at 1 PU steady state load, the steep front required for tripping would be 2 (.0125/.05) = .5 PU. When this is added to the 1 PU steady state current, a 1.5 PU total current is sufficient to initiate a trip. This would still allow for load current fluctuations of .4 PU from the nominal 1 PU without giving a nuisance trip. A circuit was designed and incorporated into the MOSFET breadboard to accomplish this change in reference voltage at pin 3 of U302. The "front end" of the overcurrent protection circuit is shown in figure 7-16. From the time an overcurrent is sensed by U302 until the gates of the power switching MOSFETS are tied to their source terminals takes approximately one microsecond.

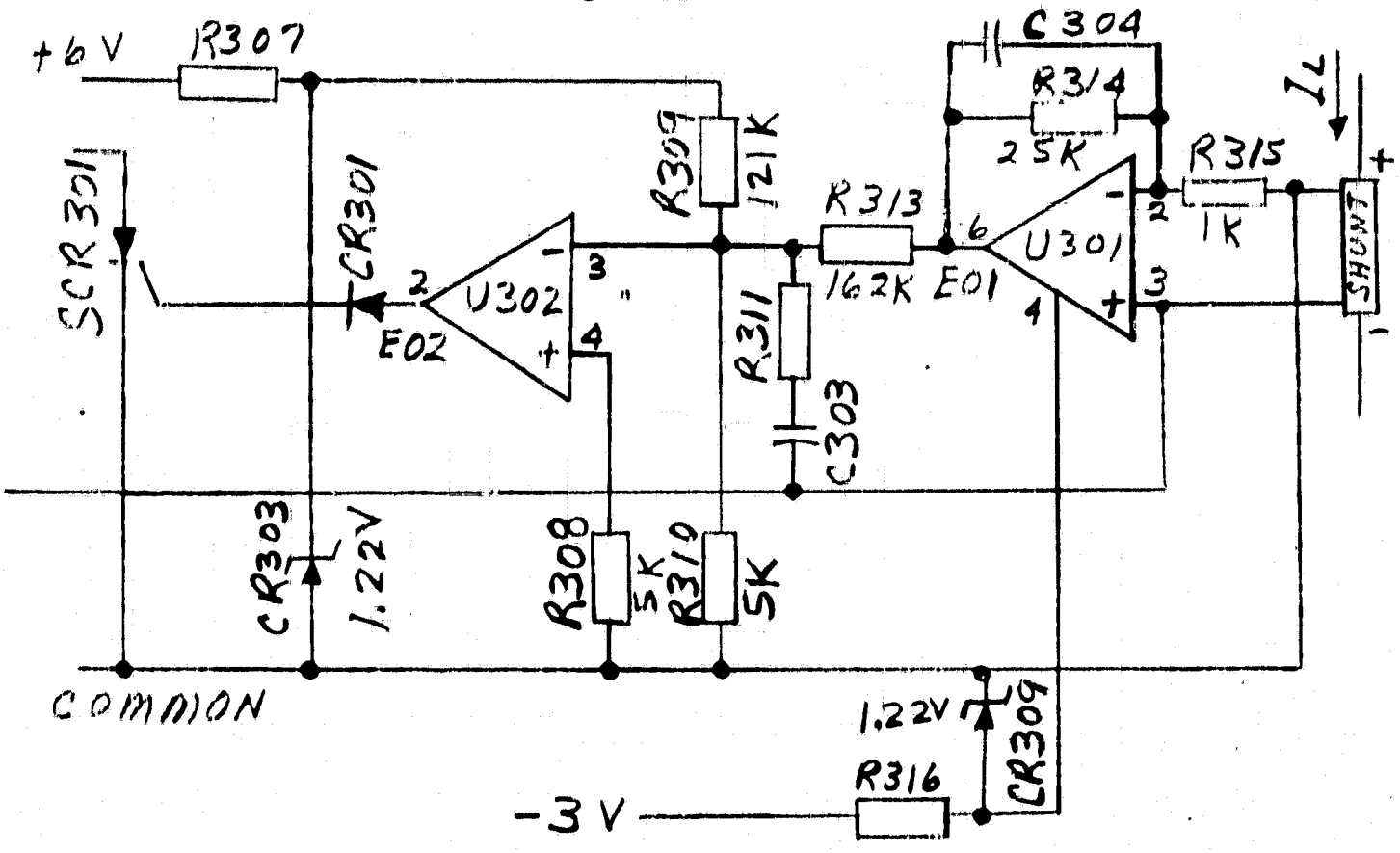


Figure 7-16 - Overcurrent Protection - Front End

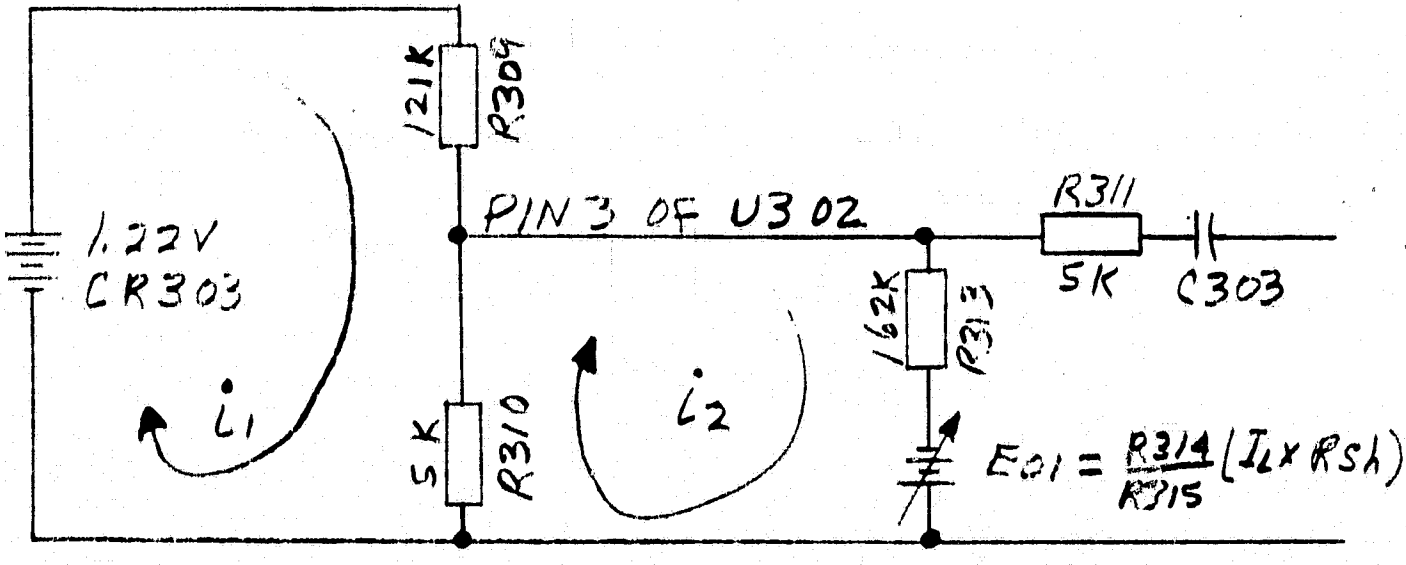


Figure 7-17 - Equivalent Circuit - Front End

7.4 New MOSFET Breadboard Description and Test Results (Figures 7-2 Through 7-24) (Continued)

Figure 7-17 shows the equivalent circuit for figure 7-16. Calculations for the 25% preload condition proceed as follows:

$$E_{01} = \frac{R314}{R315}(.05V)(IPU) = \frac{25K}{1K}(.050V)(.25) = .3125V$$

The equations for the two loop currents are:

(1) $(126K)\, i_1 - (5K)\, i_2 = 1.22$

(2) $-(5K)\, i_1 + (167K)\, i_2 = .3125$

$$5(1)\quad (630K)\, i_1 - (25K)\, i_2 = 6.1$$
$$126(2)\quad -(630K)\, i_1 + (21042K)\, i_2 = 39.375$$
$$0 + (21017K)\, i_2 = 45.475$$
$$i_2 = 2.1637\ \mu A$$

Solving for i_1 we obtain:

$$126K\, i_1 - 5K\,(2.164\ \mu A) = 1.22$$
$$(126K)\ i_1 = 1.2308$$
$$i_1 = 9.768\ \mu A$$

The reference voltage at pin 3 is:

$$(i_1 - i_2)\, 5K = .038V$$

This would require a 1.52 PU steep front current to cause pin 3 to go negative.

$$(1.52\ PU \times .05V)\ .5 = .038V$$

7.4 New MOSFET Breadboard Description and Test Results (Figures 7-2 Through 7-24) (Continued)

The steep front current of 1.52 PU must be added to the steady state current of .25 PU to obtain the total or peak current at which point U302 is ready to respond. This current is:

$$1.52 \text{ PU} + .25 \text{ PU} = 1.77 \text{ PU}$$

Thus, if the SSPC was carrying .25 PU load and the load short circuited, the current would rise rapidly (limited only by inductance). As it passed 1.77 PU, U302 would respond by sending its output (pin 2) positive. This would fire SCR301 and initiate a trip. Capacitor C304 is chosen large enough to prevent U301 from responding to the steep front of current.

Operation with a .5 PU current preload can be established by first determining the positive reference voltage at pin 3 of U302.

$$E_{01} = \frac{25K}{1K}(.050V)(.5) = .625$$

The loop equations are:

$$(1) \quad (126K)\, i_1 - (5K)\, i_2 = 1.22$$

$$(2) \quad -(5K)\, i_1 + (167K)\, i_2 = .625$$

$$5(1) \quad (630K)\, i_1 - (25K)\, i_2 = 6.1$$
$$126(2) \quad -(630K)\, i_1 + (21042K)\, i_2 = 78.75$$

$$0 + (21017K)\, i_2 = 84.85$$

$$i_2 = 4.037\ \mu A$$

7.4 New MOSFET Breadboard Description and Test Results (Figures 7-2 Through 7-24) (Continued)

Solving for i_1 we obtain:

$$126K\ i_1 - 5K\ (4.037\ \mu A) = 1.22$$
$$(126K)\ i_1 = 1.24$$
$$i_1 = 9.84\ \mu A$$

The reference voltage at pin 3 is:

$$(i_1 - i_2)\ 5K = .029V$$
$$.029V/.05V = .58\ PU$$

A steep front current of 1.16 PU (2× .58 PU) must be added to the .5 PU steady state current to get 1.66 PU total current at which value the voltage at pin 3 of U302 has been reduced to zero. A further increase in current will cause a trip-off.

By the same procedure it is found that with a .75 PU preload, response occurs at 1.55 PU. At 1 PU preload, response occurs at 1.47 PU. This information has been plotted in figure 7-18. After all testing was complete, the positive reference voltage level at pin 3 of U302 was reconsidered. It is recommended that R313 be changed to 237K, and R309 changed to 158K. This will lower the threshold with light preloads. The operation will be nearly the same regardless of the preload from no load to full load; with these values the trip will be initiated at approximately 1.5 PU when turning on into a short circuit which is the same as with 1 PU preload before the fault. Calculated results are plotted in figure 7-19.

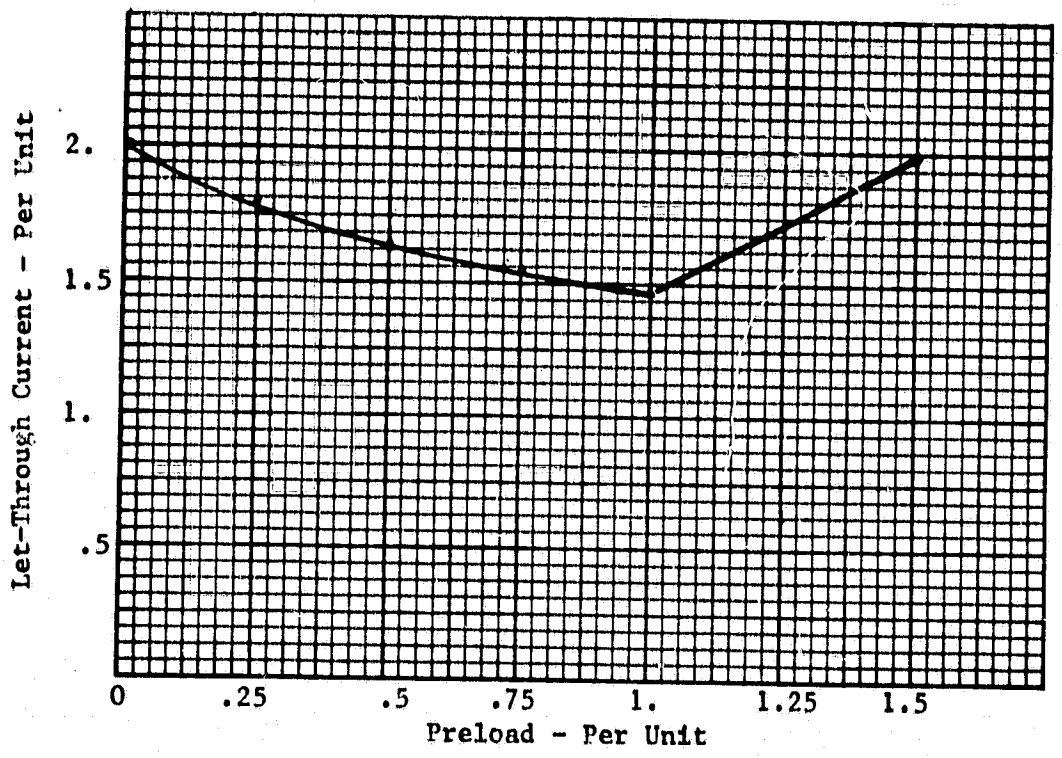


Figure 7-18 - Let-Through Current Versus Preload

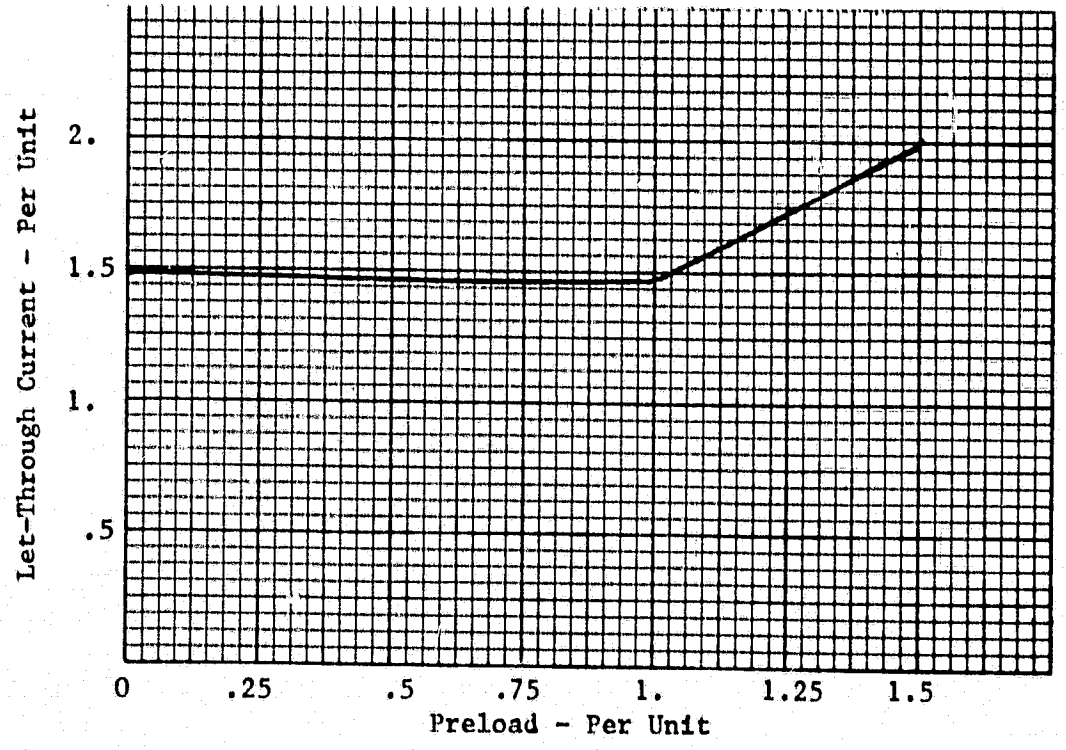


Figure 7-19 - Let-Through Current Versus Preload

7.4 New MOSFET Breadboard Description and Test Results (Figures 7-2 Through 7-24) (Continued)

The complete overcurrent protection circuit is shown in figure 7-20. Note the method of tripping is by firing SCR301 which turns on optocoupler OC3 which starts the trip lockout in the logic circuit. OC1 and OC3 which are energized by the logic convey the trip information to the bank drive circuits by bringing the inverting input of U102 to the negative bus.

Precision reference CR309 is included to limit E_{01} to 1.22 volts negative. Hence, at 1 PU preload current, E_{01} calculations give:

$$E_{01} = \frac{25K}{1K} (.050V) = 1.25V$$

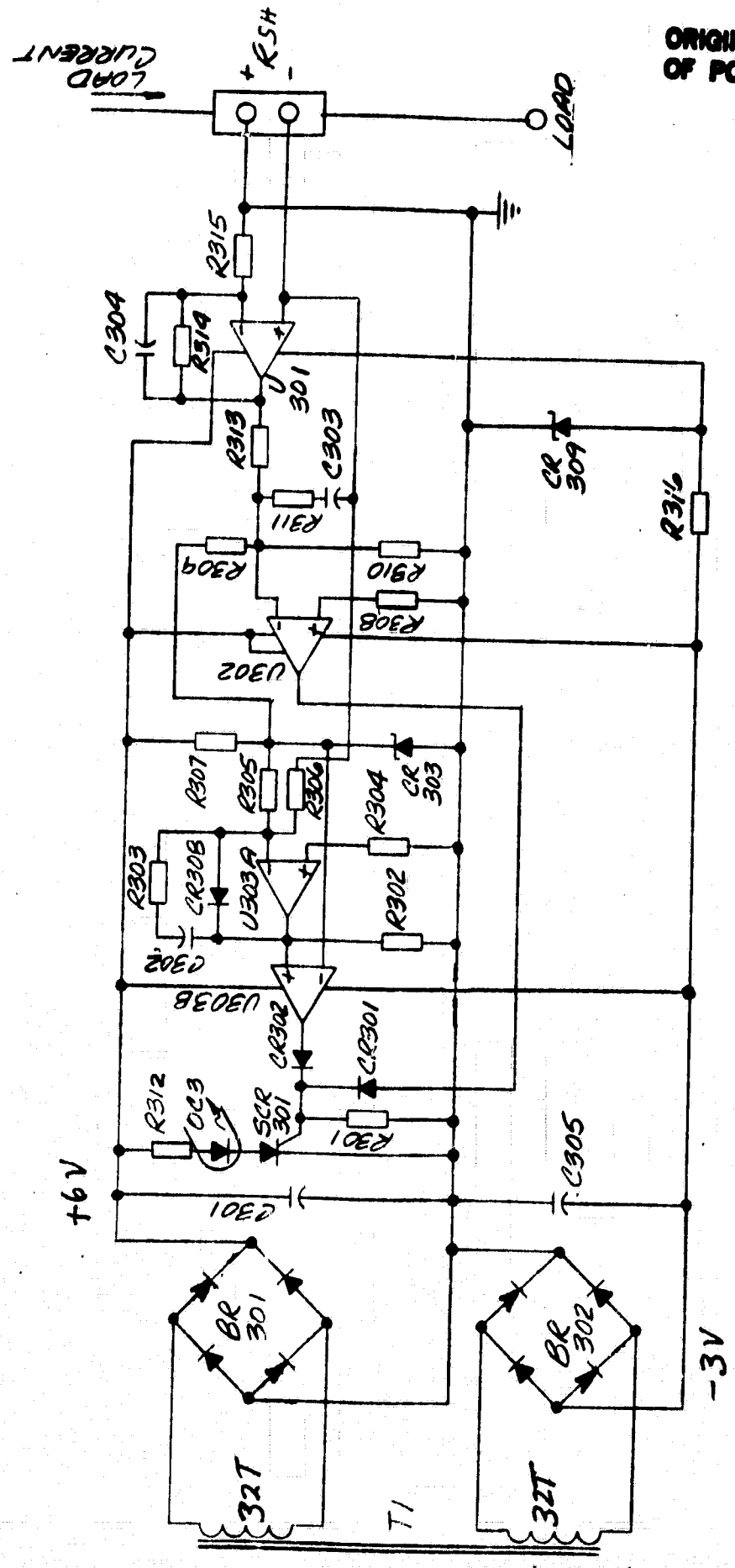


Figure 7-20 - Complete Overcurrent Protection Circuit

Table 7-5

Overcurrent Protection Parts List

Designator	Description
BR101	4 - IN4007
BR102	4 - IN4148
C301	1.0 µF Tantalum
C302	1.0 µF/50V Ceramic
C303	.0068 µF/50V Ceramic
C304	.068 µF/50V Ceramic
C305	1.0 µF Tantalum
CR301	IN4148
CR302	IN4148
CR303	ICL8069 1.22V Reference
CR308	IN4148
CR309	ICL8069 1.22V Reference
OC3	6N136 Optocoupler
R301	510Ω CC
R302	100K CC
R303	105K MF
R304	1.21K MF
R305	255K MF
R306	12.7K MF
R307	4.7K CC
R308	4.99K MF
R309	121K MF
R310	4.99K MF

Table 7-5

Overcurrent Protection Parts List

(Continued)

Designator	Description
R311	4.99K MF
R312	100Ω CC ½ Watt
R313	162K MF
R314	24.9K MF
R315	1K MF
R316	1K CC
SCR301	MCR204
U301	CA3130AS
U302	LM111J (14pin DIP)
U303	LM158AH

7.4 New MOSFET Breadboard Description and Test Results (Figures 7-2 Through 7-24) (Continued)

Since E_{01} is limited to 1.22 volts by CR309, this value is used for all preloads greater than .98 PU. This allows approximately .012 volt at pin 3 of U302 before the short circuit occurs. It is felt that a margin of approximately .25 PU should be allowed for normal current transients. If this was not done, a light overload of 29% (1.29 PU current) would lower the voltage to zero on pin 3 and any greater voltage would drive it negative resulting in an instant trip. This would defeat the purpose of the inverse current/time trip curve. For this reason, E_{01} is limited to 1.22 volts and the curve turns upward at 1 PU in both figures 7-18 and 7-19. For the values of R313 and R309 used for figure 7-19, the hair trigger point would occur at 1.45 PU. At zero load current, R313 will be in parallel with R310 and lower the reference voltage by a few percent. This is not considered significant.

The turn-on ramp of the gate voltage shown in figure 7-4 should be slowed to perhaps one fifth the present rate of rise. This would increase the turn-on time to more than 100 microseconds. According to the SOA for the IRF 450 MOSFET, switching eight amperes per transistor within 100 microseconds is within capability. With ten transistors in parallel, the normal load current would be 2.5 amperes per transistor. The maximum switching time could be almost one millisecond. This would increase the allowable load capacitance.

7.4 New MOSFET Breadboard Description and Test Results (Figures 7-2 Through 7-24) (Continued)

In summary, if a high speed switch is to be used, it is imperative that the current threshold for fast operations be set as close as practical at 1 PU current. To allow for small current transients and line disturbances without nuisance trips, a threshold of approximately 1.4 PU was considered a good compromise. To make U302 operate more quickly on a 1 PU preload, the threshold voltage at pin 3 must be a function of load current. Operational amplifier U301 (RCA3160) was added for this purpose. Its function is to reduce the threshold voltage at pin 3 of U302 as a function of load current, but not to respond to transients. In other words, the threshold at pin 3 is determined by the steady state current before the fault. Capacitor C304 slows the response sufficiently for this purpose. Precision voltage reference CR309 supplies a negative voltage for pin 4 of U301. The output at pin 6 is a function of the load current, R314, R315, and the negative voltage at CR304. As pin 6 is driven negatively, it subtracts from the 50 MV reference voltage that is normally at pin 3 of U302. This is controlled by the selection of resistors R309, R310, R313, R314, and R315. The bias at pin 3 of U302 can be completely removed at a certain load current such that a steep front exceeding that value will trip immediately. If the threshold is chosen as five millivolts with 1 PU load current, a sudden increase (caused by a short circuit) to 1.25 PU load current would give a net increase of .25 PU.

7.4 New MOSFET Breadboard Description and Test Results (Figures 7-2 Through 7-24) (Continued)

Assuming the rate of change was fast enough, C303 would be a short circuit and the 12.5 millivolts (1 PU current gives a shunt voltage of 50 millivolts) would be divided equally across R311 and R310. This would exceed the threshold at pin 3 of U302 and tripping action would begin. Thus, tripping action could be started at any value of current greater than 1 PU rather than waiting until the current reached 3 PU as it would if the threshold was held at 50 millivolts and independent of load current. In a practical case R313, R314, and R315 must be chosen to allow normal current disturbances without nuisance trips. The threshold should not be higher than necessary since the voltage "overshoot" will be higher. Figure 7-21 shows the turn-off when a short circuit was applied to a 1 PU preload. The trace is of the load current which rises from 25 amperes and peaks at 38 amperes. The source voltage was 200 volts. Figure 7-22 shows the load current when a short circuit was applied to a 1 PU preload with a source voltage of 500 volts. The load current rose from 25 amperes (1 PU) to approximately 45 amperes (1.8 PU) and was cleared in less than one microsecond. This is a tremendous improvement over the 3 PU current response that would result without U301. Of course, R311 could be reduced some to lower the peak current when turning on into a fault. The addition of U301 and associated components has allowed the lowering of the threshold voltage at pin 3 of U302 proportional to steady state load current. This allows the most troublesome faults (those that occur while carrying rated load current) to be cleared with ease.

ORIGINAL PAGE
BLACK AND WHITE PHOTOGRAPH

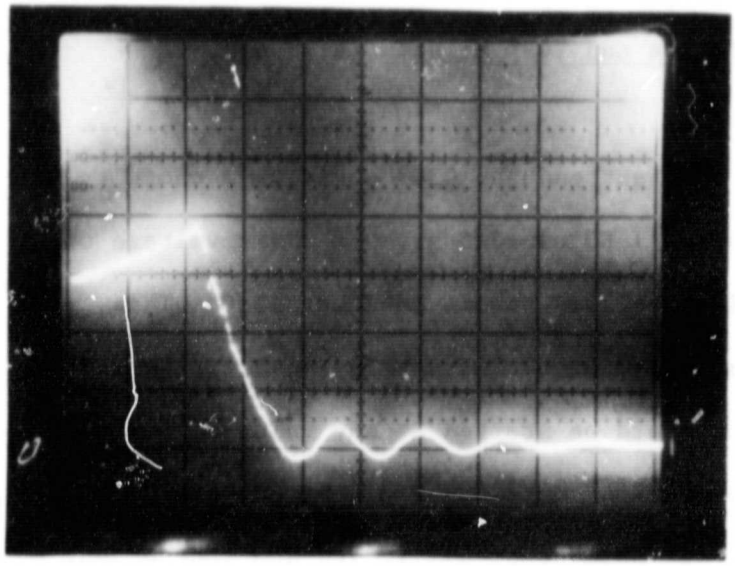


Figure 7-21 - Short Circuit with 1 PU Preload - 200V
I_{Load} = 10A/Division
Horizontal 5 µS/Division

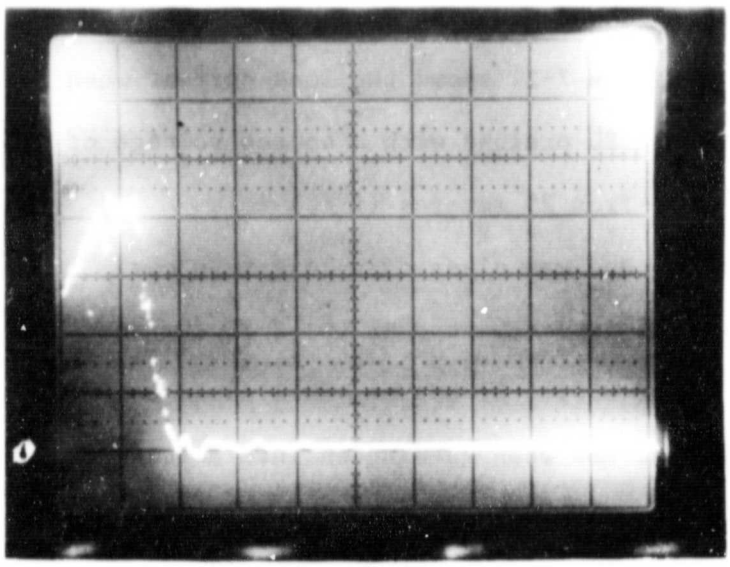


Figure 7-22 - Short Circuit Clearing with 1 PU Preload
V_{Source} = 500
I_{Load} = 10A/Division
Horizontal 1 µS/Division

7.4 New MOSFET Breadboard Description and Test Results (Figures 7-2 Through 7-24) (Continued)

Figure 7-23 shows the drain/source voltage of both banks superimposed during a normal turn-off of a 200V supply. Figure 7-24 shows the current and voltage during a normal turn-off of 250 volts.

Great progress has been made in fast switching of high voltage and current devices. Although the rapid clearing of faults may not be the most desirable in all cases, the designer now has a viable third option to consider. It may well be that a combination of fast response and current limiting may prove to be the best solution in many applications. The greatest limitation to the fast responding switch is the high Ldi/dt that appears across the switching device. Operation of two MOSFET banks in series complicates the circuit, but satisfactory operation has been obtained.

ORIGINAL PAGE
BLACK AND WHITE PHOTOGRAPH

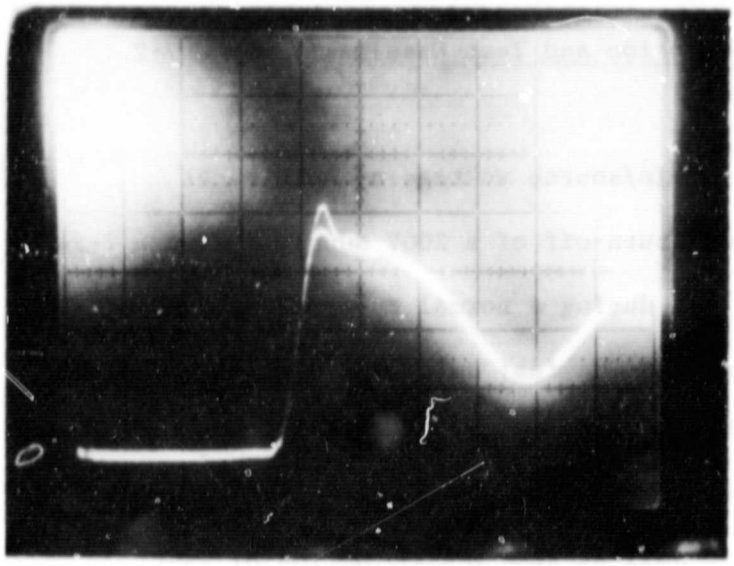


Figure 7-23 - Normal Turn-Off
V_{DS} of Both Banks
100V/Division
25A Load
Horizontal 200 NS/Division

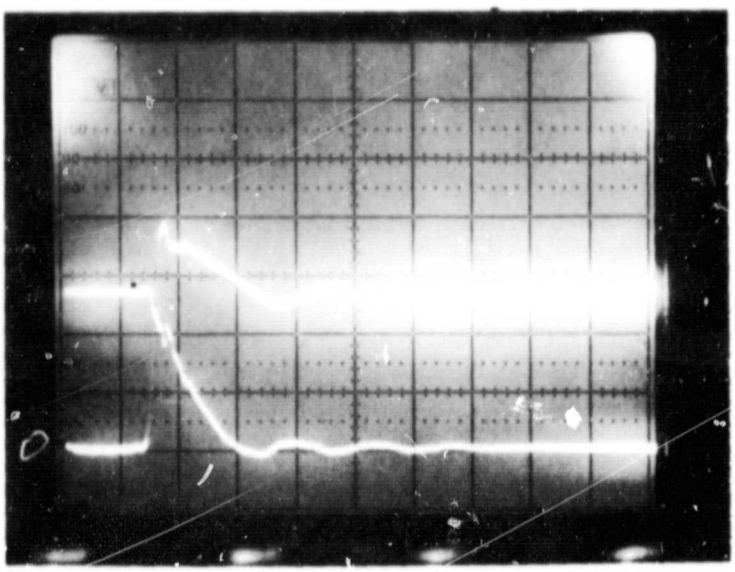


Figure 7-24 - Normal Turn-Off
V_{Source} = 250V at
100V/Division
I_{Load} = 10A/Division
Horizontal 500 NS/Division

SECTION VIII

CONCLUSIONS AND RECOMMENDATIONS

This program has demonstrated the feasibility of using fast switching on HVDC switchgear. The successful development of fast switching bipolar and MOSFET circuits gives the user options that can result in optimization to a given application. The improvements in the overcurrent protection circuit should become standard on all DC SSPCs.

The inclusion of MOSFETS for the power switch offer the possibility of hybrid packaging to reduce weight and space. The HV bipolar transistors are so large, hybrid packaging is impractical. Approximately 20 MOSFET chips (each .25 inch square, 6.25 millimeters square) could be soldered to a metallized BeO header similar to the header for the 20A Shuttle RPC. The power switch could be assembled in a package as pictured in figure 8-1. The mounting flange is metal, but the remainder of the package is ceramic giving good dielectric breakdown spacing between conductors. Power in and power out stud terminals would be located on the top surface along with other circuit connections. There is adequate space for two series banks of ten parallel MOSFET chips (.25 inch square) plus the associated gate resistor and Zener diode for each chip. The calculated temperature rise from heat sink (customer mounting surface) to power chip junction is 30°C at 75 watts. Figure 8-2 shows the header assembly for a 20A Shuttle RPC and figure 8-3 shows the header assembly for a 30A, 120 VDC RPC made for NASA-Lewis on Contract Number NAS3-17771. The remainder of the circuit could consist of a current shunt, transformer, a hybrid logic module, overcurrent protection module, and two gate drive modules.

Approximate sizes of these components are given below.

- Transformer - 2.54 cm Diameter × 1.25 cm High
- Shunt - 1.5 mm Diameter × 2.5 cm Long
- Logic Module - 2.5 cm Square × .5 cm Thick Hybrid
- Overcurrent Module - 2.5 cm Square × .5 cm Thick Hybrid
- Gate Drive Module - 2.5 cm Square × .5 cm Thick Hybrid

These components could be packaged on a PW board mounted above the power switch as shown in figure 8-4. The total assembly including the power switch would be 11 cm × 11 cm × 5.7 cm high and weigh .82 kg including potting. There is room in the power switch for a series string of five watt Zener diodes, but not enough room for varistors across the input-output terminals to suppress switching spikes appearing across the switch because of the high di/dt during turn-off. There is sufficient space between the power switch and PW board for circuit elements to control the voltage spikes within acceptable limits. The cover over the entire mounting should be an insulator and have holes for the power and control lead wires to enter. Potting with a dense material should help the dielectric breakdown voltage.

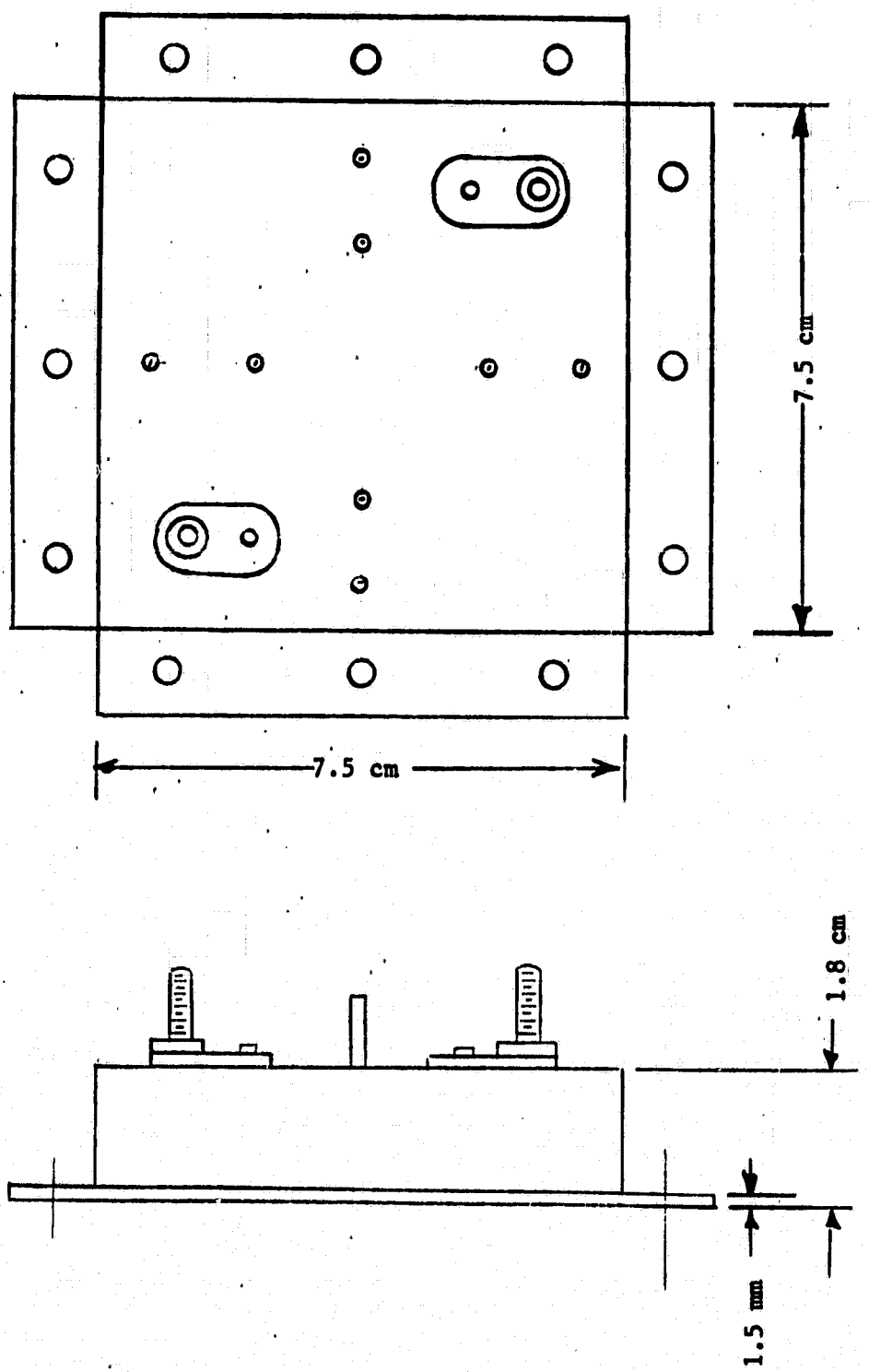


Figure 8-1 - MOSFET HV Switch - 25 Amperes, 1,000 VDC

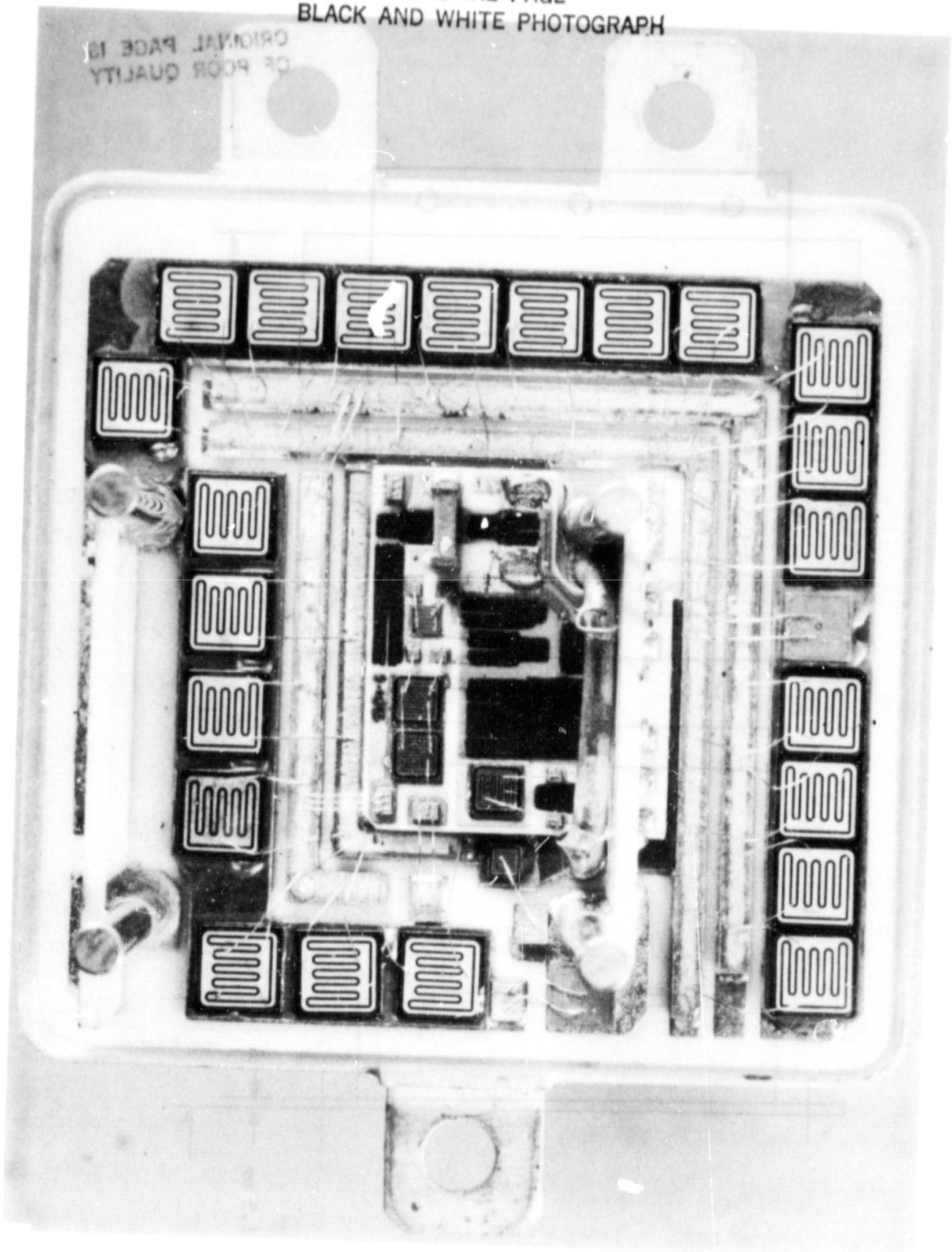


Figure 8-2 - Header Assembly for 20A RPC

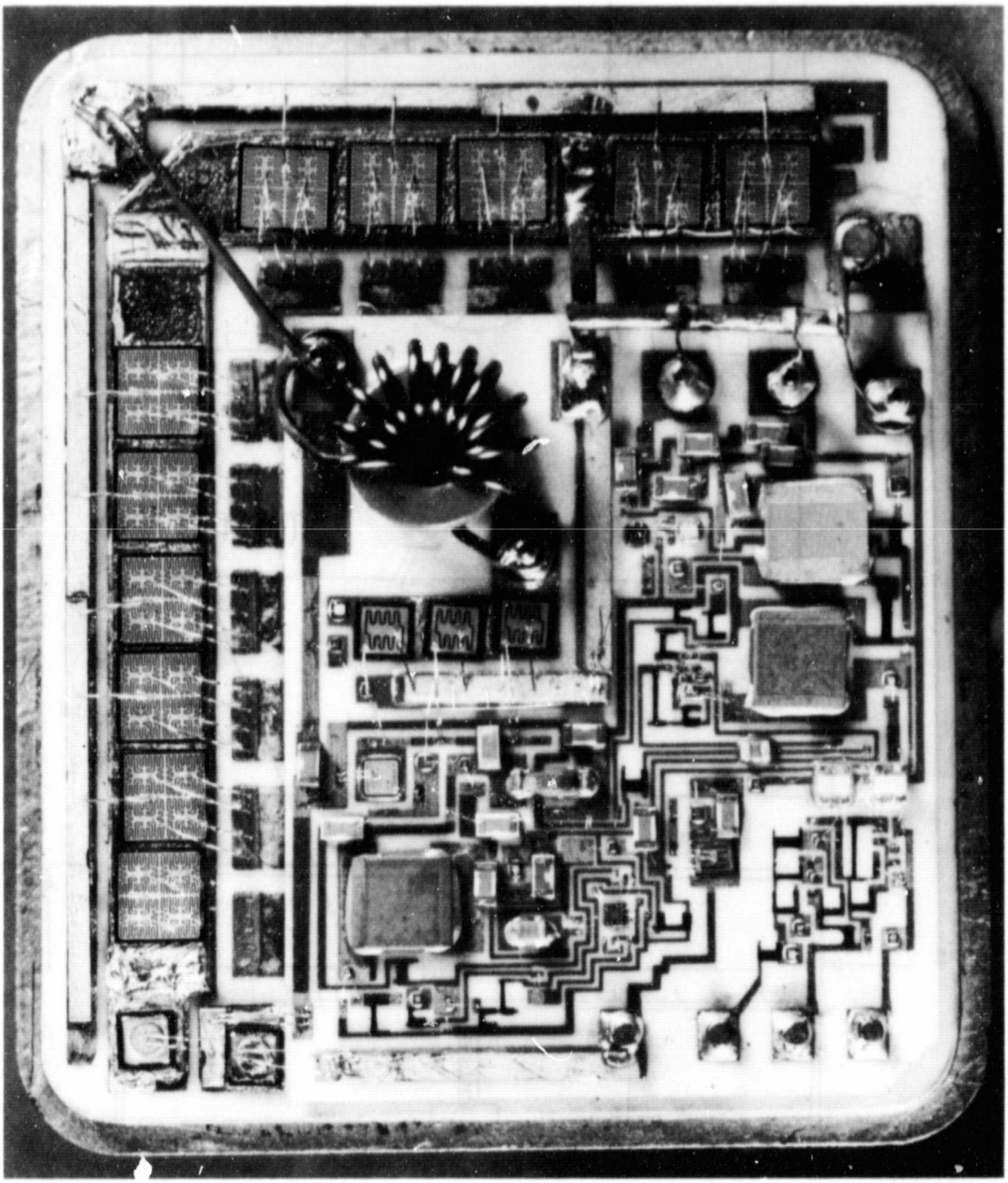


Figure 8-3 - Header Assembly for 120V, 30A RPC

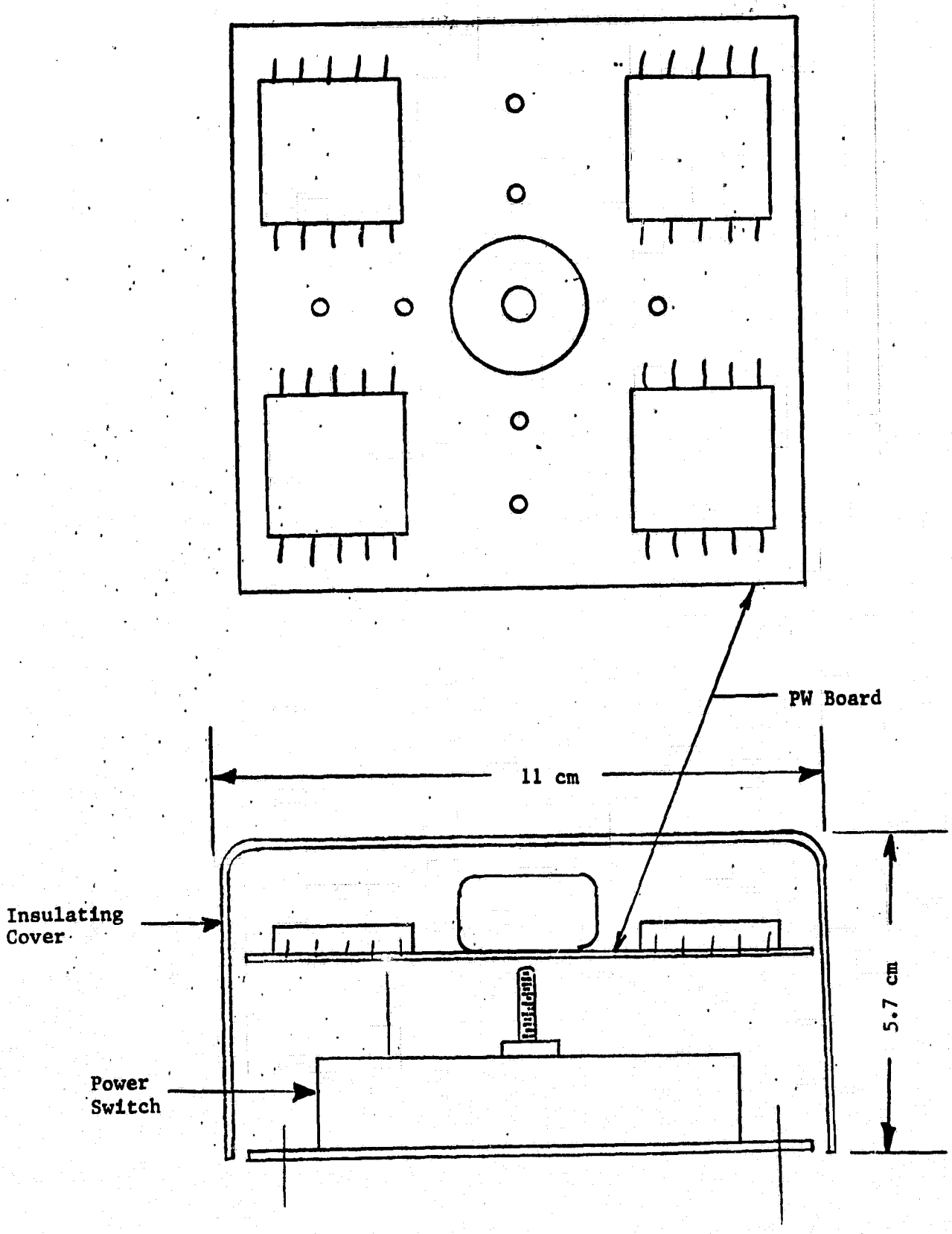


Figure 8-4 - 1 KV, 25A RPC Packaging

Approximately one watt will be taken from the 28V bus on a MOSFET SSPC. If 20 of the IRF 450 (500V) transistors were paralleled, the R_{DS-on} would be .4/20 = .02 ohm. At a load current of 50 amperes, the drop would be one volt and the loss would be 50 watts. A 270 VDC, 50A SSPC could be built in the same package as shown in figure 8-4. The efficiency would be:

$$\text{Efficiency} = (100)\ \frac{270 \times 50}{270 \times 50 + 50 + 1} = 99.62\%$$

This figure must be regarded as a maximum value. There would be some loss in the snubber network which may be in the order of three to five watts. This would reduce the efficiency to 99.58%. The losses could increase from 57 watts to 67.5 watts and still keep the efficiency at 99.5%. With 270 volts, it would not be necessary to use two power transistors in series. This would be easier to control the high Ldi/dt voltage across the transistors during switching.

APPENDIX A

APPENDIX A

DESCRIPTION

TEST PLAN FOR

1 KV/25A DC REMOTE POWER CONTROLLER

FOR

NASA-LEWIS CONTRACT NO. NAS3-22646

APPROVAL	DATE
Engineer John J. Marshall	12/8/80
Design Sect. Mgr.	
Marketing Syst. Mgr.	
Qual. & Rel. Engrg.	
Supv. Standards	

REVISIONS

WESTINGHOUSE ELECTRIC CORP.
AEROSPACE ELECTRICAL DIV.
LIMA, OHIO, U. S. A.

REV.	CODE IDENT NO. 83843
DESIGN SPEC. NO. D-774156	
SHEET 1 OF 14	

1 KV/25A DC TEST PLAN FOR REMOTE POWER CONTROLLER NASA-LEWIS CONTRACT NO. NAS3-22646

1.0 SCOPE

This document covers the test plan which will be used to evaluate the breadboard built in Task 2 and the two packaged breadboards built in Task 5.

2.0 TEST SCHEDULE

The test schedule shall be as illustrated by Table I.

3.0 TEST CIRCUIT CONFIGURATION

The test circuit shall be as shown by Figure 1 and it will be the basis of all tests performed on the B/B and packaged B/B.

3.1 Test Circuit Components

V_{Bus} Supply.....	0-1000VDC Supply
V_{cont} Supply.....	0-40 volt, 1 amp supply.
R_{Load}.....	Variable load bank, 48 x 110 /1 KW sections.
Power Circuit Impedance.....	#2/0 copper stranded wire cabling everywhere load current or fault current flows. 30 feet total length maximum.
Switch S1, S2.....	1 PST 3A toggle switch.
Switch S4, S5.....	100 amp knife switch.
V_1, V_2, V_3.....	Weston 4442 or equivalent digital voltmeter.
I_1, I_2.....	Either DVM/shunt or calibrated D'Arsonval meters.

Oscilloscope.....	Tektronix 464, DC to 100 MHZ, HP 3.5nsec rise time or equivalent.
Shunt.....	Coaxial shunt, non-inductive type.
Fault Device S3.....	Circuit breaker switch (for operator isolation).

TABLE I

TEST SCHEDULE

Item No.	Tests	Para.	Temp. °C
1.	Dielectric	4.1	25
2.	Static Tests	4.2	25 -50 +85
3.	$T_{on}, T_{off} T_{rise}, T_{fall}$	4.3	25 -50 +85
4.	Trip Characteristics	4.4	25 -50 +85
5.	Trip Free	4.5	25 -50 +85
6.	Reset Time	4.6	25 -50 +85
7.	28VDC Tests	4.7	25 -50 +85
8.	Short Circuit Response	4.8	25 -50 +85

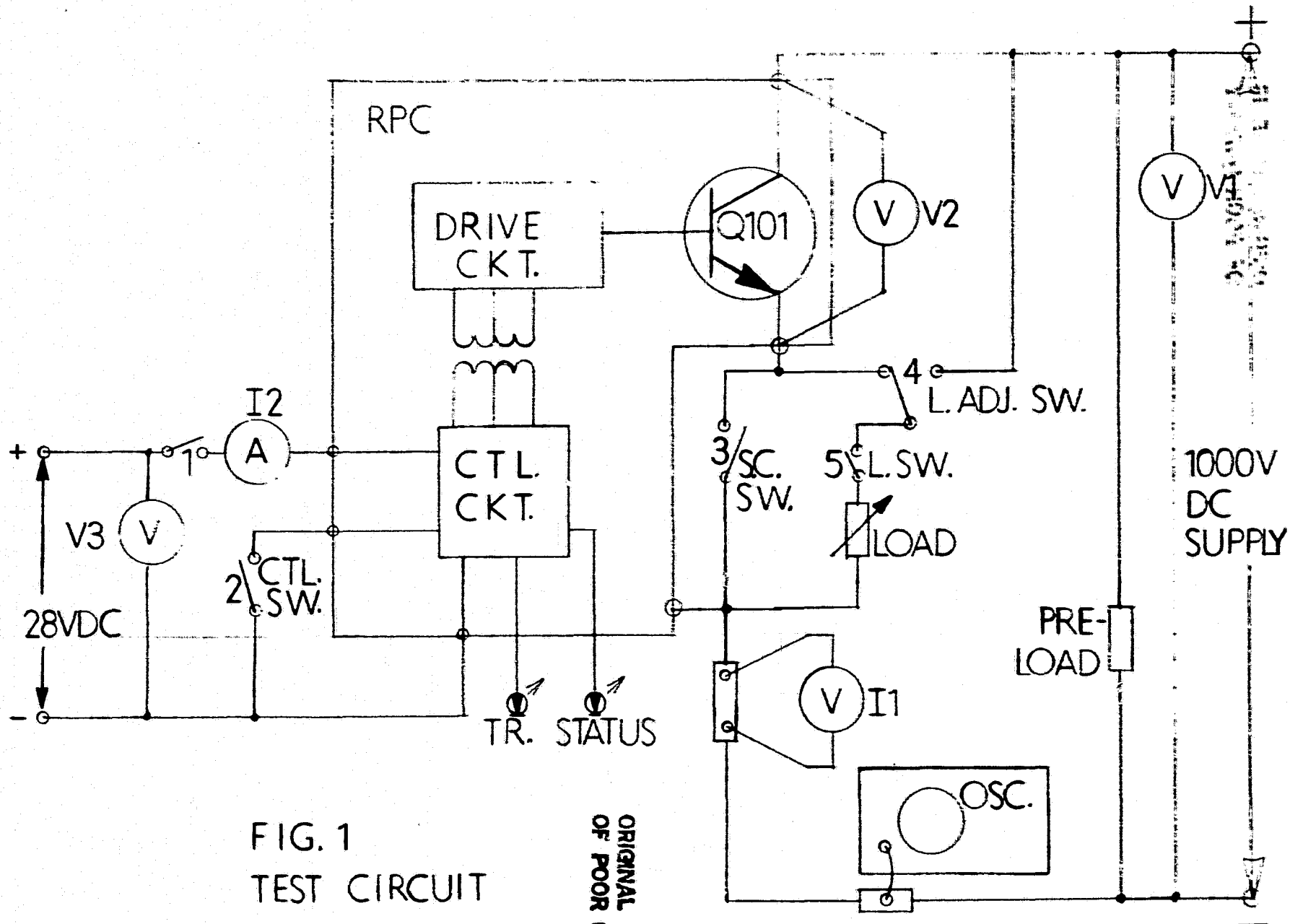


FIG. 1
TEST CIRCUIT

4.0 EVALUATION PROCEDURE

All test data shall be entered in the appropriate test data sheet shown in Appendix B. Tests at temperature extremes shall be performed as indicated in Table I.

4.1 Dielectric

There shall be no leakage current in excess of five milli-amperes nor evidence of arcing or flashover when 1500VAC, 60 Hz is applied for 5 seconds between all power terminals and all control terminals and all terminals and cover (packaged B/B).

4.2 Static Tests

With the units connected per paragraph 3.0 all meter readings shall be recorded with the RPC in an "on state" and in an "off state." Test conditions shall be V_{Bus} = 400, 700, 1000 volts dc, and ambient temperature shall be -50, +25 and +85°C. The RPC off/on operation will be accomplished by opening and closing S2, depending upon the desired RPC state. Load shall be rated resistive load.

4.3 Turn-On and Turn-Off Characteristics

Turn-on and turn-off characteristics shall be monitored by an oscilloscope (paragraph 3.0). Turn-on and turn-off times are defined as the time required for the load current to reach 90% of its final value after step application or removal of the control signal. Rise time and fall time are defined as the time required for the load current to go from 10% to 90% of its final value during turn-on or turn-off.

Test conditions shall be rated supply voltage and rated resistive load.

4.4 Trip Characteristics

Adjust load impedance to obtain an overload condition. Close the RPC by applying control voltage, monitor and record trip time. Supply voltage shall be at rated value. Overload current levels shall be as specified in the appropriate data sheet (see paragraph 4.0). The trip time is defined as the time between the current reaching 90% of the peak value at turn-on and falling to 10% of the same peak value at trip-off, the appropriate instant trip level for each test point as defined by the data sheet, paragraph 4.4.

4.5 Trip-Free

Verify during trip characteristics evaluation (paragraph 4.4) that the RPC is trip-free, i.e., the RPC will trip and remain tripped even though the control signal remains on after the trip-off occurs.

4.6 Reset Time

With the RPC in the tripped condition, measure time that the control signal must be in the "0" state before trip lockout reset occurs.

4.7 28VDC Tests

4.7.1 28VDC Undervoltage Protection Minimum Pickup

With the RPC in the "ON" state, lower Vcs (V3) from 28 volts until the RPC trips off to determine the UV protection operating level.

4.7.2 28VDC UV Time Delay

With the RPC in the "ON" state, step Vcs from 28VDC to 0VDC to measure the UVTD time.

4.7.3 28VDC Power-Up Tests

a. With S2 in the "ON" position, Vbus = 1000VDC, $R_L \approx 40$ ohms and Vcs = 0, step Vcs to 28VDC and measure the RPC turn-on time.

b. Repeat "a" except with S2 in the "OFF" position and verify that no voltage appears at the load.

4.8 Short Circuit Tests

4.8.1 With the RPC off, close the fault switch. Subsequently close the RPC and monitor the load current and record the short circuit trip time. This time is defined as the interval between the current reaching the instant trip set point level, then falling to 10% during trip off. Also record the peak current level.

4.8.2 Repeat paragraph 4.8.1 above except with the RPC closed and carrying no load current, close the fault switch.

4.8.3 Repeat test 4.8.2 above except adjust load resistance to draw 25 amps load current before the fault switch is closed.

APPENDIX A

TEST DATA SHEETS

Para. 4.1 Dielectric OK____

Para. 4.2 1 KV RAC Static Data

Device Tested_____

Test Con V_{Bus} = 400V, 700V, 1000V
I_{Load} = 25ADC
V_{CS} = 28VDC
Temp. = -50°C, +25°C, +85°C

State	Item	Units	V_{Bus} 400V Temp °C			V_{Bus} 700V Temp °C			V_{Bus} 1000V Temp °C			Limits
			-50	+25	+85	-50	+25	+85	-50	+25	+85	
ON	V_1	Volts										---
	V_2	Volts	-	-	-				-	-	-	2.0 max.
	V_3	Volts	-	-	-				-	-	-	---
	I_1	Amps										---
	I_2	Milliamps										
	*P_{Loss}	Watts										125 max.
OFF	V_1	Volts										---
	V_2	Volts										---
	V_3	Volts	-	-	-				-	-	-	---
	I_1	Microamps										0
	I_2	Milliamps										---
	*P_{Loss}	Watts										5.0 max.

*Calculated from $(V_2)(I_1) + (V_3)(I_2)$

Para. 4.2 1 KV RAC Static Data (Cont'd)
Device Tested _____

Test Conditions: V_{Bus} = 400V, 700V, and 1000VD
I_{Load} = 25ADC
V_{cs} = 28VDC
Temp. = -50°C, +25°C, +85°C

State	Item	Units	V_{Bus} 400V Temp °C -50	400V +25	400V +85	700V -50	700V +25	700V +85	1000V -50	1000V +25	1000V +85	Limits
TRIPPED	V_1 V_2 V_3	Volts Volts Volts	-	-	-				-	-		--- --- ---
	I_1 I_2	Microamps Milliamps										0 ---
	*P_{Loss}	Watts										

*Calculated from $(V_2)(I_1) + (V_3)(I_2)$

Device Tested _____

Para. 4.2 Partial Load Tests
Static Test Data (Cont'd)

V_{Bus} = 1000VDC
I_{Load} = 5A-25ADC
V_{cs} = 21, 28, 35VDC
Temp. -50°C, +25°C, +85°C

Item	Units	I_L = 5A			I_L = 5A			I_L = 10A			I_L = 15A			I_L = 20A			I_L = 25A		
		-50	+25	+85	-50	+25	+85	-50	+25	+85	-50	+25	+85	-50	+25	+85	-50	+25	+85
V_1	Volts	← 1000V →																	
V_2	Volts	← 21.0 →			← 28.0 →			← 35.0 →			← 28.0 →								
V_3	Volts																		
I_1	Amperes										-	-	-	-	-	-	-	-	-
I_5	Amperes																		

DYNAMIC TEST DATA FOR 1 KV RPC

Test Conditions: V_{Bus} = 1000VDC
V_{cs} = 28VDC
Temp. = -50°C, +25°C, +85°C

DEVICE TESTED _____

Para.	Test Description	Special Conditions Other than Rated	Units	Temp °C			Limits
				-50	+25	+85	
4.3	Turn-on Time, T_{on} Rise Time, T_R Turn-off Time, T_{off} Fall time, T_F	Rated Load Rated Load R_L 40 * Rated Load P_L 25 KW* Rated Load	Millisec Microsec Millisec Microsec				.01 - 1.0 10 min. .01 - 1.0 10 min.
4.4	Ultimate Trip Current Level	Vary R_{Load}, monitor output of oscilloscope	Amp				27.5 - 75
	37.5 Amp Trip Time	R_L 26.7 Ohms	Seconds				.3 - 1.0
	50 Amp Trip Time	R_L 20 Ohms	Seconds				.1 - .35
	62.5 Amp Trip Time	R_L 16 Ohms	Seconds				.02 - .12
	75 Amp Trip Time	R_L 13.3 Ohms	Seconds				0 - .05
4.5	Trip Free		Pass/Fail				
4.6	Reset Time		Seconds				TBD
4.7.1	UVDC Protection MPU	Lower 28VDC unit RPC trip-off occurs. Record V5	Volts				17.6 $\pm$2
4.7.2	UVDC TD	With RPC "ON," step 28VDC to zero.	Seconds				.005 - .015
4.7.3	28VDC Power-Up Tests	a. Control Signal "ON" b. Control Signal "OFF"	Seconds -				No Load Voltage or Glitch

*Record results of these tests with oscilloscope photograph.

DYNAMIC TEST DATA FOR 1 KV RPC (Cont'd)

Test Conditions: V_{Bus} = 1000VDC
V_{cs} = 28VDC
Temp. = -50°C, +25°C, +85°C

DEVICE TESTED _____

Para.	Test Description	Special Conditions Other than Rated		Temp °C			Limits
				-50	+25	+85	
4.8.1	S.C. Trip Time S.C. Peak Current (close RPC into S.C.)	*	Microsec Amperes				3 max. TBD
4.8.2	S.C. Trip Time S.C. Peak Current (applied fault with no preload)	*	Microsec Amperes	- -		- -	3 max. TBD
4.8.3	S.C. Trip Time S.C. Peak Current (applied fault with 25A preload)	*	Microsec Amperes				3 max. TBD

*Record results (I_{Load}) of these tests with oscilloscope photograph.

APPENDIX B

SOLID STATE POWER CONTROLLER

DC LOAD SWITCHING SPST-NO

25 AMPERES, 1,000 VDC

ELECTRICAL CHARACTERISTICS (-50 to +85°C ambient temperature unless otherwise specified)

General

Circuit arrangement	SPST - NO
INSULATION resistance	100 Megohms min.
Dielectric Withstand Voltage	2400VAC, 5 sec.
Isolation	2400VAC, 5 sec.
Life (operating cycles)	10^6 minimum
Radio Interference	Applicable
Leakage Current	20 milliampere max.
Power Dissipation	
"ON"	100 watts max.
"OFF"	3.0 watts max.
"Tripped"	5.0 watts max.
Efficiency (rated load)	99.6% min.

Power Circuit

Supply Voltage	
Rated Operating	1000VDC
Peak Transient	1100VDC
Minimum Operating	25VDC
Current (Min., rated)	0-25 Ampere
Voltage Drop (No-load to rated)	2.5 Volts max.
Rupture Capacity	2000 Ampere min.
Response	
Turn-on time	3-10 millisecond
Rise time	10 μ sec. min.
Turn-off time	3-10 millisecond
Fall time	100 nanosecond min.
Trip free	Applicable
Trip time	
Non-respetitive reset	See Figure 1
Repetitive resetting	30 sec. min. between resets

Control Circuit

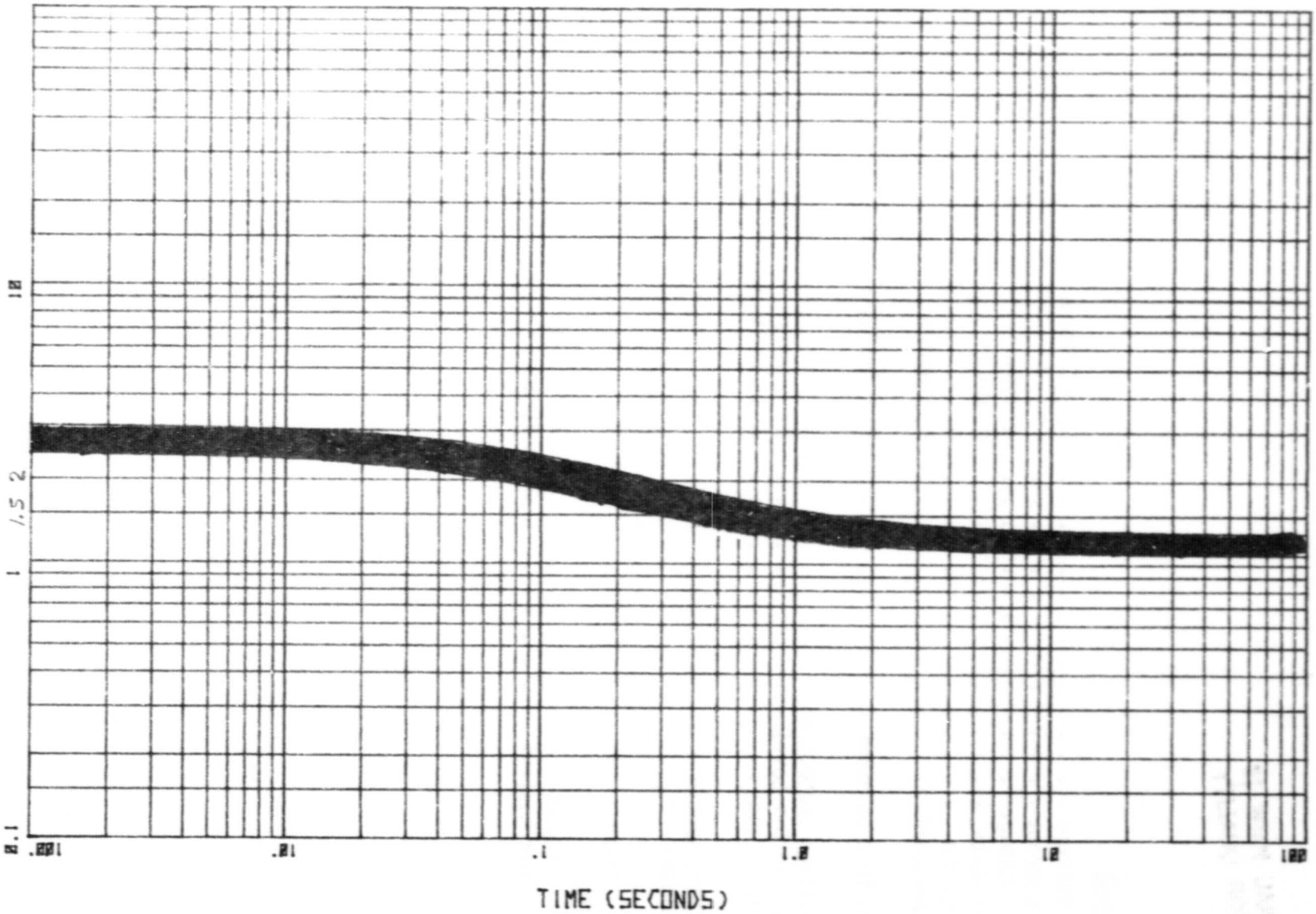
Supply Voltage	28 ± 7 Volts
Supply Current	
Turn-on Voltage	4-6Vdc
Turn-off Voltage	0-1Vdc
Input Current	0
Input Transients	Applicable
Removal time to reset	5-20 millisecond

Undervoltage Protection

Operating Level	18 ± 3Vdc
Time Delay	5-15 millisecond

Indication Signals

Status	
"ON"	5-7Vdc
"OFF"	5-
Trip	
Tripped	5-7 Volts
Not tripped	2V max.



1KV DC SSPC OVERCURRENT PROTECTION

THE END

WESTINGHOUSE ELECTRIC CORPORATION