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DIGITAL SYSTEM UPSET - THE EFFECTS OF SIMULATED LIGHTNING-INDUCED TRANSIENTS ON A GENERAL-PURPOSE MICROPROCESSOR

CELESTE M. BELCASTRO

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NASA
National Aeronautics and
Space Administration

Langley Research Center
Hampton, Virginia 23665

DIGITAL SYSTEM UPSET--THE EFFECTS OF SIMULATED LIGHTNING-INDUCED TRANSIENTS ON A GENERAL PURPOSE MICROPROCESSOR

by

Celeste M. Belcastro
NASA Langley Research Center
Hampton, Virginia 23665

ABSTRACT

Flight-critical computer-based control systems designed for advanced aircraft must exhibit ultrareliable performance in lightning-charged environments. Digital system upset can occur as a result of lightning-induced electrical transients, and a methodology has been developed to test specific digital systems for upset susceptibility. Initial upset data indicates that there are several distinct upset modes and that the occurrence of upset is related to the relative synchronization of the transient input with the processing state of the digital system. A large upset test data base will aid in the formulation and verification of analytical upset reliability modeling techniques which are being developed.

INTRODUCTION

ADVANCED AIRCRAFT of the 1990's will be designed with composite structures and computer-based digital control systems capable of performing flight-critical functions. These digital systems will be required to be ultrareliable whether the aircraft is flying through a normal or adverse environment--such as a thunderstorm. There is, therefore, a need for a better

understanding of the in-flight lightning-charged environment as well as the development of techniques for assessing the performance/reliability of digital systems on composite aircraft in that environment.

When an aircraft is struck by lightning, exterior electromagnetic fields are formed that are dependent on the geometry and structural material of the aircraft. These exterior fields are coupled to the interior of the aircraft causing transient voltages and currents to be induced on electrical cables throughout the aircraft. Onboard electronic equipment are subjected to the analog electrical transients that manage to propagate to interface circuitry, power lines, etc., despite shielding and protection devices (1)*.

Lightning-induced electrical transients can impair the operation of digital systems by either damaging components or by causing functional error modes--or upsets--in which no component damage is involved. Digital system upset is permanent in that it requires corrective action, such as resetting the system or reloading the software, to restore normal system function. Upset can be viewed from a hardware or software perspective. The hardware viewpoint is in terms of logic states, whereas the software viewpoint is in terms of program flow. There has been some ongoing work for several years to predict erroneous loop program execution using linear difference equations (2). However, there are no standard guidelines or criteria for performing upset tests or analysis of digital systems.

This paper describes a methodology whereby a microcomputer is tested in the laboratory for its susceptibility to entering upset modes and presents data obtained to date. The objectives of these tests are to investigate the

*Numbers in parentheses designate References at end of paper.

statistical nature of digital system response to analog transients and to verify potential analytical techniques for generating upset statistics for use in upset reliability models. An analytical approach for generating such statistics is based on the utilization of a special-purpose computer specifically designed to emulate and perform error mode diagnostics on a target computer (3). Once these statistics are generated and an upset model is designed, a reliability prediction can be made for the performance of the target computer, assuming that lightning-induced transients have entered the system. This reliability prediction could be generated by using existing reliability estimation programs, such as the Computer-Aided Reliability Estimation code, CARE III (4). In order to predict the reliability of the target system on an aircraft flying in a lightning-charged environment, in-flight data is needed to aid in defining the characteristics of that environment. This data is currently being obtained by tests in which a specially-instrumented aircraft is flown through thunderstorms to elicit lightning strikes (5). This lightning data, as well as data obtained through upset testing described in this paper, will aid in providing a basis from which analytical reliability prediction techniques can evolve.

UPSET TEST METHODOLOGY

The digital unit under test is the Intel Intellec 8/Mod 80 microcomputer. It is based on an 8080 microprocessor and was chosen because it is a typical, general-purpose microcomputer and comprises a small enough network to facilitate instrumentation. A simplified block diagram of the digital unit

under test is shown in Figure 1. The analog electrical transients being input into the digital unit under test are designed to model voltages and currents that are likely to be induced by electromagnetic fields in a lightning-charged environment; the waveshapes are based on those recommended for direct application to electronic equipment pins by avionics subcommittee AE4L of the Society of Automotive Engineers (6). These waveshapes, shown in Figure 2, are representative of lightning-induced voltages and currents and it is recommended that both positive and negative polarity versions of the waveforms be applied to the test unit. The amplitude of these waveforms is restricted, in this case, by the damage threshold of components within the unit under test. The analog transients are input into the digital unit under test randomly with respect to time and with respect to internal processing state of the unit being tested. Randomness is desired so that transient signal inputs are not synchronized with processing activity--thus, more realistically simulating the random process that might take place in the actual lightning-charged environment. Upset statistics collected under these conditions will enable statistical cross-tabulations to be made and will enhance a stochastic upset model in which digital system response to lightning-induced transients is modeled statistically.

The upset test hardware configuration shown in Figure 3 is based on comparison monitoring of two identical Intel microcomputers that are synchronized and executing the same program code concurrently. One microcomputer, the unit under test, is perturbed by analog electrical transients while the second one serves as an unperturbed reference unit.

Thirty-two of the forty pins from each microcomputer's central processing unit (CPU) are compared via error detection circuitry, in a bitwise fashion. These lines include the 8-bit bidirectional data bus, the 16-bit address bus, and eight CPU control lines. The analog electrical transients are generated when a relay is opened causing a capacitor in an RLC circuit to discharge; closing the relay causes the capacitor to again become charged, which is required for generating another transient signal. The random generation of the electrical transient is provided by circuitry that controls the opening and closing of the relay independently of either the unit under test or the reference unit. Transient signals can also be generated in a free-running manner in which the time between transients varies pseudo-randomly from about 5 seconds to 1.5 minutes with a resolution of approximately 350 ms. This time interval between transients can be adjusted and was chosen somewhat arbitrarily. The lower limit of 5 seconds, however, was chosen to provide enough time for a program of moderate size (about 500 instructions) to be executed in a continuous loop at least 1000 times. It is assumed that if the unit under test can correctly execute the program code 1000 times, once the transient signal has entered the system, then an error due to that transient signal will probably not occur. If no error is detected, the electrical transient is again input to the unit under test. If an error is detected, no more transient signals are generated, error data is recorded, and the test is finished.

The error data being recorded is obtained from the CPU lines that are monitored from the unit under test. These data comprise the memory addresses accessed, instructions fetched from memory, CPU data input/output (I/O), eight

CPU control signal logic states during CPU-memory data bus transactions, and the CPU status signal. The status signal is output onto the data bus by the CPU to identify the subsequent machine cycle. The 8080 microprocessor machine cycles and corresponding 8-bit status signals are shown in Table 1.

In order to statistically evaluate the effects of analog transients on the unit under test, data is generated and recorded to provide a means of determining the CPU processing state when each electrical transient was input into the test unit. This data is obtained using a 28-bit counter that is clocked by $\emptyset_1$ from the reference unit. Since processing activity is organized in the 8080 as shown in Table 2 (7), a count of the number of clock cycles that occur between transient signal inputs can be used to determine the instruction, machine cycle, and machine cycle state in progress when each transient input occurs. The clock cycle count is initialized when the microcomputers begin executing the program code. When the electrical transient is input into the unit under test, the clock cycle count is latched, the counter is reinitialized, and the clock cycle data is recorded. This process continues until an error is detected. Once the detection of an error occurs, the number of clock cycles that elapsed since the electrical transient was input into the test unit is latched, and the error data described previously is recorded.

Clock cycle data and error data are recorded on 8 x 8K bit nonvolatile random access memory cards. After each test is completed, the data on these memory cards is transcribed for permanent record onto magnetic tape and become data files. The data in these files is then processed using a specially

written FORTRAN program. Error data from the CPU data bus, address bus, and control lines of the unit under test are disassembled, formatted, and listed so that concurrent activity on these lines can be tracked. Clock cycle data is used to calculate the 8080 instruction, machine cycle, and machine cycle state in progress when each transient signal was injected and when the error was detected.

UPSET TESTS AND RESULTS

Upset tests completed to date have been performed utilizing a 1-MHz damped sinusoid of negative polarity as the perturbing electrical transient. No provisions have been made, at this time, to achieve the rise time of the S.A.E. recommended waveform. During each individual test, the analog transient signal was input on a single line in the unit under test, rather than on multiple lines throughout the unit. The program being executed in a continuous loop by the microcomputers during each test is shown in Table 3; the machine cycle, machine cycle states, and control signal corresponding to each instruction are indicated. The program causes data byte $(CB)_{16}$ to be retrieved from random access memory location $(0011)_{16}$ and input into the accumulator register of the CPU. The data byte is then stored in random access memory location $(0023)_{16}$. This program is extremely simplistic and was chosen to minimize the number of processing states to which the input of electrical transients could be correlated in a statistical analysis. Minimizing the number of processing states reduces the amount of data needed

for a statistically significant data base. Thus, a precursory analysis can be performed in a relatively short period of time to determine whether or not a correlation may exist.

The transient signal has been input into the unit under test 1101 times on lines MDI_0, MDI_3, and MDI_7 of the input data bus, DB_0 of the output data bus, D_0 of the bidirectional data bus, and MAD_0 of the memory address bus. Thirty-five of these analog transient inputs caused the unit under test to exhibit anomalous behavior, and in 30 of these cases the system was upset. The remaining five cases involved errors that have been termed as benign. Benign errors include contaminated data, temporary divergence from correct program flow, and slight instruction changes that do not prevent the system from performing the desired activity. Data recorded during the 30 tests in which the unit under test was operating in an upset mode can be categorized into three types. Type I upset data is characterized by the CPU data bus, and sometimes the address bus and/or control lines, being "stuck" at some valid or invalid sequence. Type II upset data indicates that the CPU of the unit under test was "babbling" erroneous information on the data bus, control lines, and usually the address bus as well. Table A of the appendix shows Type II upset data. Type III upset data suggests that the CPU exhibits a pattern of behavior during which it completes several program cycles correctly and then "babbles" or becomes "stuck" during several cycles. The amount of processing activity, such as CPU-RAM interaction, taking place during each upset mode is yet to be determined. The number of times that the transient signal was input on each line in the unit under test as well as the corresponding number of anomalies, benign errors, upset modes, and upset types detected are shown in Table 4.

Several general observations can be made from the upset data recorded thus far. Eight-bit signals are input into the CPU during some instruction fetch cycles that do not correspond to instructions in the test program or even represent the op-code for any of the 8080's 244 instructions. Similarly, the CPU issues status signals that do not correspond to the machine cycles which constitute execution of the test program and often do not signify any of the ten 8080 machine cycles. The CPU also issues signals on the address bus which represent memory locations in RAM other than those that should be accessed during execution of the program, memory locations in ROM, and sometimes locations outside the boundary of available hardware. In addition, control signals are issued by the CPU that either should not occur during execution of the test program or that should not occur during CPU-memory data bus transactions. This undefined CPU activity has not yet been investigated. In 18 of the 30 upset cases recorded, normal function was restored by resetting the system. In the remaining 12 cases, some or all of the memory locations allocated for the test program were overwritten requiring that the program be reloaded and initialized to restore normal system function. This information, as it relates to the number of upsets detected and the number of times the transient was input on each line of the unit under test, is included in Table 5.

The data base obtained to date is insufficient for performing a comprehensive statistical analysis to determine if the occurrence of upset can be correlated to the 8080 processing state in progress when the analog transient signal is input into the system. Nonetheless, several rudimentary

cross-tabulations were performed in which the number of observed upsets was arranged in contingency tables with several processing state subdivisions and the occurrence or nonoccurrence of upset as the random variables. The initial hypothesis being tested by each cross-tabulation is that the occurrence of upset is equi-probable for each processing state in progress when the electrical transient was input into the system. Calculating the chi-square statistic and comparing it to the appropriate value of the chi-square distribution determines whether or not the initial hypothesis should be rejected (8). Since the occurrence, rather than nonoccurrence, of upset is of primary interest, the chi-square statistic for the data in each contingency table was calculated using only the number of upsets observed and the number of upsets that would be expected to occur under the initial hypothesis for each processing state. An assumption that is implicit in the chi-square calculation for the data in each contingency table is that upset occurred with equal probability for each transient signal input point that yielded an observed upset. This assumption cannot be tested at this time due to the small quantity of data that has been obtained thus far. Tables 6-10 show the number of observed upsets, the number of upsets expected under the initial hypothesis, the calculated chi-square statistic, and appropriate values of the chi-square distribution as applied to various processing levels. Since the calculated chi-square statistic for the data in contingency Table 6 is less than the value of the chi-square distribution for an $\alpha = 0.10$ level of significance, the initial hypothesis--that the occurrence of upset is equi-probable when the transient signal is input during execution of any instruction of the test

program--cannot be rejected. On the other hand, the calculated chi-square statistic for the data as arranged in contingency Tables 7, 8, and 9 for various machine cycle categories indicates that the initial hypothesis of there being an equal probability that upset will occur when the transient signal is input during the various machine cycles, irrespective of the associated program instruction being executed, can be rejected at an $\alpha = 0.005$ level of significance. This level of significance means that the probability of having rejected the initial hypothesis when, in actuality, it should not be rejected is 0.005. Rejecting the initial hypothesis for the data in contingency Table 7 can primarily be attributed to the much smaller than expected number of observed upsets that occurred when the transient signal was input during memory write machine cycles. Rejection of the initial hypothesis for the data as arranged in contingency Tables 8 and 9 can primarily be attributed to the larger than expected number of upsets observed when the transient signal was input during instruction fetch machine cycles. The chi-square statistic calculated for the data in contingency Table 10 indicates that there is no basis on which to reject the initial hypothesis of there being an equal probability of upset occurring when the transient signal is input during various machine cycle states, irrespective of the associated machine cycle or instruction. A more complete statistical analysis associating instruction, machine cycle, and machine cycle state will be performed once a larger data base has been obtained.

A preliminary upset model has been developed and is presented in Figure 4. The probability of being in each of the defined states can be determined once the probability density functions (pdf's) $\rho(t)$, $\alpha(t)$, $\beta(\tau)$ and $\sigma(\tau)$ are determined for a specific digital system being considered. Function $\rho(t)$ is the pdf of the time it takes for upset to occur, once the transient signal has entered the system. Similarly, $\alpha(t)$ is the pdf of the time required, once the transient signal has entered the system, for benign errors to be generated. Functions $\sigma(\tau)$ and $\beta(\tau)$ are the pdf's of the time required for system recovery or system failure, respectively, once system upset has occurred. Probability density functions $\rho(t)$ and $\alpha(t)$ will be determined for the 8080-based microcomputer using upset test data currently being obtained. The clock cycle counter in the upset test circuitry is reinitialized when the transient signal is input into the test system, and the clock cycle count is latched and recorded upon detection of an error. Since the clock frequency is 2 MHz, the time required for upset to occur or benign errors to be generated, once the transient signal has entered the system, can be calculated by multiplying the clock cycle count by 500 ns. The upset propagation times calculated from each test in which upset occurred will be used to generate a histogram showing frequency of upset occurrence versus various upset propagation time intervals. Function $\rho(t)$ is then determined by approximating the histogram with a known distribution or deriving the equation of the curve which best fits the envelope of the histogram. Figure 5 shows the upset propagation time histogram formulated from the upset data obtained to date. Since the data base is small, no attempt has yet been made

to determine $\rho(t)$. Probability density function $\alpha(t)$ for benign error generation time will be determined in a similar manner. The pdf's $\sigma(\tau)$ and $\beta(\tau)$ for recovery time and failure time, respectively, cannot be determined unless upset recovery mechanisms are designed and implemented in the microcomputer system. If this is undertaken, pdf's $\sigma(\tau)$ and $\beta(\tau)$ will be determined similarly.

SUMMARY AND CONCLUSIONS

A methodology has been developed to test a general-purpose microcomputer for susceptibility to upset caused by analog transient signals which model lightning induced effects waveforms. Upset data has been obtained during 30 of 1101 transient signal injection tests and indicates that there are several distinct upset modes. Type I upset involves CPU lines and/or buses being stuck at some logic state sequence whereas, during Type II upset, the CPU "babbles" erroneous and/or undefined information on its lines and buses. Type III upset occurs when the CPU exhibits a pattern of behavior during which it completes several program cycles correctly and then "babbles" or becomes "stuck" during several cycles. Processing activity taking place during upset modes is yet to be investigated. Statistics performed thus far do not refute the claim that upset occurs with equal probability when the transient signal is input during each instruction cycle. However, there is evidence against the occurrence of upset being equi-probable when the transient signal is input during the machine cycles that occur throughout execution of the test program, irrespective of the instruction cycle in progress. At this time, there is no evidence to disclaim

the assertion that upset occurs with equal probability when the transient is input during the various machine cycle states, irrespective of the associated machine cycle or instruction cycle. A more comprehensive statistical analysis will be performed once a sufficient data base has been obtained. Upset test data will also be used to determine probability density functions of the time it takes for upset to occur and benign errors to be generated in the 8080-based microcomputer, once the analog electrical transient has entered the system. These probability density functions will be used to determine the upset susceptibility of the 8080 microcomputer via a preliminary upset reliability model that has been developed. Although extensive upset testing has not been completed, the primary conclusion that can be made at this time is that digital system upset may best be characterized at the machine cycle level of processing activity.

REFERENCES

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3. Gerard E. Migneault, "Emulation Applied to Reliability Analysis of Reconfigurable, Highly Reliable, Fault Tolerant Computing Systems for Avionics." NASA TM 80090, April 1979.

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7. Intellec 8/Mod 80 Microcomputer Development System Reference Manual, Intel Corp., 1974.

8. S. Wilks, "Mathematical Statistics." John Wiley and Sons, Inc., New York, 1962.

Table 1 - 8080 Machine Cycles and Corresponding 8-Bit Status Signals in Hexidecimal Format

MACHINE CYCLE	STATUS SIGNAL
INSTRUCTION FETCH	A2
MEMORY READ	82
MEMORY WRITE	00
STACK READ	86
STACK WRITE	04
INPUT	42
OUTPUT	10
INTERRUPT	23
HALT	8A
INTERRUPT WHILE HALT	2B

Table 2 - Processing Levels for the 8080 Microprocessor

PROCESSING LEVEL	COMMENTS
INSTRUCTION CYCLE	1. Defined by op-code for each 1-3 byte instruction 2. Consists of 1-5 machine cycles
MACHINE CYCLE	1. Identified by status signal for type of CPU-memory or CPU-I/O port transaction 2. Consists of 3-5 states
MACHINE CYCLE STATES	1. Defined by single cycle of clock signal ϕ_1 2. Smallest unit of processing activity

Table 3 - Address Bus, Data Bus, and Control Signal Activity During Execution of the Upset Test Program Code

ADDR. BUS	DATA BUS OP.CODE/INST.	STATUS SIG./MACH. CYC.	NO. OF STATES	CPU CONTROL SIGNAL WAIT	RDY	HLDA	SYNC	$\overline{WR}$	DBIN	INTE	HLD
0010	3E: MVIA	A2: INST. FETCH	5	1	1	0	0	1	1	0	0
0011	CB: CB	82: MEM. READ	4	1	1	0	0	1	1	0	0
0012	32: STA	A2: INST. FETCH	5	1	1	0	0	1	1	0	0
0013	23: 23	82: MEM. READ	4	1	1	0	0	1	1	0	0
0014	00: 00	82: MEM. READ	4	1	1	0	0	1	1	0	0
0023	CB	00: MEM. WRITE	4	1	1	0	0	0	0	0	0
0015	C3: JMP	A2: INST. FETCH	5	1	1	0	0	1	1	0	0
0016	10: 10	82: MEM. READ	4	1	1	0	0	1	1	0	0
0017	00: 00	82: MEM. READ	4	1	1	0	0	1	1	0	0

Table 4 - Breakdown of System Anomalies Observed Per Number of Transient Signal Inputs at Each Input Point in the Unit Under Test

TRANSIENT INPUT POINT	NO. OF TRANSIENT INPUTS	SYSTEM ANOMALIES	BENIGN ERRORS	TOTAL	SYSTEM UPSETS		
					TYPE I	TYPE II	TYPE III
MDI_0 (MEM. DATA IN.-LSB)	11	11	3	8	2	4	2
MDI_3 (MEM. DATA IN.-4th LSB)	11	11	0	11	0	11	0
MDI_7 (MEM. DATA IN.-MSB)	11	11	1	10	1	9	0
D_0 (CPU DATA BUS-LSB)	2	2	1	1	0	0	1
DB_0 (DATA BUS OUT.-LSB)	720	0	0	0	0	0	0
MAD_0 (MEM. ADDR. BUS-LSB)	346	0	0	0	0	0	0

Table 5 - Upsets Involving Overwritten Program Memory Per Total Number of Upsets Observed from Transient Signal Inputs at Each Input Point in the Unit Under Test

TRANSIENT INPUT POINT	NO. OF TRANSIENT INPUTS	TOTAL NO. OF UPSETS	UPSETS INVOLVING OVERWRITTEN PROGRAM MEMORY
MDI_0	11	8	3
MDI_3	11	11	2
MDI_7	11	10	7
D_0	2	1	0

Table 6 - Contingency Table and Chi-Square Statistic for the Occurrence of Upset When the Transient Signal is Input During Instruction Cycles

	MVIA	STA	JMP	
NO UPSET	245	473	353	1071
UPSET (EXPECTED)	12 (10.0)	9 (10.0)	9 (10.0)	30
TOTAL	257	482	362	1101

CALCULATED $\chi^2 = 0.6$

$\chi^2_{\alpha = 0.10} = 4.61$ $\chi^2_{\alpha = 0.05} = 5.99$

Table 7 - Contingency Table and Chi-Square Statistic for the Occurrence of Upset When the Transient Signal is Input During Machine Cycles

	INST. FETCH	MEM. READ	MEM. WRITE	
NO UPSET	392	562	117	1071
UPSET (EXPECTED)	15 (10.0)	14 (10.0)	1 (10.0)	30
TOTAL	407	576	118	1101

CALCULATED $\chi^2 = 12.2$

$\chi^2_{\alpha = 0.05} = 5.99$ $\chi^2_{\alpha = 0.005} = 10.6$

Table 8 - Contingency Table and Chi-Square Statistic for the Occurrence of Upset When the Transient Signal is Input During Machine Cycles (Memory Read Cycles are Subclassified Into Data and Addresses Read from Memory)

	INST. FETCH	MEM. RD. (DATA)	MEM. RD. (ADDR.)	MEM. WRITE	
NO UPSET	392	110	452	117	1071
UPSET (EXPECTED)	15 (7.5)	6 (7.5)	8 (7.5)	1 (7.5)	30
TOTAL	407	116	460	118	1101

CALCULATED $\chi^2 = 13.43$

$\chi^2_{\alpha = 0.05} = 7.81$ $\chi^2_{\alpha = 0.005} = 12.8$

Table 9 - Contingency Table and Chi-Square Statistic for the Occurrence of Upset When the Transient is Input During Machine Cycles (Memory Read Cycles are Subclassified into Data, Low Address Bytes, and High Address Bytes Read from Memory)

	INST. FETCH	MEM. RD. (DATA)	MEM. RD. (LOW BYTE OF ADDR.)	MEM. RD. (HIGH BYTE OF ADDR.)	MEM. WRITE	
UPSET	392	110	218	234	117	1071
NO UPSET (EXPECTED)	15 (6.0)	6 (6.0)	3 (6.0)	5 (6.0)	1 (6.0)	30
TOTAL	407	116	221	239	118	1101

CALCULATED $\chi^2 = 19.37$

$\chi^2_{\alpha = 0.05} = 9.49$ $\chi^2_{\alpha = 0.005} = 14.9$

Table 10 - Contingency Table and Chi-Square Statistic for the Occurrence of Upset When the Transient Signal is Input During Machine Cycle States

	T1	T2	TW	T3	T4	
NO UPSET	249	268	255	223	76	1071
UPSET (EXPECTED)	9 (6.0)	7 (6.0)	6 (6.0)	5 (6.0)	3 (6.0)	30
TOTAL	258	275	261	228	79	1101

CALCULATED $\chi^2 = 3.34$

$\chi^2_{\alpha = 0.1} = 7.78$ $\chi^2_{\alpha = 0.05} = 9.49$

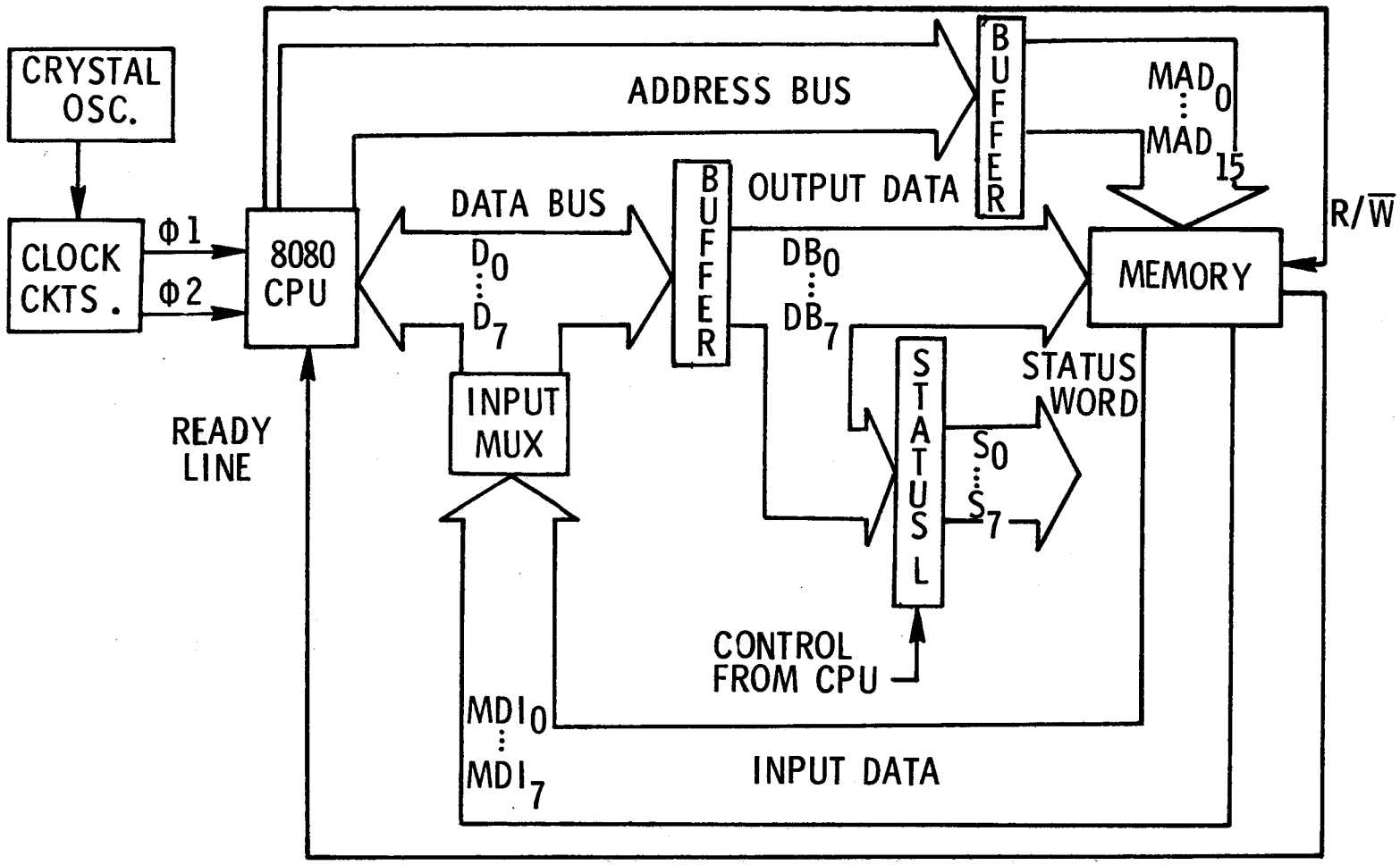


Figure 1. - Overview of digital unit under test (8080-based microcomputer).

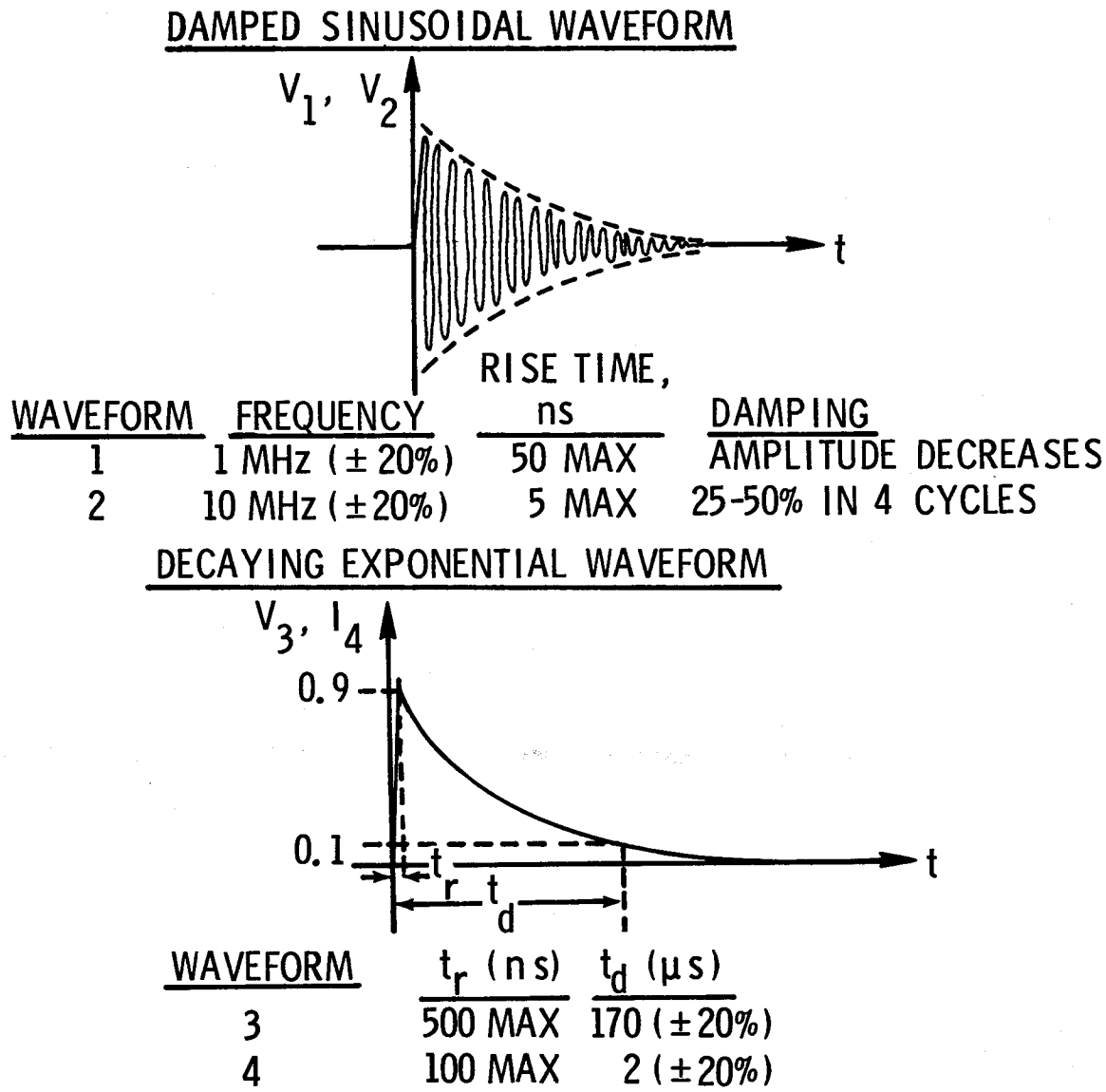


Figure 2. - S.A.E. waveforms recommended for lightning-induced effects testing.

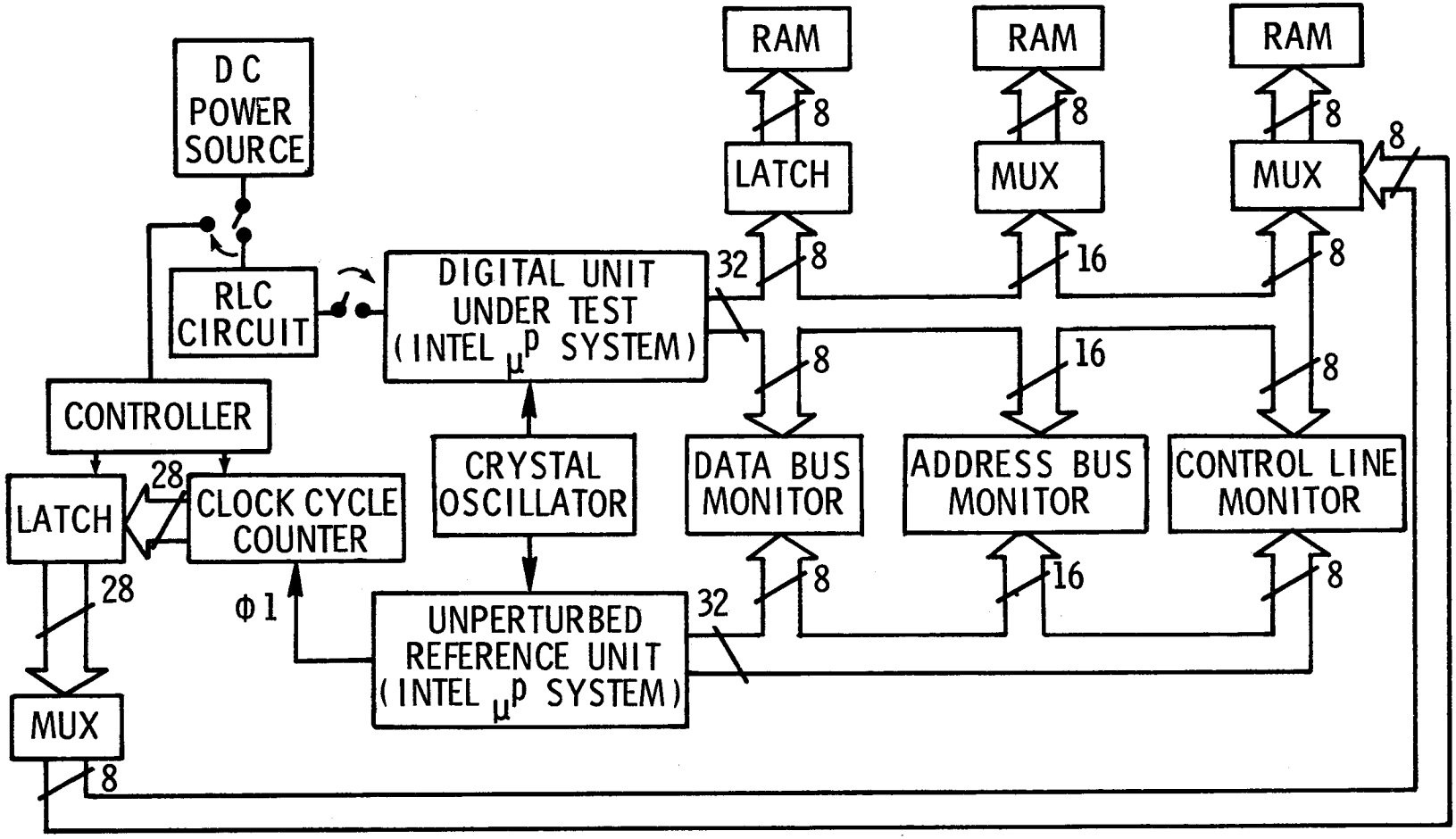
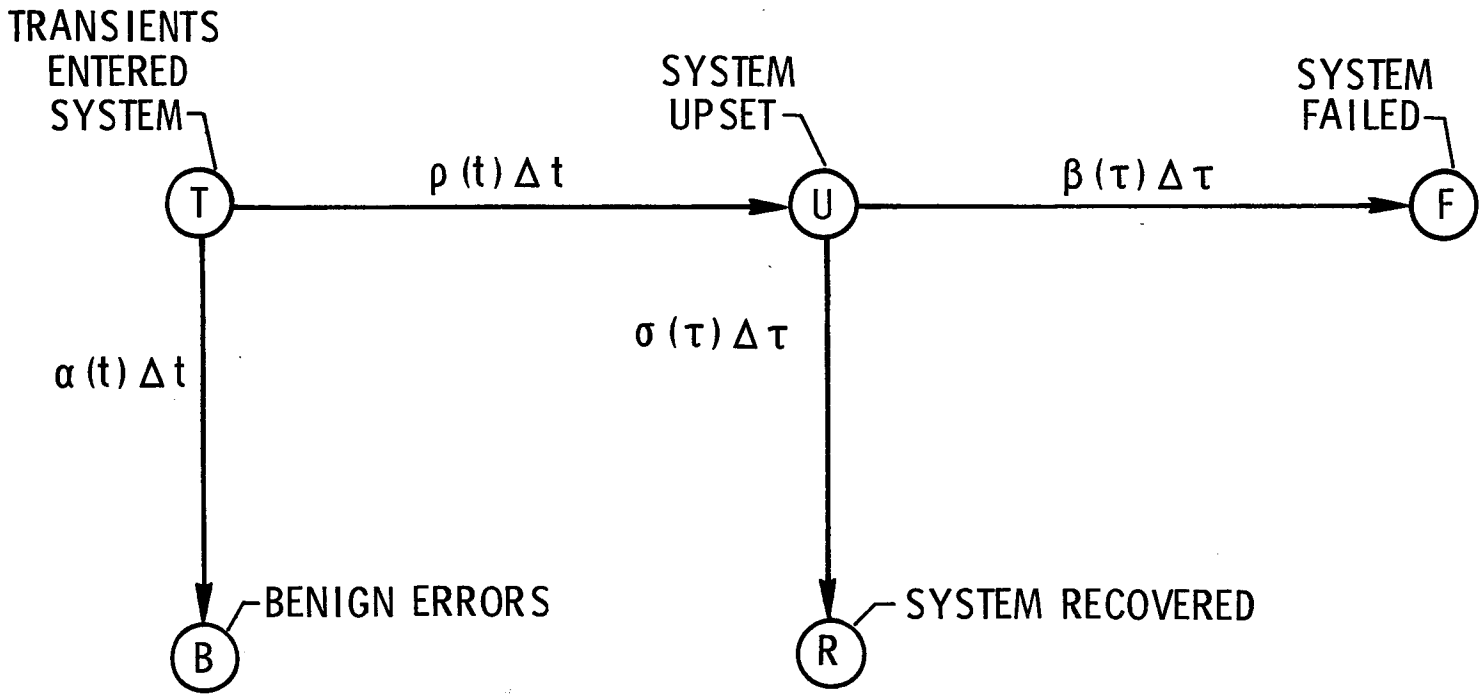


Figure 3. - Overview of upset test hardware configurations.



$\rho(t)\,\Delta t$ = PROBABILITY THAT ERRORS CAUSE SYSTEM UPSET IN TIME Δt
$\alpha(t)\,\Delta t$ = PROBABILITY THAT ERRORS WILL BE BENIGN IN TIME Δt
$\sigma(\tau)\,\Delta \tau$ = PROBABILITY THAT SYSTEM WILL RECOVER IN TIME $\Delta \tau$
$\beta(\tau)\,\Delta \tau$ = PROBABILITY THAT SYSTEM WILL FAIL IN TIME $\Delta \tau$

Figure 4. - Preliminary stochastic upset model.

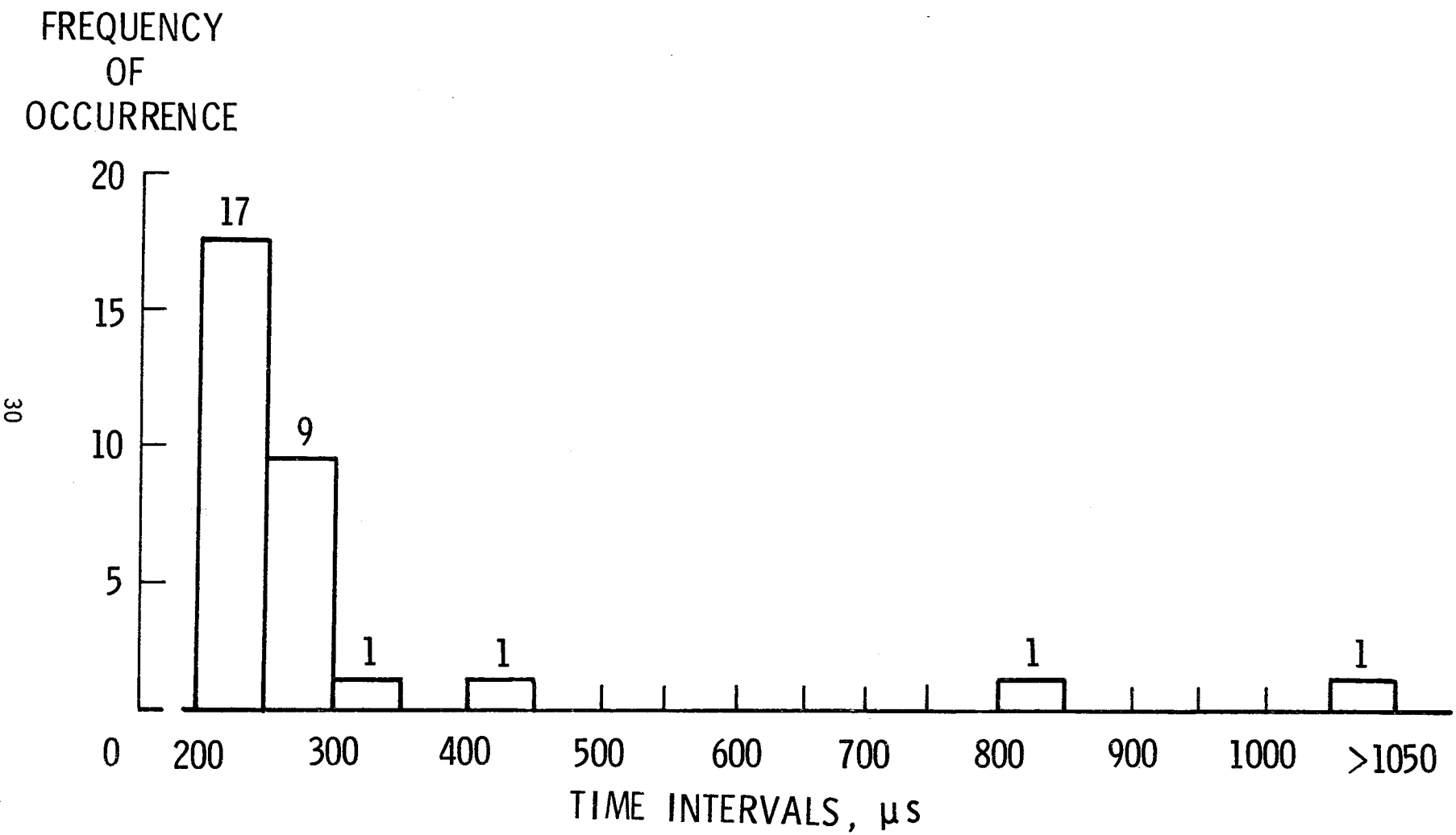


Figure 5. - Upset detection/propagation time histogram.

APPENDIX : TABLE A - UPSET TYPE II DATA EXCERPT (TRANSIENT INPUT POINT - MDI0; CPU STATE DURING TRANSIENT INPUT - JMP 0010,INST.FETCH,TW; UPSET DETECTION/PROPAGATION TIME - 228.5 US; PROGRAM MEMORY WAS NOT OVERWRITTEN)

STATUS WORD	MEMORY ADDRESS	DATA BUS I/O	CONTROL SIGNAL WAIT	RDY	HLDA	SYNC	WRNOT	DBIN	INTE	HLD
82: MEM. READ	0014	00: NOP	0	1	0	0	1	0	0	0
00: MEM. WRITE	0023	CB: ******	0	1	0	0	1	1	0	0
A2: INST.FETCH	0015	C3: JMP	1	0	0	1	0	0	0	0
82: MEM. READ	0016	10: ******	1	0	0	1	0	1	0	1
82: MEM. READ	0017	00: NOP	1	0	0	1	0	0	0	0
A2: INST.FETCH	0018	20: ******	1	0	0	1	0	1	0	1
A2: INST.FETCH	0019	01: LXI B	1	0	0	1	0	0	0	0
FF: **********	0020	20: ******	1	0	0	1	0	1	0	1
82: MEM. READ	011A	01: LXI B	1	0	0	1	0	0	0	0
A2: INST.FETCH	001C	20: ******	1	0	0	1	0	1	0	1
FF: **********	0010	01: LXI B	1	0	0	1	0	0	0	0
FD: **********	001D	82: ADD D	1	0	0	1	0	1	0	1
AE: **********	001E	01: LXI B	1	0	0	1	0	0	0	0
FF: **********	001F	CB: ******	1	0	0	1	0	1	0	1
CA: **********	0020	82: ADD D	1	0	0	1	0	0	0	0
CB: **********	0021	CB: ******	1	0	0	1	0	1	0	1
CB: **********	0022	FF: RST 7	1	0	0	1	0	0	0	0
FF: **********	00CA	04: INR B	1	0	0	1	0	1	0	1
CB: **********	21C9	04: INR B	1	0	0	1	0	0	0	0
CC: **********	21C8	A2: ANA D	1	0	0	1	0	1	0	1
20: **********	2138	FF: RST 7	1	0	0	1	0	0	0	0
01: **********	0039	FF: RST 7	1	0	0	1	0	1	0	1
20: **********	003A	20: ******	1	0	0	1	0	0	0	0
01: **********	003B	00: NOP	1	0	0	1	0	1	0	1
20: **********	003C	FF: RST 7	1	0	0	1	0	0	0	0
01: **********	003D	00: NOP	1	0	0	1	0	1	0	1
20: **********	003E	20: ******	1	0	0	1	0	0	0	0
01: **********	003F	00: NOP	1	0	0	1	0	1	0	1
20: **********	0040	20: ******	1	0	0	1	0	0	0	0
A2: INST.FETCH	0041	00: NOP	1	0	0	1	0	1	0	1
A2: INST.FETCH	0042	20: ******	1	0	0	1	0	0	0	0
FF: **********	0038	01: LXI B	1	0	0	1	0	1	0	1
FE: **********	0043	A2: ANA D	1	0	0	1	0	0	0	0
AF: **********	0044	A2: ANA D	1	1	0	0	1	1	0	0
01: **********	0045	FF: RST 7	1	0	0	1	0	0	0	0
20: **********	0046	82: ADD D	1	0	0	1	0	1	0	1
01: **********	0047	A2: ANA D	1	0	0	1	0	0	0	0
20: **********	0048	FF: RST 7	1	1	0	0	1	1	0	0
01: **********	0049	00: NOP	1	0	0	1	0	0	0	0
20: **********	004A	20: ******	1	0	0	1	0	1	0	1
A2: INST.FETCH	004B	01: LXI B	1	0	0	1	0	0	0	0
FF: **********	0020	20: ******	1	1	0	0	1	1	0	0
82: MEM. READ	0140	00: NOP	1	0	0	1	0	0	0	0
A2: INST.FETCH	004E	20: ******	1	0	0	1	0	1	0	1
A2: INST.FETCH	004F	00: NOP	1	0	0	1	0	0	0	0
FF: **********	0038	20: ******	1	0	0	1	0	1	0	1
AE: **********	0050	A2: ANA D	1	0	0	1	0	0	0	0
00: MEM. WRITE	0051	FF: RST 7	0	0	0	0	0	0	0	0
20: **********	0052	82: ADD D	1	0	0	1	0	0	0	0
01: **********	0053	A2: ANA D	1	1	0	0	1	1	0	0
20: **********	0054	FF: RST 7	1	0	0	1	0	0	0	0

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15. Supplementary Notes

16. Abstract

Flight-critical computer-based control systems designed for advanced aircraft must exhibit ultrareliable performance in lightning-charged environments. Digital system upset can occur as a result of lightning-induced electrical transients, and a methodology has been developed to test specific digital systems for upset susceptibility. Initial upset data indicates that there are several distinct upset modes and that the occurrence of upset is related to the relative synchronization of the transient input with the processing state of the digital system. A large upset test data base will aid in the formulation and verification of analytical upset reliability modeling techniques which are being developed.

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