NEW TECHNOLOGY, INC.

P.O. Box 5245

Huntsville, Alabama 35805

FR1018
16 March 1983

FINAL REPORT

CONCEPTUAL DESIGN OF A DATA REDUCTION SYSTEM

Contract NAS8-32564

Prepared for:
National Aeronautics and Space Administration
George C. Marshall Space Flight Center
Marshall Space Flight Center, Alabama 35812

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Approved by:

C S Chang

FOREWORD

This final report summarizes results of work accomplished under Contract NAS8-32564, and is published in partial fulfillment of contract requirements.

The following personnel of New Technology, Inc. worked on various tasks: R.W. Baslock, C.S. Chang, R.E. Esterling, G.F. Hart, D.M. Nilson, G.A. Ramirez, W.B. Wilson, and R.N. Yerby.

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1.0 INTRODUCTION

The purpose of this project is to define a telemetry data processing system to meet current and projected future needs of the Data Reduction Branch (AH22) of the Huntsville Computer Complex, Computer Services Office, Administration and Program Support, of George C. Marshall Space Flight Center.

Formal analyses and projections of long-term data analysis requirements were not attempted in this study. Rather, data reduction activities in support of the developmental flights of the Space Shuttle during 1981 and 1982 were used as references against which future requirements are assessed in general terms. Results are discussed in Section 2.0 of this report.

A conceptual system design believed to offer significant throughput for the anticipated types of data reduction activities is presented in Section 3.0. The design identifies the use of a large, intermediate data store as a key element in a complex of high-speed, single-purpose processors, each of which performs predesignated, repetitive operations on either "raw" or partially processed data. The recommended approach to implement the design concept is to adopt an established interface standard and rely heavily on mature or promising technologies which are considered "main stream" of the integrated circuit industry.

During the course of the study, several new technologies (such as the VLSI approach to Systolic processing) which are under development by various independent sources were noted and considered for application in the system. The design system concept, however, is believed to be implementable without reliance on exotic devices and/or operational procedures.

Numerical methods were employed to examine the feasibility of digital discrimination of FDM composite signals, and of eliminating line frequency noises in data measurements. These studies led to positive results and are described in Sections 4.0 and 5.0, respectively.

Section 6.0 describes a general-purpose controller developed during this project. A prototype was built, tested and used in actual applications. This controller is very simple and versatile, and offers an avenue for achieving computer- and language-independent means of providing a large amount of control functions effectively. The recommended data system will do well to include and to rely on this controller concept.

2.0 A SURVEY OF DATA PROCESSING REQUIREMENTS

The objective of this initial task was to establish the data processing requirements and techniques of the Data Reduction Branch (AH22) of MSFC. Data processing for the Space Transportation System (STS) is a major part of near-term activities of the branch and, hence, represents an excellent measure of both requirements and methods. These are analyzed and summarized in Section 2.1.

Requirements for the first 20 STS missions were determined from available documentation. For these missions, 22 separate payload items were identified. Payload requirements are outlined in Section 2.2.

A third source of requirements is local MSFC development test programs. For the purpose of this study, initial data reduction requirements for the Bearing/Seal Material Test Program at MSFC were analyzed to develop a feel on typical data rates and volumes. Results of this study are presented in Section 2.3.

A sample of HOSC real-time PCM data was examined for compressibility. Results are reported in Section 2.4.

2.1 STS DATA REDUCTION REQUIREMENTS AND PROCESSING PROCEDURES

The STS program provided the bulk of the data to be processed in the 1981-1982 time span. MSFC was responsible for processing Development Flight (DF) data from the Main Engines (ME's), the External Tank (ET), and Solid Rocket Boosters (SRB's). It has backup status for the processing of Orbiter FDM, DF downlink and operational downlink data at 128 kbps.

Much of the following information was gathered from NASA program documentation (Refs. 1 through 17). Requirements for processing each Measurement Identification (MSID) are defined in the Operational Master Measurement Data Base Revision D, ICD-3-0068-02, published 27 June 1979.

Main engine data are generated during the ascent phase of the mission. Each of the three main engine controllers (MEC's) generates 128-word data

blocks using 16-bit words and 51.2 kbps bit rate (Ref. 1). These data blocks go to each main engine interface unit (EIU) at the rate of 25 samples per second. Four additional words are added for synchronization, built-in test status and parity. The EIU output is at 60 kbps. This is a greater bit rate than the data from the MEC including the four added 16-bit words. One of the EIU data blocks is therefore repeated approximately every eighth block to fill the 60 kbps data stream. Data from Engines 1, 2 and 3 are then fed in parallel to the Maintenance Recorder (Tracks 1, 2 and 3, respectively). Subcarrier oscillators are frequency modulated (FM) by the data and sent to the FM signal processor where they are added to form part of the modulation of the FM downlink during the ascent phase (only). During the on-orbit mission phase, the maintenance recorder is dumped via the FM downlink. This is accomplished one track at a time with alternate tracks being read forward and in reverse. The playback tape speed (120 ips) is 16 times faster than the recording speed, thus the engine data during dump is at 960 kbps. The data are dumped one track at a time. The dumped EIU data may be either two tracks forward and one track backward, or one track forward and two tracks backward. The dumped data are received by the Goldstone ground station.

During the ascent phase, ground stations at Ponce de Leon (PDL), Merritt Island Launch Area (MILA) and Bermuda (BDA) receive the FM downlink. Each ground station separates and demodulates the subcarriers and records in real time data for each engine on a separate tape track. The tape also contains the modified IRIG B time code, receiver AGC, Development Flight Instrumentation (DFI) FDM, DFI 128-kbps data and the IRIG 200-kHz reference as specified in tape format DSS 542 (Ref. 3). A tape format is specified for each ground station and data link for all mission phases. PDL, MILA and GBI generate 7-track, half-inch tapes of the same data, but each has a slightly different time coverage. These tapes are flown to MSFC on the next available transportation. As a result, the data arrival is spread over several days.

DFI data are recorded on the 14-track Ascent Recorder and the 28-track Mission Recorder located in the Orbiter, plus one 14-track Flight Recorder in each SRB. The Ascent and Mission Recorder data are dumped after landing, and

the data received at MSFC on 14-track tapes recorded at 30 ips. These tapes arrive about 24 hours after landing. The data tape from the SRB Flight Recorders is physically recovered from the SRB's after ocean recovery and return to KSC. These tapes are sent directly to MSFC's Huntsville Computer Complex (HCC).

Data from the Mission Recorder dump are received on two 14-track tapes which are recorded at 30 ips. One tape contains all the odd numbered Mission Recorder tracks while the other contains the even numbered tracks. The Mission Recorder data consist entirely of Orbiter FDM data. Data from the Ascent Recorder dump are on one 30 ips, 14-track tape. This tape contains seven Orbiter FDM tracks, five ET FDM tracks, and one FDM track from each SRB.

Digital input data from STS are listed in Table 2-1. The number of physical sources is the number of individual tape tracks containing the same data set. These are in the tapes from the ground station and the post-flight recorder dumps. The word rates shown in the table are representative of the data word rates and do not include overhead (sync, format ID, etc.).

Table 2-1 STS Digital Data

SOURCE	SOURCE ID	NUMBER OF MSID'S	NUMBER OF PHYSICAL SOURCES	BIT RATE (kbps)	WORD RATE (kwps)	SUPPORT TIME (hr)	DATA VOLUME PER SOURCE (Mbyte)
MAIN ENGINE NO. 1	EIU-1	182	4	60**	3.3	0.142	3.27
MAIN ENGINE NO. 2	EIU-2	182	4	60**	3.3	0.142	3.27
MAIN ENGINE NO. 3	EIU-3	182	4	60**	3.3	0.142	3.27
EXTERNAL TANK	ET	303	2	16	1.6	0.25	1.62
LEFT SRB	LP1	91	2	64	7.36	0.25	6.62
LEFT SRB	LP2	72	2	64	7.36	0.25	6.62
RIGHT SRB	RP1	91	2	64	7.36	0.25	6.62
RIGHT SRB	RP2	96	2	64	7.36	0.25	6.62
ORBITER	DFI	--	--	128	15.6	0.47*	26.4
ORBITER	OD	--	--	128	7.58	0.47*	12.8

* MAXIMUM TIME ON ONE ANALOG TAPE TRACK.

** BIT RATE FOR ON-ORBIT DUMP IS 960 kbps.

FDM data for STS are listed in Table 2-2. In cases where data are not to be processed at HCC (except on backup), the number of MSID's is not provided. The Orbiter FDM's can have up to 15 MSID's. Note there is only one source (post-flight recorder dump) for the Orbiter FDM's and four of five ET FDM's. The exact support time for the FDM data is not clearly specified. Characteristics of the FDM subcarriers are listed in Tables 2-3 through 2-5.

Each serial data tape received at HCC is copied ("dubbed") on one-inch, 14-track tape. Dubbing is done track for track. One tape copy is sent to Slidell Computer Center (SCC) (if required) and one or more are used for working copies in processing the data. The original data tape is then filed in a tape library.

The MILA tape is received first and is processed first. The data are serial on the tape with the 60 kbps data for Engines 1, 2 and 3 on Tracks 1, 4 and 7, respectively. The timing for the data (other than the encoded relative time) is on Track 6. Other data include the DFI FDM and 128 kbps as well as the 200-kHz reference frequency.

The tape is played back once for each engine, thus rewinding the tape is required between each playback. The engine 60 kbps PCM is bit synchronized, bit decoded (i.e., changed to NRZ code required by the frame synchronizer), and frame synchronized. The parallel output of the frame synchronizer is 16 bits wide. The modified IRIG B timing signal from Track 6 is decoded and multiplexed with the engine data.

Analog tapes received from the Goldstone ground station contain main engine data dumped at 960 kbps rate, in forward and backward directions. The backward data are retrieved by playing the tape in the reverse direction. Since the three streams of engine data are in series in serpentine fashion on the tape, only one can be processed at a time. Here, too, the tape must be rewound (at least partially) between engine data passes.

Digital data are recorded on disc and processed by either a Perkin-Elmer Model 8/32 or a Perkin-Elmer 3244 general-purpose minicomputer using a PCM Edit and Reduction (PER) Program. Sync errors are checked, missing

Table 2-2 STS FDM Analog Data

SOURCE	SOURCE ID	NUMBER OF MSID'S	NUMBER OF PHYSICAL SOURCES	SOURCE	SOURCE ID	NUMBER OF MSID'S	NUMBER OF PHYSICAL SOURCES
EXTERNAL TANK	T-1A	10	2	ORBITER	L-2B	--	1
EXTERNAL TANK	T-2A	13	1	ORBITER	L-2C	--	1
EXTERNAL TANK	T-2B	12	1	ORBITER	L-2D	--	1
EXTERNAL TANK	T-3A	12	1	ORBITER	F-1C	--	1
EXTERNAL TANK	T-3B	12	1	ORBITER	F-1D	--	1
LEFT SRB	B-1A	12	3	ORBITER	F-2A	--	1
LEFT SRB	B-1B	10	2	ORBITER	F-2B	--	1
LEFT SRB	B-3A	7	2	ORBITER	F-2C	--	1
LEFT SRB	B-3B	7	2	ORBITER	F-2D	--	1
RIGHT SRB	B-2A	14	3	ORBITER	F-3A	--	1
RIGHT SRB	B-2B	15	2	ORBITER	F-3B	--	1
RIGHT SRB	B-4A	14	2	ORBITER	F-3C	--	1
RIGHT SRB	B-4B	14	2	ORBITER	F-3D	--	1
ORBITER	C-1C	--	1	ORBITER	R-1A	--	1
ORBITER	C-1D	--	1	ORBITER	R-1B	--	1
ORBITER	L-1A	--	1	ORBITER	R-1C	--	1
ORBITER	L-1B	--	1	ORBITER	R-1D	--	1
ORBITER	L-1C	--	1	ORBITER	R-2A	--	1
ORBITER	L-1D	--	1	ORBITER	R-2B	--	1
ORBITER	L-2A	--	1	ORBITER	R-2C	--	1
				ORBITER	R-2D	--	1

Table 2-3 SRB FDM SCO Characteristics

INPUT CHANNEL NUMBER	CBW SCO NOMENCLATURE	CENTER FREQUENCY (kHz)	MAXIMUM DEVIATION (±kHz)	PRE-EMPHASIS (MV RMS ±15%)
1	NON-IRIG	12	0.5	66
2	NON-IRIG	14	0.5	66
3	NON-IRIG	16	0.5	66
4	NON-IRIG	20	1.0	95
5	NON-IRIG	24	1.0	175
6	NON-IRIG	28	1.0	95
7	NON-IRIG	32	1.0	175
8	IRIG-4A	40	2.0	175
9	IRIG-5A	48	2.0	175
10	IRIG-7B	64	4.0	245
11	IRIG-9B	80	4.0	245
12	IRIG-11B	96	4.0	245
13	IRIG-13B	112	4.0	245
14	IRIG-15B	128	4.0	245
15	NON-IRIG	184	16.0	580
REF. CH.	REF. OSC.	240	N/A	490

Table 2-4 ET FDM SCO Characteristics

INPUT CHANNEL NUMBER	CBW SCO NOMENCLATURE	CENTER FREQUENCY (kHz)	MAXIMUM DEVIATION (±kHz)	PRE-EMPHASIS (MV RMS +10%)
1	NON-IRIG	8	0.5	76
2	NON-IRIG	10	0.5	68
3	NON-IRIG	12	0.5	61
4	NON-IRIG	14	0.5	53
5	NON-IRIG	16	0.5	51
6	IRIG 2A	24	2.0	96
7	IRIG 3A	32	2.0	91
8	IRIG 5B	48	4.0	114
9	IRIG 7B	64	4.0	119
10	IRIG 9B	80	4.0	135
11	IRIG 11B	96	4.0	152
12	IRIG 13B	112	4.0	160
13	IRIG 15B	128	4.0	170
14	IRIG 19C	160	8.0	381
15	NON-IRIG	192	8.0	480
REF. CH.	REF. OSC.	240	N/A	681

Table 2-5 Orbiter FDM MUX 1-4 SCO Characteristics

INPUT CHANNEL NUMBER	CBW SCO NOMENCLATURE	CENTER FREQUENCY (kHz)	MAXIMUM DEVIATION (±kHz)	PRE-EMPHASIS (RELATIVE)
1	NON-IRIG	12	1	1.00
2	NON-IRIG	16	1	1.00
3	NON-IRIG	20	1	1.00
4	NON-IRIG	24	1	1.00
5	NON-IRIG	28	1	1.00
6	NON-IRIG	32	1	1.00
7	NON-IRIG	36	1	1.00
8	IRIG-5B	48	4	1.66
9	IRIG-7B	64	4	1.66
10	IRIG-9B	80	4	1.66
11	IRIG-11B	96	4	1.66
12	IRIG-13B	112	4	2.01
13	IRIG-15B	128	4	2.10
14	IRIG-17B	144	4	2.91
15	NON-IRIG	184	16	7.45
REF. CH.	REF. OSC.	240	N/A	10.60

time periods identified and blanks are stuffed with the last known acceptable data. It also deletes redundant frames which were added in the data stream at the Shuttle to accommodate the 60-kbps data rate. These redundant frames were added to fill the 60-kbps bit rate. (The actual frame rate is 25 per second, but 28.41 frames are transmitted each second.) Later, when analog tapes from Ponce de Leon and Grand Bahama Island arrive (somewhere between 12 and 48 hours later), they are searched for acceptable data for periods of "missing time" from MILA and the best source used. This produces the most complete time record of data.

Results of the PER are further processed. Here data are converted to engineering units using information from the Calibration Data Base. Data are also reformatted and recorded as a Telemetry User Tape (TUT). The TUT may be copied (dubbed) and sent to a user and/or operated on using the STDBP to put in the Shuttle Telemetry Data Base.

FDM data are handled in a similar way after the subcarrier demodulation and analog-to-digital conversion. Each analog signal is routed to a multiplexer. A single analog-to-digital converter (ADC) is used. A tape record is formatted which contains time (usually from another tape track) and the sampled data. As an alternative, the Automated Telemetry Ground Station Network (ATGSN) may be used, where up to three FDM composite signals can be processed simultaneously. The resulting digital data are directly put on discs for further processing. Tapes are not generated.

Other data products are oscillograms, data books and vibro-acoustic analyses. The oscillograms are made from data taken off the FDM analog tapes. Data books are generated using the STDB as the data source. Vibro-acoustic analyses are done using the raw data tape.

2.2 PAYLOAD DATA REDUCTION REQUIREMENTS

A large part of future data processing support to be provided by AH22 may well be for Shuttle payloads. These payloads were ascertained from the STS Flight Assignment Baseline (Ref. 5). This document identifies STS payloads through Flight 68 scheduled for September 1986. Some payloads such as those for the Department of Defense (DoD) may not be supported by NASA because of their classified nature. Some payloads were listed as "payloads of opportunity," which are currently undefined. They are normally payloads which are designed to fly within the power, space, weight, telemetry and other resources remaining after other scheduled payloads are totally defined. In general, payloads fall into two categories: detachable and nondetachable. The first four flights have nondetachable payloads such as DFI, OSS and OSTA-1. Subsequent flights will have detachable payloads such as the Tracking and Data Relay Satellite (TDRS), SBS-C, Telesat-E, Intelset-A (F5), Space Telescope and Galileo Orbiters. Some of these detachable payloads use boosters to attain different orbits. These boosters, such as IUS and SSUS, are considered as separate payloads even though they work in conjunction with other payloads. Once the booster requirement is defined for the first use, it is considered to be essentially unchanged for following use. The SSUS, for example, will be used 10 times in the first 20 flights.

Definitions of data rates and types are found in the Johnson Space Center Series 14,000 documents entitled Orbiter Command and Data Annex. Each payload has its own annex. The OFT Pallet data are described in JSC 14,017 Orbiter Command and Data Annex, Annex 4, OFT Pallet System Carrier (Ref. 13). However, to get an idea of the data volume for the mission, flight operations were studied during this task. These are found in JSC 14,017 OFT Pallet Carrier, Preliminary Flight Operations Support Annex, Annex 3, 4 January 1980 (Ref. 14).

In the same way, requirements were determined for detachable payloads. The TDRS payload is separated from the Orbiter after two series of checks in the payload bay. The TDRS is released from the Orbiter and, while still in close proximity, additional checks are made. TDRS data go through

the Orbiter system during all these checks. Finally, the Orbiter moves about 1 km from the TDRS, the TDRS changes altitude, and the IUS booster is fired to put it in geostationary orbit. Based on the flight operations support plan, it is estimated that about six hours of data support would be required. Documentation for the other separable payloads was not as detailed as that for the TDRS. The six-hour support estimate, therefore, is used for the other detachable payloads using boosters.

The volume of data to be processed is estimated by the product of the data word rate times the support time. Data bit rates are reasonably well defined. The actual rate for information-bearing data is not. For example, the Operational downlink transmits one major frame per second at 128 kbps. Of this, 60.752 kbps are assigned for payload use. This corresponds to 7,594 8-bit words, of which 14 are overhead. There are then only 7,580 8-bit words per major frame available to a payload. If a particular payload does not use all these words in the major frame, or if the payload multiplexes with other payloads, the data rate for that payload would be less than 7,580 words per second. In some cases it is possible to determine the data rate because the bit rate, frame structure and number of MSID's were defined. However, most of the payloads do not have a firm number of MSID's defined as yet.

Operational support time is also not firmly defined. However, estimates on limits can be made which are quite useful. Most missions have the flight time defined, at least to the number of days. In cases where several payloads are on the same flight, the orbit time can be divided in a rational manner depending on payload types. On missions where there are both detachable payloads and nondetachable payloads (e.g., STS-17), six hours of support are estimated for each detachable payload and the remainder assigned to the nondetachable payload.

The values given in Table 2-6 are the maximum possible based on bit rate, word size and overhead. The word rates do not include overhead. One exception is the GOES-D/PAM data which are based on the actual number of data words. This example shows how little of the total PAM capability is

used -- 1.1 Mbyte out of the maximum 83.7 Mbytes, or about 1.3% of the capability. This is the result of the fact that GOES-D has only 13 MSID's. Appropriate data compression will significantly reduce the data volume.

Table 2-6 STS Payload Digital Data

SOURCE	BIT RATE (kbps)	WORD RATE (kwps)	SUPPORT TIME (hr)	DATA VOLUME (Mbyte)
OD DL	128	7.58	7.47*	203.8
DFI	128	15.6	7.47*	419.5
PDI	64	7.58	7.47*	203.8
PAM	32	3.875	6.0*	83.7
GOES-D/PAM-A	32	0.407	6.0**	1.1

* MAXIMUM TIME ON ONE ANALOG TAPE (14 TRACKS AT 28 min/TRACK).

** ESTIMATED FROM OPERATIONAL SUPPORT PLAN FOR ONE FLIGHT.

Data dumps from the STS are system limited to a 1024-kbps rate (Ref. 1). The NASCOM network also limits the bit rate to about 1 Mbps (Ref. 4). This bit rate value is then the maximum that could be expected at HCC.

The 128-kbps operational instrumentation (OI) downlink or operational downlink (OD) is a direct orbital vehicle (OV) to ground data link. This S-band, phase modulated RF link is the real-time OV performance monitor and its intelligence data content is collected from three sources within the OV and combined into a single serial bit stream by time division multiplexing. The three data sources are:

(1) Two voice channels at 32 kbps each

(2) Downlink data

(3) Downlist data.

Data routed to the PCM system from the OI mux/demux are the downlink data and contain sensor information. Data routed to the PCM system from the general-purpose controller (GPC) computer are the downlist data. The combination, downlist and downlink data with a total bandwidth of 128 kbps, is called the real-time telemetry channel. In the PCM system, these three sources are merged (time division multiplexed) and transmitted at a bit rate of 192 kbps (128 kbps + 32 kbps + 32 kbps). The receiving ground station decommutates the composite signal, routes Voice 1 and Voice 2 to their respective destinations, and remerges the data on an "analog" (PCM in BIØ-L coded format) tape in a time-continuous, bit-serial, word-serial stream with both an actual and an average bit rate of 128 kbps.

When the operational downlink is completed through the TDRSS, the downlink is transmitted in the low data rate (LDR) mode in which Voice Channel 2 is omitted and the telemetry channel (downlink, downlist) is operated in the low bit rate (LBR) mode; i.e., 64 kbps.

The 128 kbps/64 kbps telemetry frame format ID word provides the map into the major frame, not only for a particular measurement position (or positions) within the frame but its ID number, sample rate, and coding (i.e., 8-bit word, signed or unsigned, single or multiprecision, multisyllable word, etc.).

Commonality does not exist between formats. With respect to any two formats, individual parameters may:

(1) Not appear in one or both formats

(2) Appear in the same location with the same sample rate

(3) Appear in both formats but vary in one or more of the following:

  (a) Sample rate

  (b) Word slot

  (c) Frame number

  (d) Staleness factor (time delay)*

---

* Shuttle OD does not contain classical first-in/first-out data. Parameters are buffered individually. Buffering for variable periods of time causes the time correlation task to be more difficult, i.e., sequential words of the same MSID are time sequential also. However, they are not necessarily time parallel with other MSID's within that frame.

The major frame, so-called because it is the number of subframes necessary to include at least one sample of every data item specified in the format specification, is defined to be 100 subframes, 0-99, each with its own subframe counter and its own sync character.

In its simplest format, there are no subcoms contained in the OD. The data stream consists only of overhead and operational instrumentation (OI) data. Combinations of general-purpose computer and payload data interleaver (PDI) subcoms "windowed" into the OD will be considered following this simple frame (overhead plus OI only) discussion.*

The basic data monosyllable word is the 8-bit byte. Present hardware frame synchronizer equipment, upon detecting major frame sync, outputs the serial input stream as 16-bit words.** A total of 8000 (if the sync word is output) 16-bit words are output in 1 sec to complete one major frame, followed without interruption by the beginning of the next major frame. These data are sent to magnetic disc where they are packed wordwise in computer-readable format. The resulting magnetic disc file is simply a 1:1 binary image of the "analog" PCM tape. However, the disc image is organized into a frame recoverable format.

Frame analysis begins once the disc is mounted and the computer has access to the frame format ID.† Data reduction of the frame does not encompass the whole frame, however. Only the OI data are reduced for all frames since its format (i.e., MSID, word length, sample rate) is explicitly defined in the frame format ID word. The OI data word can be one of a number of different formats. For example:

---

* OV hardware capabilities limit the number of subcom data sets at any one time to (1) one overhead and OI host set, (2) five GPC subcoms, and (3) four payload (PL) subcoms.

** Sixteen-bit word output every 1/(128 k/16 bit) or 125 μsec.

† The 128-kbps frame format is always considered to be valid. However, the 64-kbps (LDR) OD takes from a few seconds to one minute to complete the changeover from one format to another and therefore inserts a predefined invalid sync character so that no data will be output to disc until frame changeover is accomplished and valid sync characters reinserted into the OD stream. This will cause variable length time gaps from format to format.

(1) Standard 8-bit analog (unipolar and bipolar)

(2) Digital words (8 bit or 16 bit)

(3) Event words.

Other windows (i.e., PDI and GPC) are simply ignored by the OI reduction algorithm in the computer. This is necessary since the frame format word does not necessarily predefine the PDI or GPC formats. These formats are identified by format words located in those windows and must be explicitly searched for. Further complicating the process is the fact that, due to timing complications within the OV, the GPC downlist data may be skewed by one or more words within its window so that the GPC sync word is displaced within the subframe. That this condition may possibly occur negates reduction of downlist data by calculated offset from OD major-minor frame sync.

Several anomalous conditions may occur in the OV data system that can cause invalid or erroneous data to be inserted into the OD data stream. In most cases a flag will be set in the built-in test equipment (BITE) word to indicate this condition. However, the BITE is sent only once every major frame or 1 s/s and this does not provide enough resolution to separate invalid/erroneous data on a less than one major frame basis. The BITE word is located in the overhead section of the major frame and can be detected soon after the start of the frame. Provisions can then be made for disposition of that frame.

Present methods of preparing analog tape for computer reduction involve PCM tape to magnetic disc conversion in image format. A large part (depending on the frame format) of the frame is not used by the computer program to build data base files (i.e., GPC downlist) or, at least, cannot be reduced with other data.

2.3 BEARING/SEAL MATERIAL TEST DATA PROCESSING REQUIREMENTS

Based on a number of MSFC internal working memorandums, initial data reduction requirements for the Bearing/Seal Materials Testing (BSMT) program as a typical support service provided by AH22 were gathered and analyzed.

The BSMT program was conceived to run in three modes: Routine Tests, Performance Tests, and Investigative Tests, with increasing amount and frequency of data reduction activities in the given order. It is anticipated that during initial phases of the program, most of the tests will be conducted in the Investigative Test mode, thus requiring maximum data reduction support.

BSMT is to be conducted on the MSFC facility. Data will be recorded on analog tapes (14 tracks, 54 channels on non-IRIG standard FDM subcarriers) at the test site and transported to Bldg. 4663. Eventually, and cost permitting, real-time support may be provided via optical or coaxial cables between these facilities.

2.3.1 Data Types and Number of Channels

BSMT data consist of time series obtained from the list of transducers in Table 2-7.

2.3.2 Data Reduction Requirements

The signal bandwidth shown in Table 2-7 is based on estimates provided by the MSFC requiring element, which also insisted on a data digitizing sampling rate of at least five times the signal bandwidth.

The type of data reduction includes plotting of selected time slices, determination of RMS and PSD, and presenting all results in "iso-plot" format on hard copies. Data reduction and output requirements are summarized in Table 2-8.

2.3.3 Data Reduction Setup and Playback

Based on AH22 data reduction equipment available during spring-summer 1981, with 28 FDM discriminators of the appropriate subcarrier frequencies, the data reduction setup will be similar to that shown in Fig. 2-1.

Table 2-7 BSMT Transducers

MEASUREMENT NAME AND DESCRIPTION	TRANSDUCER GROUP NUMBER	EXPECTED SIGNAL BANDWIDTHS
TEMP. OUTER RACE BEARING NO. 1, +Z	A-1	0-1 KHz
TEMP. OUTER RACE BEARING NO. 2, +Z	A-2	
TEMP. OUTER RACE BEARING NO. 3, +Z	A-3	
TEMP. OUTER RACE BEARING NO. 4, +Z	A-4	
LOAD AXIAL BOLT NO. 1, 0°	B-1	0-2 KHz
LOAD AXIAL BOLT NO. 2, 120°	B-2	
LOAD AXIAL BOLT NO. 3, 240°	B-3	
SHAFT LOAD RADIAL FY	B-4	
SHAFT LOAD RADIAL FX	B-5	
PR. LOX INLET CAVITY	B-6	
PR. LOX OUTLET CAVITY NO. 1	B-7	
PR. LOX OUTLET CAVITY NO. 2	B-8	
PR. SEAL DRAIN OUTLET LOAD SIDE	B-9	
PR. SEAL DRAIN OUTLET INPUT SIDE	B-10	
SHAFT AXIAL DISPLACEMENT EDGE	C-1	0-5 KHz
SHAFT AXIAL DISPLACEMENT CENTER	C-2	
SHAFT RADIAL DISPLACEMENT LOAD SIDE, -Y	C-3	
SHAFT RADIAL DISPLACEMENT LOAD SIDE, +Z	C-4	
SHAFT RADIAL DISPLACEMENT LOAD SIDE, +Y	C-5	
SHAFT RADIAL DISPLACEMENT LOAD SIDE, -Z	C-6	
SHAFT RADIAL DISPLACEMENT INPUT SIDE, -Y	C-7	
SHAFT RADIAL DISPLACEMENT INPUT SIDE, +Z	C-8	
SHAFT RADIAL DISPLACEMENT INPUT SIDE, +Y	C-9	
SHAFT RADIAL DISPLACEMENT INPUT SIDE, -Z	C-10	
TILT, BEARING NO. 1, SUP. RING, 0°	C-11	
TILT, BEARING NO. 1, SUP. RING, 120°	C-12	
TILT, BEARING NO. 1, SUP. RING, 240°	C-13	
TILT, BEARING NO. 4, OUTER RACE, 0°	C-14	0-5 KHz
TILT, BEARING NO. 4, OUTER RACE, 120°	C-15	
TILT, BEARING NO. 4, OUTER RACE, 240°	C-16	
DISPL. BEARING 2 AND 3, OUTER RING, 0°	C-17	
DISPL. BEARING 2 AND 3, OUTER RING, 90°	C-18	
VIB. HOUSING INPUT SIDE, +Y	C-19	
VIB. HOUSING INPUT SIDE, +Z	C-20	
VIB. TORSIONAL, QUILL SHAFT	C-21	
RPM, QUILL SHAFT	C-22	
TORQUE, QUILL SHAFT	C-23	
VIB. BEARING CARRIER NO. 1, Y	D-1	0-10 KHz
VIB. BEARING CARRIER NO. 1, Z	D-2	
VIB. BEARING CARRIER NO. 2, Y	D-3	
VIB. BEARING CARRIER NO. 2, Z	D-4	
VIB. BEARING CARRIER NO. 3, Y	D-5	
VIB. BEARING CARRIER NO. 3, Z	D-6	
BEARING NO. 4 OUTER RACE RADIAL LOAD, 0°	E-1	0-20 KHz
BEARING NO. 4 OUTER RACE RADIAL LOAD, 120°	E-2	
BEARING NO. 4 OUTER RACE RADIAL LOAD, 240°	E-3	
BALL PASS COUNTER BEARING NO. 1, 0°	E-4	
BALL PASS COUNTER BEARING NO. 1, 90°	E-5	
BALL PASS COUNTER BEARING NO. 2, 0°	E-6	
BALL PASS COUNTER BEARING NO. 2, 90°	E-7	
BALL PASS COUNTER BEARING NO. 3, 0°	E-8	
BALL PASS COUNTER BEARING NO. 3, 90°	E-9	
BALL PASS COUNTER BEARING NO. 4, 0°	E-10	
BALL PASS COUNTER BEARING NO. 4, 90°	E-11	

Table 2-8 BSMT Data Reduction Requirements

TRANSDUCER GROUP	SIGNAL FREQUENCY (kHz)	ON-LINE QUICK-LOOK REQUIREMENTS: RMS CHANNELS	RMS CHANNELS PER ISOPLOT	RMS TIME POINTS	RMS TOTAL TRACES	ROUTINE TESTS: RMS CHANNELS	RMS CHANNELS PER ISOPLOT	RMS TIME POINTS	RMS TOTAL TRACES	PERFORMANCE TESTS: RMS CHANNELS	RMS CHANNELS PER ISOPLOT	RMS TIME POINTS	RMS TOTAL TRACES	PSD CHANNELS	PSD CHANNELS PER ISOPLOT	PSD TIME POINTS	PSD TOTAL TRACES	INVESTIGATION TESTS: TIME ZOOM CHANNELS	TIME ZOOM CHANNELS PER ISOPLOT	TIME ZOOM TIME POINTS	TIME ZOOM TOTAL TRACES	RMS CHANNELS	RMS CHANNELS PER ISOPLOT	RMS TIME POINTS	RMS TOTAL TRACES	PSD CHANNELS	PSD CHANNELS PER ISOPLOT	PSD TIME POINTS	PSD TOTAL TRACES	TIME ZOOM CHANNELS	TIME ZOOM CHANNELS PER ISOPLOT	TIME ZOOM TIME POINTS	TIME ZOOM TOTAL TRACES	PSD SPEED RAMP (UP/DOWN) CHANNELS	PSD SPEED RAMP (UP/DOWN) CHANNELS PER ISOPLOT	PSD SPEED RAMP (UP/DOWN) TOTAL TRACES
A	0-1	4	4	1	4	4	1	4	4	1	4	4	6	24				4	1	4	4	6	24													
B	0-2	10	10	1	10	10	1	10	10	1	10	10	6	60				10	1	10	10	6	60													
C	0-5	10	10	1	10	10	1	10	10	1	10	10	6	60				10	1	10	10	6	60				10	1/1	400							
		8	8	1	8	8	1	8	8	1	8	8	6	48				8	1	8	8	6	48				8	1/1	320							
		5	5	1	5	5	1	5	5	1	5	5	6	30				5	1	5	5	6	30				5	1/1	200							
D	10	6	6	1	6	6	1	6	6	1	6	6	6	36	6	6	36	6	1	6	6	6	36	6	6	36	6	1/1	240							
E	0-20	11	11	1	11	11	1	11	11	1	11	11	6	66	11	6	66	11	1	11	11	6	66	11	6	66	11	1/1	440							
TOTAL PER TEST		54	1	54	54	1	54	54	1	54	54	6	324	17	6	102	54	1	54	54	6	324	17	6	102	40	2	1600								
NUMBER OF PLOTS: MULTI-PARAMETER ISO		7			7			7			42			12			7			42			12			80										
PARAMETER VERSUS TIME		-			-			-			-			2			-			-			2			8										
TIME SLICE		300 sec			300 sec			300 sec			200 msec			200 msec			300 sec			200 msec			200 msec			200 msec										

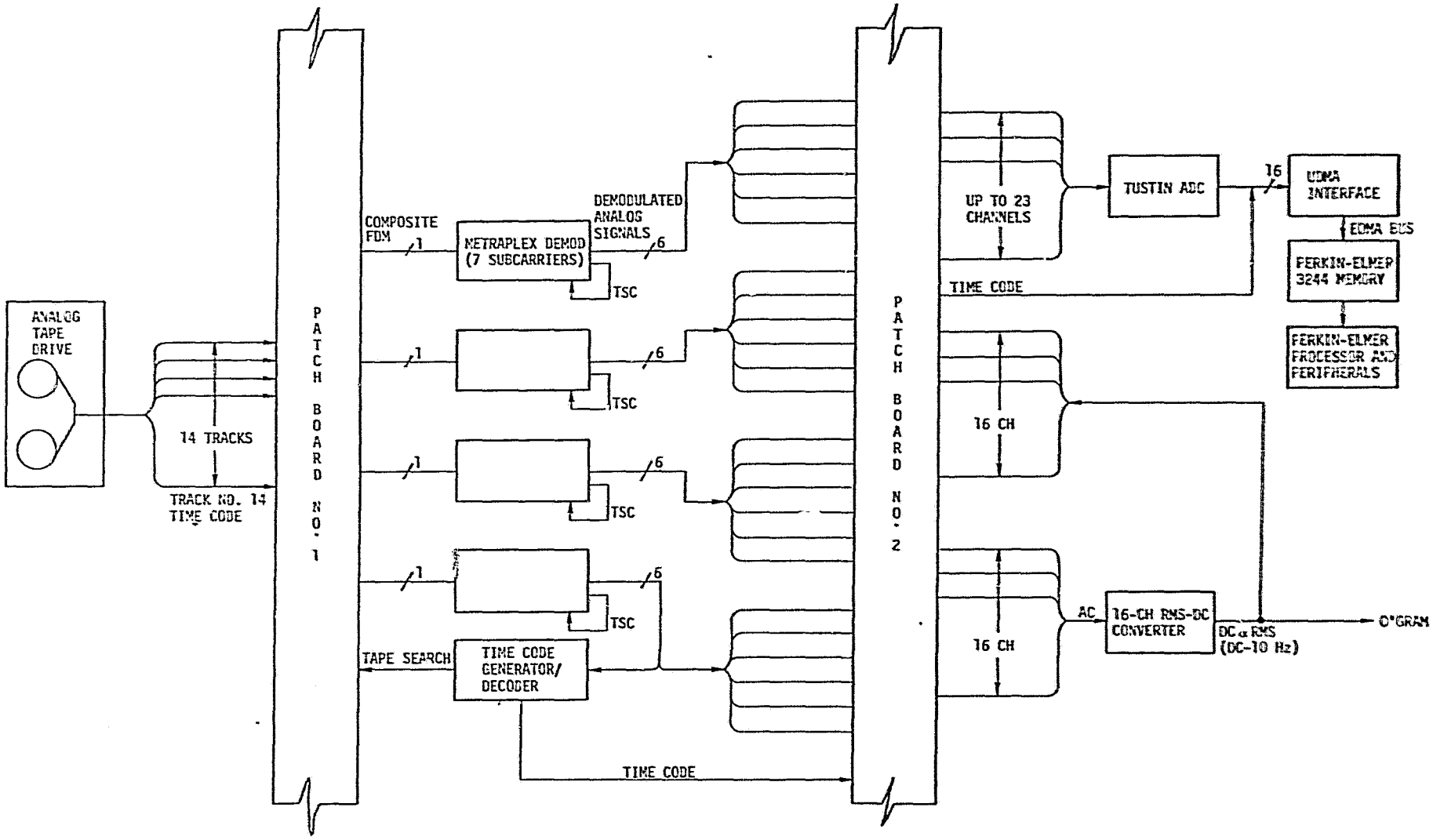

Fig. 2-1 Conceptual Data Reduction Setup for BSMT Based on Hardware Capability During 1981

Because of the high sampling rate requirement and the large number of channels of data involved, four patch configurations and seven passes of analog tape playback will be needed for each test. Recommended signal grouping, sampling rates, data volume, and output plot characteristics are listed in Table 2-9.

Sampling rate and volume requirements are both considered to be on the conservative side. It can be expected that data reduction requirements for the BSMT will be drastically changed shortly after the initial test series. Data compression will take place in the form of revised data reduction requirements as the test program matures.

Table 2-9 BSMT Data Processing Summary

PATCH BOARD NO. 1 CONFIG	DATA CHANNELS DEMODULATED	ANALOG TAPE PASS NUMBER	DATA CHANNELS PROCESSED	SAMPLING RATE EACH CHANNEL (ksamples/sec)	THROUGHPUT (ksps)		DATA VOLUME PER 0.2048-sec BURST (NUMBER OF SAMPLES)		TIME BETWEEN BURSTS (sec)		SAMPLE BLOCK SIZE FOR PSD COMPUTATIONS PER CHANNEL	PSD PLOT RESOLUTION		MAXIMUM FREQUENCY PLOTTED (KHz)
					BY GROUP	TOTAL FOR BURST	PER CHANNEL	TOTAL	PERF. TEST	INVEST. TEST		Hz	MAXIMUM FREQUENCY PLOTTED (%)	
I	L1 TO E11 D1 TO D6	1	E1 TO E4	100	400	400	20,480	81,920	59.8	14.8	5 x 4096	48.83	0.24	20
		2	E4 TO E7	100	400	400	20,480	81,920			5 x 4096	48.83	0.24	
		3	E7 TO E11	100	400	400	20,480	81,920			5 x 4096	48.83	0.24	
		4	D1 TO D6	50	300	450	10,240	92,160			2 x 4096	24.41	0.24	10
			E1,E4,E7(1)	50	150		10,240				2 x 4096	24.41	0.24	
II	C1 TO C14 E1,E4,E7(2) D1,D5,D6(2)	5	C1 TO C14	25	350	500	5,120	102,400			1 x 4096	12.21	0.24	5
			E1,E4,E7(2)	25	75		5,120				1 x 4096	12.21	0.24	
			D1,D5,D6(2)	25	75		5,120				1 x 4096	12.21	0.24	
III	C10 TO C25 E1,E4,E7(2) D1,D5,D6(2)	6	C10 TO C25	25	350	500	5,120	102,400			1 x 4096	12.21	0.24	
			E1,E4,E7(2)	25	75		5,120				1 x 4096	12.21	0.24	
			D1,D5,D6(2)	25	75		5,120				1 x 4096	12.21	0.24	
IV	B1 TO B10 A1 TO A4 E1,E4,E7(3) D1,D5,D6(3) C1,C12,C23(3)	7	B1 TO B10	10	100	230	2,048	47,104			1 x 2048	9.77	0.49	2
			A1 TO A4	10	40		2,048				1 x 2048	9.77	0.49	
			E1,E4,E7(3)	10	30		2,048				1 x 2048	9.77	0.49	
			D1,D5,D6(3)	10	30		2,048				1 x 2048	9.77	0.49	
			C1,C12,C23(3)	10	30		2,048				1 x 2048	9.77	0.49	

NOTES: (1) LPF TO 10 KHz BANDWIDTH FOR REFERENCE.

(2) LPF TO 5 KHz BANDWIDTH FOR REFERENCE.

(3) LPF TO 2 KHz BANDWIDTH FOR REFERENCE.

3.0 CONCEPTUAL DATA REDUCTION SYSTEM DESIGN

3.1 GENERAL DESIGN CONSIDERATIONS

As a data reduction institution, AH22 responds to a center-wide or even NASA-wide clientele, handling large volumes of data of many different types and qualities with varied processing requirements. The most demanding situations often occur when simultaneous support must be provided for more than one major mission over which the Branch has little control of the schedule. The magnitude of the operation which AH22 has direct responsibilities for is illustrated in a limited way by the total number of personnel involved: over 60 Government and contractor employees, and exemplified by the fact that three shift operations were often required following each Shuttle launch. Consequently, standard terms characterizing a data reduction system's reliability, modularity, component interchangeability, flexibility, throughput, maintainability, etc., take on significantly broader and deeper meanings when the application is for the purpose of data reduction in the context defined above. Additionally, the system must also serve as the starting point from which flexible and smooth flowing operating procedures emerge. And finally, for the long term, the hardware, the software, and the procedures must possess the right type of interdependency so that selective upgrading of individual elements, components or subsystems can be accomplished without invoking major rework on other parts of the total system, and without causing disruption of the overall data reduction service.

A number of basic principles are immediately apparent in the development of a design approach for the data reduction system:

- Utilize as much as possible standard processor hardware configurations and operating systems
- Minimize the use of special peripherals, interfaces and device handlers (software drivers)
- Minimize interconnections among hardware subsystems in order to reduce hardware interdependency and procedural complexity

- Pay special attention to the data reduction procedures during system design in order to minimize interdependency of the procedures, especially in the time domain, so that rework does not always have to start from the very beginning.

Ideally, the design of the data reduction system for AH22 would have hardware, software and procedures each divided into many simple stand-alone modules, each with the ability to perform its function with minimum dependency on the others. All modules can be integrated together and the process automated for maximum efficiency during normal operations, but each element would have the flexibility to continue its assigned function when others break down, or when they are used for other purposes.

Turning now to a different aspect of design and looking at the typical function of the data processing system, it will be seen that in preprocessing of "raw" data, most of the operations are simple procedures performed repetitively on large volumes of data. Only simple, logical and/or arithmetical operations are involved on data of limited word sizes. Sorting (PCM decommutating), engineering units conversion and digital filtering are typical examples of preprocessing under this definition.

Since the types of digital preprocessing tend to be limited in the number and remain constant over the long term, they are ideal candidates for hardware implementation. At least two types of hardware preprocessing approaches should be investigated and implemented:

Type 1: Obtain raw data from real-time sources or serial storage (e.g., magnetic tapes), process and (1) put results in temporary storage, or (2) pass results directly to the next processing subsystem (which, for example, may be a general-purpose computer).

Type 2: Obtain and put raw data directly into temporary storage and perform the preprocessing at a later time at maximum speed achievable by the hardware.

A well-conceived, designed and implemented hardware preprocessor complex can be a significant aid to the general-purpose computer by relieving it from those chores where it performs most inefficiently due principally to its von Neumann architecture. Major improvements in system throughput and efficiency can be expected.

3.2 PCM DATA REDUCTION SYSTEM DESIGN CONSIDERATIONS

Based on results presented in Sections 2.1 and 2.2, PCM bit rates range from 60 to 1024 kbps, and are well within standard PCM bit and frame synchronizers available from a number of sources. A four- or six-channel front-end (bit synchronizers and frame synchronizers) will not only provide the capacity to process the maximum number of parallel channels of data in real time for a long time to come, but will also provide the much needed redundancy during periods of nonpeak work load.

A high degree of data compression can be accomplished by commercially available data compressors. One such unit (EMR Model 715) can process up to six data streams, and should be acquired and incorporated into the system.

3.3 FDM DATA REDUCTION SYSTEM DESIGN CONSIDERATIONS

Unlike PCM data, all FDM data are available in parallel, and in analog form. The use of analog multiplexers and a single analog-to-digital converter (ADC) in a data reduction facility (where it will only have to be demultiplexed again) is not justifiable. Furthermore, because of various constraints usually associated with the single ADC approach (e.g., a single sampling rate and a single word size for all data channels), large amounts of redundant digital data will be inadvertently created, only to require data compression and to complicate the overall process.

Two alternative approaches of handling FDM data were considered during the course of this study project:

> Approach 1: Parallel analog discriminators, ADC and sequential storage (one component each for each data channel)
>
> Approach 2: All digital FDM demultiplexing and demodulation.

Approach 1 is definitely feasible with currently available hardware. Very high data conversion throughput is achievable. Channel redundancy is, of course, automatically achieved since it is highly unlikely that all channels would fail at the same time. But Approach 1 will require significant initial cost and lead to a system with a large amount of analog components and cabling.

The feasibility of an all-digital FDM discrimination method was investigated during this study project. An approach has been proven feasible, but real-time throughput is not achievable with currently available hardware technology. Implementation with currently available hardware will result in a nonreal-time FDM system but it is still considered to be a better selection than either the current situation or Approach 1 because it provides a straightforward path to future transition to a real-time system. In any case, even in the nonreal-time form, the all-digital FDM approach offers significant improvement over the current method -- in terms of hardware and procedural simplicity as well as throughput. Results of the feasibility study are described in Section 4.0.

3.4 CONCEPTUAL DESIGN

The design concept for a data reduction system incorporating the above outlined considerations is shown in Fig. 3-1. The most prominent and important element of the design is the large-capacity intermediate storage for partially processed data. Descriptions on it and other major components, functions and operational features are provided in this section. Two alternative design approaches are discussed in Section 3.5. A method to implement the design by adapting existing and currently available Perkin-Elmer computers is also outlined in Section 3.6. Details of selected subsystems or algorithms will follow in Sections 4.0 through 6.0.

3.4.1 Intermediate Data Storage

The requirement for a temporary storage for preprocessed data products was briefly discussed in Section 3.1. Once the concept of an intermediate data store (IDS) germinates, however, other applications rapidly emerge. Indeed, Fig. 3-1 has been deliberately composed in a manner to convey the idea that the IDS is the central element of the conceptual data processing complex, being used also as scratch pad, buffer, and "mail boxes" for communications among all general and/or special-purpose processors interfaced to it.

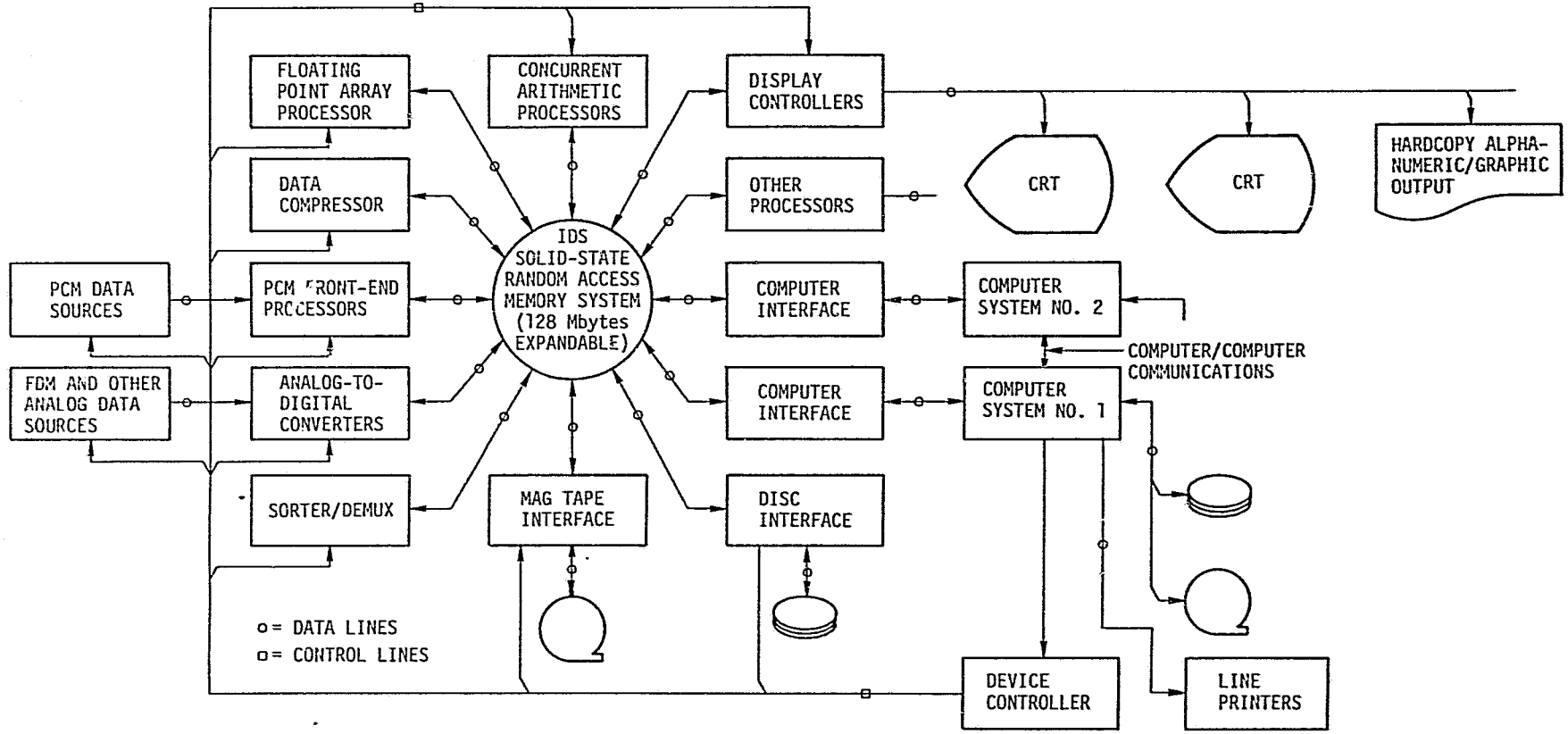

Fig. 3-1 Conceptual Data Processing System Design

3.4.1.1 Requirements

3.4.1.1.1 Speed

The speed requirement of the IDS must meet or exceed the maximum real-time data rate from the PCM preprocessors and/or the FDM ADC outputs. Based on discussions in Section 2.2, the maximum expected PCM data rate per channel is 1 Mbits per second. Even with six channels of preprocessors, each operating at this maximum speed and without real-time data compression, the maximum expected PCM data input rate is

$$\frac{6 \text{ (channels)} \times 1 \text{ M (bits/sec)}}{8 \text{ (bits/byte)}} = 768 \text{ kbytes/sec}$$

In Section 4.0, an all-digital FDM discrimination method will be described. In one version of that method, it will require 12-bit analog-to-digital conversions of the FDM composite signal, and store the samples for subsequent digital discrimination. The maximum rate could be as high as 5.6 Mwords per second per FDM composite. In the unlikely event that 14 potential analog tape tracks of FDM data require simultaneous analog-to-digital conversion at this maximum rate, the resulting total input bandwidth requirement for the IDS is

$$14 \text{ (tracks)} \times 5.6\text{M (words/sec)} \times 2 \text{ (bytes/word)} = 156.8 \text{ Mbytes/sec}$$

3.4.1.1.2 Volume

As indicated in Fig. 3-1, the IDS volume should be adaptable for future expansion. In order to develop an order-of-magnitude estimate on the initial IDS size, PCM data processing requirements outlined in Section 2.0 are used below.

For STS data reduction, Table 2-1 indicates a total volume requirement of 77 Mbytes. For Payload support, Table 2-6 indicates that upwards of 419.5 Mbytes will be required. Obviously, digital FDM discrimination exerts maximum requirement on the IDS volume as well as speed.

Based on the above requirements, it is clear that off-loading from the IDS is required for real-time data acquisition. Rigid numerical specifications on its speed and volume cannot be derived without consideration of both the overall configuration and operational schemes.

Stated in very general terms, one may conclude that the IDS should have a data transfer rate of above 10 Mbytes/sec and a volume in excess of 100 Mbytes.

3.4.1.1.3 Other Requirements

The primary use of the IDS is for temporary storage of data, not as an expansion of computer memory. True random addressing to the word level is not necessary. Rather, random access to the starting and stopping addresses of blocks of memory will be adequate. Sequential access of data words can then follow. Addressing of the IDS is, therefore, much like that used for discs, i.e., random entry via a directory to a block level, followed by data transfer in a sequential mode.

As a buffer-scratch pad, multiport access is definitely required for the IDS.

The overall system design concept is to allow additions of both data input ports and preprocessors as the requirements and the utilization grows. The IDS interface must, therefore, have provisions for expansion. Due to the heavy traffic through the IDS, error detection and correction will be required.

3.4.1.2 Selection of Technology

Competing technologies for the IDS are:

- Magnetic tape
- Magnetic disc
- Change coupled device (CCD)
- Magnetic bubble (MB)
- Solid-state random access memory (RAM).

The requirement of random block access rules out the magnetic tape as a candidate, except for the purpose of providing mass storage and off-loading of the IDS.

Both the CCD and the MB are available in major-minor loop configurations so that they do satisfy the requirement of random block addressing. Magnetic bubbles, however, are relatively slow devices. Complicated interleaving scheme will be required to achieve the desired transfer rate for application as the IDS. Neither the CCD nor the MB can be considered "main stream" technology and, as a result, they do not benefit from the type of intense development competition experienced by the RAM or the disc system. As a matter of fact, three major manufacturers have dropped out of the magnetic bubble field during 1981 alone. From both cost and future expansion and maintenance considerations, CCD and MB are not good choices for the IDS.

Disc storage appears to be an attractive approach because of low cost and random access capability. Disc operations, however, are intricately related to a computer and, in particular, to its operating system software. When one of these elements breaks down, operations of all are halted. Being an electromechanical device, and operating near the limits of the capabilities of most of its components, disc drives are not as reliable as totally solid-state devices. Discs also have a speed disadvantage stemming primarily from the latency associated with track seek time and waiting for the rotation of the disc to bring the data to the write/read head(s). Although the track seek time can be eliminated by using head-per-track drives, it cannot eliminate the rotational latency problem. A head-per-track drive would also bring a new disc design into AH22's facility which is dominated by a single model of moving-head disc systems. Interchangeability and maintenance questions also arise. Furthermore, the net data transfer rate for the disc is limited by the rotational speed and the quality of the disc surface, dimensions of read/write heads, and the distance between the head and the rotating surface. For the flying-head used in all hard disc systems, these parameters are interrelated and subject to design tradeoffs. At present, the burst data transfer rate after the head has reached the designated location is between 0.5 to 2 Mbytes per second, which could easily become a constraint when used in the IDS application.

If accessing data on disc is to be considered a step in the data reduction procedure, then, for the above reasons, it is too slow, too complicated and too dependent on other elements of the hardware, software and procedures. It will not be wise to design the data reduction system using the magnetic disc technology for the IDS. (This, however, by no means minimizes the importance of the disc in a general-purpose computer system where it will continue to be the center of activities of sophisticated system operations.)

Semiconductor random access memory possesses all desirable characteristics for the IDS design except cost. Due to extremely intense competitions, RAM technology is bound to show continued new development and refinement. Its cost (on a per bit basis) will continue to drop. For these reasons, and because it provides reserve performance capability, RAM should, and can be, depended on in the IDS design. A number of semiconductor manufacturers are currently (1983) offering large-scale memory subsystems for various requirements. See Table 3-1 for a list of available assembled systems using 64K RAM's and including PC boards, chassis, timing, refresh, addressing, error checking and correction, and power supplies. The list is certainly going to grow. The IDS design should be based on those memory system designs which have built-in capability to accommodate the upcoming 256K RAM chips.

Table 3-1 Dynamic RAM Mass Memory Products, 1983
(Made of 64K RAM Chips)

MANUFACTURER	MODEL	MEMORY SIZE	RANDOM ACCESS (nsec)	CYCLE TIME (nsec)
MOTOROLA	SYSTEM 3000 MAXI	32 MB	350/450	400/500
	SYSTEM 3000 MINI (3Q81)	4 MB	350/450	400/500
INTEL	SERIES 90 VMS	16 MB	275/400	350/400
	SERIES 90 IMS	4 MB	275/400	350/400
MOSTEK	MK8600	6 MB	250	450
NATIONAL	NURAM	8 MB	-	-
MONOLYTHIC SYSTEMS	MSC3602	2 MB	500	690
DATARAM	BULK SEMI	8 MB	-	-
PLESSEY	MEGABYTER	1 MB	-	-
INTERSIL	IMM5	4 MB	300	500
CDC	94554	8 MB	300	400

Among the mass semiconductor memory products listed, the Motorola System 3000 provides the highest potential storage capacity (32 Mbytes, expandable to 128 Mbytes with the 256K RAM), throughput (64×10^6 bytes/sec), straightforward architecture, built-in error detection and correction, self-diagnostics, and good maintainability. This memory is selected for the IDS design.

3.4.1.3 Configuration

Figure 3-2 is a block diagram of the System 3000 memory based on vendor-provided information. Dual port capability will be achievable via the two user I/O cards. Both user buses can be used for block data transfer in the DMA mode.

3.4.2 PCM Front End

The front end of the PCM system shall consist of bit and frame synchronizers, expandable to six parallel channels. An existing PCM system which includes a programmable data compressor can be used. Provisions shall be made, and additional interfaces shall be developed, so that the compressor may be used either in-line or as a separate preprocessor using the IDS.

The source of the PCM data may be either an analog tape drive, or a real-time telemetry receiver/PSK demodulator.

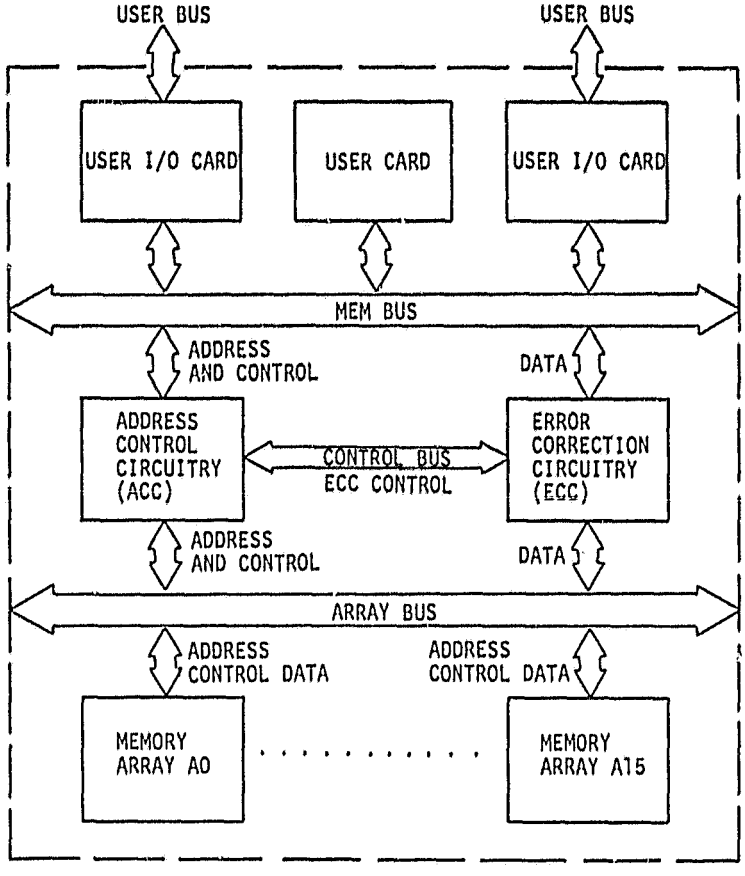

Fig. 3-2 System 3000 Block Diagram

3.4.3 FDM Front End

It is one of the principal conclusions reached early in this study that the FDM front-end data reduction system is one of the two prime contributors to the majority of the analog equipment. (The other is the oscillographic station.) In addition to requiring a significant amount of maintenance, calibration and repair, they are also responsible for the complex cabling networks, switching, patching, and complex control functions.

An all-digital FDM discrimination scheme will eliminate more than half of these analog circuitries along with their intrinsic hardware, operational and maintenance problems. A detailed feasibility study (Section 4.0) indicated that such an approach is available and can be implemented (but not for real-time throughput in the near future). On account of the tremendous potential simplification of the entire data processing system, a development effort in that direction should be undertaken. The resulting FDM front end will then consist only of the data source (analog playback tape recorders and/or real-time receivers) and, at most, 14 channels of high-speed (up to 10 MHz) analog-to-digital converters.

3.4.4 Graphic Display Controller

The primary function of the graphic display controller (GDC) is to generate hardcopy plots on plain paper of raw and/or reduced data, acquired through the PCM and FDM data channels, using high-speed line printers as the basic output devices. This will eliminate the use of oscillographs and accomplish the objective of achieving independence from analog data processing hardware and procedures. Considerable operating cost savings will also be achieved.

CRT displays may also interface to the GDC for monitoring data reduction processes and examining data stored in the IDS.

Based on preliminary product information (Ref. 18), 8000-line-per-minute printers with graphics capability of 240 dots/inch will become available in the 1984 time frame. The printer utilizes the magnetographic approach and appears to be modestly priced, and is ideally suited for this purpose.

3.4.5 Sorter/Decommutator/Compressor

With currently available monolithic digital correlators capable of parallel correlation rates up to 20 MHz (TRW Model TDC1023J), much of the PCM decommutation can be accomplished after the raw data are stored in the IDS. Sorting, decommutating or compression can then be accomplished by bringing the data out of the IDS, compare and correlate with prescribed patterns, and returned to predesignated memory locations in the IDS.

3.4.6 Floating Point Array Processors

The majority of currently available floating point array processors (AP's) can perform many types of signal analysis chores at very high speeds, (e.g., 7.5 ms for a 1024-point complex FFT in 38-bit precision using the Floating Point System Model 120B which employs early 1970 technology). The major slowdowns encountered when AP's of older designs are used in data reduction applications stem from two design shortcomings:

- Lack of direct input/output capability to communicate with external devices
- All data must be transferred to and from the AP from the host computer via I/O transfer, where the bottleneck develops.

Recent development trends in AP have been toward eliminating these architectural problems by providing direct I/O capabilities and by employing shared-memory with the host processor.

3.4.7 Special-Purpose Arithmetic Processors

Through very large-scale integration (VLSI) of semiconductor devices, it will soon be possible to create networks of processing elements which perform signal analysis tasks in real time. Systolic array processing (Refs. 19 and 20) is the name for highly parallel and pipelined architecture and is drawing significant attention in the design of high-performance signal analysis systems. In Section 4.0, the requirement of this future processing approach for FDM discrimination is suggested.

A more routine example of a special-purpose processor which can, by interfacing with the IDS, provide high-throughput preprocessing of sampled FDM samples is also outlined in Section 4.0.

3.4.8 Mass Storage

In order to offload volume demands on the IDS, magnetic tapes and discs will be used. It should be noted that perpendicular magnetic recording technology (Ref. 21) is currently on the verge of becoming available. With the tremendous market potential, such very high density recording methods for mass data will almost certainly mature within the next five years. Interfacing the IDS to such new devices developed for general-purpose computers should not present major difficulties, and design tasks can be reserved until the devices become available.

3.4.9 Control

Most of the control functions of the IDS, and the processors and input devices can be accomplished with a single general-purpose controller (GPC) which was conceived and developed during this study. The GPC is described in detail in Section 6.0.

3.4.10 Control Software

One of the major advantages of the GPC is that it is based on standard asynchronous communication interface technology between the computer and a CRT terminal. Control software can be easily developed in any high-level language so that true hardware and operating software independence is accomplished.

3.5 DESIGN APPROACHES

Two different approaches are available to implement the conceptual design outlined in Section 3.4.

3.5.1 VERSAbus* Based Approach

In Approach 1, the design centers on the IDS using Motorola System 3000 memory. The most logical method to interface the peripheral processors indicated in Fig. 3-1 and described in Section 3.4 to the System 3000 is to adopt VERSAbus specifications for each of the two external interfacing buses

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* VERSAbus is a trademark of Motorola, Inc.

of the System 3000 (identified as USER BUSES on the top of Fig. 3-2). Figure 3-3 defines the standard bus configuration. For complete specifications of VERSAbus, see Ref. 22.

The VERSAbus is a system-level bus which supports the 16/32-bit M68000* microprocessor family, but has significant expansion capabilities. The following are some of the more pertinent VERSAbus specifications:

- Data transfer bus width: 32 bits
- Addressing range: 2^{32} (=4,295 M) bytes
- Asynchronous data transfer
- Bus arbitration for multiprocessors to access global resources
- Priority interrupt: Multilevel interrupt, prioritized with masking capability
- Maximum width: in the fully expanded version, the VERSAbus is 150 lines wide
- System clock: 16 MHz.

Based on previous microprocessor development trends, once standards for a bus have been established, standard interfacing components and subsystems will indeed become commonly available, which in turn stipulates wider usage of the bus, and a snowballing effect develops. The life cycle of the bus is expected to exceed 10 years. The number of products with VERSAbus interfaces is at the initial portion of a rapidly rising curve at the present time. Its adaptation will provide the assurance that the data processing system will not become obsolete for at least 10 years.

All control functions of the IDS peripheral processors can be basically implemented with the M68000 microprocessor.

3.5.2 Perkin-Elmer 3200 MPS Approach

An entirely different approach is implemented to the total system with the so-called tightly coupled multiprocessor system of Perkin-Elmer, the Model 3200 MPS. Figure 3-4 is a top-level block diagram illustrating the concept. It features a 32-bit CPU and up to nine auxiliary processing

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* M68000 is a trademark of Motorola, Inc.

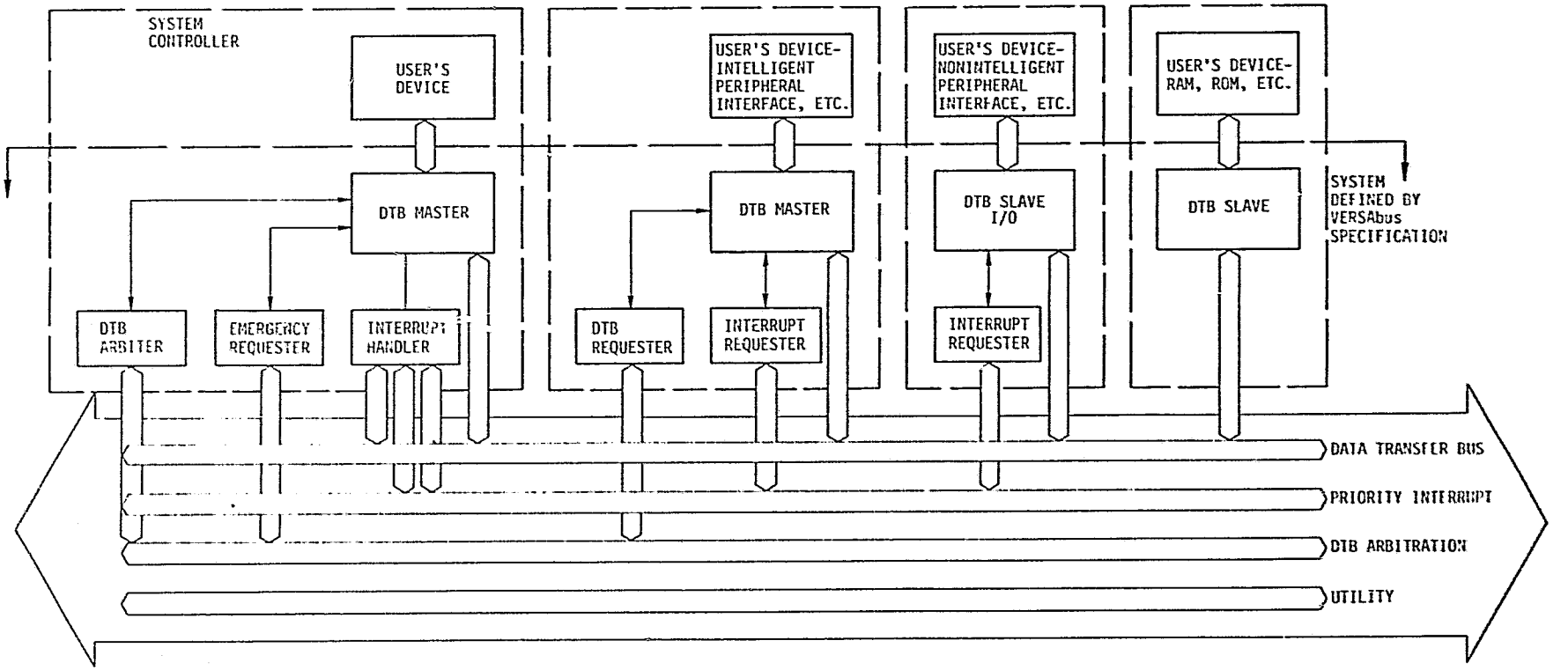

Fig. 3-3 Functional Modules and Buses Contained within the VERSAbus Definition

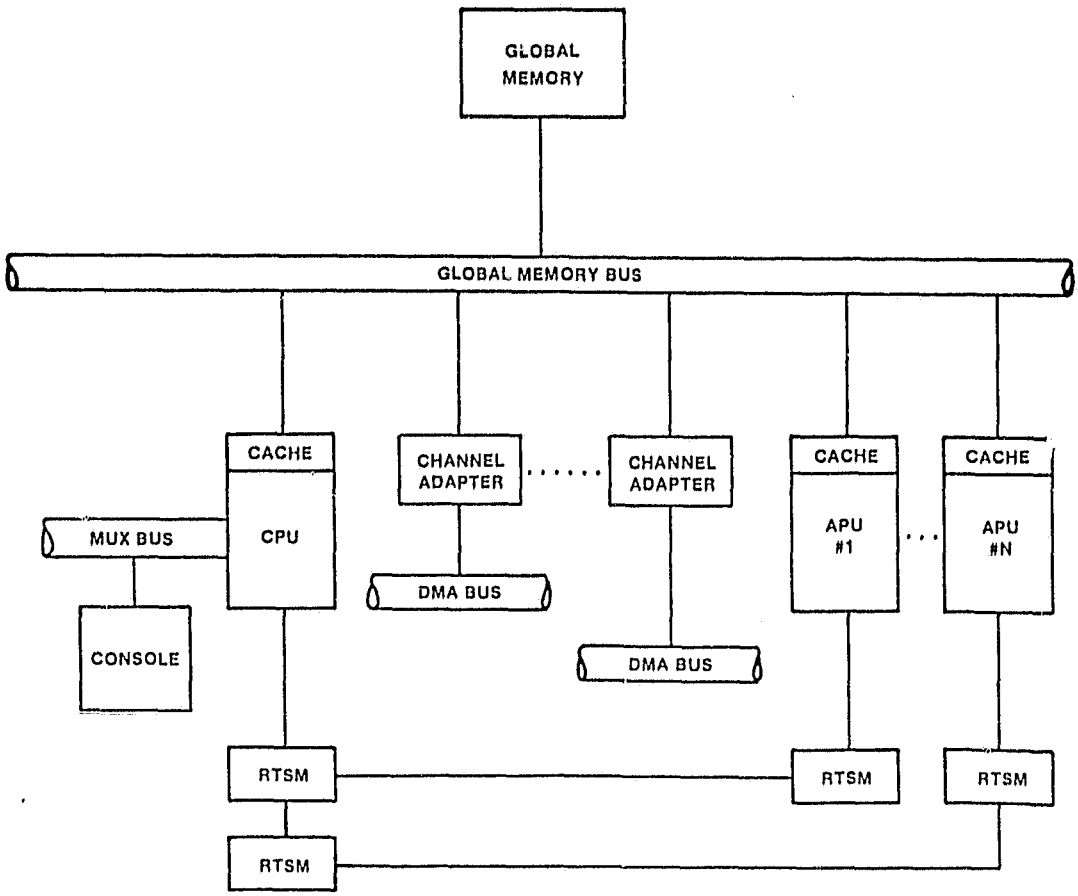

Fig. 3-4 Block Diagram of Perkin-Elmer Model 3200MPS System

units (APU's), all of which share a global memory of up to 16 Mbytes. In addition, a common shared memory subsystem can be interfaced to 14 processors of the Series 3200 family (directly to Models 3210, 3230 and 3250, but with special provisions to Model 3240).

The MPS approach capitalizes on the 64 Mbyte/sec data rate on the global memory bus and uses high-speed cache memory to increase the computational capability. Each APU of the 3200 MSP can have its own special-purpose microcode in its Writable Control Store, so that it can perform unique processing algorithms efficiently. Task scheduling is accomplished via a special multiplexer bus with the shared memory (Fig. 3-5) and a shared memory RAM bus. The basic architecture of Fig. 3-1 is accomplished.

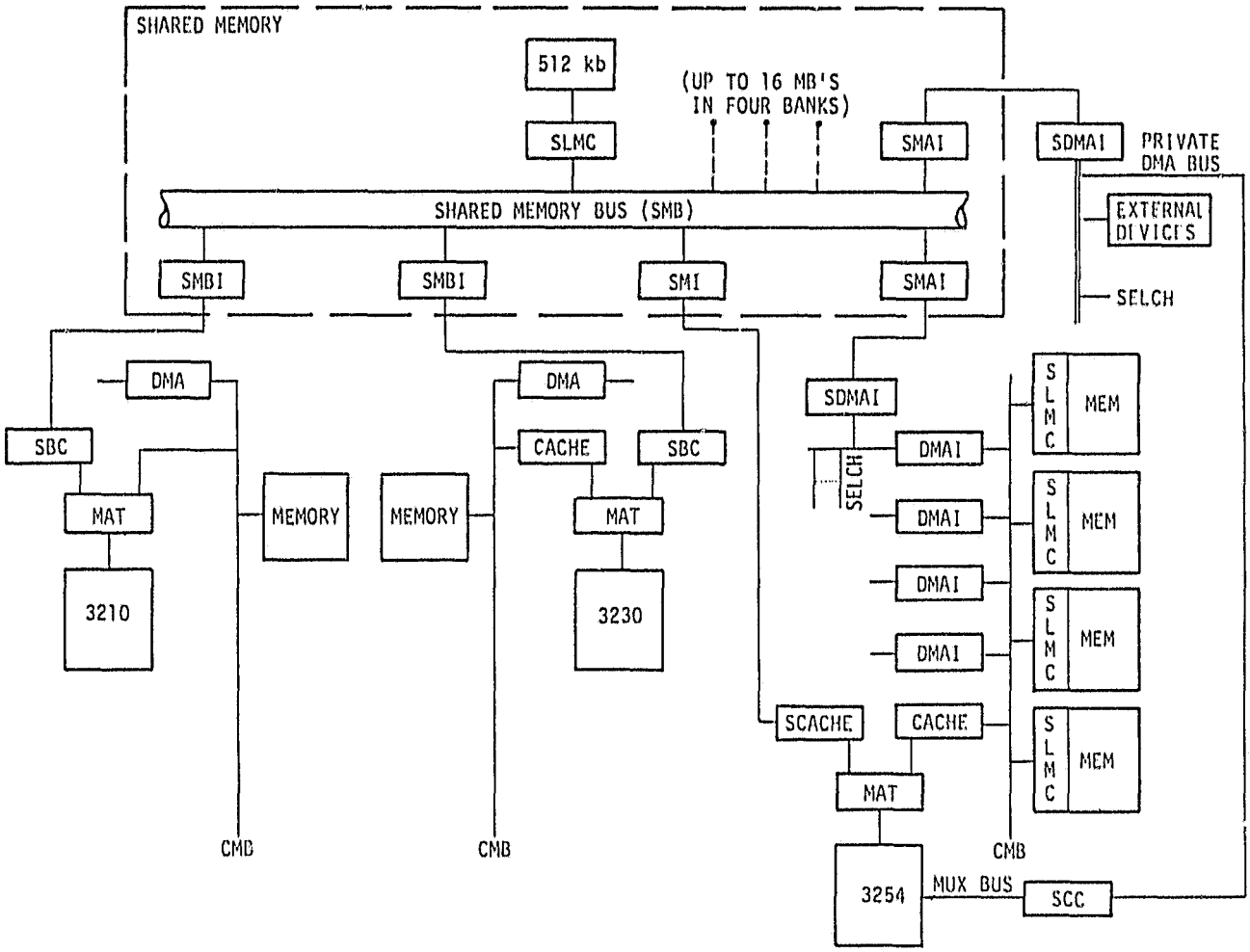

Fig. 3-5 Shared Memory with Perkin-Elmer Models 3210, 3230 and 3254

3.5.3 Comparison of Approaches

Relative advantages and disadvantages of the two approaches are discussed below.

3.5.3.1 VERSAbus Based Approach

- Advantages
  - IDS memory expandable to 128 Mbytes (projected)
  - Based on products of IC manufacturers, the resulting system will not quickly become obsolete
  - Can be expanded as requirements develop so that up-to-date hardware and design concept can be implemented
  - Configuration can be tailored to fit the requirements
- Disadvantages
  - All subsystems have to be developed, which require time
  - High development cost.

3.5.3.2 3200 MPS/Shared Memory Approach

- Advantages
  - Accomplished via adaptation to available system concept, hardware, software and operating systems
  - High commonality with existing systems in AH22 facility
- Disadvantages
  - Limited memory size for IDS (up to 16 Mbytes maximum)
  - High acquisition cost
  - Schedule of obsolescence based on business climate of the computer manufacturer and its product development strategy which is totally unrelated to this specific application.

The VERSAbus approach is recommended on the basis of its long-term potentials.

4.0 FEASIBILITY STUDY OF ALL DIGITAL FDM DISCRIMINATION

The basic motivation for achieving an all digital FDM technology is to be able to eliminate all at once (1) a large number of complex (and hence difficult to maintain) analog subcarrier discriminators, and (2) the need to digitize each of the many channels of demodulated data. Two different approaches to achieve this goal were investigated. In both cases, the composite signal is first to be digitized with a high-speed ADC (up to 5.6 x 10^6 samples per second). In the first method, digital filters are to be used to separate the subcarriers and then the frequencies are individually detected to obtain the required data. In the second method, computations are to be performed on the digital samples representing the total composite signal to identify the frequencies of the subcarriers mathematically.

Both methods proved to be feasible in principle, but since the second method offers significant potential advantages over the first, only its investigation is described in detail in this report. Information developed during the study on the first method may be found in an NTI technical memorandum (Ref. 23).

4.1 REQUIREMENTS ANALYSIS

4.1.1 Commercial Analog Discriminator Performance Characteristics

Performance characteristics for three different commercial FDM discriminators are listed in Table 4-1 to provide a basis from which performance requirements of the digital FDM discrimination approach may be established.

4.1.1.1 Composite Signal Sampling Rate

In order to cover all subcarrier frequencies offered by the commercial analog discriminators, a maximum ADC sampling rate of 5.6 x 10^6 samples per second is required (for the case of a 2 x 10^6 Hz subcarrier center frequency and a maximum deviation of +40%).

Table 4-1 Currently Used Analog FDM Discriminator Characteristics

CHARACTERISTICS	METRAPLEX CORP. FM DEMODULATOR MODEL 120	EMR TELEMETRY UNIVERSAL TUNABLE DISCRIMINATOR MODEL 410	DATA CONTROL SYSTEMS UNIVERSAL DEMODULATOR MODEL 3110/3111
SUBCARRIER FREQUENCY	300 Hz TO 2 MHz	200 Hz TO 1.999 MHz	400 Hz TO 1.5 MHz
FULL-SCALE DEVIATION	±1% TO ±40%	±1% TO ±40%	±1% TO ±25%
INPUT SIGNAL LEVEL	2 mV TO 2 V RMS	10 mV TO 3 V RMS	10 mV TO 6 V RMS
OUTPUT NOISE	<10 mV RMS FOR M≥2*	<20 mV RMS FOR M≥2	≤10 mV RMS FOR M=5
ADJACENT CHANNEL ATTENUATION	>24 dB FOR 3X DEVIATION	>60 dB FOR 3X DEVIATION AT OUTPUT	>34 dB FOR 3X DEVIATION
OUTPUT FILTER TYPE	4 OR 5 POLE CA OR LP**	5 POLE CA OR LP	4 POLE CA OR LP
BANDWIDTH	2 Hz TO 400 kHz	1 Hz TO 400 kHz (TO 3 DIGITS)	1 Hz TO 32 kHz (±1 Hz + 7%)

* M = MODULATION INDEX.

** CA = CONSTANT AMPLITUDE; LP = LINEAR PHASE. NOTE: FREQUENCIES AND BANDPASS ARE NOT ADJUSTABLE, BUT SET AT THE FACTORY.

4.1.1.2 Frequency Detection Accuracy

In order to achieve a given percent data accuracy, the frequency of subcarriers must be determined to an accuracy of that percent of the full-scale deviation (not the subcarrier). Therefore, if a ±1% data accuracy is needed, the requirement on subcarrier frequency detection would range from ±0.02% to ±0.8% for full-scale deviations of ±1% to ±40%, respectively.

4.1.1.3 Data Frequency Response

The overall data frequency response requirement directly governs the amount of time available for the proposed digital subcarrier frequency detection (if real-time throughput is the objective) and is, consequently, a very important parameter which must be established for evaluation of feasibility. Unfortunately, this characteristic is not easily deducible from specifications published by the manufacturers of the three commerical analog discriminators listed in Table 4-1. The reason for the omission is due to the fact that the overall time constant of such analog devices is directly related to the time constants of the subcarrier selecting bandpass filter and to that of the output low-pass filter and, hence, vary from subcarrier to subcarrier and from application to application, even for a single device.

4.1.2 IRIG Standards

An alternate approach is to establish an indication of the desired parameter values from IRIG standards (Ref. 24). Table 4-2 summarizes the three critical parameters needed for establishing feasibility for the all-digital approach using a mixture of IRIG standards and commercial analog product specifications.

It should be pointed out that due to intrinsic limitations of the FDM process, tradeoffs such as data accuracy for data bandwidth are usually necessary anyway. Thus, the desired parameter values in Table 4-2 should not be construed as simultaneous requirements. Rather, they represent absolute limits which can only be taken individually, and are subject to considerable tradeoffs, especially when the total number of subcarriers within a composite is also taken into account.

Table 4-2 Critical Parameter Values for Digital FDM Discrimination

CRITICAL PARAMETERS	DESIRED PARAMETER VALUES	UNITS	JUSTIFICATION					
			GOVERNING PARAMETER	PARAMETER VALUES				
				IRIG	METRAPLEX 120	EMR 410	DCS 3110/3111	UNITS
ADC SAMPLING RATE	5.6×10^6 (MAXIMUM)	SAMPLES/ sec	MAXIMUM SUBCARRIER FREQUENCY	CHANNEL LL 0.560×10^6 +30%	2.0×10^6 +40%	1.999×10^6 +40%	1.5×10^6 +25%	Hz
SUBCARRIER FREQUENCY DETECTION ACCURACY	±0.02% TO ±0.80%	--	DEVIATION BANDWIDTH	±7.5% TO ±30%	±1.0% TO ±40%	±1.0% TO ±40%	±1.0% TO ±25%	--
SUBCARRIER FREQUENCY DETECTION TIME CONSTANT	10×10^{-6}	sec	NOMINAL RISE TIME	CHANNEL LL 10×10^{-6}	--	--	--	sec

4.2 ANALYSIS

The FDM composite signal has the form

$$F(t) = \sum_{m=1}^{M} a_m \sin(\omega_m t + \phi_m) \quad , \quad \text{for} \quad t \geq -T_o/2 \tag{4-1}$$

where T_o is the length of analysis time slice, a_m and ϕ_m are constants, but where ω_m are "slowly varying" functions of t, and where the number of subcarriers, M, may be as many as 16. The objective is to find all frequencies ω_m by measuring F(t) without a-priori knowledge of the values of a_m and ϕ_m.

Over a "short" duration of t (e.g., over $2T_o$), assume that each ω_m does not change significantly so that the average values of ω_m during that time slice may be used to accurately represent the actual subcarrier frequencies. Take M samples of F(t) as follows:

$$F'_m(t) = F[t + (m-1)\Delta] \quad , \quad -T_o/2 \leq t \leq T_o/2 \quad , \quad m = 1,2,3,\ldots,M \tag{4-2}$$

where Δ is time delay selected to assure linear independency of the ensembles.

Define $F_m(t)$ as the antisymmetric component of $F'_m(t)$ about t=0, i.e.,

$$F_m(t) = \frac{1}{2}\left[F'_m(t) - F'_m(-t)\right] \quad , \quad -T_o/2 \leq t \leq T_o/2 \tag{4-3}$$

then $F_m(t)$ must be of the following form:

$$F_m(t) = \sum_{n=1}^{M} c_{mn} \sin(\omega_n t) \quad , \quad -T_o/2 \leq t \leq T_o/2 \tag{4-4}$$

Expressions for coefficients c_{mn} can be derived from Eqs. (4-1), (4-2) and (4-3) but are of no interest to this analysis. It is important to note, however, that the set of functions $F_m(t)$, m=1,2,...,M are, in general, linearly independent of one another, i.e., none of the functions can be written as a

linear combination of two or more of the others. Under this condition, the last set of equations can be formally solved:

$$d_o \sin \omega_n t = -\sum_{m=1}^{M} d_{mn} F_m(t) \tag{4-5}$$

Equation (4-5) does not actually provide solutions for the subcarrier frequencies because the d_{mn}'s are functions of the a_m's which are not known. What Eq. (4-5) does indicate, however, is that there exists a set of constant coefficients which, when used to linearly combine the functions $F_m(t)$, will produce a result which is a pure sine function over the time slice $[-T_o/2, T_o/2]$. In other words, Eq. (5) may be written as

$$-\sum_{m=1}^{M} d_m F_m(t) = d_o \sin \omega t \quad , \quad -T_o/2 \leq t \leq T_o/2 \tag{4-6}$$

where d_m and ω can be determined by the following approach.

Let F_{mk}, $-K \leq k \leq K$, be a sampled set of values of $F_m(t)$, i.e.,

$$F_{mk} = F_m(k\, t_o) \quad , \quad m = 1,2,\ldots,M \tag{4-7}$$

and let

$$F_{0k} = \sin \omega\, k\, t_o \tag{4-8}$$

where t_o is the sampling period.

It is hypothesized that the squared-error function

$$E = \sum_{k=-K}^{K} \sum_{m=0}^{M} (d_m F_{mk})^2 \tag{4-9}$$

is a minimum if the "mixing" coefficients d_m satisfy the normal equations of the least-squares criteria and when ω is one of the subcarriers ω_m

$$\sum_{m=0}^{M} d_m \sum_{k=-K}^{K} F_{mk} F_{nk} = 0 \quad , \quad n=0,1,2,\ldots,M \tag{4-10}$$

which are obtained by setting

$$\frac{\partial E}{\partial d_n} = 0 \quad \text{for each } n \tag{4-11}$$

Equation (4-12) shows details of Eq. (4-10) when the terms are written out explicitly

$$\begin{aligned}
&(\Sigma \sin^2 \omega k t_o)\ d_o + (\Sigma F_{1k} \sin\omega k t_o) d_1 + (\Sigma F_{2k} \sin\omega k t_o) d_2 + \ldots + (\Sigma F_{mk} \sin\omega k t_o) d_M = 0 \\
&(\Sigma F_{1k} \sin\omega k t_o) d_o + (\Sigma F_{1k}^2) d_1 + (\Sigma F_{1k} F_{2k}) d_2 + \ldots + (\Sigma F_{1k} F_{Mk}) d_M = 0 \\
&(\Sigma F_{2k} \sin\omega k t_o) d_o + \ldots \\
&\vdots \\
&(\Sigma F_{Mk} \sin\omega k t_o) d_o + \ldots \qquad \ldots + (\Sigma F_{Mk}^2) d_M = 0
\end{aligned} \tag{4-12}$$

with all summations performed from -K to K. Let

$$\sum_{k=-K}^{K} F_{mk} F_{nk} = A_{mn} \quad , \quad \begin{matrix} m=0,1,2,\ldots,M \\ n=0,1,2,\ldots,M \end{matrix} \tag{4-13}$$

Then Eqs. (4-10) or (4-12) may be written in matrix notation as

$$[A] \times [D] = [0] \tag{4-14}$$

where

[A] = a symmetric square matrix of dimension (M+1) x (M+1) whose elements are A_{mn}

[D] = the solution vector with elements d_n

[0] = the null vector with all zero elements.

Since Eq. (4-14) is homogeneous, a nontrivial solution [D] exists only if the determinant of the coefficient matrix [A] vanishes, i.e., when

$$|A_{mn}| = 0 \tag{4-15}$$

The unknown in Eq. (4-15) is ω, which is contained in the elements of the first row and first column of [A], in the form

$$A_{om} = A_{mo} = \sum_{k=-K}^{K} F_{mk} \sin\omega k t_o \tag{4-16}$$

If the hypothesis put forth in the paragraph following Eq. (4-8) is correct, then M solutions of Eq. (4-15) for ω are the subcarrier frequencies. An attempt to prove this argument theoretically has so far been unsuccessful. A large number of successful numerical experiments conducted on a computer, however, has firmly demonstrated its validity.

The procedure for digital FDM discrimination can be summarized as follows:

Step 1: Sample the composite signal F(t) at equal time intervals t_o.

Step 2: Select Δ and construct the ensemble $F_m(t)$, m=1,2,...,M in accordance with Eqs. (4-2) and (4-3).

Step 3: Compute the elements A_{mn} of the matrix [A] in accordance with Eq. (4-13) and (4-16). Note that due to symmetry, only $(M^2+M)/2$ distinct elements need to be computed.

Step 4: Determine the subcarrier frequencies by solving Eq. (4-15) for the unknown ω.

4.3 FEASIBILITY STUDIES

4.3.1 Solution Method

A direct method to solve Eq. (4-15), i.e., to implement Step 4, was attempted during the feasibility study, but without success. It appears, therefore, that the solutions must be obtained by an iterative process. Fortunately, the appearance of the unknown variable ω is restricted to

the first row and the column of the matrix [A] so that all other elements, i.e., A_{mn}, $m \neq 0$, $n \neq 0$, require computations only one time for the determination of a complete set of ω_m (i.e., for a given time slice of the composite signal).

During the study, a large set of different parameter values were used and the determinant was evaluated. Figure 4-1 illustrates a typical relationship between the determinant and the frequency. It is noted that determinant is nonnegative and that zeros occur where the determinant is also a minimum.

4.3.2 The Effect of Noise

When noise was added to the composite signal, and when a finite number of bits was employed to represent the samples F_{mk}, the original curve in Fig. 4-1 would change shape and in many cases not touch or cross the zero axis. In other words, the eigenvalue problem as formulated will not have a solution under these circumstances, as could be expected since there are more signal frequency components than equations. A typical curve for a "noisy" composite is also shown in Fig. 4-1. However, in all cases where the peak noise to signal ratio is less than 0.16 and where the word size is 12 bits or more, the minimums provide very accurate locations of the subcarrier frequencies if an adequate value of K is used (i.e., if an adequate amount of data from the composite signal is used in the estimate).

Since both the noise and the finite word size are unavoidable in practical constraints, Step 4 of the discrimination technique must be modified to read as follows:

> Step 4M: Determine the subcarrier frequencies by finding the locations of the minimums of the determinant of [A].

4.3.3 Scope and Typical Results of Feasibility Study

During the feasibility study, the following parameter ranges were covered:

> Wideband random noise: 0, 1, 2, 4, 6, 16 and 32 percent of peak signal
>
> Sample word size: 8 to 12 bits plus "ideal" case*

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* As simulated by a 64-bit floating point word.

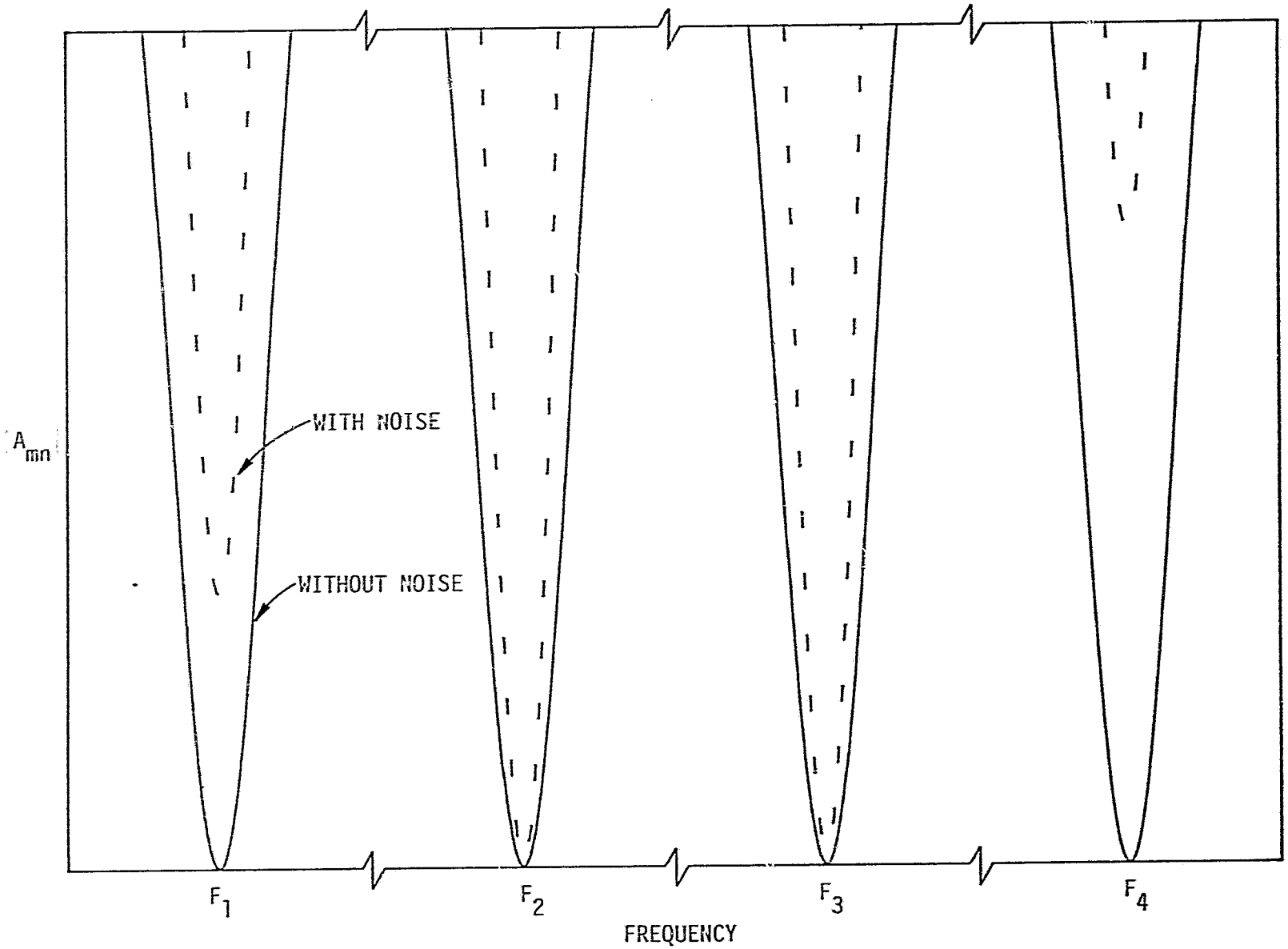

Fig. 4-1 Typical Determinant-Versus-Frequency Curve

Sampling rate: 2.01 to 2.5 times highest signal frequency content

Number of samples: 64, 128, 256 and 512 samples

Delay between ensembles: 1, 2, 4, 8 and 16 sample periods.

Results of the numerical experiments indicate that even for a composite signal containing as many as 16 subcarriers, with 4% of random wideband noise and with a sample word size of 12 bits (11 bits plus sign), excellent results were obtainable, as illustrated in Table 4-3.

Table 4-3 Example of Accuracy in Discriminating a 16-Subcarrier Composite Signal

SUBCARRIER		ERROR IN FREQUENCY DISCRIMINATION (PERCENT OF SUBCARRIER)
NUMBER	FREQUENCY (kHz)	
1	12.0	-0.02
2	14.0	0
3	18.5	+0.01
4	24.0	0
5	28.0	-0.01
6	32.0	-0.04
7	36.0	-0.01
8	48.0	0
9	56.0	0
10	62.0	+0.01
11	68.0	0
12	75.0	0
13	81.0	0
14	87.0	0
15	93.0	-0.01
16	100.0	0

It should be added, however, that in order to achieve the above accuracy, a relatively long effective averaging time was required (approximately 2.25 ms, or 512 samples per ensemble).

The most extensive numerical investigation was conducted for the case representing the seven subcarrier frequencies used for the BSMT program. Results are tabulated in Tables 4-4, 4-5, and 4-6 to provide an insight to the effects of varying some of the key parameters.

Table 4-4 Typical Effect of Sample Word Size on Accuracy of Frequency Determination

SUBCARRIER		ERROR (PERCENT OF SUBCARRIER)				
NUMBER	FREQUENCY (kHz)	WORD SIZE (BITS)				
		IDEAL	12	10	8	6
1	200	0	0	+0.01	+0.02	+0.08
2	320	0	0	0	0	-0.01
3	440	0	0	0	0	+0.01
4	560	0	0	0	-0.01	0
5	680	0	0	0	0	-0.01
6	800	0	0	0	-0.01	-0.01
7	960	0	0	0	-0.01	-0.02

SAMPLING RATE: 2,073,600 SAMPLES/SECOND
RANDOM NOISE: 0
AVERAGING: 128 SAMPLES/ENSEMBLE

Table 4-5 Typical Effect of Averaging on Accuracy of Frequency Determination

SUBCARRIER		ERROR (PERCENT OF SUBCARRIER)		
NUMBER	FREQUENCY (kHz)	SAMPLES PER ENSEMBLE		
		512	256	128
1	200	-0.01	-0.01	>0.10
2	320	+0.01	-0.05	-0.05
3	440	0	+0.02	-0.01
4	560	+0.01	+0.02	+0.03
5	680	+0.01	+0.01	0
6	800	0	0	-0.01
7	960	0	-0.01	-0.04

SAMPLING RATE: 2,073,600 SAMPLES/SECOND
RANDOM NOISE: 32%
SAMPLE WORD SIZE: 8 BITS

Table 4-6 Typical Effect of Noise on Accuracy of Frequency Determination

SUBCARRIER		ERROR (PERCENT OF SUBCARRIER)					
NUMBER	FREQUENCY (kHz)	NOISE (PERCENT PEAK NOISE TO PEAK SIGNAL)					
		1	2	4	8	12	32
1	200	0	0	-0.01	-0.01	-0.01	-0.02
2	320	0	0	0	-0.01	-0.03	-0.06
3	440	0	0	+0.01	+0.01	+0.01	+0.02
4	560	0	0	0	+0.01	+0.01	+0.02
5	680	0	0	0	+0.01	0	+0.01
6	800	0	0	0	0	0	0
7	960	0	0	0	0	0	-0.01

SAMPLING RATE: 2,073,600 SAMPLES/SECOND
SAMPLE WORD SIZE: 8 BITS
AVERAGING: 256 SAMPLES/ENSEMBLE

4.3.4 Conclusions of Feasibility Study

Based on results of the feasibility study, the following conclusions which directly affect the design approach of an all-digital FDM discrimination system are apparent:

- A 10-bit analog-to-digital converter is desirable although an 8-bit unit is adequate.
- With a noisy signal, a tradeoff between accuracy and averaging time is possible. The latter corresponds to the rise time of an analog discriminator.
- Better accuracies are usually obtained for the higher subcarrier frequencies in a given composite. For that reason, a delay time, Δ, of approximately one-half of a period of the lowest frequency subcarrier produces the optimum results by providing as much "independency" between ensembles as possible at the lowest frequency.

- The determinant of the governing frequency equation is nonnegative. To find the subcarrier frequencies, it is necessary to determine the locations of the minimums of the determinant.
- At and near each minimum, the determinant versus frequency relationship can be accurately represented by a quadratic. The subcarrier frequency can therefore be determined with sufficient accuracy by computing the value of the determinant at three distinct, nearby frequencies.

4.4 IMPLEMENTATION

Steps 1 through 3 of Section 4.? can be implemented entirely in hardware with currently available technology, and, therefore, be accomplished in real time for the maximum sampling rate. The following analysis provides the necessary details for the hardware implementation concept.

From Eqs. (4-13), (4-7) and (4-3), and for $m, n \neq 0$,

$$
\begin{aligned}
A_{mn} &= \sum F_{mk}\, F_{nk} \\
&= \sum F_m(kt_o)\, F_n(kt_o) \\
&= \frac{1}{4}\sum [F'_m(kt_o) - F'_m(-kt_o)][F'_n(kt_o) - F'_n(kt_o)] \\
&= \frac{1}{4}\sum F[kt_o + (m-1)\Delta]\, F[kt_o + (m-1)\Delta] \\
&- \frac{1}{4}\sum F[kt_o + (m-1)\Delta]\, F[-kt_o + (n-1)\Delta] \\
&- \frac{1}{4}\sum F[kt_o + (m-1)\Delta]\, F[kt_o + (n-1)\Delta] \\
&+ \frac{1}{4}\sum F[-kt_o + (m-1)\Delta]\, F[-kt_o + (n-1)\Delta]
\end{aligned}
\qquad (4\text{-}17)
$$

where all summations in Eq. (4-17) are over the range (-K,K). For that reason, term numbers 1 and 4 on the right-hand side of the last equal sign are the same; so are the term numbers 2 and 3. Consequently,

$$
\begin{aligned}
A_{mn} &= \frac{1}{2}\sum F[kt_o + (m-1)\Delta]\, F[kt_o + (n-1)\Delta] \\
&- \frac{1}{2}\sum F[kt_o + (m-1)\Delta]\, F[-kt_o + (n-1)\Delta] \\
&= \frac{1}{2}\sum F[kt_o + (m-1)\Delta]\, F[kt_o + (n-1)\Delta] - F[-kt_o + (n-1)\Delta]
\end{aligned}
\qquad (4\text{-}18)
$$

Denote

$$\Delta = ht_o \tag{4-19}$$

and

$$F(\ell t_o) = f(\ell) \tag{4-20}$$

Then Eq. (4-18), the expression for the matrix coefficient A_{mn} (for m, n $\neq$ 0), can be written in the desired form below:

$$A_{mn} = P_{mn} - N_{mn} \tag{4-21}$$

with

$$P_{mn} = \frac{1}{2}\sum f[k + (m-1)h]\ f[k + (n-1)h] \tag{4-22}$$

and

$$N_{mn} = \frac{1}{2}\sum f[k + (m-1)h]\ f[-k + (n-1)h] \tag{4-23}$$

Also,

$$A_{mo} = A_{om} = \sum f[k + (m-1)h]\ \sin(\omega k t_o) \quad , \quad m \neq 0 \tag{4-24}$$

and

$$A_{oo} = \sum \sin^2(\omega k t_o) \tag{4-25}$$

where, again, all summations are over the range (-K,K).

The real-time computation of P_{mn} is shown in concept in Fig. 4-2 for the case of seven subcarriers and using h=1 (i.e., the delay between successive ensembles in a single sampling period).

In Fig. 4-2, consider the output of Multiplier No. 1 and its associated delay register, accumulator and output register. Initially (assume all stages of all registers are filled with zeros when the first data samples reach Stage 1), the output of the multiplier becomes $f^2(-K)$, and the accumulator content also becomes $f^2(-k)$. One sample period later, the multiplier output is $f^2(-k+1)$, and the accumulator content is $f^2(-K)+f^2(-K+1)$, etc. Therefore,

after (2K+1) periods, the accumulator contains the coefficient P_{11}, which is shifted at that time into the output (matrix coefficient) register. Beginning with the next period, the delay shift register output will be generally non-zero, and will be subtracted from the previous content in the accumulator while a new squared term is added to it, producing the coefficient P_{22}. The computation of all diagonal terms of the matrix is completed in this way after (2K+7) sample periods and the results are stored in the output register as shown in Fig. 4-2.

Computation for off-diagonal terms (P_{mn},$m \neq n$) follows the same logic and is accomplished with identical hardware (as shown in Fig. 4-2) and procedure, and is accomplished in the same (2K+7) periods. Computation for the matrix components N_{mn} can be obtained by a similar setup, but by moving data samples in the reverse direction. Finally, the computation of coefficients in the first row (or the first column) can be accomplished with the setup in Fig. 4-3.

If Step 4M (Section 4.3.2) can be accomplished during an averaging period defined by the 512 samples, then the storage requirement will not be a problem because each output represents required data. However, this computational speed is clearly beyond the capability of currently available computers or even array processors, but may soon be within reach of very large-scale integration of the so-called Systotic architecture (Ref. 20) in which large arrays of simple computational elements (PE) are interconnected. Data enter into the processing array from one or more points (or a front), are partially processed by the first line of PE's, and the intermediate results are passed onto the next line of PE's, after which new data are taken in by the first-line PE's and the process repeats. The partially processed data front moves toward the final line of PE's and eventually emerges from the output ports as completely processed data. Theoretical methods to accomplish matrix arithmetics have been investigated by Ahmed, Delesone and Morf (Ref. 25). The prospect of real-time, consequently all-digital FDM discrimination using the approach developed during this study is promising.

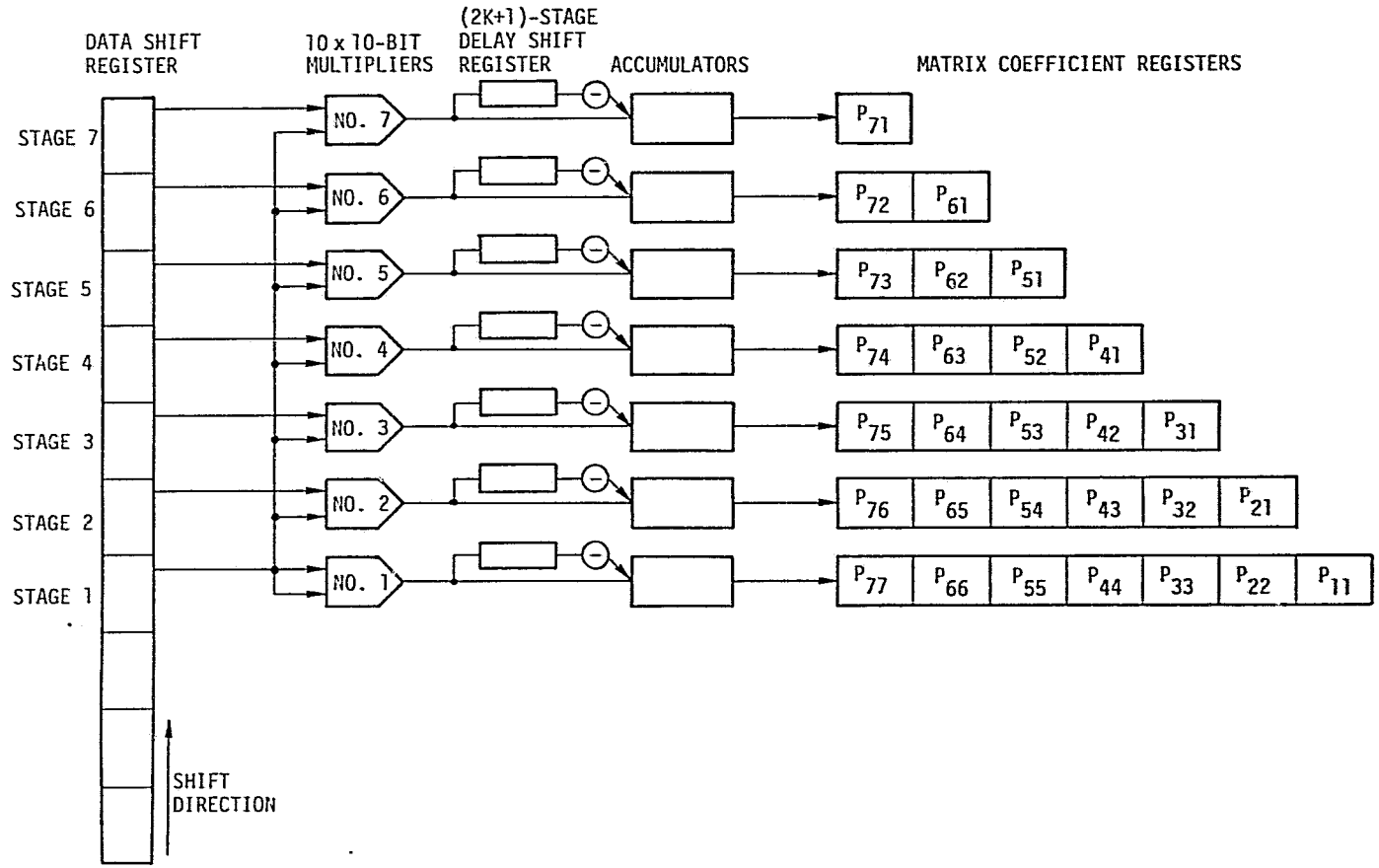

Fig. 4-2 Conceptual Design of Real-Time Matrix Coefficient Computation (Part 1)

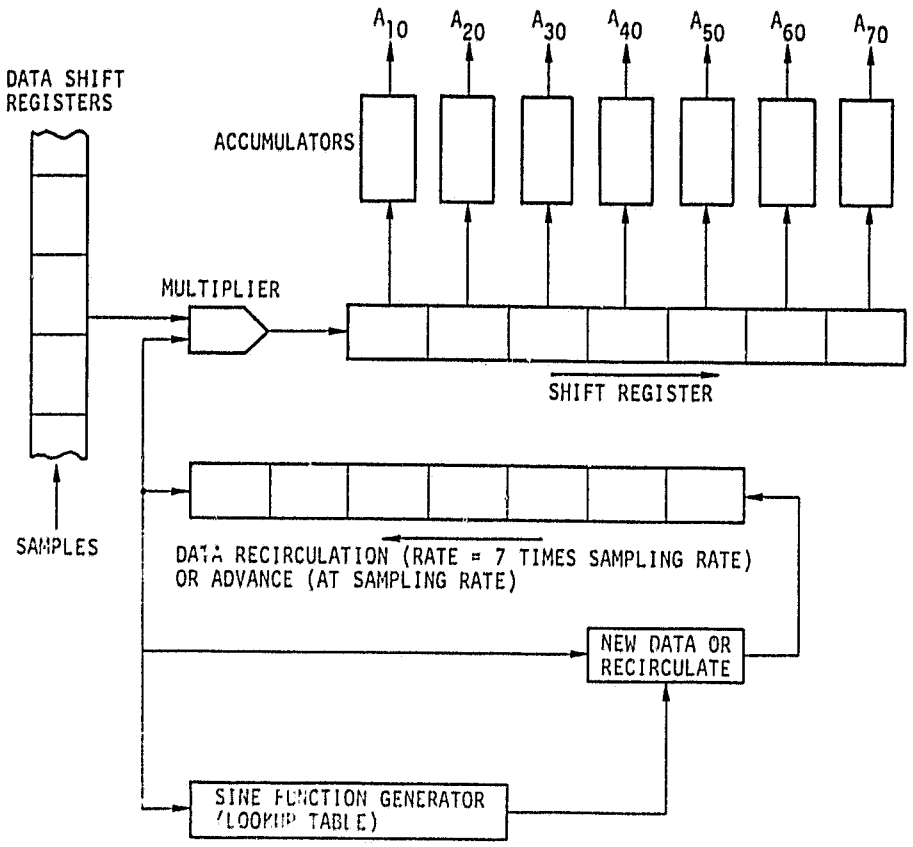

Fig. 4-3 Conceptual Design of Real-Time Matrix Coefficient Computation (Part 2)

Before real-time solution of Step 4M becomes a reality, samples of the composite or intermediate results from Steps 1 to 3 (using hardware) must be stored. Since these intermediate data are naturally grouped in small blocks, and naturally ordered in time, sequential mass storage (i.e., magnetic tape) will be adequate.

5.0 POWER LINE FREQUENCY NOISE REDUCTION STUDY

Approaches to remove line frequency induced noises from measured data were investigated. A simple method has been developed and demonstrated via numerical simulations. The algorithm can be adopted as an optional preprocessing routine for most signal analysis programs.

The problem and the preferred method of solution are described in Sections 5.1 and 5.2. A brief description of the procedure developed to accomplish the objective is included in Section 5.3. Sample results were obtained with simulated data and are shown in Section 5.5.

5.1 PROBLEM DEFINITION

5.1.1 Noise Sources and Characteristics

Due to various instrumentation and test setup difficulties which are usually encountered (and which are often impractical to eliminate) during a test, measured data frequently include noises which are harmonically related to the 60-Hz power line frequency. A drastic and not unusual example of noises of this type is the very large and sharp spikes which originate from a power supply employing SCR in a test setup which can contaminate all instrumentation and the resulting data. Noise spikes are also commonly found where thyristor AC power control is employed (e.g., to provide and control high power heating in an environmental test). Another source of line frequency noise is due to improper instrumentation practices such as bad grounding of signal returns, use of signal conditioning equipment with poor common-mode rejection capabilities, etc.

Regardless of the cause, noises of this type are periodic in nature (i.e., the fundamental and harmonic frequencies and amplitudes are practically constant) during a short time span. Over a longer duration (as compared with a single period of the noise), however, the line frequency may drift, so that the technique employed to eliminate the noise from the signal must not depend on the fundamental noise frequency to be exactly 60 Hz, or even known, a priori, to any reliable degree of accuracy. This is especially true if the signal

source is recorded on and reproduced from analog tapes where wow and flutter will modulate the noise frequency. Indeed, the technique should be such that it may be used to eliminate "almost" periodic noises of any frequency.

5.1.2 Noise Identification Difficulties

Due to a combination of common digital data reduction practices delineated below, power line noises are usually "smeared" rather than appearing as clean spectral lines on, say, a PSD plot, even when both the frequency and amplitude are perfectly constant. These factors are:

(1) Frequently, the sampling frequency of the A/D process is chosen to be 10^a samples per second, with a being an integer.

(2) Employing an FFT algorithm, time slices of 2^b samples are used* for analyses, where b is also an integer.

(3) For a noise with a 60-Hz nominal fundamental frequency, a sampling rate of 10^a does not fit an even number of cycles of the noise in a time slice of 2^b samples. For example, if the sampling rate is 10,000 sps, a time slice defined by 8,192 (2^{13}) points is 0.8192 seconds which will contain 49.152 cycles of 60-Hz noise, 98.304 cycles of the second harmonic, 147.456 cycles of the third harmonic, etc. The analysis resolution on the frequency axis for this example is (2/0.8192) sec or 2.4414 Hz. Referring to Fig. 5-1, a purely sinusoidal noise of 60 Hz would, consequently, have an apparent spectrum (even without spectral Hanning) which is not a line at all.

Hanning is used in spectrum analyses to improve confidence on the spectral magnitude -- at the sacrifice of frequency resolution. As an undesirable element, the power line noise is easy to spot. As a time series, it is not trivial to define its precise characteristics under the above circumstances. Consequently, it is also difficult to just look at the PSD and evaluate the success or failure of a technique used to eliminate the noise.

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* It is immaterial for this problem whether zero fill is made or not.

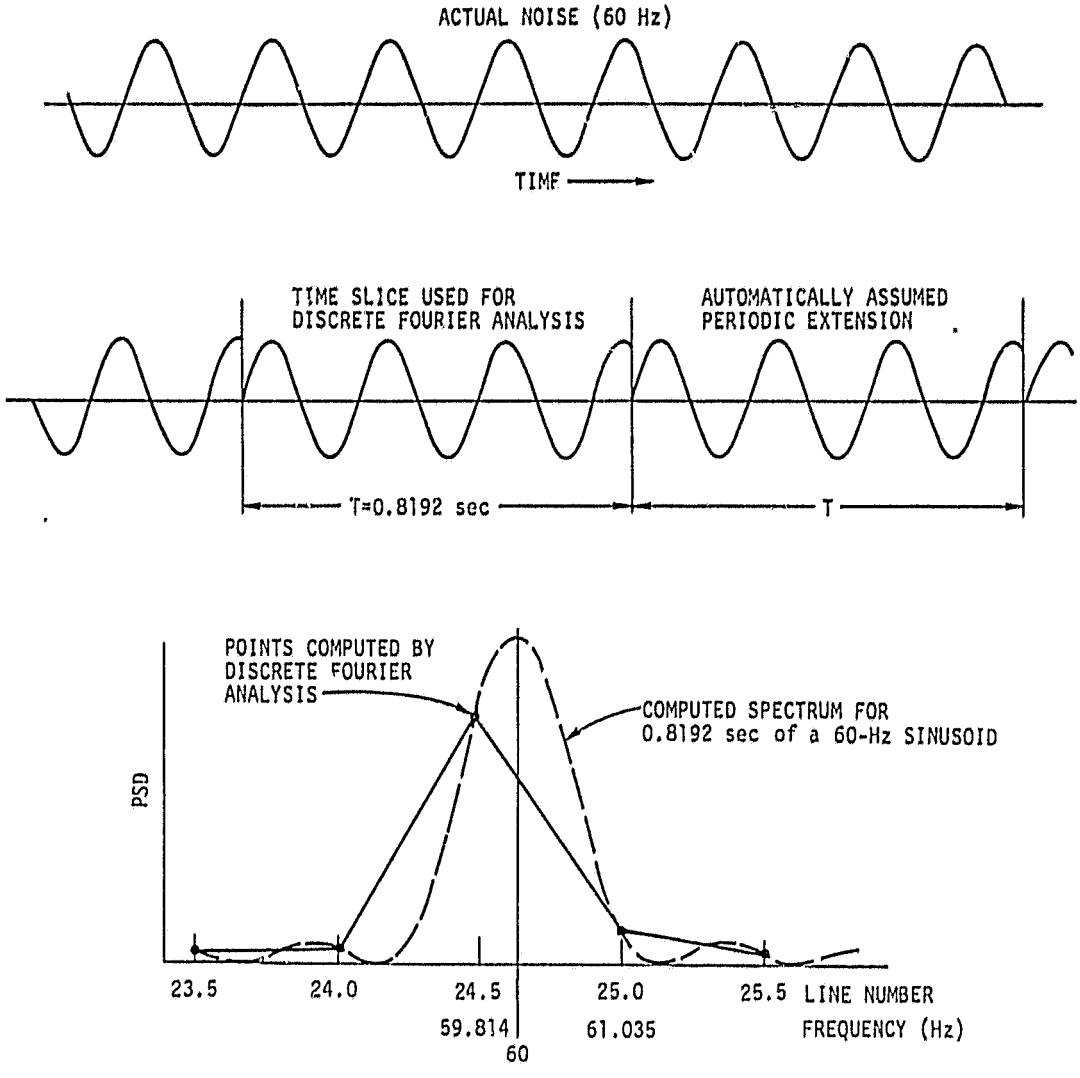

Fig. 5-7 Effect of Using Noninteger Periods of a Sinusoidal on Discrete Fourier Analysis

5.2 LINE NOISE ATTENUATION TECHNIQUE

5.2.1 General Approach

For short durations on the order of several seconds, the line noise can be regarded as both stationary and deterministic. The proper approach to eliminate such unwanted noise is to identify its characteristics, i.e., frequencies, phases and amplitudes, and then remove (subtract) it from the original signal. The resulting, cleaned signal will be in all respects identical to the original one with the exception that components at the line frequency and its harmonic frequencies have been removed. The method, in effect, will appear to perform the function of a comb filter with extremely narrow notches, but does not possess intrinsic shortcomings of narrow filters such as long-time constants, low damping, phase or spectrum distortion, etc. Conventional filtering is more applicable if noise characteristics are nonstationary and/or indeterministic, but is not a useful approach for combating line noises unless their frequencies are totally outside of the signal band(s) of interest.

5.2.2 Analysis

The effectiveness of the above outlined approach may be measured by calculating the residual noise at each of its harmonic frequencies after the attempted "cleanup" operation.

Let $x(t)$ be the total signal including line frequency noises, and more explicitly, let

$$x(t) = y(t) + z(t) \tag{5-1}$$

where $y(t)$ is the real signal and $z(t)$ is the line frequency noise, with a fundamental frequency ω and harmonics at 2ω, $3\omega,\ldots,I\omega$, where I is an integer, i.e.,

$$z(t) = \sum_{i=1}^{I} A_i \cos i\omega t + B_i \sin i\omega t$$

$$= \sum_{i=1}^{I} C_i \cos(i\omega t + \theta_i) \tag{5-2}$$

where A_i and B_i are the Fourier coefficients, $C_i^2=(A_i^2 + B_i^2)$, and θ_i are phase angles.

If the preliminary step in the noise reduction procedure is perfect, i.e., if ω, A_i and B_i were determined very accurately, then $z(t)$ is exact and when subtracted from $x(t)$, only $y(t)$, the desired signal, would remain and the objective would be achieved. Suppose, on the other hand (and being realistic), the preliminary step was only capable of yielding approximately correct estimates of ω, A_i and B_i. The degree of success of the noise reduction program is defined by the residual noise

$$\begin{aligned} R(t) &= z(t) - z'(t) \\ &= \sum_{i=1}^{I} A_i \cos i\omega t + B_i \sin i\omega t \\ &\quad - \sum_{i=1}^{I'} A_i' \cos i\omega' t + B_i' \sin i\omega' t \end{aligned} \tag{5-3}$$

where $z'(t)$, ω', A_i', B_i' and I' are approximations of $Z(t)$, ω, A_i, B_i and I, respectively. Both I and I' are integers. Clearly if $I'<I$, then noise harmonics for $I'<i\leq I$ will not be reduced. If $I'>I$, then noise components will be added. The following analysis provides a measure of the residual noise due to estimating errors on the other parameters.

The residual noise of Eq. (5-3) may be rewritten as:

$$R(t) = \sum_{i=1}^{I} R_i(t)$$

with

$$\begin{aligned} R_i(t) &= A_i(\cos i\omega t - \cos i\omega' t) + (A_i - A_i') \cos i\omega' t \\ &\quad + B_i(\sin i\omega t - \sin i\omega' t) + (B_i - B_i') \sin i\omega' t \\ &= 2\sqrt{A_i^2+B_i^2} \sin\left(i \frac{\omega+\omega'}{2} t + \psi_i\right) \sin i \frac{\omega-\omega'}{2} t \\ &\quad + (A_i - A_i') \cos i\omega' t + (B_i - B_i') \sin i\omega' t \end{aligned} \tag{5-4}$$

Let

$$\omega_1 = (\omega+\omega')/2$$

$$\omega_2 = (\omega-\omega')/\omega$$

$$T = 2/\omega$$

$$\tau = t/T$$

$$a_i = (A_i-A_i')/C_i$$

$$b_i = (B_i-B_i')/C_i$$

r_i = Maximum value of $R_i(t)/C_i$.

Then Eq. (5-4) may be rewritten in the following format for establishing an upper bound on r_i, the magnitude of the residual noise component corresponding to the i^{th} noise harmonic frequency:

$$R_i(t)/C_i = 2 \sin(i\omega_1 t+\psi_i) \sin(i\pi\omega_2\tau) + a_i \cos i\omega' t + b_i \sin i\omega' t \qquad (5\text{-}5)$$

It is obvious from the last equation that

$$r_i \leq 2 \sin(i\pi\omega_2\tau) + a_i+b_i \qquad (5\text{-}6)$$

Thus, the estimation error on each noise component amplitude, (a_i+b_i), contributes to the residual noise amplitude in direct proportion after the application of the noise reduction algorithm. A 1% error on the amplitude will leave, at most, a 2% residual noise amplitude, etc.

On the other hand, in view of the first term on the right-hand side of Eq. (5-6), an error in determination of the noise frequency could produce a residual noise amplitude which is twice as large as the original noise (i.e., a 200% worsening of the situation). Therefore, the success of the method of noise cancellation, as proposed in this approach, hinges almost totally on the ability to keep the magnitude of this term small, which can be achieved only if (1) the noise frequency can be determined accurately since

$\omega_2=(\omega-\omega')/2\omega$, and if τ is kept to a reasonable value. In order to obtain an idea on the accuracy required on frequency determination, consider the following case:

$i = 1$

$\omega_2 = 0.002$ (i.e., a 0.4% error on frequency determination)

$\tau = \pm 5$ (a time slice of 1.667 sec)

$2 \sin(i\pi\omega_2\tau) = 0.0628$

The noise magnitude is, hence, reduced from 1.0 to 0.0628, a 24-dB attenuation.

5.2.3 Procedure

The method of noise reduction depends critically on the ability to determine its frequency in the presence of the signal which could be random, wide band, narrow band, periodic or a combination of all such characteristics. Prony's method will not work due to the presence of non-harmonic signals. Several other hardware and software approaches were investigated. The most successful among them is described below. A numerical simulation was developed for the method. Typical accuracies of better than $\pm 0.05\%$ were obtainable from numerical experiments. Based on these results, it was concluded that noise attenuation of 20 dB or more is achievable for each harmonic.

In order to limit the number of noise harmonics so that the procedure will be practical, the signal is first low-pass filtered, using a filter cutoff (-3 dB) frequency of 200 Hz. The frequency and amplitude of the remaining noise components are determined by minimizing the mean-squared error

$$J = \sum_{k=1}^{K} (x_k - z_k)^2 \qquad (5\text{-}7)$$

where x is sampled values of the filtered signal containing the three lowest line frequency noise components at approximately 60 Hz, 120 Hz and 180 Hz. The sequence z_k is given by the expression:

$$z_k = \sum_{i=1}^{3} A_i \cos i\omega t_k + B_i \sin i\omega t_k \qquad (5\text{-}8)$$

with the frequency, ω and the coefficients A_i and B_i to be determined by minimizing the error J.

Following standard procedures, the normal equations for the coefficients A_i and B_i are obtained by setting partial derivatives of J with respect to the coefficients to zero:

$$\frac{\partial J}{\partial A_j} = 0 \quad \text{and} \quad \frac{\partial J}{\partial B_j} = 0 \qquad (5\text{-}9)$$

where j=1, 2 and 3. Working out the expressions, Eq. (5-9) leads to the set of six simultaneous equations below in A_i and B_i:

$$\sum_{i=1}^{3}\sum_{k=1}^{K} A_i C_k(i)C_k(j) + B_i S_k(i)C_k(j) = \sum_{k=1}^{K} x_k C_k(j), \quad j=1,2,3$$

$$\sum_{i=1}^{3}\sum_{k=1}^{K} A_i C_k(i)S_k(j) + B_i S_k(i)S_k(j) = \sum_{k=1}^{K} x_k S_k(j), \quad j=1,2,3 \qquad (5\text{-}10)$$

where $C_k(i) = \cos(i\omega t_k)$ and $S_k(i) = \sin(i\omega t_k)$. If ω is known and if K is chosen such that $t_K = 2\pi/\omega$, then Eqs. (5-10) are completely uncoupled and become simple expressions for the Fourier coefficients for the total signal at the three known frequencies. In the present case, ω is not known and no effort is made to select K to match the fundamental period. Rather, the value of ω is also to be determined by minimizing J with respect to it. Instead of attempting to find ω analytically from the seventh normal equation by the requirement $\partial J/\partial\omega=0$, the following iterative process is preferred.

An initial estimate on ω is first made and used in Eqs. (5-10) which is then solved for the A_i's and B_i's. The mean squared error, J, is computed. The above process is then repeated until a minimum value for J is found. The value of ω which yields this minimum error is taken as the best estimate of the noise frequency. Once ω is established, the original, unfiltered

signal is used to determine all noise harmonic components at ω, 2ω, 3ω, etc., using the standard Fourier method since the period over which the series is orthogonal is now known. The noise is synthesized by assigning amplitudes to $\cos(i\omega t)$ and $\sin(i\omega t)$, using the Fourier coefficients just determined. Finally, the noise attenuation process is accomplished when the synthesized noise is subtracted from the original signal.

5.3 SIMULATION

A BASIC program was developed in which a wideband signal plus noise components at 59.6 Hz, 119.2 Hz and 178.8 Hz was simulated. The above procedure was applied to find the noise frequencies. Typically, the frequency was determined to accuracies better than $\pm 0.05\%$. Based on the analysis of Section 5.2.2, this implies that a noise attenuation of better than 24 dB is achievable. Program listing and typical results are documented in Ref. 26.

5.4 CONCLUSIONS AND RECOMMENDATIONS

Based on the success of the study, it is recommended that a FORTRAN program be developed and installed as a standard data preprocessing routine.

The most time-consuming and critical step in the noise elimination procedure is that of determining the fundamental frequency of the noise. It is recommended that in the future, if a data reduction requesting organization is seriously concerned with line frequency noise problems, an option should be presented to them to reserve a data recording channel for the actual line voltage. Noise cancellation can then rely on the recorded line frequency itself and will be very easy to accomplish, and what's more important, the result will be totally accurate and question-free.

6.0 GENERAL-PURPOSE PROCESS CONTROLLER

A recurring requirement in data reduction is the controlling of various types of equipment such as PCM bit/frame synchronizers, FDM filter parameters, ADC's, oscillograms, calibration signal sources, etc. A study was conducted to develop a general-purpose control method to achieve the following objectives:

(1) The ability to control a large number of devices which could be physically separated and located in various areas within the data reduction facility

(2) Easy interface to any computer to perform the automation function

(3) Minimum or no system software modifications

(4) Easily developed application programs

(5) Manual setup provisions

(6) Display of all control functions

Since high speed is not essential, control via serial communication offers an attractive approach as all computers (from the smallest microprocessor-based system to the main frame) already have software and hardware provisions for serial communications with CRT terminals. A typical computer terminal contains nearly all of the hardware adaptable to perform the required control functions (e.g., the UART for serial/parallel data conversion reception and transmission, the CRT for display, and the keyboard for manual control), it was natural to investigate the possibility of modifying and adapting such a device for the required control system.

The Lear-Siegler ADM-3A terminal was selected for this study and a design based on this device has been developed. When in use, a six-bit control function is implemented in one-to-one correspondence with characters being displayed on the CRT. When fully implemented, a total of 1920 six-bit control characters will be available in hardware, using just one ADM-3A and one communications interface of the computer.

Figure 6-1 is a block diagram showing how the characters displayed on the CRT are brought out as hardware bits for control functions. Shift registers are employed to transport and retain control data and as output registers. The need to address individual control locations is avoided in favor of design simplicity.

At a rate of 19,200 baud per second, the entire display screen (or all 1920 x 6 bits of control) can be changed in one second. Because of the latched nature of the output of the shift registers, updating is only seen by those devices under control which require it. The actual maximum time required to update all bits is 1/30 second (which is determined by the display screen refresh rate of 1/60 second) after the data is received from the computer.

Manual interactive control is achieved via the standard keyboard and the CRT display, with the terminal set in the half-duplex mode and using a nondestructive cursor. In application, the keyboard can be locked out with a single control word from the computer to avoid accidental changes of data reduction setup.

As pointed out earlier, almost all computer systems can communicate with a CRT terminal either directly or via modems. The system software driver is already developed and requires no modification. The application program can be written in any language so that both versatility and redundancy are easily achieved.

6.1 PRINCIPLE OF OPERATION

Referring to Fig. 6-1, the image on the ADM-3A CRT is a raster-scan of ASCII characters stored in the REFRESH MEMORY (7 bits by 1920 characters) which were received by the DATA RECEIVER LOGIC AND COMMAND DECODERS. For each line of display, 80 characters are taken from the REFRESH MEMORY and kept one at a time in the LATCHES, which hold and sequentially present the data to the ROM CHARACTER MEMORY. For each row, 11 sweeps over the 80 characters are necessary to display 11 dots in a vertical column (nine dots for the displayed characters and two undots for space between rows).

For the general-purpose controller (GPC), data are taken out in parallel in the same manner from the output of the latches during the first

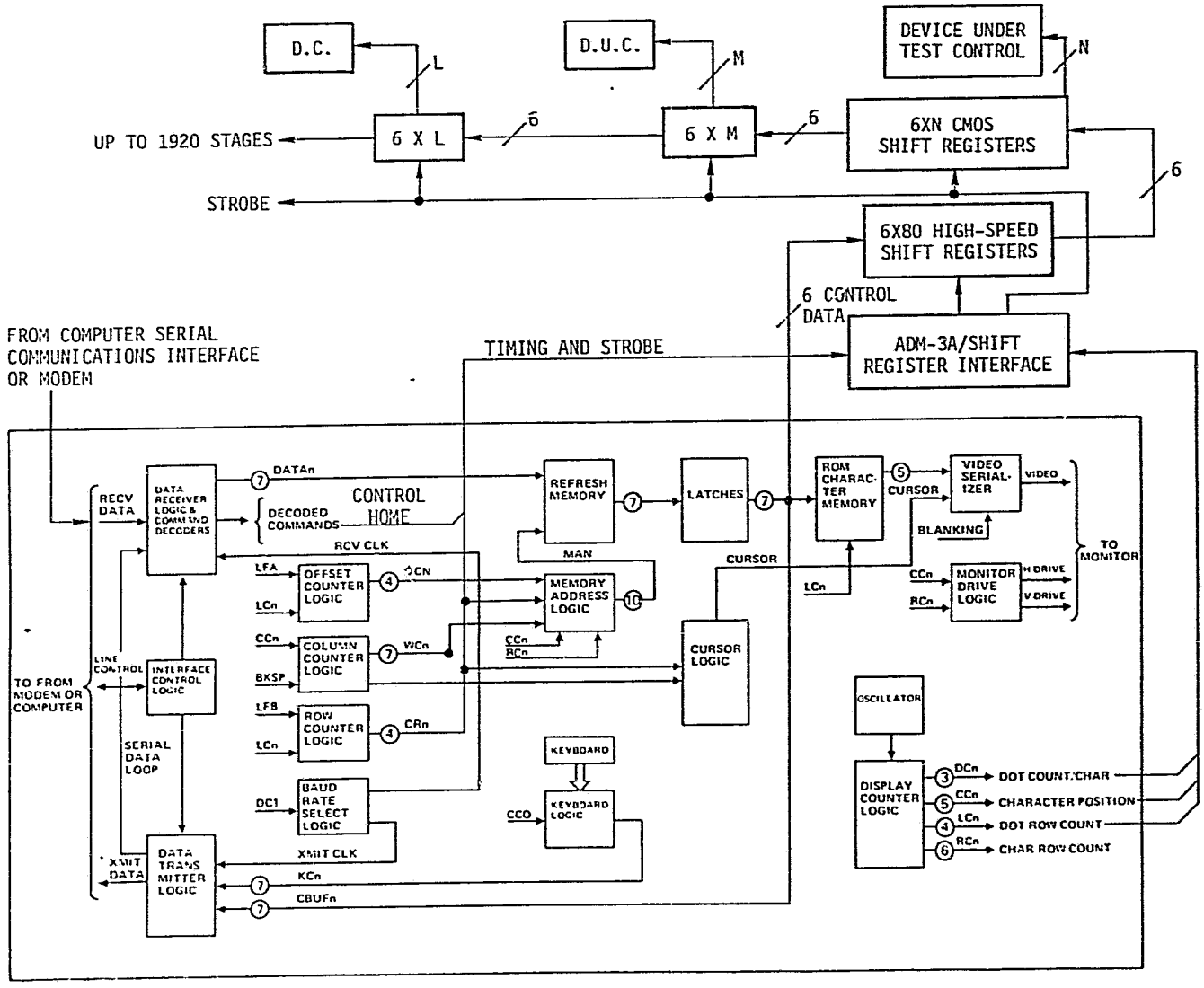

Fig. 6-1 ADM-3A Based Control System Block Diagram

of the 11 sweeps, and are loaded in the 6 x 80 high-speed (TTL) shift registers in a first-in/first-out manner. During the remaining 10 sweeps, these 80 characters (of six bits each) are shifted out into the slower CMOS shift registers. The process is repeated until the entire screen display is shifted out, in 0.0167 second. The procedure is then repeated. If new data have been received during each screen refresh cycle, they will be displayed during the next cycle.

The CMOS shift registers are serial-in parallel-out devices. Furthermore, their parallel outputs are latched so data do not change during shift. In the design, a strobe derived from a HOME input to the ADM-3A is used to update the outputs and all CMOS shift registers.

6.2 SCHEMATICS

Figure 6-2 is a schematic showing details of the interface between the ADM-3A, the GPC, and the high-speed shift registers. Figure 6-3 shows details of a typical eight-stage CMOS shift register section in the GPC. Figure 6-4 is a detailed timing diagram for the operation of the GPC.

6.3 DEVELOPMENT

The GPC design was breadboarded first. A prototype was then developed and used in subsequent study tasks of this project.

The primary advantage of the GPC lies in the fact that the computer interfacing task is already accomplished. The usual difficulties encountered in checking out and debugging new hardware and software simultaneously is completely eliminated. For a given application, the design of the overall control system is reduced to the mere interfacing of standard logic circuits.

Secondary advantages are:

(a) The ability to provide 11,520 (1920 x 6) control bits from a single, low-cost, reliable device

(b) Distributed control via long cables and/or modems

(c) Compatibility with any computer without requiring modifications or special interfaces

(d) Independence from the programming language

(e) Totally parallel manual control

(f) Total display of all control information.

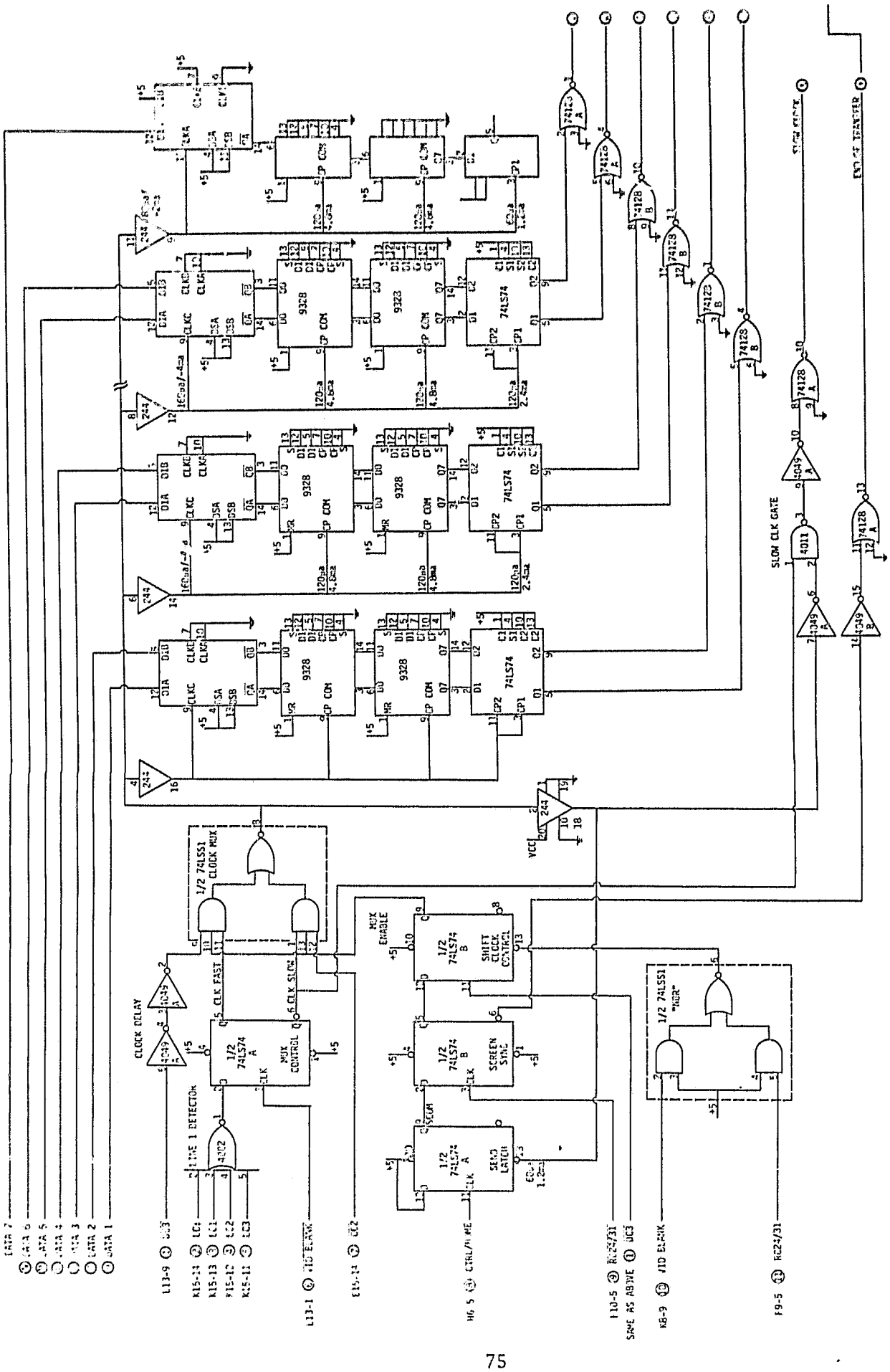

Fig. 6-2 ADM-3A/Shift Register Interface for GPC

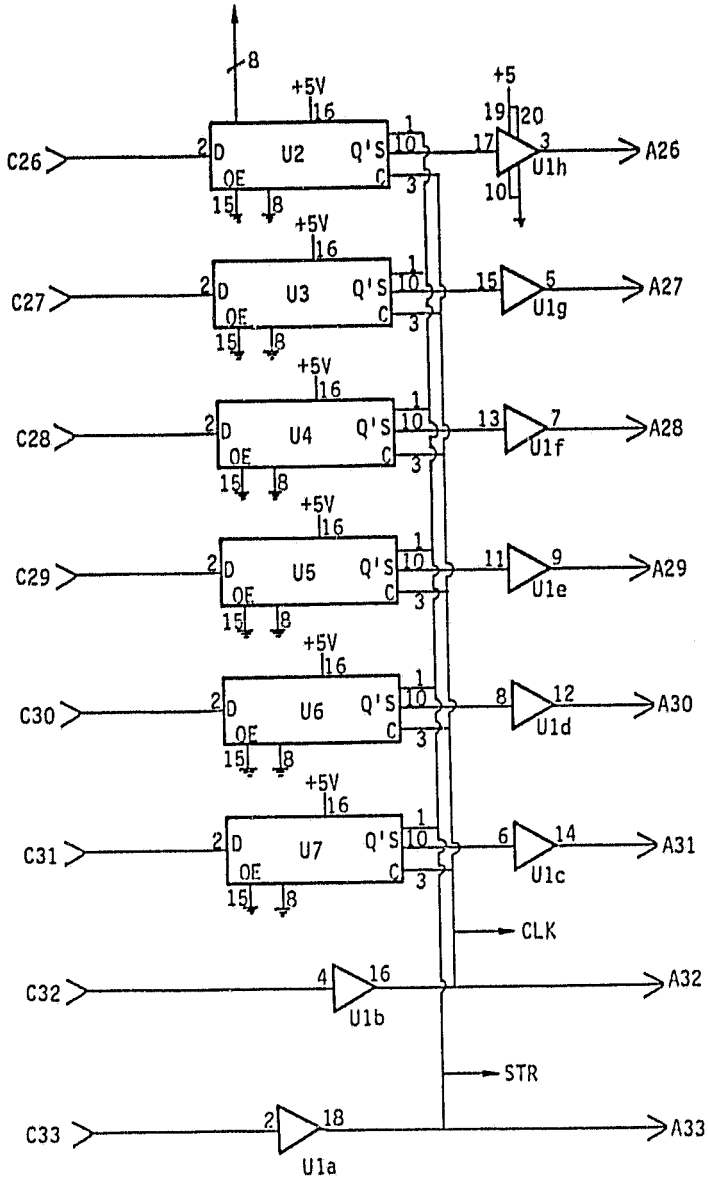

Fig. 6-3 Typical 8-Stage GPC Section

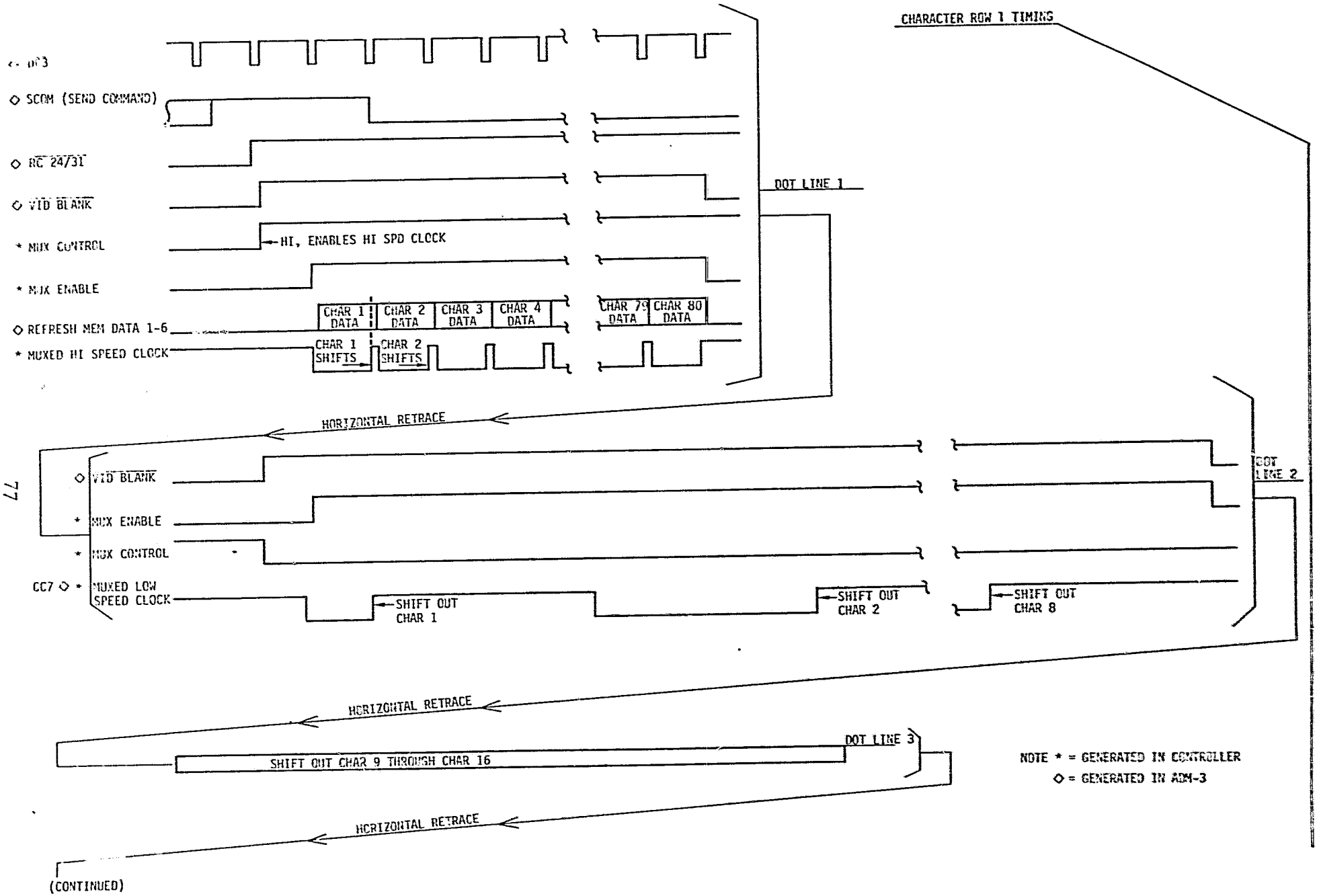

Fig. 6-4 GPC Timing Diagram

Fig. 6-4 GPC Timing Diagram (continued)

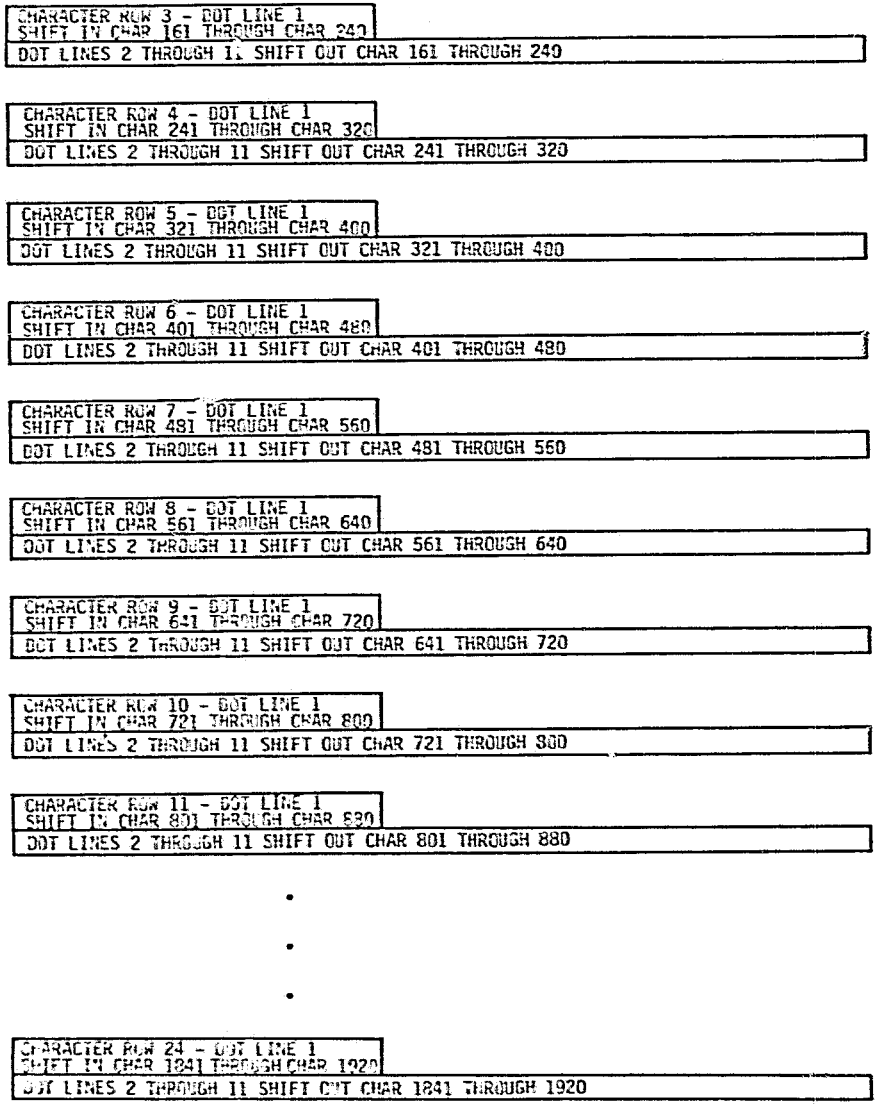

Fig. 6-4 GPC Timing Diagram (continued)

7.0 CONCLUSIONS AND RECOMMENDATIONS

7.1 CONCLUSIONS

Significant improvement in throughput, overall data reduction efficiency and operational flexibility can be realized by the system design concept of Section 3.0. Future expansion capability is provided by adopting an existing standard interfacing specification. The impact of future computer obsolescence can be minimized by delegating those processing functions whose requirements are of lasting nature to dedicated processors implemented in hardware.

Results of the feasibility study on digital FDM discrimination were positive. Large temporary storage of data is required because real-time processing is not feasible with currently available hardware. The overall data system design, however, provides the assurance that when real-time processing does become practical in the future (most likely when Systolic processors become available via VLSI), it can be easily incorporated.

7.2 RECOMMENDATIONS

It is believed that a sufficient amount of conceptual development work in defining the broader features of a high throughput data reduction has been accomplished, and that preliminary design can be initiated on information contained in this report.

Several preliminary development tasks may be undertaken immediately. A recommended initial task is to develop the grpahic display controller indicated in Section 3.4.4, but with currently available hardware, in order to obtain detailed operational requirements for replacing the oscillographs.

A concurrent task may be the breadboarding of the FDM front end to accomplish hardware computation of the matrix coefficients, as in Fig. 4-2. The solution of the frequency equation may be accomplished in the existing CSPI Model MAP300 array processor.

The line noise elimination algorithm should be implemented as a standard data preprocessing routine, as recommended in Section 5.4.

Finally, development in Systolic processing should be followed closely, not only for FDM discrimination, but for signal analysis applications in general.

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