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Item #9

PROCESS RESEARCH ON POLYCRYSTALLINE SILICON MATERIAL

(PROPSM)

QUARTERLY REPORT NO. 9

January 1, 1983 - March 31, 1983

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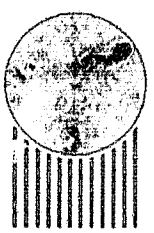

SOLAREX CORPORATION

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The JPL Flat-Plate Solar Array Project is sponsored by the U.S. Department of Energy and forms part of the Solar Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays. This work was performed for the Jet Propulsion Laboratory, California Institute of Technology by agreement between NASA and DOE.

BY

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ABSTRACT

The investigation of the performance-limiting mechanisms in large-grain (greater than 1-2 mm in diameter) polycrystalline silicon was continued by fabricating a set of "mini-cell" wafers on a selection of 10cm x 10cm wafers. A mini-cell wafer consists of an array of small (approximately 0.2cm^2 in area) photodiodes which are isolated from one another by a mesa structure.

The mini-cell wafer set is composed of: (1) three wafers from Semix brick 71-01E near the bottom, in the middle, and near the top; (2) two wafers from Semix bricks C4-108 and C4-116B; (3) a Wacker Silso wafer; and (4) a single-crystal Czochralski wafer as a control.

The junction capacitance of each mini-cell was used to obtain the dopant concentration, and therefore the resistivity, as a function of position across each wafer. The results indicate that there is no significant variation in resistivity with position for any of the polycrystalline wafers, whether Semix or Wacker. However, the resistivity of Semix brick 71-01E did decrease slightly from bottom to top.

The shunt conductance of each mini-cell was used to locate areas on each wafer where the effects of a resistive shunt on any additional electrical measurements can be ignored. The results show that each wafer has areas of contiguous mini-cells in which the values of shunt conductance are less than that which would affect the open-circuit voltage or the fill-factor. However, the dimensions and the location of these "low conductance" areas vary from wafer-to-wafer and with position in the brick.

An effort was begun to investigate the usefulness of a high-temperature heat treatment in order to getter possible minority-carrier lifetime-killing impurities from the bulk.

DESCRIPTION OF PROJECT

The purpose of this program is to determine the mechanisms affecting the conversion efficiency of polycrystalline silicon solar cells and, once knowing these mechanisms, to develop solar cell fabrication processes that take full advantage of its potential as a photovoltaic material. The primary emphasis of this work is on large-grain polycrystalline silicon as supplied by Semix, Inc. However, the results of this work are generic and will be applicable to all polycrystalline silicon materials.

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I. INTRODUCTION

This report summarizes the progress achieved during the fourth quarter of a program to determine the mechanisms affecting the conversion efficiency of polycrystalline silicon solar cells and, once knowing these mechanisms, to develop solar cell fabrication processes that take full advantage of its potential as a photovoltaic material.

Section II of this report summarizes the results that have been obtained by fabricating an array of small (approximately 0.2 cm^2) photo-diodes across several 10cm x 10cm wafers. The variation of the resistivity and the shunt conductance as a function of position across a selection of polycrystalline wafers is presented.

In Section III an experiment to evaluate the usefulness of damage gettering to improve the solar cell characteristics, specifically the short-circuit current, is described.

The conclusions to date on the mechanisms limiting the performance of polycrystalline silicon as a solar cell material are summarized in Section IV.

II. MECHANISMS LIMITING THE PERFORMANCE OF POLYCRYSTALLINE SILICON SOLAR CELLS

A. Mini-Cell Wafer Fabrication

During the previous quarter, two potential process sequences for fabricating the mini-cell wafers were evaluated [1]. A mesa etch isolation scheme was eventually chosen because of its relative insensitivity to processing variables when compared to an alternate process sequence that required an oxide diffusion mask for isolation.

During this quarter, a set of mini-cell wafers was fabricated using the mesa etch isolation process sequence described below and shown in Figure 1. The wafers, which were 10cm x 10cm in size, were chemically polished using a CP-type etch to a thickness of 250 microns, then diffused with phosphorus to a surface resistivity of 80 ohms/□. Individual test cells were isolated fom one another by etching away approximately 10 μm of silicon between the cells resulting in a mesa diode structure. A P^+ layer on the back side of the wafer was formed by alloying aluminum into the wafer. Front contact pads were deposited by evaporating Ti/Pd over photoresist which had been photolithographically patterned. Undesired metal was removed using a lift-off technique. The back contact consisted of a full-coverage Ti/Pd layer. Silver was then electroplated onto the Ti/Pd metallization, and the contacts were sintered.

FIGURE 1. PROCESS SEQUENCE FOR MESA ETCH ISOLATION

1.	Etch 1-3 ohm-cm single crystal wafer to 250±10 μm thickness.	
2.	Diffusion:	80 ohm/□
3.	Mesa Etch Mask:	Spin Photoresist Open Window Frame In Resist
4.	Mesa Etch (CP-Type, 10 μm Removed)	
5.	Strip Resist	
6.	BSF:	Aluminum Paste Bake Alloy HCl Etch
7.	Front Metallization:	Spin Photoresist Open Windows For Tabs Evaporate Ti/Pd Liftoff
8.	Rear Metallization	Ti/Pd
9.	Electroplate Ag	
10.	Sinter	

The set of mini-cell wafers consists of five polycrystalline wafers supplied by Semix, a Wacker Silso polycrystalline wafer, and a single-crystal control wafer. Three of the Semix wafers are from the central portion of an ingot (No. 71-01E) near the bottom, in the middle, and near the top. The remaining two Semix wafers are from the middle of two additional bricks (Nos. C4-108 and C4-116B). The single-crystal control wafer is Czochralski-grown with a resistivity of 1.2 ohm-cm, which is approximately the same as that of the polycrystalline wafers.

B. Variation of Resistivity With Position

Assuming that the diffused junction is abrupt, the dopant concentration of the base, and therefore the bulk resistivity, may be experimentally determined by measuring the capacitance, (C) as a function of reverse bias (V), then determining the slope of a curve of $1/C^2$ versus V [2]. The dopant concentration, N, is given by the relation

$$N = 2/q\varepsilon_{Si}\varepsilon_o\beta$$

where q is the electronic charge, ε_{Si} is the relative dielectric constant of silicon, ε_o is the permittivity of free space, and β is the slope of the $1/C^2$ versus V curve. Knowing the boron dopant concentration, the bulk resistivity is found by use of a curve of resistivity as a function of boron concentration in silicon [3].

While the above technique is rather straightforward, it is also very tedious, particularly if one anticipates evaluating 400 cells per 10cm x 10cm wafer. In order to make it possible to determine the spatial variation of resistivity for the mini-cell wafers, a simpler technique for determining the resistivity from junction capacitance data was necessary. This technique involved the measurement of the junction capacitance with no bias, then using a calibration curve of junction capacitance (at V = 0) as a function of resistivity to uniquely determine the resistivity. Such a calibration curve can be developed by using the above equation with the previously mentioned resistivity versus dopant concentration curve, and by assuming: (1) an abrupt PN junction; (2) no deviation of the value of C at V=0 from the $1/C^2$ versus V curve; and (3) carrier mobilities in polycrystalline silicon which are equal to those in single-crystal silicon. The resultant calibration curve of junction capacitance (at V = 0) versus resistivity is shown in Figure 2. Using this curve, a single capacitance measurement, rather than several, is adequate to determine the base resistivity with good accuracy.

The junction capacitance measurement was made using a General Radio 1672-A Automatic Capacitance Bridge whose oscillator voltage is 100mV with the cell in the dark and with no bias. The results for the mini-cell wafers showing the derived base resistivity, in ohm-cm, as a function of position

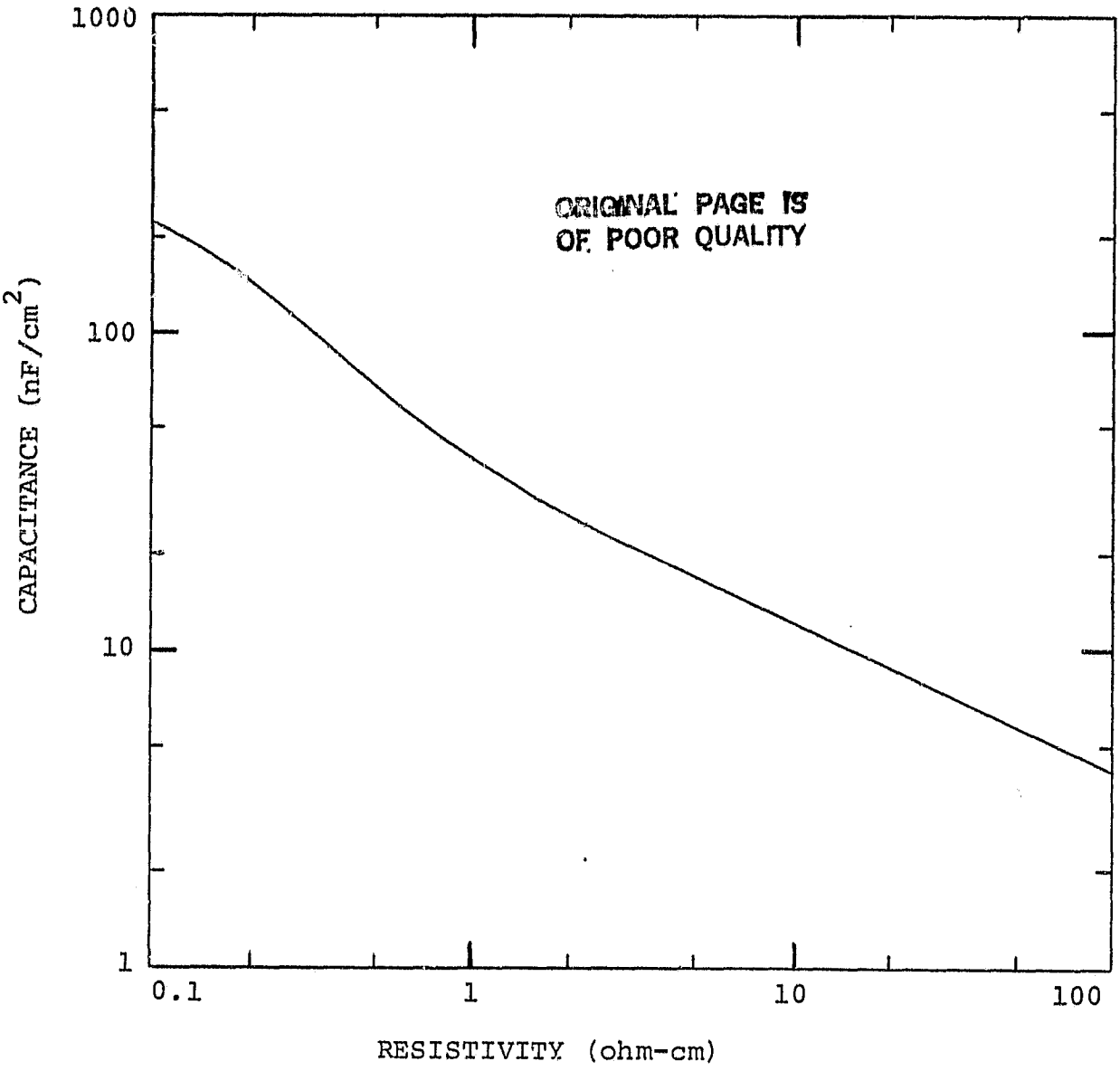

FIGURE 2. Junction capacitance as a function of resistivity; bias voltage = 0 V.

are given in Figures 3 to 9. Resistivity values that are missing in these figures indicate areas where the test cell shunt conductance is too high (greater than 1 mmho) to make a meaningful measurement of junction capacitance from which to determine resistivity. These shunted areas may possibly, though not necessarily, be due to some defect in the wafer; however, they may also be due to interaction between the silicon and the processing. The cause of higher values of shunt conductance in any particular cell can only be determined by additional measurements and observations.

Figure 3 shows the results for the single-crystal control wafer. A crack runs across the wafer from bottom left to top right; the cells along this crack were unmeasurable. In addition to these cells, there were quite a few which were shunted most likely due to a defect introduced during processing. The resistivity, which should be uniform, was measured to be 1.1 to 1.2 ohm-cm, which gives a range on the reproducibility of the single-point technique on single-crystal silicon of $\pm$ 10%.

Figures 4, 5, and 6 show the spatial variation of resistivity from wafers near the bottom, in the middle, and near the top of brick 71-01E, respectively, all of which were cut from the central portion of an ingot. The resistivity varies from 1.5 to 1.9 ohm-cm near the bottom, from 1.4 to 1.7 ohm-cm

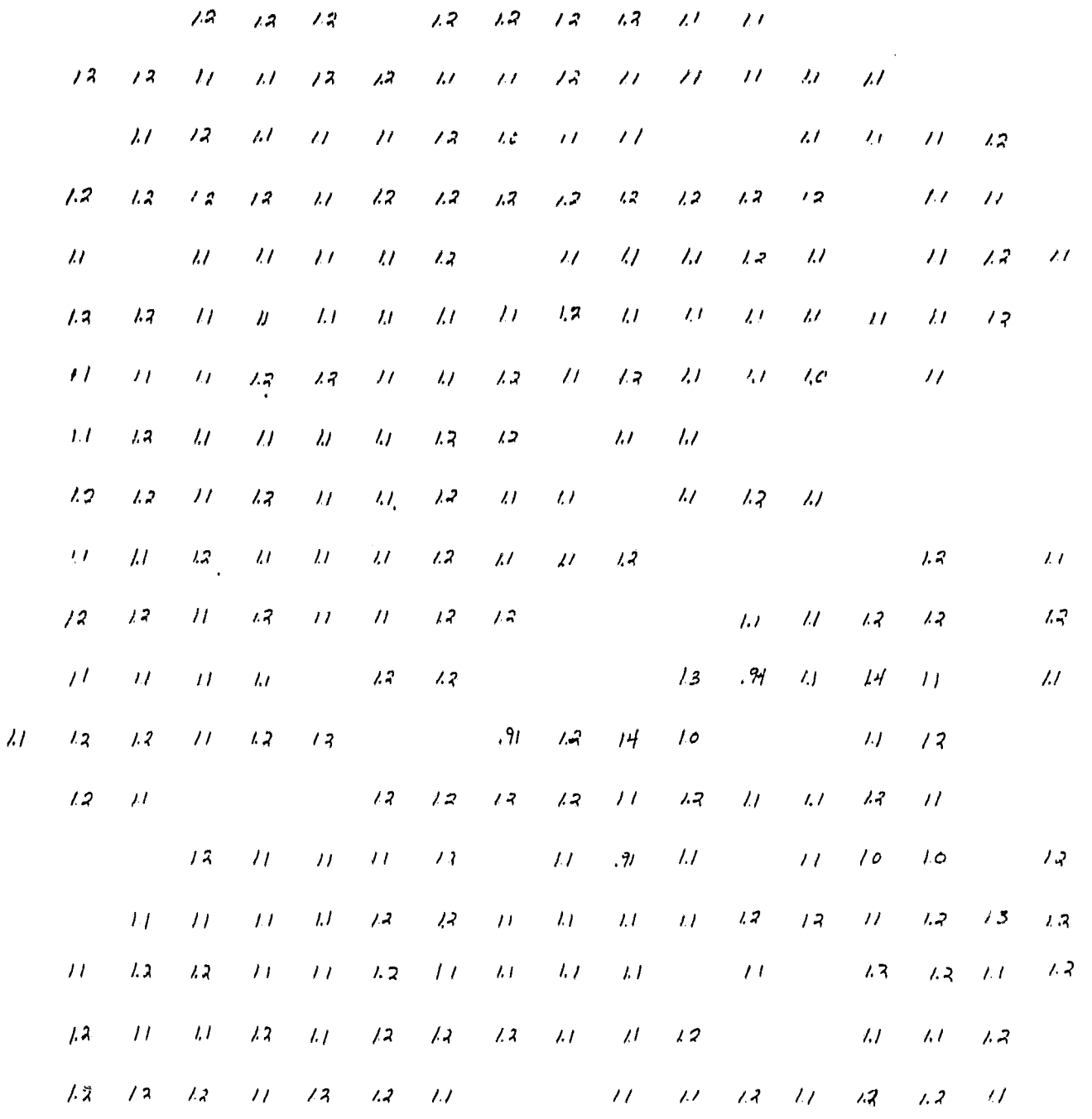

Figure 3. Resistivity (in ohm-cm) as a function of position: single-crystal (control) wafer.

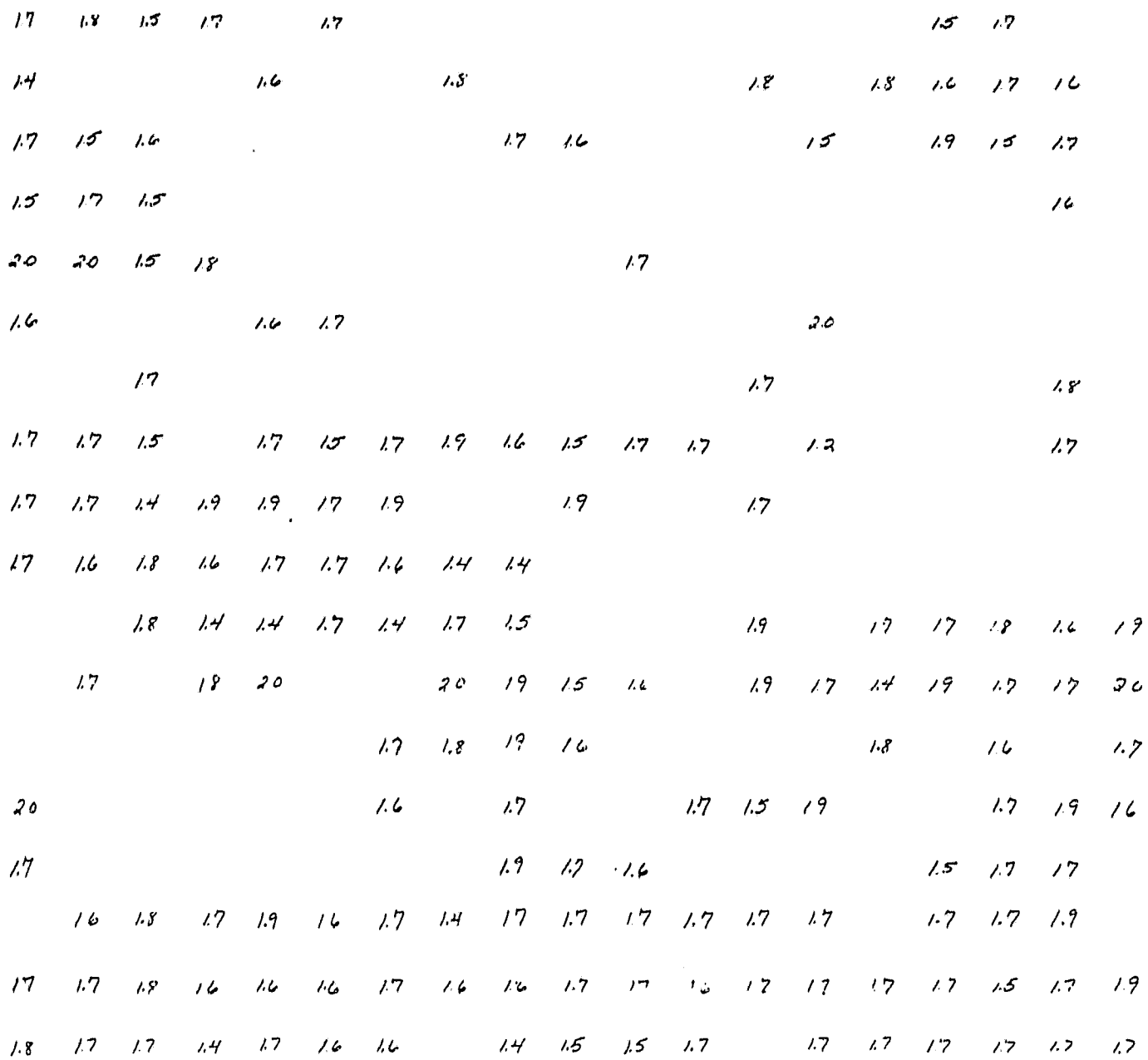

Figure 4. Resistivity (in ohm-cm) as a function of position: bottom wafer from Semix brick no. 71-01E.

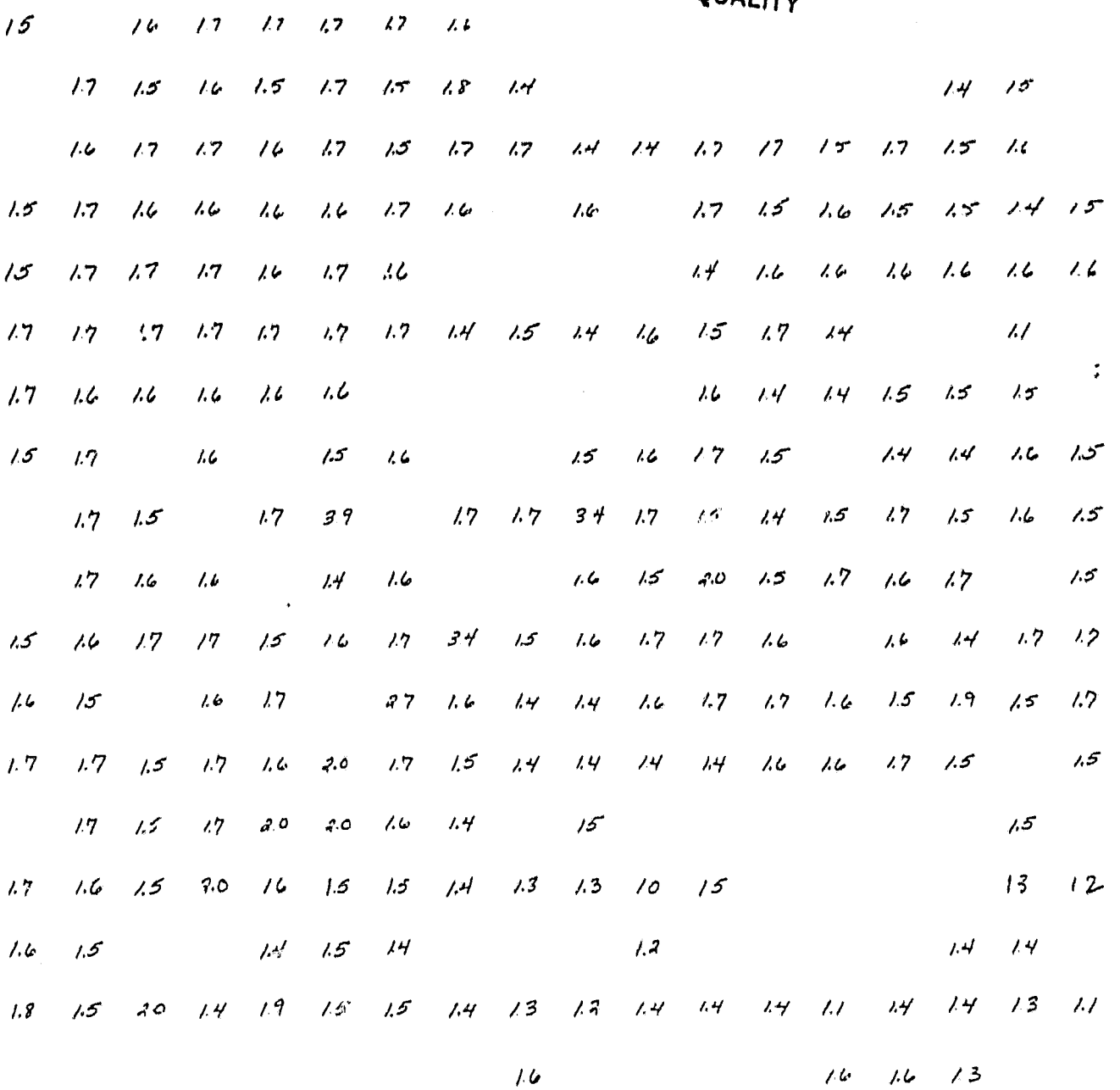

Figure 5. Resistivity (in ohm-cm) as a function of position: middle wafer from Semix brick no. 71-01E.

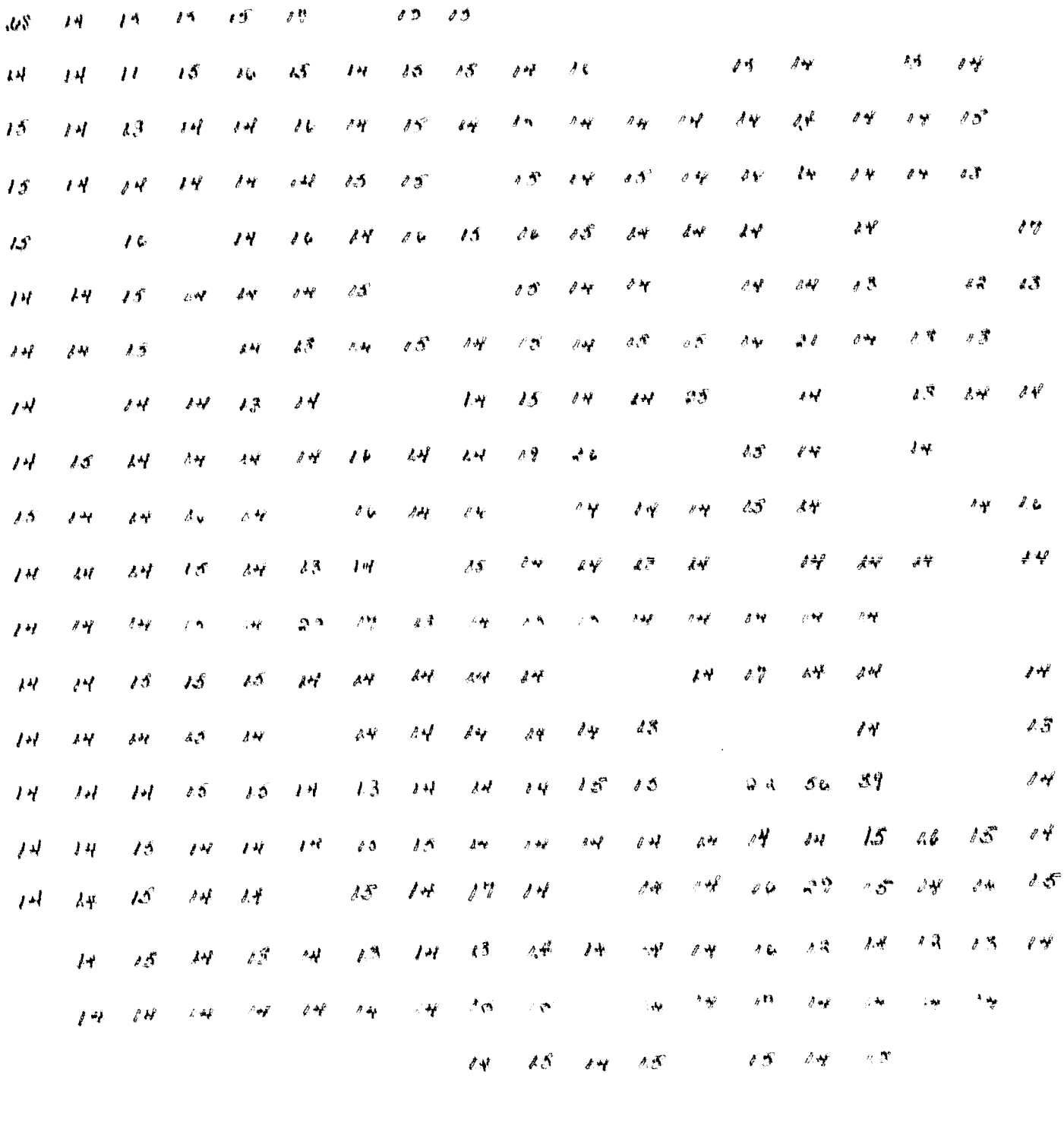

Figure 6. Resistivity (in ohm-cm) as a function of position: top wafer from Semix brick no. 71-01E.

in the middle, and from 1.3 to 1.7 ohm-cm near the top. There is a slight trend toward lower resistivity from bottom to top. There is a much higher incidence of cells with shunt conductances greater than 1 mmho for cells from the bottom than for cells from the middle or from the top. This makes analyzing the spatial variation of resistivity difficult for the wafer near the bottom. However, the resistivity data of the remaining two wafers indicates that there is no particular pattern to the spatial variation of resistivity.

The results for the wafer from the middle of brick C4-108 are shown in Figure 7. Like the bottom of brick 71-01E, this wafer has large areas of cells with shunt conductances greater than 1 mmho; it is not possible to determine the spatial variation of resistivity across this wafer.

In contrast, Figure 8 gives the results for a wafer from the middle of brick C4-116B. Only a very few mini-cells have shunt conductances greater than 1 mmho; the resistivity ranges from 2.0 to about 2.5 ohm-cm, which is fairly uniform. As before, there is no discernable pattern.

Figure 9 shows the results for a Wacker Silso wafer. Only a few cells have shunt conductances which are greater than 1 mmho. The resistivity varied from 1.4 to 1.7 ohm-cm with no pattern.

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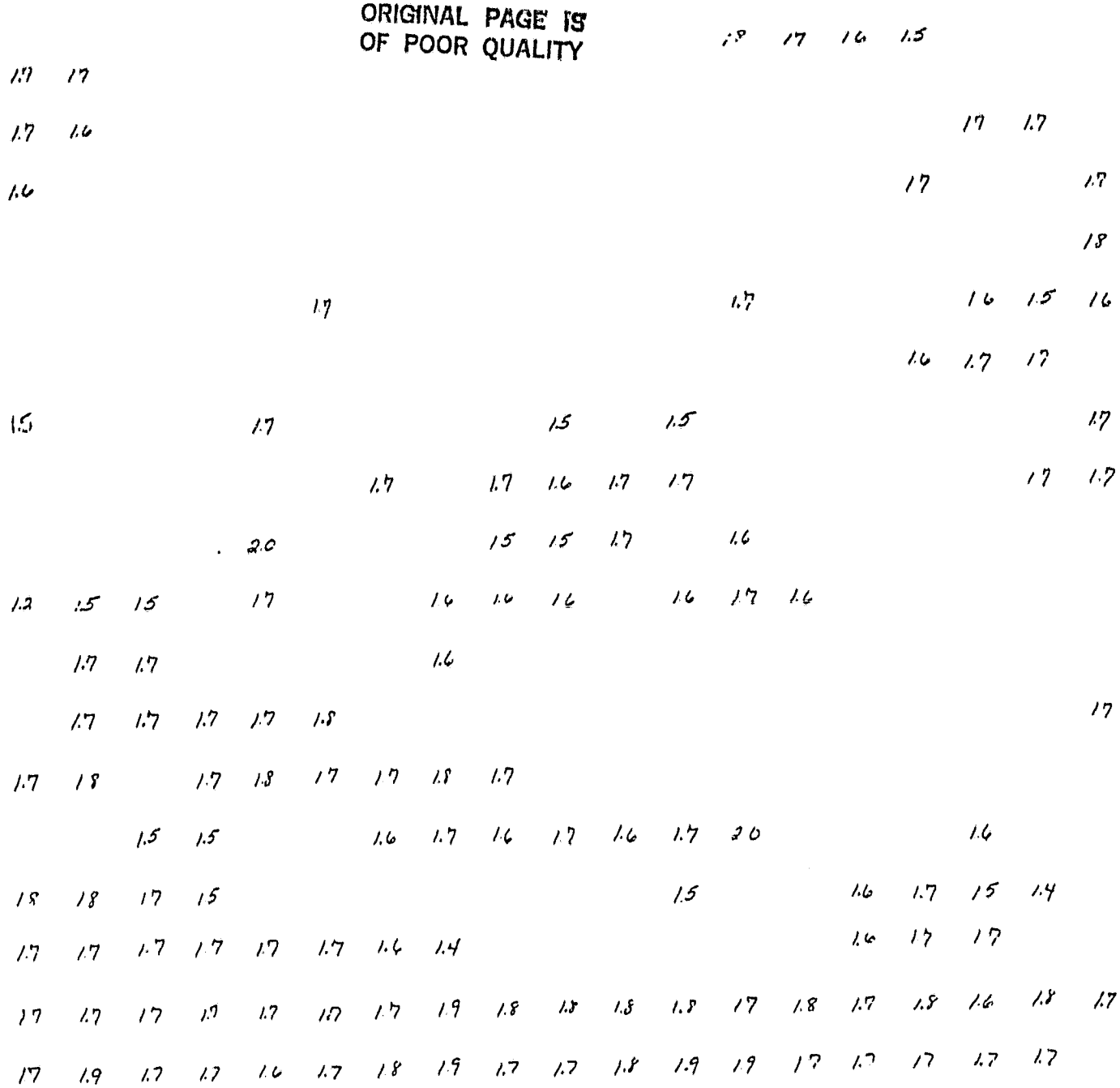

Figure 7. Resistivity (in ohm-cm) as a function of position: middle wafer from Semix brick no. C4-108.

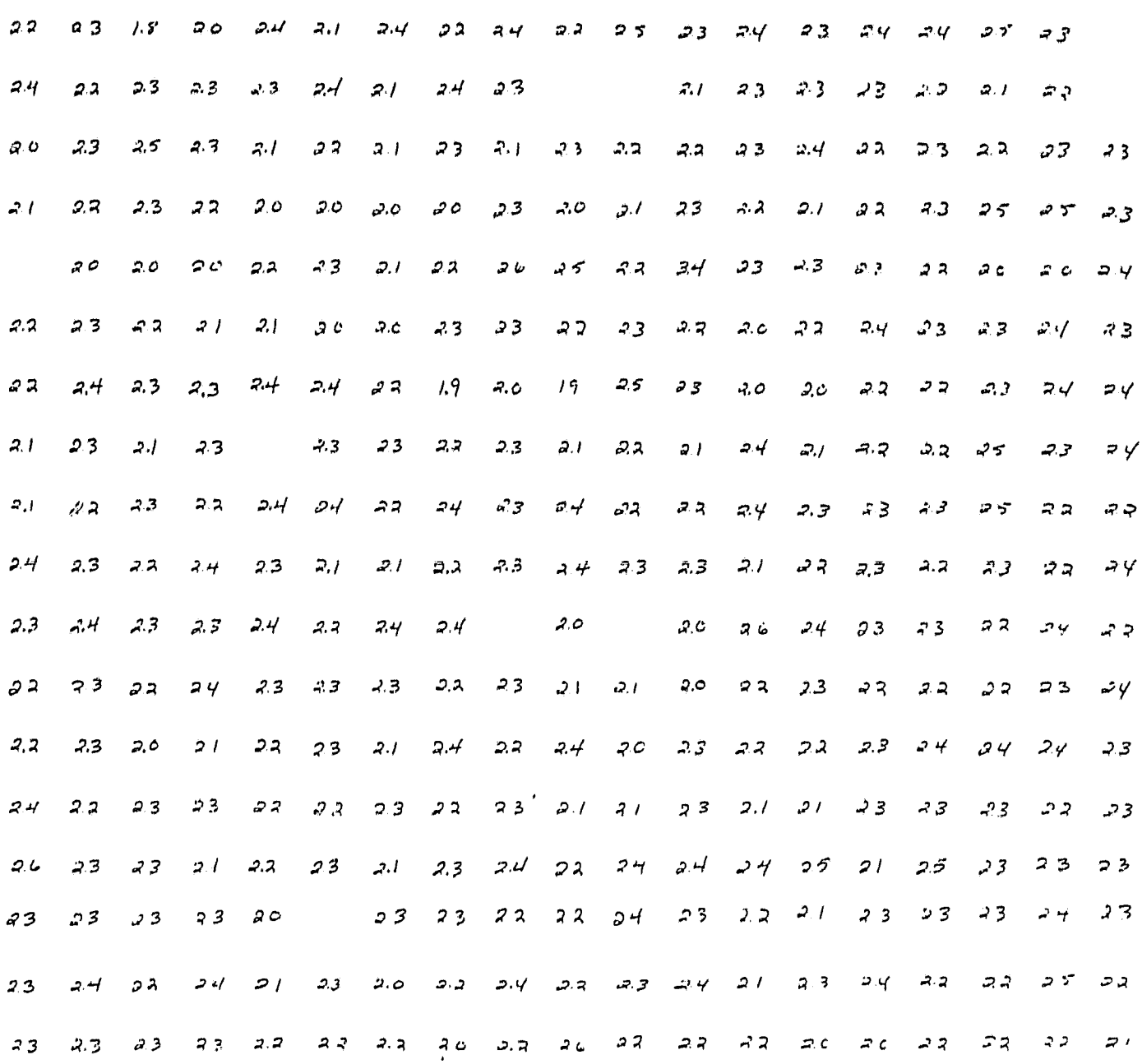

Figure 8. Resistivity (in ohm-cm) as a function of position: middle wafer from Semix brick no. C4-116B.

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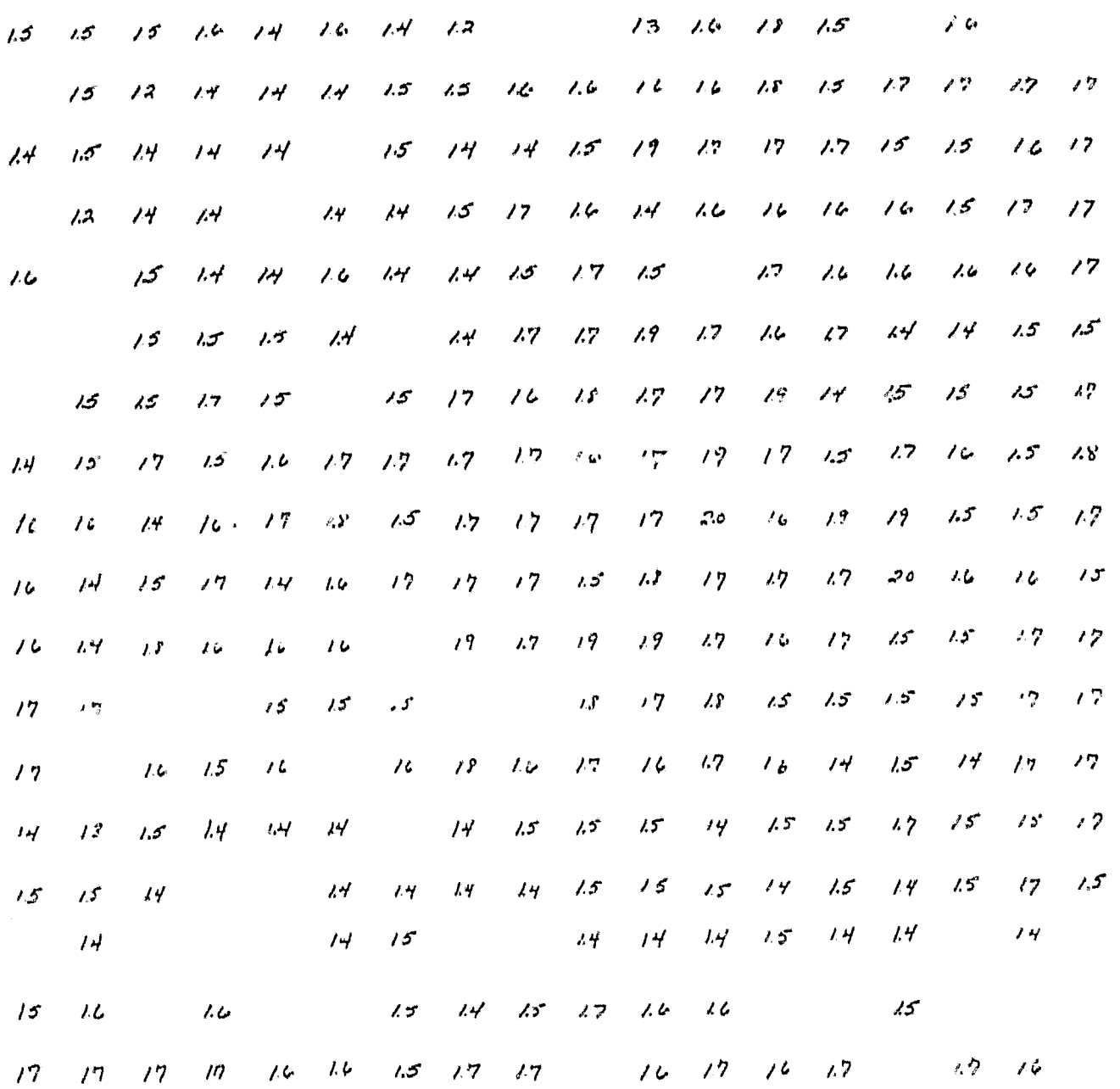

Figure 9. Resistivity (in ohm-cm) as a function of position: Wacker Silso wafer.

In summary, the resistivity of the Semix wafers from brick 71-01E tends to decrease from bottom to top. And there was no significant variation in resistivity across any of these polycrystalline wafers, whether Semix or Wacker.

C. Variation of Shunt Conductance With Position

The second part of the capacitance/conductance measurement, the junction conductance, is helpful in evaluating the validity of all other electrical and electro-optical measurements performed on the cell. The shunt conductance may be a function of the silicon material, it may be related only to processing, or it may be controlled by a combination of both. Therefore, electrical measurements that are intended to characterize the material, such as dark I-V characteristics, quantum yield, and light-spot scanning, must be performed on cells with low values of shunt conductance, to preclude the possibility of characterizing the processing, instead of the material.

The effect of shunt conductance on the current-voltage (I-V) curve of a solar cell that has been modelled by a single ideal diode (exponent n-factor of 1) and no series resistance is shown in Figure 10. Appendix A describes the particulars, but of significance is that the open-circuit voltage and the fill-factor are essentially unaffected by shunt conductances less than 1 mmho/cm^2.

Figure 10. Theoretical solar cell I-V curves as a function of shunt conductance, G_S. $I_o = 5 \times 10^{-5}$ mA/cm^2; $I_L = 25$ mA/cm^2

Maps of low shunt conductance mini-cells (that is, mini-cells whose shunt conductance is less than 1 mmho/cm^2) on each wafer, Figures 11 to 17, were prepared to locate those areas where additional measurements will be assured to electrically characterize the material. Since the junction area of the mini-cells is about 0.2cm^2, only these mini-cells whose shunt conductance is less than 0.2 mmho are included, and these are indicated by the shaded areas. The diagonally-striped mini-cells are incomplete cells, which usually occur along the edge of the wafer.

Figure 11 shows the low shunt conductance areas on the single-crystal control wafer, which was cracked during processing from the bottom left to the top right corner, as shown by the band of shunted cells. Also evident are isolated cells with high shunt conductance, many of which are marginally high. Those between 0.2 and 0.4 mmho are indicated by an asterisk. Those cells with shunt conductances greater than 0.4 mmho may have some process-related impurity penetrating the junction. However, since these cells will be excluded from further electrical measurements, any processing difficulties that did occur do not compromise the intent of this work. The occurrence of high values of shunt conductance in the single-crystal mini-cells do, however, indicate that the high shunt conductance of a polycrystalline mini-cell is not necessarily due to the material. But, the presence of large areas of

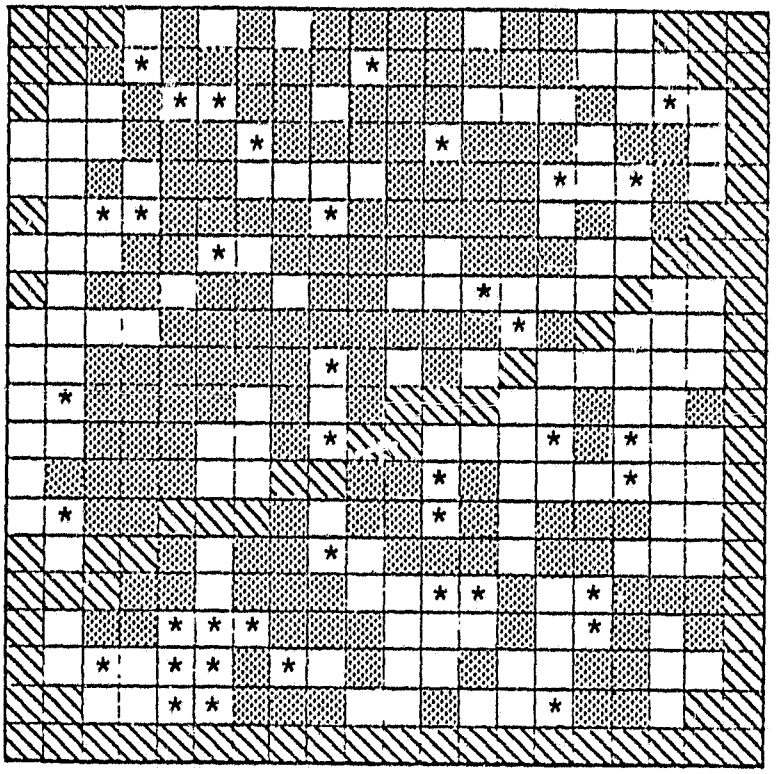

FIGURE 11. Shunt map of single-crystal (control) wafer. Shaded areas indicate shunt conductances less than 1 mmho/cm^2 Cells with asterisks have shunt conductances between 1 and 2 mmho/cm^2. Unshaded cells have shunt conductances greater than 1 mmho/cm^2. Striped cells are incomplete.

contiguous mini-cells with high shunt conductance is probably indicative of a material-related, shunt-causing defect intrinsic to the material.

Figures 12, 13, and 14 show the shunt conductance maps for wafers from near the bottom, in the middle, and near the top, respectively, of brick 71-01E. There are very few mini-cells on the bottom wafer which have values of shunt conductance less than 0.2 mmho; the total number of low conductance (less than 0.2 mmho; that is, 1 mmho/cm^2) mini-cells per wafer increases from bottom to top. The bottom wafer has a low conductance area which is 24 percent of the cells; low conductance cells comprise 39 percent of the middle wafer; and the top wafer contains 66 percent low conductance cells. This result shows that a material from the top of this particular brick yields diffused junctions which have lower values of shunt conductance. These results also indicate that further electrical measurements to characterize this material should be limited to a small area on the bottom wafer, and to several larger areas on the middle wafer; the top wafer has a large number of low shunt conductance cells, and therefore has many large areas of material which can be used for additional electrical measurements.

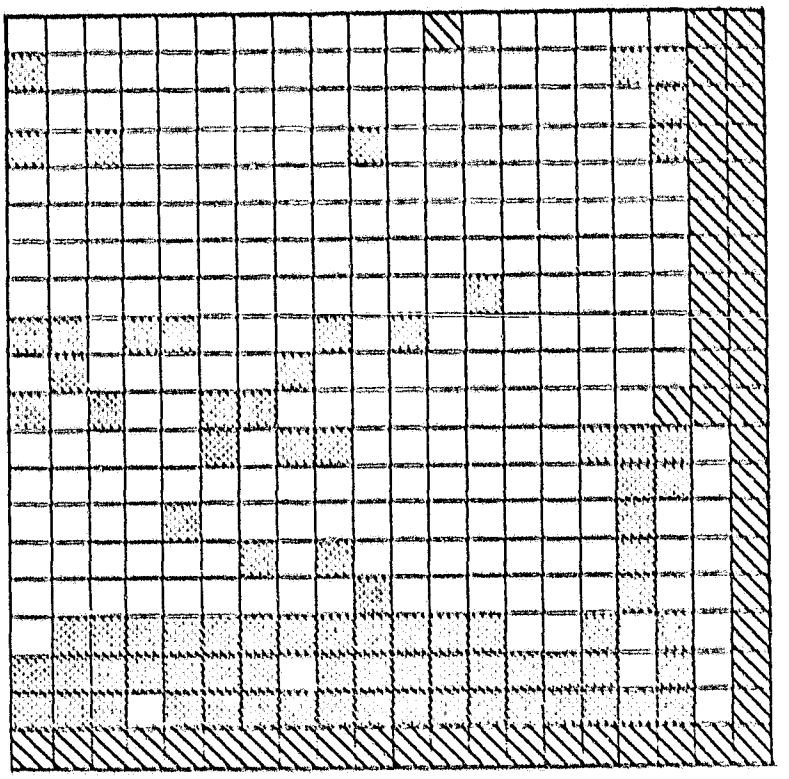

FIGURE 12. Shunt map of bottom wafer from Semix brick 71-01E. Shaded areas indicate shunt conductances less than 1 mmho/cm^2. Unshaded cells have shunt conductances greater than 1 mmho/cm^2. Striped cells are incomplete.

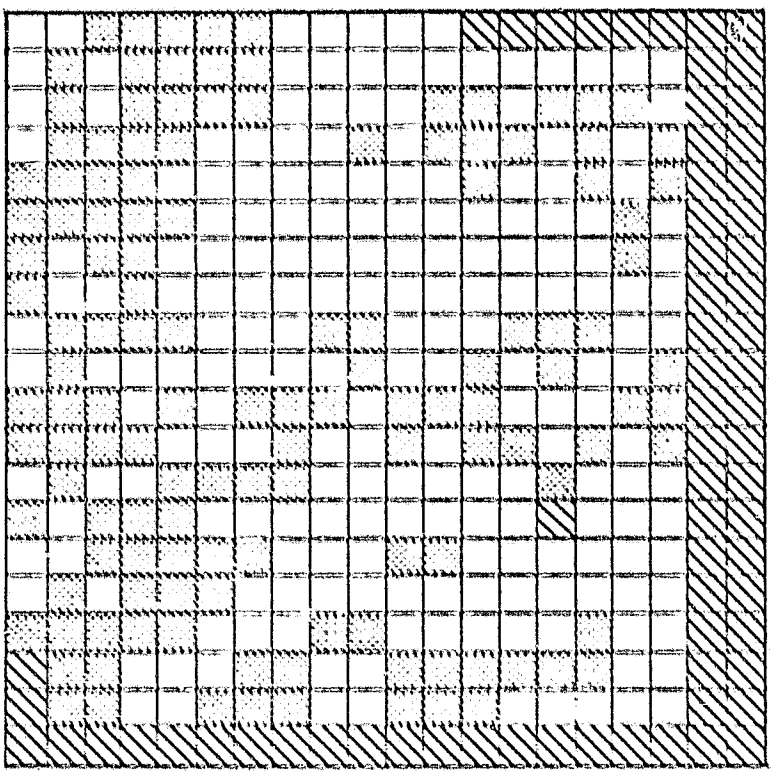

Figure 13. Shunt map of middle wafer from Semix brick 71-01E.

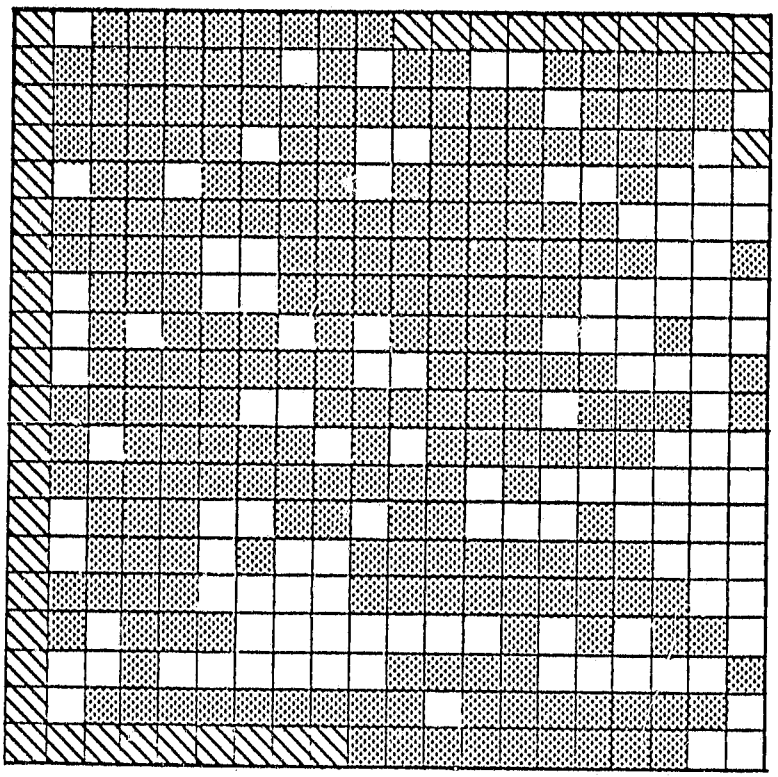

Figure 14. Shunt map of top wafer from Semix brick 71-01E.

Figure 15 shows a similar map for the wafer from brick C4-108. There are only a few cells with values of shunt conductance less than 0.2 mmho. Figure 16 shows the map for the wafer from brick C4-116, which has many large areas of low shunt conductance cells, about 64 percent of the mini-cells.

The shunt conductance map for the Wacker Silso wafer is shown in Figure 17. About 45 percent of the mini-cells have low shunt conductance, and they are located in several scattered areas.

Additional electrical measurements can be made on the Wacker wafer and the wafer from brick C4-116; it will be more difficult to make meaningful electrical measurements on the wafer from brick C4-108.

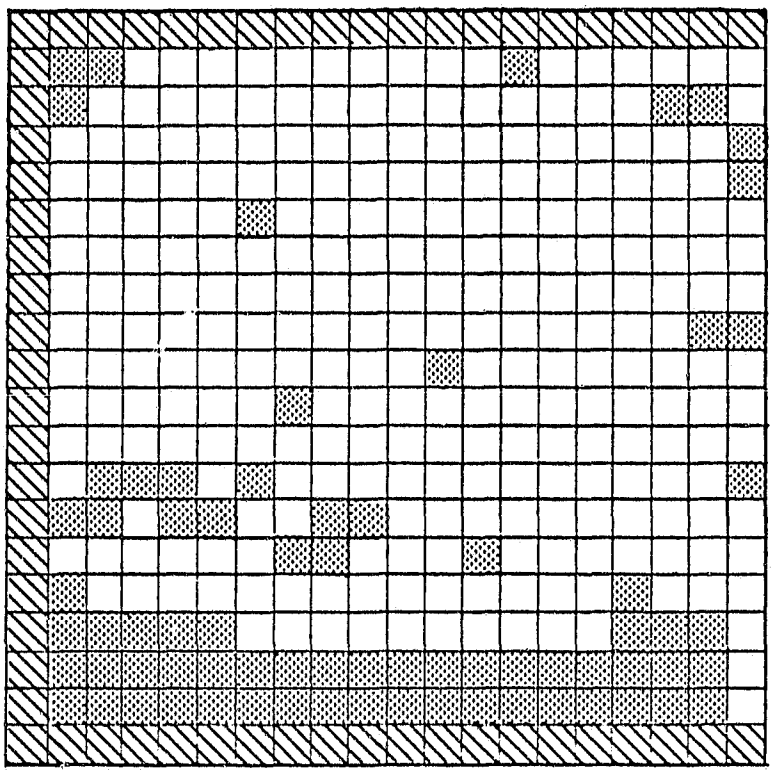

Figure 15. Shunt map of middle wafer from Semix brick C4-108.

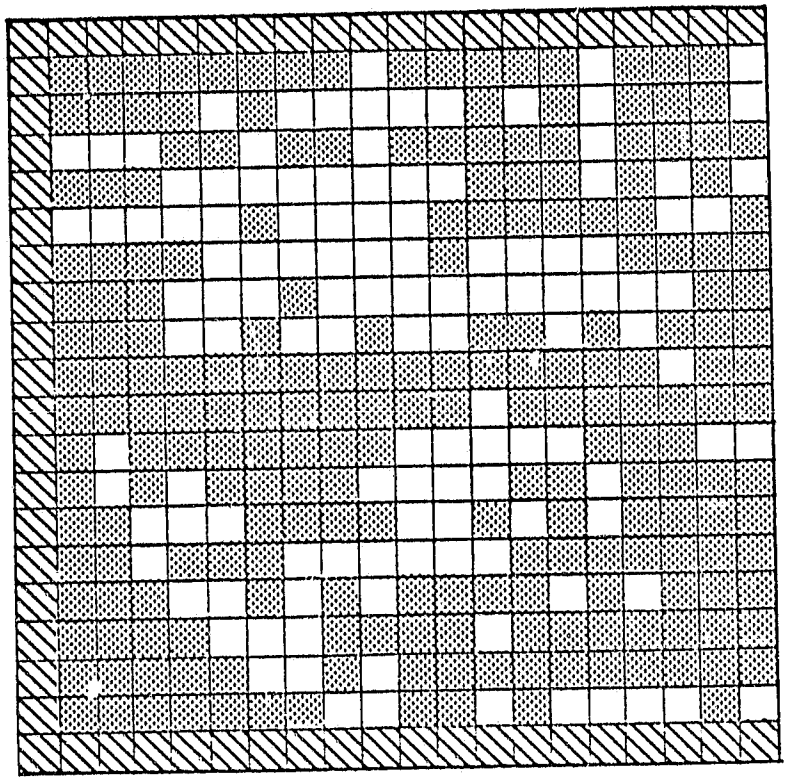

Figure 16. Shunt map of middle wafer from Semix brick C4-116B.

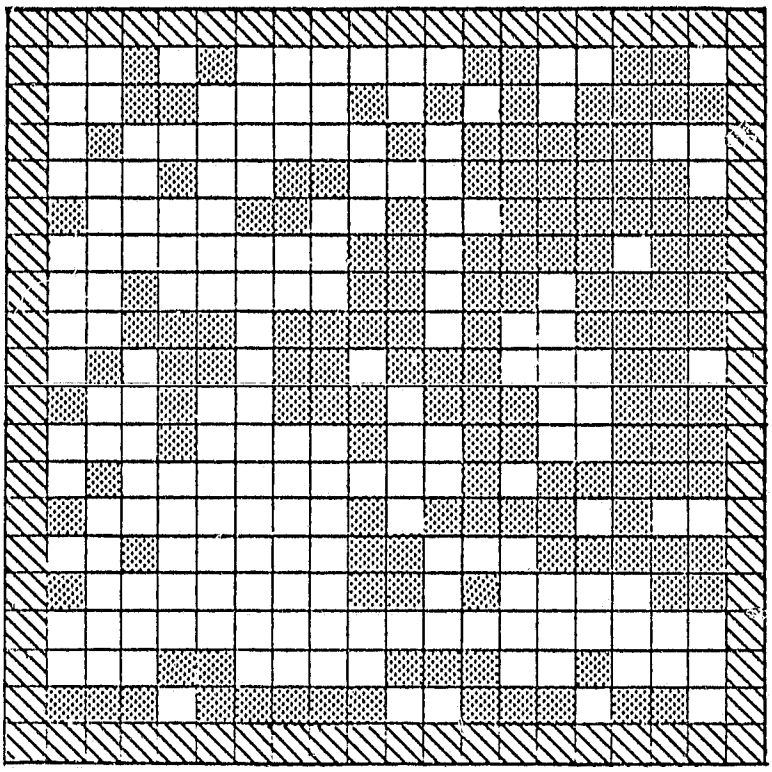

Figure 17. Shunt map of Wacker Silso wafer.

III. PROCESSES TO IMPROVE THE PERFORMANCE OF POLYCRYSTALLINE SILICON SOLAR CELLS - DAMAGE GETTERING

Results from the thickness-resistivity matrix indicated that the short-circuit current of the thicker polycrystalline cells is consistently five to ten percent lower than that of the cells fabricated from Czochralski single-crystal silicon that were used as controls for this experiment. In looking at the effect of thickness on cell I-V characteristics, the short-circuit current of the polycrystalline cells was found to saturate at a thickness that was less than that of the single-crystal (control) cells. The short-circuit current of the 1 to 2 ohm-cm polycrystalline cells saturated at a thickness of about 100 microns; the short-circuit current of the 1.7 ohm-cm single-crystal (control) cells saturated at a thickness of 150 microns. All of these results indicate that the polycrystalline silicon is presently characterized by a minority carrier diffusion length that is shorter than that of Czochralski single-crystal silicon.

The cause of the shorter minority carrier diffusion lengths in polycrystalline silicon has not been unequivocably identified, but one possibility is that this degradation is due to a minority-carrier lifetime-killing impurity. It may be possible, if this indeed is the case, to improve the short-circuit current of polycrystalline cells by removing some of

this impurity. This type of improvement has been observed for the case of metallurgical grade silicon upon annealing wafers at a temperature high enough to allow the degrading impurities to diffuse to a surface with a high dislocation density. The procedure, called damage gettering, was reported by Saitoh, et.al. [4], to result in a minority carrier diffusion length increase from 11 microns to 16 microns in twice-pulled Czochralski single-crystal wafers that had metallurgical grade silicon as the starting material.

An experiment to investigate the usefulness of damage gettering to improve the short-circuit current of cast polycrystalline silicon was designed and begun. For this experiment, a number of closely-matched 10cm x 10cm polycrystalline silicon wafers were etched using a CP-type etch to thicknesses of 200, 250, 300, and 350 microns, then quartered. Damage to one side of each 5cm x 5cm quarter wafer was introduced by sand-blasting with 320 mesh aluminum oxide particles for 30 seconds.

One quarter wafer of each thickness will be annealed in flowing dry nitrogen at 1000°C for 0, 1, 5 and 25 hours. A 5cm x 5cm single-crystal Czochralski control wafer is being co-processed with each polycrystalline quarter wafer in order to monitor the processing.

After annealing, the wafers will be etched in a CP-type etch to remove the surface damage, then prepared for measurement of "photoconductive decay time" using the microwave photoconductivity decay technique [5]. This measurement should provide an early indication of any major change in bulk properties. All wafers will then be fabricated into 2cm x 2cm solar cells using a high-efficiency process [6] in order to characterize the effect of the damage gettering on both the light and dark I-V characteristics.

IV. CONCLUSIONS

Analysis of the results of the thickness-resistivity matrix that was fabricated during the first three quarters of this program indicated that the open-circuit voltage and the fill-factor of the $4cm^2$ solar cells fabricated from large-grain (greater than 1-2 mm diameter) polycrystalline silicon) had substantial amounts of scatter which were not related to the main experimental variables - thickness and bulk resistivity. The scatter in the values of open-circuit voltage and fill-factor implies that there is an additional performance-limiting mechanism which may not be strongly associated with bulk properties. The degradation of these parameters appears to have a spatial nature and may be related to the grain structure since the grain boundary content of any particular cell on a wafer was not controlled.

Therefore, an additional experiment which consists of fabricating and testing an array of small photodiodes across a 10cm x 10cm wafer was designed to determine, first, the location of cells with degraded I-V parameters, and, second, the fundamental cause of the degradation. The work this quarter consisted of fabricating a selection of polycrystalline silicon wafers, both Semix UCP and Wacker Silso, into mini-cell wafers using a mesa structure for diode-to-diode isolation.

Junction capacitance and shunt conductance measurements on all mini-cell wafers were completed. The junction capacitance was used to evaluate the variation of the resistivity with position across the wafers. There was no significant variation in resistivity across any polycrystalline wafer, whether Semix or Wacker. The measured values of shunt conductance were used to locate areas on each wafer where the performance of the mini-cells is not affected by the presence of any resistive shunt, which might be associated with a defect introduced by processing. Each wafer has areas of contiguous mini-cells in which the values of shunt conductance are less than the value that would affect the open-circuit voltage or the fill-factor. However, the amount and the location of these "low-conductance" areas varies from wafer-to-wafer, and with position in the brick. For a particular brick analyzed, Semix No. 71-01E, the total number of low conductance cells increased from bottom to top.

The results of the thickness-resistivity matrix also indicated that the light-generated current in large-grain polycrystalline silicon is dominated by recombination of photogenerated minority carriers in the bulk, as opposed to recombination at the grain boundaries. Hence, improvements in the short-circuit current of solar cells fabricated from large-grain polycrystalline silicon will follow if the sources of recombination in the bulk are eliminated.

An effort was begun to investigate whether a damage gettering process can be used to reduce the sources of recombination in the bulk, improve the minority carrier diffusion length, and increase the short-circuit current. A number of polycrystalline wafers will be annealed at 1000°C for 1, 5, and 25 hours. These heat-treated wafers will be analyzed and fabricated into 2cm x 2cm solar cells during the next quarter, and compared to cells fabricated on un-annealed wafers.

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APPENDIX A

THEORETICAL ANALYSIS OF THE EFFECT OF SHUNT CONDUCTANCE ON SOLAR CELL OUTPUT POWER

THEORETICAL ANALYSIS OF THE EFFECT OF SHUNT CONDUCTANCE ON SOLAR CELL OUTPUT POWER

The simplest solar cell equation, excluding the effects of series resistance and shunt conductance, is given by the expression:

$$I = I_o [\exp(V/\beta) - 1] - I_L \qquad (1)$$

where I is the output current of the cell, I_o is the reverse saturation current, β is a constant which at room temperature is approximately equal to 26 mV, V is the output voltage, and I_L is the light-generated current. Though simple in form, this equation is generally adequate to describe the current-voltage (I-V) curve of most silicon solar cells, whether single crystal or polycrystalline. The effect of a shunt conductance may be included by modifying Equation (1) to:

$$I = I_o [\exp (V/\beta) - 1] - I_L + VG_s \qquad (2)$$

where G_s is the shunt conductance. The additional term, VG_s, will act to reduce the output current at a given voltage since the sign of I_L and the sign of VG_s are opposite. The reduction in output current increases as either the value of the shunt conductance or the voltage increases. Hence the characteristic shape of the I-V curve of a shunted solar cell is a sloped, rather than flat, line near the short-circuit current point.

In order to get an appreciation of the effect of shunt conductance on a solar cell I-V curve, Equation 2 was used to generate a series of I-V curves, shown in Figure 1, for various values of shunt conductance, all other parameters being constant. The light-generated current, I_L, for a typical $100cm^2$ semicrystalline silicon solar cell with nickel-solder metallization is 2.5A; the value of I_o was chosen to be 5×10^{-10}A. Values of shunt conductance were chosen to be 0.0, 0.1, 0.2, 0.5, and 1.0 mho.

It is clear, from looking at the curves in Figure 1, that the output power of the cell is dependent on the value of the shunt conductance. In fact, the decrease in output power is roughly proportional to the shunt conductance; a shunt conductance of 0.2 mho will result in a power loss of approximately four percent while a shunt conductance of 0.5 mho increases the power loss to approximately eleven percent. However, a shunt conductance of less than 0.1 mho (equivalent to a shunt resistance of 10 ohms and greater) will account for at most a loss of three percent of the maximum theoretically possible output power. For shunt conductances less than 0.1 mho on a $100cm^2$ solar cell, very little power is lost through the shunt; therefore, very little is gained in output power by decreasing the shunt conductance below 0.1 mho for a $100cm^2$ cell.

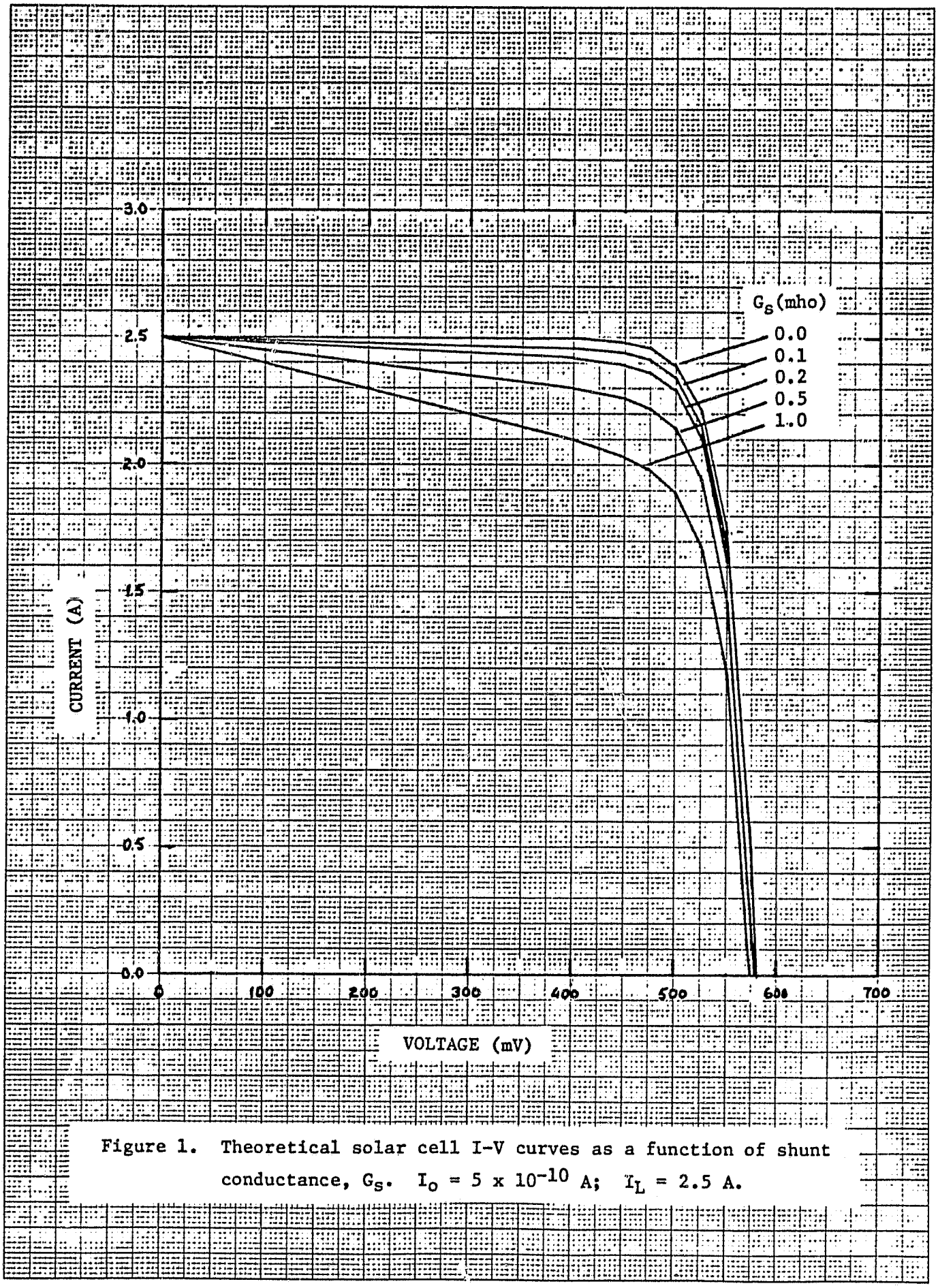

Figure 1. Theoretical solar cell I-V curves as a function of shunt conductance, G_S. $I_o = 5 \times 10^{-10}$ A; $I_L = 2.5$ A.