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SPACECRAFT IF SWITCH MATRIX FOR WIDEBAND SERVICE APPLICATIONS IN 30/20 GHz COMMUNICATION SATELLITE SYSTEMS EXECUTIVE SUMMARY/FINAL REPORT

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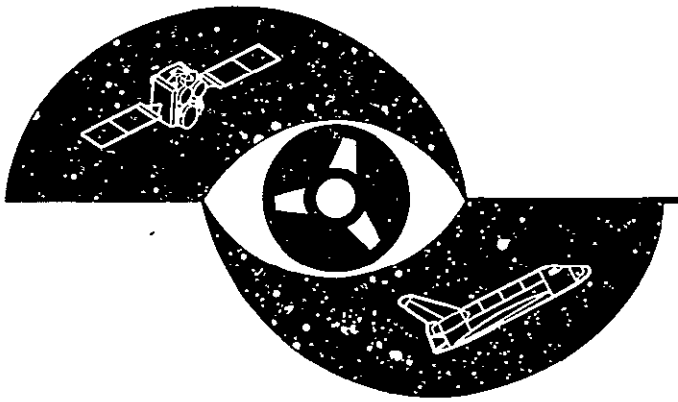

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16 Abstract

This report describes the design and fabrication of a 20 x 20 Satellite Switched - Time Division Multiple Access (SS-TDMA) IF Switch Matrix for application in a 30/20 GHz Communications Satellite. Development of this 3-8 GHz switch matrix was sponsored by NASA Lewis Research Center as a part of their Advanced Communications Satellite Technology Program. The switch matrix was one of several key technologies requiring development to realize wideband, high capacity satellite communications systems for the 1990's.

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SECTION 1

SUMMARY

This report describes the design and fabrication of a 20 x 20 Satellite Switched - Time Division Multiple Access (SS-TDMA) IF Switch Matrix for application in a 30/20 GHz Communications Satellite. Development of this 3-8 GHz switch matrix utilizing available technology was sponsored by NASA Lewis Research Center as a part of their Advanced Communications Satellite Technology Program. The switch matrix was one of several key technologies requiring development to realize wideband, high capacity satellite communications systems for the 1990's.

An assessment in 1980 of switch architecture concluded that the coupled crossbar switch matrix, designed with Gallium Arsenide FET (GaAs FET) devices for microwave switching, and with high-speed CMOS LSI logic, for switch crosspoint addressing, were the optimum available technologies for satellite communications switching by 1982. The major decision factors in this assessment were bandwidth, switching speed, off-state isolation, and reliability over a ten-year mission life. Following breadboard work, a Proof-Of-Concept (POC) Model was fabricated and tested, to prove feasibility of the concept.

A conceptual design study was also completed for a wideband, 100 x 100 switch matrix using forecasted 1987 technology. The study resulted in a switch matrix design concept utilizing a coupled crossbar architecture implemented with Monolithic Microwave Integrated Circuits (MMIC). The design consists of a basic building block MMIC, permitting flexible growth, and efficient wraparound redundancy to increase reliability.

SECTION 2

INTRODUCTION

The Switch Matrix Program was subdivided into major tasks. Task I developed a conceptual design of a 20 x 20 Switch Matrix utilizing 1982 technology, whereby Task II pursued a conceptual design of a 100 x 100 Switch Matrix based on projected 1987 Technology.

The Task I effort began with an assessment of available 1982 technologies. Architectures were evaluated considering design goal requirements, size, weight, redundancy, and expandable of design to matrices of N x N sizes other than 20 x 20. Available microwave switching devices were categorized to switching speed, gain bandwidth product, switching power, and off-state isolation. Control logic devices were evaluated for switching speed and low power dissipation.

An Architecture and Switch Device trade-off was then completed from the findings of the assessment study. The coupled crossbar design was the selected architecture because it offered immunity to single point failures by the use of couplers that isolate the switching devices from the main input and output transmission lines. Redundancy to achieve a desired switch matrix reliability is readily implemented into the coupled crossbar design.

The Gallium Arsenide FET (GaAs FET) was the selected device for microwave switching. The GaAs FET provides high speed switching, low power switching drive signals, gain, wide bandwidth, and good off-state isolation. For the logic control circuits, custom designed CMOS LSI devices were selected as the desired technology. It offers high speed switching, low power dissipation, high reliability, and high density packaging.

A parametric trade-off study was then undertaken to develop the concepts of the first two studies. An in-depth analysis of the selected architecture indicated the flexibility and expandability of the row and column channel packaging concept. Redundant channel modules could readily be provided to improve reliability of the switch matrix with the design approach. This concept appeared to be feasible for large (20 x 20) switch matrices as well as small (3 x 3) matrices. Packaged GaAs FETs were selected mainly to eliminate hermetic sealing of the row and column channels.

Sample GaAs FET devices were obtained from various suppliers and were tested and evaluated for use in the switch matrix design. Dexcel supplied the best devices to meet the switch matrix requirements at that period of time. However, future surveillance of device suppliers should be maintained, because much research is being pursued in the manufacturing of high speed, low power GaAs FET devices.

A conceptual design of a 20 x 20 Switch Matrix was then completed using the previous studies as a basis of the design. Reliability analysis (Task VIII) of the design indicated that five wraparounds would be a conservative estimate in order to have all input and outputs operating over the duration of a ten year mission.

Reliability analysis also concluded that a 32 bit address code for the logic control functions provided an optimum reliability figure. A scheme was developed to update three switch matrix crosspoints with one 32 bit code. To update the full 20 x 20 matrix including five wraparounds, nine data transfers of the 32 bit code would be required. Matrices of smaller size would require less than nine data transfers. The control logic design included an approach for LSI implementation.

As a result of the 1982 technology study, a 5 x 5 Breadboard Switch Matrix (Task III) was fabricated and tested. The matrix was the mechanical size of a 5 x 5; however, to prove feasibility of the conceptual design while minimizing costs, only nine of the possible twenty-five crosspoints were populated. The average switch crosspoint bandwidth measured 2.0 GHz and switching speed measured 12 nsecs. The problems experienced were an out of spec input and output mainline VSWR, and an average switch crosspoint insertion loss of 17 db versus the design goal of 15 db. Off-state isolation, a major concern during the study phase, was found not to be a problem. In general, the breadboard results indicated that the conceptual switch matrix design was feasible.

A proof-Of-Concept (POC) Model design (Task V) was next to be completed. Based on the breadboard test results, a gain bandwidth trade-off was made to permit meeting the design goal requirements of 1 GHz minimum bandwidth and 15 db minimum insertion loss. A solution was also incorporated to eliminate the VSWR problem. The POC model was designed as a 20 x 20 matrix with one wraparound; however, sixty-one carefully selected switch crosspoints (including the wraparound) rather than four hundred and forty were populated in order to reduce cost but prove feasibility of the design. Due to cost and schedule limitations the control logic design was implemented by discrete devices rather than the recommended CMOS LSI approach.

Special Test Equipment was designed to simulate an on-board spacecraft computer. The Special Test Set provides a 32 bit digital code sent to either a manual or automatic mode to the Switch Matrix. The 32 bit code provides crosspoint (row, column) addressing information. Used with an external word generator, the test set operating in the automatic mode can accommodate sixteen different switch matrix configurations and provide a variable routing sequence that would closely simulate a SS-TDMA system. Operating DC voltages for the Switch Matrix are also provided by the test equipment.

During Task VI, the POC model and Special Test Equipment were fabricated. Expandability of the POC model design was proven by going from the 5 x 5 breadboard model to the 20 x 20 POC model. Test fixtures were also designed and fabricated to tune and test the microwave switch crosspoints.

Testing and data analysis of the POC model took place during Task VII. Most of the microwave measurements were made using a Hewlett Packard Automatic Network Analyzer. Noise figure, intermod distortion, and switching speed measurements were accomplished with manually operated test equipment. The switch matrix was tested in accordance to the POC Top Level TEst Plan developed during Task IV. A statistical analysis of the data was completed and has provided confidence, tolerance, and prediction limits of all the measured parameters in order to evaluate what the POC model performance would be if all four hundred and forty switch crosspoints had been fabricated. A detailed analysis of the POC model test results will be found in a subsequent section of this report.

Task II studies of a 100 x 100 switch matrix utilizing projected 1987 technologies, evaluated a conceptual design of an IF Switch Matrix for operation in the 3.0 - 8.0 GHz frequency band, and a second conceptual design of a switch matrix operating at Baseband. Both studies followed the same format of first evaluating projected Architectures and Switch Devices for 1987 implementation, followed by a detailed parametric tradeoff analysis. In both cases, the partitioned coupled crossbar matrix was selected as the most desirable architecture. For the IF design an MSI GaAs MESFET was the selected device technology. The microwave switch elements and control logic elements would be integrated into a subassembly matrix (typically 12 x 12) fabricated with Monolithic Microwave Integrated Circuits (MMIC) using the GaAs MESFET technology. The baseband design would be similar except that CMOS/SOS would be used for the integrated switching and control logic elements. A Final Design Concept was then completed for the IF and Baseband Switch Matrices.

A Switch Matrix comparison was then completed. The first comparison evaluated the 100 x 100 IF Switch Matrix to the 100 x 100 Baseband Switch Matrix. Comparisons were made in terms of functional performance, scaleability, reliability, weight, volume, power consumption, and projected costs. The baseband switch included modems required for IF/baseband translation. The IF Switch Matrix design was selected as the most desirable approach. A second comparison was then completed between the 1987 100 x 100 IF Switch Matrix design to a scaled up version of the 1982 20 x 20 IF Switch Matrix design. A 1982 discrete component 100 x 100 Switch Matrix was rejected for large scale switching due to the extreme weight and size penalty versus the smaller 1987 MMIC design. A conclusion of the Task II study was that future large scale switching would be most feasible at microwave IF frequencies, implemented with GaAs MMIC Technology.

SECTION 3

1982 20 x 20 IF SWITCH MATRIX

The purpose of the IF Switch Matrix Design subtask is to complete the conceptual design of a 20 x 20 SS-TDMA IF Switch Matrix. The design to be presented is based on the results of studies that included a technology assessment, architecture and switch device trade-off, and parametric trade-off analyses. The concepts incorporated in the design utilize 1982 technologies.

3.1 IF SWITCH DESIGN

The general concept of the coupled crossbar is shown in Figure 3.1 and crosspoint design is given in more detail in Figure 3.2. A two stage switching amplifier is loosely coupled to the input and output lines. The loose coupling will maintain the input and output VSWR's within specification. For the 15 dB coupler used in this design as many as 20 perfect shorts can be tolerated on any coupled line without exceeding the specification of a 1.2:1 VSWR. The quarter wave directional couplers are centered at the upper end of the 2.5 GHz (i.e., $\lambda/4$ @ 7.5 GHz) bandwidth so that the low frequency rolloff of the couplers will compensate in part for the 2 stage FET amplifier rolloff. Each coupler will contribute slightly more than 1 dB of rolloff compensation over the 5-7.5 GHz band.

In order to meet the insertion loss requirements of 15 dB maximum, a two stage dual gate GaAs FET switching amplifier is employed. The predicted performance from the preliminary modeling of the dual gate FET indicates that the forward gain will be at least 20 dB over the 5-7.5 GHz band with more than 40 dB of "OFF" state isolation. The input and output matching circuits reduce the VSWR and enable the amplifier to provide the required gain. The interstage matching network has the added requirement of providing most of the amplifier rolloff compensation. Incorporated into the interstage design is the mechanical interconnect which must have low insertion loss and VSWR and high isolation from crosstalk in order for the total crosspoint to meet the overall switch matrix requirements. The GaAs FET will require gate voltage levels of 0 and -4 volts for ON/OFF switching which are provided by the logic driver circuitry.

The controlled gates are commanded to an amplifier "ON" state when the crosspoint is activated. The two stages are operated in the pinched off state when the subject input/output path is to remain in the "OFF" state. Figure 3.2 indicates the signal flow through crosspoint. The logic commands are separately decoded to each amplifier stage in a redundant scheme, to reduce the probability of an uncommanded crosspoint closure.

The switch circuit is comprised of lumped constant elements and transmission line elements implemented on 0.025" thick Alumina substrates. The microstrip circuit topology is etched to form gold conductor patterns, arranged to provide component elements which form matching networks for the switching devices. The switching devices are packaged dual-gate GaAs FET's biased to provide acceptable gain in the "ON" state. The circuit topology and switching device were selected

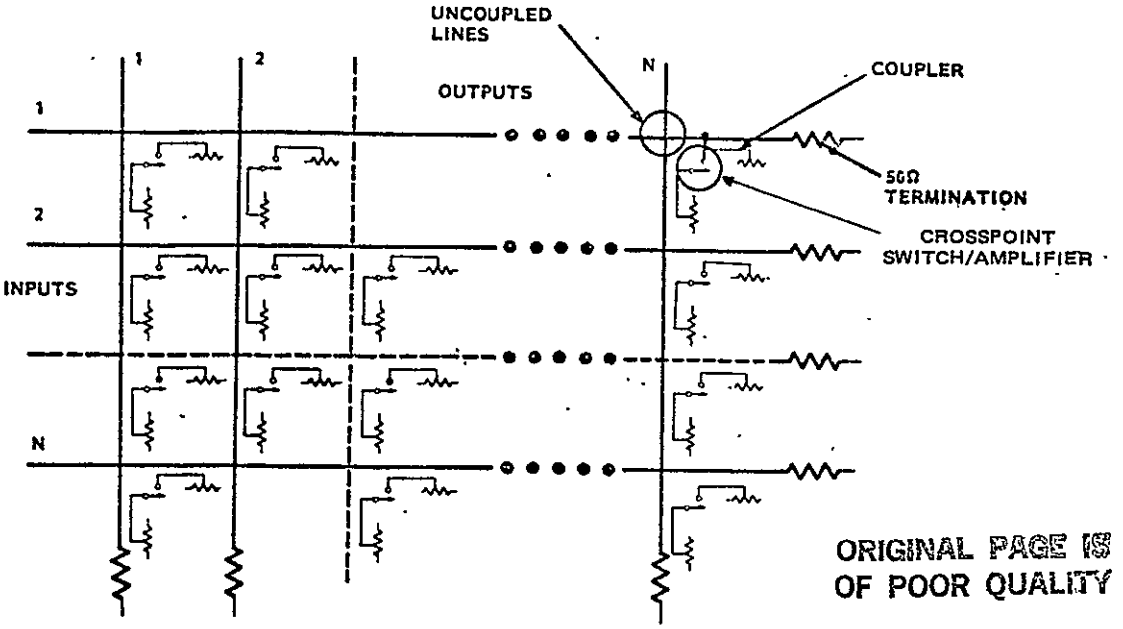


Figure 3.1. Coupled Crossbar Switch Matrix Concept

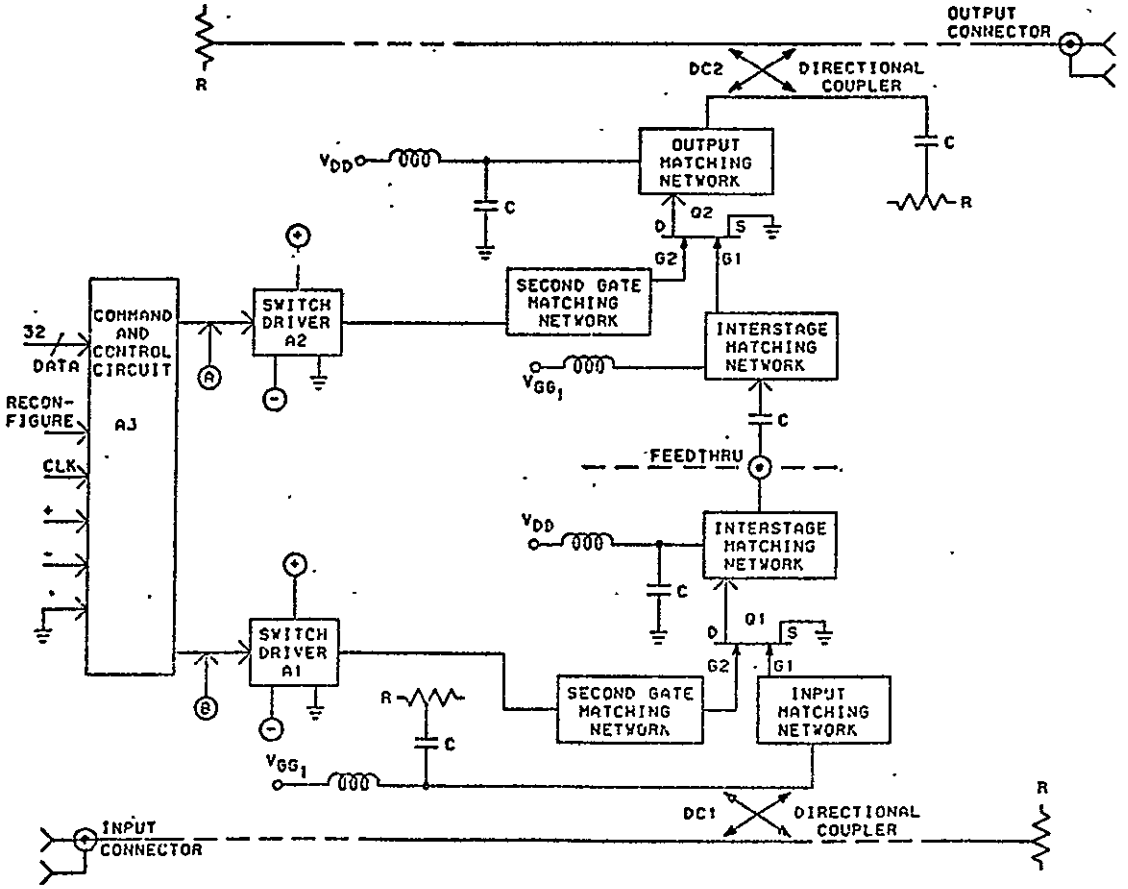


Figure 3.2. Crosspoint Switch/Amplifier Block Diagram

to provide gain of 15 dB in the ON state and isolation approaching 60 dB in the OFF state. The division of the switch circuit into two separate modules located on opposite sides of an interface mounting plate is an important feature in attaining the high isolation "OFF" state performance.

The interface between input and output modules of a crosspoint is made through a connector insert in each module. The actual connection occurs within the mounting plate; the outer conductor by resilient conductive contacts and the center conductors via a male-to-male pin.

The directional coupler was chosen as the circuit element to provide immunity to single point failure of a crosspoint. The coupling value designated to be 15 dB is dependent upon the level of gain achieved over the specified bandwidth, using two amplifier stages. This selection is a tradeoff to achieve the specified value of switch matrix insertion loss of 15 dB.

The directional coupler circuit is separated from the switching amplifier portion by a wall in order to preclude the existence of waveguide modes and thereby compromising the OFF state isolation performance. The concept of the wall separation allows maximum allocation of space for the amplifier matching circuitry.

The allocation of space (0.575" x 0.600" per amplifier stage) is sufficient for matching circuit topology. The design has separated the amplifier stages into input and output substrate areas of 0.250" x 0.600". A mounting rail (0.075" width) for the GaAs FET grounding is machined on the Kovar carrier.

3.2 IF FREQUENCY

The switch matrix IF frequency was selected to be as high as possible within the constraints of minimum crosspoint spacing and switching device isolation. In the proposed design, the method of module packaging limits the maximum frequency due to a 0.585" minimum dimension between coupler crosspoints. Another consideration favoring a high IF frequency is the requirement to achieve wide bandwidth. Thus it is necessary to push the upper frequency limit to keep the percentage bandwidth low with a consequent reduction of mismatch losses.

The IF frequency was selected at 5 - 7.5 GHz for the 2.5 GHz bandwidth design goal, and 5.75 - 6.75 for the specified 1 GHz bandwidth.

3.3 SCHEMATIC

The schematic of a two stage RF circuit is given in Figure 3.3. The representation of distributed circuitry is given as a block with an impedance and element length computed for a dielectric constant of 9.8. The circuit shown was designed to use a Dexcel 2703AP70 GaAs FET device bonded in a cascade configuration (second gate internally grounded).

The lumped elements of the circuit are either etched as part of the circuits in the case of resistors, or are attached by reflow soldering to the appropriate circuit pad in a separate operation. The capacitors are single layer chips bonded with low inductance ribbon. The resistors etched as part of the conductor pattern are formed in a tantalum nitride metalization and are passivated through the formation of a tantalum pentoxide over-layer.

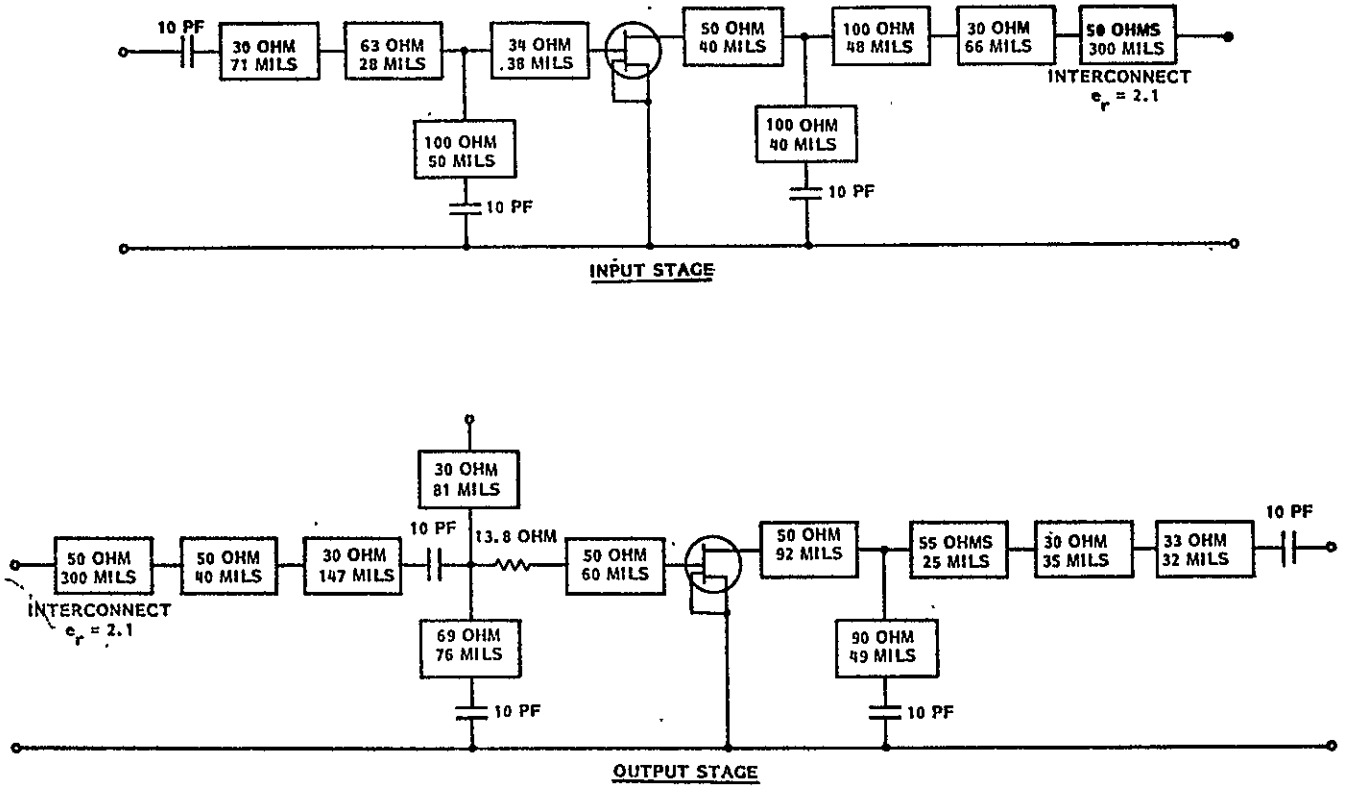


Figure 3.3. Two Stage Circuit Schematic

3.4 CONTROL LOGIC DESIGN

A block diagram of the control logic is illustrated in Figure 3.4, and the logic control format in Figure 3.5.

The command data is organized as a 32 bit parallel word with a read pulse required to store the decoded data in the update memory (see Figure 3.6 for the data format definition).

Each input/output command pair address is decoded by one of the three 5:25 row and three column decoders. The decoded data is OR'd and routed to the appropriate update memory cell. The update memory is thus programmed during the dwell interval for the next desired matrix state.

The reconfiguration or execute pulse transfers the contents of the update memory to the matrix configuration memory. A high speed driver circuit buffers the RF switch amplifier from the matrix configuration memory. The matrix configuration memory contains the current commanded network pattern.

The control logic is organized in terms of controlling a 1 x 25 segment of the matrix. This permits possible utilization of a single custom LSI containing the control functions of the 1 x 25 sub-matrix. The control logic LSI would contain the decoding logic and the update configuration memory, and as such provides a logical compatible partitioning of the system.

The matrix configuration memory and the RF switch interface drivers may be packaged as another custom LSI . The present concept is to incorporate five latch/drivers into a smaller package so that the RF switch-latch/driver interface path, hence delays, can be minimized.

The control logic circuitry for column decoding consists basically of three 5 to 25 decoders and a 25 bit memory cell. The outputs of the three decoders are OR'd and the result stored in the update memory by the read pulse associated with the data transfer.

The row decoding scheme is similar but does not require the memory feature. The three 5 to 25 row decoders simply provide a sixth input, an enable, to the column decoders.

After completion of the necessary assignments for the next desired network pattern, the data is transferred from the update memory to the matrix configuration memory (high speed latch driver) and subsequently switches the RF amplifier upon receipt of the reconfiguration pulse.

The logic diagram, Figure 3.7, of the digital control unit illustrates the decoding function that would comprise a row or a column decoder. The column logic is slightly more complex than the row logic as it requires an ORing function and memory to store the results in addition to the decoding network.

The logic diagram illustrates the row decoder in its simplest form. It decodes the three bits of data into five of the eight possible states. The decoded row output enables one of five column decoders.

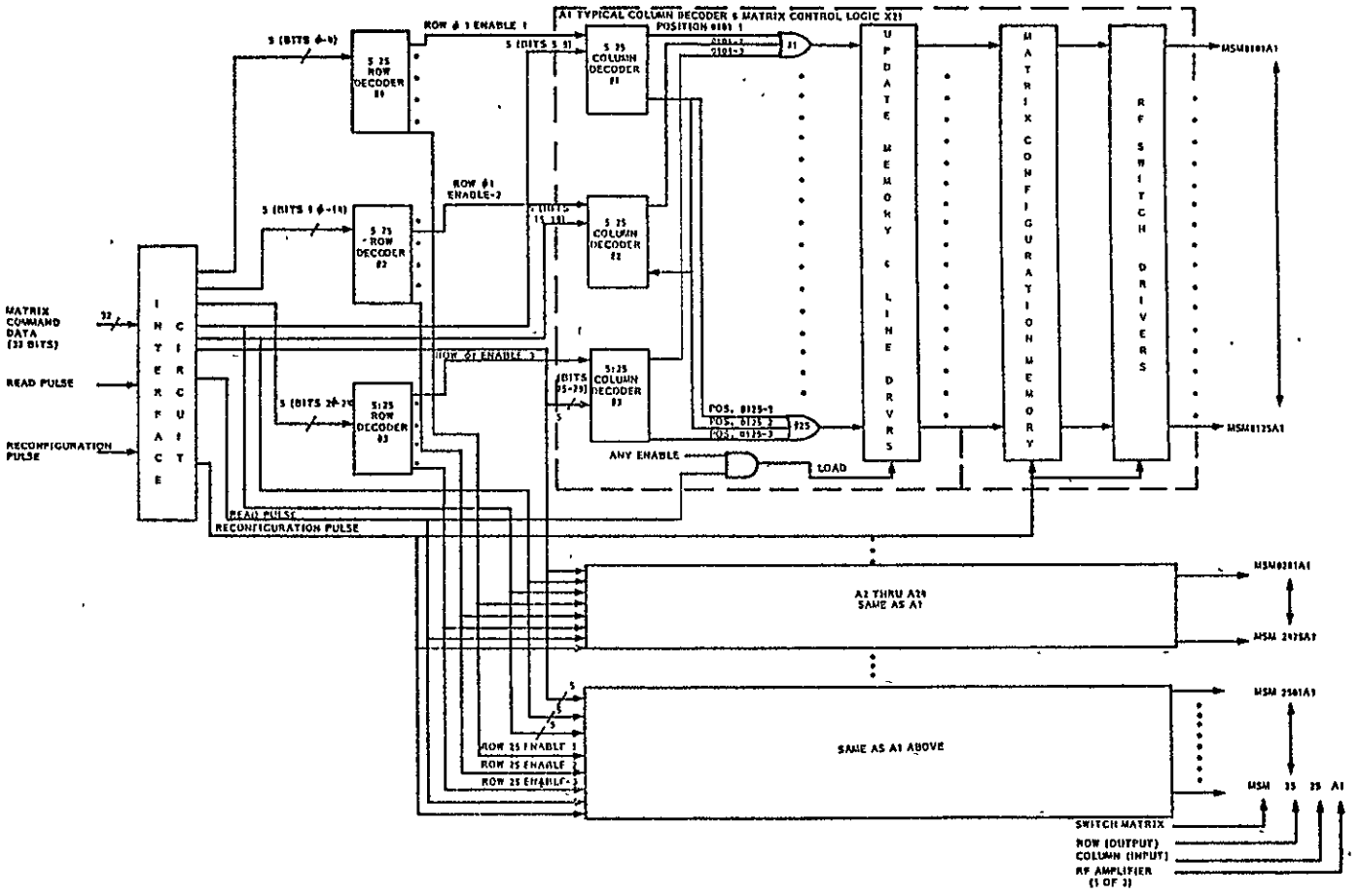


Figure 3.4. Control Logic Block Diagram

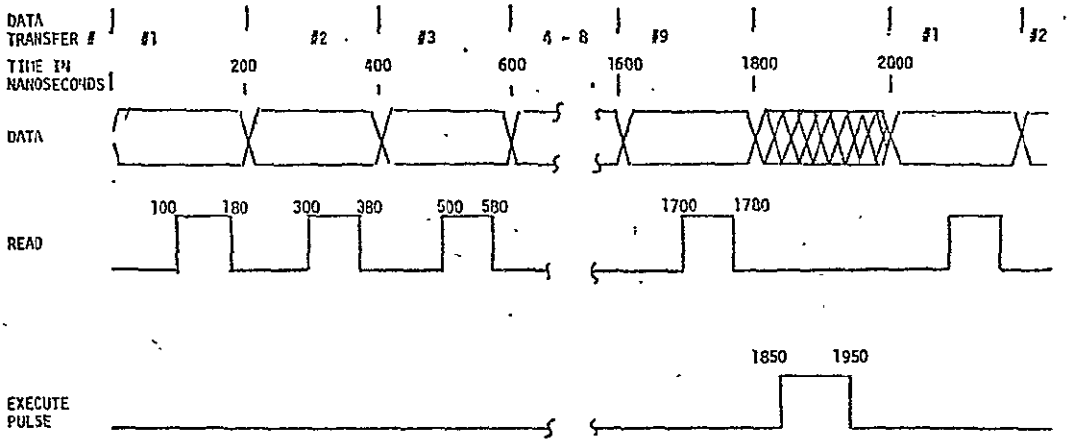
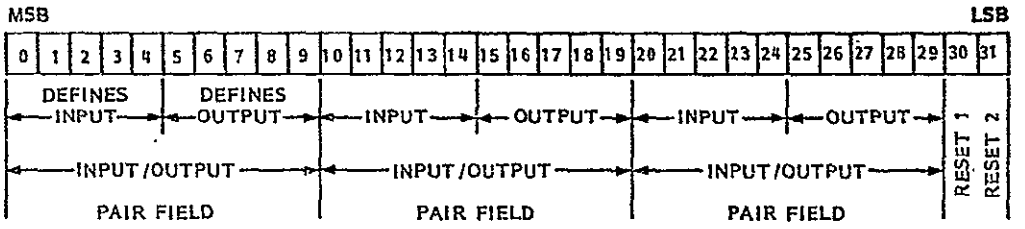


Figure 3.5. Timing Diagram for Switch Matrix Control

DATA FORMAT

32 BIT PARALLEL DATA BYTE



DATA TRANSFER NUMBER	BIT NUMBER						
	0 4	5 9	10 14	15 19	20 24	25 29	30 31
1	INPUT ROW ADR	OUTPUT COL. ADR	INPUT ROW ADR	OUTPUT COL. ADR	INPUT ROW ADR	OUTPUT COL. ADR	
2							
3							
4							
5							
6							
7							
8							
9							

Figure 3.6. Switch Matrix Data Format

The data field to the enabled column decoder selects the memory cell in that column to be activated. The accompanying read pulse clocks the data into the flip-flop thereby completing the crosspoint selection for a data transfer.

The logic schematic in Figure 3.7 indicates the logic for a 5 x 5 matrix. The logic circuitry is repeated to achieve a full 20 x 20 switch matrix with redundancy.

For a 20 x 20 matrix with five wraparound redundancy, nine data transfers consisting of three crosspoint selections per transfer are required to completely rearrange the entire matrix per the data format illustration Figure 3.6.

3.5 LOGIC CIRCUIT INTEGRATION

The control logic as described above can be partitioned into two LSI devices for development of the POC model. The basic decoding logic and its associated update memory constitute one LSI while the second is comprised of the latch/drivers circuitry needed to provide the matrix configuration memory and RF switch interface functions.

3.5.1 Decoding and Update Logic LSI

The 1 x 25 sub-matrix organization provided a convenient "building block" for the decode logic and its required update memory. The number of inputs, outputs, and logical functions needed blend into a suitable 48 pin custom LSI utilizing CMOS-bulk technology.

3.4.2 Special Geometry Latch/Driver LSI

The matrix configuration memory which basically breaks down to be a latch/driver combination is presently conceived to be another LSI utilizing CMOS-bulk techniques. The need to minimize system propagation delays, hence line lengths and capacitances, dictates that the latch/driver network be positioned as close as possible to its associated RF amplifier switch control. Ideally a one for one relationship would allow the latch/driver to be located almost directly behind the RF network it controls, hence the shortest lead length possible is obtained. Practically, it is not the best situation for signal distribution of the clock pulse required to interface with all matrix configuration memory devices. Each clock input of the matrix configuration memory adds to the propagation delay because of the increase in line length and associated capacitances. The compromise design solution is to package five latch-drivers circuits and a clock buffer on a special geometry custom LSI.

The two basic LSI components that comprise the control logic are integrated into the 1 x 25 building block as illustrated in Figure 3.8.

3.6 PACKAGING DESIGN

The 20 x 20 coupled crossbar matrix is made up of three basic components. These components are:

1. Channel Modules
2. Mounting Plate
3. Interfacing Circuitry Modules

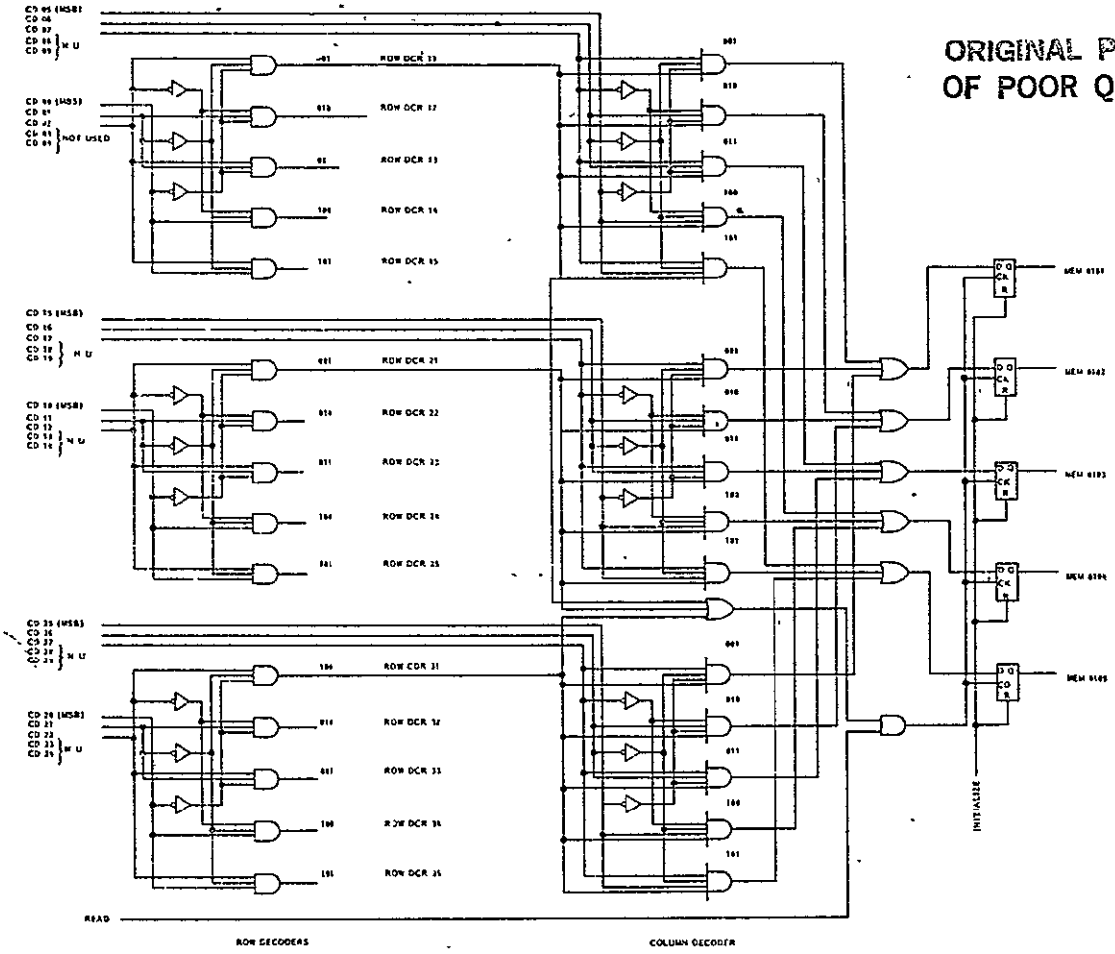


Figure 3.7. Row or Column Decoder

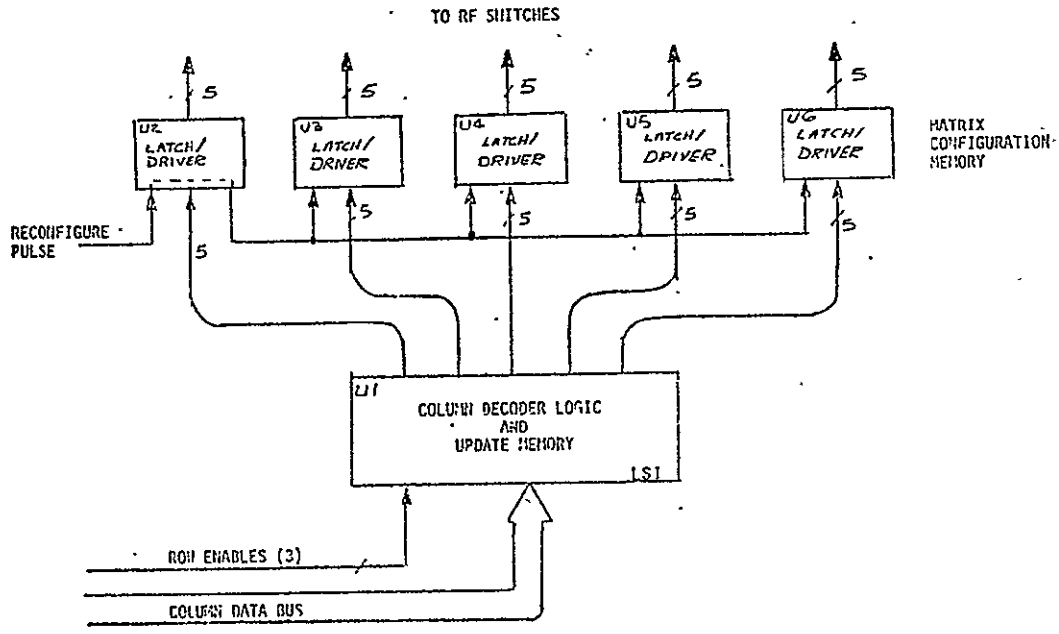


Figure 3.8. Sub-Matrix (1 x 25) Building Block for Switch Matrix Using Custom CMOS/SOS LSI

Forty (40) channel modules (20 input and 20 output), two (2) interfacing circuitry modules and one (1) mounting plate make up the 20 x 20 switch matrix. This arrangement is illustrated in Figure 3.9.

As can be seen, the channel modules are of an I-Beam type construction. This design was chosen for the following reasons:

1. It forms a very rigid structure
2. It forms a partition between RF and logic circuits.
3. It allows the RF circuits to be close enough to the logic circuits so that interfacing the two is not a problem.

The partition formed by the I-Beam design provides two chambers. One chamber will house a string of twenty (20) RF switching circuits and the other chamber will contain a PC board to mount the accompanying logic. Input and output of the modules is through an RF connector mounted to the front wall. Logic interfacing circuitry is wired to the module logic board through a connector mounted on the rear wall as shown in Figure 3.9.

The mounting plate serves as a mounting surface for the modules and also as a mounting fixture for the overall matrix. The input and output modules are assembled on the mounting plate at 90° to each other and are bolted, to the plate, at front and rear. The interfacing circuitry will be mounted to the plate adjacent to the rear of the modules. This allows the most efficient use of space and also minimum cable lengths as shown in Figure 3.9. The mounting of these modules as described above forms a very solid structure while also allowing any individual module to easily be removed for repair or replacement.

In this design, the mounting plate is structured to support the interfacing modules and to act as a mounting fixture for the entire switch matrix. The mounting plate concept results in a significant weight reduction. It eliminates the need of a larger and heavier housing.

The interface logic circuitry modules contain printed circuit board plug-in connectors on one side and mounting provisions on the adjacent side. This allows the modules to be mounted with a minimum cable length to the channel modules.

Each channel module is approximately 13" long x 0.6" wide x 1.6" high; with space allocated for the interfacing circuitry, the overall size and weight of the 20 x 20 matrix becomes 16" long x 16" wide x 3.4" high. Weight of the structure will be approximately 35 lbs. With redundancy included, 5 wrap-arounds, the overall matrix dimensions increase to 19" long x 19" long x 3.4" high at a weight of 40 pounds.

A cutaway view showing the RF circuit side of the channel module is illustrated in Figure 3.10. This is the basic design for the 20 x 20 switch matrix. The same pattern is extended to accommodate 20 RF circuits.

Each RF circuit consists of three substrates which includes a coupler, GaAs FET, and FET circuitry. The substrates are mounted on a Kovar carrier which separates the coupler from the FET circuitry as shown in Figure 3.11. The

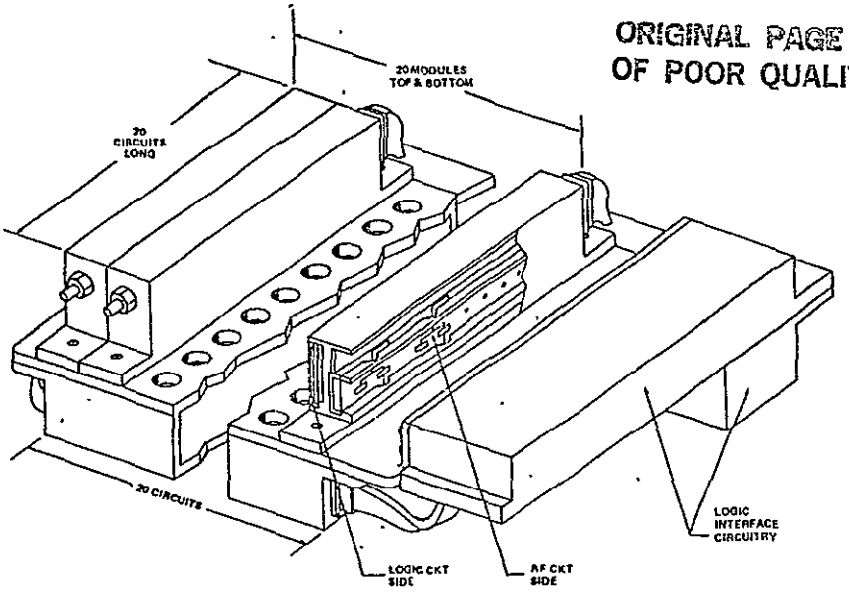


Figure 3.9. 20 x 20 Switch Matrix Packaging

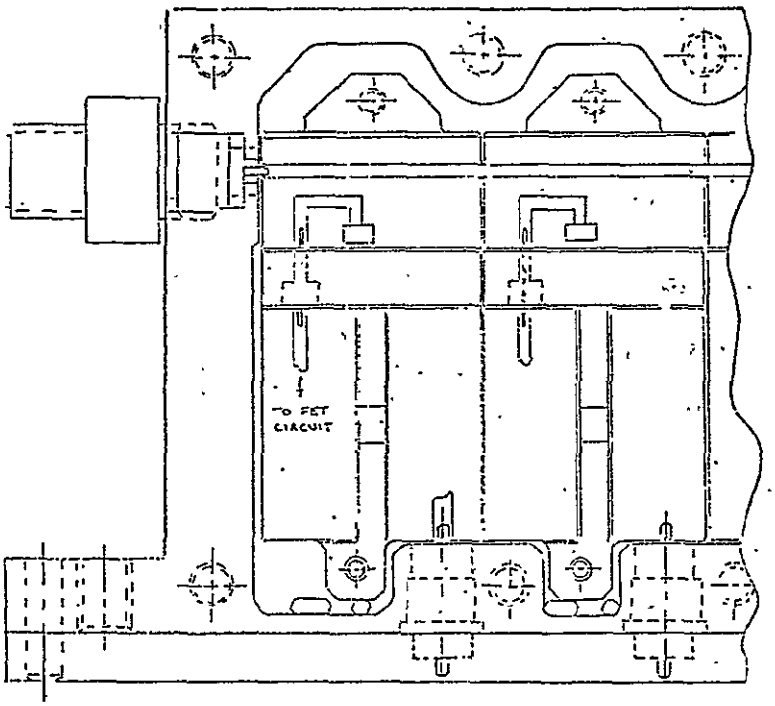


Figure 3.10. Channel Module - RF Circuit

usable coupler area is 0.3" x 0.585" and the usable FET circuit area is 0.6" x 0.585". Interconnection of the coupler and FET circuit is through an RF feed-through which is bonded in an opening milled in the Kovar wall. The Kovar carrier is mounted to the channel module at the top and bottom mounting feet. Input to the coupler is accomplished by means of an RF connector which is mounted on the corner of the channel module. Output of the FET circuit is through a 50 ohm interconnect, located in the lower right hand corner of the amplifier assembly. The interconnects are placed into counterbored holes, in the base of the channel module, and secured with press fit retaining rings. The interconnect extends from the base of the module so that positioning in the mounting plate will be simplified. This design allows the upper and lower modules to mate within the mounting plate and thus reduces the amount of play between the two interconnects.

Interfacing between the RF circuits and the logic circuits is accomplished by bringing wires from the logic circuit through holes drilled in the partitioning wall, and terminating at pads on the FET circuit.

The logic circuit side of the channel module consists of a printed circuit board which spans the entire module length, and a 32 pin connector wired to the PC board. The connector mounts on the channel module back wall, and allows connection to the external interface circuitry.

3.7 RELIABILITY

This section presents the results of the reliability analyses that have been completed relative to the 20 x 20 IF switch matrix.

If no redundancy is employed within the switch matrix, the probability that any one of n inputs can be connected to any one of n outputs at any time during a ten (10) year mission is calculated as follows:

$$P_s = R^N$$

where P_s = Probability of success

N = Number of crosspoints (n^2)

R = e^{-T} = Probability of success of one crosspoint

T = 87600 hours (10 years)

λ = Failure rate of a crosspoint

This matrix, for n = 20 and with no redundancy included, will result in a low probability of mission success (0.30065 for ten years for an assumed crosspoint reliability of 0.997). To increase this probability of mission success, redundancy is incorporated using the "wraparound" technique as illustrated in Figure 3.12.

To assess the reliability of the IF switch matrix using the "wraparound" technique for redundancy, the following guidelines and/or assumptions were used:

1. For success any input can be connected to any output at any time.

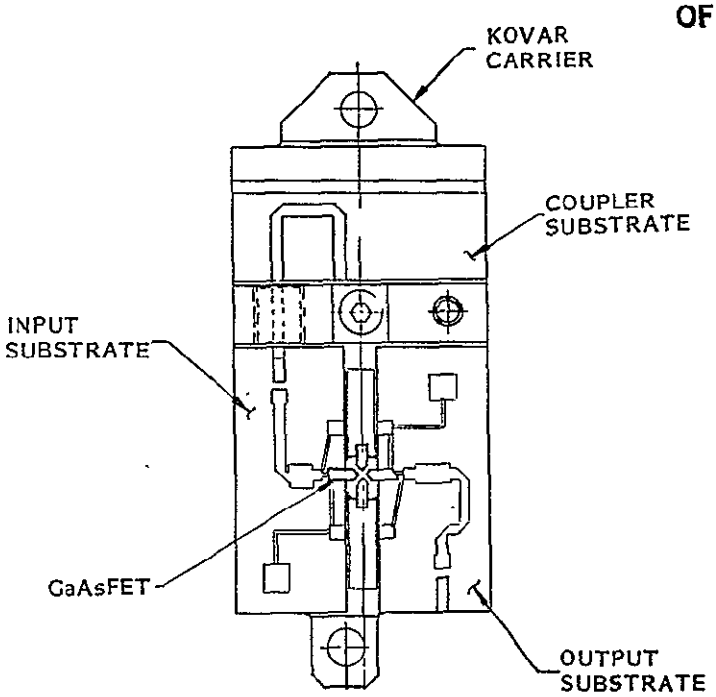


Figure 3.11. Microwave Switch Crosspoint Carrier Assembly

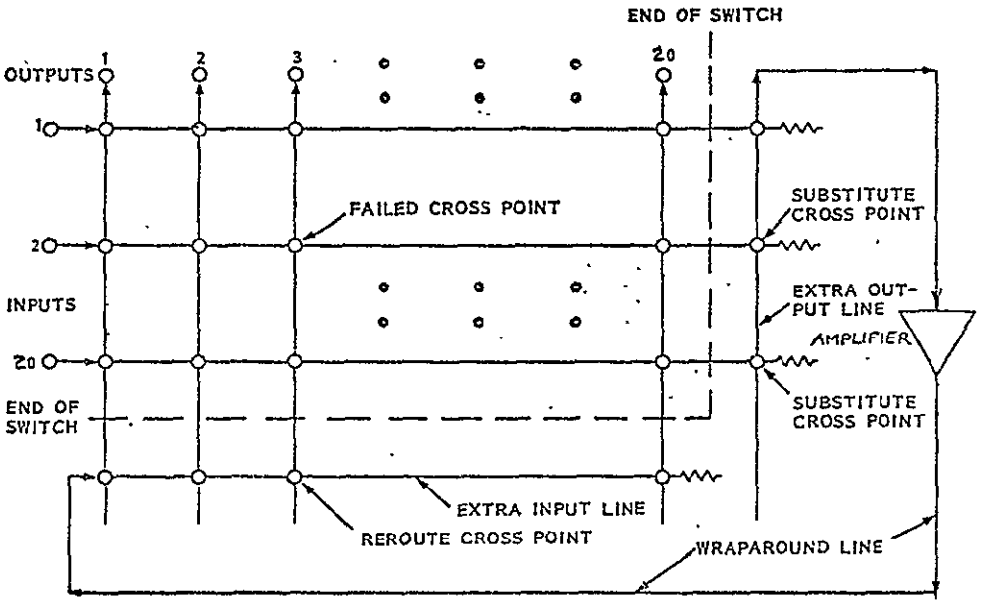


Figure 3.12. Wraparound Redundancy for Crossbar Switch Matrix

2. Mission life is 10 years.

3. Two crosspoints in a wraparound can be activated to connect an input to an output if its crosspoint fails to close.

4. No single failure in a crosspoint results in either a short between an input an output line, or a short to ground on an input or output line.

5. One wraparound (two crosspoints) can successfully connect an input to any output if one or all crosspoints fail to close on an input row or one or all crosspoints fail to close on an output column.

6. A switchable amplifier is required in each wraparound to compensate for loss of signal gain due to coupler loss in the second crosspoint of the wraparound. This amplifier is equivalent to an additional crosspoint for reliability calculations.

7. Each input line and each output line requires a coax connector. Each coax connector is a potential single point failure for the overall switch matrix. The probability of success for the overall switch matrix is then calculated as the probability of success of 40 coax connectors times the probability of success of the switching matrix.

8. The probability of success of the switch matrix was calculated by using a truth table.

3.8 RESULTS OF RELIABILITY TRADE STUDIES

During the initial design stages, reliability trade studies were conducted. The results of these studies has shown that the optimum design for a 20 x 20 IF switch matrix based on weight, power consumption and reliability is one that contains:

1. Five wraparounds for redundancy.

2. Separate IC logic to control each GaAs FET switch in a crosspoint, to eliminate single point failures.

3. The optimum building block for the switching logic (to control the switch of each crosspoint) when considering the IC packaging complexity and output pins, is a 1 x 25 matrix. The use of 25 of these building blocks readily provides a 20 x 20 switch matrix with 5 wraparounds.

4. A 32 bit interface method of decoding the input logic to control the switches of a crosspoint.

The reliability success diagram and the predicted reliability for a 20 x 20 IF switch matrix is shown on Figure 3.13. The overall probability of success for the IF switch matrix is limited by the forty non-redundant coax input and output connectors.

3.9 CONCLUSIONS

A 20 x 20 IF switch matrix containing five wraparounds and controlled by a 32 bit interface logic is the optimum design. This optimum design will provide an IF switch matrix that has a 0.97992 probability of success for ten years with only the input and output coax connectors as potential single point failures.

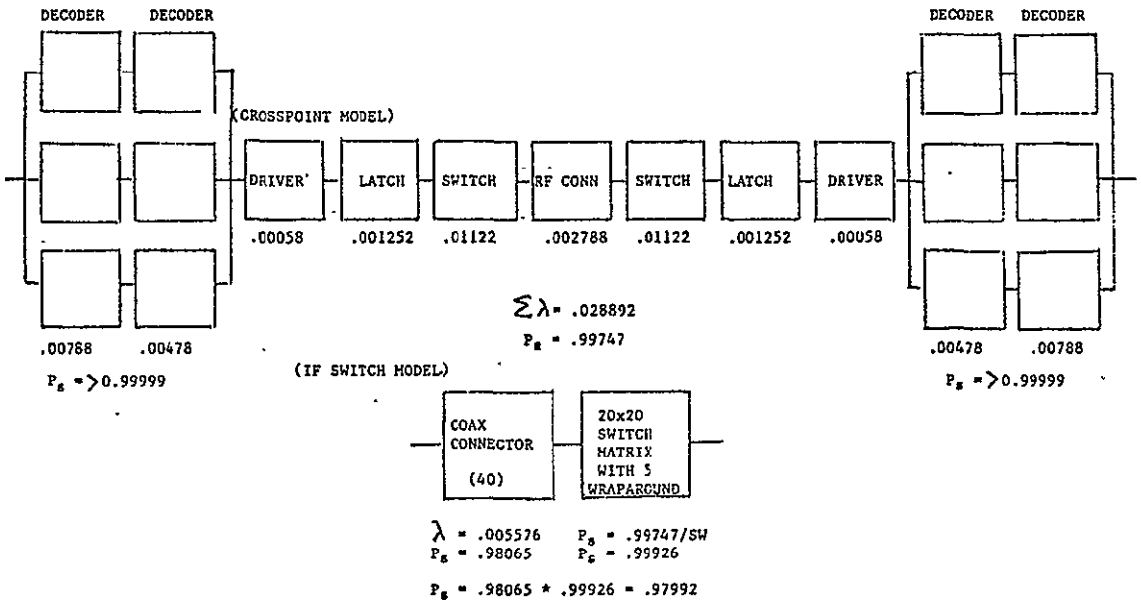


Figure 3.13. Switch Matrix Reliability Success Diagram

SECTION 4

BREADBOARD DEVELOPMENT

A Breadboard Development Task was undertaken to prove feasibility of the technical concepts developed during the Task I Switch Matrix Design study. Individual microwave couplers were first evaluated prior to fabrication and test of a cascade of five couplers. A single stage, followed by a two stage GaAs FET switch/amplifier design was then evaluated. A test fixture to verify the performance of the two stage switch/amplifier interconnect system was completed. Test results of a fully integrated microwave switch crosspoint was then evaluated (Figure 4.1).

In order to minimize breadboard costs, it was elected to build a 5 x 5 switch matrix mechanical model, but populate only nine of the crosspoints with microwave switches as shown in Figure 4.2. The control logic design was evaluated using integrated circuits for all of the design with the exception of the high speed switch drivers which utilized discrete bipolar devices. High speed switch drivers were located at crosspoints 1,1 and 5,1. The balance of the microwave switches were driven with regular TTL devices.

A block diagram of the breadboard switch matrix design is shown in Figure 4.3. The only difference between this and the Task I design was the grounding of Gate 2 on both GaAs FETs. Because of the high output Q of the GaAs FETs, 2.5 GHz bandwidths could not be achieved in the computer design model. By grounding Gate 2 of the FETs, 2.0 GHz bandwidth was achieved. Figure 4.4 illustrates a block diagram of the control logic. Row and Column decorders, and memory circuits for twenty-five crosspoints were provided for evaluation; however, only nine switch drivers were assembled.

A fully populated input row channel module is shown in Figure 4.5. This view shows the microwave integrated circuit (MIC) side of the channel assembly. The crosspoint interconnect system is shown on the bottom edge of the channel. A center conductor pin is seated in the one connector at the left side of the assembly. A wire provides the logic drive signal from the reverse side of the channel.

The fully integrated breadboard switch matrix is shown in Figure 4.6. The discrete component high speed switch drivers are shown in the logic side of the channel modules. As shown, space was the limiting factor of providing only two high speed switch drivers. This picture also shows the basic structure of the switch matrix. The output column channels are shown on the top of the matrix, the mounting plate in the center, and the input row channels on the bottom.

Figure 4.7 shows the two control logic printed wiring boards and the breadboard test box. Toggle switches on the test box are used to set the switch matrix crosspoint address data.

A summary of the breadboard test data is as follows:

- IF Frequency 6.25 GHz
- Bandwidth 2.0 GHz

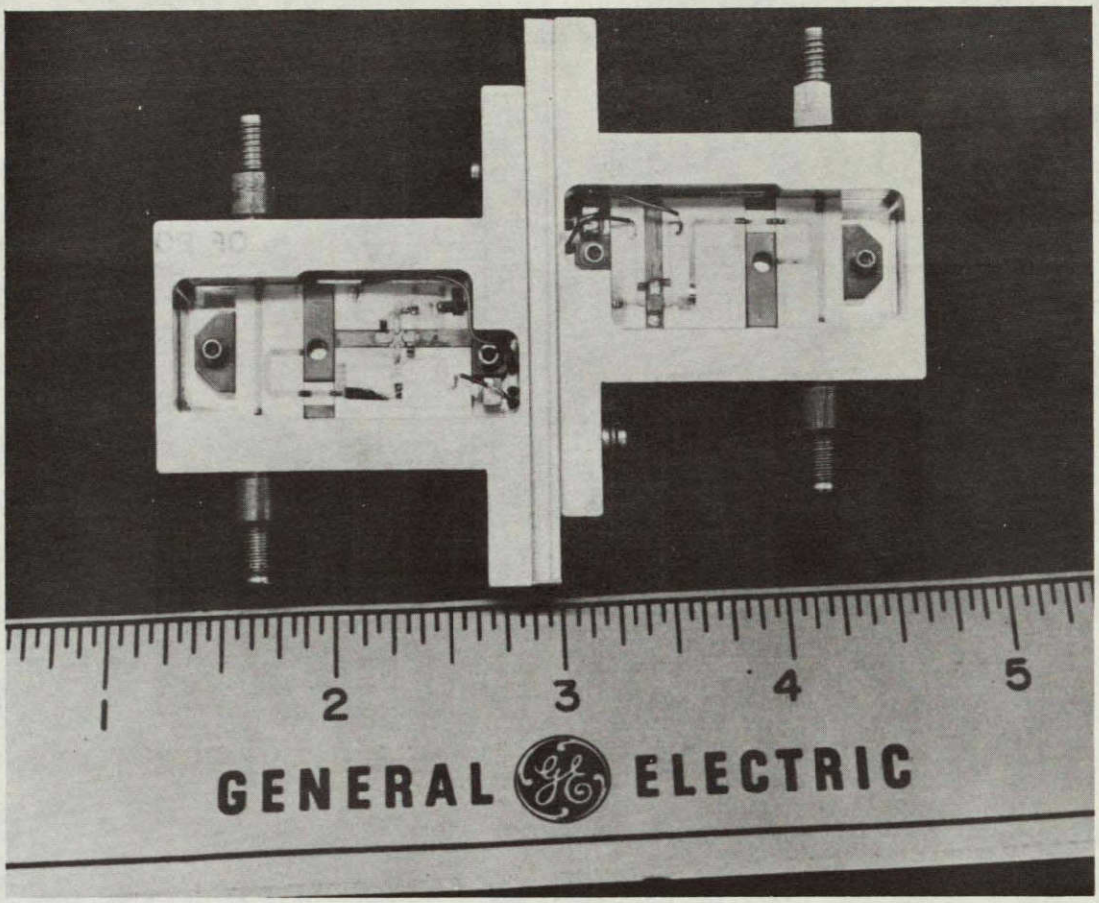


Figure 4.1. Two Stage Switch Crosspoint Mounted in a Test Fixture

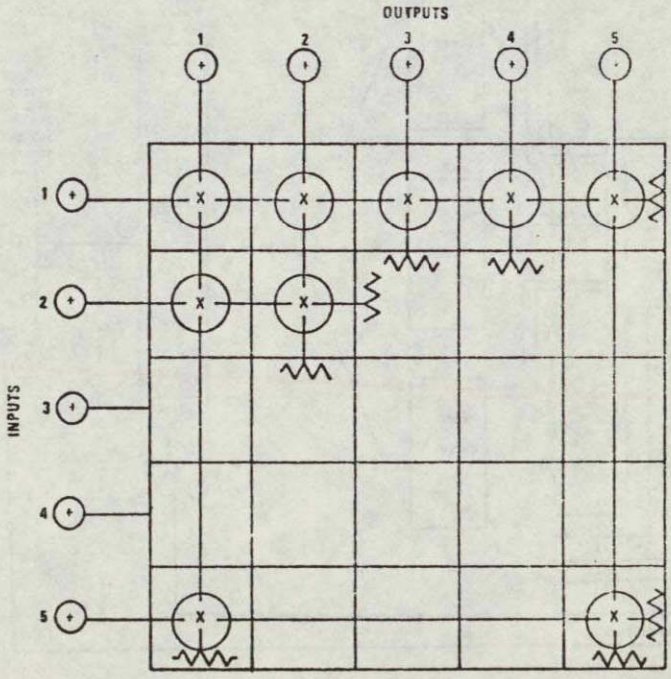


Figure 4.2. Breadboard Switch Matrix Crosspoint Allocation

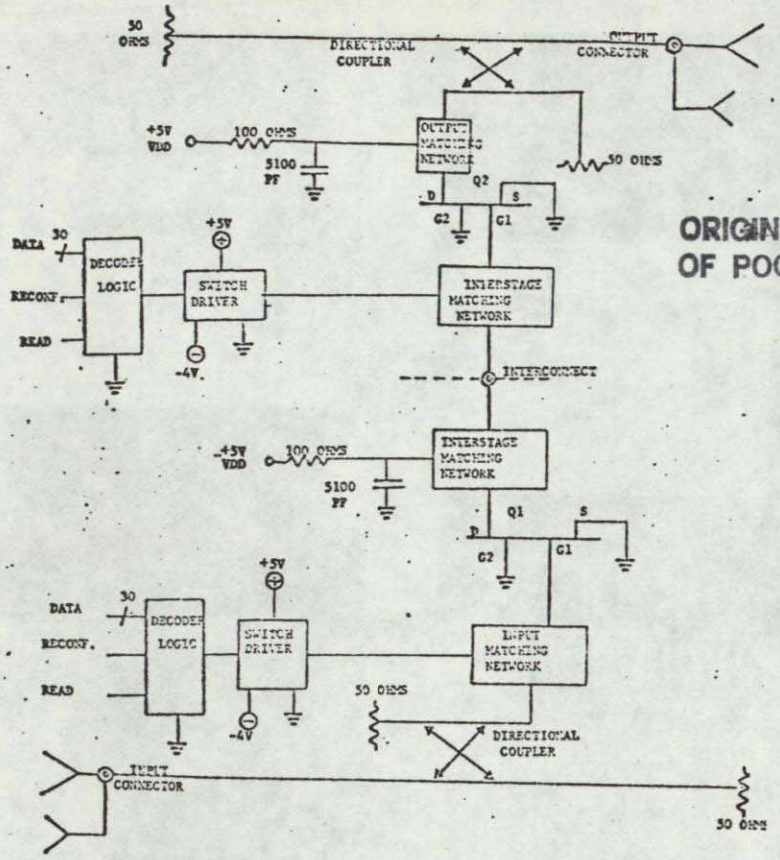


Figure 4.3. Crosspoint Block Diagram

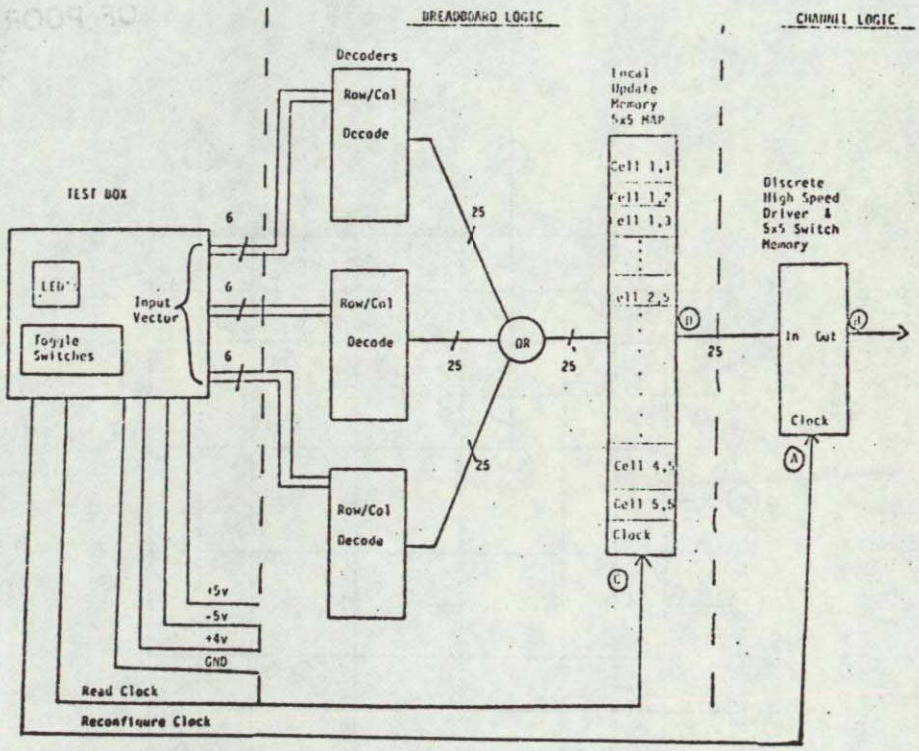


Figure 4.4. Control Logic Block Diagram

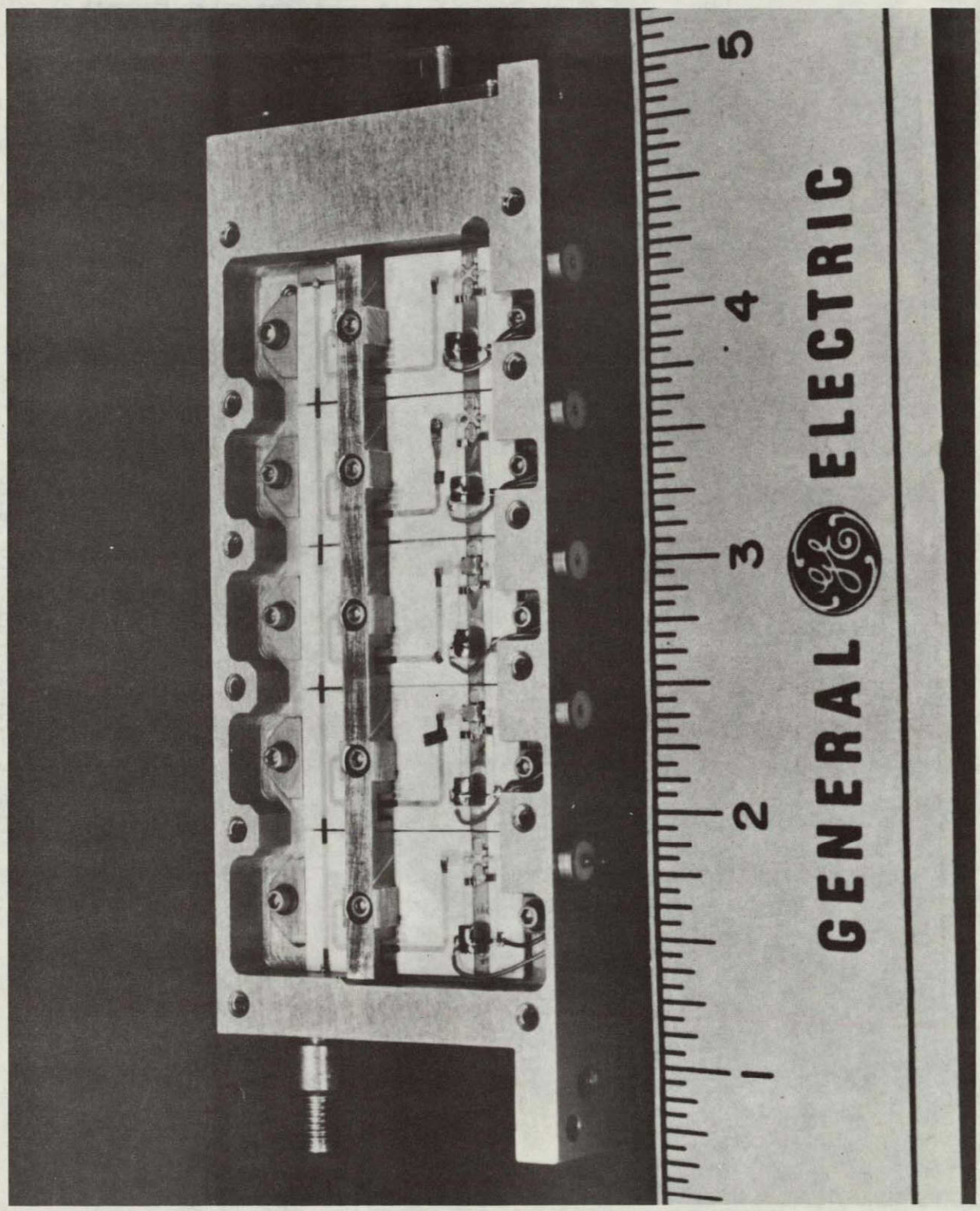


Figure 4.5. Breadboard Channel Assembly

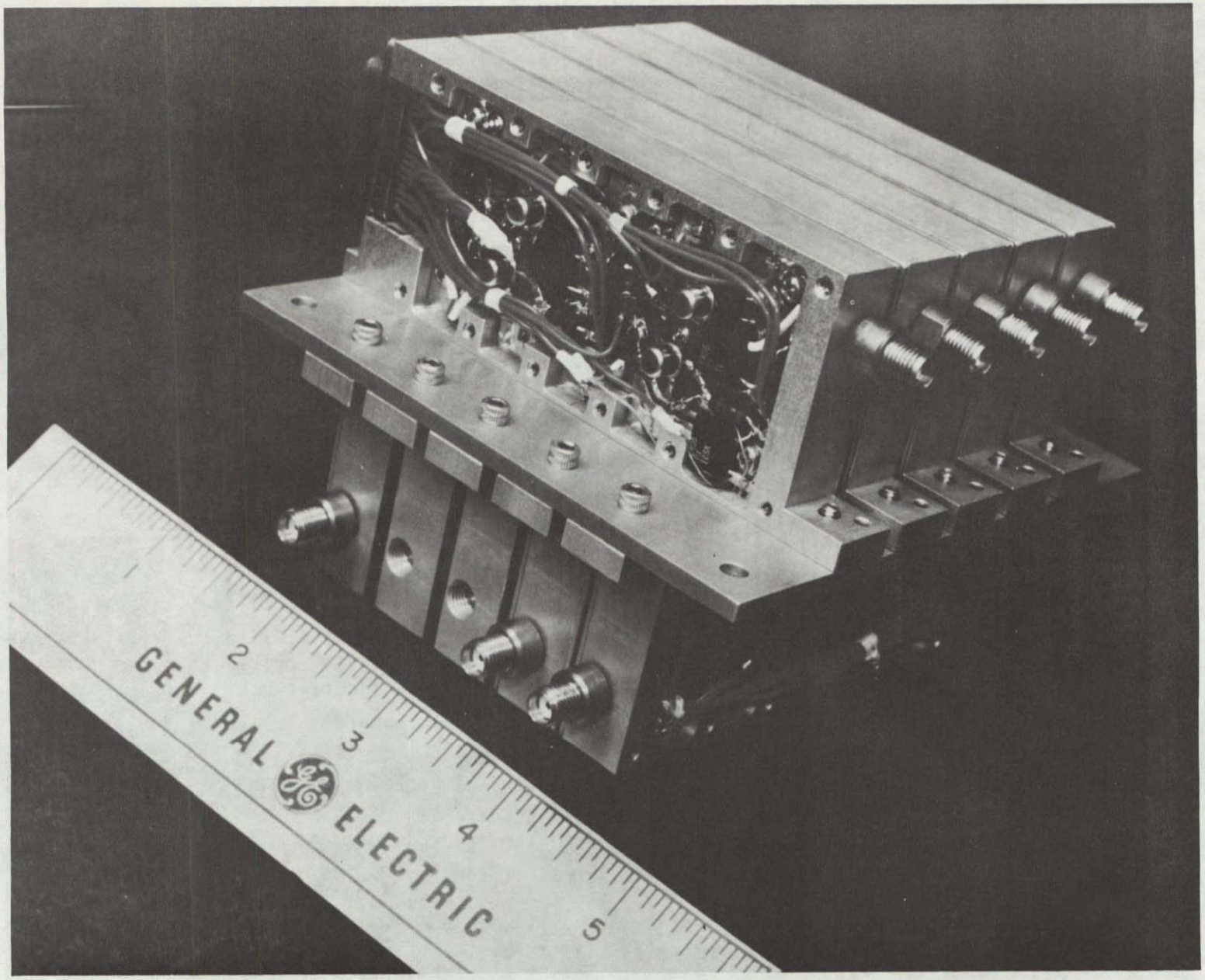


Figure 4.6. Breadboard Switch Matrix

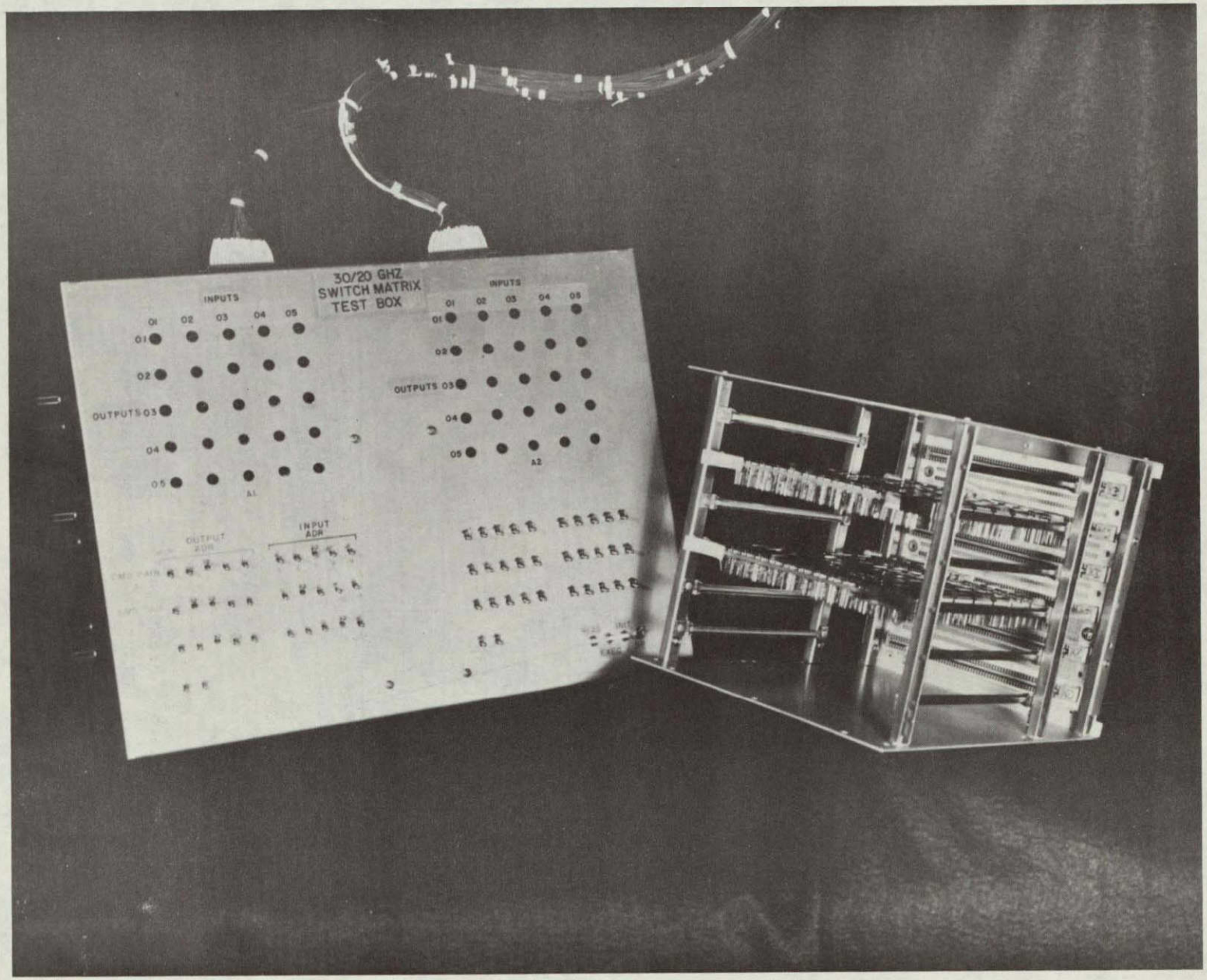


Figure 4.7. Breadboard Switch Matrix Control Logic and Test Box

- Off-State Isolation > 65 dB
- Insertion Loss 17 dB
- Switching Speed 2 nsec's
- VSWR 1.4:1

Figure 4.8 shows a data plot from an HP Automated Network Analyzer of a cross-point (2,1) insertion loss versus frequency over temperature.

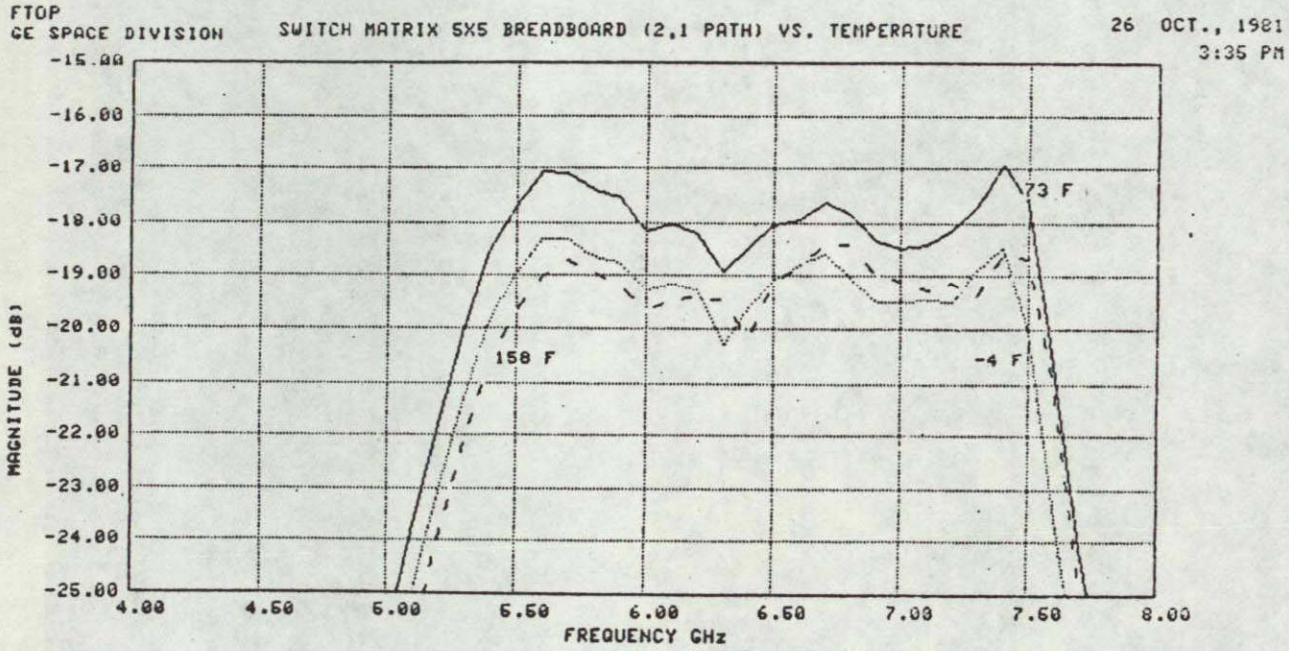


Figure 4.8. Breadboard (2.1) Insertion Loss vs. Frequency over Temperature

SECTION 5

PROOF OF CONCEPT MODEL DEVELOPMENT

5.1 SWITCH MATRIX

A major effort of the Switch Matrix Program was the design, fabrication, and test of a Proof-Of-Concept (POC) Model of the 20 x 20 IF Switch Matrix utilizing 1982 Technology. The POC design was basically the same as the breadboard design. Design efforts evaluated and improved the coupler performance and termination in order to meet the VSWR requirement of 1.2:1. A tradeoff between gain vs bandwidth was completed in order to improve insertion loss of the switch crosspoints. Gain bandwidth is primarily a function of the GaAs FET device. It was decided to redesign the crosspoint for a bandwidth of 1.3 GHz at an insertion loss of 11 dB.

The POC model was physically the size of a 20 x 20 matrix with one wraparound channel for redundancy. The unit was populated with only sixty-one crosspoints in order to minimize cost, but be able to demonstrate feasibility of the conceptual design. The active crosspoints are shown in Figure 5.1. It was also decided that the control logic would be fabricated using discrete integrated circuits rather than a custom LSI design in order to minimize costs. The complete logic design concept was incorporated into the POC model; however, crosspoint addressing was only provided for the sixty-one crosspoints as shown in Figure 5.2. Control logic timing and data formating are the same as discussed in Section 3.4.

A close-up view of the microwave integrated circuit (MIC) carrier assembly is shown in Figure 5.3. This photograph shows the output stage of the microwave switch crosspoint, and Figure 5.4 shows the complete output column channel assembly. Figure 5.5 shows the reverse side of the channel which is a close-up of the logic switch drivers. For a flight model switch matrix, the discrete logic components would be replaced with a custom LSI package. Figure 5.6 shows the complete logic switch driver assembly.

The POC model control logic, excluding the switch drivers, are shown in Figure 5.7. Both boards are identical; the board on the right is the front side, and the board on the left is the rear side. The control logic assembly consists of two multilayer printed wiring boards. Each board contains 122 integrated circuits and provides the redundant logic control system for addressing the switch crosspoints. A heat sink design extracts heat from under each IC package and conducts it to the outer edges of the board where it is distributed via the mounting clips to the switch matrix housing. The heat sinks were chemically milled six-ounce copper foil, plated and bonded to both sides of the printed wiring boards.

The fully integrated POC Model is shown in Figure 5.8. The Switch Matrix is shown with the cover removed, exposing the input row channel assemblies. In Figure 5.9 the bottom of the Switch Matrix is shown with the output column channels and the control logic printed wiring board assemblies exposed.

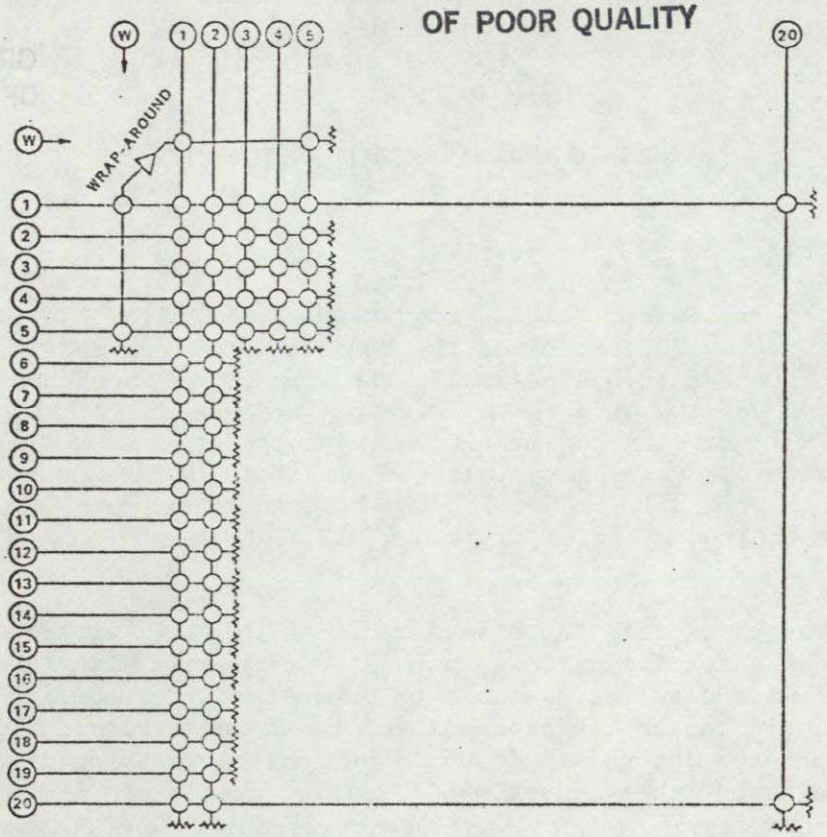


Figure 5.1. POC Switch Matrix Crosspoint Distribution

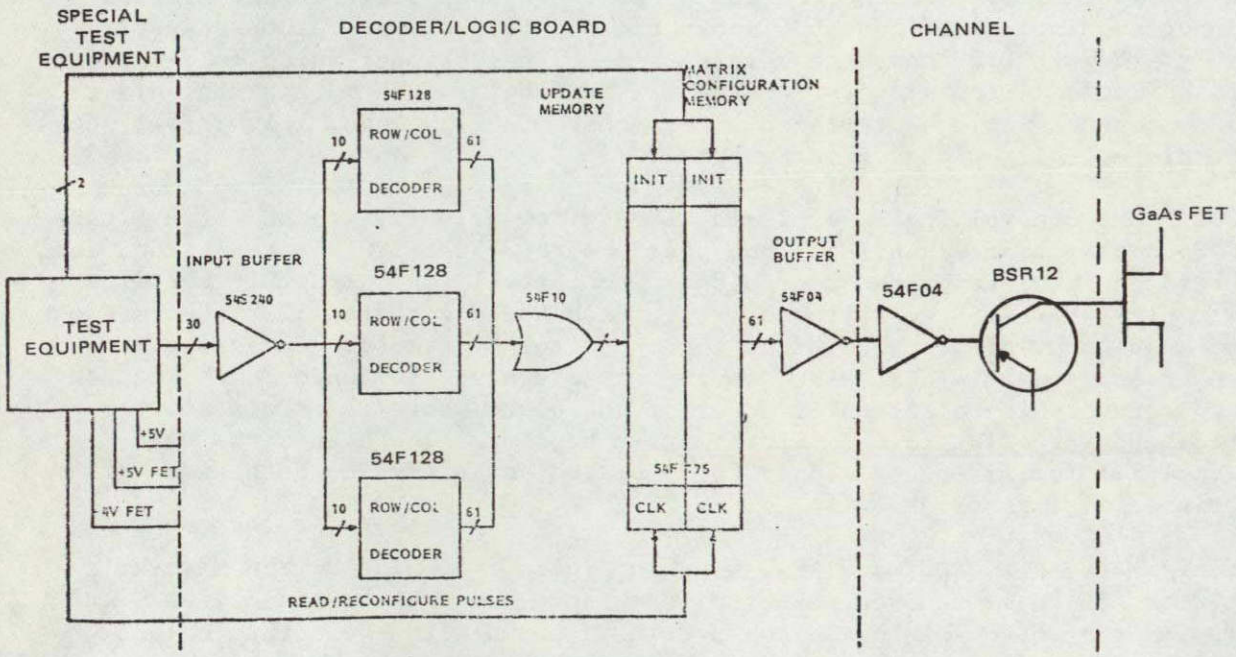


Figure 5.2. POC Model Control Logic Block Diagram

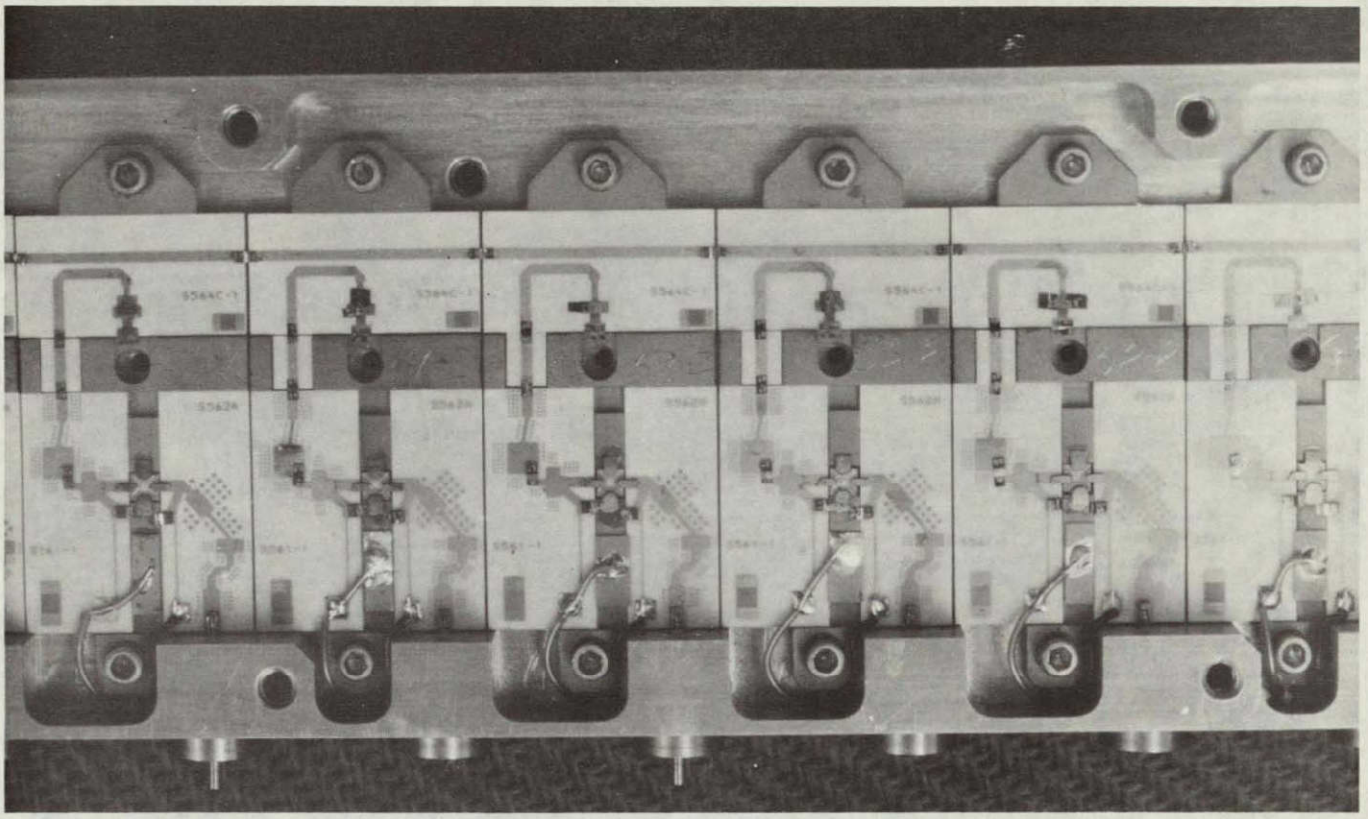


Figure 5.3. MIC Carrier Assembly

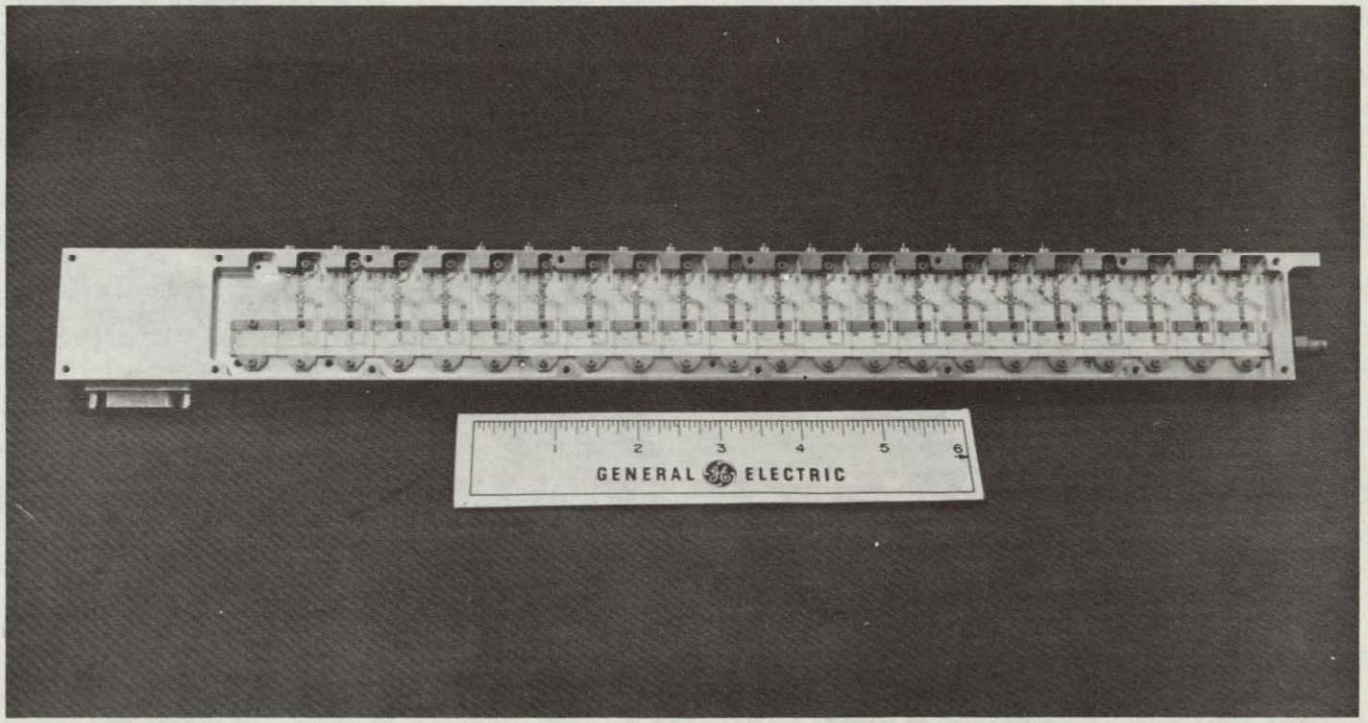


Figure 5.4. POC Column Channel Assembly (MIC Side)

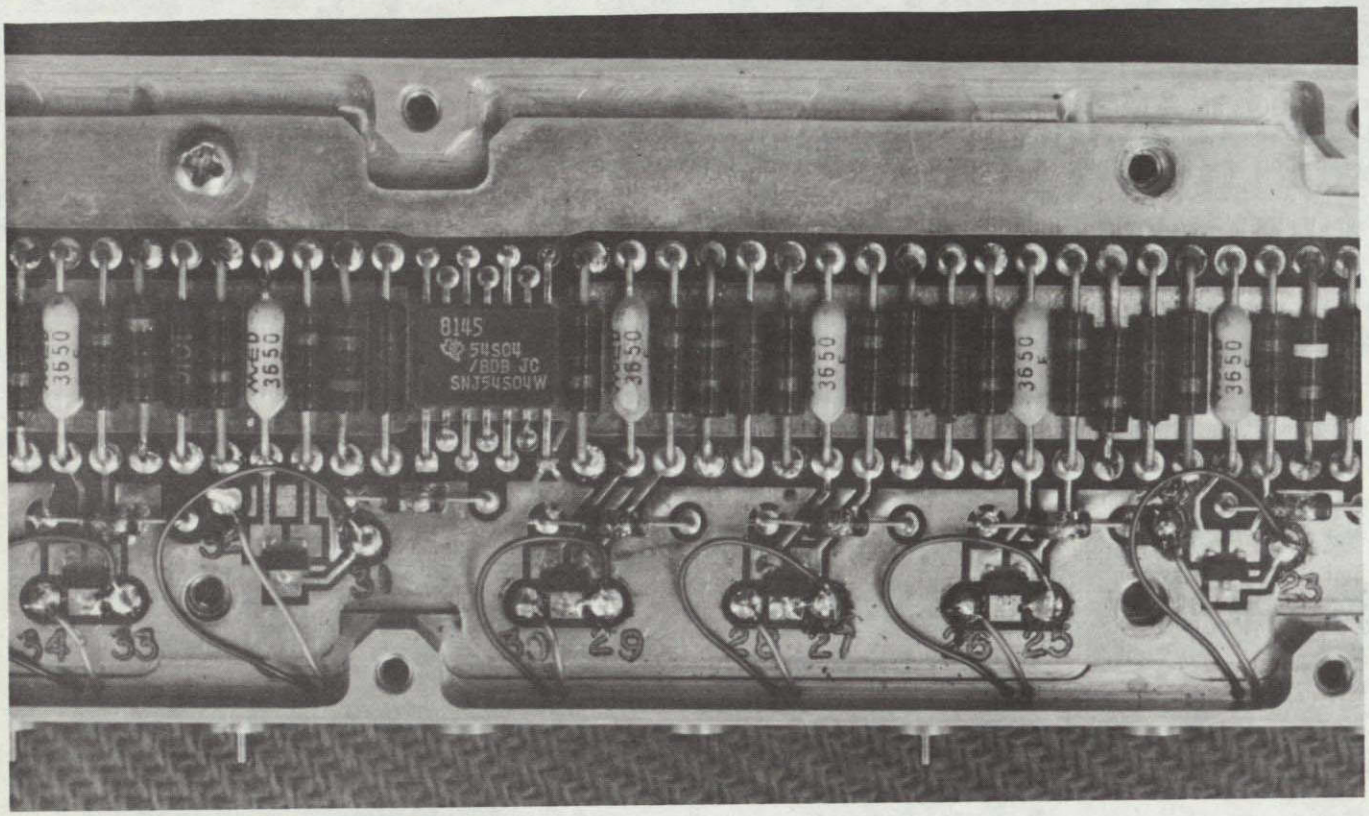


Figure 5.5. Logic Switch Driver Assembly

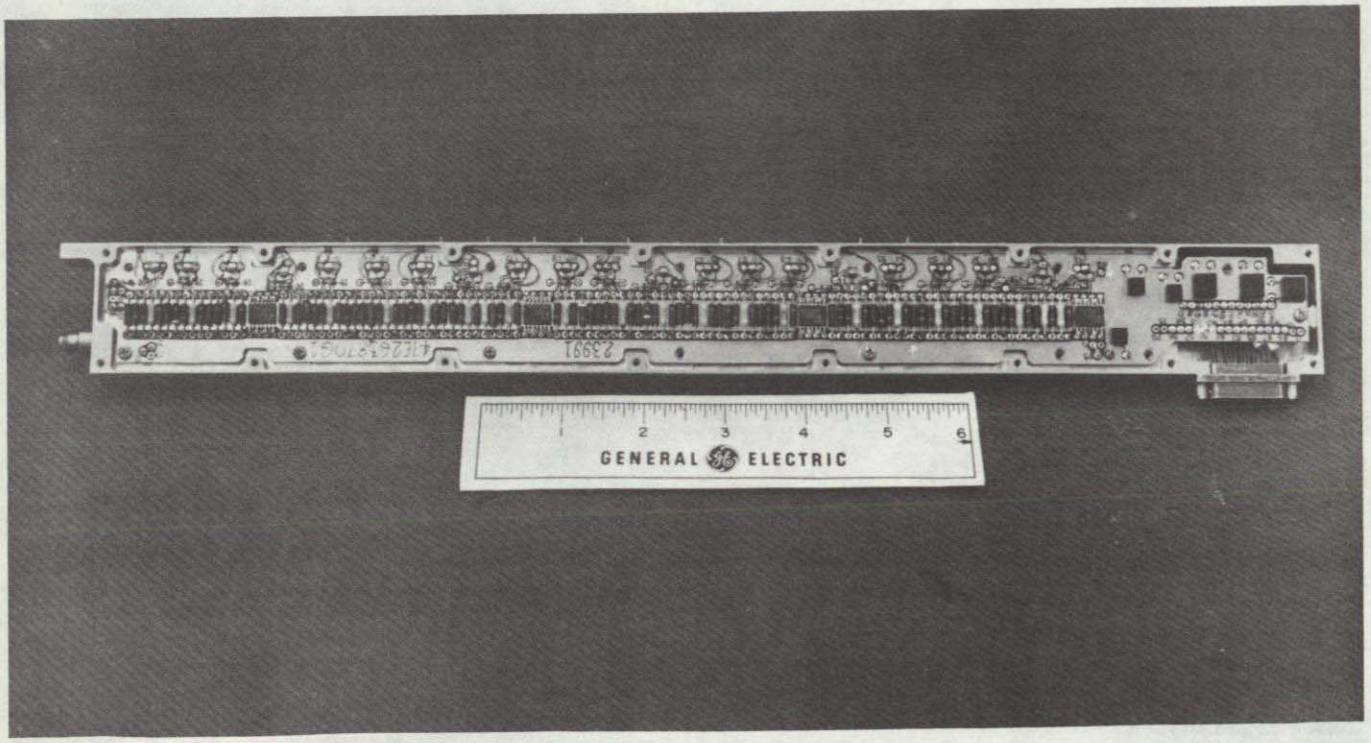


Figure 5.6. POC Column Channel Assembly
(Logic Switch Driver Side)

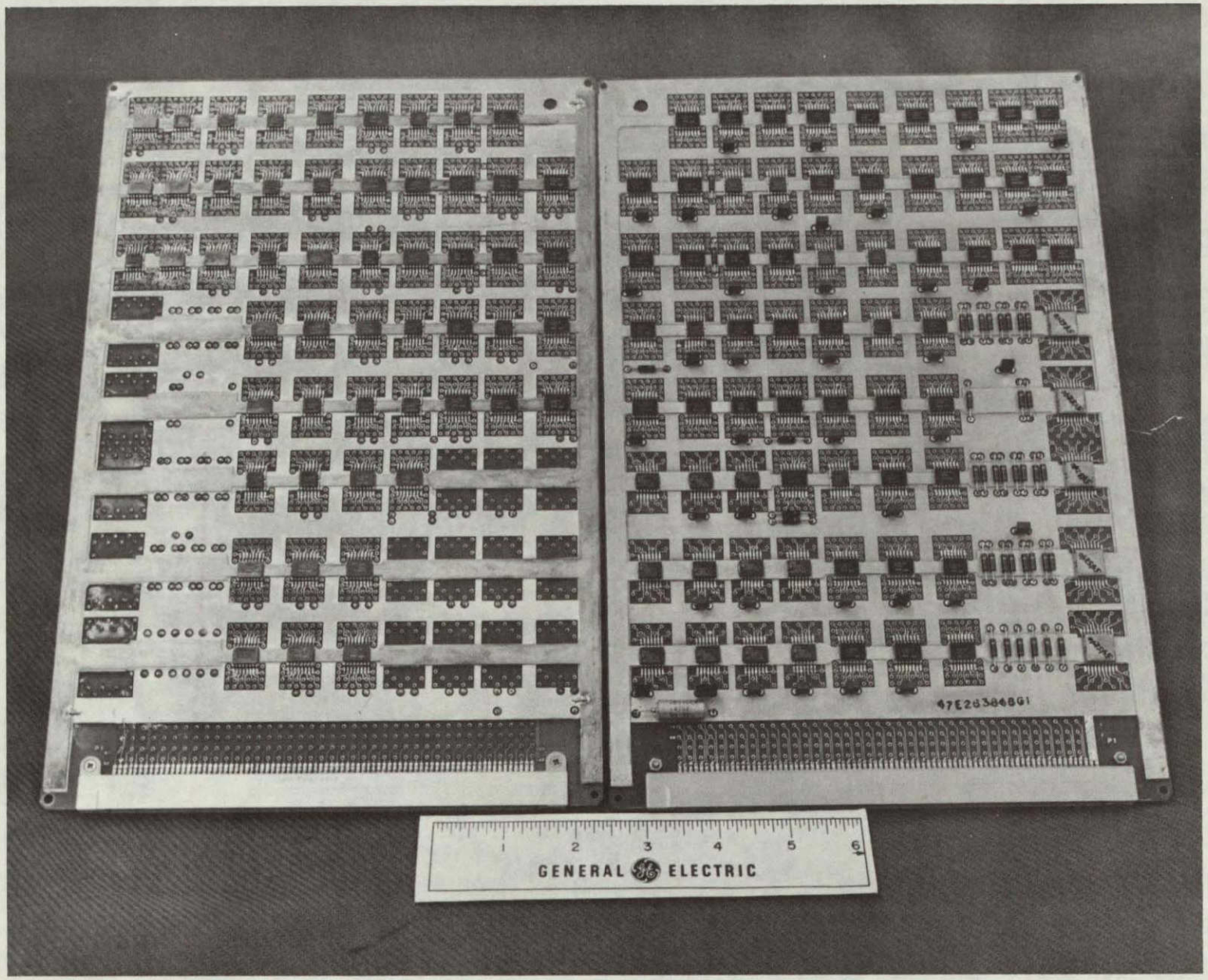


Figure 5.7. POC Control Logic Printed Wiring Assemblies

Figure 5.8. POC Model Switch Matrix (Top)

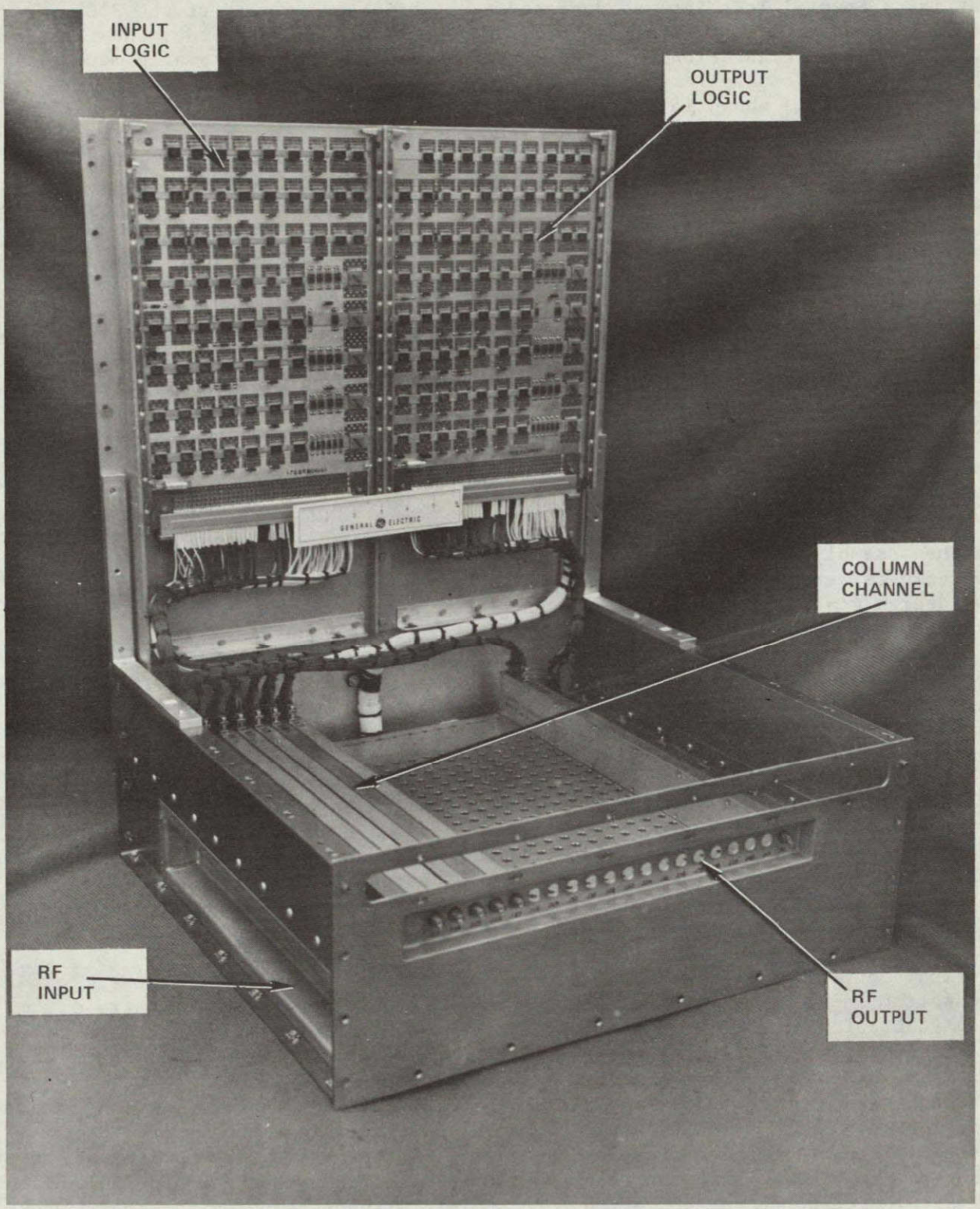


Figure 5.9. POC Model Switch Matrix (Bottom)

5.2 SPECIAL TEST EQUIPMENT

In order to simulate an on-board satellite computer controlling the Switch Matrix, a Special Test Set was designed and fabricated as part of the POC Model Development. This Test Set provides the 32 bit address code, the read pulse, and reconfiguration pulse in either a manual mode or automatic mode. The test set also supplies the DC voltages to the switch matrix. The Special Test Equipment is shown in Figure 5.10.

In the manual mode, one to three crosspoints are addressed by setting the front panel thumb wheel switches to the desired switch crosspoint address. A manually activated read pulse followed by a reconfiguration pulse updates the switch matrix with the new crosspoint data. The selected crosspoints will remain activated until another combination is dialed into the test set. The configuration display indicates which crosspoints are addressed. In the automatic mode, one through sixteen predefined matrices, stored in internal ROM are selected at the front panel. A reconfiguration rate of 2 to 128 useconds may be selected. Once initiated, the test set will automatically transmit the matrix configuration address codes, read pulses, and reconfiguration pulses, repeating the sequence as long as desired. An external word generator may be used with the test set to provide a random reconfiguration sequence in order to simulate an SS-TDMA operating system.

5.3 POC TEST RESULTS

As the assembly of POC model components were completed, Component Acceptance Tests were performed to evaluate performance versus breadboard results and design goals. A summary of this data is shown in Figure 5.11. With the exception of switching speed, the data indicates that the POC model design meets or exceeds the design goal requirements. The difference in switching speed was found to be caused by the narrow range of GaAs FET gate voltage vs. gain at the top of the bias/gain curve. In the off state the GaAs FET gate is biased at -4 VDC, whereby the bias is switched to approximately -0.5 VDC for the on state. Full amplifier turn-on does not occur until the gate bias reaches approximately 95% of its final value. The slope of the turn-on voltage time constant therefore controls the switch on time of the GaAs FET. Switching the GaAs FET off is accomplished within 3 nseconds. This problem can be resolved by additional design effort within the logic switch driver and GaAs FET bias circuits. It was considered a design problem and not a technology problem, therefore rework of the switch crosspoints was not considered cost effective at this time.

As final testing of the POC model proceeded, fractures were found at the crosspoint interconnect tab welds. The tabs are welded to an MIC substrate pad. Gap tolerances between the connector and MIC pads (10 mils) were enough to stress the welds when the channels were plugged in and out of the matrix assembly. To correct this problem, a small ribbon wire service loop was welded between the connector pad and the MIC substrate pad. This fix was implemented in both row and column channels; however, since the interconnect system is a part of the crosspoint bandpass filter, the two ribbon wires added a series impedance within the filter which resulted in detuning of the filter. It was elected to retune 50% of the crosspoints without removing the substrates from the channels because the problem was considered a process problem and not a technology problem. A statistical analysis was completed with new data after retuning the crosspoints and is summarized in Figure 5.12.

Figure 5.10. POC Model Special Test Equipment

	Design Goal	Breadboard	POC
Bandwidth 1 dB (GHz)	1.0-2.5	2.0	1.05
Insertion Loss (dB)	15 (max.)	17	10.7
Off State Isolation (dB)	40 (min.)	65	70
VSWR	1.2 (min.)	1.4	1.2
Switching speed (nsec)	10 (min.)	12	25
Gain Ripple (dB)	1 (max.)	1	0.56
Reconfiguration rate (usec)	2 (max.)	2	2
IF Frequency (GHz)	3-8	6.25	6.5

Figure 5.11. Component Acceptance Tests

SWITCH MATRIX

PERFORMANCE REQUIREMENTS VS POC MODEL RESULTS

TITLE	REQUIREMENT	POC TEST RESULTS
RECONFIGURATION RATE	2 USEC's MAX	2 USEC's
SWITCHING TIME (90% POINTS)	10 NSEC's MAX	24.9 NSEC's
INTERMEDIATE FREQUENCY	3.0 TO 8.0 GHz	6.5 GHz
BANDWIDTH 1 DB	1.0 GHz MIN	0.95 GHz
GAIN RIPPLE (OVER BW)	1.0 DB MAX	1.1 DB
PHASE LINEARITY DEVIATION	$\pm 5^{\circ}$ MAX	8.9°
INSERTION LOSS	15 DB MAX	16.1 DB
ISOLATION	40 DB MIN	>75 DB
IMPEDANCE (INPUT/OUTPUT)	50 OHMS	50 OHMS
VSWR (INPUT)	1.2 MAX	1.3
VSWR (OUTPUT)	1.2 MAX	1.4
SIGNAL TO NOISE	35 DBC MIN	50 DBC
INTERMOD DISTORATION	35 DBC MIN	52 DBC
1 DB GAIN COMPRESSION	N.A.	0 DBM
SIZE	16" x 16" x 6"	16.6" x 18.6" x 6.6"
MATRIX SIZE	20 x 20 MECH 57 ACTIVE CROSS-POINTS	20 x 20 MECH 57 ACTIVE CROSSPOINTS 1 WRAPAROUND PATH
POWER	NA	33 W
WEIGHT	NA	35 LBS

Figure 5.12. POC Model Switch Matrix Test Summary

SECTION 6.0

RELIABILITY PROJECTIONS

A reliability model and analysis was completed for the 20 x 20 IF Switch Matrix during the Task I study. An update of the preliminary reliability studies was undertaken after completion of the POC model design. The basic change is the incorporation of the microwave switch crosspoint design utilized in the POC model. Since a discrete IC design was used in the POC model for the control and switch driver logic, and an LSI custom design would be used for the flight model, the original logic circuit assumptions used for the preliminary analyses are valid for this update.

The revised Probability of Success model is shown in Figure 6.1. It consists of three major parts: input/output microwave coax connectors, redundant row and column decoders, and the switch matrix. The switch matrix includes the control logic memory latches, switch drivers, GaAs FET switches, and the crosspoint interconnects. Based on the model, the total IF Switch Matrix probability of success for a ten year mission life is a function of the number of wraparounds. A computer program was developed to determine the switch matrix reliability versus the number of wraparounds for different failure patterns. A summary of the computer analysis is shown in Figure 6.2. With zero wraparounds the probability of success (P_{SW}) for the switch crosspoints is 0.30065 with a resulting probability of success for the complete switch matrix (P_M) 0.29483. As the number of wraparounds increase, P_{SW} increases with a corresponding increase of P_M; however, when five wraparounds are considered, the incremental change of P_M becomes limited by the probability of success of the input/output coax connectors (P_C) and not by P_{SW}.

For a future flight model, the number of wraparounds used would be based on system requirements and the resulting probability of success assigned to the IF Switch Matrix.

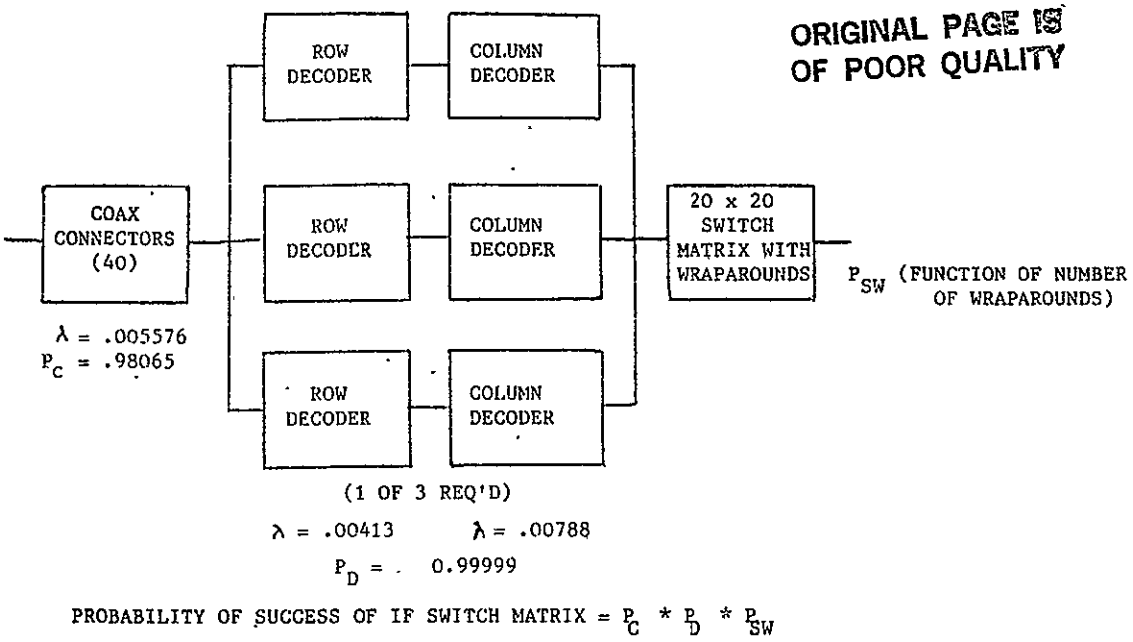


Figure 6.1. Flight Model Reliability Model

$$P_m = P_C * P_D * P_{SW}$$

No. of Wraparounds	P_C	P_D	P_{SW}	P_M
0	0.98065	0.99999	0.30065	0.29483
1			0.68172	0.66853
2			0.90154	0.88408
3			0.97822	0.95929
4			0.99606	0.97678
5			0.99848	0.97916

P_C = Coax Connectors
P_D = Row & Column Decoders
P_{SW} = Switch Crosspoints
P_M = Switch Matrix

Figure 6.2. Probability of Success vs Number of Wraparounds for 10 Years

SECTION 7

1987 100 x 100 SWITCH MATRICES

Task II studies evaluated projected technologies that would be available by 1987 for the development of large scale (100 x 100) high speed data switching at both microwave IF frequencies and at baseband. The first sub-task, for both designs, was an Architecture and Switch Device study which evaluated and compared the projected technologies for an optimum architecture, switch device, and control logic, that would meet the requirements of a 100 x 100 switch matrix. Next a Parametric Tradeoff analysis was completed between functional performance, matrix size, and reliability in order to determine the optimum design approach. Utilizing the results of the first two sub-tasks, a final design concept was developed for both IF and Baseband switch matrices.

Included in this study was a Switch Matrix Comparison which compared the Large IF Switch Matrix to the Large Baseband Switch Matrix. To make the comparison meaningful, the baseband switch included the modems required for an IF to baseband translation. A second comparison was made of the Large IF Switch Matrix to a scaled up version of the 20 x 20 IF Switch Matrix, utilizing 1982 technology.

7.1 100 X 100 IF SWITCH MATRIX

The coupled crossbar architecture was selected as the optimum architecture based on functional performance, expandability of design, and reliability. GaAs MESFET technology was determined to be best for wideband, high speed switching devices. The optimum approach was the integration of both the control logic and microwave switching devices into GaAs MESFET substrates utilizing Monolithic Microwave Integrated Circuit (MMIC) technology. Since state of the art processing restricts the useful size of GaAs substrates, an approach to the design of a 100 x 100 switch matrix was the development of smaller 12 x 12 submatrices.

Figure 7.1 indicates the concept of assembling sixty-four 12 x 12 submatrices into a resulting 96 x 96 Switch Matrix.

Reliability analysis concluded that the optimum submatrix design would include four internal wraparounds rather than redundancy around the complete 96 x 96 matrix (Figure 7.2). Each crosspoint would include a two stage microwave switch/amplifier isolated from the input/output lines with 20 db couplers. To achieve the full size reduction offered by MMIC technology, high reliability active couplers must be developed to replace the larger quarter-wave high reliability passive couplers. For reliability, redundant logic switch drivers were included in the crosspoint design (Figure 7.3). A switch crosspoint MMIC layout, Figure 7.4, indicates a design using passive couplers. A metal plate is shown between the upper and lower GaAs substrates. This would provide isolation, reducing the possibility of unwanted input line signals leaking through to the output lines. The complete two stage switch/amplifier and redundant control logic would be fabricated on the upper substrate. A feedthru connection would transfer the signal to the lower substrate which contains the output coupler and output transmission line.

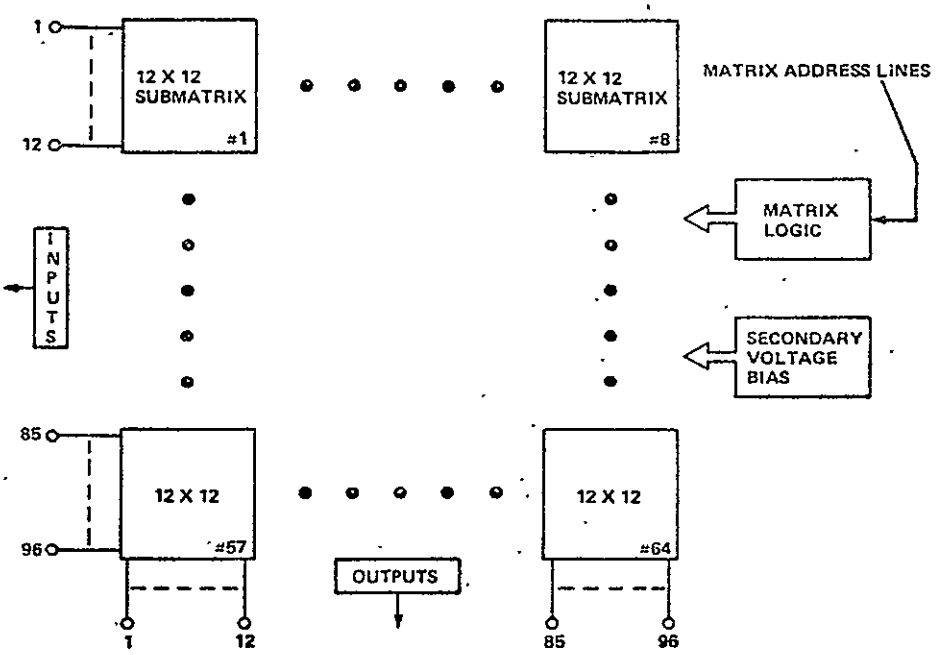


Figure 7.1. 96 x 96 Switch Matrix

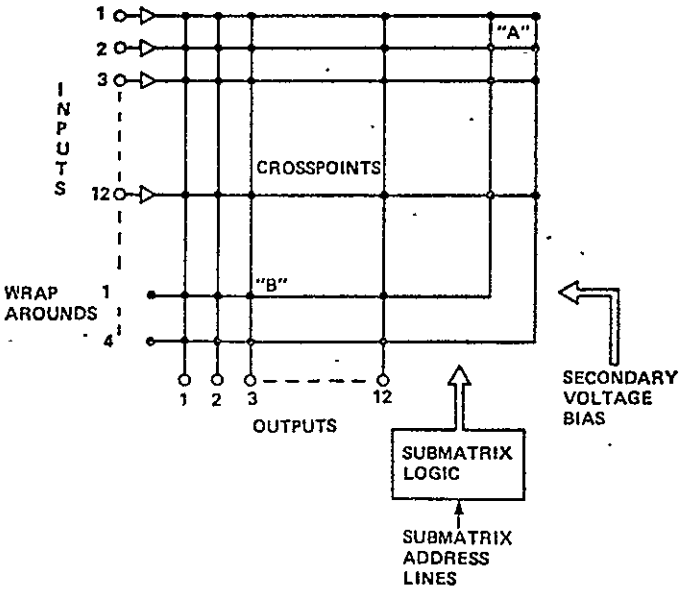


Figure 7.2. 12 x 12 Submatrix

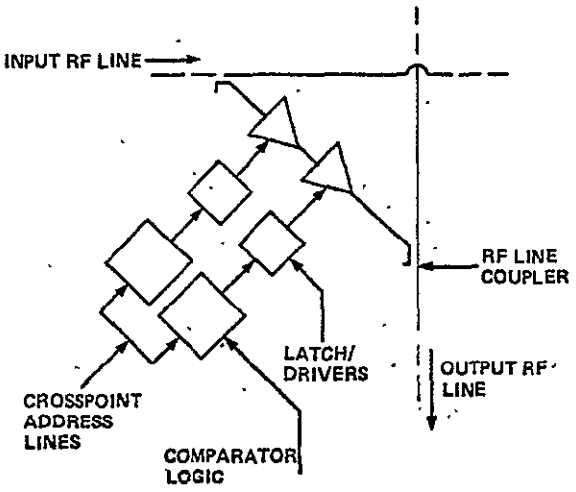


Figure 7.3. Switch Crosspoint Block Diagram

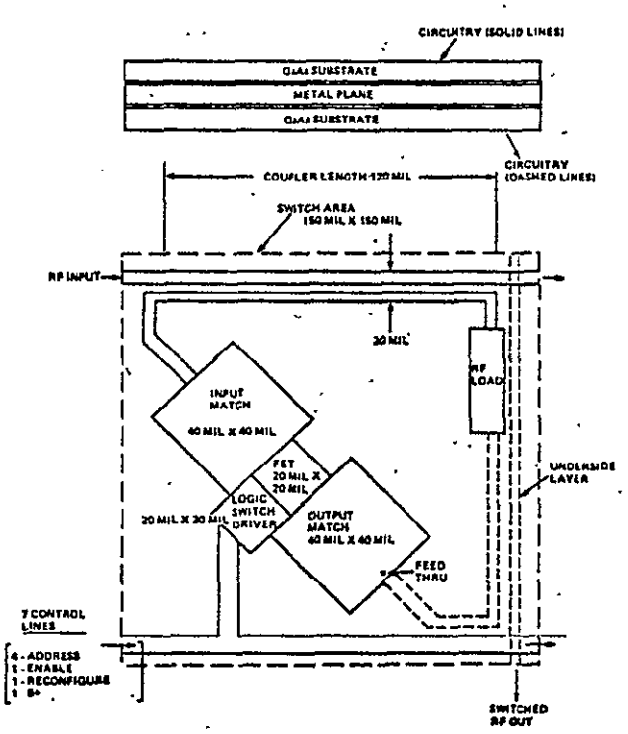


Figure 7.4. Switch Crosspoint MMIC Layout

7.2 100 X 100 BASEBAND SWITCH MATRIX

The optimum architecture for the 100 x 100 Baseband Switch Matrix is the same as the coupled crossbar method developed for the IF Switch Matrix. Sixty-four 12 x 12 submatrices would be assembled into a 96 x 96 matrix structure. At baseband, CMOS technology would be best for integration of the analog switching devices and control logic. Reliability studies concluded that at baseband, redundancy would be best implemented at the crosspoint, which would therefore eliminate the four wraparound paths within each submatrix.

The redundant crosspoint, Figure 7.5, consists of cascaded switchable dual gate CMOS FETS, two of them in parallel. The redundant crosspoint amplifiers are passively coupled to the input/output lines via 23 db resistive line couplers. Separate latch/driver and comparator logic circuits for each amplifier are driven in tandem at the crosspoint address lines.

7.3 SWITCH MATRIX COMPARISON

Summary results of the comparison between the large IF and the large baseband switch matrices are shown in Figure 7.6. The baseband switch was made functionally equivalent to the large IF switch by adding a QPSK modem to each channel. No significant difference in performance exists between the two implementations. However, a severe penalty is paid in the baseband approach in terms of power consumption, reliability, size and weight. The large IF switch is clearly the preferred choice unless significant system advantages accrue from having the data at baseband.

For the next comparison, the 1982 20 x 20 POC Model IF Switch Matrix was scaled up to a 96 x 96 matrix. It was then compared to the 1987 large IF Switch Matrix, with the results shown in Figure 7.7. Allowing for some differences in performance characteristics, the large IF switch and the scaled-up POC model were roughly equivalent except for size, weight, and reliability. The scaled POC model is much larger and heavier because of the discrete technology employed in its implementation. The large IF switch matrix is clearly the preferred design.

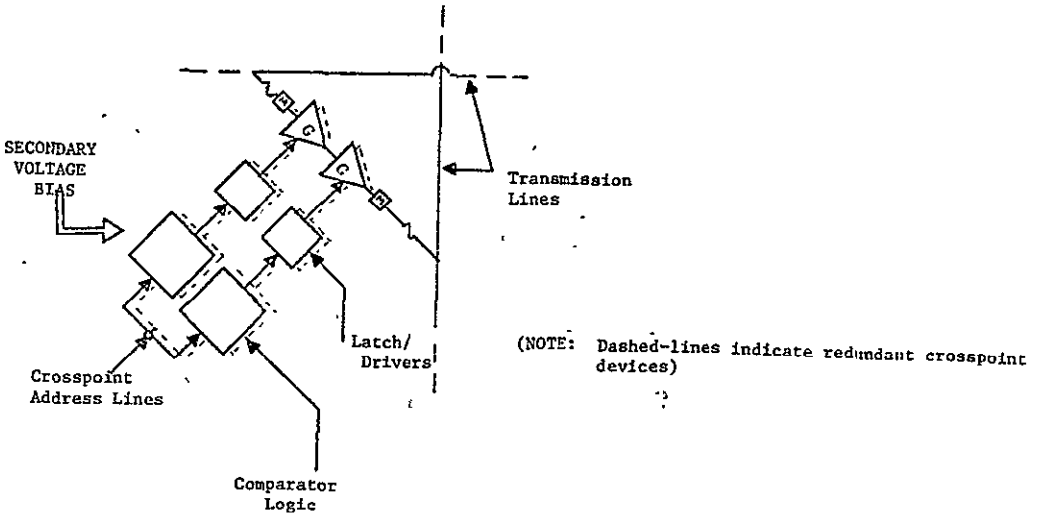


Figure 7.5. Baseband Switch Matrix Crosspoint Block Diagram

Parameter	Large IF Switch	Baseband Switch	Baseband Switch plus QPSK Modems
Matrix size	96 x 96	Same	Same
Connectivity	Any of the inputs to any of the outputs. One for one.	Same	Same
Reconfiguration rate	< 2 microseconds	Same	Same
Switching time	< 10 nanoseconds	< 10 nanoseconds	< 12 nanoseconds
Computer interface	61 lines	Same	Same
Electrical performance			
Input signal level	-5 ± 5 dBm	-6 ± 5 dBm	-5 ± 5 dBm
Frequency spectrum	8 ± 0.25 GHz	25 to 500 MHz	8 ± 0.25 GHz
Flatness	± 1 dB	± 1 dB	< ± 1 dB
Phase linearity	± 5° max.	± 50 max.	N/A
Isolation	> 40 dB all inputs Equal signal strength	> 42 dB all inputs Equal signal strength	Negligible S/N degradation
Insertion loss	30 dB max.	32 dB max.	32 dB max.
Noise	> 35 dB below output signal level	> 35 dB below output signal level	N/A
Intermodulation (3rd order)	- 30 dB Two equal tones	- 34 dB Two equal tones	N/A
Impedance (input/output)	50 ohms	Same	Same
VSWR (input/output)	1.2:1	Same	Same
Power consumption	129.3 watts	63 watts	500 to 1000 watts
Reliability (10 year mission)	0.76867	0.91019	0.3998* (Redundant Modems)
Mechanical			
Size	12 x 12 x 2 in.	10.5 x 10.5 x 3.5 in.	10 x 10 x 15 in.*
Weight	11.5 lbs	12.7 lbs	60 lbs.
Projected costs			
Hardware development	$3.1 million	$3.1 million	$4.5 million
New technology	$4.58 million	$4.21 million	$6.3 million
Scaleability beyond 96 x 96	Feasible with degraded performance	Same	Same
Growth to larger bandwidth	Same as above.	Same	Same
Operating temperature	-10°C to +50°C	Same	Same

*Based on a ground equipment design (DSCS III QPSK BER Test Equipment) reconfigured for flight operation.

Figure 7.6. Large IF vs. Baseband Switch Matrix

Parameter	Large IF Switch	POC Model	POC Model Scaled Up
Matrix size	96 x 96	20 x 20	96 x 96
Connectivity	Any of the inputs to any of the outputs. One for one.	Same	Same
Reconfiguration rate	< 2 microseconds	Same	Same
Switching time	< 10 nanoseconds	Same	Same
Computer interface	61 lines	100 lines	700 lines
Electrical performance			
Input signal level	-5 ± 5 dBm	0 ± 5 dB	0 ± 5 dB
Frequency spectrum	8 ± 0.25 GHz	(5.5 to 7.85) ± 1.25 GHz	(5.5 to 7.85) ± 0.5 GHz
Flatness	± 1 dB	± 1 dB/2.5 GHz, ± 0.5 dB/ 500 MHz	± 1 dB/1.0 GHz
Phase linearity	± 5° max.	Same	Same
Isolation	> 40 dB all inputs	> 40 dB all inputs equal signal	> 33 dB - same crosspoint signal strength
Insertion loss	30 dB max.	15 dB max.	21 dB max.
Noise	> 35 dB below output signal level	Same	Same
Intermodulation (3rd order)	- 30 dB Two equal tones	- 35 dB Two equal tones	- 35 dB Two equal tones
Impedance (input/output)	50 ohms	Same	Same
VSWR (input/output)	1.2:1	Same	Same
Power consumption	129.3 watts	8 watts	44 watts
Reliability (10 year mission)	0.76867	≃ 0.97	≃ 0.751
Mechanical			
Size	12 x 12 x 2 in.	485 in^3	12,000 in^3
Weight	11.5 lbs	20 lbs.	500 lbs.
Projected costs			
Hardware development	$3.1 million	$1.3 million	$12.7 million
New technology	$4.58 million	None	None
Growth to larger bandwidth	Feasible with degraded performance.	Same.	Same
Operating temperature	-10°C to +50°C	Same	Same

Figure 7.7. Large IF vs. POC Model Switch Matrix

SECTION 8

FUTURE TECHNOLOGY DEVELOPMENT

8.1 REDUNDANCY MANAGEMENT

Redundancy management is a major technology issue which, while briefly addressed in the Task I studies, must be fully resolved preparatory to operational use of the system. In particular, for the Switch Matrix, corrective action in the event of a failure must be promptly implemented to avoid unacceptable operational down-time.

The principal feature by which the matrix realizes the desired reliability is through wraparound circuitry. Thus, redundancy management entails continual on-board self test to:

1. Determine if a crosspoint has failed
2. Locate the failed crosspoint
3. Determine which wraparound paths are available
4. Reroute signal traffic from the failed crosspoint through the selected wraparound path to the desired output.

There are two methods of implementing the control or intelligence function of the self test system, namely: (1) use of the on-board computer to control decision functions, and (2) a microprocessor integrated in the matrix. The on-board computer could determine when to test the switch matrix and which wrap-around to employ. Alternatively the switch matrix could embody its own internal control capability by use of an integrated microprocessor to control the self test function. This would make the switch matrix entirely self-contained.

Study of redundancy management should address how frequent and the optimal time to test to minimize traffic interruptions. In addition, an algorithm for control of the self test system needs to be developed and demonstrated. A suggested plan for the study of such a self test approach is shown in Figure 8.1. The 5 x 5 Breadboard Switch Matrix could be utilized for the self test proof of concept model, to minimize study costs.

A block diagram of a candidate self test system concept is shown in Figure 8.2. A test oscillator, stepped automatically, injects a signal into each input row of the switch matrix. A detector measures the signal at each column output. The detected signal is compared to determine if a specific switch matrix crosspoint has failed.

A column is added to the switch matrix for injection of a test oscillator signal into the input rows, and a row is added for coupling the switch matrix test signal from a desired output column to the detector circuit. An amplifier may also be required to compensate for the insertion loss of the extra switches within the switch matrix path. The wraparound paths would also be tested. The switch matrix is tested by sequentially connecting the appropriate oscillator column switch and the appropriate detector row switch to the switch crosspoint

- SYSTEM DESIGN FOR SS-TDMA TRAFFIC
  - FREQUENCY OF TEST
  - WHEN TO TEST
  - INTERNAL OR EXTERNAL ROUTING CONTROL
- ALGORITHM
- DESIGN POC MODEL

  INTEGRATE WITH 5 X 5 BREADBOARD SW MATRIX
- FABRICATE AND TEST POC MODEL
- STUDY FLIGHT MODEL IMPLEMENTATION

Figure 8.1. Redundancy Management Suggested Study Plan

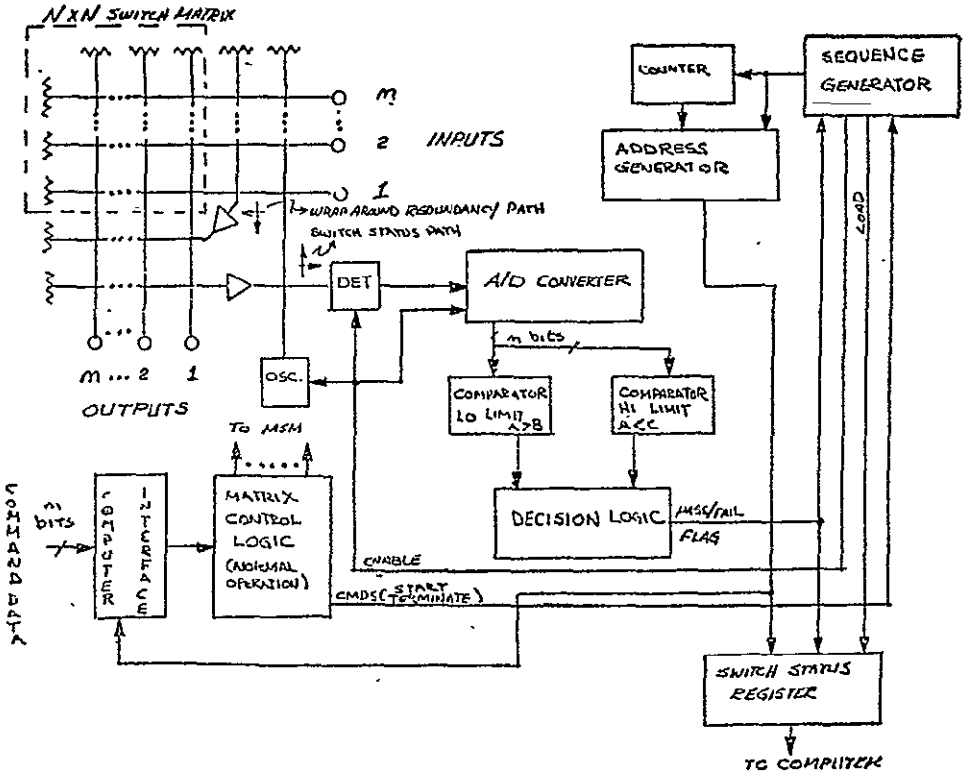


Figure 8.2. Block Diagram of a Conceptual Self Test System

under test. Absence or deterioration of the desired detector output would flag the control logic and indicate a failed crosspoint.

The oscillator-detector operation can also be checked independent of the switch matrix. The total communications system could be tested by monitoring uplink signals at the detector, and by generating downlink signals with the test oscillator appropriately modulated.

During normal switch matrix operations, command data from the on-board computer defining the matrix configuration passes through the interface circuitry and is acted upon by the Matrix Control Logic. The matrix control logic establishes the switch matrix configuration. For the self test feature, the control computer could issue a command via the command data base, to initiate self test. That command is decoded in the matrix control logic and initiates a start signal to the sequence generator. The sequence generator initializes the program counter to a known starting state, thus enabling the oscillator and detector. The address generator establishes the routing of the test signal from the oscillator through the matrix to the detector. The output of the detector is digitized in an A/D converter. The digital signal is then compared with high and low limit references for acceptability. The output should fall within this range or the switch is considered failed. Decision logic determines the results of the comparison and issues a Pass/Fail Flag to the sequence generator. If a failure is identified, the sequence generator loads the address location of the failed switch and a fail status bit to the switch status register for transfer to the computer.

8.2 MONOLITHIC MICROWAVE INTEGRATED CIRCUITS

A major technology issue for future high capacity switch matrices is the development of an appropriate monolithic microwave integrated circuit (MMIC) including both the microwave switch crosspoints and associated control logic as discussed in Section 7 of this report. The key technology advancements required to realize such an MMIC switch matrix design suitable for eventual flight realization are summarized as follows:

- A mature high reliability GaAs MMIC process suitable for both RF switch and high speed logic implementation into a common chip.
- The development of high isolation multilayer substrate techniques for fabricating switch crosspoints.
- The development of high quality RF submatrix and large numbers of input/output connections.
- The development of a 12 x 12 submatrix building block embodying high-isolation RF transmission lines and passive distributed couplers, with large area GaAs wafer construction up to approximately two square inches. Active device matching should also be evaluated.

A development program for an MMIC Switch Matrix should include a comparative study of passive and active couplers. Improving the reliability of active couplers for spare missions would be extremely valuable since high reliability active couplers are required to realize the full miniaturization potential of MMIC designs.

General Electric, Valley Forge Space Center, has recently achieved promising results in the design and fabrication of a two stage GaAs MMIC switch/amplifier for use in switch matrix designs. This effort was completed with IR&D funds. This technology achievement can be extended to the integration of a complete switch crosspoint, including couplers, microwave switch, and control logic. Further evolution would include development of an MMIC 4 x 4 fully integrated switch matrix, followed by the development of a complete 12 x 12 GaAs submatrix, including four wraparounds for redundancy.

SECTION 9

CONCLUSION

This multi-year Switch Matrix program, sponsored by NASA Lewis Research Center as a part of their Advance Communications Satellite Technology Program, has culminated in the development of a Proof of Concept Model 20 x 20 IF Switch Matrix utilizing 1982 technology. The IF Switch Matrix was one of the identified key technologies that was to be developed in order to realize future operational high capacity, multibeam, high speed switching, satellite communications systems.

For both 1982 and 1987 IF Switch Matrix implementation, the coupled crossbar matrix was selected as the optimum architecture. Loose signal coupling ($>$ 15 db) of the switch crosspoints to the input and output transmission lines prevents both main lines from being disabled in the case of a switch crosspoint failure that results in a short to ground. Therefore, single point failures of a complete input row or output column are eliminated.

To achieve a package size which provides a reasonable weight and volume for spacecraft applications, the IF frequency has been chosen to be as high as possible. Within the constraints imposed by the various design goal requirements, the 5.0 to 7.5 GHz band was selected as the optimum IF frequency. The goal of achieving 2.5 GHz bandwidth also favors a high center frequency where the percentage bandwidth is minimized for best possible amplifier stage matching.

A dual gate GaAs FET was the selected device for microwave crosspoint switching. Good on/off gain ratios provide the required off state isolation. Low power gate switching and low on state drain current requirements are most favorable when operating the switch matrix from a limited power battery system. The dual gate FET does exhibit a higher output Q than the single gate FET, therefore resulting in a gain bandwidth compromise. GaAs FETs also exhibit high speed switching capabilities which meets the system switching requirements.

The switch crosspoint consists of a two stage dual gate GaAs FET switch/amplifier providing approximately 19 db gain. This gain reduces the combined input/output 30 db coupler losses to a typical crosspoint insertion loss of 11 db. Independent logic switch drivers are used to control the on/off state of the cascaded GaAs FETs. Redundant logic switch drivers were chosen to eliminate single point failures in either of the GaAs FETs or in the logic switch drivers.

The selected computer interface for switch crosspoint addressing is a 32 bit parallel code. The 32 bit interface, which is TTL compatible, was selected because it is a logical extension of current computer architecture and offered an optimum design in the areas of speed and interconnections when alternate options were studied. The control logic design provides redundancy for the elimination of single point failures.

For a flight model design, a custom CMOS LSI was the selected control logic device technology. The logic design is partitioned so that only two basic custom LSI chips are required. To prove feasibility of the control logic design, discrete components were used in the Proof of Concept model to reduce

development costs. Fabrication of the custom LSI chips were not considered to be a technology issue.

The switch matrix packaging design features an integrated modular approach utilizing individual input and output channel modules which are connected by an RF interconnect system. I-beam construction of the channel modules separates and isolates the microwave switch circuits from the logic control circuitry. The channel modules are mounted to a base plate with the input row channels on one side of the base plate, and the output column channels mounted orthogonally on the reverse side. The base plate aides in the alignment of the channel modules, and becomes a part of the input/output crosspoint microwave interconnect system.

In summary, results of the 20 x 20 Switch Matrix Proof Of Concept Model indicates that the design is feasible for application in a multichannel SS-TDMA communications system. Expandability, a design goal requirement, for switch matrices of sizes other than 20 x 20 can be readily achieved with this design. Gain bandwidth products of available GaAs FETs for the microwave switch crosspoint would be the limiting component for switch bandwidth and insertion loss requirements of an operational transponder.

Reliability of the switch matrix for a ten-year mission life would be a function of the size of the matrix and the number of wraparounds required to meet the reliability figure allocated to the switch matrix by transponder tradeoff studies. It is concluded from the Proof Of Concept model efforts that wideband, high speed switching is practicable for flight model application utilizing 1982 technology.

Results of the 1987 100 x 100 IF Switch Matrix conceptual design study illustrates an approach to the future requirements of a high capacity, wideband SS-TDMA switch matrix. The design approach stresses high reliability to assure a mission life of ten years.

GaAs Monolithic Microwave Integrated Circuits are key technologies to be developed to realize such high capacity switch matrices. Integration of the control logic into the GaAs substrate is essential to meet the high speed switching requirements. High reliability active couplers, to replace the passive couplers, must be included in the GaAs substrate development in order to achieve full miniaturization advantages of monolithic circuits.

NASA CR-168089

SPACECRAFT IF SWITCH MATRIX FOR WIDEBAND SERVICE APPLICATIONS IN 30/20 GHz COMMUNICATION SATELLITE SYSTEMS FINAL REPORT

GENERAL ELECTRIC COMPANY

PREPARED FOR

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

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15. Supplementary Notes

16. Abstract

This report describes the design and fabrication of a 20 x 20 Satellite Switched - Time Division Multiple Access (SS-TDMA) IF Switch Matrix for application in a 30/20 GHz Communications Satellite. Development of this 3-8 GHz switch matrix was sponsored by NASA Lewis Research Center as a part of their Advanced Communications Satellite Technology Program. The switch matrix was one of several key technologies requiring development to realize wideband, high capacity satellite communications systems for the 1990's.

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SECTION 1.0

SUMMARY

This report presents a summary of the Proof Of Concept (POC) Model Switch Matrix test results and analysis. Results of the Component Acceptance tests and the integrated Switch Matrix tests are included. Component Acceptance tests were performed on each of the Microwave Integrated Circuit (MIC) crosspoints after they were assembled and tuned. Special test fixtures were fabricated to house the two stage GaAs FET switch crosspoint. The MIC circuits were readily tuned and tested in these fixtures. Once tested, the MIC substrates were assembled into the row and column channel assemblies. The logic switch drivers were tested at the printed wiring board level, prior to integration with the MIC crosspoints. Each of the two control logic printed wiring boards were independently tested in the Switch Matrix assembly. Once the channel assemblies and control logic boards were assembled into the Switch Matrix, testing of the complete system commenced.

As final testing of the POC model proceeded, fractures were found at the crosspoint interconnect tab welds. The tabs are welded to an MIC substrate pad. Gap tolerances between the connector and MIC pads (10 mils) were enough to stress the welds when the channels were plugged in and out of the matrix assembly. To correct this problem, a small ribbon wire service loop was implemented in both row and column channels; however, since the interconnect system is a part of the crosspoint bandpass filter, the two ribbon wires added a series impedance within the filter which resulted in detuning of the filter. It was elected to retune 50% of the crosspoints without removing the substrates from the channels because the problem was considered a process problem and not a technology problem. A statistical analysis was completed with new data after retuning the crosspoints.

A statistical analysis was completed for both the Component Acceptance and integrated Switch Matrix test data. This analysis evaluates anticipated performance of a fully populated 20 x 20 Switch Matrix (400 crosspoints) based on parameter data from the 61 populated crosspoints of the POC model. Standard statistics of the mean, standard deviation, and range were provided. Included are confidence limits of a two-sided interval for the population mean. A Confidence level of 95% is shown which results in an Alpha risk of 2.5%. Prediction limits to contain the next observation, and approximate tolerance limits to contain 95% of the population are also provided using a 95% confidence level. A histogram is presented to illustrate the actual recorded data.

Table 1.1 compares the design goal requirements to summary data of the breadboard and POC model manufacturing test results. The POC data are the average results of the MIC crosspoints before integration into the Switch Matrix.

Table 1.1. Test Comparison

	Design Goal	Breadboard	POC Model
Bandwidth 1 dB (GHz)	1.0-2.5	2.0	1.05
Insertion Loss (dB)	15 max.	17	10.7
Off State Isolation (dB)	40 min.	65	70
VSWR	1.2 min.	1.4	1.2
Switching Speed (nsec)	10 min.	12	25
Gain Ripple (dB)	1 max.	1	0.56
Reconfiguration Rate (usec)	2 max.	2	2
IF Frequency (GHz)	3-8	6.25	6.5

During the breadboard phase, 2.0 GHz bandwidth was achieved at a sacrifice of insertion loss. A tradeoff between gain vs. bandwidth was completed in order to improve insertion loss of the switch crosspoints. Gain bandwidth is primarily a function of the GaAs FET device. It was decided to redesign the POC model crosspoint for a bandwidth of 1.3 GHz at an insertion loss of 11 dB. Results of the tradeoff are indicated in Table 1.1. Switching speed measurements were made after integration of all crosspoints into the POC model.

The major performance design goal requirements are shown in Table 1.2 with integrated POC model test results, after resolution of the channel interconnect problem. Retuning the MIC crosspoints did not fully achieve the original bandwidth and insertion loss results. Because the problem was process design related and not a technology problem, it was not economically feasible to remove the crosspoints from the channels in order to retune the crosspoints to the original test results. Table 1.2 indicates the test results after retuning 30 of the crosspoints.

Table 1.2. Performance Requirements vs. POC Model Results

TITLE	REQUIREMENT	TEST RESULTS
RECONFIGURATION RATE	2 USEC's MAX	2 USEC's
SWITCHING TIME (90% POINTS)	10 NSEC's MAX	24.9 NSEC's
INTERMEDIATE FREQUENCY	3.0 TO 8.0 GHz	6.5 GHz
BANDWIDTH 1 DB	1.0 GHz MIN	0.95 GHz
GAIN RIPPLE (OVER BW)	1.0 DB MAX	1.1 DB
PHASE LINEARITY DEVIATION	$\pm 5^{\circ}$ MAX	8.9°
INSERTION LOSS	15 DB MAX	16.1 DB
ISOLATION	40 DB MIN	>75 DB
IMPEDANCE (INPUT/OUTPUT)	50 OHMS	50 OHMS
VSWR (INPUT)	1.2 MAX	1.3
VSWR (OUTPUT)	1.2 MAX	1.4
SIGNAL TO NOISE	35 DBC MIN	50 DBC
INTERMOD DISTORATION	35 DBC MIN	52 DBC
1 DB GAIN COMPRESSION	N.A.	0 DBM
SIZE	16" x 16" x 6"	16.6" x 18.6" x 6.6"
MATRIX SIZE	20 x 20 MECH 57 ACTIVE CROSS-POINTS	20 x 20 MECH 57 ACTIVE CROSSPOINTS 1 WRAPAROUND PATH
WEIGHT	N/A	35 LBS
POWER	N/A	33 W

SECTION 2.0

PROOF OF CONCEPT MODEL DESIGN

Studies of available technologies and design trades led to the conceptual design of a 20 x 20 IF Switch Matrix utilizing 1982 available technology. To show feasibility a 20 x 20 Proof Of Concept (POC) Model was fabricated and tested. The POC Model was physically the size of a full 20 x 20 matrix but only partially populated with 57 carefully chosen active crosspoints to reduce development costs while still validating the concept. One wraparound network with 4 crosspoints was also included to demonstrate redundancy.

The 20 x 20 IF Switch Matrix was developed to operate in an SS-TDMA communications system. Ground signals transmitted to the satellite at 30 GHz, are received through a multibeam antenna and receiver system, and down converted to the switch IF at 6.5 GHz. An on-board computer provides a 32-bit address code to the switch matrix which defines the switch matrix configuration. Once reconfigured, the IF input signals are routed to the appropriate outputs. The output signals are then up-converted to 20 GHz and transmitted via the multibeam antenna to the ground.

A coupled crossbar matrix with a constant coupling ratio of 15.2 dB for all couplers was the selected architecture (Figure 2.0). Its primary advantages are: (1) absence of single point switch matrix failure modes and (2) readily implemented redundancy with wraparound techniques. The basic elements of the switch matrix include 50-ohm Input Transmission Lines from which signals are coupled by the 15.2 dB Input Couplers and applied to a two-stage microwave Switch/Amplifier. The switc state is controlled by the switch matrix Logic System. When a specific switch is activated the microwave signal is coupled from the main transmission line, amplifi approximately 20 dB and coupled through the 15.2 dB Output Coupler to the Output Transmission Line. In the following sections, additional details of the switch mat elements are discussed.

2.1 MICROWAVE

A block diagram of the microwave switch/amplifier crosspoint is shown in Figure 2.1. The input and output directional couplers are edge-coupled microstrip lines etched on 0.025" alumina substrate. The terminations are thin film tantalum nitride resistors with a two-section matching network to achieve greater than 25 dB return loss from 180 MHz to 8 GHz. Coupler impedance is 50.7 ohms with -15.2 dB coupling. The inherent low directivity of the microstrip coupler required that all reflections be minimized so that the ripple in the coupling response and the mainline VSWR remain within acceptable limits. Analysis indicated that couplers with 15 dB insertion loss on both input and output lines would provide adequate isolation in the event of a short to ground within the microwave switch circuitry.

A dual gate GaAs FET was chosen as the switch device because of its high gain, high isolation, high speed switching, and low power switching capabilities. Selection of the critical gain-bandwidth product was complicated by the high input/output Q of the GaAs FET devices. Amplifier tuned elements and bias lines were etched on alumina substrates. Thin film series resistors were used for gain ripple damping and amplifier stabilization. Packaged GaAs FET devices were used to avoid hermetic sealing of the row or column channels. The GaAs FET device, coupler substrate, and amplifier substrates are mounted to a kovar carrier as shown in Figure 2.2. This carrier assembly forms half

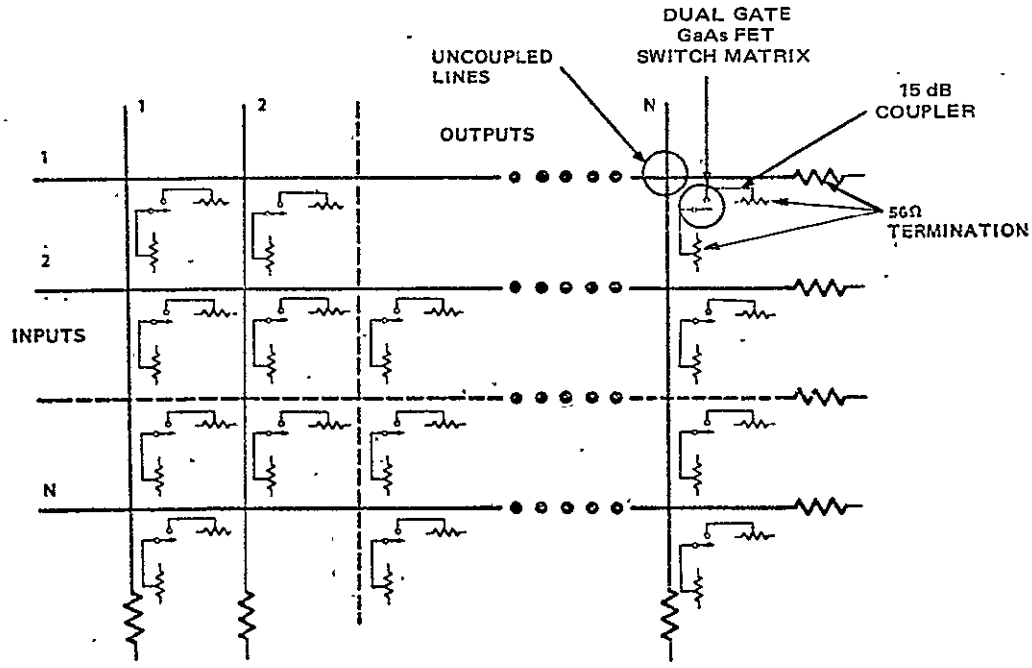


Figure 2.0. Coupled Crossbar Architecture

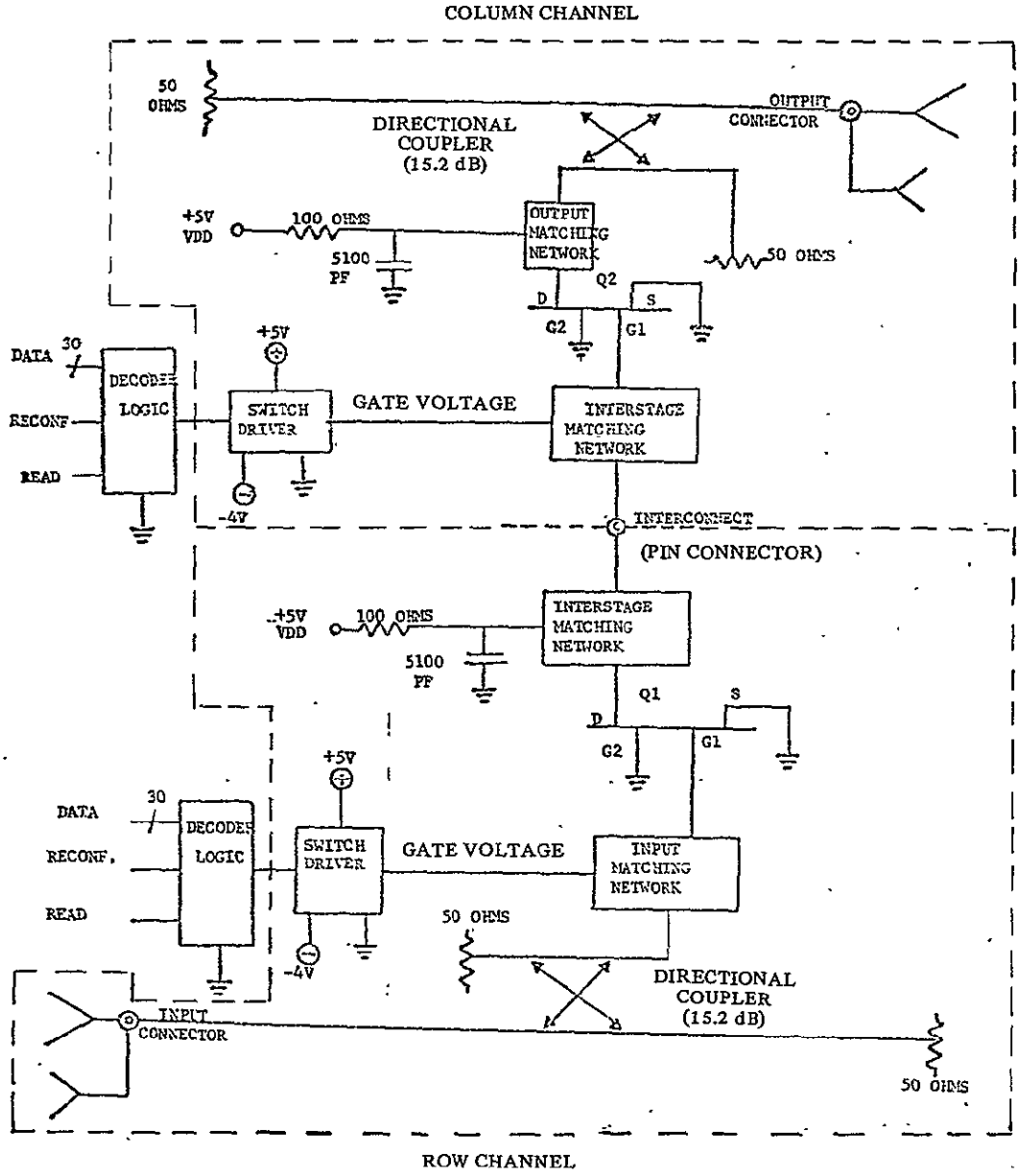


Figure 2.1. Crosspoint Block Diagram

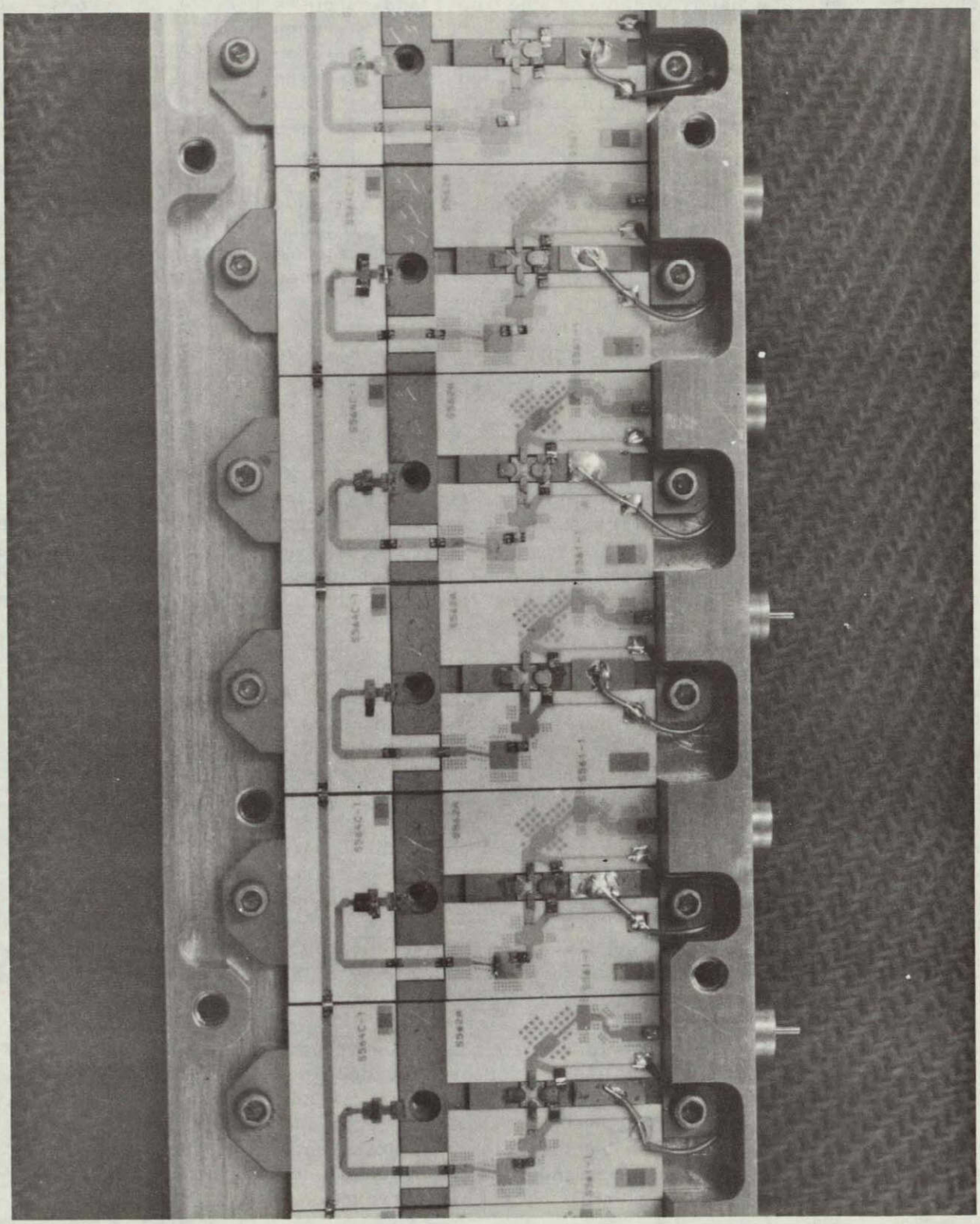


Figure 2.2. MIC Carrier Assembly

of the switch crosspoint. The input amplifiers are assembled into the switch matrix input row channels, and the output amplifiers are assembled into the output column channels. The POC Model output channel assembly in Figure 2.3 shows twenty output amplifier carriers plus one amplifier for the wraparound path. The interface used to connect the input and output stages of the crosspoints is provided by a connector wall insert which is seen along the upper edge of the channel assembly in Figure 2.3. This interconnect system permits an in-line test fixture configuration for tuning of the input/output amplifiers prior to their assembly into their respective row or column channel assemblies. Once assembled into the channels, the interconnect system permits an orthogonal input/output assembly.

Separately controlled gate switching voltages are supplied to the FET amplifiers from the logic switch drivers to improve reliability in the event that the logic drive signal would fail in the ON state. The remaining amplifier can be independently turned off and would provide enough isolation to the input/output transmission lines. Measurements of OFF state isolation were made in order to determine isolation in the event of such a failure. Results of the test are shown in Figure 2.4. Data shown was plotted from measured data of an automatic network analyzer.

2.2 CONTROL LOGIC

The control logic interfaces with special test equipment to simulate an on-board satellite computer which supplies traffic routing information in the form of a 32-bit code. This code supplies switch crosspoint addressing information to the switch matrix. The control logic interprets the computer address code and provides gate bias signals to the appropriate GaAs FET switch crosspoints, thus configuring the matrix. The control logic also stores in memory the reconfiguration addresses for the next time frame.

The switch matrix control circuitry is divided into a decoder section and a switch driver section, as shown in Figure 2.5. The test box shown was built as a part of the POC effort to simulate an on-board computer operating in a SS-TDMA mode. Operating DC voltages are also supplied by the test box. The switch matrix decoder accepts the 32-bit address code through the input buffer. The buffer provides a compatible interface to the computer as well as supplying the address code to the switch matrix row and column decoders. The decoders interpret the address code and load the update memory with the next time period switch configuration upon receipt of a read pulse from the test box. A reconfiguration pulse supplied by the test box transfers the data from the update memory to the matrix configuration memory. The configuration memory provides a voltage level through the output buffer and switch driver to the gate lead of the switch crosspoint GaAs FETS. The GaAs FET switch is then controlled on or off as required.

The 32-bit data word is divided into three 10-bit pair fields (input, output) and two reset bits. Each pair field is further divided into two 5-bit subfields. The first 5-bits define the input channel of the matrix and the second group of 5-bits defines the output channel. Within each pair field, any crosspoint in the 20 x 20 matrix can be defined. Since the data rate requirement was 200 nanoseconds, the input command will be decoded and latched in the update memory by a read pulse within this time interval. After a total of

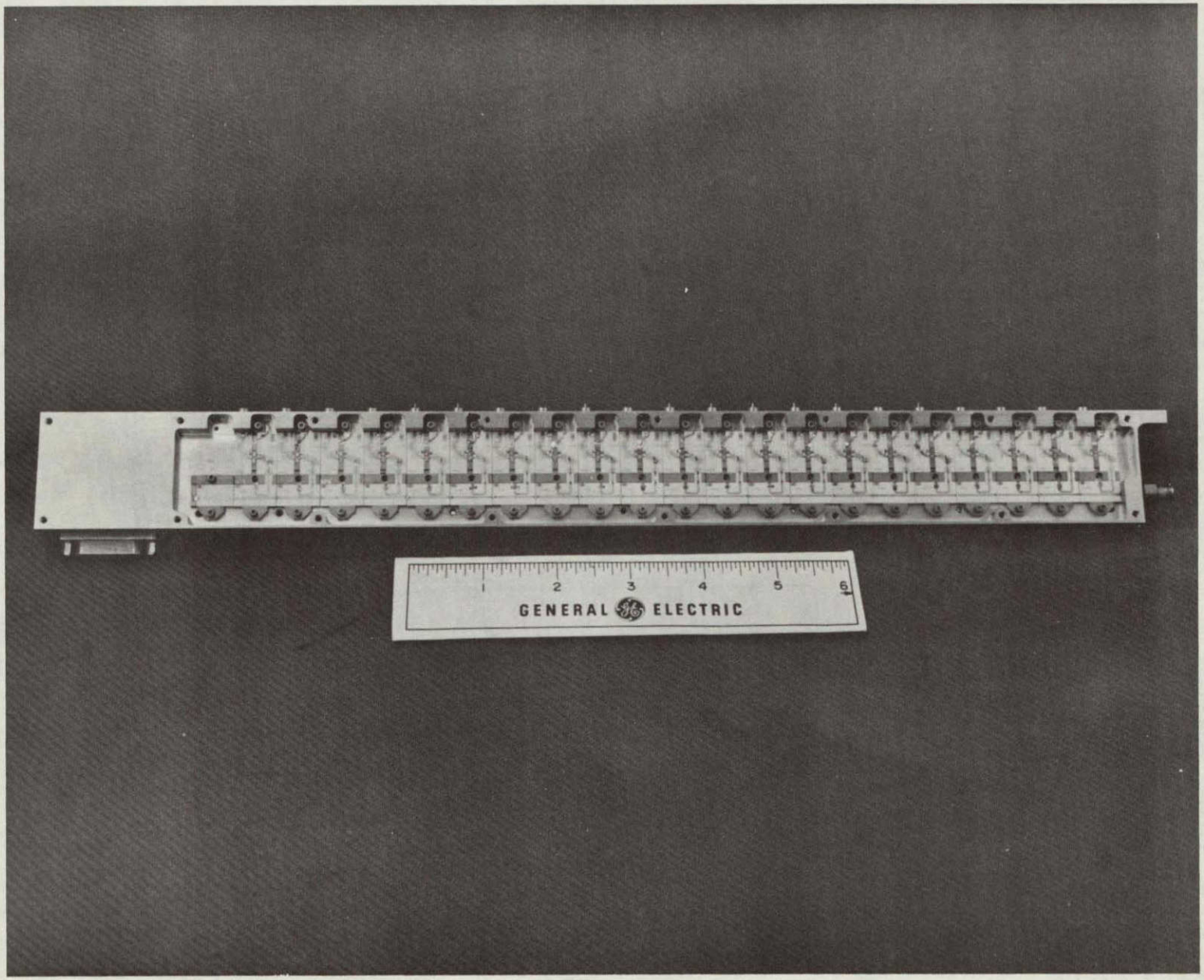


Figure 2.3. Output Column Channel MIC Assembly

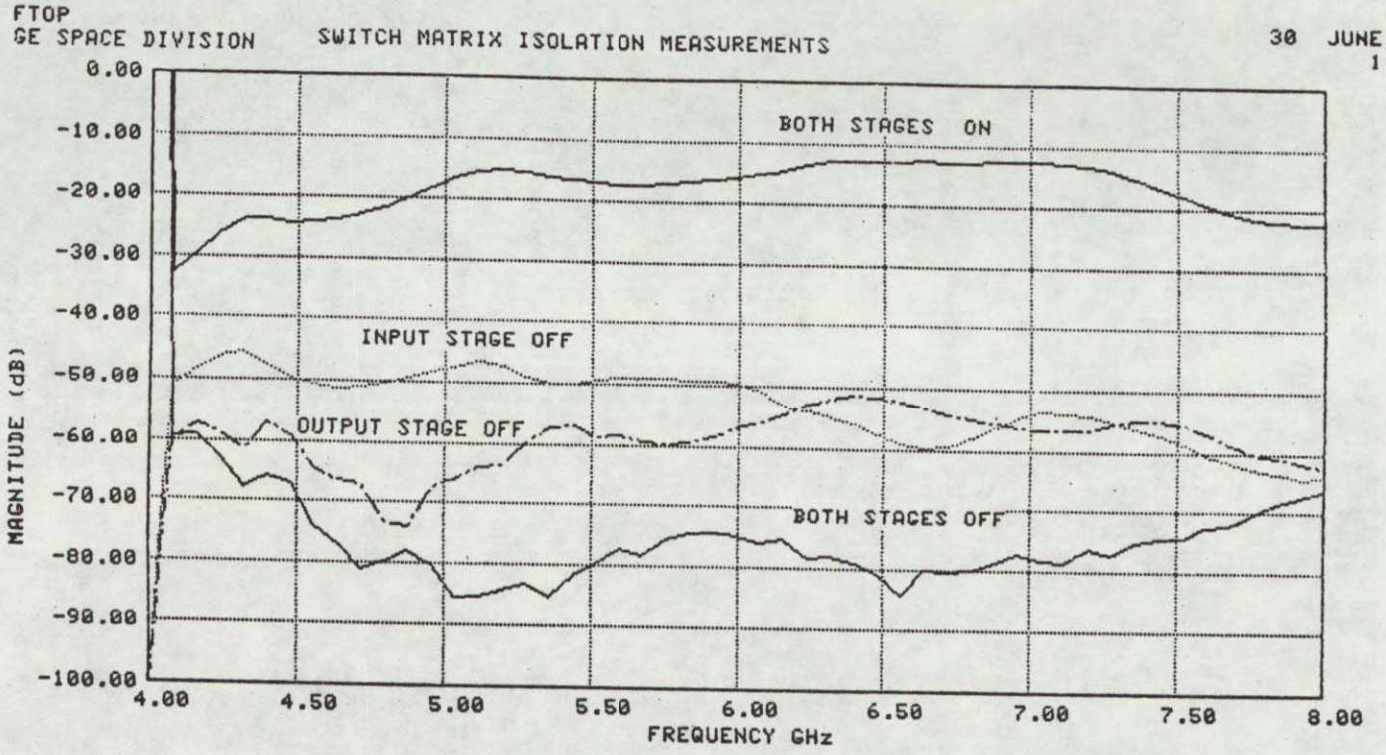


Figure 2.4. Switch Matrix Isolation Measurements

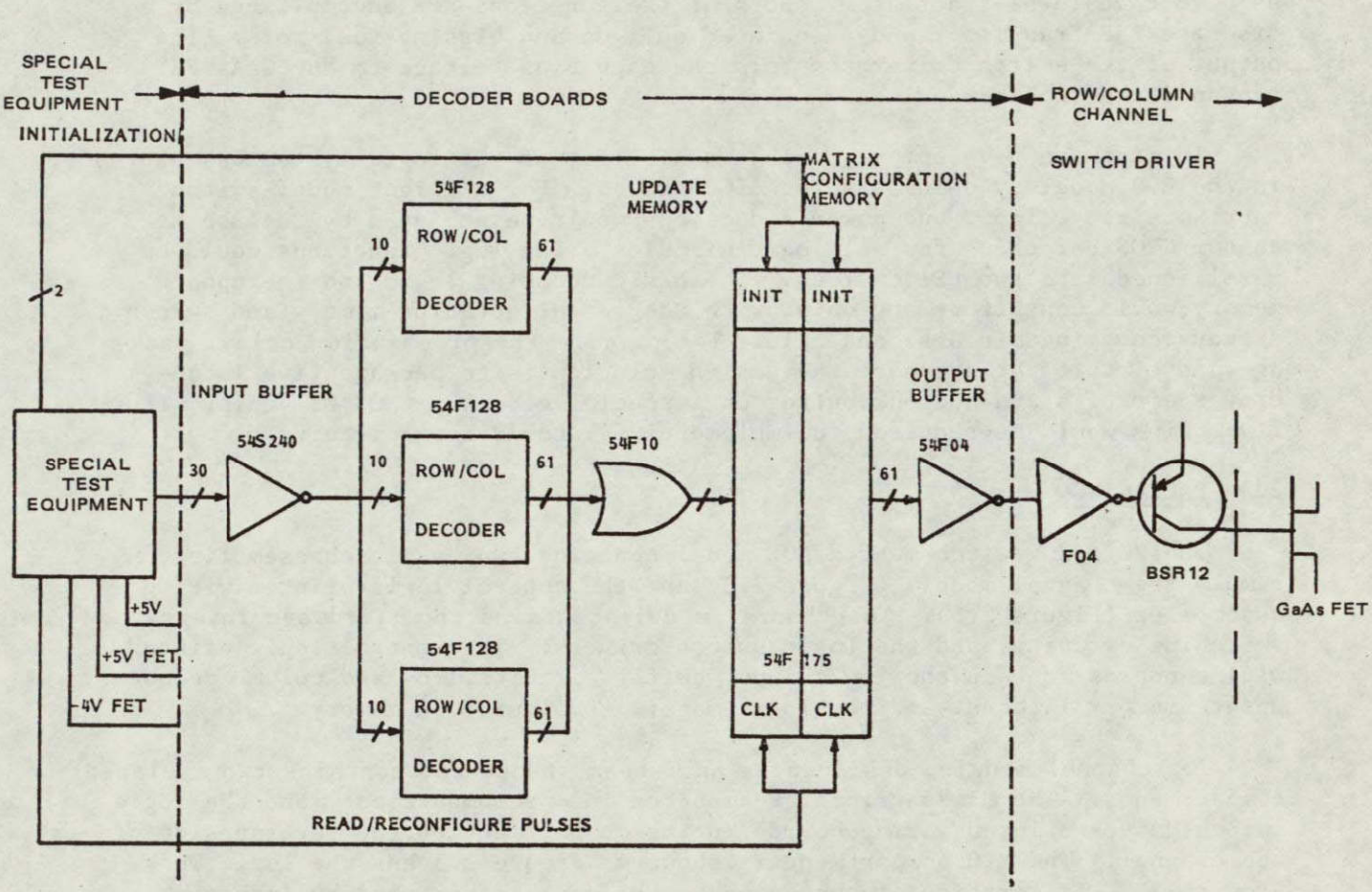


Figure 2.5. Digital Control Block Diagram

nine data transfers, a reconfiguration pulse will clock the update memory data into the configuration memory. Nine data transfers were selected for a 20 x 20 switch matrix with five redundant wraparound paths, or in effect a 25 x 25 switch matrix. For switch matrices of smaller size, a reduction from the nine data transfers would be required. This method of switch crosspoint reconfiguration meets the design goal requirements of total switch reconfiguration within 2 microseconds. For the POC model, two identical decoders, one for input channels and the other for output channels, were assembled on separate 12" x 8", multilayer printed wiring boards as shown in Figure 2.6. This dual decoder system provides full redundancy in order to meet system reliability requirements over a mission life of ten years.

The logic switch driver functions as a switching control device as well as a voltage level translator. Both of the functions are accomplished by a discrete PNP transistor and associated pull-up and biasing resistors. The output of the switch driver controls the gate bias voltage to the GaAs FET crosspoint switching devices.

To minimize development costs, feasibility of the logic system was proven in the POC Model by using discrete IC devices. For a flight model switch matrix, size, weight, and power reductions would be achieved by the use of custom CMOS LSI chips for all logic circuits. The logic functions could be partitioned into two LSI devices. The basic decoding logic and the update memory would constitute one chip, with the reconfiguration memory and switch drivers contained in a second chip. To optimize the propagation delay, package and circuit performance, the design solution is to package five latch-driver circuits and a clock buffer on a special geometry CMOS LSI chip. Thus, five chips would be required to implement 25 latch/driver circuits.

2.3 PACKAGING

The 20 x 20 switch matrix POC model contains two basic subassemblies, namely the channel module (Figure 2.3) and the control logic printed wiring assemblies (Figure 2.6). The channel module contains the microwave integrated switching circuits, and the logic switch drivers. The control logic printed wiring boards contain the logic input buffer circuits, row and column decoders, update memory latches, and the logic matrix configuration memory.

The channel module, designed as an I-beam structure, contains two isolated compartments. The MIC carriers are mounted in one compartment, and the logic switch driver printed wiring boards in the compartment on the reverse side of the channel. The MIC compartment is shown in Figure 2.3 and the logic in Figure 2.7. Integration of the compartments was accomplished by inserting small gauge wires connected to pads on the switch driver printed wiring boards, through 40-mil holes, and then connected to pads on the MIC carriers.

SMA connectors, mounted on the front of the channel module, provide input row and output column IF signal access. Logic control signals and supply voltages are connected to the channel via the 31 pin MDM connector located at the rear of the channel module. Each channel module is a self contained input row or output column. This design is readily expandable to any switch matrix size.

The switch matrix is readily assembled by attaching the input and output channel modules, which are mechanically identical, to a mounting plate. The

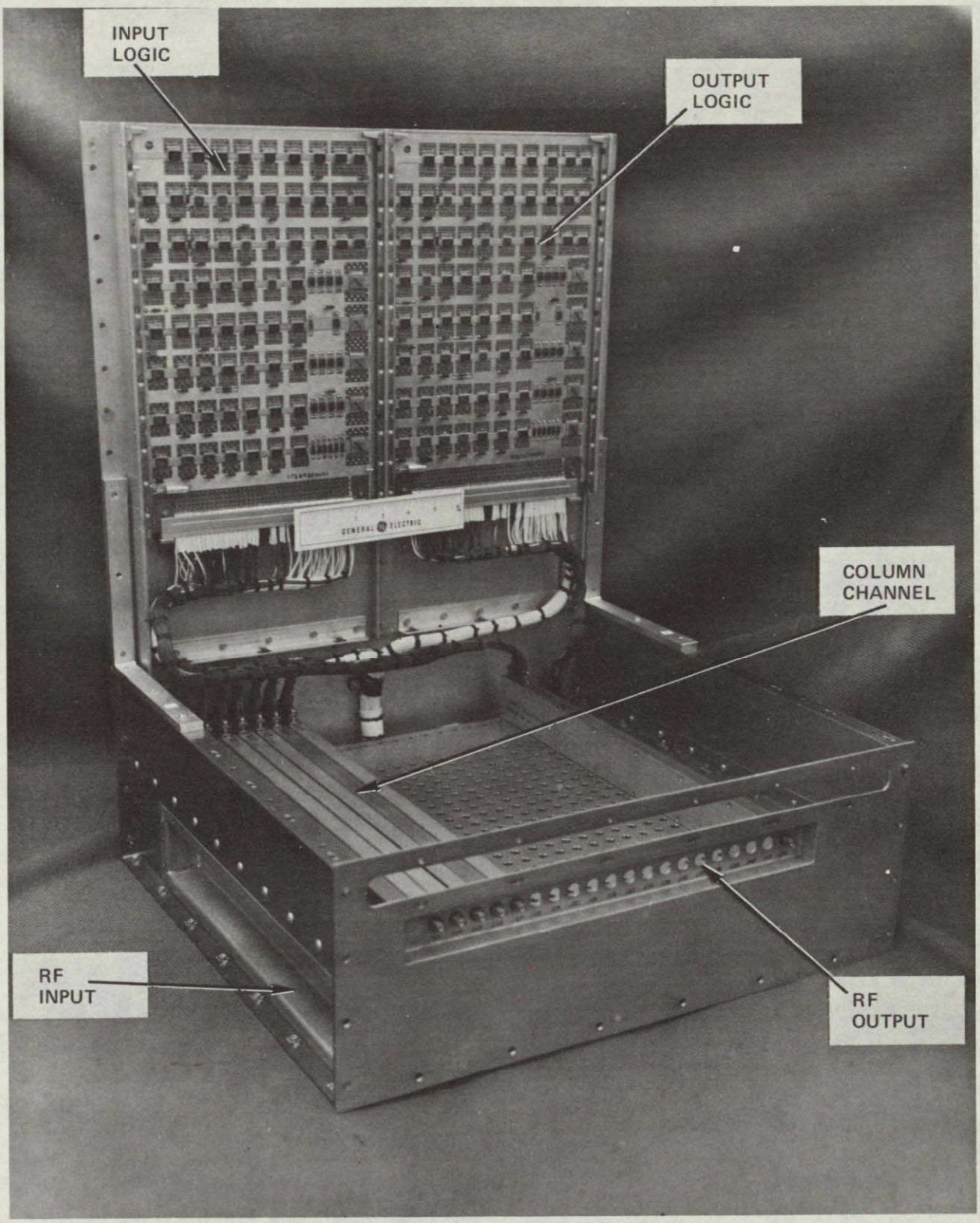


Figure 2.6. POC Model Switch Matrix

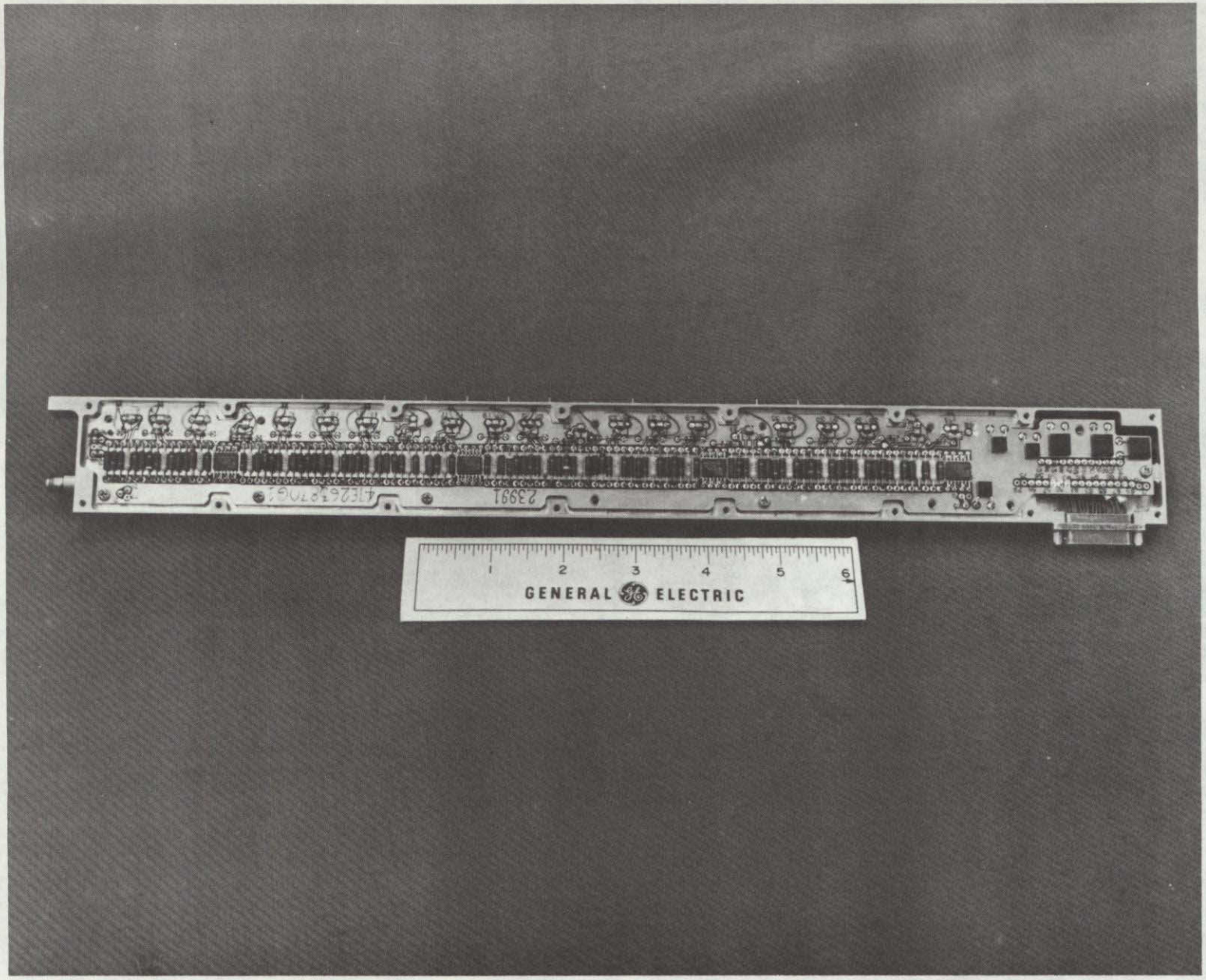


Figure 2.7. Channel Logic Assembly

plate serves in the alignment of the channel modules and as part of the IF signal interconnect system between input and output channels.

The control logic assembly consists of two multilayer printed wiring boards. Each board contains 122 integrated circuits and a small number of discrete components. Total heat dissipation of each board is approximately 11 watts, necessitating special heat sinks to transfer heat from under the components. The heat sinks were chemically milled six-ounce copper foil, plated and bonded to both sides of the printed wiring boards. Heat is removed from the boards by thermally conductive card guides (Figure 2.7). The card guides were riveted to the bottom plate of the switch matrix assembly.

The switch matrix is assembled by mounting the channel housing assemblies and the control logic printed wiring boards into the matrix housing shown in Figure 2.6. The switch matrix is shown with the bottom plate open to facilitate testing of the control logic. The channel modules and logic boards are interconnected by a flexible wire harness. The channel input/output RF connectors protrude through openings in the matrix housing for ease of connection when the matrix housing covers are in place.

2.4 RELIABILITY

Trade-off studies have shown that the optimum design for a 20 x 20 IF switch matrix based on weight, power consumption, and reliability is one that contains:

- Wraparounds for redundancy
- Separate IC logic to control each GaAs FET switch in a crosspoint, to eliminate single point failures
- Channel construction of the input rows and output columns
- A 32-bit logic interface address code.

Without redundancy the probability that any one of N inputs can be connected to any one of N outputs at any time during a ten-year mission life was calculated as 0.30065 with an assumed crosspoint reliability of 0.997. To increase this probability of mission success, redundancy is incorporated using the wraparound technique as shown in Figure 2.8. To illustrate, if the crosspoint at input row 2 and output column 3 failed, the substitute crosspoint of row 2 would be activated permitting the signal to flow through the wraparound amplifier to the redundant input line. Column 3 crosspoint would also be turned on connecting the signal to the desired column 3 output. A successful wraparound must have its amplifier and two specific switches operating. However, when more than one wraparound is available, there is considerable redundancy in the switches of the wraparounds which permit an interchange of amplifiers. The probability of success of a wraparound would therefore be the probability that the amplifier is working successfully.

To evaluate the predicted reliability of a flight model 20 x 20 Switch Matrix with a ten-year mission, the microwave switching crosspoint design of the POC model and a control logic design in CMOS LSI technology were assumed

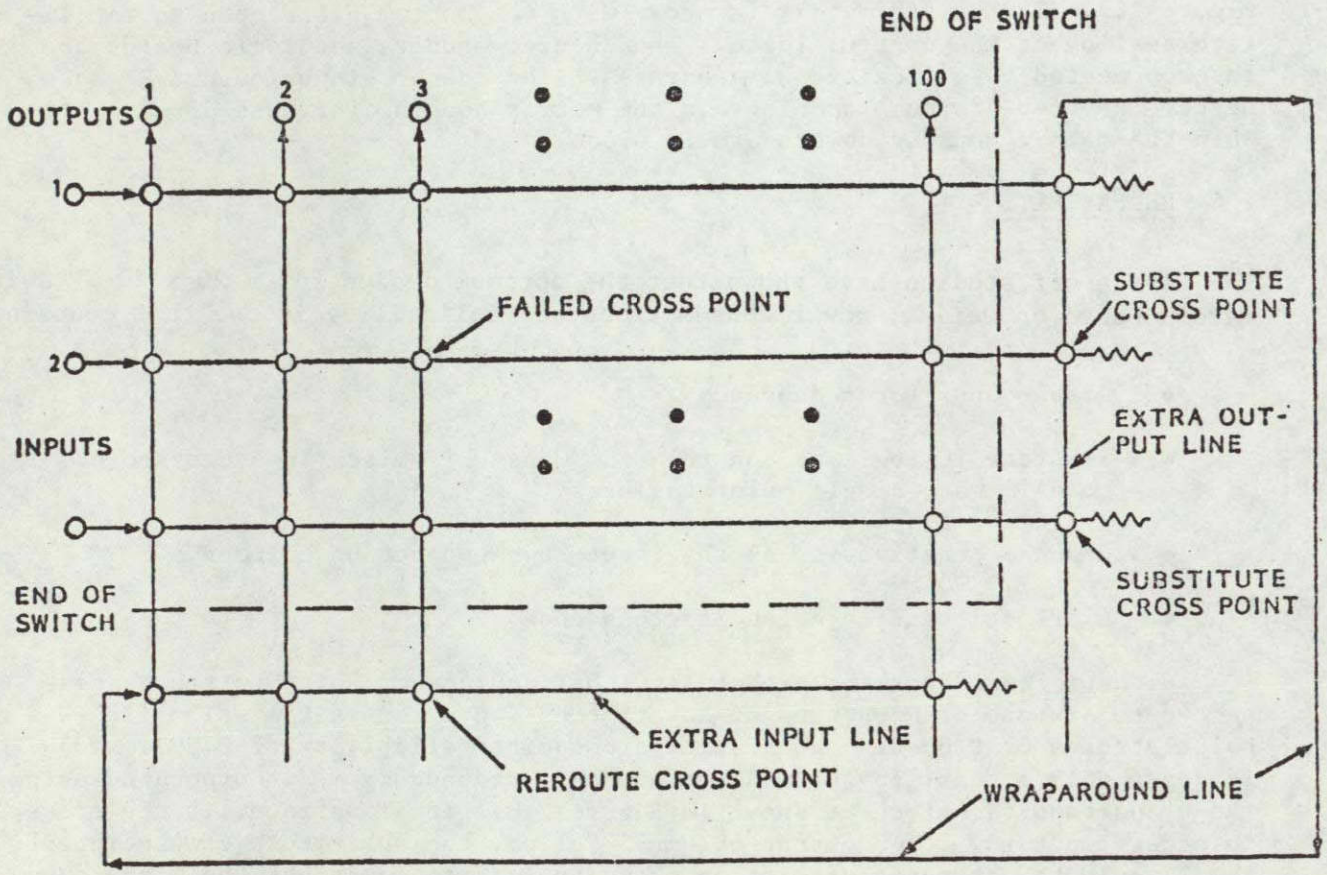


Figure 2.8. Wraparound Redundancy for Crossbar Switch Matrix

for the analysis. The results of this analysis indicated a probability of success which is dependent on the number of wraparounds; i.e.:

- Zero Wraparounds 0.19483
- One Wraparound 0.66853
- Two Wraparounds 0.88408
- Three Wraparounds 0.95929
- Four Wraparounds 0.97678
- Five Wraparounds 0.97916

The probability of success is then limited by the 40 input and output RF connectors which have a probability of success of 0.98065.

Figure 2.9 shows the POC Model with one wraparound.

Figure 2.9. Switch Matrix - Input Channels

2.5 SPECIAL TEST EQUIPMENT

In order to test the Switch Matrix POC Model, a special test set was designed and fabricated. The test set is capable of sending crosspoint addressing information in both manual and automatic modes. A 32 bit code is generated and permits three Switch Matrix crosspoint locations to be updated simultaneously. The total number of codes to be transmitted would depend on the number of crosspoints to be updated. For a 20 x 20 Switch Matrix with five wraparounds, nine data transfers would be required.

A block diagram of the special test equipment is shown in Figure 2.10. There are two different methods to input data; one through thumbwheel input switches, the second through internal PROM. The inputs are multiplexed into a redundant RAM. The output control takes over multiplexing a single word at a time, then latches the data to the front panel display and to the Switch Matrix digital decoder logic. A separate control selects the rate of the read and reconfiguration pulses. Capability is also provided for inputing an external read and reconfiguration rate pulse. If a commercial variable word generator is used for this purpose, the special test equipment has the capability of simulating an on-board spacecraft computer operating in an SS-TDMA mode.

In the manual mode, one to three crosspoint locations may be inputed by setting the thumbwheel switches, shown in Figure 2.11, to the desired switch matrix crosspoint address. The read pulse and reconfiguration pulses are then transmitted manually to the switch matrix. The test box display indicates which crosspoint location has been selected.

In the automatic mode, nine read pulses are sent followed by a single reconfiguration pulse to update one entire matrix. The rate of completing an update of the matrix is determined by the setting of the front panel rate control, in steps between 2 usecs up to 128 usecs or by an external source. Each read pulse transfers the 32-bit address code to the switch matrix. There are sixteen different switch matrix configurations stored in the test equipment PROM. Capability was provided for the option of selecting 1 to 16 different matrix configurations to be transmitted before repeating the first matrix again.

The Special Test Equipment also supplies DC voltages to the Switch Matrix. Power supplies were chosen with current limiting and over voltage protection, with < 250 uV ripple, over a voltage range between 0 to 7 volts. Current and voltage monitoring test points were also provided.

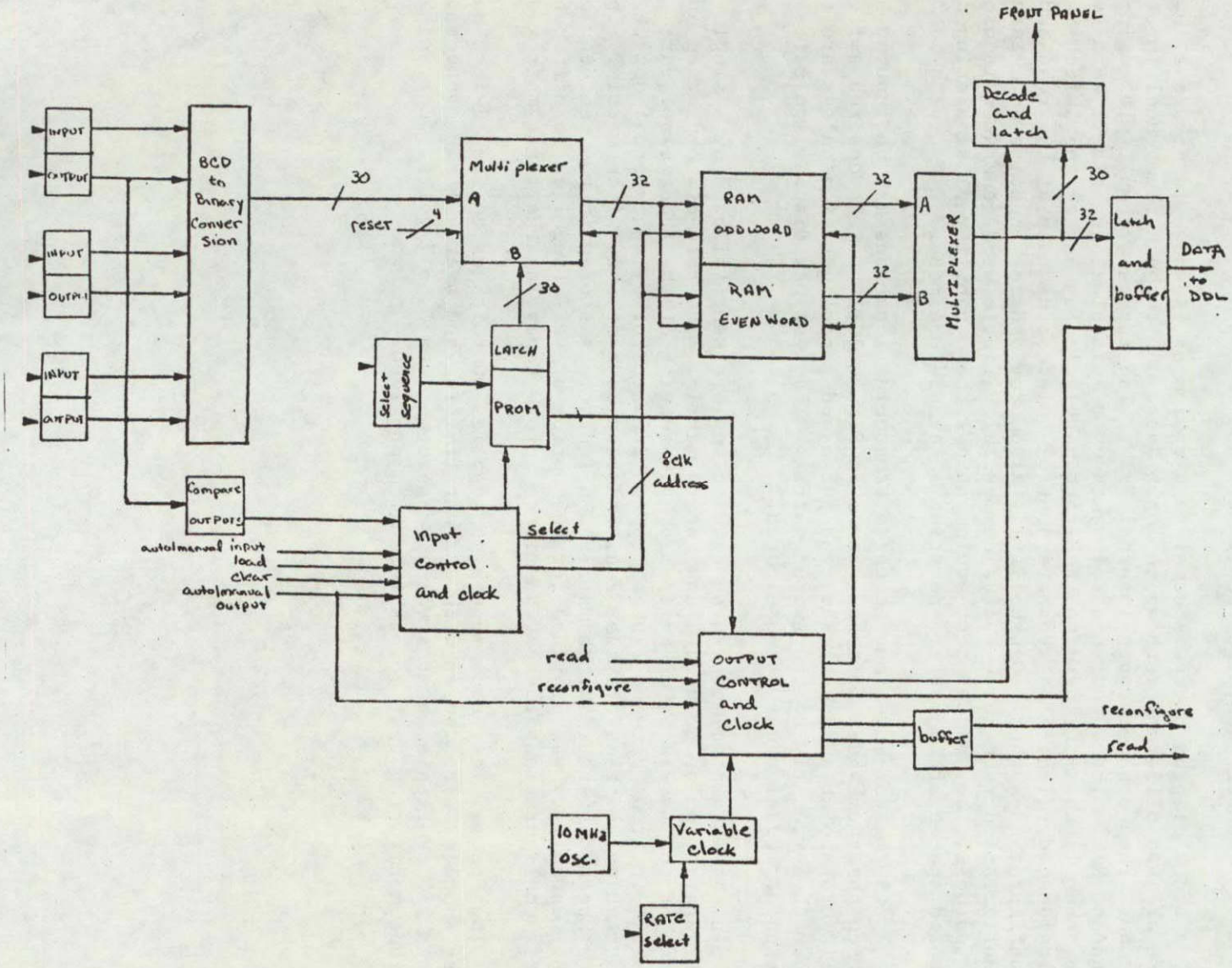


Figure 2.10. Special Test Equipment Block Diagram

Figure 2.11. Special Test Equipment

SECTION 3.0

COMPONENT ACCEPTANCE TESTS

3.1 MICROWAVE CROSSPOINT ACCEPTANCE TESTING

Individual crosspoints were tuned and tested using a Hewlett Packard Frequency Response Test Set. Each crosspoint was tuned to meet or exceed the requirements of 1 dB bandwidth, insertion loss and loss ripple. As tuning was completed on a crosspoint, the loss, ripple, 1 dB bandwidth and individual gate voltages were recorded. Table 3.1-1 is a statistical summary of the insertion loss and 1 dB bandwidth of 63 individual crosspoints. Given for each parameter are the spec. value, the sample size, sample mean, range of parameter values, 95% confidence level limits on the sample mean, prediction limits on next observation, tolerance to contain 95% of population with 95% confidence, and the sample standard deviation.

Automated Network Analyzer (A.N.A.) testing was performed on a selected basis to verify the data taken on the Frequency Response Test Set and to confirm that the parameters of phase linearity and VSWR would meet or exceed the design goals and earlier predictions. Thorough A.N.A. testing was performed at the POC assembly level and is discussed in Section 4.2.1. The data on the individual crosspoints verifies the design readiness for integration and establishes that the design goals are being met.

Results of the statistical analysis for 1 dB bandwidth is shown in Figure 3.1-1 with a histogram of the data points. The range of data points was between 0.85 GHz and 1.2 GHz with an average mean value of 1.055 GHz. Tight parameter process control can be achieved at the Microwave Integrated Circuit (MIC) substrate fabrication level with the selected switch/amplifier crosspoint design. The major contributor to any parameter variation would be from the GaAs FETS. No attempt was made during POC fabrication to match GaAs FETS for specific crosspoint performance, although the devices were tested upon receipt from Dexcel. Test results have indicated that there are no critical GaAs FET parameters for devices fabricated from a specific wafer.

Crosspoint insertion loss as shown in Figure 3.1-2 exhibited a mean value of 10.75 dB with a range of 6.9 to 16 dB. A feature of the crosspoint design is a select at test resistor in the switch driver circuit (Figure 3.1-3) that provides the capability of matching the crosspoint insertion loss throughout the switch matrix. As stated above there were no critical GaAs FET parameters evidenced within devices; however, to reduce the insertion loss gain spread of the tolerance limits, a gain specification for the GaAs FET would be desirable to reduce the time to match the gain of crosspoints at the select at test functions.

TABLE 3.1-1.

INDIVIDUAL CROSSPOINT DATA STATISTICAL SUMMARY

	SPEC	N	$\bar{X}$	RANGE SM	RANGE LG	CONFIDENCE LIMITS ON $\bar{X}$ (1)		PREDICATION LIMITS ON NEXT Xi (2)		TOLERANCE TO CONTAIN 95% (3)		σ
BANDWIDTH	1.0 GHz	63	1.05 GHz	.85	1.2	1.04	1.07	.94	1.17	.92	1.19	.06
INSERTION LOSS	15 dB	63	10.75 dB	6.9	16.0	10.25	11.25	6.75	14.76	6.1	15.4	2.0

1. CONFIDENCE LIMITS ON THE POPULATION MEAN.
2. PREDICTION LIMITS TO CONTAIN THE NEXT OBSERVATION.
3. TOLERANCE LIMITS TO CONTAIN 95% OF THE POPULATION.

SAMPLE STATISTICS FOR BW

NO. OF OBSERVATIONS	63
AVERAGE:	1.05492
STANDARD DEVIATION:	0.05648
SMALLEST OBSERVATION:	0.85000
LARGEST OBSERVATION:	1.20000

FREQ	CELL LOWER ENDPT	
	BELOW	
0	0.800	
0	0.800	
1	0.850	*
0	0.900	
2	0.950	**
26	1.000	**************************
18	1.050	******************
14	1.100	**************
1	1.150	*
1	1.200	*
	ABOVE	
0	1.250	

Figure 3.1-1. Observed 1 dB Bandwidth for Individual Crosspoint

SAMPLE STATISTICS FOR IL

NO. OF OBSERVATIONS	63
AVERAGE:	10.75238
STANDARD DEVIATION:	1.98802
SMALLEST OBSERVATION:	6.30000
LARGEST OBSERVATION:	16.00000

FREQ	CELL LOWER ENDPT	
	BELOW	
0	5.00	
0	5.00	
1	6.00	*
4	7.00	****
6	8.00	******
12	9.00	************
10	10.00	**********
11	11.00	***********
8	12.00	********
8	13.00	********
2	14.00	**
0	15.00	
1	16.00	*
0	17.00	
	ABOVE	
0	18.00	

Figure 3.1-2. Observed Insertion Loss for Individual Crosspoints.

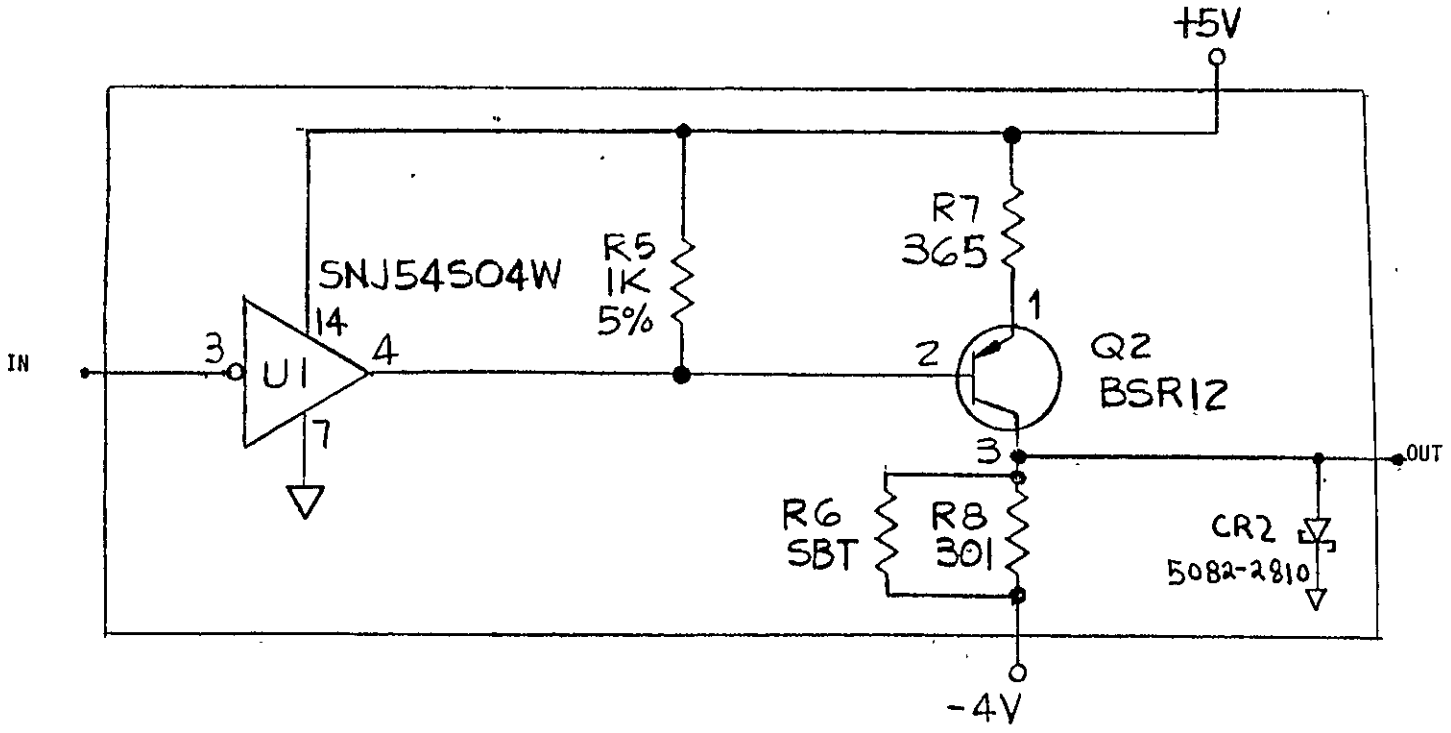


Figure 3.1-3. GaAs FET Switch Driver

3.2 CONTROL LOGIC TEST RESULTS

The test results for the decoder boards and High Speed Logic (HSL) switch drivers of the "30/20 GHz Switching Matrix" are discussed here. These tests were completed using the "30/20 GHz Digital Control Circuitry Test Procedure."

The results of the decoders and drivers tests are tabulated in Table No.1 and Table No. 2, respectively. Both tables summarize the results of power and timing measurements. Average values reflect the general characteristics of the circuit, however, minimum and maximum values indicate the variations from different circuit assemblies.

Figure No. 1 and Figure No. 2 are typical timing measurements taken at the digital control circuit. The driver assembly and the RF channel assembly are connected to the decoder board. The switching command and reconfigure pulse are provided by "the Decoder Test Box". The rise/fall time of the switching pulse, as well as, the 50%:50% propagation delay of the switching pulse with respect to the reconfigure pulse are measured at the output of the driver (the collector of the transistor). This propagation delay results as a function of the signal traveling through the decoder board, wires and the driver board. The average rise and fall times are 15 nsec and 19 nsec, respectively. The average switching pulse delay is 32 nsec. The power consumption per board is 9.85 W @ + 5.00 V.

As shown in Figure No. 3, different data rates had virtually no effect on the switching pulse rise/fall time or delays. However, the power supplies do affect the switching speed as expected. Higher voltage causes faster switching. A 2 nsec delay can be seen as the voltage is changed from + 5.50 V to + 5.00 V and from + 5.00 V to + 4.50 V. The difference between the switching pulse in Figure No. 1 and Figure No. 4 resulted from the fact that Figure No. 1 was taken with RF channel assembly connected, but Figure No. 4 was not. The additional capacitance of the RF channel in Figure No. 1 shows the response time of the waveform and attenuates the higher order frequencies inherent in fast switching devices. Figures 5 and 6 are the switching pulses at the output of the decoder boards without switch driver connected. Timing measurements on the decoder boards is also shown in Table 1.B.

The characteristics of the drivers are tabulated in Table No. 2. These tests on the drivers were made without RF channel assembly connected. Power consumption, depending on the number of crosspoints, varied for each subgroup of the drivers. The average rise time of the switching pulse is 6 nsec and fall time is 11.5 nsec. The average 50% : 50% propagation delay of the switching pulse is 14 nsec. Typical timing measurements are shown in Figure No. 7 and Figure No. 8.

The output of the driver swing between the high level at -0.7V ('ON' state) and low level at -3.8V ("OFF" state), but the "ON" state will be biased to different voltage by "Select By Test (SBT) resistor" to meet the requirement of each individual RF crosspoint.

Table 1.A: Power Measurements of the Decoder Boards

CURRENT MEASUREMENT OF								
+5V POWER SUPPLY								
+5.00V			+4.50V			+5.50V		
Avg.	Board #1* / Board #2	Two Boards	Avg.	Board #1* / Board #2	Two Boards		Board #1* / Board #2	Two Boards
1.97	1.96 / 1.98	3.94	1.54	1.56 / 1.62	3.18	2.15	2.12 / 2.18	4.30

*There are two identical decoder boards in the system.

Table 1.B: The Timing Measurements of the Decoder Boards

Timing Measurement** Without HSL Driver (nsec)				Timing Measurement** With HSL Driver (nsec)							
50% : 50% Propagation Delay				Rise Time (10%:90%)		Fall Time (90%:10%)		50% : 50% Propagation Delay			
Rise*		Fall*		Avg.	Min / Max	Avg.	Min / Max	Rise*		Fall*	
Avg	Min / Max	Avg	Min / Max					Avg	Min / Max	Avg	Min / Max
20	16 / 24	23	21 / 25	15	15 / 15	19	18 / 20	32	30 / 35	32	30 / 35

* Rise, fall means a positive and negative going switching pulses, respectively.

** Timing measurements were done at the output of the decoder board/at the output of the switch driver for without HSL Driver/with HSL Driver incorporated. The reference is the reconfigure pulse at the input of the decoder board.

Table 2.A: The Power Measurements of the High Speed Logic Switch Driver Boards

PWB Assembly #	# of Crosspts	Current Measurement of -4V FET Power Supply (mA)				Current Measurement of the +5V Power Supply (mA)					
		All* Off	Only* One On	All On*		All Off*		Only One On*		All On*	
				Avg	Min**/Max	Avg	Min**/Max	Avg	Min**/Max	Avg	Min**/Max
G1	21	0.0	10.8	219		57.5		74.8		415	
G2	20			209		59.3		77.3		406	
G3	5			54.0	53.9/54.2	15.3	15.1/15.5	33.6	32.9/34.2	104.6	102.1/105.9
G4	6			64.3		15.5		33.9		122.1	
G5	2			21.9		31.1		49.7		68.2	
G6	7			75.3		31.0		49.0		153.8	
G7	3			32.4		29.4		47.6		82.8	
G8	2			21.6	21.5/22.0	14.6	14.0/16.3	32.7	31.0/35.6	50.6	48.6/54.0
G9	3	13.3***	24.2	35.1		27.9		46.0		63.8	

* All ON = All crosspoints in channel "ON". All OFF = All crosspoints in channel "OFF". Only One On = Only crosspoint in channel "ON".

** Min/Max only applies to those groups with 3 or more channels.

*** G9 has a wraparound channel amplifier which is always on.

Table 2.B: Output Voltage Swing and Timing Measurements of the High-Speed Logic Switch Driver Boards

Switch Driver Output Voltage Swing (V)		Switching Pulse Timing Measurements (nsec)					
Avg	Min / Max	Rise Time (10% : 90%)		Fall Time (90% : 10%)		Propagation Delay*	
		Avg	Min / Max	Avg	Min / Max	Avg	Min / Max
-0.7	-0.6 / -0.8						
-3.8	-3.8 / -3.9	6	6/7	11.5	5/9	4	2/6

*Propagation delay is measured by 50%=50% referred to the input clock signal.

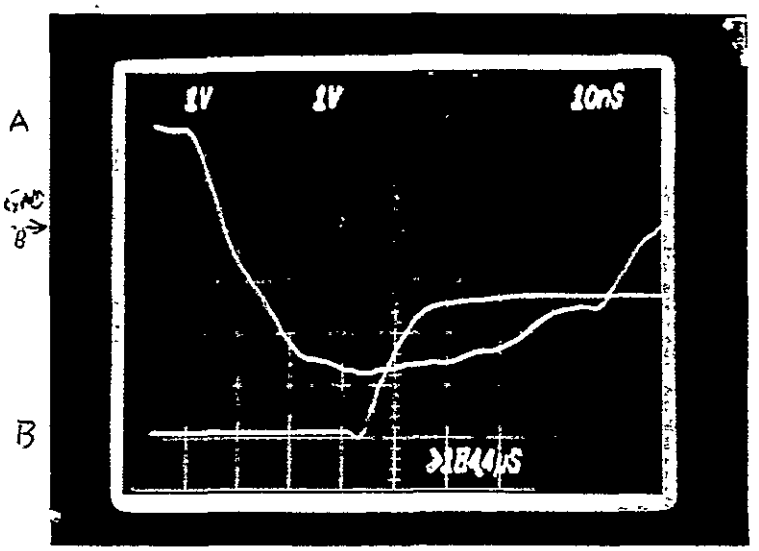


Fig. 1. Propagation delay for switching "ON" pulse. "A" is a reconfigure pulse at the input of the decoder. "B" is the switching pulse at the output of the driver (with RF channel incorporated). GND reference for "B" only.

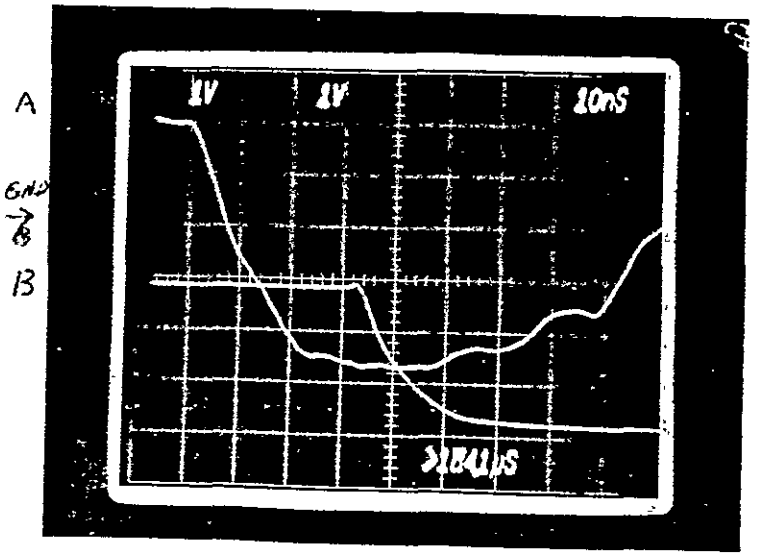


Fig. 2. Propagation delay for switching "OFF" pulse.

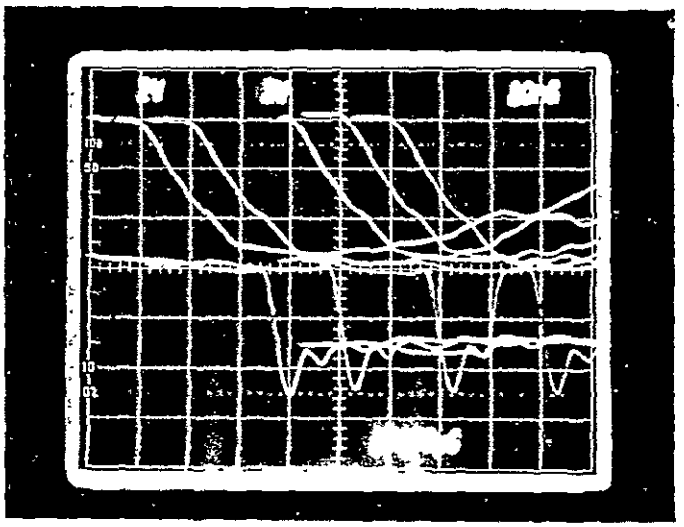


Fig. 3. "A's" are reconfigure pulses. "B's" are the corresponding switching pulses with the different data rates. [1], [2], [3], [4] and [5] are at the data rate of 2, 4, 8, 16 and 32 usec respectively.

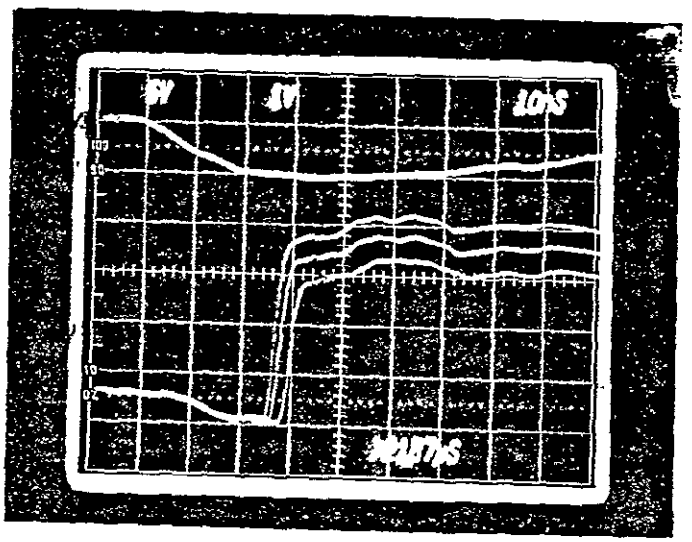


Fig. 4. Power supplies may affect the switching speed. [1] is measured at +5.50V, [2] at +5.00V, and [3] at +4.50V. "A" is a reconfigure pulse as a reference.

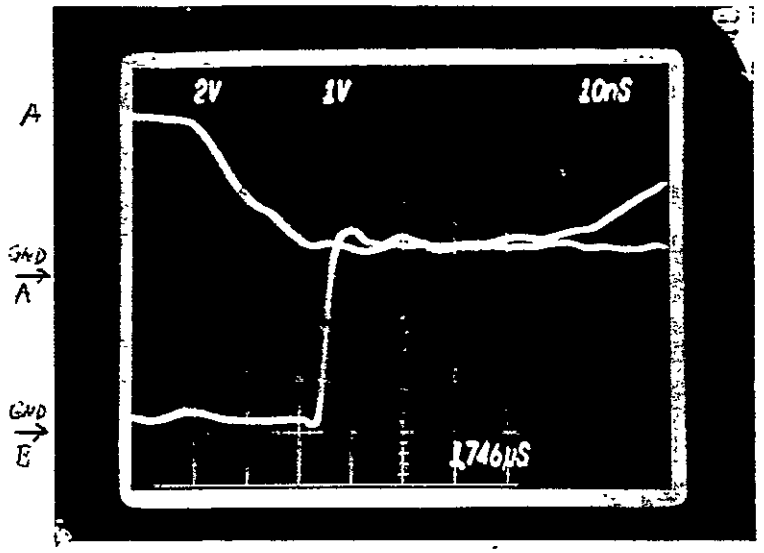


Fig. 5. Propagation delay for switching "ON" pulse. "A" is a reconfigure pulse at the input of the decoder. "B" is the switching pulse at the output of the decoder (without driver connected).

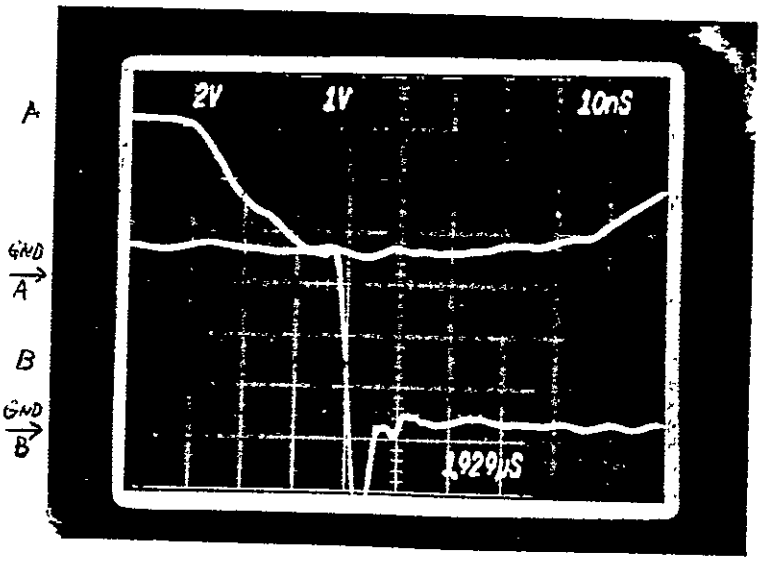


Fig. 6. Propagation delay for switching "OFF" pulse.

NOTE: Figure 5 and Figure 6 were taken without RF channel assembly connected.

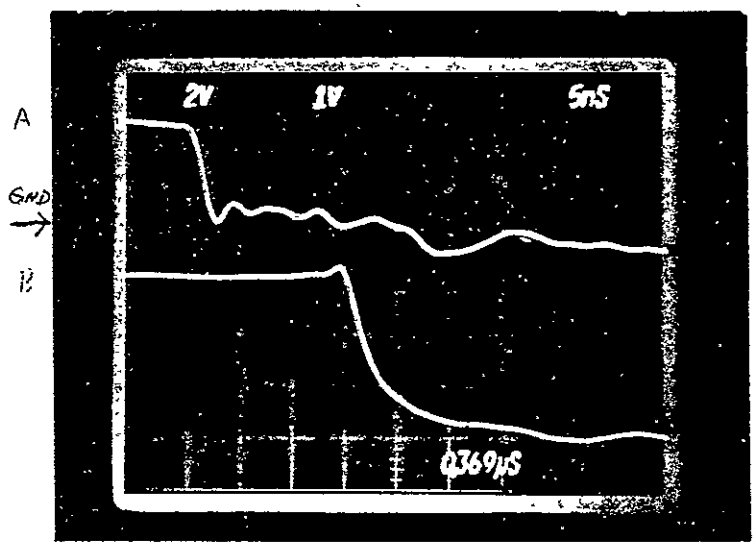


Fig. 7. Driver switching. A is the external clock at the input of "The Driver Test Box" to deactivate the crosspoint. "B" is the switching pulse at the output of the drive.

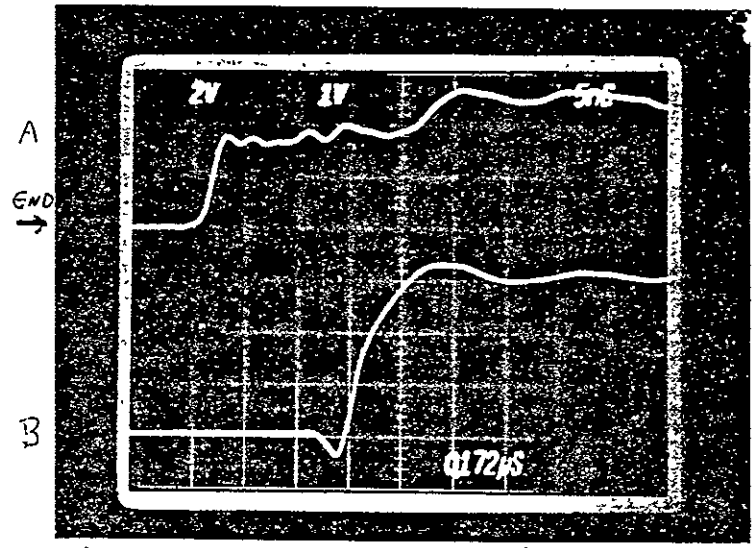


Fig. 8. Similar measurement as in Figure 5; activating the crosspoint.

SECTION 4.0

POC MODEL TEST DATA AND EVALUATION

4.1 POC MODEL FUNCTIONAL PERFORMANCE

The POC Design Goal specification and statement of work documents established the performance requirements for the POC Model 20 x 20 Switch Matrix. This section serves as an overview of the POC functional performances.

4.1.1 ELECTRICAL CONFIGURATION

Figure 4.1.1-1 is the selected POC Switch Matrix crosspoint distribution that was assembled and tested. In addition to the required number of crosspoints (57), four wraparound crosspoints and a wraparound amplifier were included to confirm that the conceptual design of the wraparound method was feasible in the switch matrix.

Connectivity was verified by extensive microwave testing. Control circuitry required to command the routing of RF signals was composed of the switch driver, decoder, and switch memory circuits. Reconfiguration rate was demonstrated to be superior to the 2 microsecond requirement. Switching time as defined in the POC specification document was impaired due partially to improved logic switch rise and fall times. This is discussed in more detail in Section 4.2. The I.F. was selected to be at 6.25 GHz based on analysis of the crossbar architecture; however, the results of the first POC crosspoints indicating that the actual center frequency was 6.5 GHz, did not significantly impact other functional performances. Bandwidth and insertion loss requirements were known to be critical technology challenges and great care was taken in developing better devices through interfaces with Dexcel and through screening of the devices suitable for use in a large gain bandwidth product design. Gain ripple and phase linearity were found to be related to both gain and bandwidth (Section 4.2) and were carefully traded off to determine the optimum design. As a result, loss ripple and bandwidth were very near the design goals of 1.0 dB and 1.0 GHz respectively. Phase linearity measurements indicated that the earlier predictions of $\pm 8^{\circ}$ max. for this design were very accurate. An interface problem was encountered in the interconnect system which did not occur in the breadboard or in the individual channel housings. Rework was performed which compensated partly for the problem but some degradation in bandwidth and insertion loss resulted. The rationale for the interconnect system was validated by the large amount of isolation afforded by this system.

Input and output VSWR was recognized as another significant technology goal as early as the architecture selection study. The results of the study were verified by the measurements of the POC model. The model used in the study showed that there would be peaks and nulls in the reflected power (equivalently VSWR) frequency response due to the periodic structure of the cascaded directional couplers. The optimum design was to place the center frequency of the crosspoint at a null, and have the peaks occur outside of the passband. The nulls and peaks occurred as predicted; however, the amplifier passband was shifted and hence in band VSWR was compromised. Noise and input signal level are two parameters which were not only met or exceeded over the relatively wide range of input signal level specified in the statement of work, but also over the range which was determined to be desirable based on additional third order

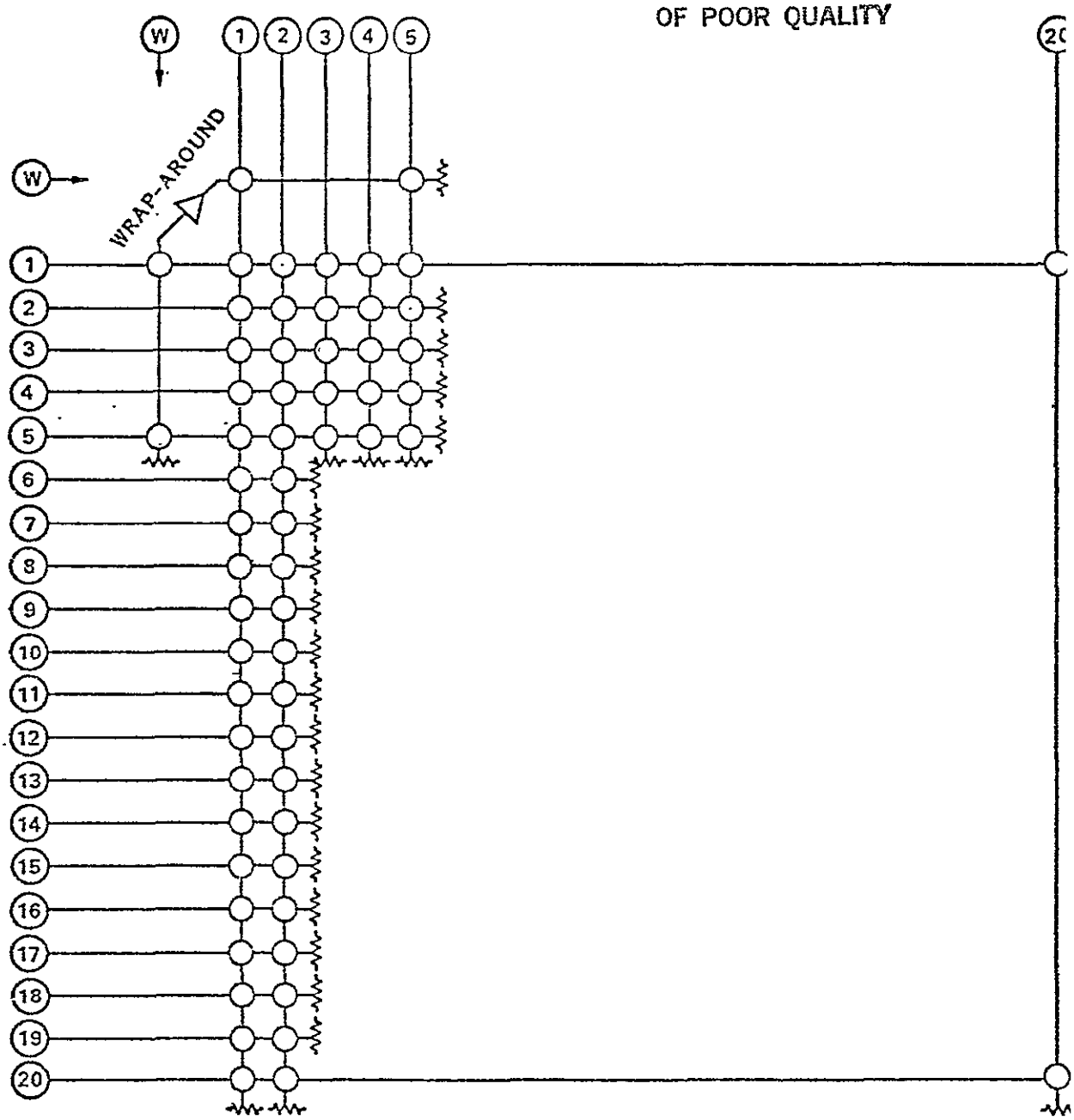


Figure 4.1.1-1. POC Switch Matrix Crosspoint Distribution

intermodulation and gain compression requirements. The analysis performed in determining signal level and noise figure performance in the design phase proved to be accurate as indicated by the POC test data.

4.2 TEST DATA ANALYSIS

The Detailed POC Model Test Plan specified the following parameters to be measured in order to verify the I.F. Switch Matrix performance.

- Microwave Parameters (Automated Network Analyzer Testing)
- Noise Figure
- Third Order Intermodulation
- Switching Speed
- Gain Compression

Test results of the above parameters are discussed in the following sections.

4.2.1 NETWORK ANALYZER TESTING

All of the POC crosspoints were characterized using the Hewlett Packard 8542B Automated Network Analyzer (ANA) in order to verify the functional performance of the switch matrix. The crosspoint amplifiers were initially tuned and tested as a single crosspoint on a manually operated frequency response test set, which is shown in Figure 4.2.5-1. The ANA served as a verification of the parameters determined by the scalar measurement method and provided information to confirm that the amplifier design had met or exceeded the predictions and specifications of phase linearity and VSWR. From ANA characterization, the following parameters were obtained for each of the switch matrix 61 crosspoints.

- Bandwidth
- Phase Linearity
- Insertion Loss
- Insertion Loss Ripple
- VSWR
- Isolation

Figure 4.2.1-1 shows a typical crosspoint ANA data plot before integration into the POC model. This crosspoint exhibits a 1 db bandwidth of 1 GHz at an insertion loss of approximately 12.6 db. After integration of the crosspoint into the POC model, the interconnect problem occurred and was corrected using the two welded ribbon wires. Addition of the ribbon wires, which are in series with the bandpass filter, detuned the crosspoint response as shown in Figure 4.2.1-2. Retuning of the crosspoint was completed without removing the two microwave integrated circuit substrates from the channel assembly. Results of the retuning are shown in Figure 4.2.1-3. Retuning had improved the bandpass and insertion loss; however, the crosspoint could not be retuned to the original band shape without removing the substrates from the channel. Since the interconnect problem was a process problem and not a technology problem, it was

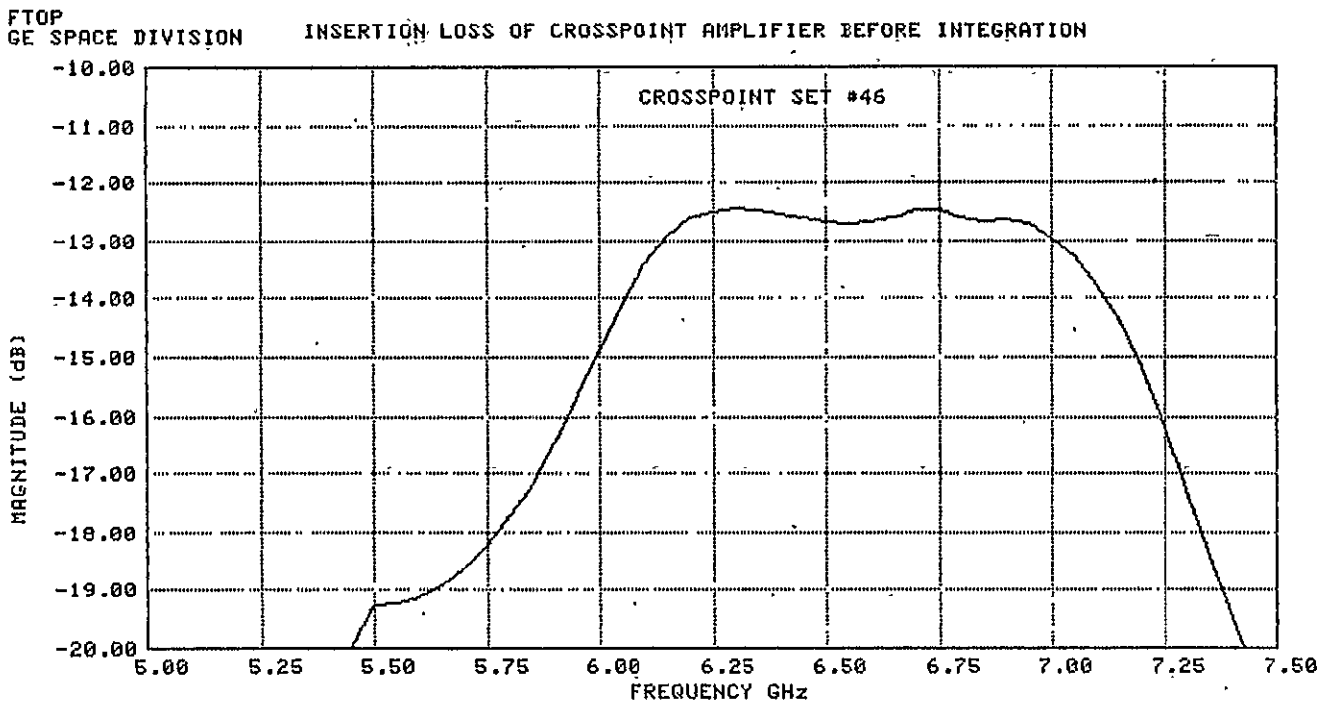


Figure 4.2.1-1. Frequency vs. Insertion Loss
(Pre-Integration)

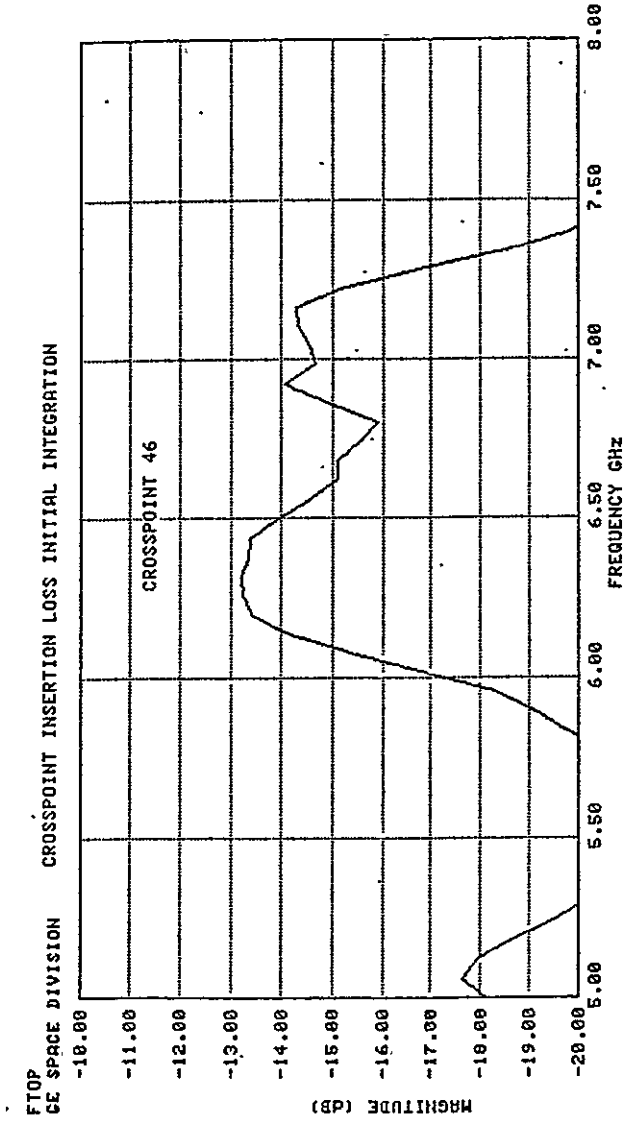


Figure 4.2.1-2. Frequency vs. Insertion Loss
(Post Integration)

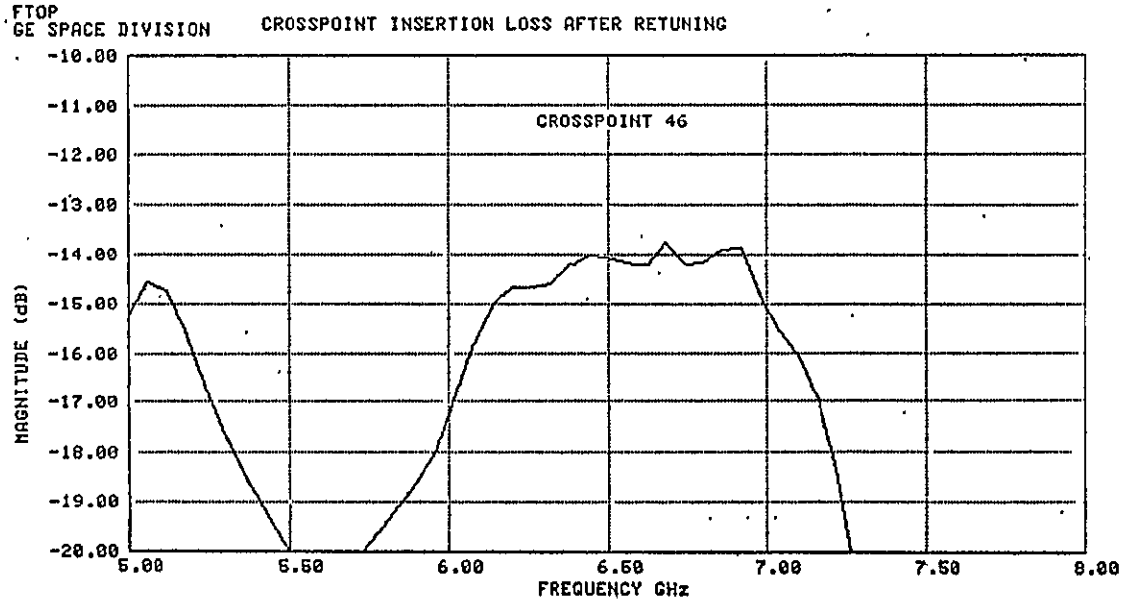


Figure 4.2.1-3. Frequency vs. Insertion Loss
(Post Retuning)

decided to retune 30 of the crosspoints without removing them from the channels. This decision was based on cost effectiveness.

The following figures illustrate the ANA data taken for each of the crosspoints in the POC model. Figure 4.2.1-4 shows bandwidth, insertion loss, and ripple. Figure 4.2.1-5 shows crosspoint nonlinear phase, Figure 4.2.1-6 input VSWR, and Figure 4.2.1-7 output VSWR. Additional data is included in Appendix A.

OFF state isolation measurements were made, using the ANA, on a selected number of crosspoints. Figure 4.2.1-8 shows a superimposed data plot with both stages ON as a reference of the crosspoint insertion loss vs. the input and output stages alternately turned OFF, and with both stages simultaneously turned OFF.

4.2.2 NOISE FIGURE

This test as outlined in the detailed test plan uses the Y factor method. A noise diode of known excess noise ratio is alternately turned on and off while monitoring the switch matrix output. The output on-to-off ratio is then related to noise figure and thence output signal-to-noise ratio. This test is performed in order to verify that the minimum output signal to noise ratio is greater than 35 dB. The noise figure of the total system shown in Table 4.2.2-1 is given by:

$$NF_T = 10 \log \frac{10^{\frac{ENR}{10}}}{10^{\frac{Y}{10}} - 1}$$

To calculate the noise figure of the crosspoint alone, the second stage contribution of the mixer must be

$$NF_1 = N_{FT} - \frac{NF_2 - 1}{G_1}$$

where

NF_T = Total system noise figure
ENR = Excess noise ratio of diode
Y = Y factor
NF_1 = Switch matrix noise figure
NF_2 = Mixer noise figure
G_1 = Gain of switch matrix

A representative path (3,3) will be used as an example.

Y = 0.34
NF_2 = 6.5 dB
ENR = 15.15 dB
G_1 = 16.5 dB

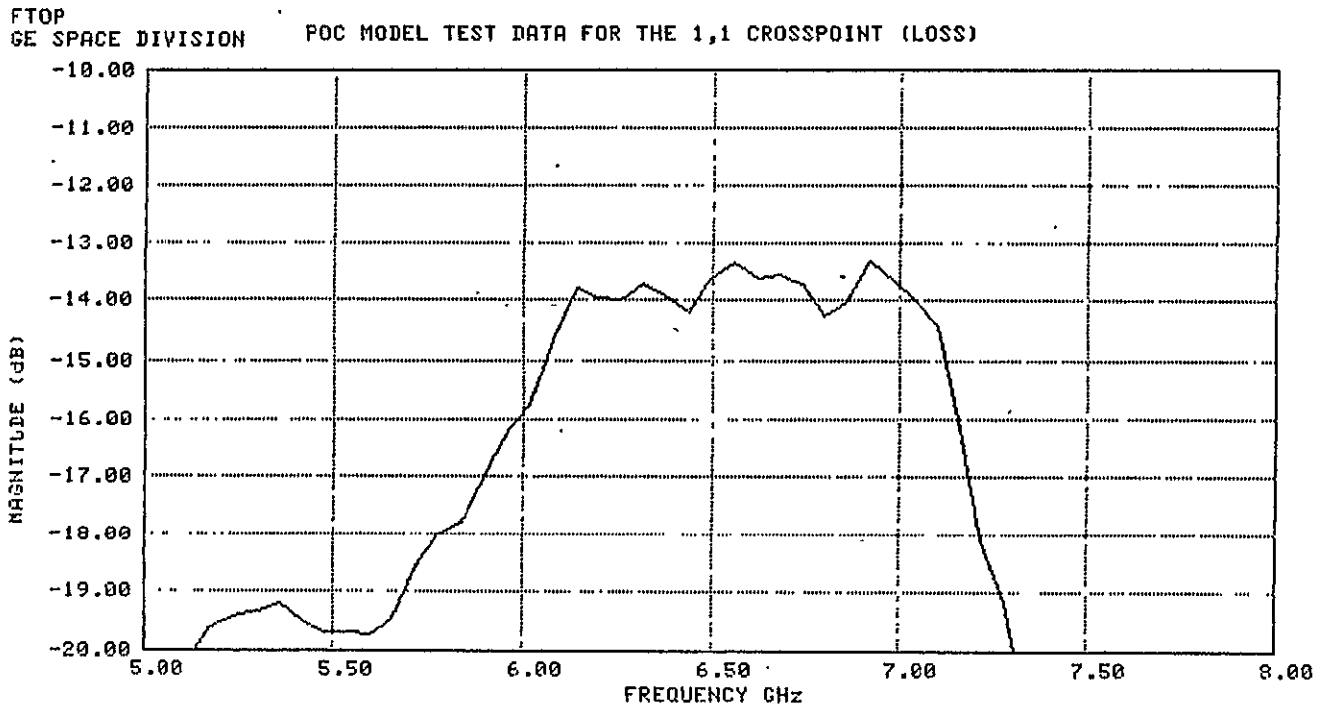


Figure 4.2.1-4. Frequency vs. Insertion Loss

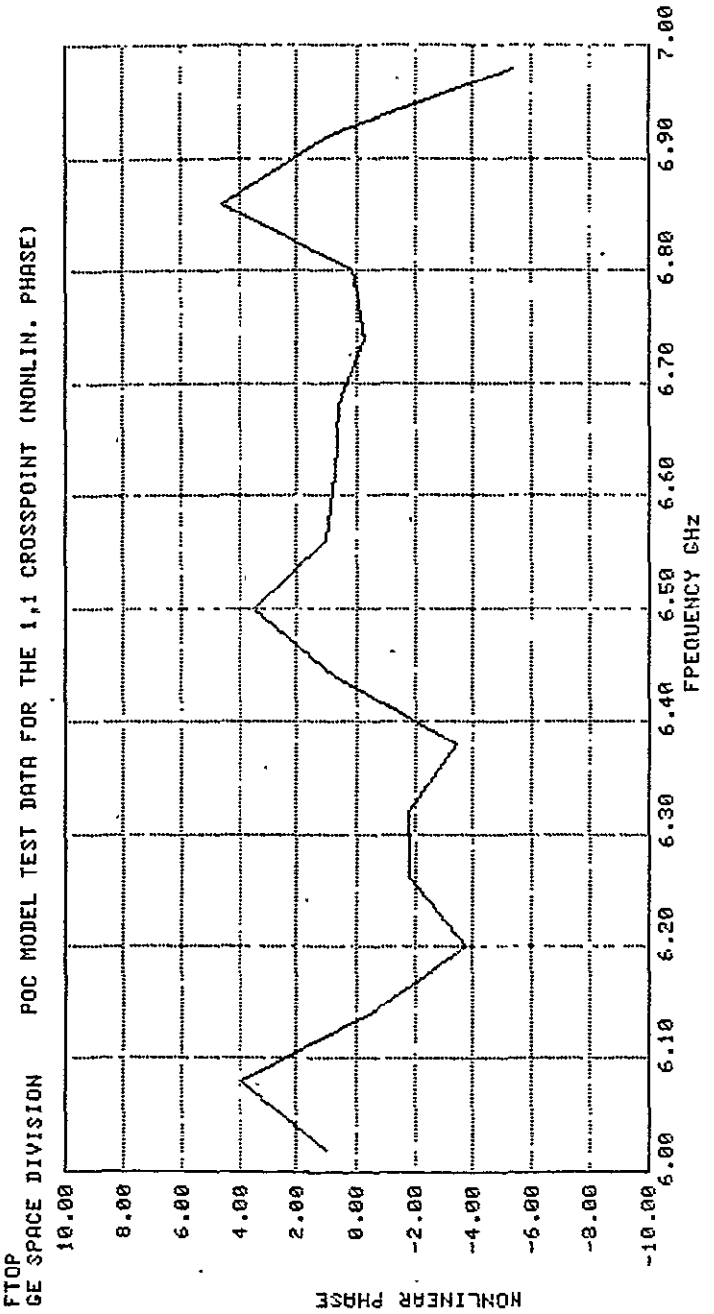


Figure 4.2.1-5. Frequency vs. Nonlinear Phase

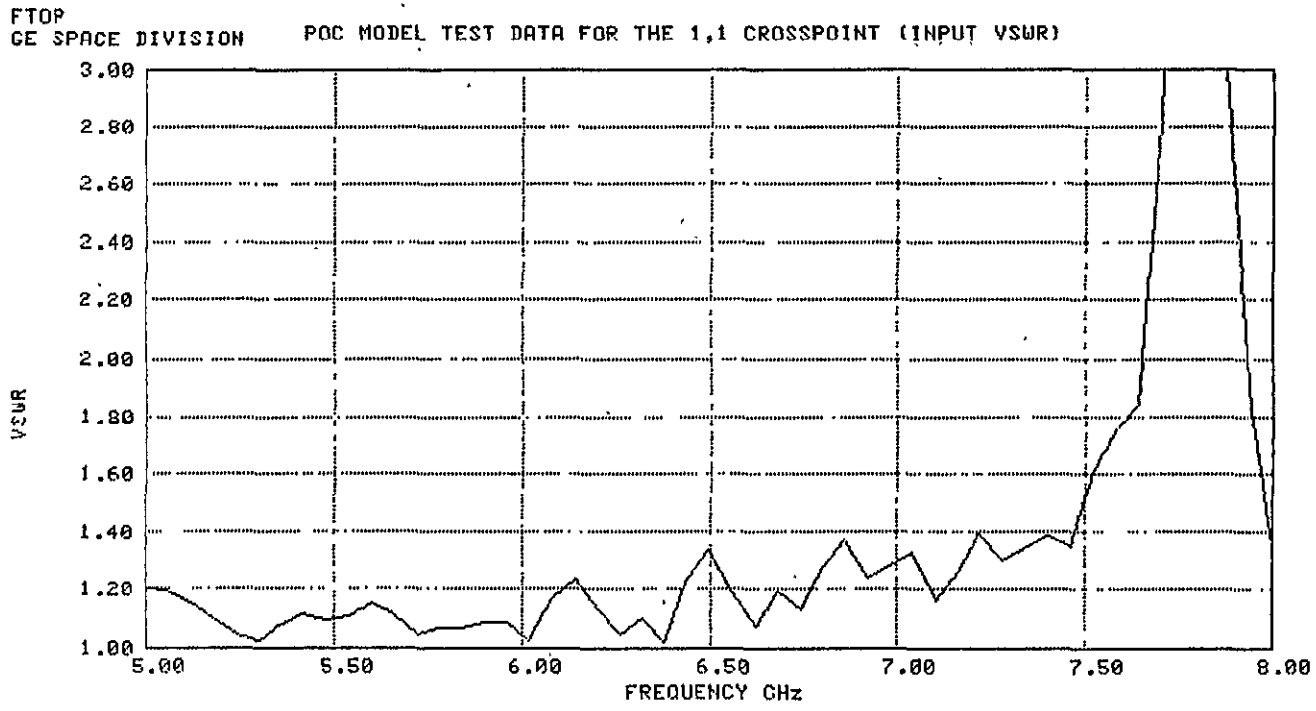


Figure 4.2.1-6. Frequency vs. Input VSWR

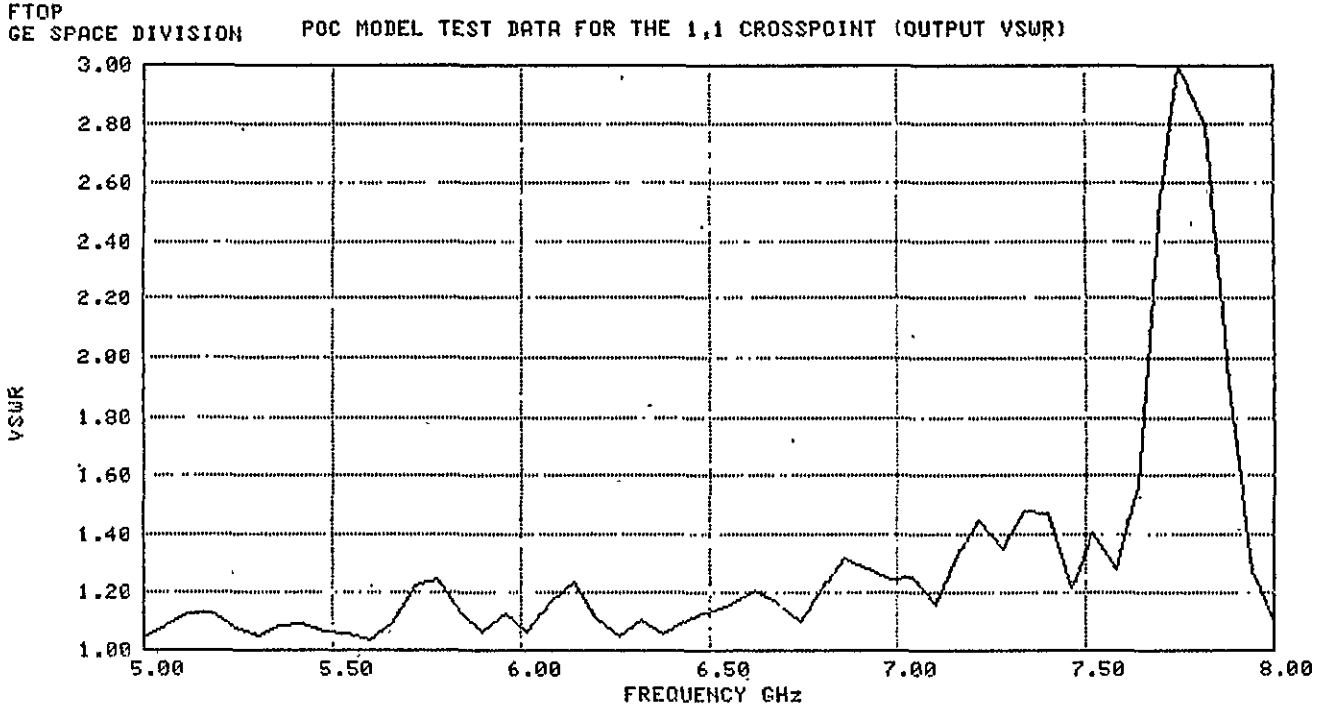


Figure 4.2.1-7. Frequency vs. Output VSWR

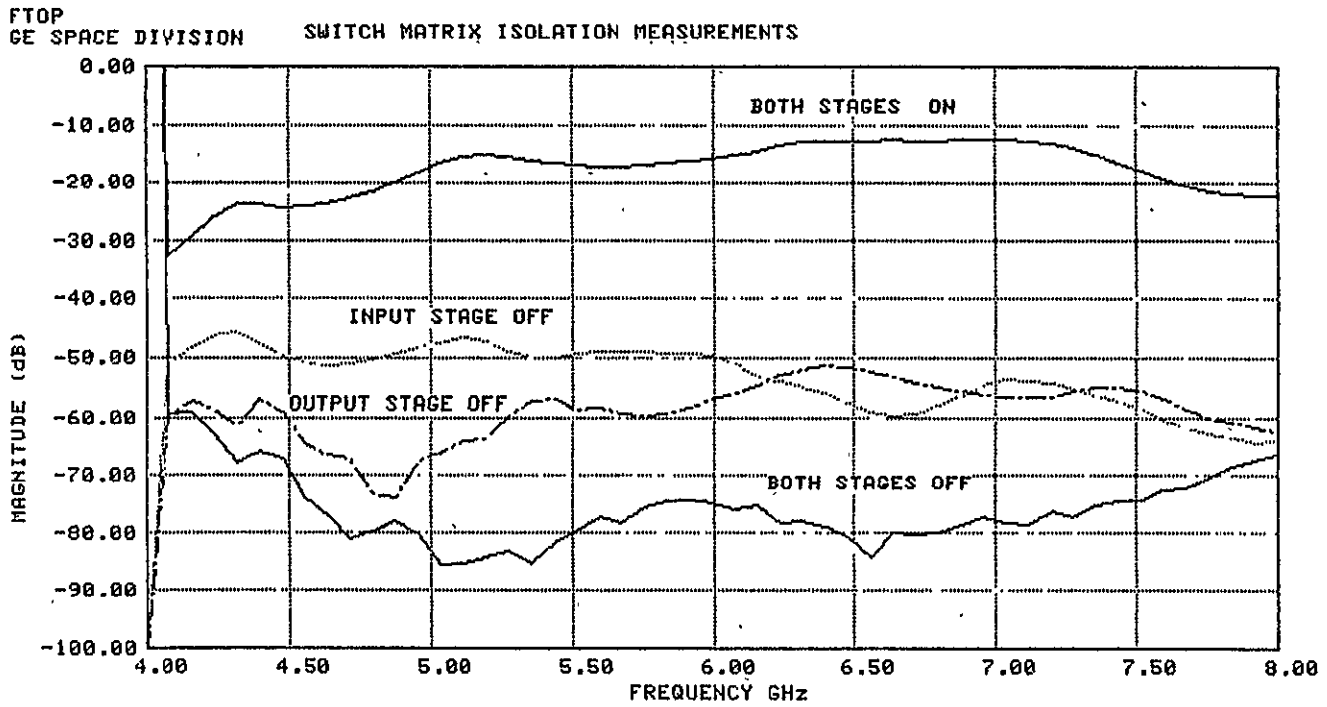


Figure 4.2.1-8. Frequency vs. Isolation

$$N_{FT} = 10 \text{ Log } \frac{10^{1.515}}{10^{0.034}-1}$$

$$= 10 \text{ Log } 402$$

$$= 26 \text{ dB}$$

$$NF_1 = 402 - \frac{4.47-1}{.022}$$

$$= 245.5$$

$$= 23.9 \text{ dB}$$

For a 1 GHz bandwidth, the noise power at the input is -84 dBm. The minimum signal power required for the above crosspoint to achieve a 35 dB signal to noise ratio is given by:

$$Si = S_o/N_o + NF + Ni$$

$$= 35 + 24 - 84$$

$$= -25 \text{ dBm}$$

In order to predict the worst case limit of noise figure performance that still maintains a 35 dB output signal to noise ratio, we restrict the minimum signal power to the range of -20 to -10 dBm. -10 dBm is about 10 dB below the 1 dB gain compression point, and our design goal is a 10 dB dynamic range of input signal level. From this condition we find that:

$$NF_{max} = Si - S_o/N_o - Ni$$

$$= -20 -35 +84 \text{ dBm}$$

$$= -29 \text{ dB}$$

Output signal to noise ratio given in Table 4.2.2-1 has been computed for an input signal level of -10 dBm or:

$$S_o/N_o = Si - Ni - NF$$

$$= 74 - NF$$

All calculations are performed for F = 6.5 GHz.

4.2.3 INTERMODULATION DISTORTION

The test equipment used for this measurement follows the setup suggested in the Detailed POC Test Plan. This setup is presented here for reference as Figure 4.2.3-1. Two synthesized signal generators are programmed at slightly different frequencies (F_1 = 6.500 GHz and F_2 = 6.501 GHz). The two signal levels are independently adjusted for 0 dBm input power to the Switch Matrix. A precision rotary vane attenuator is programmed to provide 0 and 10 dB attenuation to both signal paths. An H-P 8566A Spectrum Analyzer is used to

Table 4.2.2-1

Switch Matrix Noise Figure

Path	NF	S_o/N_o
1,1	23.0	51.0
2,2	22.6	51.4
3,3	23.9	50.1
4,4	22.7	51.3
5,5	26.6	47.4
5,4	23.5	50.5
5,3	23.3	50.7
5,2	24.2	49.8
5,1	25.3	48.7
1,2	23.6	50.4
1,3	22.8	51.2
1,4	24.6	49.4
1,5	23.4	50.6

measure the spectral output power of the switch matrix. The fundamental (F1 and F2) power is recorded in absolute power level (dBm). The IMD (2F1-F2 and 2F2-F1) power is recorded in dBc referenced to the fundamental signals. Previous predictions and earlier measurements indicated that the 1 dB Gain Compression Point would occur at 0 dBm, referred to the input. The design goal for the switch matrix was to achieve an IMD response better than -35 dBc for two signals at a power level that is 10 dB below the 1 dB Gain Compression Point. The data is presented in Table 4.2.3-1 for two input power levels, 0 and -10 dBm. The 2F1-F2 and 2F2-F1 products are shown in decibels below the desired fundamental signals (dBc). This shows that the design goal has been met or in many cases has been far exceeded. Figure 4.2.3-2 which was generated using the statistical averages of the IMD data, can be used to determine limits of input power and IMD performance. For instance, if the -35 dBc distortion requirement was the only factor limiting the input power level (disregarding gain compression temporarily), then the input power could be increased to -2.0 dBm, thus expanding the input dynamic range to about 20 dB. Conversely with the input dynamic range restricted between -10 and -20 dBm, the IMD performance is better than -50 dBc.

4.2.4 SWITCHING SPEED

Figure 4.2.4-1 shows a block diagram of the switching speed test setup. The switching speed measurement is accomplished by monitoring an output column with a sampling scope while toggling between two input rows, using the control logic. For example, Figure 4.2.4-2 was taken with the sampling scope monitoring output column 1 while the logic toggles between input rows 2 and 1. Included in the figure with the RF envelope is the control logic reconfiguration pulse. Switchin speed was defined by measurement of the RF envelope as shown in Figure 4.2.4-3.

Switching speed in the POC model was measured at an average value of 24.9 nsecond as compared to the breadboard measurement of 12 nseconds. Evaluation of the problem found that the row being turned off was switching at a faster rate in

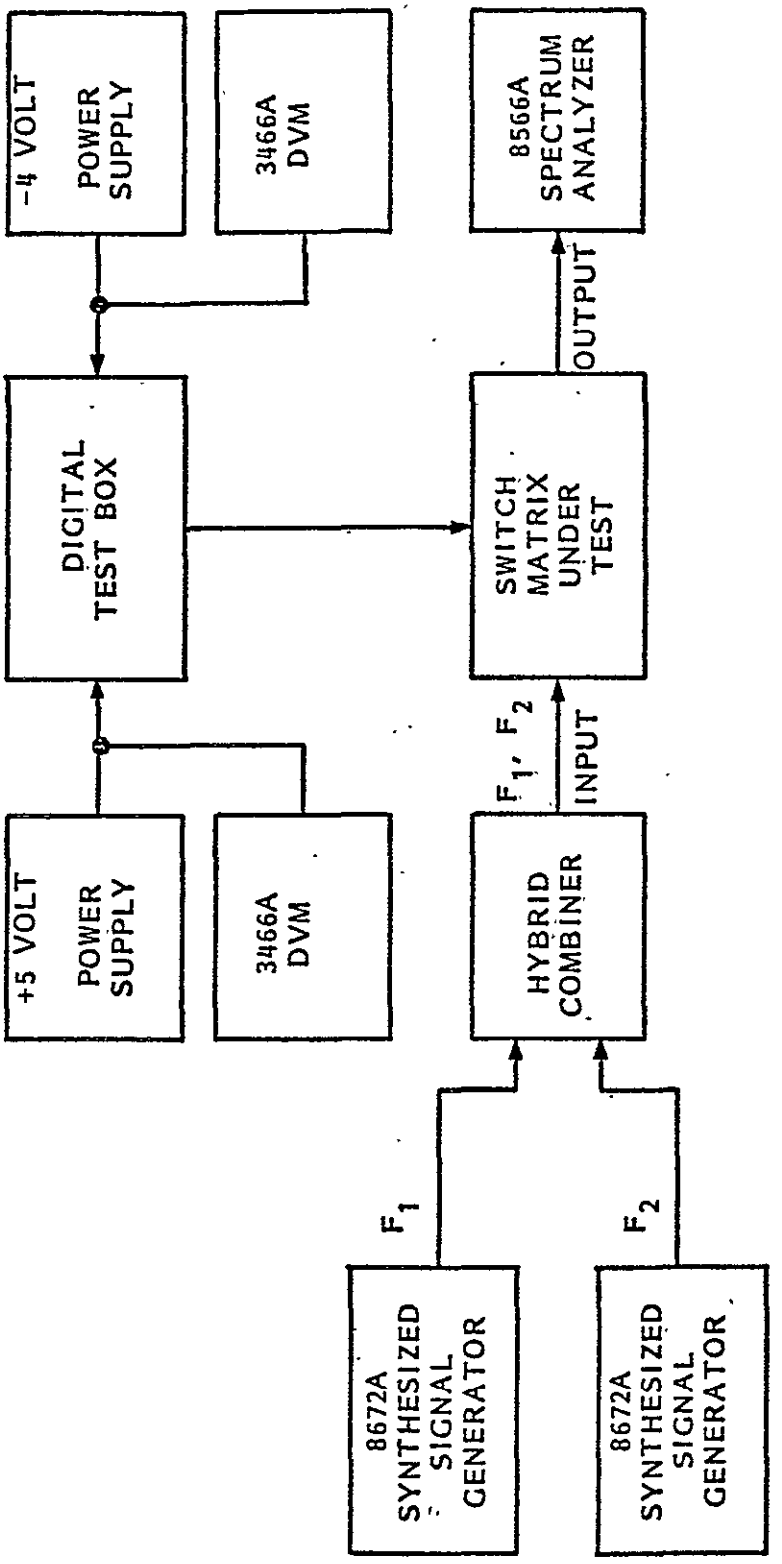


Figure 4.2.3-1. Intermodulation Distortion Test Set-Up

Table 4.2.3-1

Third Order Intermodulation

Crosspoint Path	IMD PRODUCTS			
	$2F_1-F_2$ (dBc)		$2F_2-F_1$ (dBc)	
	P1 = 0 dBm	-10 dBm	P1 = 0 dBm	-10 dBm
(1,1)	-31.3	-51.5	-30.9	-52.0
(1,2)	-34.7	-56.0	-34.4	-55.0
(1,3)	-35.9	-54.8	-35.9	-55.4
(1,4)	-37.7	-55.8	-37.6	-56.0
(1,5)	-31.2	-52.5	-31.0	-52.0
(1,20)	-44.5	-61.0	-44.3	-61.0
(2,5)	-26.3	-50.3	-26.3	-51.0
(2,2)	-25.5	-49.8	-25.5	-49.4
(2,1)	-30.5	-51.7	-30.4	-51.9
(3,1)	-25.8	-49.1	-25.7	-49.6
(3,3)	-37.2	-54.8	-37.1	-55.7
(3,5)	-28.3	-51.5	-28.2	-51.5
(4,5)	-31.4	-53.1	-31.3	-52.8
(4,4)	-24.5	-43.7	-24.3	-44.0
(4,1)	-30.6	-46.8	-29.9	-45.9
(5,1)	-31.4	-53.3	-31.1	-51.9
(5,2)	-28.1	-50.9	-28.2	-51.3
(5,3)	-25.6	-48.7	-25.4	-48.3
(5,4)	-31.5	-54.0	-31.5	-53.9
(5,5)	-35.6	-53.7	-35.0	-54.6
(10,1)	-21.4	-45.0	-21.3	-45.2
(10,2)	-33.6	-53.2	-33.4	-54.0
(15,2)	-41.8	*	-41.4	-59.0
(15,1)	-34.4	-56.7	-34.3	-55.0
(20,1)	-28.8	-54.0	-28.7	-54.0
(20,2)	-25.9	-38.3	-25.8	-37.8
(20,20)	-54.2	*	-51.7	*

*Not accurately measurable ($\geq$-59 dBc)

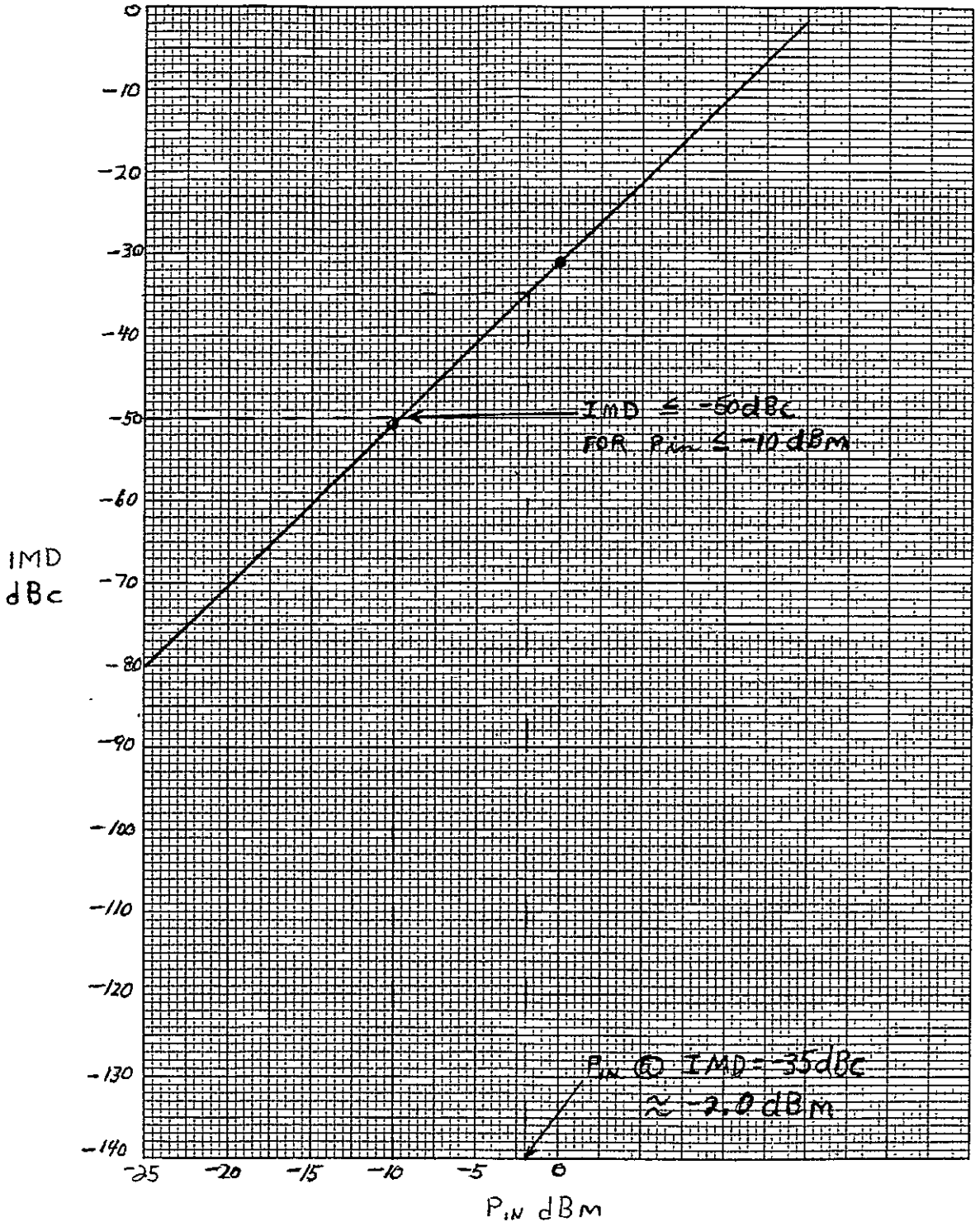


Figure 4.2.3-2. P_{IN} vs. IMD

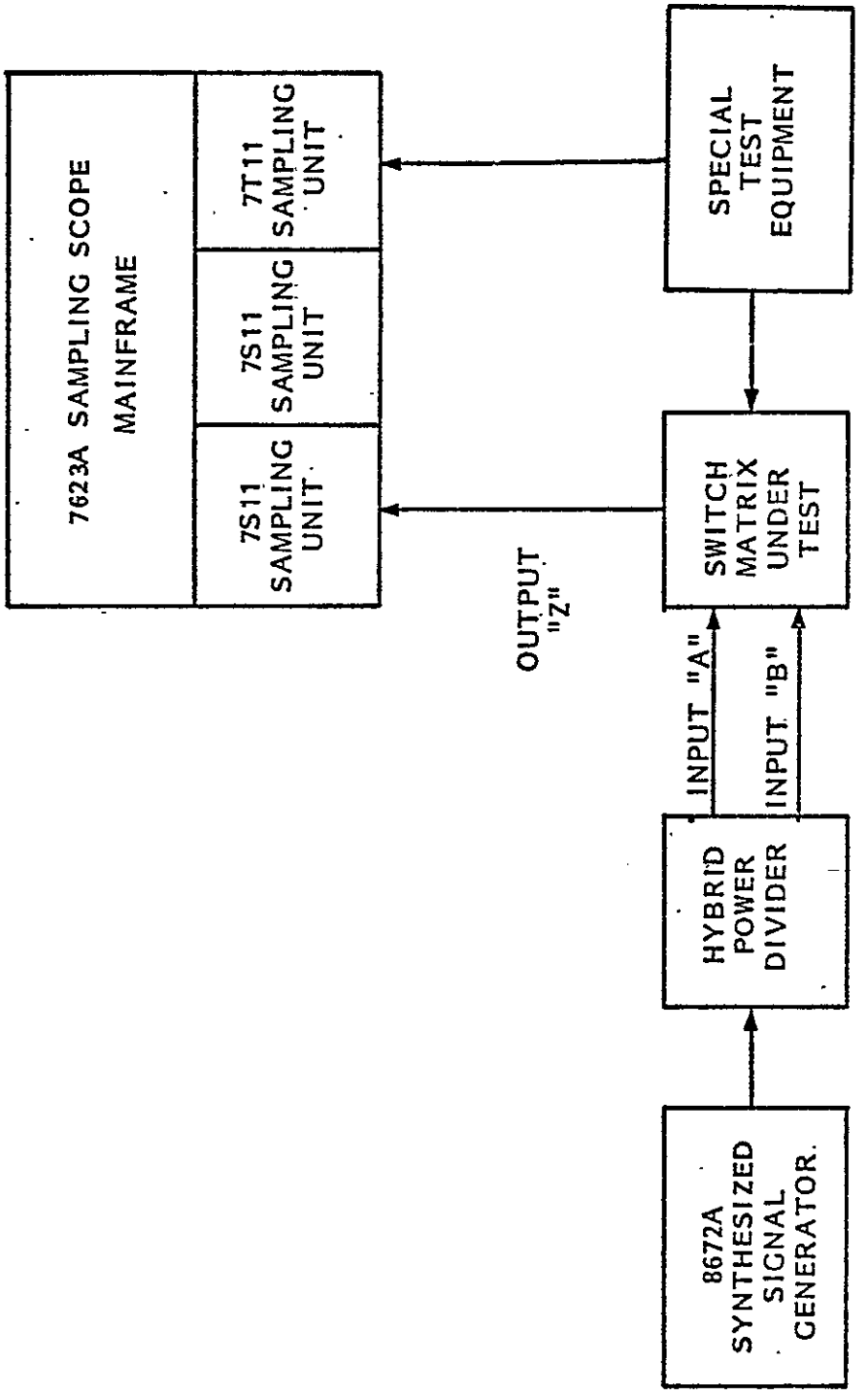


Figure 4.2.4-1. Switching Speed Test Set-Up

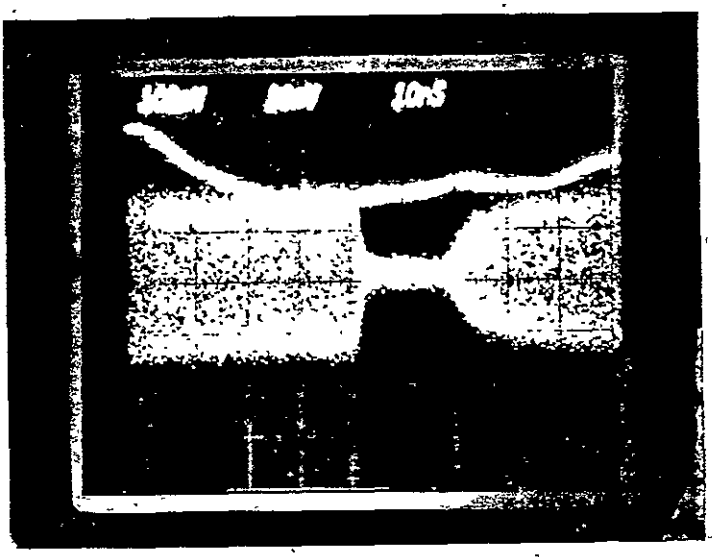


Figure 4.2.4-2. Switching Speed Measurement

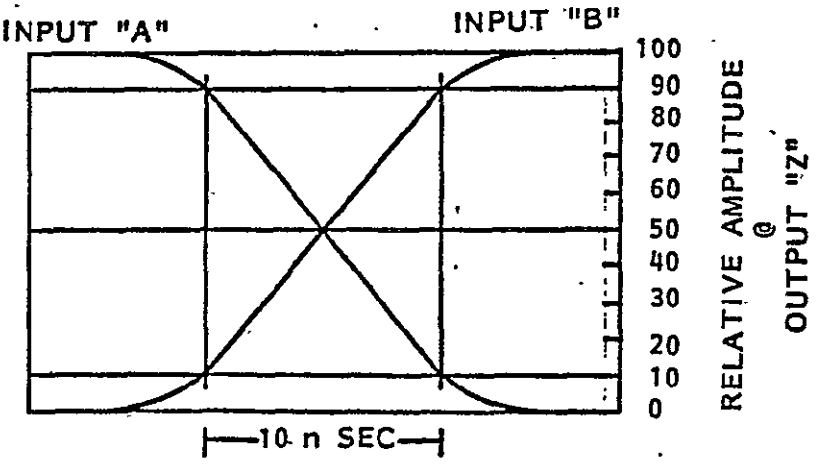


Figure 4.2.4-3. Switching Speed Definition

the POC model (Figure 4.2.4-4) due to the reduction of stray capacitances between the logic switch drivers and the gate circuit of the switching RF GaAs FETs. Figure 4.2.4-4 also shows the switch driver pulse that controls the gate of the GaAs FET. Since the POC model GaAs FET is switching off faster than the breadboard, by definition of switching speed the result is an increase of switching speed. The other cause of increased switching speed is due to the turn-on gate bias range of the GaAs FET. Figure 4.2.4-5 shows the gate logic control pulse in relationship to the RF envelope of the FET that was turned on. The difference in switching speed was found to be caused by the narrow range of GaAs FET gate voltage vs. gain at the top of the bias/gain curve. In the off state the GaAs FET gate is biased at -4 VDC, whereby the bias is switched to approximately -0.5 VDC for the on state. Full amplifier turn-on does not occur until the gate bias reaches approximately 95% of its final value. The slope of the turn-on voltage time constant therefore controls the switch on time of the GaAs FET. Switching the GaAs FET off is accomplished within 3 nseconds. This problem can be resolved by additional design effort within the logic switch driver and GaAs FET bias circuits. It was considered a design problem and not a technology problem, therefore rework of the switch crosspoints was not considered cost effective at this time.

4.2.5 GAIN COMPRESSION

One dB gain compression as a function of frequency measurements were performed using the test set-up as shown in Figure 4.2.5-1. This set-up is the conventional frequency response arrangement which is discussed in detail in H-P Application Note 155 with two exceptions. First, B/R (loss) is displayed on the left channel simultaneously with B (P_{out}) on the right channel. The reasoning behind this will be apparent later. Secondly, the normalizer is used to store the small signal loss of the crosspoint under test. The normalizer is used to display the loss-memory. This establishes a reference line since loss and memory input are equal. As the power level is increased, the crosspoint/amplifier begins to compress increasing the loss and hence causes the loss-memory trace to deflect from the reference position. The power level at which this deflection reaches 1 dB in any portion of the 1 GHz bandwidth is defined as the 1 dB compression point. The output power is measured directly with the B detector. The input power level is determined by adding the loss of switch (small signal) to the output power.

The 1 dB gain compression point measurements were made on a representative sample of crosspoints. The data of Table 4.2.5-1 are the results of these measurements. Compression was observed first for the higher frequency as expected since the device gain decreases with frequency. The input power required for 1 dB gain compression is nominally between -1 and 0 dBm, which agrees with previous predictions and observations made during IMD measurements where the input power level was programmed to 0 and -10 dBm.

4.2.6 STATISTICAL ANALYSIS

The previously mentioned performance parameters of the POC model switch matrix will now be examined in more detail. The statistics of the observations are useful in predicting limits for the performance parameters of a fully populated matrix.

Table 4.2.6-1 is a summary of the POC model test data statistics. Given for each performance parameter are the specification value, the sample size, the

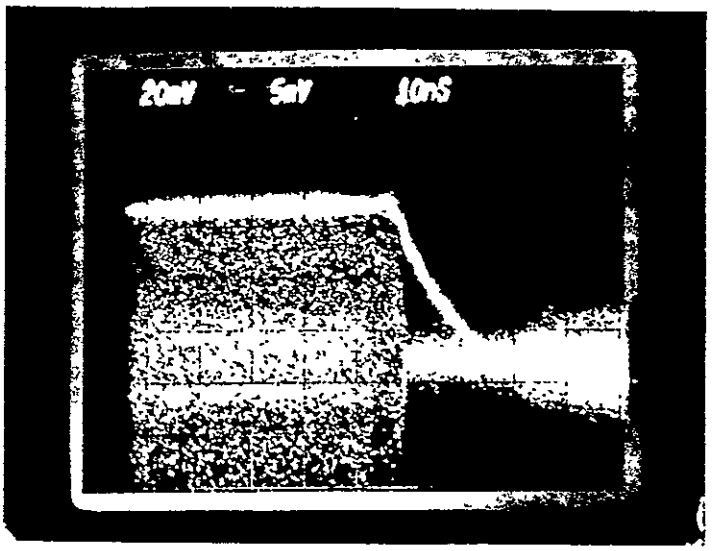


Figure 4.2.4-4. Switching Crosspoint "Off"

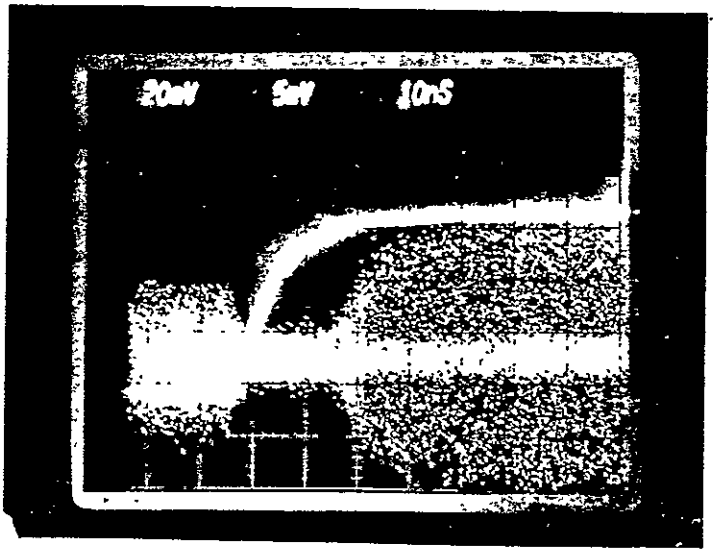


Figure 4.2.4-5. Switching Crosspoint "On"

Figure 4.2.5-1. Frequency Response & Gain Compression Test Set

Table 4.2.5-1

Path	P_{out} @ 1 dB Compression	S.S.L.	$P_{in}=P_{out}-SSL$
1,1	-14.0	13.0	-1.0
1,2	-15.0	14.3	-0.7
1,3	-16.0	14.1	+1.9
1,4	-15.0	15.5	+0.5
1,5	-13.4	13.5	+0.1
1,20	-15.2	17.9	+2.7
2,4	-16.3	14.2	-2.1
2,3	-15.2	14.8	-0.4
2,2	-17.8	13.3	-4.5
2,1	-17.6	13.7	-3.9
2,5	-18.0	13.7	-4.3
3,5	-14.0	-13.7	-0.3
3,4	-13.0	-15.2	+1.8
3,3	-14.0	-15.2	+0.8
3,2	-15.0	-15.2	+0.2
3,1	-18.0	-13.0	-5.0
4,1	-18.0	-14.0	-4.0
4,2	-17.0	-14.5	-2.5
4,3	-17.0	-18.0	+1.0
4,4	-17.0	-14.0	-3.0
4,5	-15.0	-14.5	-0.5
5,5	-15.4	-17.5	+2.1
5,4	-16.4	-16.2	-0.2
5,3	-16.0	-13.8	-2.2
5,2	-15.0	-14.2	-0.8
5,1	-15.0	-15.6	+0.6
10,1	-18.0	-13.7	-4.3
10,2	-16.7	-17.9	+1.2
15,1	-17.7	-21.0	+3.3
15,2	-16.7	-21.1	+4.3
20,2	-18.7	-19.9	+1.2

Table 4.2.6-1

POC Model Test Data Statistical Summary

	Spec Value	N	$\bar{X}$	Range Min.	Range Max.	Confidence Limits (1)		σ	Prediction Limits (2)		Tolerance Limits (3)	
Center Frequency	3-8 GHz	30	6.52	6.25	6.73	6.48	6.56	0.11	6.29	6.74	6.24	6.79
Bandwidth 1 dB	1.0 GHz	30	0.95	0.8	1.2	0.92	0.99	0.11	0.74	1.17	0.69	1.22
Bandwidth 3 dB	1.0 GHz	30	1.24	1.05	1.42	1.20	1.28	0.11	1.01	1.47	0.96	1.52
Insertion Loss	15 dB	30	16.1	13.5	21.3	15.3	16.9	2.17	11.6	20.6	10.6	21.7
Gain Ripple	1.0 dB	13	1.1	0.5	1.8	0.86	1.32	0.38	0.22	1.95	0	2.3
Input VSWR	1.2	13	1.3	1.2	1.4	1.31	1.38	0.06	1.22	1.47	1.17	1.52
Output VSWR	1.2	13	1.4	1.2	1.5	1.34	1.45	0.1	1.18	1.61	1.10	1.69
Signal/Noise	35 dBc	13	50.2	47	51	49.4	50.9	1.21	47.4	52.9	46.4	53.9
Noise Figure	(TBD) dB	13	23.9	23	27	23.2	24.6	1.19	21.2	26.6	20.3	27.6
Non-linear Phase	$\pm 5^{\circ}$	13	8.85	5	20	6.4	11.3	3.99	-0.2	17.9	-3.5	21.2
Intermod Distoration	35 dBc	13	52	44	56	49.9	54.1	3.44	44.2	59.8	41.4	62.6
Gain Compression 1 dB	(TBD) dBm	13	-0.58	-4.5	2.1	-1.70	0.53	1.85	-4.76	3.6	-6.29	5.12
Switching Speed	10 nsecs	16	24.9	17	32	22.8	27.1	4.0	16.2	33.7	13.3	36.5

(1) 95% confidence limits on the population mean
(2) 95% prediction limits to contain the next observation
(3) 95% approximate tolerance limits to contain 95% of the population

sample mean, limits of the 95% confidence interval on the population mean, sample standard deviation, limits for the 95% confidence level of predicting the next observation, and finally tolerance limits to contain 95% of the population with a 95% confidence level. It can be seen from this table that while the sample mean may meet or exceed the design goals, the range of the parameters is such that some observations are below the design goal. Deviation from the specification is indicative of the process problems incurred during final integration.

The crosspoint/amplifier small signal parameters of insertion loss, ripple, bandwidth and nonlinear phase are all interdependent. It was apparent from the breadboard switch that the gain of the amplifier would have to be increased which resulted in a reduction of bandwidth. Ripple and nonlinear phase are known to be interrelated, however, the computer aided modelling performed in the POC design indicated that there was also a tradeoff between ripple and insertion loss. With a high Q device such as the dual gate GaAs FET, there would be a high SWR present in the interstage and represents large ripples in the gain shape. The ripple was decreased by inserting a small value series resistor in the interstage, resulting in a subsequent reduction of gain. Thus gain, bandwidth, ripple and nonlinear phase were carefully traded off to insure the optimum design.

Input and output VSWR are dependent on the quality of the termination and the input connector as well as the coupling factor and the number of couplers in the channel. The termination and connector were measured together and were found to be better than a 1.11:1 VSWR. A mismatch of this magnitude in the mainline of the coupler will be enough to cause the design goal to be exceeded. As was evidenced by the breadboard effort there are many sources of mismatch associated with the directional coupler, but with the proper choice of interconnecting lengths these sources are designed to constructively add at frequencies out of band. This was also apparent from the parametric tradeoff studies. The VSWR figures of Section 4.2.1 show that the resonant frequencies of the coupler discontinuity are indeed out of band; however, the base of the peak at 7.75 GHz is rather broad which leads to an undesirable increase in the VSWR in the 6.0-7.0 GHz band.

A histogram for each of the parameters indicating the specific observations are shown in the following figures.

4.3 POC MODEL FUNCTIONAL REQUIREMENTS AND TEST RESULTS COMPARISON

Table 4.3-1 lists the POC model performance requirements, the sample mean for each parameter, and the expected results from analysis of the design.

Gain, bandwidth, phase linearity, and ripple were carefully traded off to insure an optimum design. Expected values for these parameters based on the design model are 11 dB insertion loss nominal, 1.0 GHz bandwidth minimum, 1 dB ripple (.5 dB maximum over 500 MHz), and $\pm 8^{o}$ phase linearity. The measured results confirm that the design concept has been implemented quite well. Input and output VSWR does exceed the design goal and earlier prediction in a narrow band sense; however, the measured results generally follow the prediction of the coupled crossbar model over the I.F. range of 3-8 GHz. The reason for the disagreement can be seen by examining Figure 4.3-1.

SAMPLE STATISTICS FOR FO

NO. OF OBSERVATIONS	30
AVERAGE:	6.51733
STANDARD DEVIATION:	0.10736
SMALLEST OBSERVATION:	6.25000
LARGEST OBSERVATION:	6.73000

FREQ	CELL LOWER ENDPT	
0	6.150	
0	6.200	
1	6.250	*
1	6.300	*
0	6.350	
4	6.400	****
8	6.450	********
4	6.500	****
3	6.550	***
6	6.600	******
1	6.650	*
2	6.700	**
0	6.750	
0	6.800	

Figure 4.2.6-2. Center Frequency (GHz)

SAMPLE STATISTICS FOR BW1

NO. OF OBSERVATIONS	30
AVERAGE:	0.95467
STANDARD DEVIATION:	0.10454
SMALLEST OBSERVATION:	0.80000
LARGEST OBSERVATION:	1.20000

FREQ	CELL LOWER ENDPT	
	BELOW	
0	0.500	
0	0.500	
0	0.550	
0	0.600	
0	0.650	
0	0.700	
0	0.750	
5	0.800	*****
5	0.850	*****
1	0.900	*
6	0.950	******
7	1.000	*******
2	1.050	**
3	1.100	***
0	1.150	
1	1.200	*
0	1.250	
0	1.300	
0	1.350	
0	1.400	
0	1.450	
0	1.500	
0	1.550	
0	1.600	
	ABOVE	
0	1.650	

Figure 4.2.6-3. 1 dB Bandwidth (GHz)

SAMPLE STATISTICS FOR BW3

NO. OF OBSERVATIONS	30
AVERAGE:	1.24000
STANDARD DEVIATION:	0.10954
SMALLEST OBSERVATION:	1.05000
LARGEST OBSERVATION:	1.42000

FREQ	CELL LOWER ENDPT	
	BELOW	
0	0.500	
0	0.500	
0	0.550	
0	0.600	
0	0.650	
0	0.700	
0	0.750	
0	0.800	
0	0.850	
0	0.900	
0	0.950	
0	1.000	
3	1.050	***
2	1.100	**
4	1.150	****
7	1.200	*******
4	1.250	****
3	1.300	***
2	1.350	**
5	1.400	*****
0	1.450	
0	1.500	
0	1.550	
0	1.600	
	ABOVE	
0	1.650	

Figure 4.2.6-4. 3 dB Bandwidth (GHz)

SAMPLE STATISTICS FOR IL

NO. OF OBSERVATIONS	30
AVERAGE:	15.12000
STANDARD DEVIATION:	2.16928
SMALLEST OBSERVATION:	13.30000
LARGEST OBSERVATION:	21.30000

FREQ	CELL LOWER ENDPT	
	BELOW	
0	10.00	
0	10.00	
0	11.00	
0	12.00	
1	13.00	*
10	14.00	**********
6	15.00	******
5	16.00	*****
3	17.00	***
1	18.00	*
1	19.00	*
1	20.00	*
2	21.00	**
0	22.00	
0	23.00	
0	24.00	
0	25.00	
	ABOVE	
0	26.00	

Figure 4.2.6-5. Insertion Loss (dB)

SAMPLE STATISTICS FOR RP

NO. OF OBSERVATIONS	13
AVERAGE:	1.08462
STANDARD DEVIATION:	0.38045
SMALLEST OBSERVATION:	0.50000
LARGEST OBSERVATION:	1.80000

FREQ	CELL LOWER ENDPT	
	BELOW	
0	0.40	
0	0.40	
2	0.50	++
0	0.60	
1	0.70	+
0	0.80	
0	0.90	
4	1.00	++++
1	1.10	+
0	1.20	
2	1.30	++
1	1.40	+
1	1.50	+
0	1.60	
0	1.70	
1	1.80	+
0	1.90	
0	2.00	
	ABOVE	
0	2.10	

Figure 4.2.6-6. Gain Ripple (dB)

SAMPLE STATISTICS FOR VF

NO. OF OBSERVATIONS	13
AVERAGE:	1.34231
STANDARD DEVIATION:	0.05644
SMALLEST OBSERVATION:	1.21000
LARGEST OBSERVATION:	1.43000

FREQ	CELL LOWER ENDPT	
	BELOW	
0	1.190	
1	1.190	*
0	1.230	
1	1.270	*
4	1.310	****
5	1.350	*****
1	1.390	*
1	1.430	*
0	1.470	
	ABOVE	
0	1.510	

Figure 4.2.6-7. Input VSWR

SAMPLE STATISTICS FOR VR

NO. OF OBSERVATIONS	13
AVERAGE:	1.39385
STANDARD DEVIATION:	0.09527
SMALLEST OBSERVATION:	1.21000
LARGEST OBSERVATION:	1.53000

FREQ	CELL LOWER ENDPT	
	BELOW	
0	1.190	
1	1.190	*
0	1.230	
1	1.270	*
2	1.310	**
2	1.350	**
3	1.390	***
1	1.430	*
0	1.470	
3	1.510	***
0	1.550	
	ABOVE	
0	1.590	

Figure 4.2.6-8. Output VSWR

SAMPLE STATISTICS FOR SN

NO. OF OBSERVATIONS	13
AVERAGE:	50.15385
STANDARD DEVIATION:	1.21423
SMALLEST OBSERVATION:	47
LARGEST OBSERVATION:	51

FREQ	CELL LOWER ENDPT	
	BELOW	
0	45	
0	45	
0	46	
1	47	*
0	48	
2	49	**
3	50	***
7	51	*******
0	52	
0	53	
0	54	
0	55	
	ABOVE	
0	56	

Figure 4.2.6-9. Signal/Noise Ratio (dBc)

SAMPLE STATISTICS FOR NF

NO. OF OBSERVATIONS	13
AVERAGE:	23.32308
STANDARD DEVIATION:	1.18754
SMALLEST OBSERVATION:	23
LARGEST OBSERVATION:	27

FREQ	CELL LOWER ENDPT	
	BELOW	
0	20	
0	20	
0	21	
0	22	
6	23	******
4	24	****
2	25	**
0	26	
1	27	*
0	28	
0	29	
0	30	
	ABOVE	
0	31	

Figure 4.2.6-10. Noise Figure (dBm)

SAMPLE STATISTICS FOR NP

NO. OF OBSERVATIONS	13
AVERAGE:	8.84615
STANDARD DEVIATION:	3.99679
SMALLEST OBSERVATION:	5
LARGEST OBSERVATION:	20

FREQ	CELL LOWER ENDPT	
	BELOW	
0	4	
2	4	**
3	6	***
4	8	****
2	10	**
1	12	*
0	14	
0	16	
0	18	
1	20	*
0	22	
	ABOVE	
0	24	

Figure 4.2.6-11. Nonlinear Phase (deg.)

SAMPLE STATISTICS FOR ID

NO. OF OBSERVATIONS	13
AVERAGE:	52.00000
STANDARD DEVIATION:	3.43996
SMALLEST OBSERVATION:	44
LARGEST OBSERVATION:	56

FREQ	CELL LOWER ENDPT	
	BELOW	
0	42	
0	42	
1	44	*
0	46	
2	48	**
2	50	**
2	52	**
5	54	*****
1	56	*
0	58	
	ABOVE	
0	60	

Figure 4.2.6-12. Intermod Distoration (dBc)

SAMPLE STATISTICS FOR CM

NO. OF OBSERVATIONS	13
AVERAGE:	-0.58462
STANDARD DEVIATION:	1.85061
SMALLEST OBSERVATION:	-4.50000
LARGEST OBSERVATION:	2.10000

FREQ	CELL LOWER ENDPT	
	BELOW	
0	-5.00	
0	-6.00	
1	-5.00	*
0	-4.00	
2	-3.00	**
0	-2.00	
5	-1.00	*****
3	0.00	***
1	1.00	*
1	2.00	*
0	3.00	
0	4.00	
0	5.00	
0	6.00	
	ABOVE	
0	7.00	

Figure 4.2.6-13. Gain Compression (dBm)

SAMPLE STATISTICS FOR SWSPEED

NO. OF OBSERVATIONS	16
AVERAGE:	24.93750
STANDARD DEVIATION:	3.99114
SMALLEST OBSERVATION:	17
LARGEST OBSERVATION:	32

FREQ	CELL LOWER ENDPT	
	BELOW	
0	16	
1	16	*
1	18	*
0	20	
3	22	***
3	24	***
4	26	****
2	28	**
1	30	*
1	32	*
0	34	
	ABOVE	
0	36	

Figure 4.2.6-14. Switching Speed (nsecs).

Table 4.3-1

Parameter	Requirement	Result Expected	Result Achieved
I.F.	3-8 GHz	6.25 GHz	6.52 GHz
Bandwidth (1 dB)	1.0 GHz min	1.0 GHz min	0.95 GHz
Insertion Loss	15 dB max	11 dB	16.1 dB
Ripple	1.0 dB max	1.0 dB max	1.1 dB
VSWR (FWD)	1.2:1 max	1.2:1 max	1.3:1
VSWR (REV)	1.2:1 max	1.2:1 max	1.4:1
S/N	35 dB min	35 dB min	50 dB
Noise Figure	N/A	24 dB nom.	24 dB
Nonlinear Phase	$\pm 5^{o}$ max	$\pm 8^{o}$ nom.	$\pm 8.8^{o}$
Third Order IMD.	N/A	35 dBc max	52 dBc
1 dB Compression (Input)	N/A	0 dBm	-0.6 dBm
Switching Time	10 nS max	10 nS max	25 nS

Figure 4.3-1 is a representative of the topology model used to simulate the coupled crossbar mainline. The terminations are considered ideal. Since a 20 dB return loss termination is employed, this is a valid assumption. To assess the worst case mainline VSWR, a 1 ohm resistor was used to simulate a high reflection coefficient amplifier. The resistor does not allow for a relative phase shift which would normally occur due to FET device variations. The model does not include any inductance that results from the interconnecting ribbon weld. By trying to maintain equal spacing between adjacent carriers and hence the periodic nature of the structure, the effect of the discontinuity should be a minimum at 6 GHz and maximum at 7 and 8 GHz. The results show that the maximum VSWR occurred at 7.8 GHz and by analysis there should be a maximum at 3.9 GHz. The slight deviation from the expected results is attributed to the process related problem. The shift of the peak to 7.8 GHz and the shift of the amplifier passband center frequency to 6.5 GHz contribute to excessive VSWR. This is seen from the fact that the maximum VSWR occurs at the upper edge of the passband. Noise figure, third order IMD, and 1 dB compression were all well within expectations based on the performance of the breadboard. Switching time represents the most significant departure from the design goals, and the breadboard results. The actual rise and fall times of the switch were improved over the breadboard effort while having the effect of increasing the switching time.

Figure 4.3-1. Mainline Coupled Crossbar Model

SECTION 5.0.

CRITICAL REVIEW OF POC DESIGN

Experience in the fabrication and test of the POC model have indicated features of the present design to be evaluated prior to the design of a flight model switch matrix. Some of these considerations were analyzed during the Task I, 1982 Switch Matrix Design, and the Task V, POC Model design, efforts of the program; however, they are reiterated as a summary of features that would require additional design consideration.

5.1 CROSSPOINT GAIN BANDWIDTH

Gain bandwidth of the individual switch crosspoints is a function of the GaAs FET. It would be most desirable to add to the GaAs FET specification a tighter tolerance limit of gain at a specific frequency. This would reduce the range of device parameters so that improved process controls could be achieved in the tuning and test of the individual switch crosspoints. Consideration should also be given to the integration of the logic bipolar switching device and the GaAs FET gate bias resistors to the microwave integrated circuit substrate. This would aid in tuning the amplifier, minimize the time required to set the gain of a crosspoint, and reduce stray capacitances within the switch driver circuit. Reduced capacitance would result in faster crosspoint switching speeds.

5.2 SWITCH DRIVER DESIGN

The GaAs FET gate bias turn-on time constant problem that was discussed in Section 4.2.4 would require additional design effort to increase switching speed, as currently defined. One method to consider would be to drive the FET gate from a higher voltage source which would permit operating the gate on the fast rising portion of the gate pulse. The voltage would be clamped at the appropriate gate bias level to avoid overdriving the FET. From the results obtained in the POC model, this new method should decrease the switching speed to less than 10 nanoseconds. Integrating the bipolar switch driver onto the MIC substrate as discussed in 5.1 would also help increase switching speed.

5.3 INTERCONNECT SYSTEM

Further tolerance studies of the materials used in the interconnect system must be completed to improve process control during fabrication and assembly of the channel modules. Tolerance variation between the MIC substrate to the connector pin was measured and found to be within the anticipated range of 10 mils. This required a service loop in the ribbon wire connecting the pin to the MIC pad, which resulted in detuning of the bandpass filter. Another approach to be evaluated would be to remove the interconnect system from the bandpass filter. This could be accomplished by designing the filter into the input circuit of the first switch/amplifier stage, and the output circuit of the second switch/amplifier stage. The interconnect system would not be a part of the filter frequency determining elements. This method would provide the required isolation between amplifier stages without being a part of the filter.

5.4 CUSTOM LOGIC LSI DESIGN

The logic design for the POC model was implemented using packaged integrated circuits and discrete bipolar devices. This approach worked well for the POC fabrication as it proved system feasibility at a reduced cost. A size penalty was exhibited by the number of integrated circuits contained in the two logic printed wiring boards that were required to address sixty-one active crosspoints. For a flight model switch matrix, it is highly recommended to implement the custom LSI logic design, as discussed in detail in the Task I 1982 Switch Matrix Design report. The approach taken for the LSI design would result in a smaller package size and would be readily expandable to matrices of sizes other than 20 x 20.

5.5 CABLING

The cabling method used in the POC model consisted of a multiwire harness which was functional for this build; however, the harness would become bulky for a fully populated 20 x 20 matrix. For flight model implementation, a flex wire system would be desirable. By implementing the custom logic LSI design as discussed in Section 5.4, this system would reduce the number of wires routed to the channel modules and would therefore result in a smaller flex wire system.

5.6 SWITCH MATRIX SIZE

The main mechanical supporting member of the Switch Matrix design is the base plate. The channel modules are directly attached to the base plate and are completely inclosed so that no further environmental or electrical protection is required. For the POC model design, a housing was used as a support for the base plate and the two control logic printed wiring board assemblies. For a flight model switch matrix, the control logic would be implemented with custom LSI devices which, in most cases, would be assembled into the logic side of the channel housings. The remaining addressing functions would be assembled into a smaller housing that would be mounted to the base plate as indicated in the Task I Switch Matrix design report. This would result in the elimination of the housing used in the POC model. The base plate would be mounted directly to the spacecraft structure, resulting in a smaller switch matrix package. This design approach could be utilized regardless of the switch matrix N x N size.

The width of a MIC substrate, within the channel assembly, is determined mainly by the $\frac{1}{4}\lambda$ coupler; however, the height of the assembly is determined by the number of parts and filter size of the GaAs FET circuit. As shown in the POC fabrication, excess space on the substrate was provided as a contingency. For a flight model, the length of the input and output substrates could be reduced which in turn would reduce the height of the channel modules.

5.7 CONCLUSION

During the course of the program, a switch matrix conceptual design was developed. From this design, a breadboard 5 x 5 switch matrix was fabricated and tested. Based on results of the breadboard effort, a design for the POC Model 20 x 20 switch matrix was completed. The design was fabricated using sixty-one active switch crosspoints including one wraparound path for redundancy. Testing of the POC model was the last program task. The intent of the POC Model fabrication and test was to prove feasibility of the conceptual design to solve the

problems of multibeam switching in an advance technology 30/20 GHz SS-TDMA communications system.

Key design goal requirements, such as bandwidth, insertion loss, high speed switching and isolation, were the major design considerations throughout the development program.

As predicted in the study phase of the program, the coupled crossbar architecture has been proven to meet the established requirements. Its immunity to single point failures makes it the most promising architecture for a system mission life of ten years. This immunity is enhanced by the use of 15 dB couplers on both input and output transmission lines. The 15 dB coupler insertion loss provides more than adequate isolation in the event of a failed switch crosspoint.

The dual gate GaAs FET is still considered to be the best device for the application of microwave signal switching. It provides low power, high speed switching with the only major parameter compromise being a tradeoff between gain and bandwidth. The packaged FET worked well in the design which eliminated hermetic sealing of the entire channel assembly.

The control logic with its 32 bit code addressing format exhibited no problems during the fabrication and test efforts. The design concept was proven to be feasible and would only have to be fabricated into a custom LSI package for flight model implementation. The switch driver design concept worked favorably but would require additional design effort to reduce the average switching speed from 25 nsecs to the desired 10 nsecs. This was considered to be a design problem and not a technology problem.

One of the key switch matrix requirements was expandability of the selected designs. Expandability of the design was proven by the fabrication of a 5 x 5 breadboard switch matrix assembly and the 20 x 20 POC model. The channel assemblies were designed so that only the length of the channel is changed dependent on the selected matrix size. Each of the input and output crosspoint microwave integrated circuits are assembled on individual kovar carriers. One set of carriers is added to the row and column channels for each desired crosspoint of a N x N matrix. The length of the channel assembly would therefore be determined by the number of required kovar carriers. The base plate design remains the same with the only change being the plate length, width, and number of interconnect holes to be drilled in the plate dependent upon matrix size. Since the custom logic LSI design would consist of two basic chips, the number of chips to be used would be dependent on the matrix N x N size. These concepts have resulted in a switch mattix design that is readily expandable.

Fabrication and test results of the breadboard and POC models have proven that the selected switch matrix design is feasible for implementation into a flight system. The program effort has shown that 1982 technology will provide a wide band, high speed IF Switch Matrix up to an N x N size of 20 x 20. Reliability predications of the design have indicated that the design would meet the requirements of a ten year mission.

SECTION 6.0

RELIABILITY

This analysis is an update of the preliminary reliability studies completed for the Task 1, Conceptual Switch Matrix Design. The basic change is the incorporation of the microwave switch crosspoint design utilized in the POC model. Since a discrete IC design was used in the POC model for the control and switch driver logic and a LSI custom design would be used for the flight model, the original logic circuit assumptions used for the preliminary analyses are valid for this update.

This document presents the theory, calculations, and results of the reliability analyses that have been completed relative to a flight model 20 x 20 IF Switch Matrix.

6.1 THEORY

If no redundancy is employed within the switch matrix, the probability that any one of n inputs can be connected to any one of n outputs at any time during a ten (10) year mission is calculated as follows:

$$P_s = R^N$$

where P_s = Probability of success

N = Number of Crosspoints (n^2)

R = $e^{-\lambda T}$ = Probability of Success of One Crosspoint

T = 87600 Hours (10 years)

λ = Failure Rate of a Crosspoint

This matrix, for n = 20 and with no redundancy included, will result in a low probability of mission success (0.30065 for ten years for an assumed crosspoint reliability of 0.997). To increase this probability of mission success, redundancy is incorporated using the "wraparound" technique as illustrated in Figure 6.1.1.

6.2 GUIDELINES AND ASSUMPTIONS

To assess the reliability of the IF switch matrix using the "wraparound" technique for redundancy, the following guidelines and/or assumptions were used:

1. For success any input can be connected to any output at any time.

2. Mission life is 10 years.

3. Two crosspoints in a wraparound can be activated to connect an input to an output if its crosspoint fails to close.

4. No single failure in a crosspoint results in either a short between an input and output line or a short to ground on an input or output line.

5. One wraparound (two crosspoints) can successfully connect an input to any output if one or all crosspoints fail to close on an input row or one or all crosspoints fail to close on an output column.

6. A switchable amplifier is required in each wraparound to compensate for loss of signal gain due to coupler loss in the second crosspoint of the wraparound.

7. Each input line and each output line requires a coax connector. Each coax connector is a potential single point failure for the overall switch matrix. The probability of success for the overall switch matrix is then calculated as the probability of success of 40 coax connectors times the probability of success of the switching matrix.

8. A wraparound to be successful must have its amplifier and two specific switches working. However when more than one wraparound is available, there is considerable redundancy in the switches of the wraparounds which permit an interchange of amplifiers. Therefore, the probability of success of a wraparound is the probability that the amplifier is working successfully. (Figure 6.2.1)

9. The probability of success of the switch matrix was calculated by using a truth table and is given by the general equation shown in Figure 6.2.2.

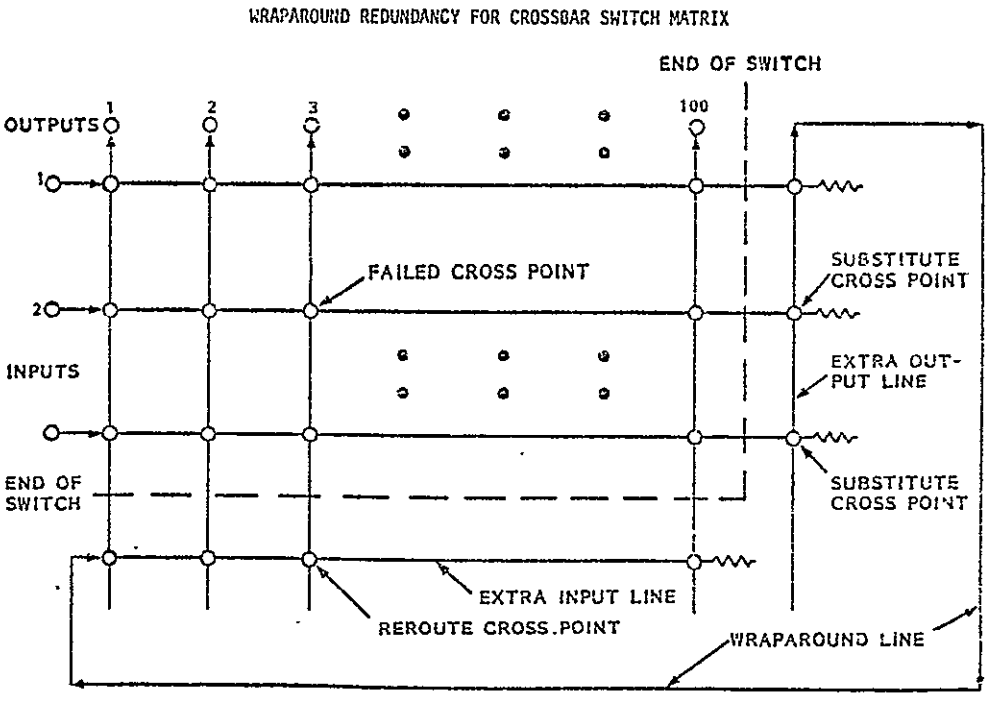


Figure 6.1.1.

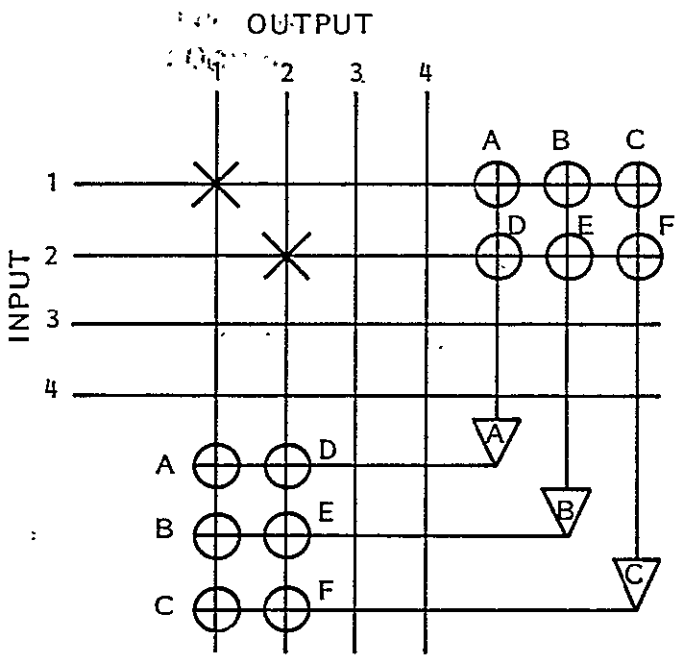


Figure 6.2.1

Failure of Switch 1-1 can be corrected by:

1. Switches A and Amplifier A

OR 2. Switches B and Amplifier B

OR 3. Switches C and Amplifier C

Failure of Switch 2-2 can be corrected by:

1. Switches D and Amplifier A

OR 2. Switches E and Amplifier B

OR 3. Switches F and Amplifier C

Therefore, for matrix success in the event of failure of switch 1-1 and switch 2-2, two of the three amplifiers must be working. In the wraparound switches associated with the amplifiers, many combinations of switch failures can occur before two wraparound paths fail. Therefore, the reliability of the switches in the wraparound is essentially 1.0, when more than one wraparound is available.

$$
\begin{aligned}
PS &= R^{N} \\
&+ N*R^{(N-1)} * Q * W_1 \\
&+ B_1 * R^{(N-2)} * Q^2 * W_1 \\
&+ (A_1 - B_1) * R^{(N-2)} * Q^2 * W_2 \\
&+ B_2 * R^{(N-3)} * Q^3 * W_1 \\
&+ D_1 * R^{(N-3)} * Q^3 * W_2 \\
&+ (A_2 - B_2 - D_1) * R^{(N-3)} * Q^3 * W_3 \\
&+ B_3 * R^{(N-4)} * Q^4 * W_1 \\
&+ D_2 * R^{(N-4)} * Q^4 * W_2 \\
&+ D_3 * R^{(N-4)} * Q^4 * W_2 \\
&+ D_4 * R^{(N-4)} * Q^4 * W_3 \\
&+ [A_3 - B_3 - D_2 - D_3 - D_4] * R^{(N-4)} * Q^4 * W_4 \\
&+ B_4 * R^{(N-5)} * Q^5 * W_1 \\
&+ D_5 * R^{(N-5)} * Q^5 * W_2 \\
&+ D_6 * R^{(N-5)} * Q^5 * W_2 \\
&+ D_7 * R^{(N-5)} * Q^5 * W_3 \\
&+ D_8 * R^{(N-5)} * Q^5 * W_3 \\
&+ D_9 * R^{(N-5)} * Q^5 * W_4 \\
&+ D_{10} * R^{(N-5)} * Q^5 * W_5 \\
&+ B_5 * R^{(N-6)} * Q^6 * W_1 \\
&+ D_{11} * R^{(N-6)} * Q^6 * W_2
\end{aligned}
$$

Figure 6.2.2. General Equation

where:

P_S = Probability of success of the Switch Matrix

R = Reliability of a crosspoint

N = Number of crosspoints

C = Number of crosspoints in a row or column of the matrix

Q = (I-R) Unreliability of a crosspoint

W_1 = Probability that one of X wraparounds is working

W_2 = Probability that two of X wraparounds are working

W_3 = Probability that three of X wraparounds are working

W_X = Probability that all of the wraparounds are working

X = Number of wraparounds

S = Probability of success of wraparound

T = (I-S) Unreliability of a wraparound

W_1 = Sum of the first X terms of the following equation

W_2 = Sum of the first (X-1) terms of the following equation

W_3 = Sum of the first (X-2) terms of the following equation

W_X = The first term of the following equation

$$S^X + X\,S^{X-1}T + (X * \frac{X-1}{2})\,S^{(X-2)}T^2 + (X * (\frac{X-1}{2}) * (\frac{X-2}{3}))\,S^{X-3}T^3 \ldots + T^X = 1$$

A_1 = $N * (\frac{N-1}{2})$

A_2 = $N * (\frac{N-1}{2}) * (\frac{N-2}{3})$

A_3 = $N * (\frac{N-1}{2}) * (\frac{N-2}{3}) * (\frac{N-3}{4})$

B_1 = $2 * C^2 * (\frac{C-1}{2})$

B_2 = $2 * C^2 * (\frac{C-1}{2}) * (\frac{C-2}{3})$

B_3 = $2 * C^2 * (\frac{C-1}{2}) * (\frac{C-2}{3}) * (\frac{C-3}{4})$

Figure 6.2.2. General Equation (Cont'd)

$$B_4 = 2 * C^2 * \left(\frac{C-1}{2}\right) * \left(\frac{C-2}{3}\right) * \left(\frac{C-3}{4}\right) * \left(\frac{C-4}{5}\right)$$

$$B_5 = 2 * C^2 * \left(\frac{C-1}{2}\right) * \left(\frac{C-2}{3}\right) * \left(\frac{C-3}{4}\right) * \left(\frac{C-4}{5}\right) * \left(\frac{C-5}{6}\right)$$

$$D_1 = 2 * C * (C-1)^2 * C * \left(\frac{C-1}{2}\right)$$

$$D_2 = 2 * C^2 * (C-1) * C \left(\frac{C-1}{2}\right) * \left(\frac{C-2}{3}\right)$$

$$D_3 = (C-1) * [(C-1) + (C-2)] * \left[C * \frac{(C-1)}{2}\right]^2$$

$$D_4 = C * (C-1)^2 * (C-2)^2 * C * \frac{(C-1)}{2}$$

$$D_5 = 2 * C^2 * (C-1) * C * \frac{(C-1)}{2} * \frac{(C-2)}{3} * \frac{(C-3)}{4}$$

$$D_6 = C^2 * \frac{(C-1)}{2}^2 * \frac{(C-2)}{3}^2 * \left[\frac{C-3}{2} + \frac{C}{2} + C * \frac{(C-1)}{(C-2)}\right]$$

$$D_7 = C^2 * \frac{(C-1)}{2}^2 * \frac{(C-2)}{3}^2 * [6 + 6\ (C-3) + (C-3) + (C-4)]$$

$$D_8 = C^2 * \frac{(C-1)}{2}^2 * \frac{(C-2)}{3}^2 * \left[\frac{15}{2} + 12\ (C-3) + \frac{3}{2}\ (C-3)^2 + \frac{3}{2}\ (C-3)(C-4)\right]$$

$$D_9 = C^2 * \frac{(C-1)}{2}^2 * \frac{(C-2)}{3}^2 * \frac{(C-3)}{4}^2 * [4 * (C-1)]$$

$$D_{10} = C^2 * \frac{(C-1)}{2}^2 * \frac{(C-2)}{3}^2 * \frac{(C-3)}{4}^2 * \frac{(C-4)}{5}^2$$

$$D_{11} = 2 * C^2 * (C-1) * C * \frac{(C-1)}{2} * \frac{(C-2)}{3} * \frac{(C-3)}{4} * \frac{(C-4)}{5}$$

Figure 6.2.2. General Equation (Cont'd)

6.3 RELIABILITY TRADE STUDIES

During the initial design stages, reliability trade studies were conducted. The results of these studies has shown that the optimum design for a 20 x 20 IF switch matrix based on weight, power consumption, and reliability is one that contains:

1. Wraparounds for redundancy.

2. Separate IC logic to control each GaAs FET switch in a crosspoint, to eliminate single point failures.

3. The optimum building block for the switching logic (to control the switch of each crosspoint) when considering the IC packaging complexity and output pins, is a 1 x 25 matrix. The use of 25 of these building blocks readily provides a 20 x 20 switch matrix with the capability of providing up to 5 wraparounds.

4. A 32 bit interface method of decoding the input logic to control the switches of a crosspoint.

6.4 CROSSPOINT RELIABILITY ASSESSMENT

6.4.1 GENERAL

Each crosspoint has two GaAs FET switches in series that are RF coupled to and isolated from the input and output lines. Each GaAs FET switch is controlled separately by IC logic so that the only single failure mode for a crosspoint is the failure of either GaAs FET switch to latch closed.

If either GaAs FET or its associated IC logic fails to close, two switches in a wraparound circuit can be closed to provide an alternate path for the signals, thereby eliminating this potential single point failure. If either GaAs FET switch or its associated logic fails so as to close the switch inadvertently the other series switch can be commanded open by its IC logic. The probability that both switches will fail closed at the same time is a double failure with an extremely low probability of occurrence.

6.4.2 IC LOGIC FAILURE RATE CALCULATIONS

The decoding of the switch control signals, drivers and latch circuits required to switch the GaAs FETs off and on are contained in IC devices. The failure rates for these IC devices was calculated in accordance with the equation,

$$\lambda_P = \pi_Q [C_1 \pi_T \pi_V + (C_2 + C_3) \pi_E] \pi_2 * 10^{-6}$$

failures per hour, of Section 2.0 of MIL-HDBK-217C, Notice 1, for ICs. To this failure rate is added the failure rate of .00008 x 10^{-6} per solder joint and .000006 x 10^{-6} for each hole on the printed wiring board times the number of pins of each IC. The calculated failure rate of each IC including its connection is as follows:

1) 32 Bit Interface (Row Decoder)

Number Gates = 300
Power Dissipated = 0.2W
Number Pins = 52
$T_J = 40 + 25 * .2 = 45$
$\pi_T = .49$
$C_1 = .01714$
$C_2 = .00091$
$C_3 = .035$
$\pi_Q = 0.5$
$\pi_E = 1$
$\pi_L = 1$
$\pi_V = .2872$

$$\lambda_P = .5[.01714 * .49 * .2872 + (.00091 + .035) * 1] * 1 * 10^{-6}$$

$$\lambda_P = .01916 * 10^{-6} + 52 * .000086 * 10^{-6}$$

$$= .02363 * 10^{-6}$$

Each Row Decoder = $1/3 * .02363 * 10^{-6} = .00788 * 10^{-6}$

2) 32 Bit Interface (Column Decoder and Drivers)

Number Gates = 550
Power Dissipated = 0.4W
Number Pins = 52
$T_J = 40 + 25 * .4 = 50$

$\pi_T = .707$
$C_1 = .02184$
$C_2 = .00105$
$C_3 = .035$
$\pi_Q = 0.5$
$\pi_E = 1$
$\pi_C = 1$
$\pi_V = .2938$

$$\lambda_P = .5\,[.02184 * .707 * .2938 + (.00105 + .035) * 1] * 1 * 10^{-6}$$

$$= .02029 * 10^{-6} + 52 * .000086 * 10^{-6}$$

$$= .02476 * 10^{-6}$$

Each Column Decoder = $1/6 * .02476 * 10^{-6} = .00413 * 10^{-6}$
A Crosspoint Driver = $1/50 * .02476 * 10^{-6} = .00050 * 10^{-6}$

3) Latch Circuit

Number Gates = 50
Power Dissipated = 0.3W
Number Pins = 18
$T_J = 40 + 30 * .3 = 49$

$\pi_T = 0.66$
$C_1 = .00877$
$C_2 = .00062$
$C_3 = .0071$
$\pi_Q = 0.5$
$\pi_E = 1$
$\pi_L = 1$
$\pi_V = .2924$

$$\lambda_P = .5\,[.00877 * .66 * .2924 + (.00062 + .0071) * 1] * 1 * 10^{-6}$$

$$= .00471 * 10^{-6} + 18 * .000086 * 10^{-6}$$

$$= .006258 * 10^{-6}$$

Each Latch = $1/5 * .006258 * 10^{-6} = .001252 * 10^{-6}$

On some of these IC's, the gates associated with a particular crosspoint are physically separated from the gates of other crosspoints. For these IC's the calculated failure rate is divided by the number of crosspoints the IC controls to apportion the failure rate to a crosspoint.

Examples;

1. Each latch IC contains the circuits for control of one switch in 5 crosspoints.

2. Each row and column decoder/driver IC contains circuits for control of one switch in 25 crosspoints.

6.4.3 RF SECTION OF A CROSSPOINT FAILURE RATE CALCULATIONS

The failure rate of the RF portion of a crosspoint was calculated using failure rate data from MIL-HDBK-217C, Notice 1, and other sources as shown below.

(1/2 of a crosspoint)

3 10pf chip capacitors	@ .0000085	.000025	MIL-HDBK-217C
1 5100 pf chip capacitor	@ .0000169	.000017	MIL-HDBK-217C
1 Etch resistor		.0001	MIL-HDBK-217C
16 Micro-strip conductors	@ .0001	.0016	MIL-HDBK-217C
8 Welded ribbons	@ .000218	.001744	MIL-HDBK-217C
1 Kovar carrier		.0001	Engr. Estimate
4 Alum. substrates	@ .0001	.0004	Engr. Estimate
1 GaAs FET		.010	(See below)
		$.013986*10^{-6}$	

The failure rate of .010 x 10^{-6} for a GaAs is a conservative estimate based on:

1. GE test data from accelerated life test on other programs MTBF = 1 x 10^{8} hours.

2. Information from RADC that they have data for TI power GaAs FET of .0003 x 10^{-6}.

3. Failure rate for a GaAs FET calculated in accordance with MIL-HDBK-217C Notice 1 of 0.140 x 10^{-6} for 20% stress and junction temperature of 50°C. This base failure rate is the same as that for Silicon FETs and is based on limited data.

4. GaAs FET failure rate data presented in GE proposal of .0003 x 10^{-6}.

5. Aerospace (SAMSO) has concurred that a failure rate of .010 x 10^{-6} for a low noise GaAs FET is acceptable for use on the DSCS Program.

6.4.4 RF PORTION OF A WRAPAROUND AMPLIFIER FAILURE RATE CALCULATION

The failure rate for the RF portion of the wraparound amplifier was calculated using failure rate data from MIL-HDBK-217C, Notice 1 and other sources as shown below.

1/2 of Wraparound Amplifier

8 10 pf chip capacitors	@ .0000085	.000068	MIL-HDBK-217C
4 2 pf chip capacitors	@ .0000071	.000014	MIL-HDBK-217C
2 Etched resistor	@ .0001	.0002	MIL-HDBK-217C
26 Microstrip conductor	@ .0001	.0026	MIL-HDBK-217C
14 Welded ribbons	@ .000218	.00305	MIL-HDBK-217C
8 Wire bonds	@ .000218	.00174	MIL-HDBK-217C
1 Kovar carrier		.0001	Engr. Estimate
2 Substrates Alum.	@ .0001	.0002	Engr. Estimate
2 GaAs FET	@ .010	.020	(Same as crosspoint)
		.026406*10^{-6}	

6.4.5 CONNECTOR FAILURE CALCULATIONS

The failure rate for the input and output RF COAX connectors was calculated in accordance with Section 2.0 of MIL-HDBK-217C, Notice 1, as follows:

$$\lambda_P = \lambda_b (\pi_E * \pi_P * \pi_K)$$

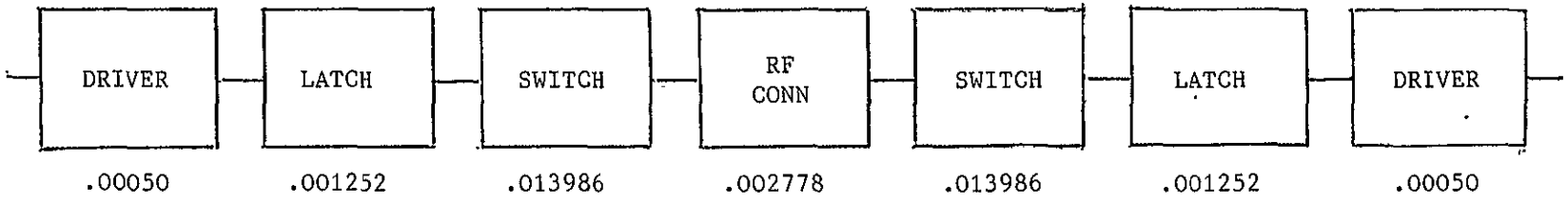
$$= .0041 * (1 * 1.36 * 1)$$

$$= .005576 * 10^{-6}$$

The RF connection between the two GaAs FET Switches in a crosspoint is estimated to be one half the failure rate of a coax connection i.e., .002788 x 10^{-6}.

6.5 RELIABILITY PREDICTION OF AN IF SWITCH MATRIX

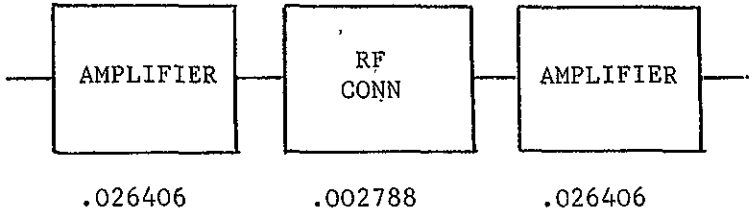
Figures 6.5.1 thru 6.5.3 depict the Reliability Success Diagrams for a 20 x 20 IF Switch Matrix containing wraparounds. The calculations for the probability that the switch crosspoints will operate successfully over ten years with zero thru five wraparounds are shown in Figures 6.5.4 thru 6.5.9. The probability that the 20 x 20 Switch Matrix will operate successfully over a mission life of ten years is shown in Table 6.5.1.



$$= .034264 * 10^{-6}$$

$$P_S = .99700$$

Figure 6.5.1. Reliability Success Diagram
Individual Crosspoint



$$= .0556 * 10^{-6}$$

$$P_S = .99514$$

Figure 6.5.2. Reliability Success Diagram
Wraparound Amplifier

Figure 6.5.3. Reliability Success Diagram
IF Switch Matrix

CALCULATION OF PROBABILITY OF SUCCESS
WITH M OF N UNITS REQUIRED FOR SUCCESS

ENTER TOTAL NUMBER OF CROSSPOINTS
=400
RELIABILITY OF EACH CROSSPOINT
=.99700
NO OF WRAPS
=0
RELIABILITY OF EACH WRAPAROUND
=.99514

RELIABILITY OF SW MATRIX WITH--

FAILURE PATTERN	NO OF WAYS FAILURE PATTERN CAN OCCUR	WRAPAROUND NR/NA	WRAPAROUND RELIABILITY	RELIABILITY OF SW MATRIX
0	--	0/0		0.300651E 00
1	0.40000000000E 03	1/0	0.	0.
		SUBTOTAL		0.300651E 00
2	0.76000000000E 04	1/0	0.	0.
1-1	0.72200000000E 05	2/0	0.	0.
		SUBTOTAL		0.300651E 00
3	0.45600000000E 05	1/0	0.	0.
1-2	0.27436000000E 07	2/0	0.	0.
1-1-1	0.77976000000E 07	3/0	0.	0.
		SUBTOTAL		0.300651E 00
4	0.19380000000E 06	1/0	0.	0.
1-3	0.17328000000E 08	2/0	0.	0.
2-2	0.25378300000E 08	2/0	0.	0.
1-1-2	0.44446320000E 09	3/0	0.	0.
1-1-1-1	0.56337660000E 09	4/0	0.	0.
		SUBTOTAL		0.300651E 00
5	0.62016000000E 06	1/0	0.	0.
1-4	0.73644000000E 08	2/0	0.	0.
2-3	0.30887160000E 09	2/0	0.	0.
1-1-3	0.29630880000E 10	3/0	0.	0.
2-2-1	0.82108728000E 10	3/0	0.	0.
1-1-1-2	0.42816621600E 11	4/0	0.	0.
1-1-1-1-1	0.28844881920E 11	5/0	0.	0.
		SUBTOTAL		0.300651E 00
6	0.15504000000E 07	1/0	0.	0.
1-5	0.23566080000E 09	2/0	0.	0.
		TOTAL		0.300651E 00

Figure 6.5.4. Reliability of 20 x 20 Switch Matrix With Zero Wraparounds

```
ENTER TOTAL NUMBER OF CROSSPOINTS
=400
RELIABILITY OF EACH CROSSPOINT
=.99700
NO OF WRAPS
=1
RELIABILITY OF EACH WRAPAROUND
=.99514
```

RELIABILITY OF SW MATRIX WITH--

FAILURE PATTERN	NO OF WAYS FAILURE PATTERN CAN OCCUR	WRAPAROUND NR/NA	RELIABILITY	RELIABILITY OF SW MATRIX
0	--	0/1		0.300651E 00
1	0.40000000000E 03	1/1	0.995140E 00	0.360109E 00
		SUBTOTAL	0.660760E 00	
2	0.76000000000E 04	1/1	0.995140E 00	0.205880E-01
1-1	0.72200000000E 05	2/1	0.	0.
		SUBTOTAL	0.681348E 00	
3	0.45600000000E 05	1/1	0.995140E 00	0.371698E-03
1-2	0.27436000000E 07	2/1	0.	0.
1-1-1	0.77976000000E 07	3/1	0.	0.
		SUBTOTAL	0.681720E 00	
4	0.19380000000E 06	1/1	0.995140E 00	0.475341E-05
1-3	0.17328000000E 08	2/1	0.	0.
2-2	0.25378300000E 08	2/1	0.	0.
1-1-2	0.44446320000E 09	3/1	0.	0.
1-1-1-1	0.56337660000E 09	4/1	0.	0.
		SUBTOTAL	0.681725E 00	
5	0.62016000000E 06	1/1	0.995140E 00	0.457701E-07
1-4	0.73544000000E 08	2/1	0.	0.
2-3	0.30887160000E 09	2/1	0.	0.
1-1-3	0.29630880000E 10	3/1	0.	0.
2-2-1	0.82108728000E 10	3/1	0.	0.
1-1-1-2	0.42816621600E 11	4/1	0.	0.
1-1-1-1-1	0.28844881920E 11	5/1	0.	0.
		SUBTOTAL	0.681725E 00	
6	0.15504000000E 07	1/1	0.995140E 00	0.344309E-09
1-5	0.23566080000E 09	2/1	0.	0.
		TOTAL	0.681725E 00	

Figure 6.5.5. Reliability of 20 x 20 Switch Matrix With One Wraparound

ENTER TOTAL NUMBER OF CROSSPOINTS
=400
RELIABILITY OF EACH CROSSPOINT
=.99700
NO OF WRAPS
=2
RELIABILITY OF EACH WRAPAROUND
=.99514

RELIABILITY OF SW MATRIX WITH-;

FAILURE PATTERN	NO OF WAYS FAILURE PATTERN CAN OCCUR	WRAPAROUND NR/NA	WRAPAROUND RELIABILITY	RELIABILITY OF SW MATRIX
0	--	0/2		0.300651E 00
1	0.40000000000E 03	1/2	0.999976E 00	0.361859E 00
		SUBTOTAL	0.662510E 00	
2	0.76000000000E 04	1/2	0.999976E 00	0.206880E-01
1-1	0.72200000000E 05	2/2	0.990304E 00	0.194635E 00
		SUBTOTAL	0.877833E 00	
3	0.45600000000E 05	1/2	0.999976E 00	0.373505E-03
1-2	0.27436000000E 07	2/2	0.990304E 00	0.222552E-01
1-1-1	0.77976000000E 07	3/2	0.	0.
		SUBTOTAL	0.900462E 00	
4	0.19380000000E 06	1/2	0.999976E 00	0.477552E-05
1-3	0.17328000000E 08	2/2	0.990304E 00	0.422946E-03
2-2	0.25378300000E 08	2/2	0.990304E 00	0.619439E-03
1-1-2	0.44446320000E 09	3/2	0.	0.
1-1-1-1	0.56337650000E 09	4/2	0.	0.
		SUBTOTAL	0.901509E 00	
5	0.62016000000E 06	1/2	0.999976E 00	0.459925E-07
1-4	0.73644000000E 08	2/2	0.990304E 00	0.540878E-05
2-3	0.30887160000E 09	2/2	0.990304E 00	0.226851E-04
1-1-3	0.29630880000E 10	3/2	0.	0.
2-2-1	0.82108728000E 10	3/2	0.	0.
1-1-1-2	0.42816621600E 11	4/2	0.	0.
1-1-1-1-1	0.28844881920E 11	5/2	0.	0.
		SUBTOTAL	0.901537E 00	
6	0.15504000000E 07	1/2	0.999976E 00	0.345362E-09
1-5	0.23566080000E 09	2/2	0.990304E 00	0.520806E-07
		TOTAL	0.901537E 00	

Figure 6.5.6. Reliability of 20 x 20 Switch Matrix With Two Wraparounds

```
ENTER TOTAL NUMBER OF CROSSPOINTS
=400
RELIABILITY OF EACH CROSSPOINT
=.99700
NO OF WRAPS
=3
RELIABILITY OF EACH WRAPAROUND
=.99514
```

RELIABILITY OF SW MATRIX WITH--

FAILURE PATTERN	NO OF WAYS FAILURE PATTERN CAN OCCUR	WRAPAROUND NR/NA	RELIABILITY	RELIABILITY OF SW MATRIX
0	--	0/3		0.300651E 00
1	0.40000000000E 03	1/3	0.100000E 01	0.361867E 00
		SUBTOTAL	0.5625196 00	
2	0.76000000000E 04	1/3	0.100000E 01	0.206885E-01
1-1	0.72200000000E 05	2/3	0.999929E 00	0.196527E 00
		SUBTOTAL	0.8797346 00	
3	0.45600000000E 05	1/3	0.100000E 01	0.373514E-03
1-2	0.27436000000E 07	2/3	0.999929E 00	0.224715E-01
1-1-1	0.77976000000E 07	3/3	0.985491E 00	0.629441E-01
		SUBTOTAL	0.9655236 00	
4	0.19380000000E 06	1/3	0.100000E 01	0.477663E-05
1-3	0.17328000000E 08	2/3	0.999929E 00	0.427057E-03
2-2	0.25378000000E 08	2/3	0.999929E 00	0.625460E-03
1-1-2	0.44446320000E 09	3/3	0.985491E 00	0.107958E-01
1-1-1-1	0.56397660000E 09	4/3	0.	0.
		SUBTOTAL	0.9773766 00	
5	0.62016000000E 06	1/3	0.100000E 01	0.459936E-07
1-4	0.73644000000E 08	2/3	0.999929E 00	0.546136E-05
2-3	0.30887160000E 09	2/3	0.999929E 00	0.229056E-04
1-1-3	0.29630880000E 10	3/3	0.985491E 00	0.216566E-03
2-2-1	0.82108728000E 10	3/3	0.985491E 00	0.600117E-03
1-1-1-2	0.42816621600E 11	4/3	0.	0.
1-1-1-1-1	0.28844681920E 11	5/3	0.	0.
		SUBTOTAL	0.9782226 00	
6	0.15504000000E 07	1/3	0.100000E 01	0.345990E-09
1-5	0.23566080000E 09	2/3	0.999929E 00	0.525868E-07
		TOTAL	0.9782226 00	

Figure 6.5.7. Reliability of 20 x 20 Switch Matrix With Three Wraparounds

```
ENTER TOTAL NUMBER OF CROSSPOINTS
=400
RELIABILITY OF EACH CROSSPOINT
=.99700
NO OF WRAPS
=4
RELIABILITY OF EACH WRAPAROUND
=.99514
```

RELIABILITY OF SW MATRIX WITH--

FAILURE PATTERN	NO OF WAYS FAILURE PATTERN CAN OCCUR	WRAPAROUND NR/NA	RELIABILITY	RELIABILITY OF SW MATRIX
0	--	0/4		0.300651E 00
1	0.40000000000E 03	1/4	0.100000E 01	0.361867E 00
		SUBTOTAL	0.662519E 00	
2	0.78000000000E 04	1/4	0.100000E 01	0.206885E-01
1-1	0.72200000000E 05	2/4	0.100000E 01	0.196541E 00
		SUBTOTAL	0.879748E 00	
3	0.45600000000E 05	1/4	0.100000E 01	0.373514E-03
1-2	0.27436000000E 07	2/4	0.100000E 01	0.224731E-01
1-1-1	0.77976000000E 07	3/4	0.999859E 00	0.638618E-01
		SUBTOTAL	0.966456E 00	
4	0.19380000000E 06	1/4	0.100000E 01	0.477663E-05
1-3	0.17328000000E 08	2/4	0.100000E 01	0.427087E-03
2-2	0.25378300000E 08	2/4	0.100000E 01	0.625504E-03
1-1-2	0.44446320000E 09	3/4	0.999859E 00	0.109532E-01
1-1-1-1	0.56337660000E 09	4/4	0.980701E 00	0.136177E-01
		SUBTOTAL	0.992085E 00	
5	0.62016000000E 06	1/4	0.100000E 01	0.459936E-07
1-4	0.73644000000E 08	2/4	0.100000E 01	0.546174E-05
2-3	0.30887160000E 09	2/4	0.100000E 01	0.229072E-04
1-1-3	0.29630880000E 10	3/4	0.999859E 00	0.219724E-03
2-2-1	0.82108728000E 10	3/4	0.999859E 00	0.608866E-03
1-1-1-2	0.42816821600E 11	4/4	0.980701E 00	0.311417E-02
1-1-1-1-1	0.28844881920E 11	5/4	0.	0.
		SUBTOTAL	0.996056E 00	
6	0.15504000000E 07	1/4	0.100000E 01	0.345390E-09
1-5	0.23566080000E 09	2/4	0.100000E 01	0.525905E-07
		TOTAL	0.996056E 00	

Figure 6.5.8. Reliability of 20 x 20 Switch Matrix With Four Wraparounds

```
ENTER TOTAL NUMBER OF CROSSPOINTS
=400
RELIABILITY OF EACH CROSSPOINT
=.99700
NO OF WRAPS
=5
RELIABILITY OF EACH WRAPAROUND
=.99514
```

RELIABILITY OF SW MATRIX WITH--

FAILURE PATTERN	NO OF WAYS FAILURE PATTERN CAN OCCUR	WRAPAROUND NR/NA	WRAPAROUND RELIABILITY	RELIABILITY OF SW MATRIX
0	--	0/5		0.300651E 00
1	0.40000000000E 03	1/5	0.100000E 01	0.361867E 00
		SUBTOTAL	0.662519E 00	
2	0.76000000000E 04	1/5	0.100000E 01	0.206885E-01
1-1	0.72200000000E 05	2/5	0.100000E 01	0.196541E 00
		SUBTOTAL	0.879748E 00	
3	0.45600000000E 05	1/5	0.100000E 01	0.373514E-03
1-2	0.27436000000E 07	2/5	0.100000E 01	0.224731E-01
1-1-1	0.77976000000E 07	3/5	0.999999E 00	0.688708E-01
		SUBTOTAL	0.966465E 00	
4	0.19380000000E 06	1/5	0.100000E 01	0.477663E-05
1-3	0.17328000000E 08	2/5	0.100000E 01	0.427087E-03
2-2	0.25378300000E 08	2/5	0.100000E 01	0.625504E-03
1-1-2	0.44446320000E 09	3/5	0.999999E 00	0.109548E-01
1-1-1-1	0.56337660000E 09	4/5	0.999766E 00	0.138824E-01
		SUBTOTAL	0.992360E 00	
5	0.62016000000E 06	1/5	0.100000E 01	0.459936E-07
1-4	0.73644000000E 08	2/5	0.100000E 01	0.546174E-05
2-3	0.30887160000E 09	2/5	0.100000E 01	0.229072E-04
1-1-3	0.29630880000E 10	3/5	0.999999E 00	0.219755E-03
2-2-1	0.82108728000E 10	3/5	0.999999E 00	0.608951E-03
1-1-1-2	0.42816621600E 11	4/5	0.999766E 00	0.317471E-02
1-1-1-1-1	0.28844881920E 11	5/5	0.975935E 00	0.208777E-02
		SUBTOTAL	0.998480E 00	
6	0.15504000000E 07	1/5	0.100000E 01	0.345990E-09
1-5	0.23566080000E 09	2/5	0.100000E 01	0.525905E-07
		TOTAL	0.998480E 00	

Figure 6.5.9. Reliability of 20 x 20 Switch Matrix With Five Wraparounds

Table 6.5.1. 20 x 20 Switch Matrix Probability of Success

$$P_m = P_C * P_D * P_{SW}$$

No. of Wraparounds	P_C	P_D	P_{SW}	P_M
0	0.98065	0.99999	0.30065	0.29483
1			0.68172	0.66853
2			0.90154	0.88408
3			0.97822	0.95929
4			0.99606	0.97678
5			0.99848	0.97916

P_C = Coax Connectors
P_D = Row & Column Decoders
P_{SW} = Switch Crosspoints
P_M = Switch Matrix

6.6 CONCLUSIONS

The General Electric flight model design for a 20 x 20 IF switch matrix that employs wraparounds for redundancy and controlled by a 32 bit interface logic is a reliable design. The actual reliability is dependent on the number of wraparounds. The overall probability of success for the IF Switch Matrix is limited by the forty non-redundant coax input and output connectors. The number of wraparounds to be used for an IF Switch Matrix will be dependent on the reliability goals or allocations assigned by further system requirements.

APPENDIX A

POC MODEL

TEST DATA

GPM4 614001 T[illegible]78 0 13 SEP 82 14:10:33

SWITCH MATRIX POC MODEL TESTING
REFERENCE LWD NOTEBOOK 386-2 P42
6,1 DN NA[illegible]201::41

FREQ-MHZ	VSWR FORWARD	LOSS-DB FORWARD	PTH LOSS FORWARD	VSWR REVERSE	LOSS-DB REVERSE	PTH LOSS REVERSE
5000.000	1.25	21.98	19.21	1.43	86.11	37.04
5060.000	1.23	21.11	19.90	1.37	79.10	29.01
5120.000	1.16	20.71	22.43	1.13	81.68	24.15
5180.000	1.13	20.67	24.57	1.14	85.34	23.57
5240.000	1.12	20.81	24.95	1.08	81.53	27.90
5300.000	1.12	21.03	24.66	1.05	77.56	31.60
5360.000	1.12	21.51	25.00	1.09	74.15	27.47
5420.000	1.09	22.02	26.88	1.08	90.36	28.28
5480.000	1.09	22.39	27.42	1.05	80.46	32.30
5540.000	1.10	22.59	26.77	1.05	71.12	31.85
5600.000	1.12	22.83	25.10	1.03	78.44	36.74
5660.000	1.11	22.98	25.97	1.08	91.50	28.02
5720.000	1.08	22.72	27.86	1.19	85.31	21.04
5780.000	1.07	22.00	28.86	1.23	77.50	19.67
5840.000	1.08	21.13	28.33	1.14	84.01	23.49
5900.000	1.09	20.45	27.68	1.06	79.15	30.73
5960.000	1.07	19.79	29.53	1.12	75.10	24.87
6020.000	1.09	18.70	27.78	1.07	70.75	29.36
6080.000	1.11	17.75	25.85	1.15	78.54	23.02
6140.000	1.10	17.19	26.41	1.22	78.19	20.13
6200.000	1.14	16.66	23.71	1.10	80.21	26.06
6260.000	1.16	15.97	22.56	1.06	78.13	31.24
6320.000	1.16	15.50	22.43	1.11	71.41	25.99
6380.000	1.17	15.44	22.23	1.07	77.94	29.20
6440.000	1.18	15.66	21.71	1.09	77.09	26.88
6500.000	1.20	16.28	20.73	1.10	71.46	26.12
6560.000	1.20	16.44	20.96	1.13	80.12	24.08
6620.000	1.15	16.10	23.35	1.21	86.43	20.63
6680.000	1.15	17.93	23.00	1.15	76.30	23.10
6740.000	1.11	17.85	25.40	1.13	79.90	24.02
6800.000	1.09	17.60	27.17	1.24	73.53	19.44
6860.000	1.07	17.12	29.97	1.30	76.22	17.71
6920.000	1.03	17.66	38.04	1.25	79.14	19.08
6980.000	1.09	17.79	27.72	1.24	78.80	19.48
7040.000	1.14	17.62	23.45	1.23	87.86	19.87
7100.000	1.17	17.37	22.31	1.12	76.74	24.69
7160.000	1.20	17.57	20.83	1.27	67.22	18.41
7220.000	1.26	18.44	18.65	1.38	72.15	15.94
7280.000	1.34	18.88	16.80	1.30	74.00	17.79
7340.000	1.34	19.44	16.80	1.38	74.14	15.96
7400.000	1.34	20.66	16.70	1.37	74.21	16.07
7460.000	1.39	22.33	15.83	1.15	72.84	23.00
7520.000	1.42	23.46	15.19	1.36	77.65	16.43
7580.000	1.40	24.04	15.57	1.27	68.65	18.63
7640.000	1.35	26.34	16.46	1.47	76.61	14.43
7700.000	1.34	30.60	16.83	2.23	71.64	8.39
7760.000	1.33	32.39	16.95	2.66	73.41	6.87
7820.000	1.35	30.82	16.59	2.42	70.68	7.63
7880.000	1.31	28.94	17.38	1.74	77.69	11.34
7940.000	1.27	28.68	18.62	1.22	74.81	20.04
8000.000	1.26	29.60	18.88	1.07	71.93	29.32

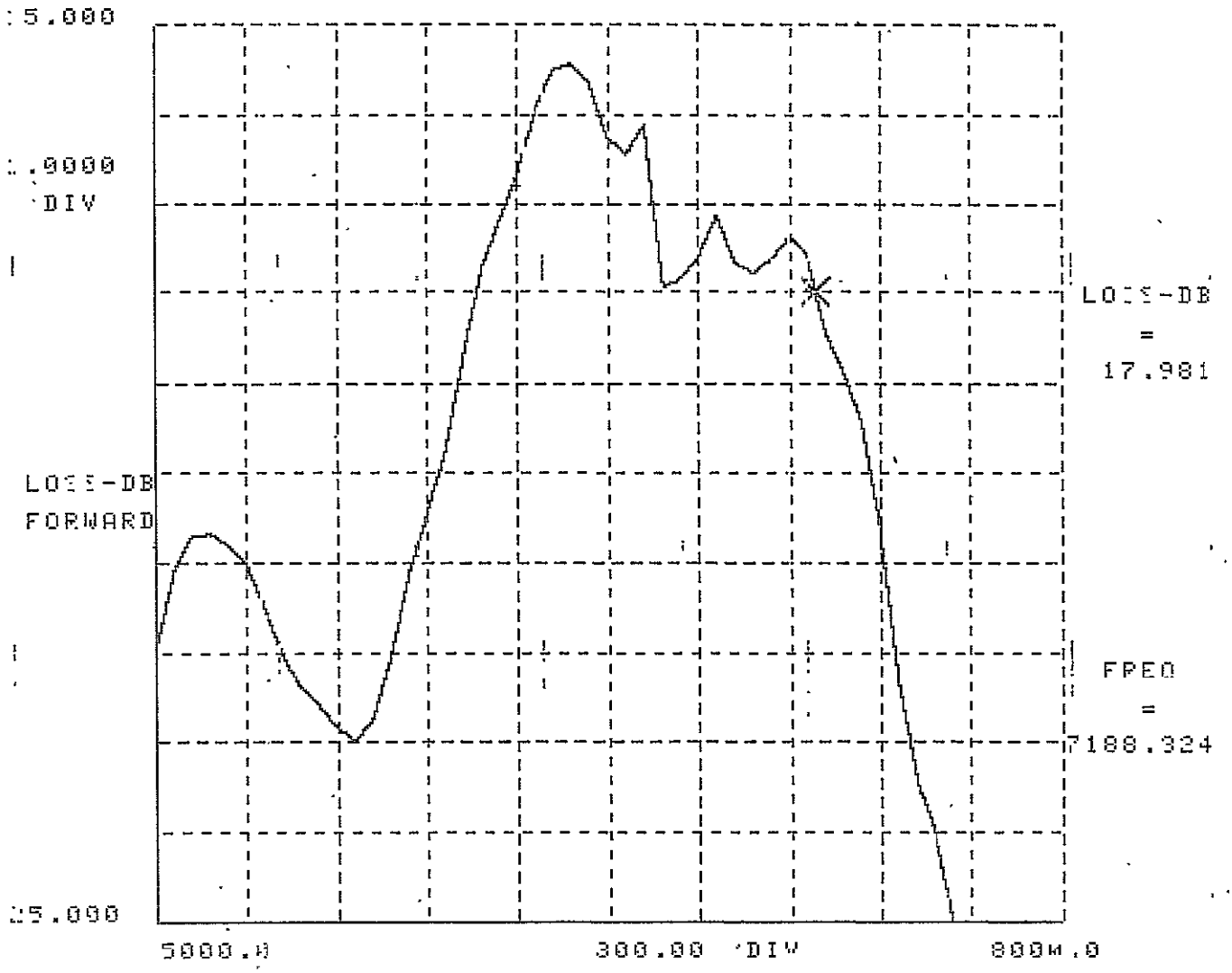
REF PLANE EXT.(M): INPUT= .00 TRAN= .00 OUTPUT= .00
NPAIL(1)= 4

APM4 614001 7.:8/78 0 :3 SEP 82 14:17:59

SWITCH MATRIX POC MODEL TESTING

REFERENCE LAB NOTEBOOK 38A-2 P42

6,1 DN HA:201::41a

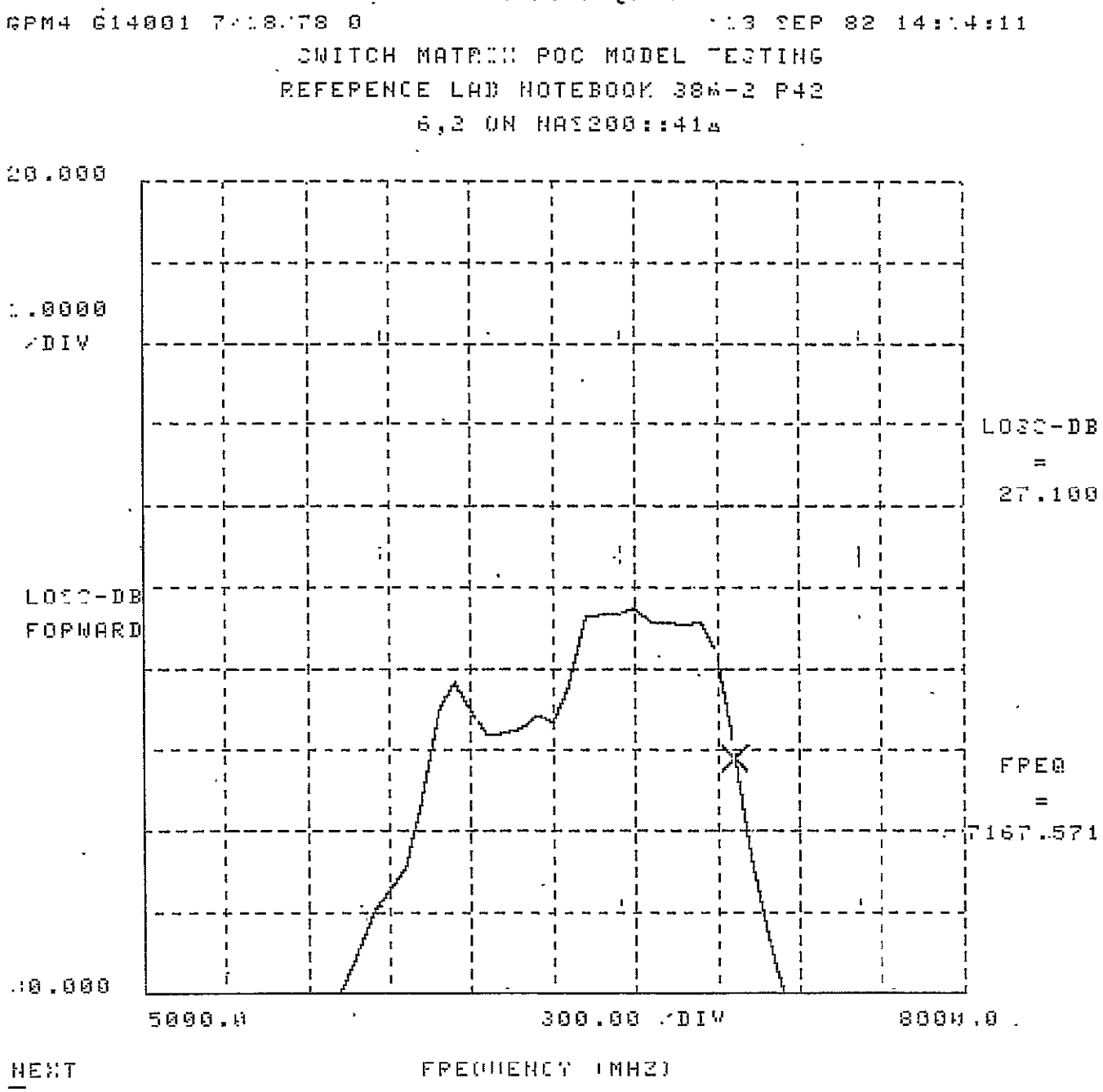


HPM4 G14001 7 18-78 0 13 SEP 82 14:15:00
SWITCH MATRIX POC MODEL TESTING
REFERENCE LAB NOTEBOOK 38K-2 P42
6,2 ON HA8200::41

FREQ-MHZ	VSWR FORWARD	LOSS-DB RTN LOSS FORWARD	VSWR REVERSE	LOSS-DB RTN LOSS REVERSE
5000.000	1.26	30.51	18.92	1.04	77.39	33.82
5060.000	1.24	30.36	19.46	1.02	84.34	38.40
5120.000	1.18	30.55	21.81	1.04	81.78	33.59
5180.000	1.14	30.84	23.61	1.09	82.09	27.11
5240.000	1.14	30.62	23.72	1.15	87.10	23.36
5300.000	1.14	30.72	23.60	1.13	74.30	24.58
5360.000	1.13	30.94	24.04	1.06	75.25	30.27
5420.000	1.11	31.12	25.65	1.08	94.04	28.83
5480.000	1.09	31.62	27.08	1.14	74.76	23.53
5540.000	1.09	31.60	27.41	1.12	71.49	24.62
5600.000	1.10	31.03	26.27	1.04	76.66	33.16
5660.000	1.09	30.50	27.70	1.06	79.69	30.91
5720.000	1.07	30.04	29.92	1.07	81.56	29.51
5780.000	1.04	29.53	33.56	1.02	74.66	38.25
5840.000	1.05	29.01	32.09	1.06	79.70	30.10
5900.000	1.06	28.72	30.31	1.24	82.07	19.37
5960.000	1.06	28.45	30.59	1.43	75.56	15.02
6020.000	1.10	27.59	26.67	1.41	71.97	15.40
6080.000	1.13	26.53	24.17	1.19	76.02	21.07
6140.000	1.13	26.17	24.01	1.17	82.42	22.29
6200.000	1.18	26.52	21.46	1.21	83.71	20.46
6260.000	1.21	26.82	20.39	1.08	74.14	27.84
6320.000	1.21	26.80	20.27	1.11	78.00	25.72
6380.000	1.22	26.74	20.25	1.16	85.92	22.79
6440.000	1.21	26.57	20.26	1.17	74.08	22.27
6500.000	1.23	26.66	19.89	1.19	69.93	21.14
6560.000	1.21	26.17	20.54	1.20	77.27	20.71
6620.000	1.16	25.37	22.80	1.11	93.67	25.43
6680.000	1.14	25.34	23.71	1.09	77.01	27.10
6740.000	1.09	25.32	27.42	1.06	80.66	30.22
6800.000	1.05	25.26	32.01	1.06	75.42	30.51
6860.000	1.02	25.44	40.70	1.08	73.99	27.83
6920.000	1.03	25.43	36.79	1.15	92.94	23.22
6980.000	1.12	25.47	24.87	1.21	77.30	20.56
7040.000	1.18	25.43	21.64	1.17	74.21	22.17
7100.000	1.21	25.81	20.48	1.04	76.10	33.63
7160.000	1.25	26.93	19.18	1.13	68.57	24.52
7220.000	1.31	28.27	17.43	1.15	76.72	23.29
7280.000	1.39	29.22	15.84	1.14	78.58	23.92
7340.000	1.39	30.14	15.83	1.25	82.38	18.94
7400.000	1.38	31.49	15.85	1.28	84.62	21.79
7460.000	1.42	33.18	15.22	1.20	78.55	20.69
7520.000	1.46	33.94	14.63	1.54	81.53	13.42
7580.000	1.43	33.53	15.05	1.47	68.79	14.36
7640.000	1.38	34.18	15.91	1.35	80.62	16.64
7700.000	1.36	36.97	16.39	2.05	76.73	9.25
7760.000	1.35	39.41	16.45	2.64	69.61	6.92
7820.000	1.37	38.91	16.14	2.46	68.83	7.49
7880.000	1.34	36.47	16.78	1.78	73.65	11.04
7940.000	1.30	35.14	17.79	1.27	70.72	18.50
8000.000	1.29	34.71	18.07	1.18	69.32	27.97

REF PLANE ENT: MI: INPUT= .00 TRAN= .00 OUTPUT= .00
NPAIL: 1:= 4

ORIGINAL PAGE IS
OF POOR QUALITY

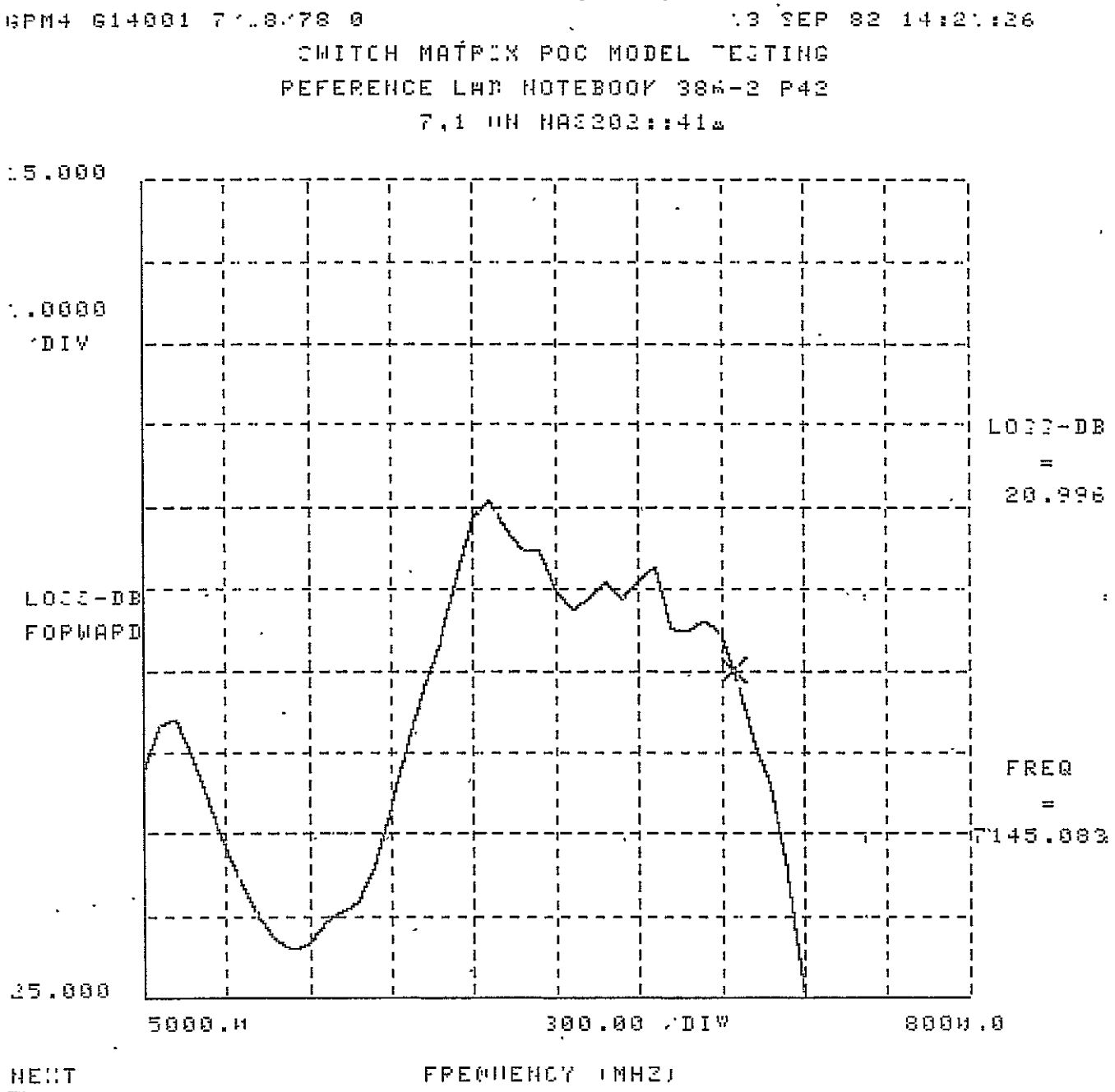


GPM4 G14001 7/18/78 0 13 SEP 82 14:22:01

SWITCH MATRIX POC MODEL TESTING
REFERENCE LAB NOTEBOOK 386-2 P42
7,1 ON NAC202::41

FREQ-MHZ	VSWR FORWARD	LOSS-DB FORWARD	RTN LOSS FORWARD	VSWR REVERSE	LOSS-DB REVERSE	RTN LOSS REVERSE
5000.000	1.20	22.24	21.00	1.03	83.29	36.83
5060.000	1.18	21.67	21.63	1.07	78.86	28.95
5120.000	1.13	21.60	24.53	1.03	94.79	24.12
5180.000	1.10	22.05	26.27	1.04	81.51	23.52
5240.000	1.08	22.63	28.10	1.09	88.41	27.77
5300.000	1.09	23.16	27.67	1.05	72.96	31.75
5360.000	1.08	23.63	27.99	1.09	75.16	27.72
5420.000	1.07	24.02	29.25	1.08	79.43	28.71
5480.000	1.05	24.29	32.75	1.05	77.04	33.03
5540.000	1.04	24.39	33.33	1.05	74.42	32.28
5600.000	1.07	24.33	29.69	1.03	75.26	37.84
5660.000	1.06	24.08	30.37	1.08	78.00	38.22
5720.000	1.06	23.94	30.73	1.09	77.58	21.10
5780.000	1.04	23.83	34.11	1.23	75.34	19.64
5840.000	1.04	23.38	33.82	1.05	74.32	23.38
5900.000	1.06	22.65	30.78	1.05	75.28	31.67
5960.000	1.04	21.90	33.29	1.01	74.89	25.31
6020.000	1.04	21.20	34.77	1.07	71.68	29.59
6080.000	1.05	20.65	33.02	1.06	82.14	22.84
6140.000	1.03	19.87	35.75	1.22	86.14	19.97
6200.000	1.06	19.11	30.38	1.11	85.28	25.56
6260.000	1.08	18.91	28.11	1.06	73.02	31.19
6320.000	1.08	19.27	28.17	1.10	74.88	26.84
6380.000	1.08	19.52	27.98	1.06	97.66	31.04
6440.000	1.09	19.53	27.03	1.10	77.26	26.78
6500.000	1.11	20.01	25.97	1.12	74.09	24.80
6560.000	1.10	20.26	26.27	1.15	79.70	23.18
6620.000	1.04	20.11	33.25	1.21	91.15	20.55
6680.000	1.07	19.91	29.54	1.13	75.55	24.63
6740.000	1.07	20.13	29.11	1.12	76.93	25.22
6800.000	1.10	19.89	26.10	1.24	76.36	19.29
6860.000	1.14	19.73	23.93	1.32	76.26	17.26
6920.000	1.16	20.50	22.36	1.27	74.29	18.42
6980.000	1.27	20.52	18.57	1.25	74.67	19.08
7040.000	1.34	20.40	16.74	1.22	83.46	20.05
7100.000	1.37	20.54	16.16	1.10	85.09	26.08
7160.000	1.41	21.15	15.41	1.27	68.59	18.46
7220.000	1.48	21.89	14.21	1.19	75.98	15.81
7280.000	1.58	22.43	13.00	1.31	93.61	17.48
7340.000	1.57	23.50	13.03	1.39	80.19	15.77
7400.000	1.57	25.23	13.03	1.38	80.47	15.96
7460.000	1.62	26.92	12.51	1.15	75.17	23.29
7520.000	1.66	27.90	12.09	1.35	76.20	16.64
7580.000	**1.63**	**28.82**	**12.44**	**1.26**	**68.90**	**18.87**
7640.000	1.56	31.69	13.16	1.48	79.58	14.32
7700.000	1.54	36.16	13.44	2.23	72.67	8.38
7760.000	1.52	37.67	13.70	2.65	69.22	6.88
7820.000	1.52	35.88	13.75	2.42	70.21	7.63
7880.000	1.44	33.59	14.87	1.74	78.04	11.33
7940.000	1.35	32.80	16.47	1.22	70.65	19.93
8000.000	1.34	33.31	16.77	1.08	64.82	28.79

REF PLANE ENT.(M): INPUT= .00 TRAN= .00 OUTPUT= .00
NPAIL(1)= 4



GPM4 G14001 7.18/78 0 13 SEP 82 14:25:58

SWITCH MATRIX POC MODEL TESTING

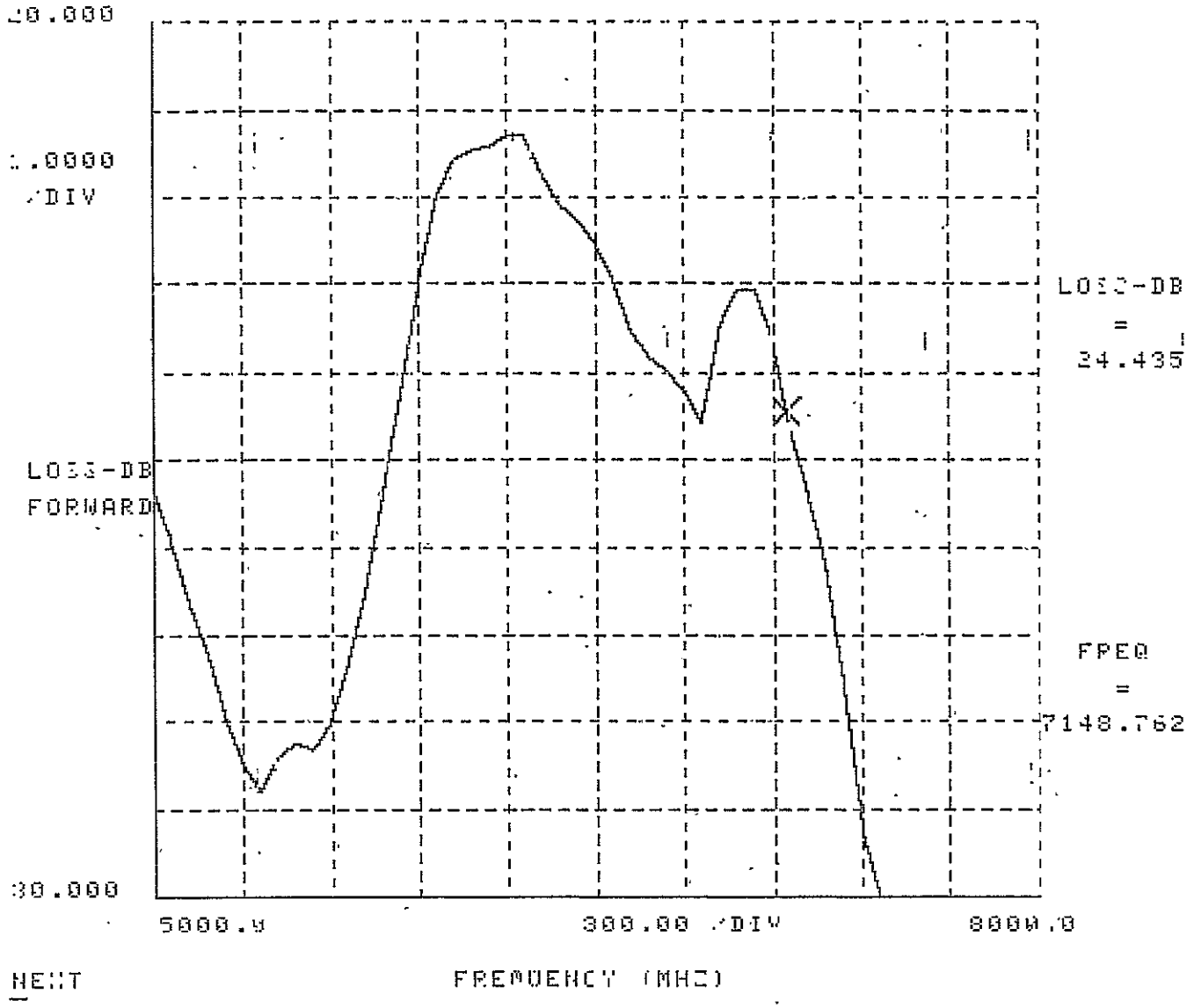
REFERENCE LAB NOTEBOOK 386-2 P42

7,2 ON NAS203::41

FREQ-MHZ	VSWR FORWARD	LOSS-DB FTN LOSS FORWARD	VSWR REVERSE	LOSS-DB REVERSE	FTN LOSS REVERSE
5000.000	1.22	25.35	20.18	1.04	33.47	33.99
5060.000	1.21	25.94	20.58	1.03	79.34	37.90
5120.000	1.16	26.63	22.82	1.04	88.50	33.98
5180.000	1.14	27.19	23.74	1.09	89.06	27.59
5240.000	1.13	27.94	24.45	1.14	85.66	23.60
5300.000	1.13	28.48	24.20	1.13	75.49	24.34
5360.000	1.12	28.80	24.74	1.07	81.60	29.41
5420.000	1.11	28.39	25.30	1.07	79.00	29.24
5480.000	1.09	28.24	27.67	1.15	81.99	23.38
5540.000	1.07	28.32	29.28	1.13	70.53	24.09
5600.000	1.07	28.00	28.98	1.05	75.25	32.10
5660.000	1.06	27.32	30.83	1.06	79.51	31.07
5720.000	1.05	26.43	32.18	1.08	76.93	28.82
5780.000	1.02	25.33	42.20	1.04	76.05	35.21
5840.000	1.01	24.22	42.98	1.06	77.48	30.79
5900.000	1.02	23.02	38.23	1.24	84.57	19.44
5960.000	1.03	22.03	36.31	1.43	77.72	15.00
6020.000	1.06	21.57	30.05	1.41	79.09	15.32
6080.000	1.09	21.45	27.34	1.20	77.06	20.82
6140.000	1.08	21.42	27.94	1.17	81.47	22.04
6200.000	1.12	21.30	25.14	1.22	74.46	20.19
6260.000	1.13	21.28	24.22	1.09	87.23	27.05
6320.000	1.12	21.73	24.63	1.12	75.77	25.29
6380.000	1.11	22.10	25.56	1.16	84.16	22.68
6440.000	1.10	22.27	26.61	1.16	75.82	22.60
6500.000	1.09	22.54	26.96	1.19	74.15	21.18
6560.000	1.07	22.96	29.22	1.21	80.13	20.58
6620.000	1.02	23.54	40.93	1.12	82.79	25.10
6680.000	1.03	23.83	37.37	1.08	79.77	28.05
6740.000	1.08	23.97	28.64	1.05	76.76	31.59
6800.000	1.13	24.19	24.60	1.06	75.82	30.57
6860.000	1.17	24.59	22.09	1.09	74.81	27.26
6920.000	1.22	23.51	19.97	1.15	78.17	23.17
6980.000	1.32	23.06	17.18	1.21	76.56	20.56
7040.000	1.39	23.06	15.71	1.18	81.25	21.76
7100.000	1.42	23.63	15.23	1.05	84.47	31.63
7160.000	1.45	24.62	14.65	1.12	68.97	25.12
7220.000	1.53	25.37	13.66	1.14	73.66	23.60
7280.000	1.60	26.23	12.68	1.13	77.04	24.13
7340.000	1.60	27.61	12.74	1.25	79.09	18.96
7400.000	1.60	29.22	12.77	1.18	88.49	21.64
7460.000	1.64	30.56	12.33	1.20	79.84	20.99
7520.000	1.67	31.32	11.97	1.54	79.52	13.45
7580.000	1.64	31.75	12.32	1.48	68.95	14.28
7640.000	1.57	33.18	13.07	1.35	74.73	16.53
7700.000	1.55	36.19	13.38	2.87	75.70	9.16
7760.000	1.53	37.60	13.63	2.68	73.67	6.81
7820.000	1.52	37.41	13.73	2.51	72.64	7.33
7880.000	1.44	36.88	14.85	1.00	77.25	10.91
7940.000	1.36	36.94	16.43	1.27	71.51	18.52
8000.000	1.34	37.29	16.68	1.48	69.53	28.76

REF PLANE EXT(M): INPUT= .00 TRAN= .00 OUTPUT= .00

NRAIL(1)= 4



GPM4 G14001 7/18/78 0 13 SEP 82 14:30:04

SWITCH MATRIX POC MODEL TESTING
REFERENCE LAB NOTEBOOK 386-2 P42
8,1 MH HA3205::41

FREQ-MHZ	VSWR FORWARD	LOSS-DB FORWARD	PTH LOSS FORWARD	VSWR REVERSE	LOSS-DB REVERSE	PTH LOSS REVERSE
5000.000	1.09	23.49	26.95	1.03	90.59	35.42
5060.000	1.07	23.84	29.95	1.08	82.25	28.46
5120.000	1.04	24.32	33.33	1.13	92.81	24.09
5180.000	1.06	24.85	31.32	1.14	82.17	23.43
5240.000	1.07	25.45	29.20	1.09	83.01	27.33
5300.000	1.07	25.95	29.56	1.06	78.63	31.02
5360.000	1.06	26.36	30.37	1.09	75.24	26.97
5420.000	1.06	26.52	30.58	1.09	86.01	27.27
5480.000	1.08	26.35	28.10	1.06	75.28	30.77
5540.000	1.09	26.23	27.49	1.06	74.66	30.71
5600.000	1.10	25.92	26.77	1.03	75.64	37.38
5660.000	1.09	25.45	27.53	1.09	78.67	27.18
5720.000	1.09	24.59	27.75	1.22	73.76	20.13
5780.000	1.10	23.60	26.33	1.25	72.96	19.17
5840.000	1.10	22.71	26.22	1.14	73.07	23.81
5900.000	1.10	22.08	26.56	1.07	71.87	29.75
5960.000	1.09	21.34	27.52	1.14	72.03	23.97
6020.000	1.10	20.27	26.40	1.08	73.96	27.87
6080.000	1.11	19.39	26.04	1.17	78.23	22.28
6140.000	1.09	19.06	27.35	1.22	86.76	19.94
6200.000	1.12	19.19	25.23	1.10	84.78	26.45
6260.000	1.14	19.48	23.62	1.07	78.70	29.48
6320.000	1.14	19.73	23.46	1.12	78.73	24.92
6380.000	1.15	19.84	23.18	1.06	83.66	30.52
6440.000	1.17	20.14	22.09	1.09	76.24	27.47
6500.000	1.19	20.74	21.16	1.12	74.21	24.79
6560.000	1.19	20.87	21.25	1.16	80.63	22.45
6620.000	1.15	20.92	23.18	1.22	81.32	20.25
6680.000	1.14	20.92	23.79	1.16	71.74	22.61
6740.000	1.14	21.70	23.81	1.12	78.19	24.91
6800.000	1.11	21.87	25.59	1.25	72.50	19.15
6860.000	1.09	21.96	27.36	1.34	74.16	16.71
6920.000	1.11	21.21	25.88	1.30	76.14	17.69
6980.000	1.15	21.62	22.91	1.27	81.27	18.61
7040.000	1.21	21.56	20.41	1.25	74.10	19.24
7100.000	1.25	21.76	18.95	1.13	77.75	24.56
7160.000	1.32	21.99	17.24	1.29	71.42	17.96
7220.000	1.41	22.05	15.46	1.41	79.16	15.44
7280.000	1.49	22.90	14.08	1.33	76.45	16.92
7340.000	1.53	24.18	13.64	1.44	74.63	14.90
7400.000	1.57	25.51	13.12	1.41	77.68	15.34
7460.000	1.64	26.50	12.31	1.17	95.65	22.27
7520.000	1.70	27.44	11.76	1.37	85.45	16.04
7580.000	1.69	28.59	11.85	1.28	78.57	18.23
7640.000	1.65	31.06	12.25	1.53	93.02	13.51
7700.000	1.65	34.27	12.25	2.08	74.11	7.76
7760.000	1.64	35.26	12.30	2.05	80.42	6.37
7820.000	1.62	34.59	12.53	2.55	71.92	7.20
7880.000	1.52	33.95	13.71	1.00	79.87	10.90
7940.000	1.42	34.25	15.22	1.24	72.02	19.45
8000.000	1.40	35.46	15.52	1.08	78.42	27.96

REF PLANE EXTENSION: INPUT= .00 TRAN= .00 OUTPUT= .00
NPAIL(1)= 4

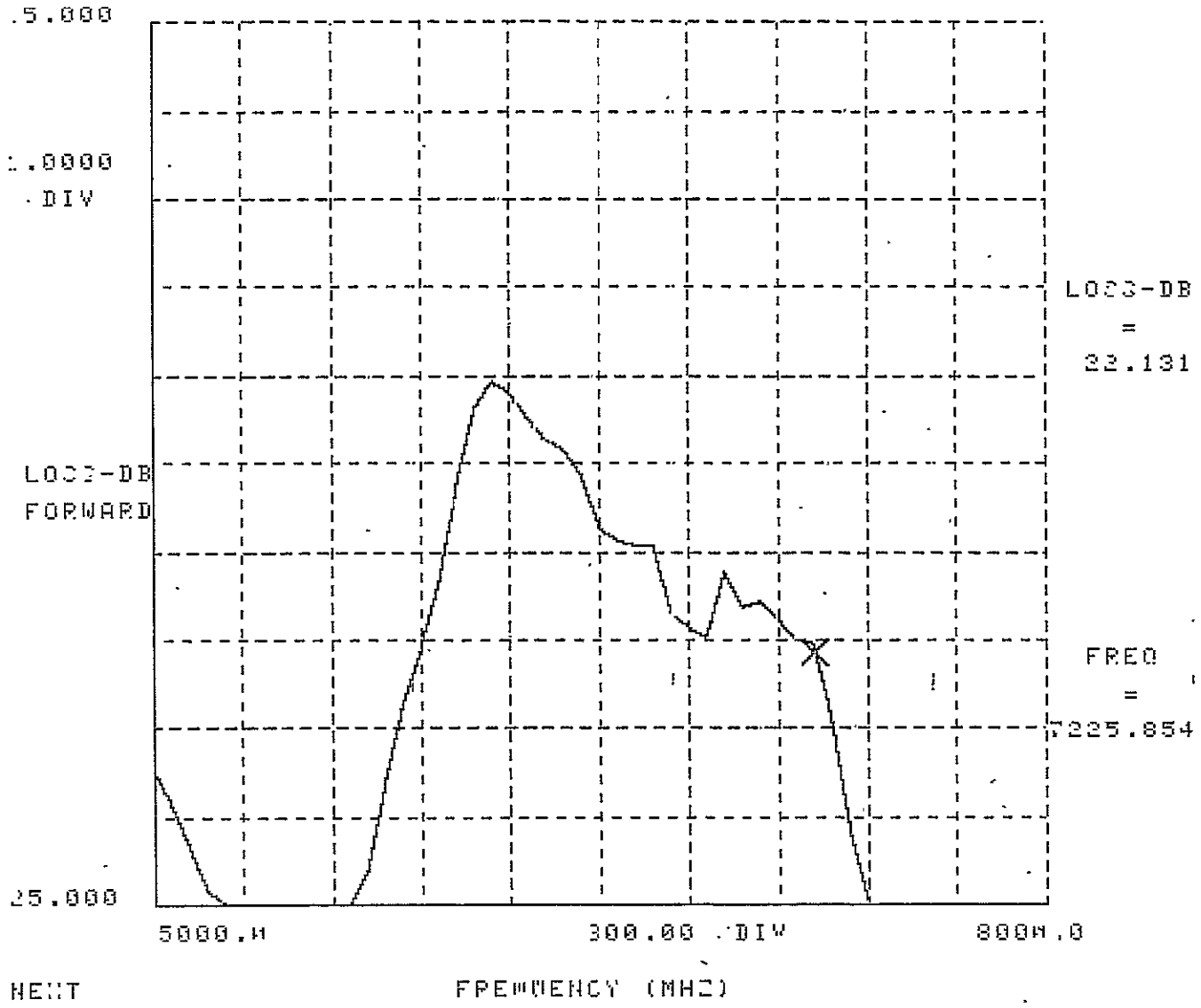
ORIGINAL PAGE IS
OF POOR QUALITY

GPM4 G14001 7/18/78 0 13 SEP 82 14:07:26

SWITCH MATRIX POC MODEL TESTING

REFERENCE LAB NOTEBOOK 38M-2 P42

8,1 MN MA3205::41M

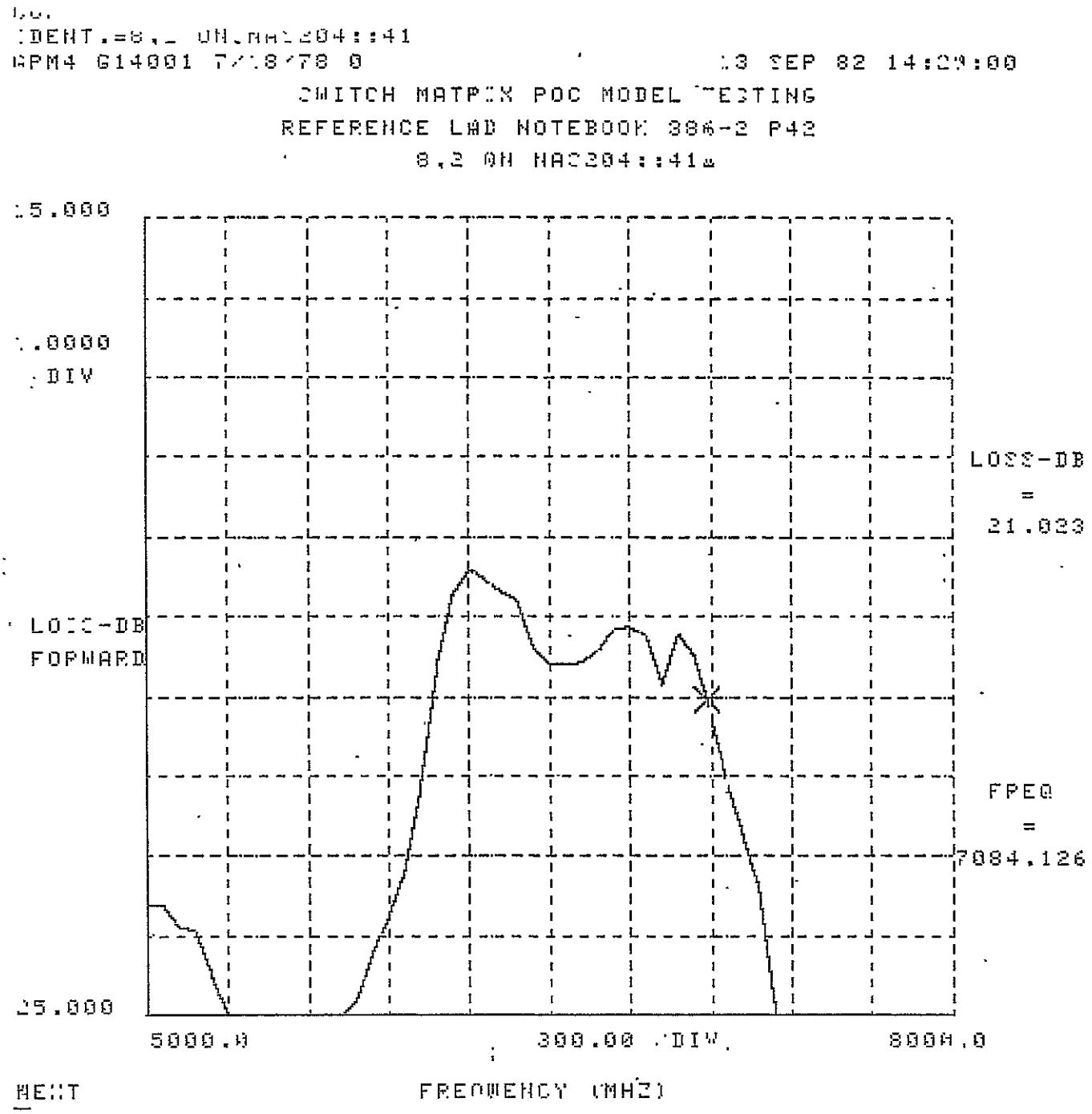


GPM4 G14001 T.:8.78 0 :3 SEP 82 14:29:51

SWITCH MATRIX POC MODEL TESTING
REFERENCE LWD NOTEBOOK 386-2 P42
8.2 MN NAC204::41

FREQ-MHZ	VSWR FORWARD	LOSS-DB FORWARD	RTN LOSS FORWARD	VSWR REVERSE	LOSS-DB REVERSE	RTN LOSS REVERSE
5000.000	1.12	23.62	25.13	1.04	87.52	34.34
5060.000	1.09	23.60	27.29	1.03	87.50	36.36
5120.000	1.06	23.89	30.76	1.05	95.09	33.04
5180.000	1.07	23.94	29.47	1.09	80.10	27.35
5240.000	1.07	24.50	29.22	1.14	82.94	23.41
5300.000	1.07	25.16	29.94	1.13	82.40	24.02
5360.000	1.05	25.91	31.52	1.07	76.22	29.15
5420.000	1.03	26.25	35.37	1.07	81.55	29.49
5480.000	1.04	26.50	34.18	1.14	76.59	23.44
5540.000	1.04	26.21	34.26	1.13	68.78	24.17
5600.000	1.05	25.83	32.28	1.05	78.01	32.71
5660.000	1.04	25.53	34.96	1.06	79.25	30.70
5720.000	1.03	25.27	37.37	1.08	81.71	28.51
5780.000	1.05	24.81	32.42	1.04	74.96	34.89
5840.000	1.07	24.20	29.68	1.07	75.39	29.75
5900.000	1.08	23.76	28.76	1.25	77.41	19.04
5960.000	1.09	23.19	27.73	1.45	76.42	14.75
6020.000	1.12	22.15	24.82	1.43	73.28	15.04
6080.000	1.15	20.66	23.11	1.21	76.78	20.54
6140.000	1.15	19.73	23.10	1.17	76.10	22.13
6200.000	1.19	19.42	21.14	1.22	85.47	20.22
6260.000	1.21	19.53	20.34	1.09	73.76	27.46
6320.000	1.21	19.68	20.43	1.12	76.75	24.99
6380.000	1.20	19.78	20.69	1.17	78.68	22.22
6440.000	1.20	20.40	20.85	1.17	79.53	22.22
6500.000	1.20	20.59	20.76	1.19	75.69	21.11
6560.000	1.18	20.60	21.50	1.20	81.33	20.73
6620.000	1.13	20.57	24.23	1.12	79.72	25.26
6680.000	1.10	20.42	26.53	1.07	78.10	28.92
6740.000	1.06	20.16	30.35	1.05	83.52	32.75
6800.000	1.05	20.13	32.04	1.06	79.18	30.84
6860.000	1.06	20.23	30.63	1.10	70.64	26.77
6920.000	1.11	20.86	25.49	1.16	77.22	22.85
6980.000	1.20	20.22	20.66	1.21	79.27	20.33
7040.000	1.28	20.51	18.35	1.18	79.63	21.50
7100.000	1.32	21.21	17.24	1.06	76.81	31.11
7160.000	1.37	22.07	16.14	1.12	70.48	25.02
7220.000	1.45	22.74	14.66	1.15	80.57	23.38
7280.000	1.53	23.42	13.52	1.14	84.79	23.73
7340.000	1.55	25.12	13.34	1.26	79.26	18.71
7400.000	1.57	26.75	13.13	1.18	87.28	21.50
7460.000	1.63	27.72	12.46	1.20	82.98	20.85
7520.000	1.68	28.23	11.91	1.55	73.05	13.28
7580.000	1.67	28.70	12.01	1.49	75.23	14.12
7640.000	1.63	30.58	12.46	1.36	78.74	16.28
7700.000	1.62	33.94	12.50	2.11	84.58	8.96
7760.000	1.62	35.84	12.50	2.74	73.81	6.66
7820.000	1.62	35.02	12.57	2.55	73.34	7.20
7880.000	1.52	33.39	13.66	1.82	78.03	10.76
7940.000	1.42	32.60	15.19	1.28	72.54	18.34
8000.000	1.40	32.46	15.53	1.08	71.75	28.49

REF PLANE ENT(MM): INPUT= .00 TRAN= .00 OUTPUT= .00
MPAIL(1)= 4



GPM4 G14001 7[illegible] 0 [illegible] 13 SEP 82 15:[illegible]:33

SWITCH MATRIX POC MODEL TESTING
REFERENCE LAB NOTEBOOK 386-2 P43
9,1 HN NAS206::41

FREQ-MHZ	VSWR FORWARD	LOSS-DB FORWARD	RTN LOSS FORWARD	VSWR REVERSE	LOSS-DB REVERSE	RTN LOSS REVERSE
5000.000	1.14	20.66	23.47	1.04	82.48	34.93
5060.000	1.11	20.49	25.95	1.08	90.63	28.69
5120.000	1.10	20.73	26.05	1.13	104.69	24.37
5180.000	1.13	21.10	24.20	1.14	80.27	23.63
5240.000	1.12	21.61	24.78	1.09	82.12	27.53
5300.000	1.11	22.08	25.67	1.06	75.63	30.42
5360.000	1.10	22.58	26.76	1.10	77.63	26.49
5420.000	1.10	23.04	26.75	1.10	78.94	26.70
5480.000	1.10	23.32	26.64	1.06	75.73	30.29
5540.000	1.08	23.34	28.13	1.06	75.43	30.76
5600.000	1.06	23.22	30.68	1.03	72.17	37.50
5660.000	1.06	23.07	30.30	1.10	74.97	26.62
5720.000	1.06	22.91	30.48	1.23	81.98	19.78
5780.000	1.06	22.57	30.93	1.25	73.70	18.94
5840.000	1.07	21.79	29.12	1.14	75.23	23.55
5900.000	1.08	20.70	28.11	1.07	83.30	29.04
5960.000	1.10	19.62	26.28	1.13	75.59	24.21
6020.000	1.12	18.68	25.15	1.07	81.44	29.25
6080.000	1.13	17.96	24.29	1.17	70.02	21.93
6140.000	1.15	17.39	23.28	1.25	73.57	19.20
6200.000	1.17	16.71	21.90	1.13	74.79	24.44
6260.000	1.19	16.31	21.11	1.05	76.65	32.72
6320.000	1.19	16.37	21.34	1.10	90.43	26.85
6380.000	1.20	16.71	20.84	1.07	80.45	29.08
6440.000	1.22	17.10	20.14	1.11	73.28	25.39
6500.000	1.21	17.63	20.30	1.12	82.35	25.27
6560.000	1.20	18.03	20.88	1.14	77.55	23.45
6620.000	1.17	18.53	22.07	1.20	84.02	20.64
6680.000	1.16	18.91	22.38	1.17	72.52	22.01
6740.000	1.16	19.42	22.72	1.14	76.46	23.97
6800.000	1.14	19.50	23.64	1.25	75.30	19.19
6860.000	1.14	19.12	23.41	1.24	72.99	16.84
6920.000	1.17	18.39	22.13	1.29	75.05	17.82
6980.000	1.21	18.74	20.58	1.27	75.29	18.51
7040.000	1.25	18.95	19.17	1.26	75.60	18.78
7100.000	1.28	19.36	18.19	1.14	87.75	23.96
7160.000	1.34	19.89	16.86	1.29	68.92	18.07
7220.000	1.39	20.61	15.75	1.40	74.53	15.51
7280.000	1.45	21.91	14.79	1.34	74.89	16.76
7340.000	1.46	23.74	14.60	1.46	71.95	14.54
7400.000	1.49	25.27	14.19	1.43	72.86	15.02
7460.000	1.53	26.21	13.56	1.17	82.63	22.13
7520.000	1.55	27.22	13.37	1.38	70.36	15.99
7580.000	1.51	28.68	13.82	1.28	73.94	18.14
7640.000	1.46	31.80	14.53	1.56	78.77	13.24
7700.000	1.45	36.09	14.65	2.43	87.01	7.58
7760.000	1.43	37.65	15.09	2.91	75.20	6.22
7820.000	1.38	36.52	15.91	2.60	76.68	7.06
7880.000	1.30	34.93	17.76	1.81	79.54	10.77
7940.000	1.22	34.51	20.08	1.24	81.90	19.31
8000.000	1.22	35.17	19.92	1.48	72.95	28.17

REF PLANE EXT (M): INPUT= .00 TRAN= .00 OUTPUT= .00
NFAIL(1)= 4

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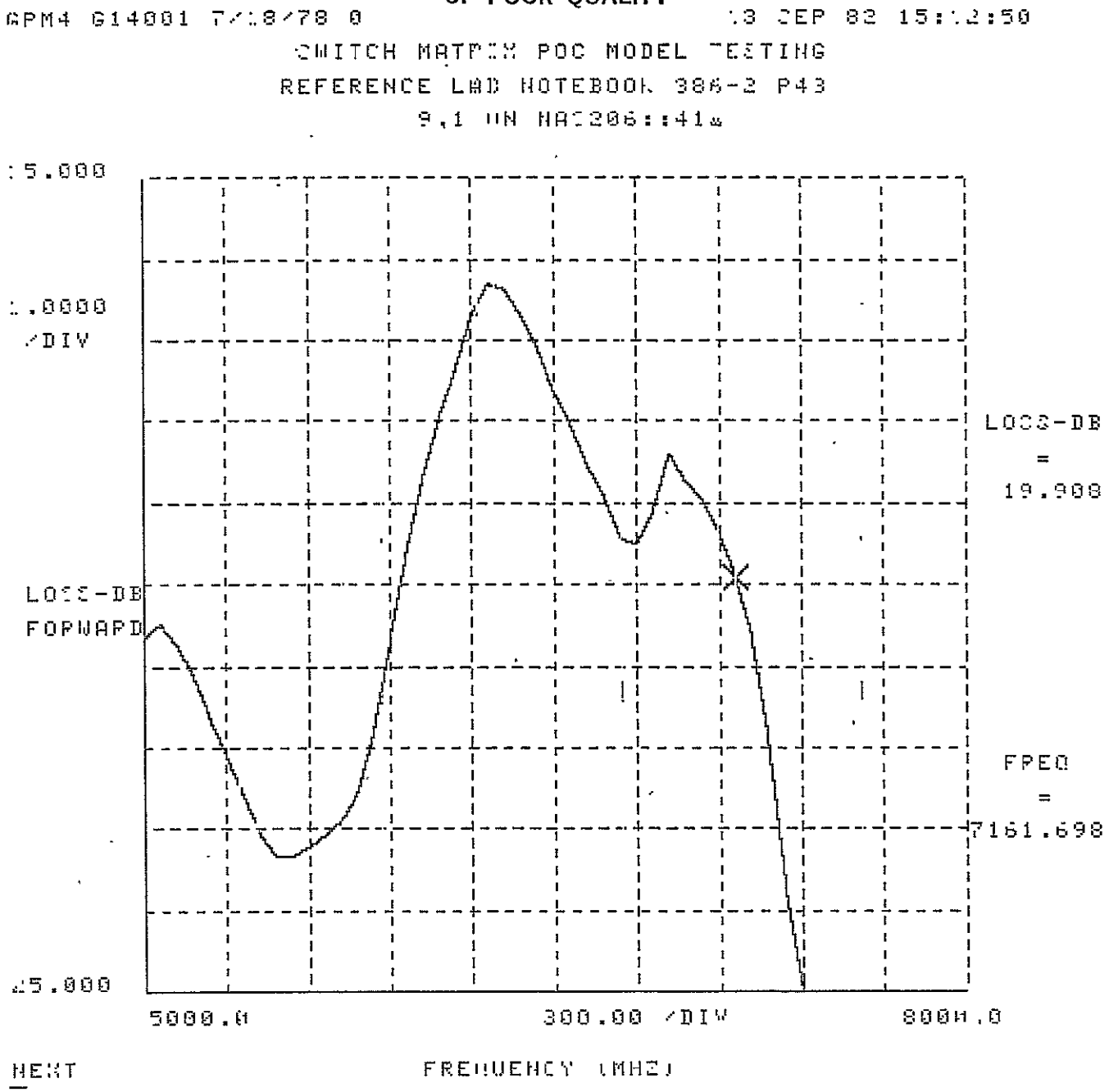

HPM4 G14001 7.18.78 0 13 SEP 82 15:17:04

SWITCH MATRIX POC MODEL TESTING
REFERENCE LAB NOTEBOOK 38A-2 P43
9.2 ON HAC207::41

FREQ-MHZ	VSWR FORWARD	LOSS-DB FORWARD	PTN LOSS FORWARD	VSWR REVERSE	LOSS-DB REVERSE	PTN LOSS REVERSE
5000.000	1.17	23.84	22.12	1.04	80.72	33.32
5060.000	1.13	23.34	24.57	1.04	75.66	34.00
5120.000	1.10	23.38	26.42	1.05	80.17	31.62
5180.000	1.11	23.70	25.72	1.10	84.83	26.20
5240.000	1.09	23.83	27.28	1.06	81.49	22.76
5300.000	1.07	24.34	29.85	1.04	79.09	23.45
5360.000	1.05	24.85	32.08	1.07	74.28	29.44
5420.000	1.06	25.06	31.06	1.08	87.91	28.47
5480.000	1.06	25.57	30.14	1.15	81.18	23.06
5540.000	1.06	25.86	30.62	1.13	72.41	24.27
5600.000	1.06	25.69	31.16	1.05	79.90	32.02
5660.000	1.09	25.20	27.72	1.07	79.33	28.88
5720.000	1.10	24.64	26.54	1.08	77.03	27.95
5780.000	1.10	23.89	26.19	1.03	74.15	35.73
5840.000	1.13	22.97	24.37	1.08	74.29	27.98
5900.000	1.14	22.00	23.55	1.28	78.42	18.10
5960.000	1.16	21.03	22.38	1.48	75.96	14.28
6020.000	1.18	20.14	21.65	1.44	77.24	14.92
6080.000	1.19	19.42	21.34	1.20	82.52	20.94
6140.000	1.19	19.06	21.06	1.18	79.03	21.76
6200.000	1.21	18.63	20.33	1.22	80.33	20.03
6260.000	1.22	18.21	20.14	1.08	89.65	28.15
6320.000	1.19	18.18	21.03	1.12	90.19	25.29
6380.000	1.18	18.67	21.55	1.16	84.94	22.61
6440.000	1.18	19.38	21.70	1.16	80.94	22.69
6500.000	1.16	19.99	22.58	1.20	74.33	20.67
6560.000	1.13	20.12	24.22	1.22	78.46	20.09
6620.000	1.09	19.98	27.27	1.15	78.98	23.22
6680.000	1.08	19.87	27.91	1.10	71.38	26.45
6740.000	1.10	19.95	26.71	1.07	77.97	29.61
6800.000	1.12	20.03	24.79	1.06	72.14	30.10
6860.000	1.17	20.09	22.28	1.10	74.80	26.76
6920.000	1.23	20.54	19.59	1.16	73.96	22.38
6980.000	1.30	20.33	17.69	1.23	70.90	19.81
7040.000	1.35	20.48	16.54	1.19	75.49	21.07
7100.000	1.38	20.61	15.86	1.15	78.86	32.46
7160.000	1.43	20.65	15.03	1.13	73.12	24.22
7220.000	1.46	20.52	14.50	1.16	79.30	22.69
7280.000	1.50	21.55	14.04	1.17	80.86	22.25
7340.000	1.48	23.10	14.26	1.20	75.40	17.79
7400.000	1.48	24.34	14.27	1.19	79.92	21.14
7460.000	1.51	25.09	13.88	1.22	84.50	19.94
7520.000	1.51	25.98	13.81	1.60	75.44	12.78
7580.000	**1.48**	**27.14**	**14.32**	**1.52**	**72.31**	**13.76**
7640.000	1.42	29.38	15.16	1.40	79.30	15.57
7700.000	1.41	32.96	15.31	2.20	80.68	8.50
7760.000	1.39	35.01	15.68	2.86	70.79	6.35
7820.000	1.35	34.67	16.47	2.63	72.56	6.95
7880.000	1.23	33.73	18.22	1.85	99.49	10.49
7940.000	1.20	30.40	20.71	1.30	81.09	17.70
8000.000	1.21	28.46	20.38	1.10	76.75	26.59

REF PLANE EXT (M): INPUT= .00 TRAN= .00 OUTPUT= .00
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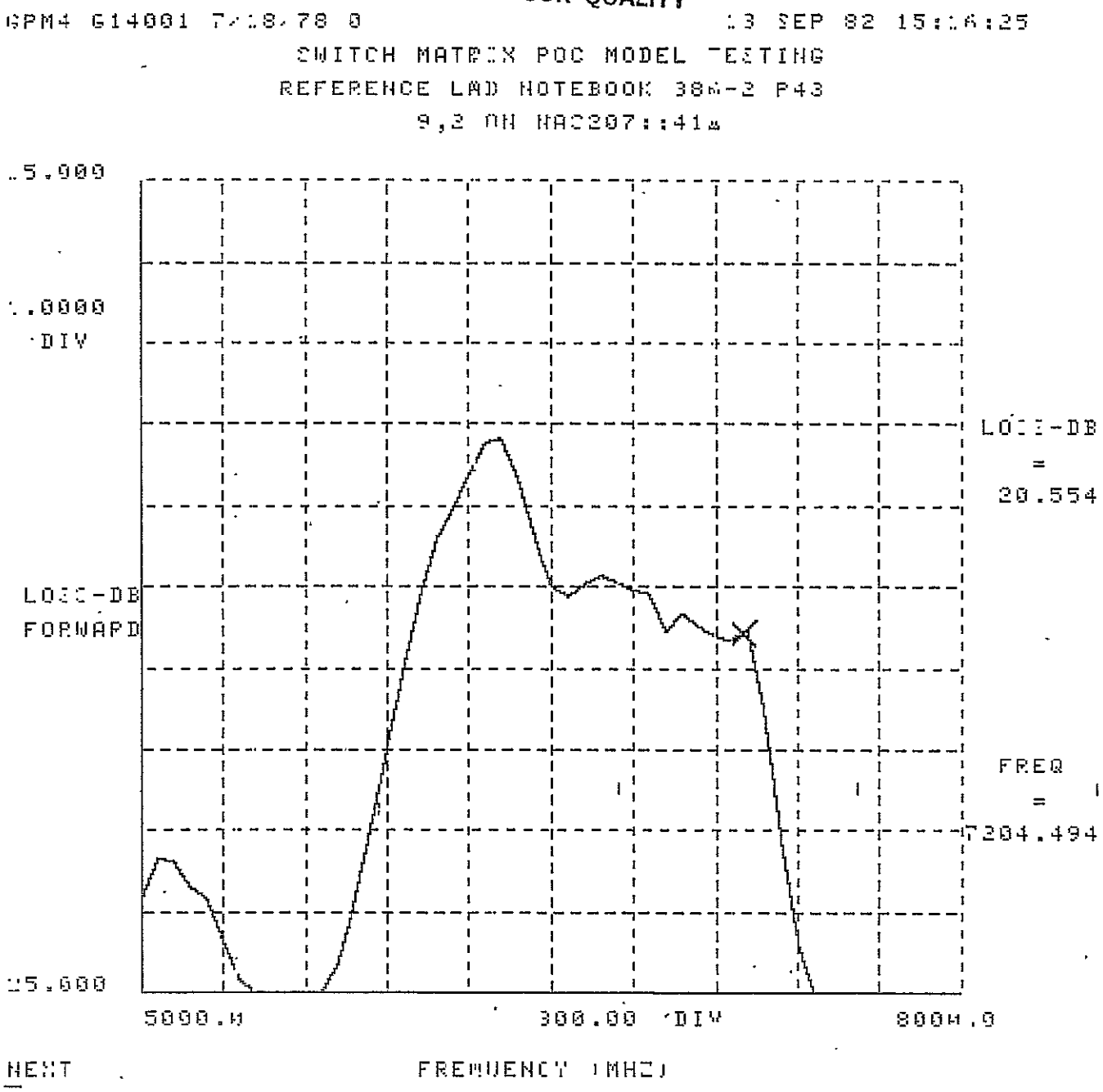

GPM4 G14001 7/18/78 0 .8 SEP 82 15:24:42

SWITCH MATRIX POC MODEL TESTING
REFERENCE LAB NOTEBOOK 386-2 P43
11,1 ON MAR209::41

FREQ-MHZ	VSWR FORWARD	LOSS-DB FORWARD	RTN LOSS FORWARD	VSWR REVERSE	LOSS-DB REVERSE	RTN LOSS REVERSE
5000.000	1.10	24.65	26.50	1.03	86.77	35.35
5060.000	1.09	24.88	27.21	1.08	90.14	28.10
5120.000	1.07	25.12	29.67	1.04	83.47	23.95
5180.000	1.06	25.34	30.07	1.05	80.06	23.29
5240.000	1.06	25.51	31.35	1.09	87.05	27.17
5300.000	1.08	25.70	28.75	1.06	76.31	30.98
5360.000	1.09	25.88	27.37	1.00	74.49	26.82
5420.000	1.11	25.93	25.40	1.10	81.42	26.85
5480.000	1.12	25.71	24.66	1.06	79.08	30.09
5540.000	1.12	25.51	24.63	1.06	72.45	30.36
5600.000	1.12	25.16	24.95	1.03	76.08	36.55
5660.000	1.14	24.86	23.75	1.10	83.03	26.54
5720.000	1.15	24.52	23.12	1.23	77.43	19.70
5780.000	1.15	23.92	22.92	1.26	79.36	18.85
5840.000	1.15	23.04	23.00	1.15	80.21	23.39
5900.000	1.15	22.10	23.29	1.07	84.36	29.43
5960.000	1.14	21.37	23.50	1.12	73.29	24.63
6020.000	1.15	21.02	23.31	1.08	73.47	28.40
6080.000	1.13	21.03	24.01	1.09	74.19	21.37
6140.000	1.11	21.19	25.75	1.25	73.52	19.21
6200.000	1.11	21.14	25.34	1.11	75.58	25.64
6260.000	1.12	20.87	25.10	1.06	82.85	30.08
6320.000	1.10	20.57	26.42	1.13	76.60	24.49
6380.000	1.09	20.37	27.05	1.07	90.74	29.66
6440.000	1.11	20.38	25.61	1.08	84.84	27.95
6500.000	1.12	20.52	24.68	1.12	77.52	24.71
6560.000	1.12	20.42	24.64	1.17	78.12	21.99
6620.000	1.12	20.10	25.02	1.21	80.25	20.27
6680.000	1.14	19.72	23.94	1.16	77.92	22.85
6740.000	1.16	19.02	22.82	1.12	78.15	24.84
6800.000	1.15	19.66	23.03	1.27	72.03	18.59
6860.000	1.16	19.72	22.54	1.26	71.79	16.29
6920.000	1.18	19.72	21.66	1.30	71.08	17.60
6980.000	1.22	19.62	19.90	1.25	72.91	19.00
7040.000	1.24	19.85	19.34	1.25	77.38	19.17
7100.000	1.26	19.99	18.72	1.14	73.47	23.43
7160.000	1.30	20.75	17.66	1.29	71.78	17.88
7220.000	1.36	21.52	16.34	1.41	76.71	15.47
7280.000	1.40	23.36	15.56	1.04	83.20	16.80
7340.000	1.42	24.63	15.19	1.46	73.81	14.60
7400.000	1.46	25.21	14.55	1.43	93.46	15.05
7460.000	1.52	25.62	13.65	1.17	92.29	21.94
7520.000	1.56	26.70	13.16	1.38	78.32	15.85
7580.000	1.56	28.28	13.16	1.28	73.02	18.14
7640.000	1.54	31.06	13.41	1.56	86.03	13.25
7700.000	1.56	34.34	13.20	2.45	83.48	7.55
7760.000	1.57	34.94	13.11	2.92	73.13	6.19
7820.000	1.54	33.21	13.43	2.60	72.33	7.04
7880.000	1.46	31.10	14.51	1.82	78.01	10.75
7940.000	1.39	29.82	15.83	1.25	85.29	19.22
8000.000	1.40	29.80	15.55	1.08	87.28	28.00

REF PLANE EXTENSION: INPUT= .00 TRAN= .00 OUTPUT= .00
NPAIL(1)= 4

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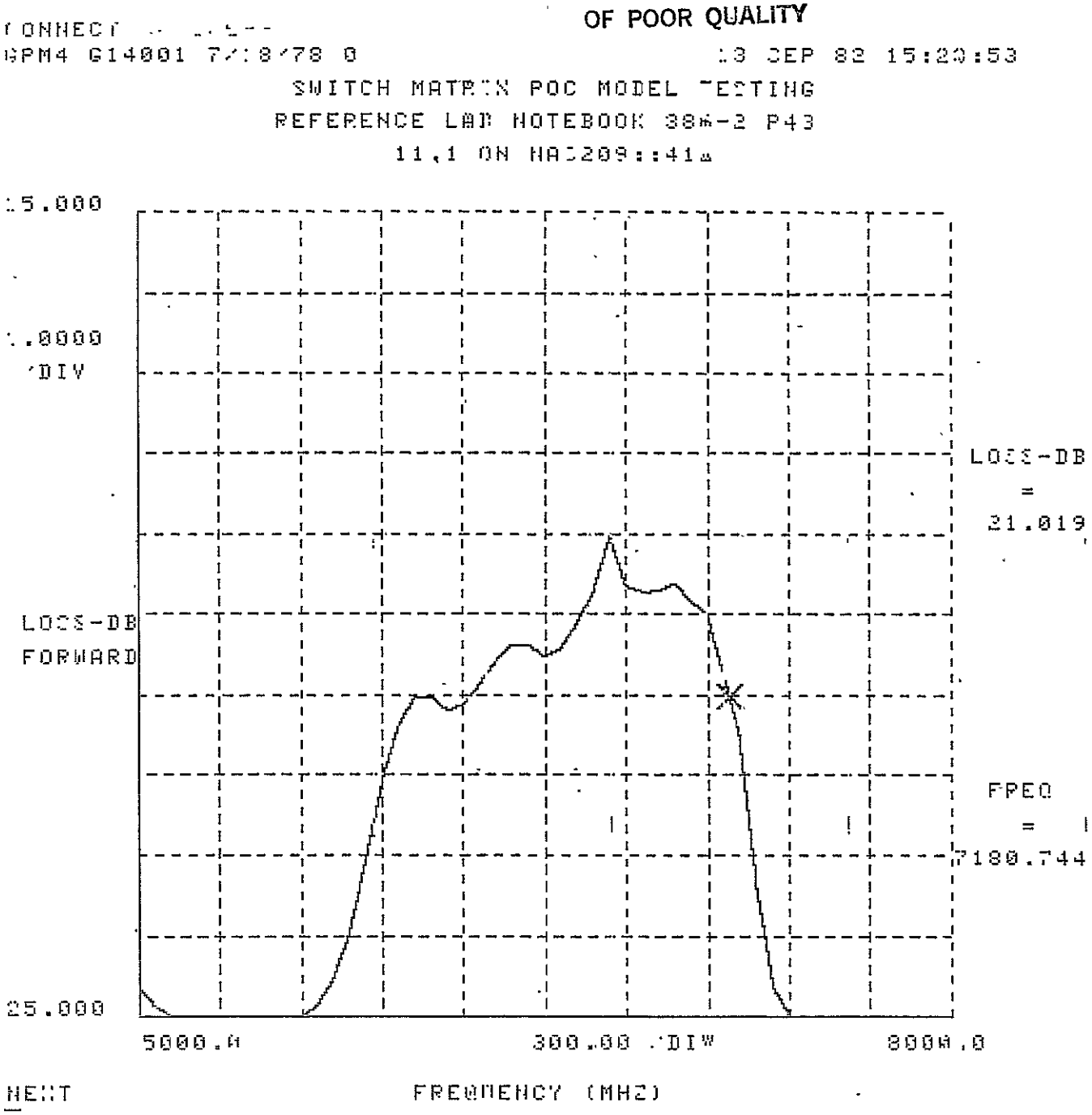


GPM4 G14001 T[illegible] 0 13 SEP 82 15:2M:50

SWITCH MATRIX POC MODEL TESTING
REFERENCE LMB NOTEBOOK 38[illegible]-2 P43
11,2 MN MAC208::41

FREQ-MHZ	VSWR FORWARD	LOSS-DB FORWARD	RTN LOSS FORWARD	VSWR REVERSE	LOSS-DB REVERSE	RTN LOSS REVERSE
5000.000	1.10	21.20	26.61	1.04	77.82	33.46
5060.000	1.09	21.17	27.39	1.04	98.32	33.89
5120.000	1.05	21.52	31.58	1.05	79.23	31.49
5180.000	1.04	22.16	33.68	1.10	86.97	26.08
5240.000	1.03	22.68	36.99	1.06	79.76	22.65
5300.000	1.05	23.54	32.31	1.05	83.54	23.37
5360.000	1.07	24.54	29.83	1.07	73.62	29.56
5420.000	1.09	24.96	27.61	1.08	76.50	28.60
5480.000	1.10	25.52	26.80	1.05	78.37	23.02
5540.000	1.10	25.78	26.41	1.03	71.45	24.19
5600.000	1.10	25.35	26.59	1.05	72.96	32.01
5660.000	1.12	24.95	24.73	1.07	80.13	29.10
5720.000	1.13	24.48	24.09	1.08	77.66	28.05
5780.000	1.14	23.90	23.66	1.03	74.44	35.96
5840.000	1.15	23.05	23.19	1.08	72.22	28.24
5900.000	1.15	22.07	23.02	1.28	83.13	18.17
5960.000	1.16	21.03	22.80	1.48	78.09	14.32
6020.000	1.17	20.09	22.31	1.43	76.82	14.96
6080.000	1.16	19.33	22.47	1.20	78.78	20.94
6140.000	1.14	19.06	23.46	1.18	79.01	21.61
6200.000	1.15	19.10	22.90	1.22	74.41	19.95
6260.000	1.16	19.03	22.80	1.08	83.53	28.70
6320.000	1.14	19.07	23.91	1.02	81.07	25.00
6380.000	1.12	19.25	24.96	1.17	84.76	21.96
6440.000	1.12	19.78	24.85	1.17	81.48	22.32
6500.000	1.12	20.54	24.65	1.19	71.78	21.13
6560.000	1.11	21.32	25.32	1.20	76.72	20.84
6620.000	1.09	21.81	26.99	1.13	83.70	24.24
6680.000	1.10	22.04	26.44	1.09	74.19	27.61
6740.000	1.11	22.11	25.77	1.07	79.59	29.68
6800.000	1.11	22.30	25.34	1.08	71.44	28.14
6860.000	1.13	22.26	24.11	1.11	75.22	25.54
6920.000	1.16	22.27	22.48	1.06	79.75	22.70
6980.000	1.24	22.39	19.55	1.21	76.65	20.51
7040.000	1.27	21.54	18.36	1.17	75.87	21.89
7100.000	1.31	21.64	17.47	1.13	73.73	35.65
7160.000	1.36	22.41	16.40	1.13	73.05	24.24
7220.000	1.42	23.73	15.17	1.15	76.44	23.09
7280.000	1.46	24.55	14.58	1.16	82.10	22.66
7340.000	1.47	25.75	14.44	1.20	73.74	17.80
7400.000	1.49	26.46	14.07	1.20	81.17	20.94
7460.000	1.55	27.28	13.37	1.23	78.62	19.87
7520.000	1.58	28.64	12.95	1.59	73.57	12.80
7580.000	1.57	30.02	13.06	1.51	74.76	13.84
7640.000	1.54	32.21	13.44	1.40	81.47	15.62
7700.000	1.55	35.23	13.31	2.21	81.28	8.49
7760.000	1.56	36.66	13.23	2.06	71.84	6.34
7820.000	1.53	36.05	13.52	2.63	74.09	6.94
7880.000	1.46	34.88	14.59	1.86	97.15	10.46
7940.000	1.38	34.11	15.93	1.30	80.36	17.68
8000.000	1.39	33.34	15.73	1.30	72.12	26.48

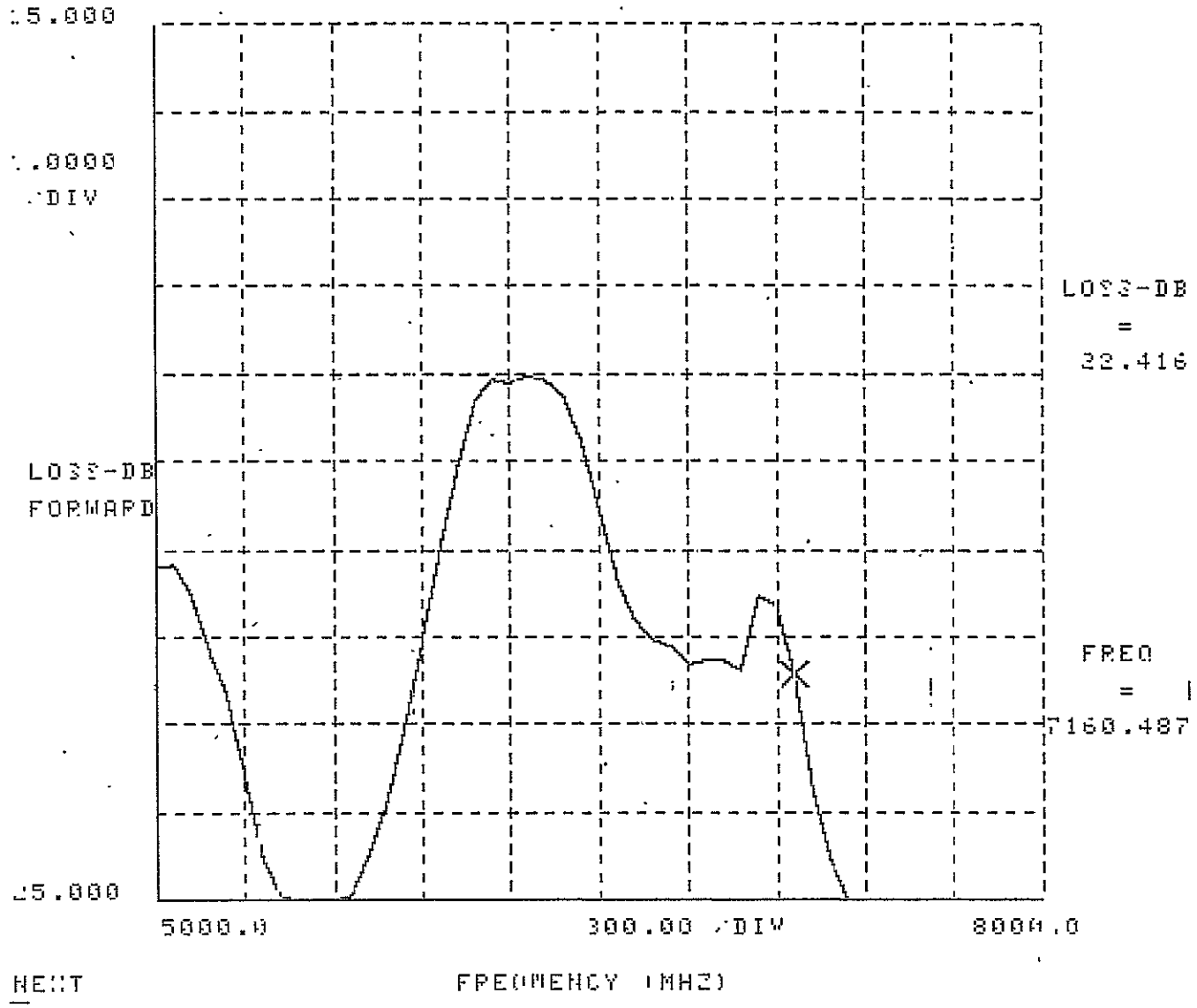
REF PLANE EXT (M): INPUT= .00 TRAN= .00 OUTPUT= .00
MPAIL(1)= 4

GPM4 G14001 7/18/78 0 13 SEP 82 15:28:13

SWITCH MATRIX POC MODEL TESTING

REFERENCE LAB NOTEBOOK 386-2 P43

11.2 GN HA3208::41m



GPM4 G14001 T[illegible]8/78 0 13 SEP 82 15:29:14

SWITCH MATRIX POC MODEL TESTING
REFERENCE LAB NOTEBOOK 386-2 P43
12.1 DH HA3210::41

FREQ-MHZ	VSWR FORWARD	LOSS-DB FORWARD	RTN LOSS FORWARD	VSWR REVERSE	LOSS-DB REVERSE	RTN LOSS REVERSE
5000.000	1.13	23.15	24.30	1.04	77.28	34.85
5060.000	1.09	23.51	27.47	1.08	82.04	28.45
5120.000	1.04	23.76	33.59	1.13	81.15	24.20
5180.000	1.05	24.15	32.37	1.14	75.32	23.49
5240.000	1.05	24.64	31.79	1.09	80.14	27.38
5300.000	1.05	25.00	32.76	1.06	72.75	30.46
5360.000	1.04	25.28	33.83	1.10	72.79	26.58
5420.000	1.07	25.54	29.95	1.10	83.33	26.82
5480.000	1.08	25.72	28.35	1.06	79.06	30.60
5540.000	1.08	25.73	28.11	1.06	71.51	30.95
5600.000	1.08	25.52	27.93	1.02	74.48	38.19
5660.000	1.09	25.07	26.90	1.10	85.13	26.77
5720.000	1.11	24.53	26.01	1.23	73.74	19.86
5780.000	1.12	24.01	25.04	1.25	75.17	19.05
5840.000	1.13	23.46	24.51	1.14	76.50	23.91
5900.000	1.14	22.88	23.86	1.07	78.98	29.02
5960.000	1.15	22.13	22.91	1.14	74.76	23.74
6020.000	1.18	21.28	21.68	1.08	77.67	28.26
6080.000	1.19	20.43	21.11	1.17	78.66	22.28
6140.000	1.20	19.77	21.01	1.23	82.30	19.70
6200.000	1.23	19.45	19.75	1.11	79.73	25.53
6260.000	1.25	19.54	19.02	1.06	85.14	30.32
6320.000	1.25	19.98	19.09	1.10	78.09	26.08
6380.000	1.24	20.45	19.34	1.06	78.12	30.61
6440.000	1.24	21.03	19.37	1.11	78.97	25.97
6500.000	1.24	21.79	19.34	1.12	73.49	24.88
6560.000	1.22	22.20	20.15	1.15	79.26	22.98
6620.000	1.17	22.65	22.16	1.21	77.97	20.52
6680.000	1.13	22.93	24.17	1.17	71.32	22.11
6740.000	1.08	22.68	28.15	1.13	85.55	24.52
6800.000	1.04	23.45	34.22	1.25	72.58	19.20
6860.000	1.01	23.22	42.68	1.35	73.36	16.57
6920.000	1.08	22.74	27.95	1.01	87.19	17.37
6980.000	1.16	22.07	22.56	1.27	81.59	18.47
7040.000	1.22	22.18	19.94	1.24	78.15	19.34
7100.000	1.28	22.12	18.11	1.13	75.58	24.28
7160.000	1.36	22.47	16.39	1.31	71.95	17.48
7220.000	1.44	23.20	14.95	1.42	82.22	15.25
7280.000	1.51	24.04	13.80	1.33	84.12	17.01
7340.000	1.55	25.05	13.34	1.45	75.22	14.76
7400.000	1.59	25.84	12.89	1.43	79.02	15.05
7460.000	1.65	26.91	12.21	1.18	81.51	21.61
7520.000	1.70	28.70	11.74	1.38	70.46	15.95
7580.000	1.70	30.66	11.75	1.28	69.62	18.31
7640.000	1.66	33.44	12.15	1.56	75.40	13.17
7700.000	1.64	36.78	12.32	2.44	80.80	7.55
7760.000	1.64	37.92	12.32	2.91	75.93	6.22
7820.000	1.62	37.40	12.48	2.59	75.86	7.06
7880.000	1.54	36.30	13.45	1.01	82.29	10.80
7940.000	1.45	35.83	14.68	1.24	83.43	19.35
8000.000	1.43	36.11	15.09	1.09	80.12	27.76

REF PLANE ENTERED: INPUT= .00 TRAN= .00 OUTPUT= .00
NPAIRS = 4

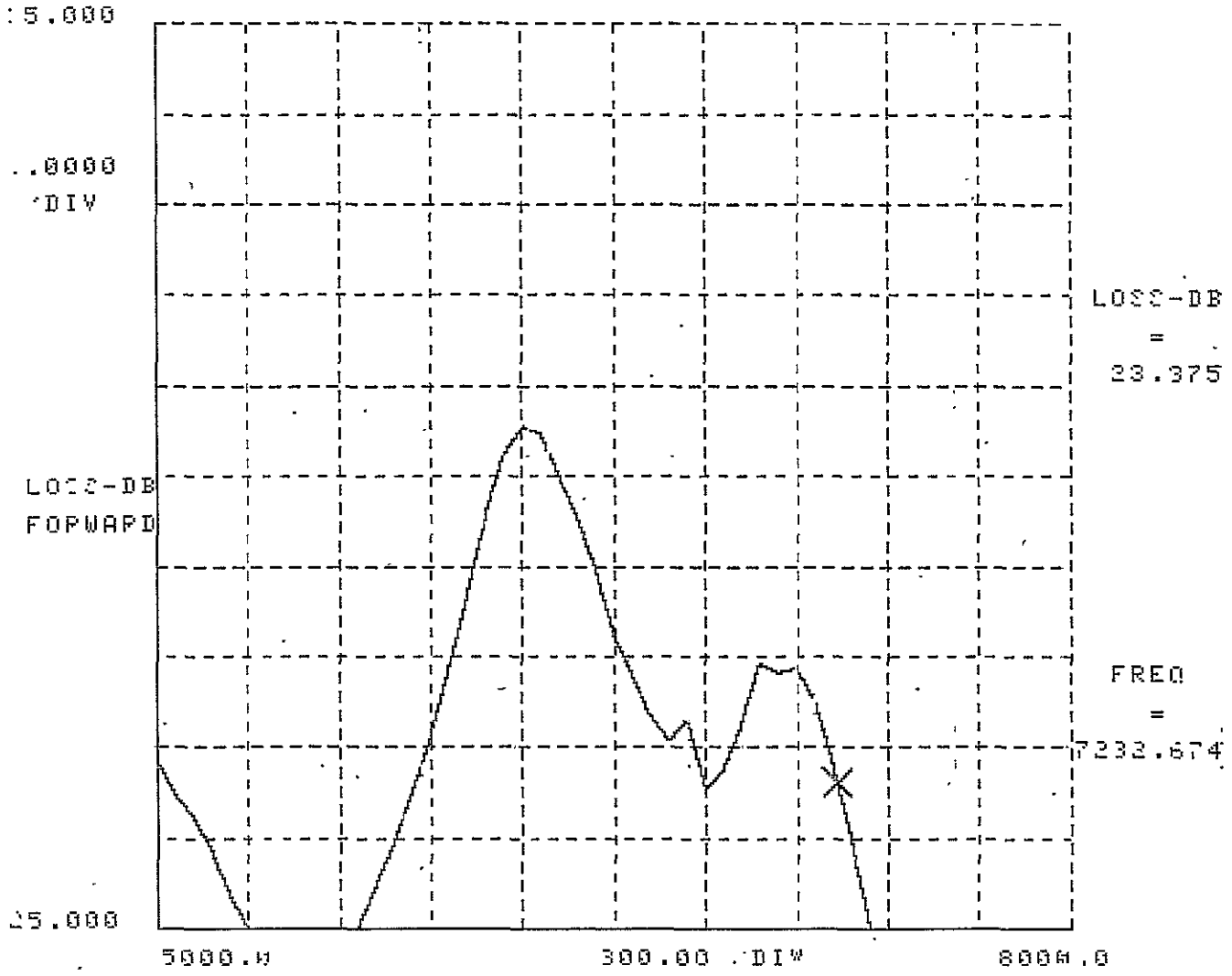
ORIGINAL PAGE IS
OF POOR QUALITY

GPM4 G14001 T/L8.T8 0 :3 SEP 82 15:27:24

SWITCH MATRIX POC MODEL TESTING

REFERENCE LAB NOTEBOOK 386-2 P43

12,1 DH HA:210::41a



NEXT

FREQUENCY (MHZ)

GPM4 G14001 7[illegible].8[illegible]78 0 [illegible] 13 SEP 82 15:[illegible]:49

SWITCH MATRIX POC MODEL TESTING
REFERENCE LAB NOTEBOOK 386-2 P43
12,2 ON HA2211::41

FREQ-MHZ	VSWR FORWARD	LOSS-DB FORWARD	RTN LOSS FORWARD	VSWR REVERSE	LOSS-DB REVERSE	RTN LOSS REVERSE
5000.000	1.15	25.67	23.08	1.04	88.04	33.45
5060.000	1.11	25.61	25.43	1.04	84.98	33.41
5120.000	1.07	26.02	30.01	1.06	83.53	31.22
5180.000	1.06	26.50	31.03	1.10	88.51	26.16
5240.000	1.05	26.62	31.68	1.16	82.66	22.75
5300.000	1.04	26.90	34.45	1.14	76.64	23.45
5360.000	1.02	27.02	41.16	1.07	76.94	29.49
5420.000	1.03	27.25	36.51	1.08	81.09	28.39
5480.000	1.04	27.18	33.85	1.15	73.47	22.99
5540.000	1.04	27.10	33.33	1.13	69.18	24.21
5600.000	1.05	27.03	32.53	1.05	76.50	31.63
5660.000	1.07	26.75	29.21	1.08	80.65	28.77
5720.000	1.09	25.92	27.57	1.09	75.42	27.78
5780.000	1.11	25.21	25.95	1.03	74.50	35.38
5840.000	1.13	24.35	24.42	1.09	77.31	27.61
5900.000	1.15	23.70	23.12	1.09	78.43	17.92
5960.000	1.18	22.97	21.67	1.49	80.44	14.19
6020.000	1.22	22.10	20.24	1.44	76.66	14.84
6080.000	1.24	21.09	19.50	1.20	78.55	20.97
6140.000	1.25	20.26	19.17	1.17	84.05	21.92
6200.000	1.29	19.81	18.07	1.22	77.41	19.92
6260.000	1.31	19.66	17.48	1.08	78.80	27.85
6320.000	1.30	20.15	17.60	1.11	79.48	25.52
6380.000	1.29	20.87	17.98	1.16	87.59	22.53
6440.000	1.28	21.63	18.32	1.16	76.85	22.36
6500.000	1.27	22.33	18.55	1.21	73.94	20.63
6560.000	1.23	22.85	19.57	1.21	86.07	20.41
6620.000	1.18	23.18	21.73	1.13	85.18	24.02
6680.000	1.13	23.33	24.21	1.09	75.61	27.77
6740.000	1.08	23.43	28.40	1.06	76.69	30.58
6800.000	1.03	23.52	36.29	1.07	74.75	29.07
6860.000	1.05	23.37	33.04	1.11	73.82	25.44
6920.000	1.11	23.17	25.50	1.17	80.07	22.21
6980.000	1.20	23.93	20.73	1.22	77.93	20.22
7040.000	1.26	22.91	18.64	1.18	78.38	21.80
7100.000	1.32	23.03	17.10	1.04	72.09	35.03
7160.000	1.40	23.59	15.62	1.14	80.35	23.89
7220.000	1.47	24.31	14.38	1.15	76.96	22.93
7280.000	1.55	24.91	13.34	1.16	76.55	22.85
7340.000	1.58	25.45	13.01	1.29	84.73	17.86
7400.000	1.60	25.93	12.68	1.20	93.83	21.03
7460.000	1.66	26.85	12.12	1.23	83.19	19.81
7520.000	1.70	28.35	11.72	1.60	75.60	12.77
7580.000	1.70	29.81	11.77	1.51	73.39	13.84
7640.000	1.65	31.87	12.20	1.40	78.25	15.60
7700.000	1.63	34.43	12.41	2.21	78.69	8.47
7760.000	1.63	35.89	12.40	2.87	73.11	6.32
7820.000	1.62	36.11	12.56	2.64	93.43	6.93
7880.000	1.52	35.72	13.53	1.06	80.34	10.44
7940.000	1.45	35.67	14.73	1.30	72.37	17.59
8000.000	1.42	35.86	15.15	1.20	73.67	26.10

REF PLANE ENT CM1: INPUT= .00 TRAN= .00 OUTPUT= .00
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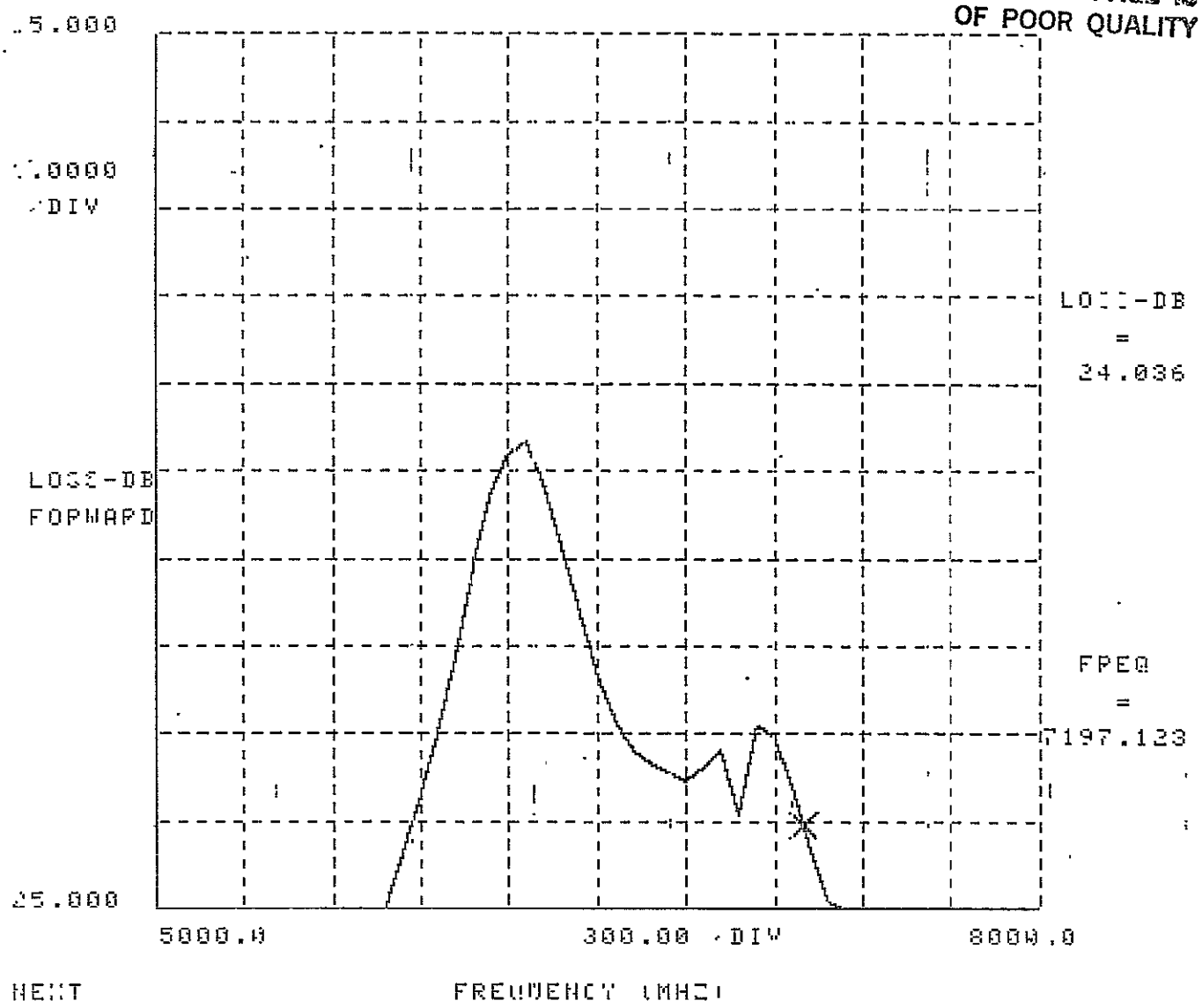
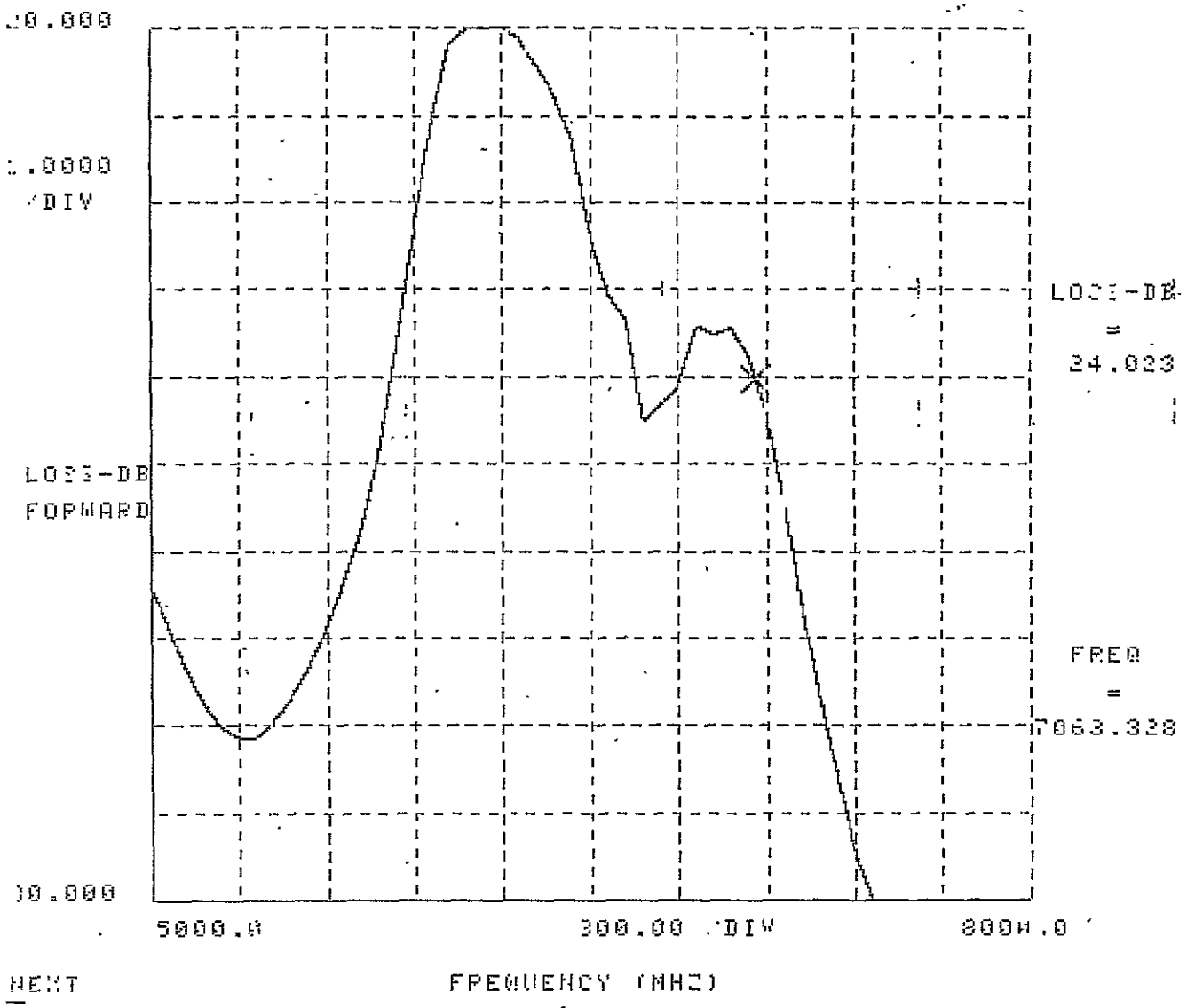


GPM4 G14001 7.18.78 0 13 SEP 82 15:09:05

SWITCH MATRIX POC MODEL TESTING
REFERENCE LAB NOTEBOOK 386-2 P43
13.1 DH NA3213::41

FREQ-MHZ	VSWR FORWARD	LOSS-DB FORWARD	RTN LOSS FORWARD	VSWR REVERSE	LOSS-DB REVERSE	RTN LOSS REVERSE
5000.000	1.10	26.43	26.45	1.03	85.82	36.14
5060.000	1.09	26.86	26.96	1.07	79.10	28.89
5120.000	1.07	27.37	29.62	1.13	86.40	24.15
5180.000	1.05	27.76	31.80	1.15	78.40	23.22
5240.000	1.06	28.02	31.39	1.10	83.07	26.83
5300.000	1.06	28.14	30.98	1.06	82.77	30.55
5360.000	1.07	28.13	29.60	1.10	75.12	26.74
5420.000	1.06	27.93	30.19	1.10	87.41	26.75
5480.000	1.04	27.69	34.94	1.06	83.90	30.04
5540.000	1.02	27.32	40.20	1.06	72.20	30.26
5600.000	1.02	26.89	41.62	1.03	77.32	37.15
5660.000	1.00	26.37	56.16	1.10	79.51	26.54
5720.000	1.03	25.72	37.97	1.23	77.64	19.63
5780.000	1.05	24.87	31.56	1.26	73.64	18.87
5840.000	1.07	23.63	29.65	1.14	76.97	23.67
5900.000	1.08	22.31	27.89	1.07	81.15	28.94
5960.000	1.10	21.11	26.19	1.13	77.80	24.02
6020.000	1.14	20.18	23.95	1.08	76.89	28.19
6080.000	1.15	19.65	23.04	1.18	75.70	21.77
6140.000	1.15	19.66	23.16	1.24	80.93	19.52
6200.000	1.17	19.82	21.92	1.11	78.39	25.96
6260.000	1.20	20.12	20.89	1.07	74.13	29.54
6320.000	1.20	20.44	20.76	1.12	78.89	25.03
6380.000	1.19	20.78	21.24	1.06	77.59	31.16
6440.000	1.19	21.31	21.41	1.10	72.72	26.51
6500.000	1.20	22.38	21.02	1.13	73.28	24.14
6560.000	1.17	23.05	21.89	1.16	76.05	22.50
6620.000	1.12	23.35	24.63	1.20	91.58	20.74
6680.000	1.11	24.50	25.47	1.16	75.81	22.52
6740.000	1.07	24.31	29.85	1.14	78.88	23.96
6800.000	1.02	24.11	38.34	1.26	73.26	18.80
6860.000	1.05	23.42	32.97	1.05	76.75	16.62
6920.000	1.10	23.51	26.56	1.00	76.51	17.62
6980.000	1.18	23.44	21.80	1.27	82.33	18.47
7040.000	1.25	23.77	19.18	1.25	79.85	19.03
7100.000	1.31	24.41	17.39	1.13	71.79	24.07
7160.000	1.39	25.40	15.72	1.00	74.56	17.72
7220.000	1.47	26.64	14.41	1.41	77.81	15.33
7280.000	1.56	27.65	13.17	1.34	79.24	16.72
7340.000	1.61	28.60	12.63	1.46	71.45	14.64
7400.000	1.65	29.46	12.22	1.42	91.33	15.13
7460.000	1.71	30.47	11.66	1.17	74.87	22.03
7520.000	1.76	32.27	11.20	1.39	75.90	15.79
7580.000	1.76	34.16	11.18	1.29	76.12	18.05
7640.000	1.72	36.90	11.56	1.55	91.00	13.29
7700.000	1.69	40.08	11.81	2.44	78.46	7.56
7760.000	1.69	41.05	11.85	2.92	70.99	6.20
7820.000	1.66	40.12	12.06	2.60	77.11	7.03
7880.000	1.56	38.52	13.18	1.82	80.56	10.72
7940.000	1.45	37.35	14.67	1.25	85.93	19.16
8000.000	1.42	36.88	15.22	1.09	82.13	27.72

REF PLANE ENT (M): INPUT= .00 TRAN= .00 OUTPUT= .00
NFAIL(1)= 4



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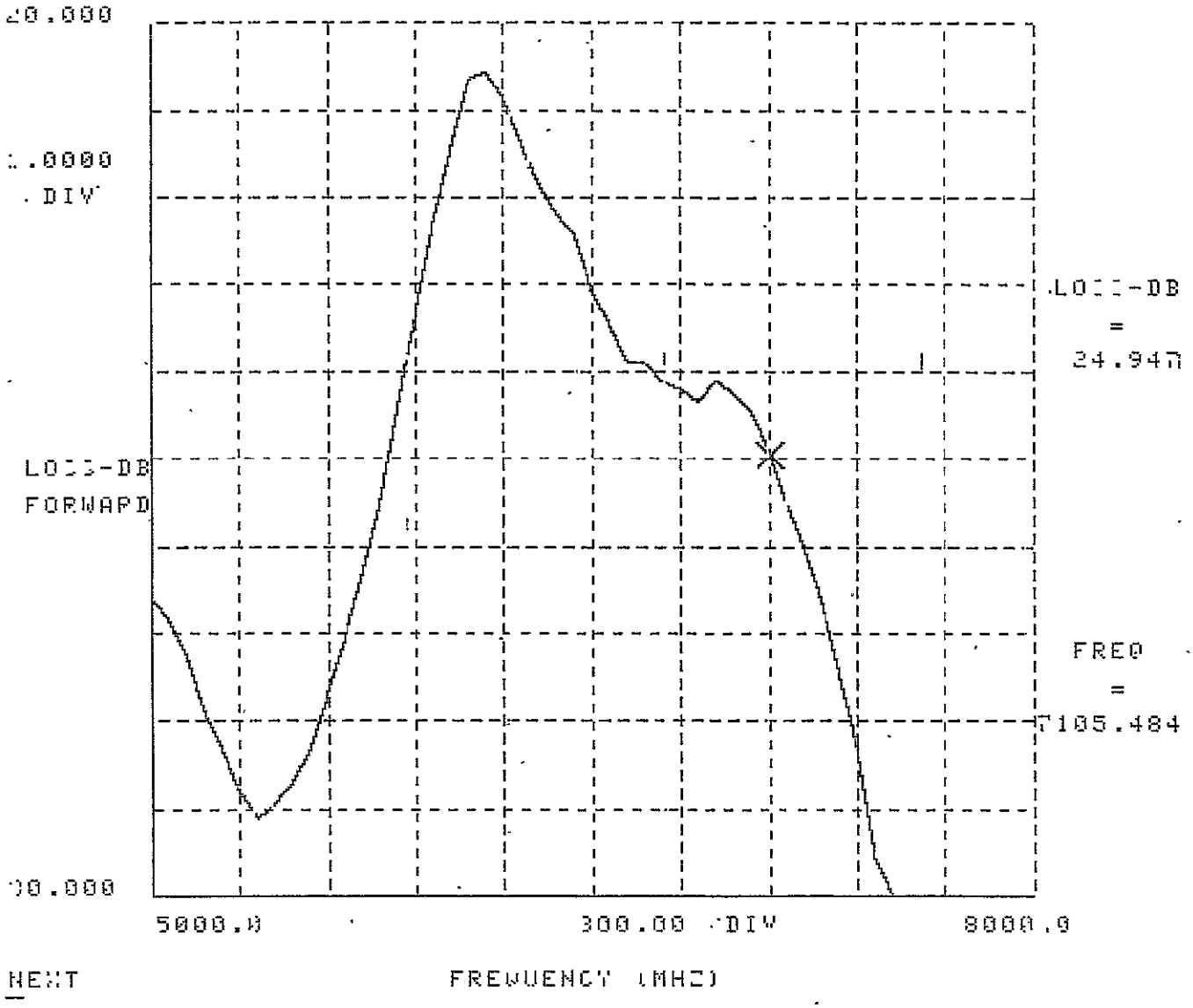
OF POOR QUALITY

GPM4 G14001 7/18/78 0 13 SEP 82 15:05:28

SWITCH MATRIX POC MODEL TESTING
REFERENCE LWD NOTEBOOK 386-2 P43
13,2 DN MAR212::41

FREQ-MHZ	VSWR FORWARD	LOSS-DB FORWARD	RTN LOSS FORWARD	VSWR REVERSE	LOSS-DB REVERSE	RTN LOSS REVERSE
5000.000	1.11	26.61	25.50	1.04	80.83	33.31
5060.000	1.11	26.83	25.65	1.04	86.68	33.38
5120.000	1.08	27.26	28.22	1.06	79.55	31.39
5180.000	1.06	27.90	30.27	1.10	77.52	26.23
5240.000	1.07	28.32	29.69	1.06	83.91	22.72
5300.000	1.08	28.80	28.11	1.05	78.72	23.35
5360.000	1.10	29.10	26.65	1.07	72.73	29.24
5420.000	1.09	28.94	27.27	1.08	81.66	28.59
5480.000	1.07	28.70	29.79	1.05	75.55	23.14
5540.000	1.06	28.30	30.72	1.03	71.59	24.35
5600.000	1.06	27.69	30.92	1.05	74.86	32.14
5660.000	1.05	27.05	32.71	1.07	77.11	29.17
5720.000	1.03	26.30	37.12	1.08	75.37	28.23
5780.000	1.03	25.49	37.56	1.03	74.81	36.36
5840.000	1.05	24.40	32.93	1.08	82.24	27.95
5900.000	1.07	23.34	29.07	1.28	83.03	18.09
5960.000	1.11	22.32	25.61	1.48	76.38	14.29
6020.000	1.15	21.44	22.90	1.44	77.00	14.91
6080.000	1.18	20.63	21.49	1.20	74.80	20.91
6140.000	1.20	20.56	20.84	1.18	78.07	21.59
6200.000	1.24	20.87	19.27	1.22	80.96	20.08
6260.000	1.28	21.38	18.34	1.07	80.12	29.08
6320.000	1.28	21.85	18.17	1.12	77.58	24.69
6380.000	1.27	22.20	18.51	1.17	98.96	22.22
6440.000	1.26	22.43	18.84	1.16	77.98	22.86
6500.000	1.25	23.09	18.94	1.20	76.02	21.02
6560.000	1.22	23.45	19.96	1.21	75.97	20.38
6620.000	1.17	23.91	22.10	1.14	90.12	23.50
6680.000	1.12	23.90	24.80	1.10	72.39	26.84
6740.000	1.07	24.13	29.65	1.07	82.24	29.63
6800.000	1.04	24.19	34.16	1.07	72.31	29.22
6860.000	1.08	24.35	28.24	1.11	72.25	26.01
6920.000	1.15	24.10	23.25	1.17	76.78	22.28
6980.000	1.23	24.24	19.62	1.22	77.73	20.02
7040.000	1.31	24.45	17.44	1.18	84.37	21.50
7100.000	1.38	24.89	15.90	1.24	73.98	33.83
7160.000	1.46	25.49	14.58	1.14	72.49	23.83
7220.000	1.53	26.00	13.53	1.16	80.07	22.75
7280.000	1.62	26.66	12.55	1.16	76.13	22.82
7340.000	1.66	27.46	12.13	1.29	71.88	17.96
7400.000	1.68	28.32	11.87	1.19	77.34	21.14
7460.000	1.73	29.56	11.43	1.23	84.36	19.71
7520.000	1.78	31.35	11.04	1.60	69.64	12.76
7580.000	1.78	32.80	11.06	1.51	74.23	13.84
7640.000	1.73	34.70	11.48	1.40	79.24	15.63
7700.000	1.69	37.00	11.77	2.21	87.89	8.46
7760.000	1.69	37.87	11.78	2.07	73.32	6.31
7820.000	1.67	37.51	11.98	2.64	80.77	6.92
7880.000	1.57	36.55	13.04	1.06	79.35	10.43
7940.000	1.47	35.80	14.46	1.30	71.55	17.50
8000.000	1.43	35.16	15.00	1.10	74.37	26.11

REF PLANE EXT(M): INPUT= .00 TRAN= .00 OUTPUT= .00
NFAIL(1)= 4



GPM4 G14001 T<1.8/78 0 :3 SEP 82 15:42:41

SWITCH MATRIX POC MODEL TESTING
REFERENCE LAB NOTEBOOK 386-2 P43
14,1 WH HA3214::41

FREQ-MHZ	VSWR FORWARD	LOSS-DB RTN LOSS FORWARD	VSWR REVERSE	LOSS-DB RTN LOSS REVERSE
5000.000	1.10	26.17	1.03	31.09	35.96
5060.000	1.12	26.12	24.68	1.08	32.86	28.64
5120.000	1.18	26.13	21.64	1.13	35.12	24.08
5180.000	1.20	26.39	20.80	1.15	31.38	23.24
5240.000	1.25	26.70	19.11	1.19	76.54	26.97
5300.000	1.26	26.97	18.91	1.16	76.12	30.80
5360.000	1.26	27.16	18.86	1.10	74.50	26.63
5420.000	1.30	27.17	17.63	1.10	35.45	26.51
5480.000	1.32	26.97	17.22	1.07	78.93	29.89
5540.000	1.31	26.64	17.37	1.06	73.99	30.61
5600.000	1.31	26.19	17.48	1.03	79.22	38.12
5660.000	1.31	25.66	17.35	1.10	89.54	26.57
5720.000	1.32	25.18	17.15	1.23	77.56	19.72
5780.000	1.33	24.53	16.99	1.25	74.89	18.99
5840.000	1.31	23.89	17.41	1.13	75.41	23.99
5900.000	1.29	23.13	17.87	1.08	79.64	28.53
5960.000	1.27	22.36	18.58	1.14	80.66	23.69
6020.000	1.25	21.53	19.02	1.08	74.13	28.60
6080.000	1.22	20.83	20.07	1.17	77.13	21.99
6140.000	1.17	20.42	21.89	1.24	76.81	19.45
6200.000	1.12	20.11	24.79	1.11	75.61	25.37
6260.000	1.08	20.16	28.35	1.06	81.34	30.73
6320.000	1.08	20.55	28.79	1.11	81.60	25.53
6380.000	1.10	21.09	26.57	1.07	81.84	29.80
6440.000	1.14	21.84	23.62	1.10	76.10	26.74
6500.000	1.16	22.84	22.37	1.12	76.50	24.64
6560.000	1.19	23.27	21.21	1.17	79.99	22.31
6620.000	1.22	23.15	20.00	1.21	77.44	20.47
6680.000	1.23	24.38	19.79	1.16	76.65	22.59
6740.000	1.23	24.07	19.71	1.13	78.02	24.25
6800.000	1.21	23.53	20.54	1.26	71.11	18.73
6860.000	1.19	22.72	21.05	1.35	76.72	16.50
6920.000	1.15	22.72	23.30	1.30	73.76	17.68
6980.000	1.13	22.56	24.46	1.26	83.53	18.64
7040.000	1.12	22.64	24.87	1.25	82.92	18.93
7100.000	1.14	22.98	23.67	1.14	72.15	23.88
7160.000	1.20	23.43	20.64	1.29	70.61	17.86
7220.000	1.29	24.25	18.02	1.41	77.78	15.36
7280.000	1.37	24.98	16.09	1.35	80.94	16.64
7340.000	1.43	25.91	14.97	1.46	74.54	14.59
7400.000	1.52	26.95	13.73	1.42	86.21	15.18
7460.000	1.62	28.27	12.55	1.17	77.90	22.05
7520.000	1.68	30.15	11.93	1.09	73.74	15.76
7580.000	**1.70**	**31.93**	**11.76**	**1.29**	**72.52**	**18.03**
7640.000	1.68	34.40	11.87	1.55	78.01	13.32
7700.000	1.71	37.36	11.65	2.44	88.20	7.57
7760.000	1.71	38.81	11.60	2.91	75.69	6.32
7820.000	1.69	38.87	11.86	2.60	82.05	7.05
7880.000	1.65	37.14	12.60	1.82	70.39	10.74
7940.000	1.54	38.26	13.50	1.55	72.44	19.12
8000.000	1.56	38.68	13.23	1.49	74.59	27.55

REF PLANE ENT CM1: INPUT= .00 TRAN= .00 OUTPUT= .00
NPAIL(1)= 4

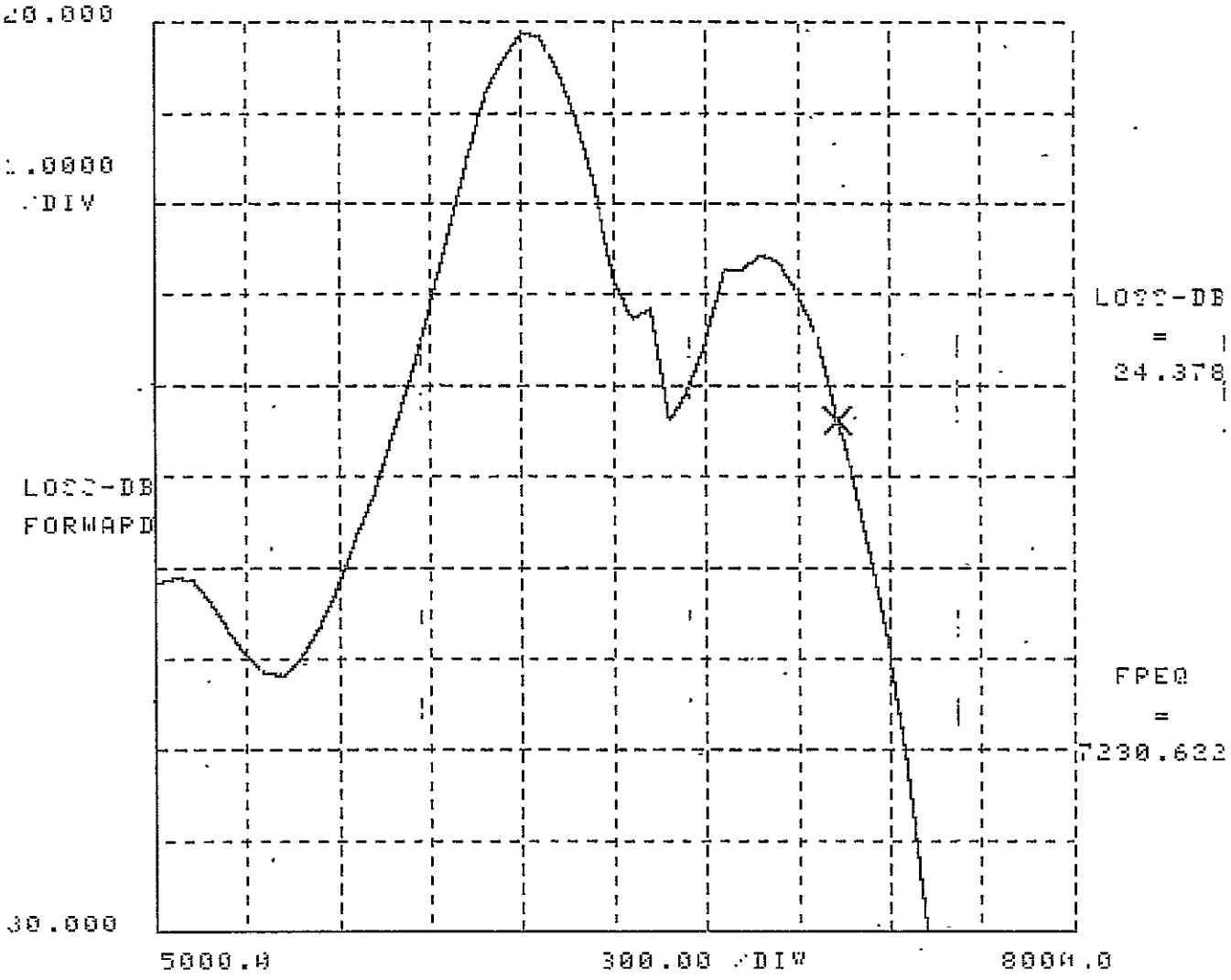
GPM4 614001 7/18/78 0 13 SEP 82 15:41:57

SWITCH MATRIX POC MODEL TESTING

REFERENCE LWD NOTEBOOK 38m-2 P43

14,1 MN MAS214::41m

ORIGINAL PAGE IS
OF POOR QUALITY



NEXT

SWITCH MATRIX POC MODEL TESTING
REFERENCE LMD NOTEBOOK 386-2 P43
14,2 UN NA3215::41

FREQ-MHZ	VSWR FORWARD	LOSS-DB FORWARD	RTN LOSS FORWARD	VSWR REVERSE	LOSS-DB REVERSE	RTN LOSS REVERSE
5000.000	1.07	26.26	29.77	1.04	83.52	33.62
5060.000	1.09	26.48	27.38	1.04	84.61	33.71
5120.000	1.14	26.95	23.65	1.06	83.50	31.34
5180.000	1.16	27.37	22.61	1.10	78.09	26.13
5240.000	1.20	27.83	20.95	1.16	76.63	22.71
5300.000	1.20	28.36	20.77	1.15	76.77	23.38
5360.000	1.20	28.79	20.72	1.07	74.23	29.49
5420.000	1.25	28.90	19.19	1.08	81.02	28.54
5480.000	1.26	29.09	18.64	1.15	76.77	22.97
5540.000	1.26	29.04	18.85	1.13	72.48	24.15
5600.000	1.25	28.57	19.04	1.05	82.26	31.74
5660.000	1.26	28.02	18.66	1.07	76.24	28.89
5720.000	1.28	27.25	18.30	1.08	77.41	27.86
5780.000	1.28	26.37	18.12	1.03	75.68	35.36
5840.000	1.27	25.38	18.59	1.08	75.63	27.91
5900.000	1.25	24.48	19.08	1.29	92.83	18.00
5960.000	1.23	23.57	19.62	1.48	79.01	14.21
6020.000	1.23	22.58	19.86	1.44	73.85	14.82
6080.000	1.20	21.51	20.88	1.20	73.54	20.89
6140.000	1.15	20.76	22.98	1.18	82.90	21.88
6200.000	1.11	20.28	25.38	1.23	74.91	19.83
6260.000	1.08	20.08	28.39	1.08	83.24	27.95
6320.000	1.05	20.26	31.99	1.11	84.12	25.34
6380.000	1.02	20.75	38.30	1.17	76.85	22.24
6440.000	1.06	21.44	31.37	1.16	81.61	22.36
6500.000	1.08	22.39	28.20	1.20	83.19	20.90
6560.000	1.10	23.00	26.18	1.21	78.79	20.61
6620.000	1.13	23.33	24.47	1.13	75.02	24.02
6680.000	1.15	23.51	23.08	1.09	74.09	27.48
6740.000	1.16	23.38	22.48	1.07	73.89	29.72
6800.000	1.15	23.22	23.01	1.08	73.22	28.48
6860.000	1.15	23.28	22.89	1.11	72.51	25.89
6920.000	1.15	23.03	22.96	1.16	74.73	22.56
6980.000	1.17	23.15	22.10	1.22	80.55	20.16
7040.000	1.19	23.26	21.28	1.18	89.68	21.48
7100.000	1.22	23.49	20.24	1.04	77.40	33.92
7160.000	1.27	23.80	18.56	1.14	74.09	23.95
7220.000	1.33	24.12	17.04	1.16	78.84	22.76
7280.000	1.39	24.90	15.73	1.16	76.81	22.77
7340.000	1.43	26.00	14.97	1.29	76.74	17.93
7400.000	1.50	27.37	13.96	1.19	83.16	21.11
7460.000	1.59	29.08	12.88	1.23	88.85	19.72
7520.000	1.65	31.25	12.24	1.40	76.61	12.74
7580.000	**1.66**	**32.89**	**12.09**	**1.51**	**73.17**	**13.82**
7640.000	1.65	34.71	12.16	1.40	73.59	15.64
7700.000	1.68	36.98	11.91	2.21	84.55	8.47
7760.000	1.69	38.21	11.80	2.07	74.99	6.32
7820.000	**1.67**	**38.32**	**11.99**	**2.64**	**96.75**	**6.92**
7880.000	1.60	37.89	12.79	1.06	83.48	10.43
7940.000	1.53	37.71	13.60	1.30	76.18	17.59
8000.000	1.56	37.33	13.26	1.10	79.64	26.16

REF PLANE EXT(CM): INPUT= .00 TRAN= .00 OUTPUT= .00
NPAIL(1)= 4

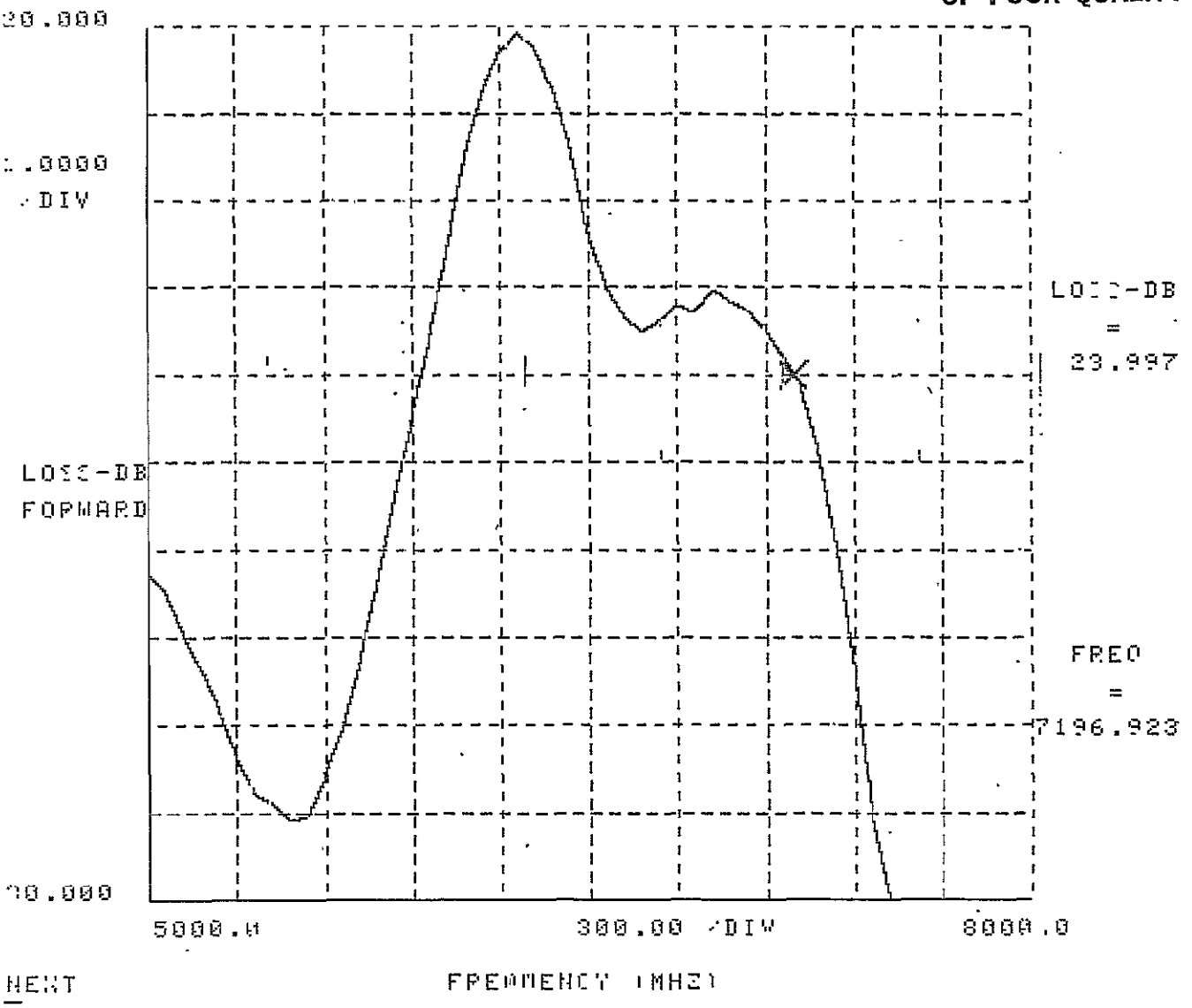
GPM4 G14001 T.^.8/78 0 :3 SEP 82 15:45:54

SWITCH MATRIX POC MODEL TESTING

REFERENCE LWD NOTEBOOK 38#-2 P43

14.2 ON NAC215::41▲

ORIGINAL PAGE IS
OF POOR QUALITY



GPM4 G14001 7[illegible]78 0 13 SEP 82 15:54:05

SWITCH MATRIX POC MODEL TESTING

REFERENCE LMR NOTEBOOK 386-2 P43

16,1 DN NAS217::41

ORIGINAL PAGE IS OF POOR QUALITY

FREQ-MHZ	VSWR FORWARD	LOSS-DB FORWARD	RTN LOSS FORWARD	VSWR REVERSE	LOSS-DB REVERSE	RTN LOSS REVERSE
5000.000	1.10	27.19	26.17	1.03	88.95	35.60
5060.000	1.07	26.63	29.66	1.08	80.02	28.62
5120.000	1.00	26.43	66.70	1.13	77.57	24.20
5180.000	1.03	26.52	35.45	1.15	88.76	23.33
5240.000	1.08	26.72	28.54	1.10	82.25	26.80
5300.000	1.09	26.92	27.57	1.06	77.60	30.53
5360.000	1.09	27.08	27.20	1.10	74.73	26.79
5420.000	1.14	27.07	23.78	1.10	83.12	26.68
5480.000	1.16	27.06	22.63	1.07	83.14	29.87
5540.000	1.16	26.84	22.83	1.06	72.35	30.25
5600.000	1.15	26.59	23.11	1.03	74.48	37.48
5660.000	1.17	26.25	21.93	1.10	85.19	26.50
5720.000	1.19	25.83	21.18	1.23	79.97	19.63
5780.000	1.19	25.32	21.11	1.26	73.74	18.89
5840.000	1.19	24.71	21.28	1.14	79.30	23.81
5900.000	1.19	23.90	21.43	1.08	80.94	28.55
5960.000	1.19	23.09	21.29	1.14	79.66	23.79
6020.000	1.19	22.18	21.27	1.08	78.24	28.39
6080.000	1.17	21.41	22.29	1.18	78.53	21.82
6140.000	1.14	20.70	23.89	1.24	76.28	19.40
6200.000	1.14	20.09	23.67	1.11	74.37	25.52
6260.000	1.13	19.81	23.98	1.06	79.31	30.23
6320.000	1.11	19.91	26.02	1.12	76.89	25.13
6380.000	1.08	20.26	28.56	1.06	78.44	30.30
6440.000	1.08	20.90	28.52	1.10	76.42	26.68
6500.000	1.08	21.73	28.74	1.13	80.80	24.27
6560.000	1.06	22.36	31.45	1.16	79.68	22.41
6620.000	1.02	22.88	38.53	1.21	79.50	20.61
6680.000	1.03	23.07	36.25	1.17	75.58	22.27
6740.000	1.03	23.70	35.78	1.13	89.98	24.25
6800.000	1.05	23.63	31.96	1.26	78.14	18.93
6860.000	1.10	23.14	26.27	1.36	71.31	16.41
6920.000	1.13	23.20	24.15	1.31	75.73	17.42
6980.000	1.19	22.75	21.14	1.26	76.97	18.76
7040.000	1.24	22.20	19.36	1.25	78.39	19.13
7100.000	1.29	21.71	17.88	1.15	74.34	23.33
7160.000	1.36	21.45	16.36	1.29	68.82	17.94
7220.000	1.41	21.96	15.39	1.40	74.61	15.51
7280.000	1.45	22.47	14.73	1.35	78.47	16.47
7340.000	1.46	23.45	14.49	1.47	70.89	14.45
7400.000	1.50	24.57	13.98	1.42	78.48	15.20
7460.000	1.54	26.08	13.40	1.17	76.73	22.19
7520.000	1.55	28.03	13.28	1.40	75.45	15.56
7580.000	1.52	29.86	13.65	1.29	70.07	17.95
7640.000	1.49	32.03	14.17	1.55	74.50	13.28
7700.000	1.48	34.89	14.33	2.46	78.74	7.50
7760.000	1.45	36.29	14.76	2.94	69.49	6.16
7820.000	1.40	36.08	15.57	2.61	86.06	7.01
7880.000	1.32	35.13	17.11	1.02	86.46	10.74
7940.000	1.26	34.67	18.84	1.25	78.10	19.20
8000.000	1.26	34.59	18.79	1.19	72.72	27.69

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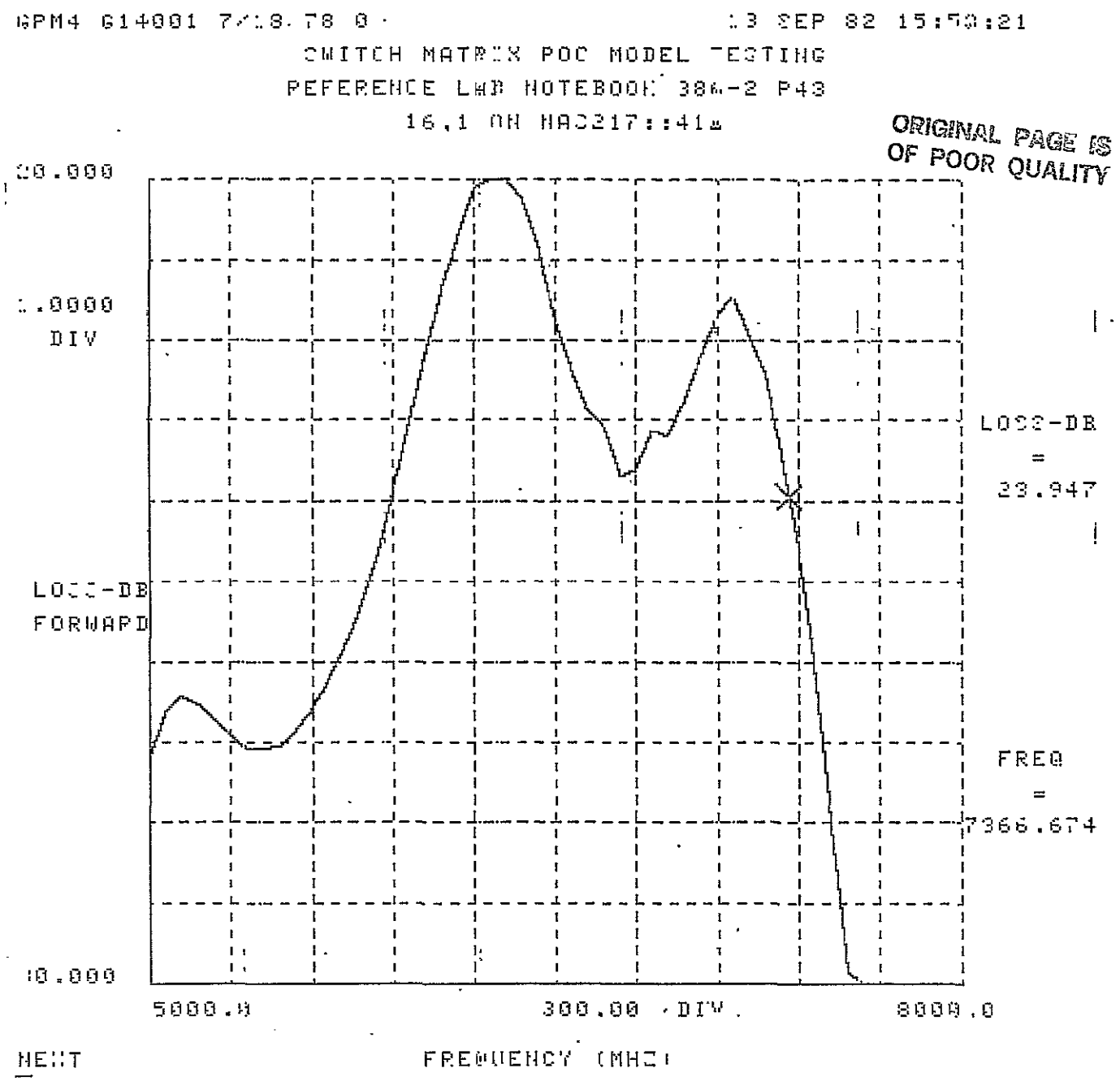
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13 SEP 82 15:50:21
SWITCH MATRIX POC MODEL TESTING
REFERENCE LAB NOTEBOOK 384-2 P43
16.1 OH HAC217::41
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20.000
1.0000
DIV
LOSS-DB
FORWARD
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LOSS-DB
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23.947
FREQ
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7366.674
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300.00 /DIV
8000.0
NEXT
FREQUENCY (MHZ)

GPM4 G14001 T'.8/T8 0 :9 SEP 82 15:5M:27
SWITCH MATRIX POC MODEL TESTING
REFERENCE LAB NOTEBOOK 386-2 P43
16,2 ON HA3216::41

FREQ-MHZ	VSWR FORWARD	LOSS-DB FORWARD	RTN LOSS FORWARD	VSWR REVERSE	LOSS-DB REVERSE	RTN LOSS REVERSE
5000.000	1.12	25.87	25.22	1.04	77.80	33.55
5060.000	1.08	25.76	28.13	1.04	83.35	33.62
5120.000	1.03	26.13	37.77	1.06	81.75	31.45
5180.000	1.03	26.46	35.58	1.10	83.28	26.17
5240.000	1.05	27.15	31.66	1.16	78.09	22.73
5300.000	1.06	27.79	31.09	1.15	75.85	23.37
5360.000	1.06	28.35	30.87	1.07	75.10	29.44
5420.000	1.10	28.70	26.36	1.08	95.72	28.53
5480.000	1.12	28.82	24.84	1.15	77.11	22.99
5540.000	1.12	28.71	24.72	1.13	74.00	24.21
5600.000	1.12	28.46	24.68	1.05	75.55	31.79
5660.000	1.15	28.11	22.99	1.07	76.03	28.88
5720.000	1.17	27.55	21.99	1.08	79.33	27.81
5780.000	1.18	26.88	21.67	1.03	76.79	35.52
5840.000	1.19	26.14	21.39	1.08	81.66	27.83
5900.000	1.19	25.42	21.30	1.29	86.18	17.99
5960.000	1.20	24.70	20.86	1.48	81.46	14.22
6020.000	1.21	23.71	20.61	1.44	75.08	14.89
6080.000	1.19	22.48	21.12	1.20	77.45	20.90
6140.000	1.17	21.63	22.02	1.18	73.10	21.74
6200.000	1.18	21.03	21.51	1.22	73.44	19.94
6260.000	1.19	20.68	21.44	1.08	75.19	28.41
6320.000	1.16	20.75	22.62	1.12	90.83	25.01
6380.000	1.13	20.90	24.25	1.17	79.84	22.26
6440.000	1.12	21.49	25.07	1.16	76.62	22.69
6500.000	1.11	22.27	25.66	1.20	71.49	20.88
6560.000	1.08	23.04	27.95	1.21	85.88	20.37
6620.000	1.04	23.65	33.73	1.14	80.43	23.67
6680.000	1.02	24.05	40.78	1.09	75.50	27.26
6740.000	1.03	24.12	35.64	1.06	85.83	30.34
6800.000	1.07	24.18	28.86	1.07	69.78	29.17
6860.000	1.13	24.11	24.46	1.11	73.89	25.47
6920.000	1.18	23.70	21.62	1.17	78.84	22.26
6980.000	1.24	23.40	19.46	1.21	80.99	20.31
7040.000	1.28	23.04	18.11	1.18	78.97	21.83
7100.000	.33	22.96	16.98	1.83	73.62	35.33
7160.000	1.39	23.11	15.70	1.13	69.45	24.33
7220.000	1.44	23.19	14.89	1.15	78.83	23.08
7280.000	1.47	23.93	14.36	1.16	77.77	22.46
7340.000	1.48	25.02	14.25	1.29	72.64	17.89
7400.000	1.51	26.14	13.82	1.19	84.22	21.28
7460.000	1.55	27.70	13.29	1.23	78.48	19.59
7520.000	1.56	29.46	13.18	1.60	72.06	12.71
7580.000	1.53	30.81	13.56	1.51	70.80	13.83
7640.000	1.49	32.18	14.06	1.40	77.40	15.63
7700.000	1.49	34.35	14.17	2.22	86.67	8.44
7760.000	1.46	35.79	14.53	2.08	74.53	6.29
7820.000	1.42	36.13	15.24	2.64	74.94	6.92
7880.000	1.35	36.21	16.64	1.06	79.68	10.45
7940.000	1.28	36.48	18.16	1.30	75.14	17.59
8000.000	1.28	36.53	18.08	1.10	78.88	26.06

REF PLANE ENTERED: INPUT= .00 TRAN= .00 OUTPUT= .00
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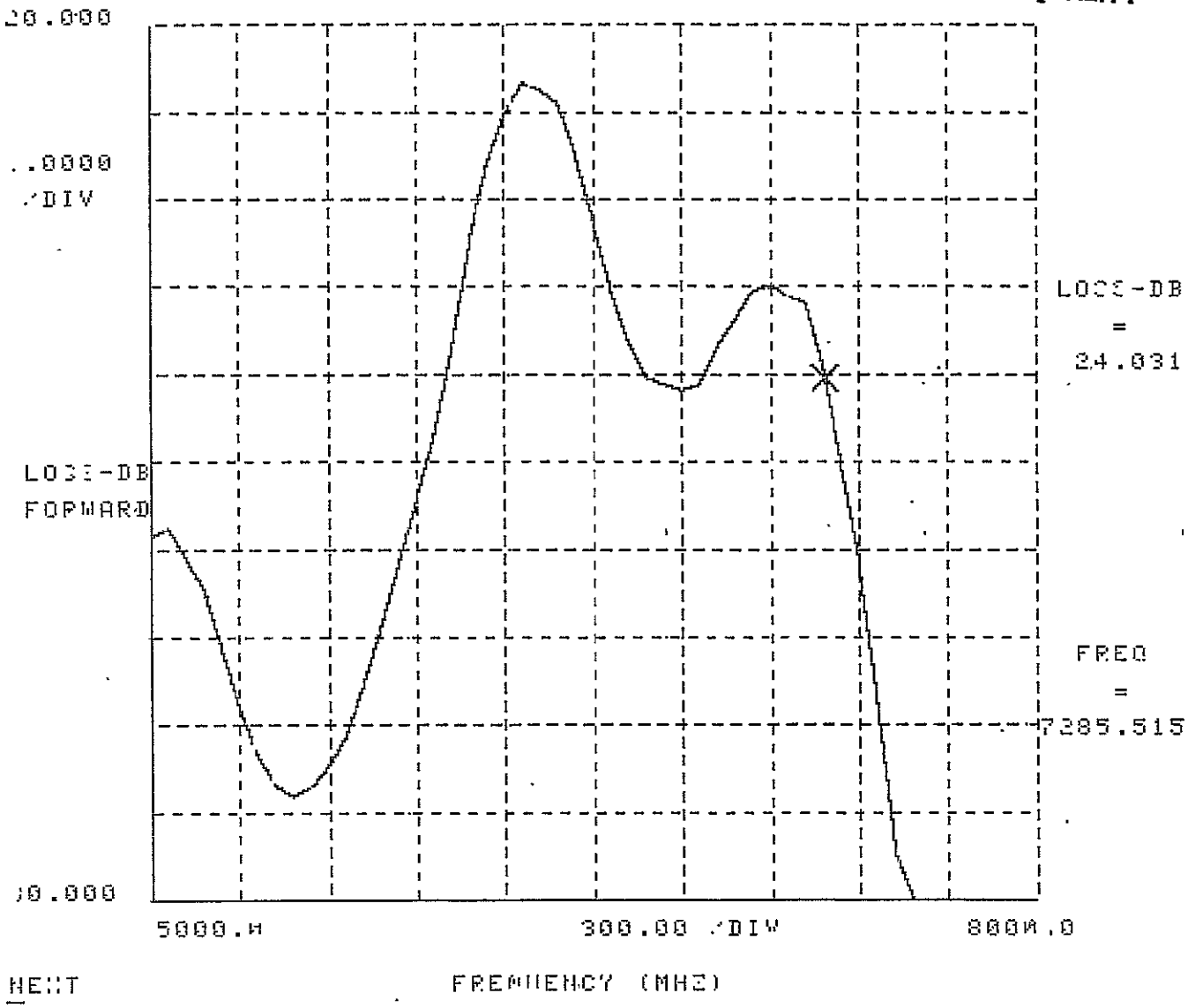

GPM4 614001 7.18.78 0 13 SEP 82 15:57:42

SWITCH MATRIX POC MODEL TESTING
REFERENCE LWD NOTEBOOK 386-2 P43
17,1 UN NAS218::41

FREQ-MHZ	VSWR FORWARD	LOSS-DB FORWARD	RTN LOSS FORWARD	VSWR REVERSE	LOSS-DB REVERSE	RTN LOSS REVERSE
5000.000	1.27	25.54	18.44	1.43	85.41	35.98
5060.000	1.21	25.55	20.60	1.08	84.84	28.63
5120.000	1.13	25.79	24.24	1.13	94.12	24.10
5180.000	1.11	26.18	25.85	1.15	85.50	23.22
5240.000	1.11	26.57	25.47	1.10	86.51	26.85
5300.000	1.11	27.04	25.81	1.06	77.97	30.67
5360.000	1.10	27.43	26.10	1.10	75.79	26.70
5420.000	1.14	27.74	23.68	1.10	81.70	26.63
5480.000	1.17	27.81	22.07	1.06	80.63	30.15
5540.000	1.18	27.75	21.69	1.06	71.25	30.55
5600.000	1.19	27.61	21.40	1.03	76.58	37.68
5660.000	1.23	27.33	19.74	1.10	85.34	26.75
5720.000	1.26	26.82	18.74	1.23	79.90	19.76
5780.000	1.28	26.11	18.34	1.26	74.02	18.93
5840.000	1.30	25.16	17.68	1.14	77.66	23.61
5900.000	1.32	24.24	17.30	1.07	81.26	28.91
5960.000	1.34	23.24	16.79	1.13	79.15	24.05
6020.000	1.35	22.33	16.50	1.09	75.30	27.77
6080.000	1.34	21.60	16.75	1.17	75.67	21.91
6140.000	1.33	21.03	17.09	1.23	74.91	19.66
6200.000	1.33	20.77	16.87	1.11	77.49	25.71
6260.000	1.32	20.88	17.25	1.06	77.32	30.25
6320.000	1.26	21.32	18.64	1.11	80.20	25.70
6380.000	1.22	21.90	19.92	1.07	82.61	29.60
6440.000	1.20	22.66	20.72	1.10	80.04	26.62
6500.000	1.16	23.54	22.39	1.12	75.36	24.68
6560.000	1.12	24.00	24.85	1.17	86.88	22.22
6620.000	1.11	24.31	25.67	1.21	76.93	20.43
6680.000	1.15	24.26	22.97	1.16	74.35	22.64
6740.000	1.19	24.90	21.29	1.13	80.75	24.15
6800.000	1.25	24.30	19.10	1.26	74.89	18.79
6860.000	1.32	23.65	17.09	1.35	74.55	16.58
6920.000	1.39	23.85	15.82	1.30	73.56	17.61
6980.000	1.48	23.41	14.33	1.27	73.66	18.59
7040.000	1.54	23.29	13.48	1.25	79.02	19.15
7100.000	1.59	23.46	12.90	1.24	75.24	23.60
7160.000	1.64	24.02	12.29	1.29	68.44	17.89
7220.000	1.68	25.21	11.94	1.40	73.83	15.52
7280.000	1.71	26.43	11.60	1.45	77.16	16.55
7340.000	1.70	27.91	11.77	1.47	72.53	14.48
7400.000	1.67	29.31	11.99	1.42	86.44	15.19
7460.000	1.66	30.69	12.09	1.17	79.37	22.22
7520.000	1.63	32.26	12.45	1.40	73.86	15.58
7580.000	1.54	33.54	13.44	1.29	73.50	17.98
7640.000	1.44	35.44	14.80	1.55	82.31	13.30
7700.000	1.38	38.00	16.00	2.45	88.38	7.52
7760.000	1.32	39.17	17.16	2.93	76.74	6.18
7820.000	1.29	39.06	17.98	2.60	94.57	7.03
7880.000	1.25	38.22	19.11	1.82	75.47	10.75
7940.000	1.24	37.71	19.28	1.25	76.73	19.18
8000.000	1.29	37.61	18.07	1.49	78.22	27.73

REF PLANE ENTERED: INPUT= .00 TRAN= .00 OUTPUT= .00
NPAIL(1)= 4

C3

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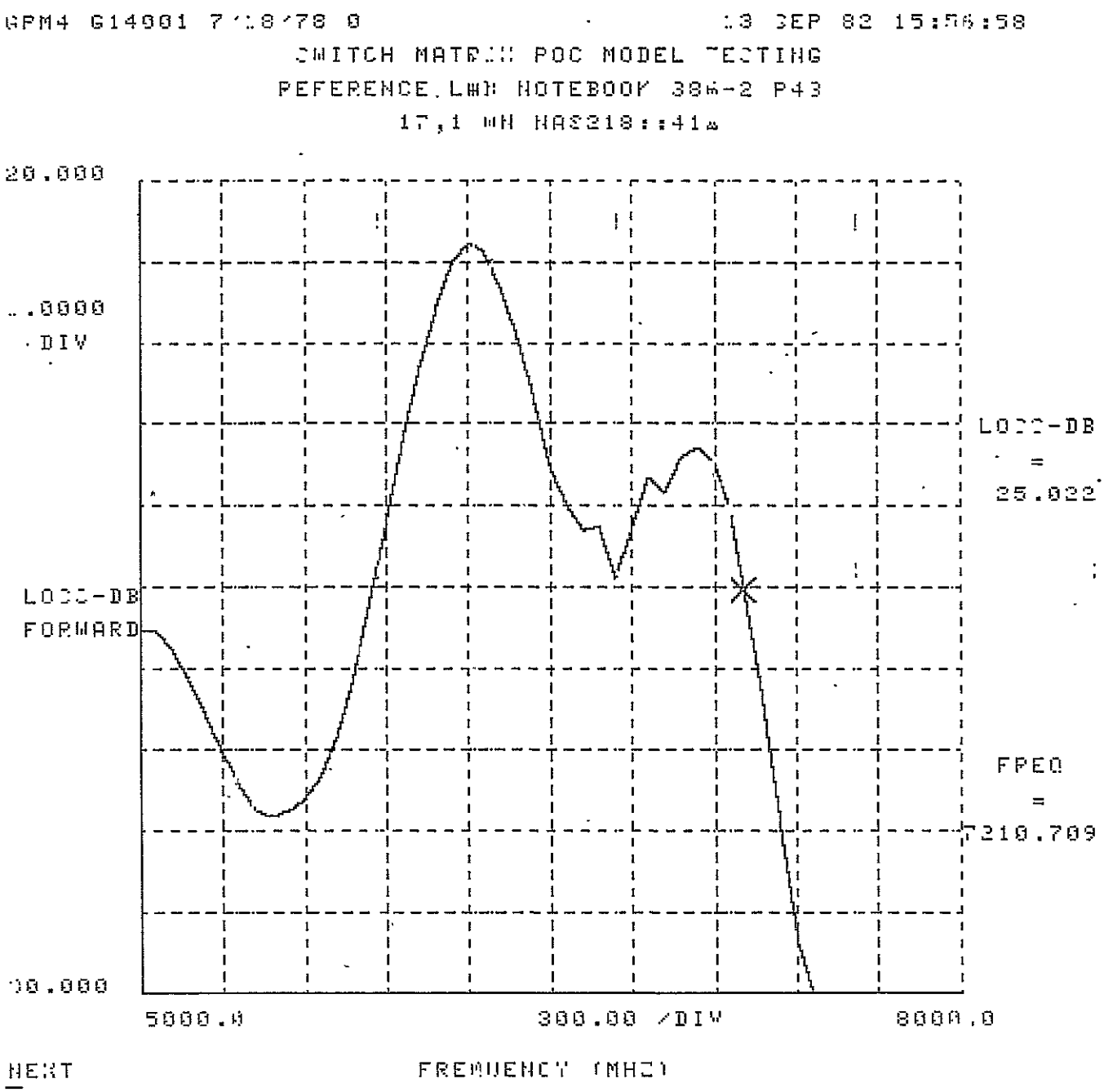
OF POOR QUALITY



GPM4 G14001 7.:8.78 0 .3 SEP 82 16:0::02

SWITCH MATRIX POC MODEL TESTING
REFERENCE LAB NOTEBOOK 386-2 P43
17,2 UH HA2219::41

FREQ-MHZ	VSWR FORWARD	LOSS-DB FORWARD	RTN LOSS FORWARD	VSWR REVERSE	LOSS-DB REVERSE	RTN LOSS REVERSE
5000.000	1.31	23.60	17.38	1..2	81.49	24.64
5060.000	1.26	23.62	18.83	1.:2	79.35	24.91
5120.000	1.18	23.92	21.67	1.:3	78.84	24.05
5180.000	1.14	24.32	23.62	1.:6	81.06	22.83
5240.000	1.11	25.15	25.90	1.:3	82.50	24.43
5300.000	1.07	25.90	29.40	1.05	75.77	32.84
5360.000	1.04	26.48	33.37	1.04	75.94	34.12
5420.000	1.09	26.85	26.98	1.05	83.23	33.13
5480.000	1.14	27.25	23.70	1.05	76.24	32.15
5540.000	1.17	27.42	22.27	1.:2	71.73	24.83
5600.000	1.19	27.32	21.19	1.:4	72.10	23.73
5660.000	1.25	27.04	18.94	1.08	79.11	28.77
5720.000	1.30	26.69	17.76	1.01	75.78	45.08
5780.000	1.32	26.03	17.28	1.08	78.02	28.53
5840.000	1.35	25.23	16.55	1.:5	75.16	23.01
5900.000	1.37	24.41	16.08	1.26	82.64	18.84
5960.000	1.40	23.46	15.52	1.33	77.51	16.93
6020.000	1.42	22.45	15.25	1.30	76.96	17.80
6080.000	1.40	21.35	15.49	1.:5	72.07	23.26
6140.000	1.39	20.84	15.75	1.08	80.28	28.49
6200.000	1.40	20.62	15.63	1.:5	77.08	22.94
6260.000	1.37	20.67	16.08	1.:0	77.42	26.67
6320.000	1.31	21.17	17.50	1.02	82.90	42.06
6380.000	1.25	21.75	19.03	1.08	82.41	28.58
6440.000	1.21	22.51	20.41	1.:0	90.45	26.82
6500.000	1.16	23.40	22.60	1.:4	72.98	23.50
6560.000	1.09	24.00	26.99	1.21	82.36	20.34
6620.000	1.06	24.43	31.26	1.21	78.77	20.58
6680.000	1.10	24.41	26.19	1.:8	73.72	21.81
6740.000	1.17	24.52	22.08	1.:3	78.81	24.25
6800.000	1.25	24.23	19.18	1..1	70.57	25.60
6860.000	1.34	23.83	16.80	1..2	74.90	24.66
6920.000	1.43	23.26	15.05	1.:4	76.47	23.76
6980.000	1.53	22.99	13.59	1.:3	76.73	24.47
7040.000	1.60	22.83	12.71	1.08	77.36	27.89
7100.000	1.66	23.26	12.11	1.:1	80.11	25.92
7160.000	1.72	24.39	11.56	1.:5	68.46	23.25
7220.000	1.75	25.72	11.29	1.:0	70.88	26.71
7280.000	1.78	27.67	11.07	1.:3	73.18	24.16
7340.000	1.75	29.70	11.32	1.20	70.43	20.82
7400.000	1.71	31.33	11.60	1.09	80.19	27.68
7460.000	1.70	33.04	11.73	1.:9	82.79	21.19
7520.000	1.66	34.76	12.15	1.44	73.27	14.85
7580.000	1.57	35.70	13.07	1.36	80.53	16.41
7640.000	1.47	36.74	14.42	1.26	79.26	18.78
7700.000	1.40	38.55	15.54	1.91	81.43	10.09
7760.000	1.35	39.42	16.58	2.54	72.51	7.24
7820.000	1.32	39.50	17.25	2.56	79.40	7.18
7880.000	1.28	39.24	18.20	1.94	80.79	9.94
7940.000	1.28	38.87	18.34	1.99	71.62	15.77
8000.000	1.32	38.24	17.32	1.:7	74.87	21.99

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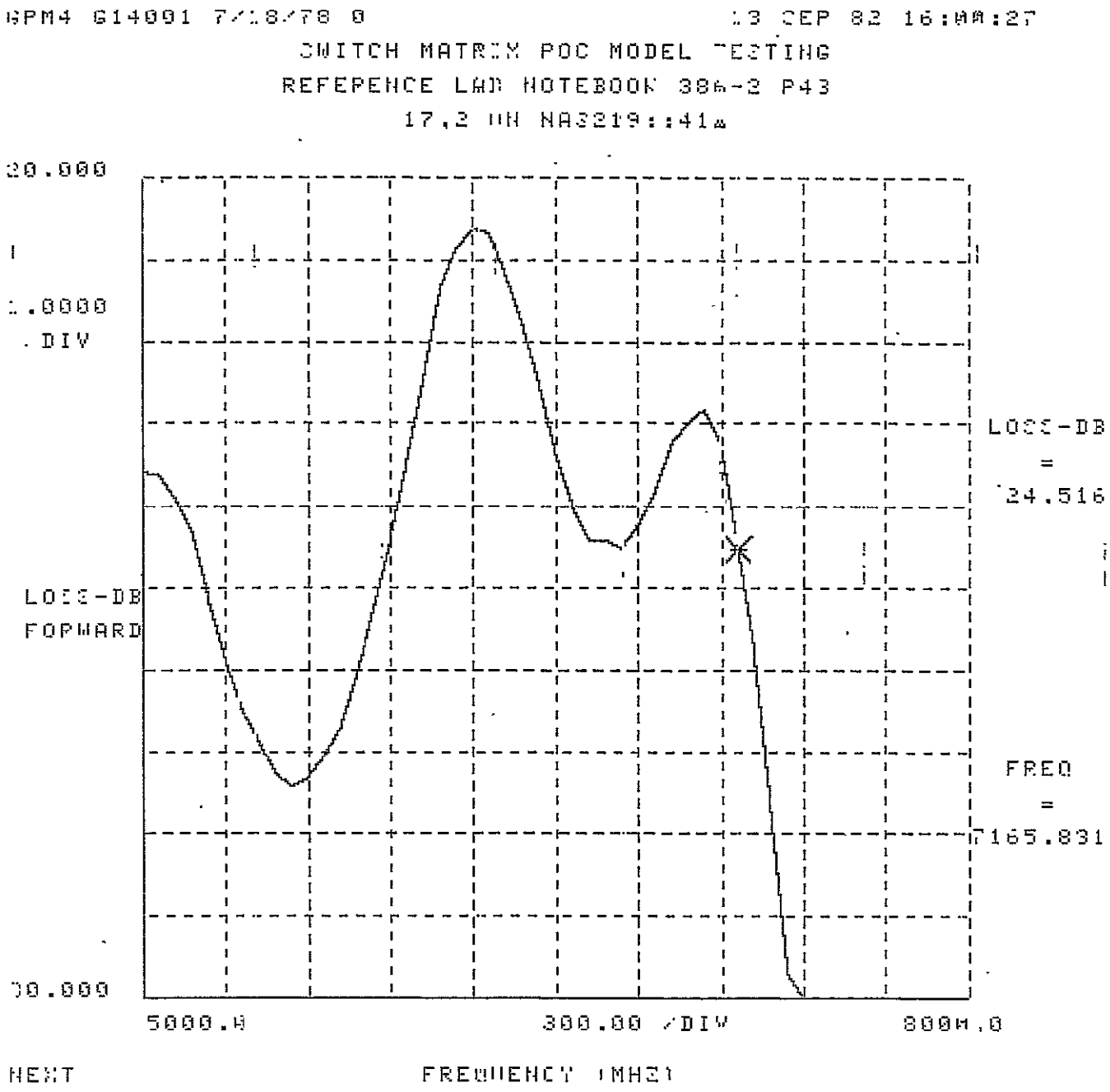

GPM4 G14001 7.18.78 0 13 SEP 82 16:07:54

SWITCH MATRIX POC MODEL TESTING
REFERENCE LAB NOTEBOOK 386-2 P43
18,1 WN NA2231::41

FREQ-MHZ	VSWR FORWARD	LOSS-DB FORWARD	RTN LOSS FORWARD	VSWR REVERSE	LOSS-DB REVERSE	RTN LOSS REVERSE
5000.000	1.07	25.46	29.66	1.03	88.50	36.12
5060.000	1.05	24.44	32.06	1.08	101.28	28.62
5120.000	1.08	23.92	28.08	1.13	83.00	24.20
5180.000	1.12	23.89	24.65	1.15	79.70	23.29
5240.000	1.17	24.05	22.11	1.10	78.59	26.77
5300.000	1.20	24.21	20.93	1.06	75.64	30.28
5360.000	1.22	24.36	20.21	1.10	73.37	26.65
5420.000	1.27	24.51	18.50	1.10	79.60	26.63
5480.000	1.31	24.51	17.56	1.07	82.58	29.72
5540.000	1.31	24.37	17.38	1.07	70.11	29.97
5600.000	1.31	24.22	17.48	1.03	75.47	37.47
5660.000	1.33	23.90	17.08	1.00	87.87	26.37
5720.000	1.33	23.57	16.87	1.24	75.73	19.56
5780.000	1.33	23.09	16.98	1.26	78.75	18.88
5840.000	1.31	22.40	17.52	1.14	78.27	23.90
5900.000	1.28	21.65	18.33	1.08	103.95	28.20
5960.000	1.25	20.89	19.14	1.14	82.29	23.73
6020.000	1.23	20.12	19.83	1.08	74.70	28.34
6080.000	1.18	19.40	21.67	1.18	76.52	21.72
6140.000	1.12	19.00	25.19	1.24	73.87	19.43
6200.000	1.09	18.77	27.41	1.11	79.73	25.81
6260.000	1.08	18.91	28.71	1.07	85.01	29.45
6320.000	1.06	19.37	30.53	1.12	77.97	25.20
6380.000	1.10	19.91	26.43	1.06	84.32	30.59
6440.000	1.16	20.54	22.51	1.01	74.90	25.83
6500.000	1.19	21.47	21.05	1.13	72.04	24.48
6560.000	1.22	21.90	20.19	1.16	79.01	22.54
6620.000	1.24	22.18	19.42	1.22	88.70	20.24
6680.000	1.27	21.90	18.36	1.17	74.72	22.33
6740.000	1.28	22.61	18.25	1.13	83.47	24.39
6800.000	1.26	22.18	18.66	1.27	73.25	18.60
6860.000	1.25	21.60	19.07	1.35	75.16	16.44
6920.000	1.24	21.39	19.30	1.30	76.76	17.67
6980.000	1.22	21.45	19.96	1.27	77.74	18.51
7040.000	1.21	21.26	20.50	1.25	80.40	18.98
7100.000	1.20	21.32	20.88	1.14	80.01	23.93
7160.000	1.22	21.63	20.21	1.30	71.29	17.70
7220.000	1.24	22.48	19.30	1.41	74.50	15.38
7280.000	1.29	23.58	18.06	1.34	74.92	16.70
7340.000	1.31	24.93	17.34	1.46	76.18	14.50
7400.000	1.36	26.26	16.24	1.43	92.25	15.11
7460.000	1.43	27.76	15.03	1.17	78.23	22.14
7520.000	1.47	29.54	14.45	1.39	79.63	15.70
7580.000	1.47	31.09	14.42	1.29	73.87	18.04
7640.000	1.46	33.17	14.52	1.55	79.05	13.28
7700.000	1.49	36.08	14.16	2.44	79.50	7.55
7760.000	1.48	37.73	14.27	2.91	77.16	6.22
7820.000	1.44	38.06	14.86	2.59	77.45	7.06
7880.000	1.37	37.55	16.11	1.82	80.43	10.75
7940.000	1.31	37.22	17.56	1.25	75.09	19.11
8000.000	1.32	37.21	17.30	1.89	93.98	27.43

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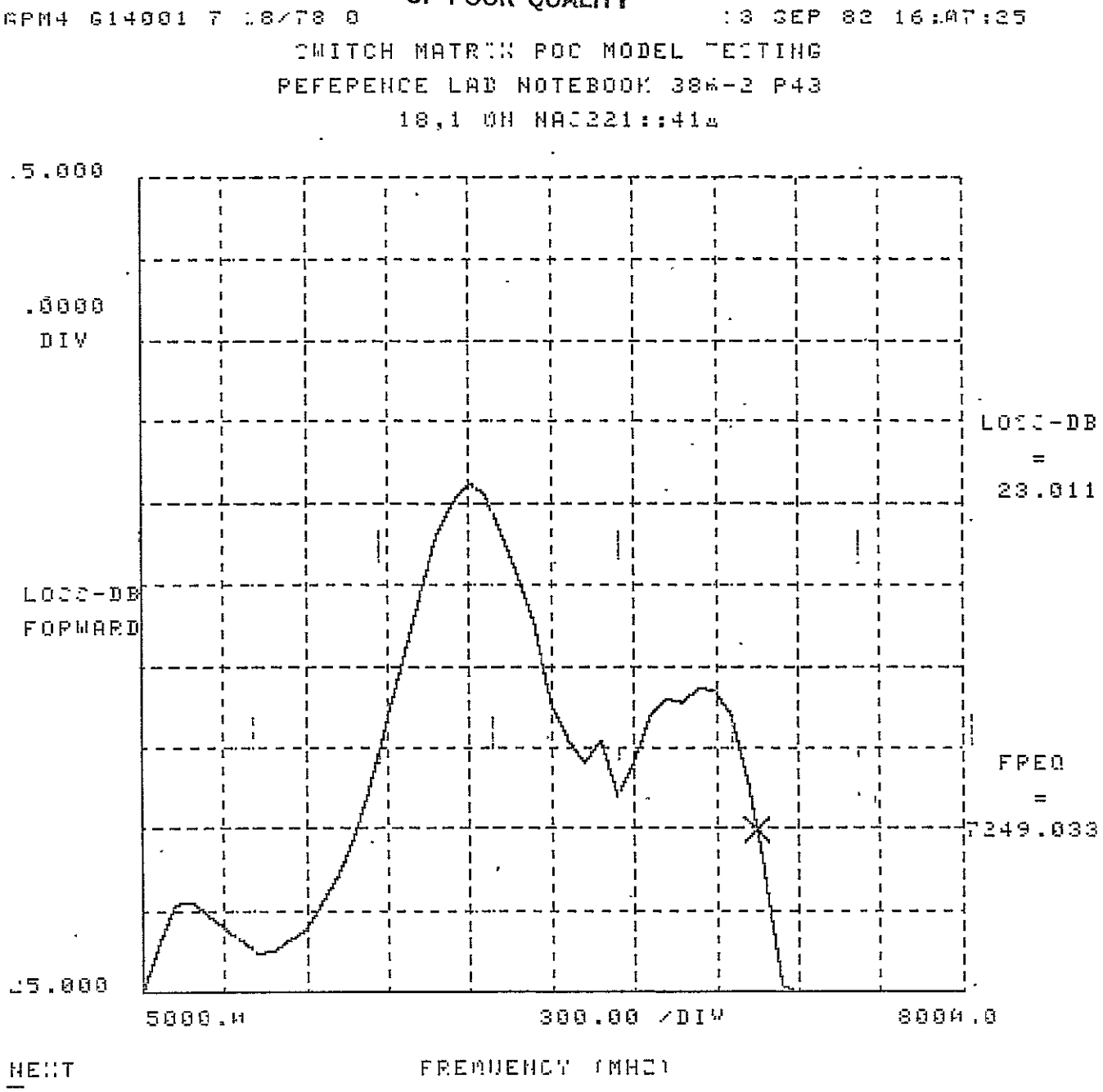

RPM4 G14001 T[illegible]8/78 0 13 SEP 82 16:04:22

SWITCH MATRIX POC MODEL TESTING
REFERENCE LWR NOTEBOOK 38[illegible]-2 P43
18.2 ON HA2220::41

FREQ-MHZ	VSWR FORWARD	LOSS-DB FORWARD	RTN LOSS FORWARD	VSWR REVERSE	LOSS-DB REVERSE	RTN LOSS REVERSE
5000.000	1.07	27.71	29.58	1.07	82.81	29.60
5060.000	1.04	28.10	33.21	1.07	82.62	29.88
5120.000	1.06	28.61	30.88	1.08	82.02	28.34
5180.000	1.10	29.18	26.47	1.11	82.19	25.81
5240.000	1.13	29.20	24.13	1.12	74.17	24.89
5300.000	1.15	29.52	22.87	1.09	79.81	26.92
5360.000	1.18	29.65	21.82	1.05	87.70	32.88
5420.000	1.23	29.35	19.86	1.04	80.19	34.87
5480.000	1.26	29.41	18.85	1.11	88.15	25.71
5540.000	1.26	29.10	18.69	1.13	69.64	24.33
5600.000	1.26	28.44	18.73	1.09	70.12	27.40
5660.000	1.29	27.92	18.01	1.04	78.62	33.18
5720.000	1.30	27.28	17.63	1.04	74.16	33.16
5780.000	1.30	26.34	17.68	1.05	76.40	32.60
5840.000	1.29	25.33	17.96	1.10	78.86	26.20
5900.000	1.27	24.25	18.41	1.25	74.91	18.97
5960.000	1.26	23.25	18.66	1.40	86.81	15.52
6020.000	1.25	22.14	19.01	1.38	76.08	15.98
6080.000	1.22	21.04	20.15	1.18	73.54	21.69
6140.000	1.17	20.41	22.05	1.14	85.81	23.72
6200.000	1.16	20.18	22.58	1.20	75.96	20.86
6260.000	1.14	20.30	23.58	1.09	80.62	27.65
6320.000	1.10	20.69	26.21	1.08	89.21	28.70
6380.000	1.09	21.26	27.50	1.13	100.21	24.40
6440.000	1.12	21.94	25.19	1.13	84.83	24.08
6500.000	1.14	22.87	23.96	1.18	78.60	21.55
6560.000	1.15	23.57	23.02	1.22	81.63	20.07
6620.000	1.17	24.09	21.97	1.17	78.86	22.01
6680.000	1.21	24.37	20.63	1.12	77.19	24.81
6740.000	1.23	24.75	19.88	1.08	80.88	28.29
6800.000	1.23	24.69	19.82	1.07	78.99	29.34
6860.000	1.23	24.62	19.80	1.09	79.11	27.40
6920.000	1.24	24.50	19.38	1.13	72.55	24.54
6980.000	1.25	24.02	19.13	1.16	80.75	22.59
7040.000	1.25	23.74	19.11	1.14	80.39	23.66
7100.000	1.25	23.58	19.08	1.07	81.00	29.07
7160.000	1.27	23.74	18.58	1.11	75.33	25.45
7220.000	1.28	23.90	18.12	1.10	76.78	26.22
7280.000	1.31	24.72	17.40	1.12	77.88	24.98
7340.000	1.32	25.94	17.14	1.23	77.47	19.76
7400.000	1.36	27.25	16.31	1.14	73.73	23.74
7460.000	1.42	28.88	15.16	1.19	78.86	21.37
7520.000	1.46	30.58	14.54	1.50	72.35	13.93
7580.000	1.46	31.66	14.53	1.44	73.88	14.95
7640.000	1.46	33.05	14.62	1.32	84.08	17.21
7700.000	1.48	35.07	14.23	2.05	85.32	9.27
7760.000	1.48	36.63	14.23	2.70	78.88	6.74
7820.000	1.45	37.28	14.74	2.62	80.92	6.98
7880.000	1.38	37.45	15.91	1.90	82.66	10.15
7940.000	1.32	37.64	17.26	1.14	71.19	16.82
8000.000	1.33	37.47	16.90	1.12	72.47	24.91

REF PLANE EXT CNT: INPUT= .00 TRAN= .00 OUTPUT= .00
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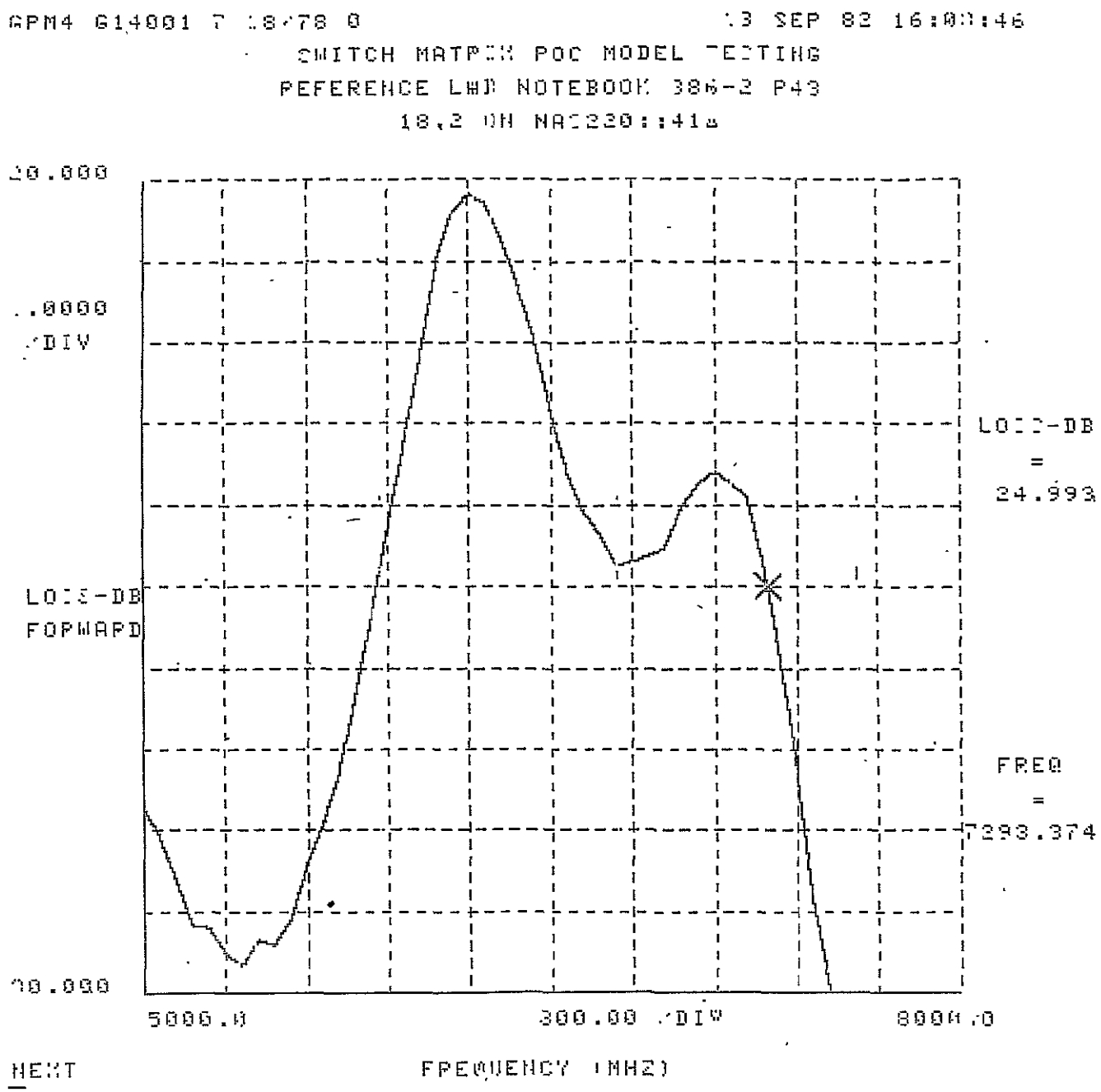

SWITCH MATRIX POC MODEL TESTING
REFERENCE LAB NOTEBOOK 38M-2 P43
19,1 ON HA3222::41

FREQ-MHZ	V MP FORWARD	LOSS-DB FORWARD	PTN LOSS FORWARD	VSWR REVERSE	LOSS-DB REVERSE	PTN LOSS REVERSE
5000.000	1.09	24.17	27.09	1.03	81.94	36.22
5060.000	1.11	23.35	25.99	1.08	80.43	28.58
5120.000	1.15	23.00	23.30	1.13	91.81	24.16
5180.000	1.17	22.96	22.28	1.15	75.03	23.27
5240.000	1.20	23.12	20.76	1.10	83.77	26.75
5300.000	1.21	23.54	20.61	1.06	75.57	30.26
5360.000	1.21	24.01	20.52	1.10	75.61	26.66
5420.000	1.25	24.33	19.14	1.10	77.83	26.55
5480.000	1.28	24.65	18.18	1.07	77.96	29.66
5540.000	1.28	24.71	18.08	1.06	70.59	30.25
5600.000	1.28	24.65	18.09	1.03	77.09	38.03
5660.000	1.29	24.43	17.83	1.10	78.10	26.49
5720.000	1.31	24.10	17.43	1.23	73.37	19.58
5780.000	1.33	23.59	17.07	1.26	77.49	18.87
5840.000	1.31	22.93	17.45	1.14	75.68	23.82
5900.000	1.29	22.29	17.94	1.08	76.74	28.37
5960.000	1.27	21.97	18.54	1.14	79.41	23.86
6020.000	1.26	21.41	18.89	1.09	75.47	27.78
6080.000	1.22	20.37	20.09	1.17	74.42	21.91
6140.000	1.17	19.60	22.34	1.24	75.57	19.50
6200.000	1.11	19.08	25.45	1.11	73.38	25.53
6260.000	1.07	19.00	29.69	1.06	82.35	30.11
6320.000	1.03	19.28	36.17	1.12	91.46	25.16
6380.000	1.03	19.76	35.73	1.06	90.44	30.07
6440.000	1.09	20.52	26.95	1.10	74.37	26.28
6500.000	1.13	21.57	24.36	1.13	78.84	24.18
6560.000	1.16	22.35	22.59	1.16	77.38	22.52
6620.000	1.19	22.83	21.34	1.21	85.64	20.43
6680.000	1.23	23.05	19.65	1.17	74.59	22.21
6740.000	1.24	23.81	19.55	1.13	85.85	24.94
6800.000	1.22	23.34	19.94	1.26	72.60	18.71
6860.000	1.21	22.31	20.27	1.06	76.64	16.35
6920.000	1.20	22.38	20.75	1.00	78.94	17.61
6980.000	1.19	21.96	21.07	1.26	79.08	18.70
7040.000	1.20	21.70	21.01	1.26	75.26	18.88
7100.000	1.21	21.66	20.45	1.14	79.23	23.76
7160.000	1.25	21.82	18.96	1.29	72.75	17.83
7220.000	1.30	22.64	17.60	1.41	79.05	15.39
7280.000	1.38	23.45	16.02	1.35	77.29	16.59
7340.000	1.42	24.58	15.19	1.47	73.52	14.48
7400.000	1.48	25.80	14.30	1.42	76.97	15.14
7460.000	1.55	27.18	13.28	1.17	79.62	22.22
7520.000	1.61	29.02	12.64	1.40	72.29	15.61
7580.000	1.62	30.69	12.54	1.29	71.96	17.97
7640.000	1.60	32.88	12.71	1.55	81.94	13.29
7700.000	1.61	36.02	12.58	2.45	87.06	7.54
7760.000	1.62	37.83	12.47	2.92	75.31	6.19
7820.000	1.61	38.26	12.64	2.60	81.77	7.04
7880.000	1.54	38.05	13.50	1.02	77.19	10.74
7940.000	1.47	37.86	14.47	1.25	78.09	19.10
8000.000	1.48	38.12	14.30	1.09	86.46	27.63

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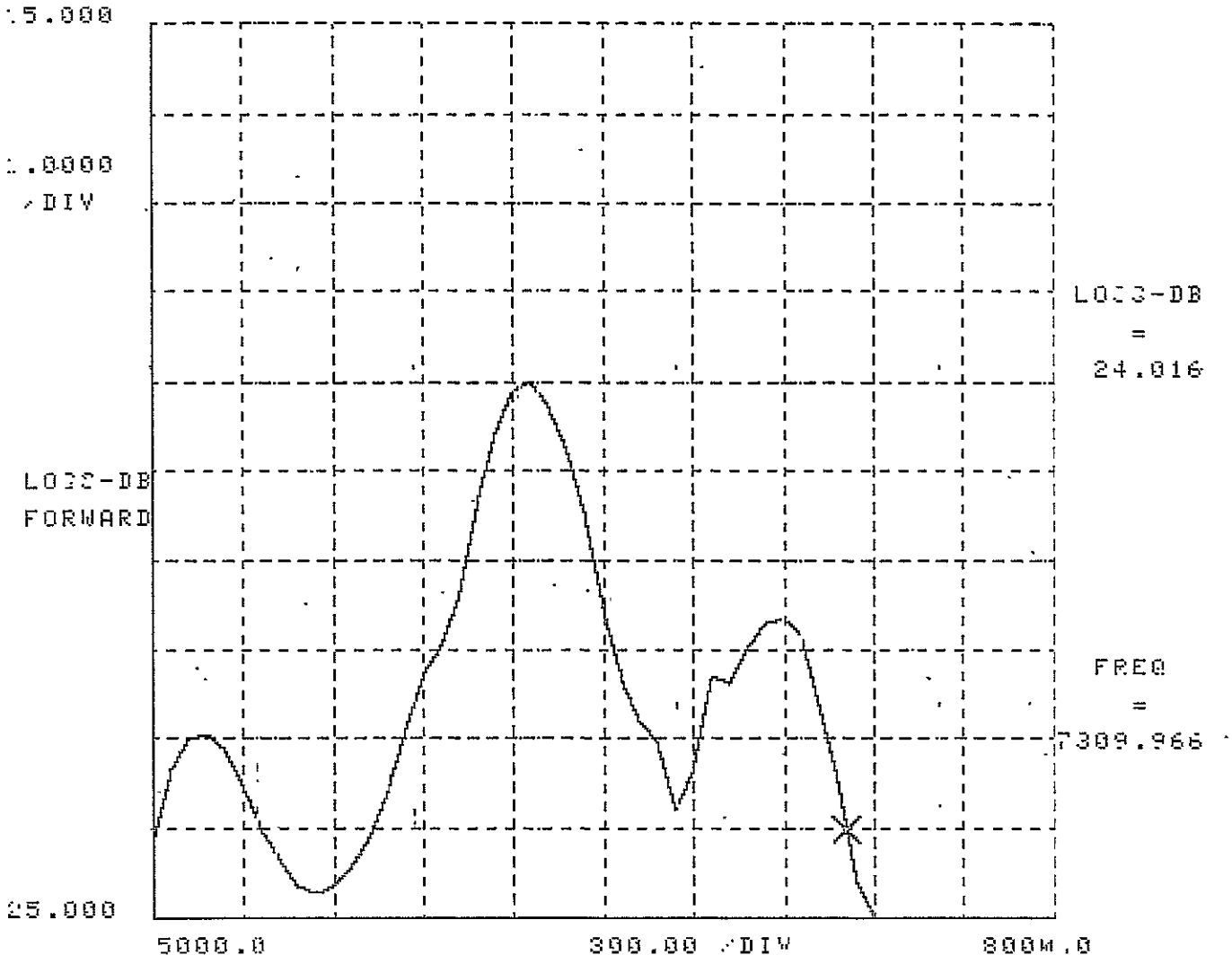
GPM4 G14001 7/18/78 0 13 SEP 82 16:10:42

SWITCH MATRIX POC MODEL TESTING

REFERENCE LAB NOTEBOOK 386-2 P43

19.1 dB HA3222::41a



NEXT

FREQUENCY (MHZ)

GPM4 G14001 7/18/78 0 13 SEP 82 16:17:40

SWITCH MATRIX POC MODEL TESTING
REFERENCE LMD NOTEBOOK 386-2 P43
19,2 MN HAS223::41

FREQ-MHZ	VSWR, FORWARD	LOSS-DB FORWARD	RTN LOSS FORWARD	VSWR REVERSE	LOSS-DB REVERSE	RTN LOSS REVERSE
5000.000	1.08	28.95	28.60	1.04	89.70	33.51
5060.000	1.09	29.39	27.20	1.04	80.80	33.37
5120.000	1.13	30.01	24.36	1.06	77.74	31.13
5180.000	1.15	30.51	23.35	1.10	76.55	26.08
5240.000	1.17	30.90	22.19	1.16	83.99	22.76
5300.000	1.17	31.32	21.96	1.15	79.67	23.38
5360.000	1.18	31.58	21.58	1.07	70.05	29.39
5420.000	1.22	31.43	20.04	1.08	87.63	28.58
5480.000	1.25	31.42	19.12	1.15	80.36	23.02
5540.000	1.25	31.07	19.00	1.13	75.71	24.15
5600.000	1.26	30.51	18.90	1.05	74.53	31.62
5660.000	1.27	29.87	18.42	1.07	83.43	28.87
5720.000	1.29	29.04	17.95	1.08	75.95	27.93
5780.000	1.30	28.03	17.60	1.03	75.50	36.01
5840.000	1.29	26.90	17.88	1.08	75.70	27.87
5900.000	1.28	25.78	18.24	1.29	76.52	18.06
5960.000	1.26	24.63	18.64	1.48	81.21	14.24
6020.000	1.26	23.45	18.84	1.44	80.70	14.82
6080.000	1.23	22.48	19.82	1.20	80.60	20.85
6140.000	1.18	21.96	21.76	1.10	81.55	21.79
6200.000	1.14	21.88	23.87	1.22	74.57	19.98
6260.000	1.10	22.09	26.48	1.08	85.53	28.43
6320.000	1.06	22.61	30.32	1.12	90.83	25.02
6380.000	1.01	23.25	47.37	1.07	86.34	22.35
6440.000	1.05	24.06	32.09	1.16	79.16	22.76
6500.000	1.08	25.28	27.80	1.20	79.53	20.78
6560.000	1.11	26.22	25.40	1.21	77.38	20.39
6620.000	1.14	27.04	23.60	1.14	77.14	23.86
6680.000	1.18	27.58	21.85	1.09	76.43	27.55
6740.000	1.20	27.04	20.74	1.06	83.60	30.16
6800.000	1.21	26.70	20.57	1.08	72.92	28.48
6860.000	1.21	26.40	20.32	1.11	80.10	25.51
6920.000	1.23	25.78	19.68	1.16	75.07	22.63
6980.000	1.25	25.45	19.17	1.21	86.21	20.29
7040.000	1.25	25.24	18.97	1.18	78.44	21.48
7100.000	1.26	25.40	18.75	1.04	79.49	33.60
7160.000	1.29	25.98	18.04	1.14	68.92	23.86
7220.000	1.32	26.57	17.27	1.16	78.56	22.82
7280.000	1.37	27.58	16.19	1.16	77.26	22.82
7340.000	1.40	28.89	15.61	1.29	73.80	17.85
7400.000	1.44	30.00	14.83	1.19	81.97	21.10
7460.000	1.52	31.28	13.76	1.23	92.75	19.77
7520.000	1.57	32.68	13.10	1.60	70.98	12.74
7580.000	**1.58**	**33.75**	**12.93**	**1.51**	**76.25**	**13.83**
7640.000	1.57	35.09	13.03	1.39	85.11	15.66
7700.000	1.60	37.35	12.76	2.21	83.23	8.48
7760.000	1.61	38.99	12.58	2.07	73.66	6.32
7820.000	**1.60**	**39.97**	**12.70**	**2.64**	**73.10**	**6.92**
7880.000	1.54	40.54	13.18	1.96	84.11	10.41
7940.000	1.47	41.12	14.39	1.31	75.63	17.47
8000.000	1.49	41.54	14.14	1.11	76.78	25.91

REF PLANE EXT(MI: INPUT= .00 TRAN= .00 OUTPUT= .00
NRAIL(1)= 4

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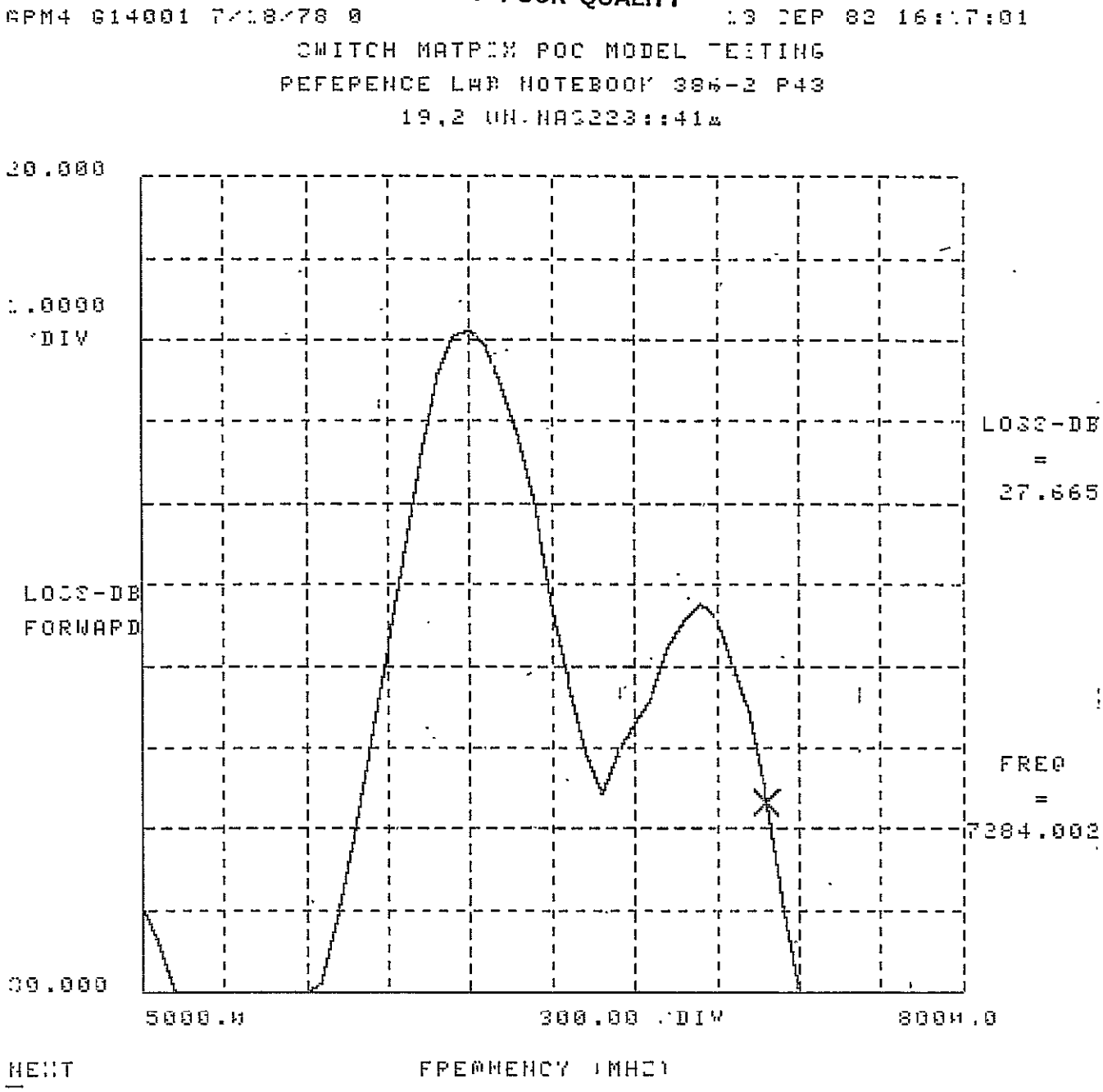

GPM4 G14001 7/18/78 0 13 SEP 82 16:22:20

SWITCH MATRIX POC MODEL TESTING
REFERENCE LAB NOTEBOOK 38%-2 P43
1,1 W ON HAC224::4'

FREQ-MHZ	VSWR FORWARD	LOSS-DB FORWARD	RTN LOSS FORWARD	VSWR REVERSE	LOSS-DB REVERSE	RTN LOSS REVERSE
5000.000	1.22	22.46	20.10	1.03	78.80	36.15
5060.000	1.20	21.47	20.74	1.07	92.83	28.88
5120.000	1.14	20.61	23.42	1.03	81.91	24.22
5180.000	1.10	20.07	26.85	1.05	75.20	23.31
5240.000	1.05	20.00	32.41	1.09	80.53	26.89
5300.000	1.02	19.95	39.18	1.06	75.57	30.25
5360.000	1.06	19.86	30.68	1.00	75.08	26.53
5420.000	1.09	20.17	27.15	1.03	81.10	26.47
5480.000	1.08	20.40	27.90	1.07	72.14	29.53
5540.000	1.10	20.41	26.82	1.07	74.78	30.03
5600.000	1.14	20.47	23.83	1.03	73.50	36.68
5660.000	1.10	20.24	26.11	1.03	78.56	26.68
5720.000	1.06	19.30	31.20	1.23	81.59	19.81
5780.000	1.06	18.76	30.05	1.25	76.21	19.06
5840.000	1.05	18.57	32.27	1.03	80.89	24.11
5900.000	1.08	17.85	28.75	1.07	83.53	29.07
5960.000	1.08	16.98	28.77	1.03	75.14	24.09
6020.000	1.03	16.50	36.86	1.08	75.04	28.65
6080.000	1.18	15.36	21.49	1.08	77.94	21.80
6140.000	1.23	14.47	19.64	1.24	73.57	19.54
6200.000	1.12	14.64	25.24	1.01	82.45	26.00
6260.000	1.07	14.53	29.86	1.07	76.11	29.24
6320.000	1.12	14.00	24.95	1.02	78.57	24.97
6380.000	1.03	14.16	37.31	1.07	78.93	29.30
6440.000	1.25	14.51	19.12	1.01	72.79	25.57
6500.000	1.35	14.11	16.46	1.03	71.82	24.11
6560.000	1.21	13.83	20.58	1.06	77.27	22.57
6620.000	1.07	14.15	28.96	1.20	82.50	20.72
6680.000	1.19	14.13	21.18	1.05	84.79	22.89
6740.000	1.13	14.39	24.22	1.01	77.70	25.50
6800.000	1.26	14.92	18.84	1.25	72.55	19.19
6860.000	1.35	14.58	16.47	1.34	70.71	16.76
6920.000	1.23	13.83	19.71	1.29	73.76	17.99
6980.000	1.27	14.05	18.59	1.25	76.05	18.96
7040.000	1.31	14.31	17.56	1.25	73.21	19.03
7100.000	1.15	14.69	22.98	1.05	72.49	23.19
7160.000	1.26	16.22	18.71	1.01	73.24	17.56
7220.000	1.37	17.99	16.09	1.42	85.98	15.25
7280.000	1.28	19.05	18.15	1.35	74.13	16.46
7340.000	1.33	21.00	16.93	1.47	79.70	14.43
7400.000	1.36	22.27	16.25	1.43	74.31	15.04
7460.000	1.36	22.61	16.42	1.17	78.36	22.08
7520.000	1.63	24.88	12.38	1.39	77.67	15.67
7580.000	1.77	26.63	11.11	1.29	72.85	17.98
7640.000	1.87	27.51	10.38	1.54	81.94	13.40
7700.000	2.86	32.48	6.33	2.44	87.78	7.58
7760.000	4.11	38.19	4.31	2.92	75.46	6.21
7820.000	4.08	35.10	4.35	2.61	77.82	7.02
7880.000	2.78	30.30	6.55	1.83	87.40	10.66
7940.000	1.74	29.30	11.35	1.26	73.12	18.93
8000.000	1.31	30.40	17.47	1.09	72.34	27.45

REF PLANE EXT CM: INPUT= .00 TRAN= .00 OUTPUT= .00
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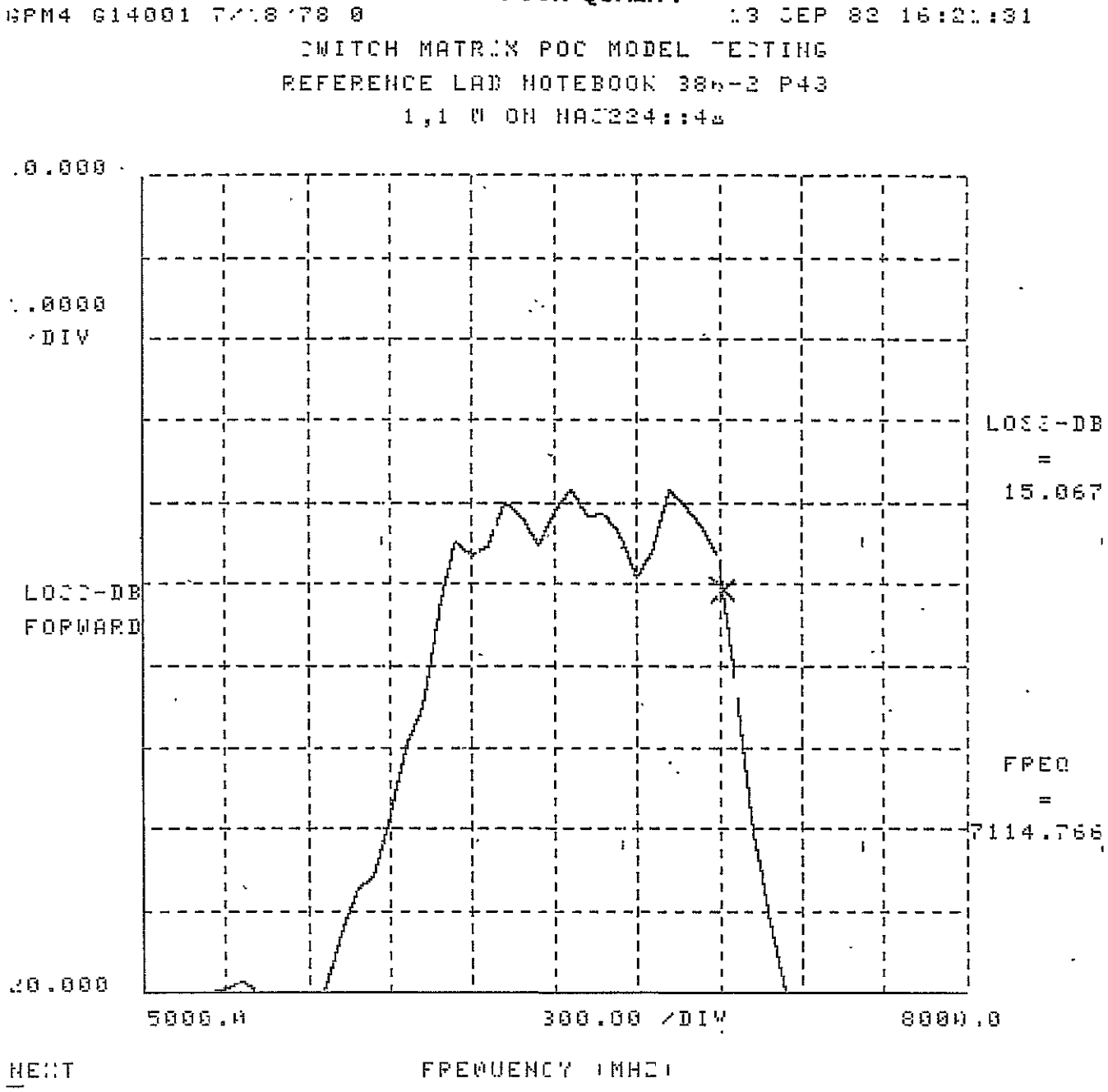

APM4 G14001 7[illegible] 0 13 SEP 82 16:27:31

SWITCH MATRIX POC MODEL TESTING
REFERENCE LAB NOTEBOOK 38%-2 P43
5,1 W UH NA3225:::4[illegible]

FREQ-MHZ	VSWR FORWARD	LOSS-DB FORWARD	RTN LOSS FORWARD	VSWR REVERSE	LOSS-DB REVERSE	RTN LOSS REVERSE
5000.000	1.26	30.05	18.75	1.04	82.50	34.92
5060.000	1.25	29.62	18.99	1.08	79.89	28.23
5120.000	1.19	29.44	21.08	1.14	80.60	23.95
5180.000	1.16	29.68	22.51	1.15	81.61	23.18
5240.000	1.15	29.81	23.06	1.10	83.53	26.86
5300.000	1.14	29.80	23.48	1.06	75.05	30.09
5360.000	1.13	30.02	24.37	1.10	74.17	26.41
5420.000	1.10	29.98	26.73	1.10	94.07	26.57
5480.000	1.08	29.69	28.69	1.07	81.77	29.78
5540.000	1.09	29.19	27.56	1.06	74.31	30.31
5600.000	1.11	28.37	25.48	1.02	73.82	39.14
5660.000	1.17	27.89	22.02	1.10	77.27	26.19
5720.000	1.21	27.83	20.52	1.24	79.91	19.46
5780.000	1.24	27.30	19.55	1.26	74.99	18.81
5840.000	1.24	25.80	19.50	1.14	87.62	23.88
5900.000	1.20	23.79	20.86	1.08	85.87	28.17
5960.000	1.15	22.40	22.96	1.14	78.28	23.58
6020.000	1.12	20.91	25.27	1.09	76.36	27.79
6080.000	1.07	19.53	29.91	1.19	71.57	21.42
6140.000	1.07	18.20	29.54	1.25	74.55	19.14
6200.000	1.15	16.80	23.04	1.12	71.82	25.04
6260.000	1.22	16.21	20.14	1.08	86.46	28.70
6320.000	1.24	15.57	19.32	1.13	79.08	24.55
6380.000	1.25	14.59	19.16	1.06	83.36	30.09
6440.000	1.23	13.73	19.88	1.09	80.28	27.68
6500.000	1.18	13.01	21.46	1.10	72.18	26.11
6560.000	1.11	12.48	25.91	1.14	80.44	23.76
6620.000	1.05	12.48	33.04	1.18	77.94	21.45
6680.000	1.10	12.78	26.06	1.15	73.47	23.31
6740.000	1.19	13.43	21.10	1.13	81.28	24.16
6800.000	1.27	14.68	18.48	1.28	72.61	18.31
6860.000	1.33	16.50	16.92	1.37	74.04	16.12
6920.000	1.36	18.48	16.25	1.31	81.51	17.34
6980.000	1.35	19.09	16.53	1.27	75.89	18.40
7040.000	1.29	19.78	17.84	1.27	80.01	18.64
7100.000	1.21	19.78	20.48	1.15	74.31	23.12
7160.000	1.12	20.30	25.26	1.30	76.46	17.80
7220.000	1.14	22.66	23.53	1.41	80.27	15.40
7280.000	1.26	24.20	18.76	1.75	76.82	16.62
7340.000	1.43	27.31	14.97	1.46	74.32	14.56
7400.000	1.64	31.31	12.34	1.42	78.09	15.14
7460.000	1.84	34.84	10.56	1.17	84.65	22.32
7520.000	1.99	40.00	9.58	1.39	72.83	15.74
7580.000	2.08	44.97	9.12	1.28	83.11	18.10
7640.000	2.10	48.80	8.98	1.55	78.20	13.38
7700.000	2.11	53.73	8.95	2.44	78.48	7.57
7760.000	2.03	59.48	9.35	2.91	71.96	6.22
7820.000	1.90	55.77	10.19	2.60	86.02	7.85
7880.000	1.69	52.39	11.82	1.82	100.56	10.72
7940.000	1.50	51.47	13.93	1.25	76.35	19.05
8000.000	1.41	50.85	15.47	1.08	73.97	27.84

REF PLANE EXT (CM): INPUT= .00 TRAN= .00 OUTPUT= .00
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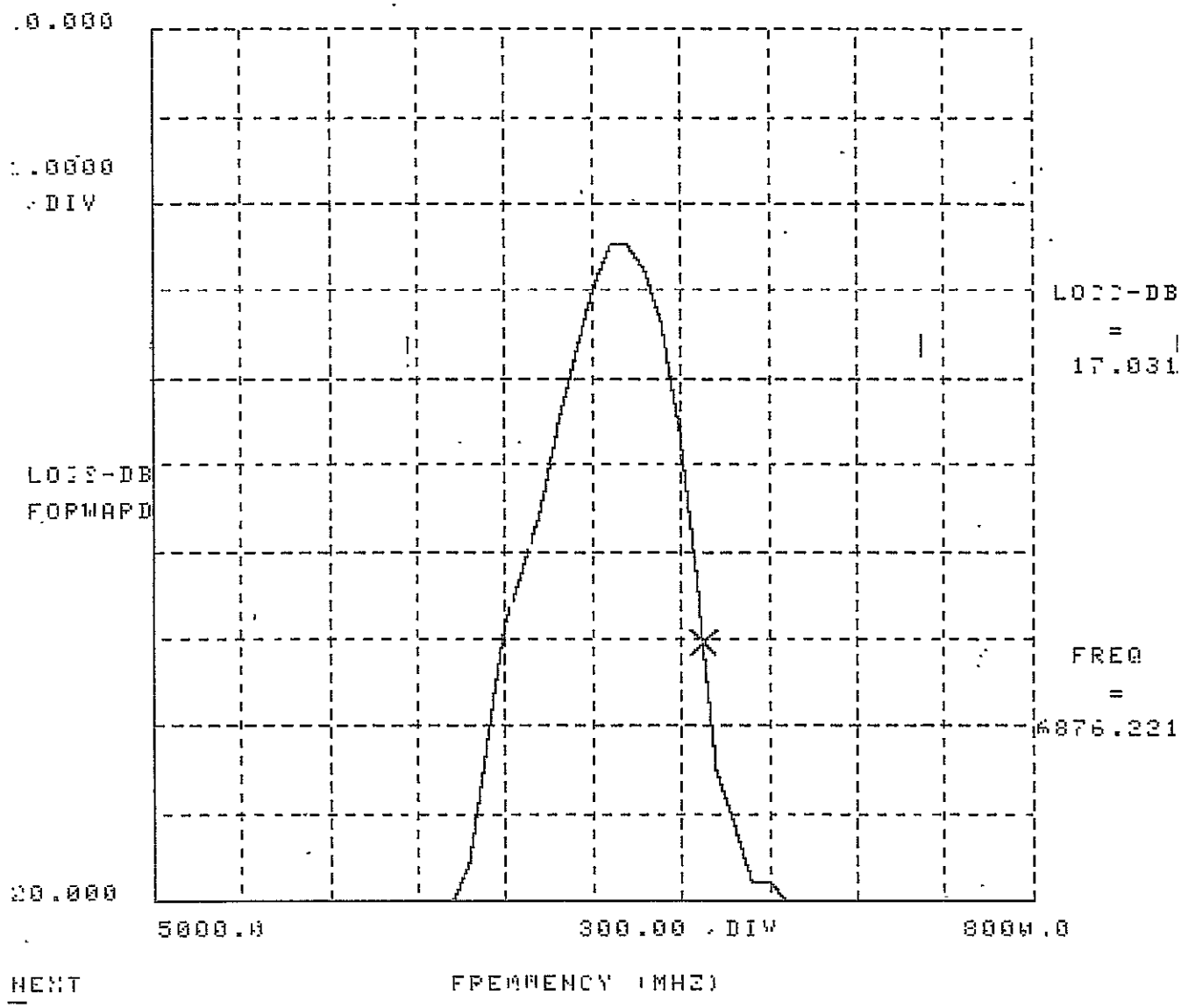

GPM4 G14001 T..:8.:78 0 ..3 SEP 82 16:3..:11

SWITCH MATRIX POC MODEL TESTING
REFERENCE LAB NOTEBOOK 3846-2 P43
5,5 W ON HAC226::4..

FREQ-MHZ	VSWR FORWARD	LOSS-DB FORWARD	RTN LOSS FORWARD	VSWR REVERSE	LOSS-DB REVERSE	RTN LOSS REVERSE
5000.000	..27	29.55	18.58	1..1	92.36	25.76
5060.000	..25	28.63	18.94	1..0	91.81	26.72
5120.000	..19	27.82	21.10	1..0	78.83	26.84
5180.000	..17	27.83	22.35	1..0	76.26	26.32
5240.000	..16	28.47	22.86	1..1	90.90	25.94
5300.000	..15	29.22	23.29	1..0	78.65	26.60
5360.000	..13	29.99	24.36	1..1	78.78	25.74
5420.000	..10	30.42	26.82	1..3	91.95	24.19
5480.000	..07	30.22	28.96	1..5	81.95	23.13
5540.000	..09	29.70	27.63	1..6	71.51	22.81
5600.000	..11	29.29	25.49	1..6	71.36	22.43
5660.000	..17	29.32	21.92	1..8	74.20	21.74
5720.000	..21	29.09	20.28	1.20	76.05	20.92
5780.000	..24	28.61	19.35	1.20	73.13	20.80
5840.000	..24	27.27	19.24	1..9	76.73	21.20
5900.000	..20	24.75	20.80	1..7	84.28	22.03
5960.000	..15	22.83	22.92	1..5	80.78	23.27
6020.000	..12	20.95	25.17	1..0	73.75	26.52
6080.000	..07	18.79	29.87	1.06	75.90	31.02
6140.000	..07	16.89	29.59	1.06	74.22	30.75
6200.000	..15	15.50	23.00	1..2	75.04	24.94
6260.000	..22	14.64	20.10	1..9	84.27	21.44
6320.000	..24	14.27	19.31	1.24	78.83	19.38
6380.000	..25	13.93	19.16	1.26	82.07	18.65
6440.000	..23	13.45	19.80	1.26	83.60	18.87
6500.000	..19	13.26	21.30	1.24	76.39	19.50
6560.000	..11	13.00	25.58	1..9	77.84	21.19
6620.000	..05	12.82	32.77	1..3	84.99	24.17
6680.000	..11	13.04	25.94	1.06	76.91	30.13
6740.000	..19	13.81	21.06	1.02	79.27	38.24
6800.000	..27	15.05	18.51	1.07	73.32	29.60
6860.000	..33	16.85	16.92	1..3	74.07	24.60
6920.000	..37	18.62	16.19	1..7	78.39	21.90
6980.000	..36	20.31	16.38	1.21	90.67	20.59
7040.000	..30	21.67	17.73	1.22	77.58	20.21
7100.000	..21	22.48	20.47	1..9	73.98	21.32
7160.000	..11	23.13	25.36	1..3	70.51	24.01
7220.000	..14	24.68	23.59	1.08	80.32	28.22
7280.000	..26	26.12	18.75	1.08	78.66	28.52
7340.000	..44	28.84	14.91	1..6	72.89	22.51
7400.000	..65	32.44	12.25	1.26	80.29	18.65
7460.000	..85	36.81	10.48	1..7	85.82	16.09
7520.000	2.00	41.97	9.54	1.47	75.73	14.43
7580.000	2.09	47.53	9.07	1.55	74.32	13.37
7640.000	2.12	53.48	8.91	1.57	77.78	13.10
7700.000	2.12	56.93	8.89	1.56	77.12	13.18
7760.000	2.04	59.72	9.30	1.54	74.89	13.46
7820.000	..90	58.90	10.16	1.48	82.09	14.33
7880.000	..69	56.41	11.82	1.38	79.28	15.86
7940.000	..51	54.90	13.91	1..0	73.02	17.63
8000.000	.. 41	52.65	15.38	1..5	72.40	19.01

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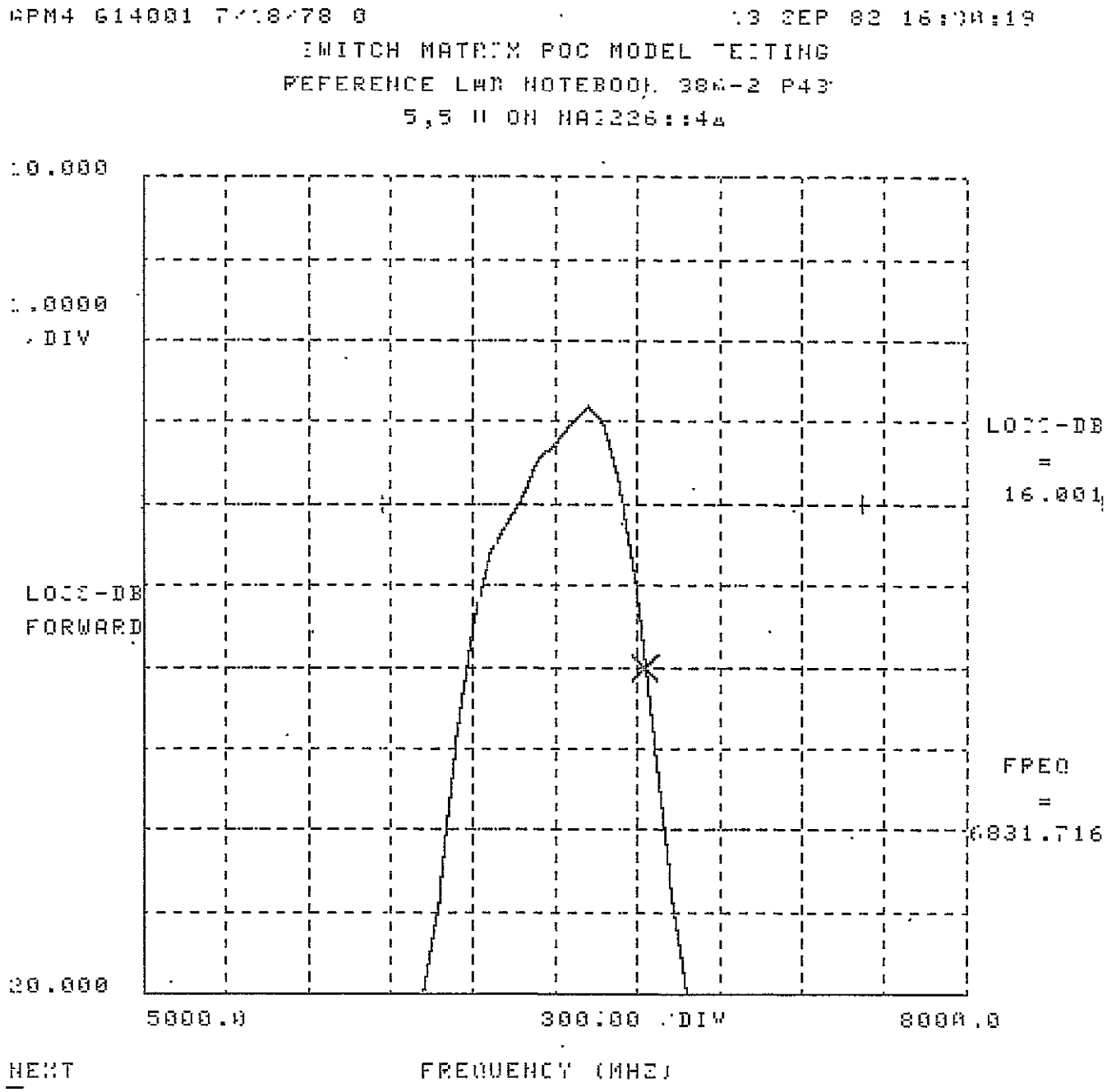

SWITCH MATRIX POC MODEL TESTING
REFERENCE LAB NOTEBOOK 38M-2 P43
1.5 M ON HA3227:41

FREQ-MHZ	VSWR FORWARD	LOSS-DB FORWARD	RTN LOSS FORWARD	VSWR REVERSE	LOSS-DB REVERSE	RTN LOSS REVERSE
5000.000	1.23	16.39	19.84	1.11	85.41	25.76
5060.000	1.21	14.58	20.54	1.10	80.65	26.71
5120.000	1.15	13.49	23.31	1.10	84.90	26.82
5180.000	1.10	13.81	26.56	1.10	83.45	26.27
5240.000	1.06	15.34	31.22	1.11	91.72	25.94
5300.000	1.03	17.67	37.69	1.10	76.10	26.56
5360.000	1.05	21.17	31.61	1.11	77.59	25.66
5420.000	1.09	21.07	27.17	1.13	87.11	24.13
5480.000	1.09	21.34	27.66	1.15	74.95	23.09
5540.000	1.10	21.43	26.81	1.16	72.14	22.78
5600.000	1.14	21.18	23.76	1.16	70.77	22.40
5660.000	1.11	20.75	25.47	1.18	83.44	21.72
5720.000	1.06	20.49	30.24	1.20	75.57	20.89
5780.000	1.06	20.19	31.39	1.20	77.55	20.79
5840.000	1.04	19.02	34.67	1.19	78.96	21.18
5900.000	1.06	17.51	30.20	1.17	79.33	21.97
5960.000	1.06	15.84	30.62	1.15	73.91	23.23
6020.000	1.04	13.72	33.20	1.10	80.28	26.43
6080.000	1.20	12.01	20.88	1.06	77.11	31.01
6140.000	1.24	9.99	19.41	1.06	76.46	30.70
6200.000	1.11	7.53	25.44	1.12	83.96	24.94
6260.000	1.08	6.30	27.92	1.09	78.94	21.43
6320.000	1.14	5.53	23.43	1.24	79.04	19.36
6380.000	1.03	5.01	35.37	1.26	95.84	18.65
6440.000	1.24	5.47	19.30	1.26	81.23	18.87
6500.000	1.37	6.78	16.17	1.24	76.56	19.47
6560.000	1.23	6.95	19.78	1.19	79.03	21.15
6620.000	1.06	7.21	31.03	1.13	84.17	24.18
6680.000	1.17	8.84	22.35	1.06	77.67	30.08
6740.000	1.11	9.73	25.90	1.02	82.20	38.37
6800.000	1.23	11.02	19.72	1.07	72.36	29.62
6860.000	1.32	13.28	17.19	1.13	74.16	24.59
6920.000	1.20	14.85	20.90	1.18	77.25	21.87
6980.000	1.24	16.62	19.32	1.21	80.29	20.59
7040.000	1.27	18.67	18.37	1.22	80.03	20.17
7100.000	1.14	18.88	23.62	1.19	73.98	21.24
7160.000	1.30	19.90	17.80	1.14	70.32	23.91
7220.000	1.40	21.64	15.48	1.08	78.33	28.09
7280.000	1.32	23.00	17.14	1.08	84.54	28.52
7340.000	1.38	25.20	15.92	1.16	73.79	22.55
7400.000	1.41	28.73	15.31	1.26	83.62	18.67
7460.000	1.39	33.06	15.75	1.37	79.44	16.06
7520.000	1.64	38.29	12.31	1.47	71.09	14.39
7580.000	1.77	43.82	11.09	1.55	80.08	13.32
7640.000	1.85	49.27	10.52	1.57	77.02	13.03
7700.000	2.83	54.28	6.42	1.57	86.92	13.13
7760.000	4.13	61.11	4.29	1.54	71.49	13.41
7820.000	4.18	58.34	4.23	1.48	80.86	14.29
7880.000	2.89	53.37	6.27	1.09	85.03	15.83
7940.000	1.83	50.62	10.69	1.00	76.90	17.61
8000.000	1.37	50.49	16.09	1.25	77.35	19.00

REF PLANE ENT CMD: INPUT= .00 TRAN= .00 OUTPUT= .00
NPAIL(1)= 4

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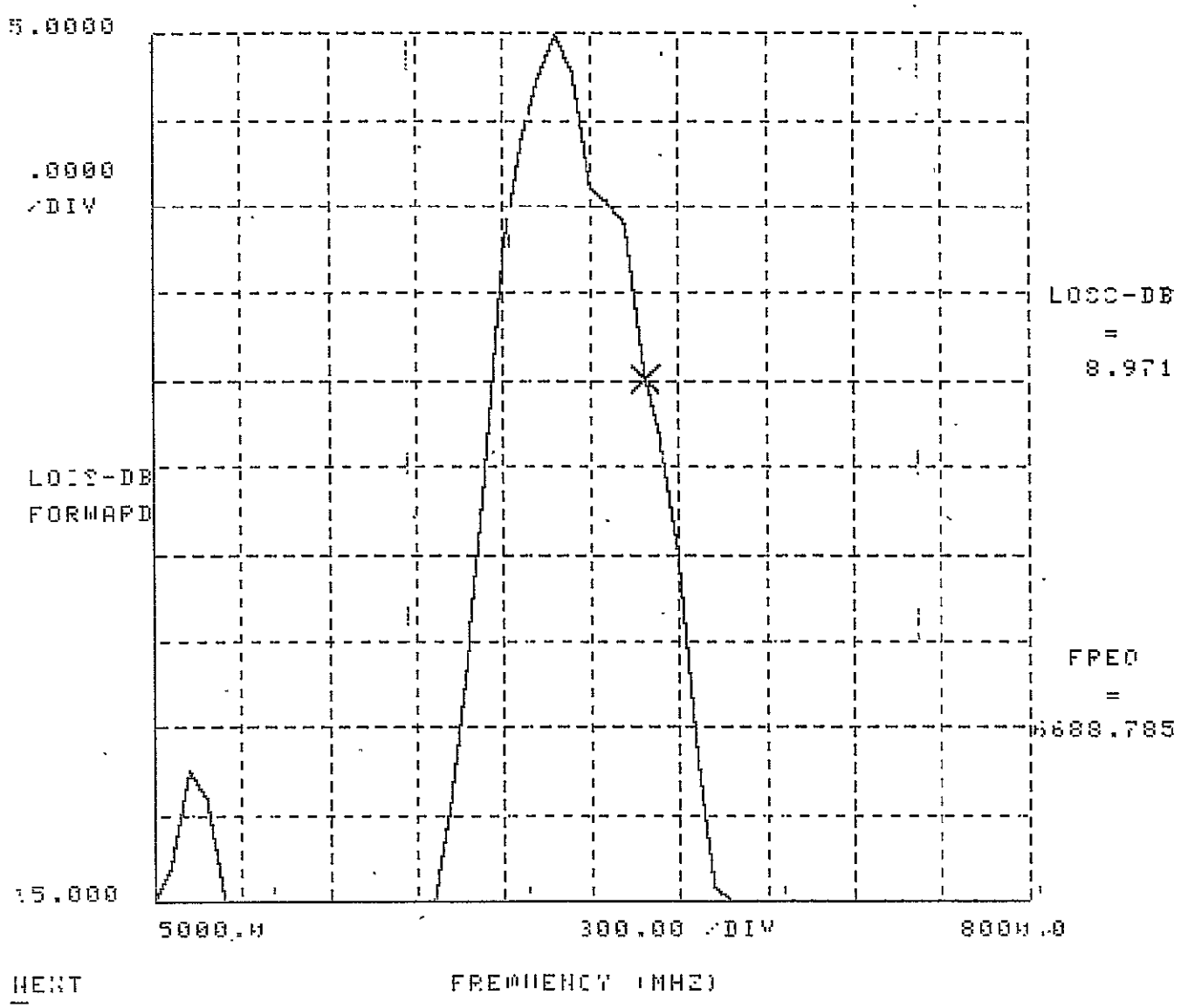

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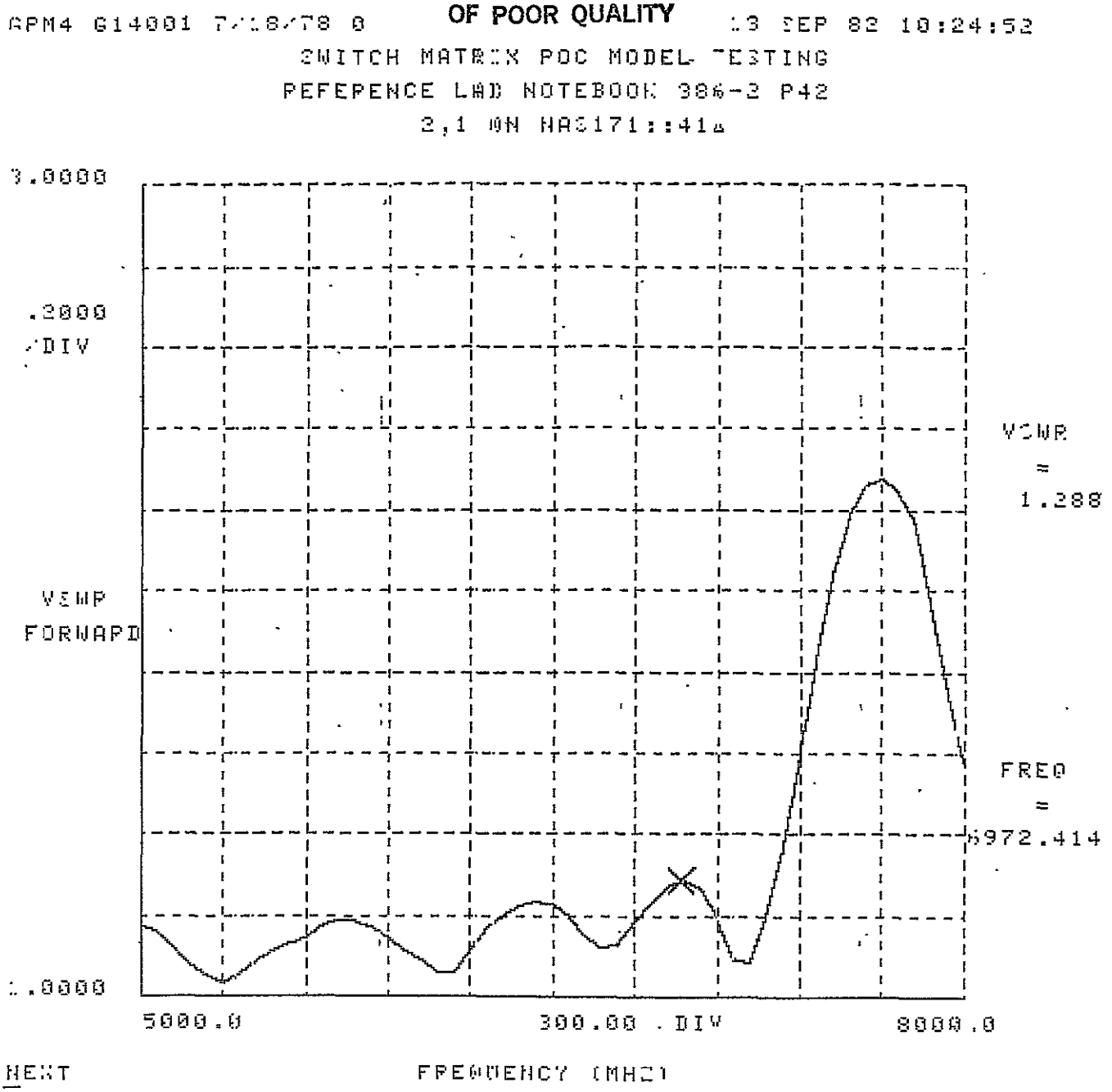

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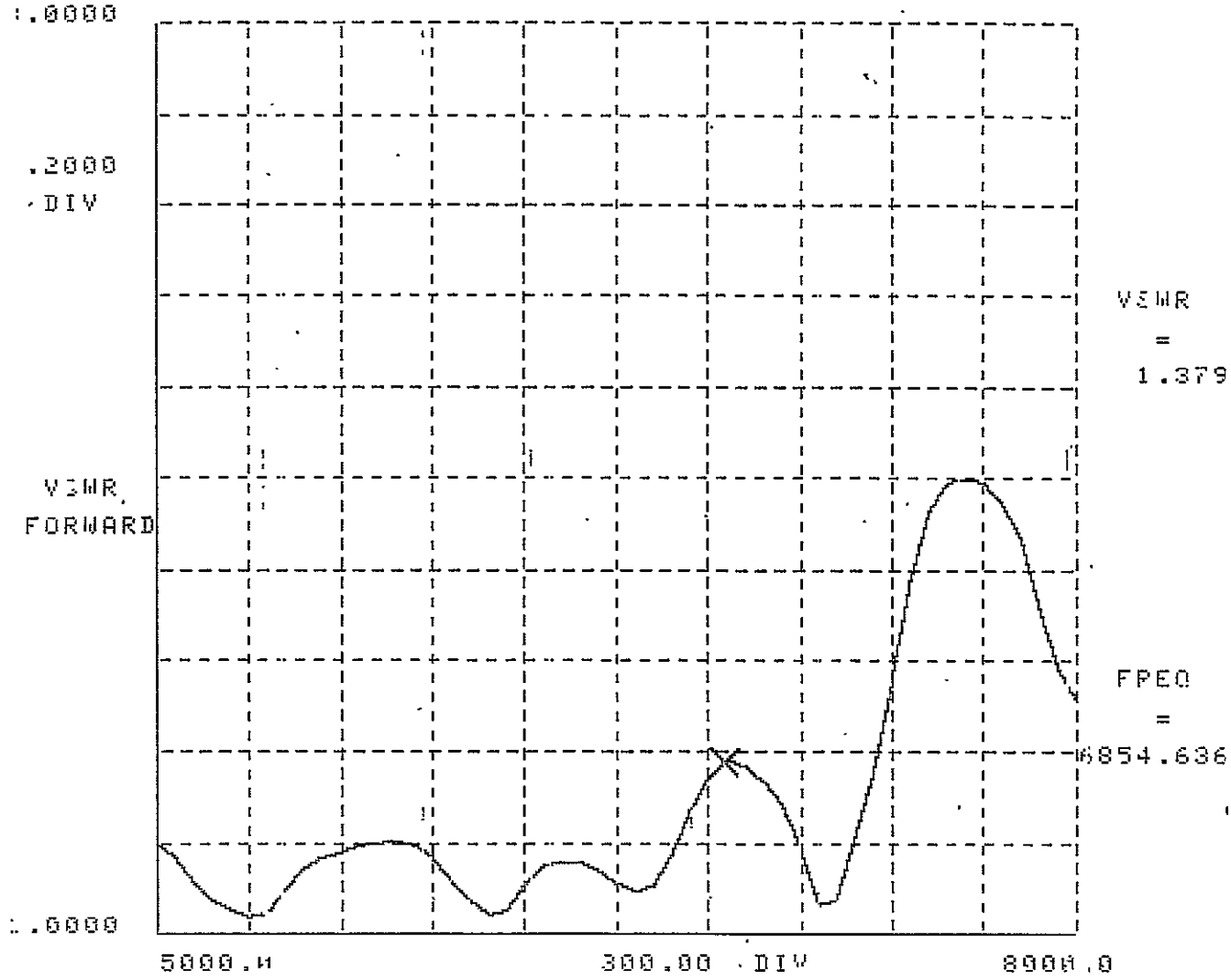
SWITCH MATRIX POC MODEL TESTING

REFERENCE LAB NOTEBOOK 386-2 P42

3.1 OH HAC172::41@



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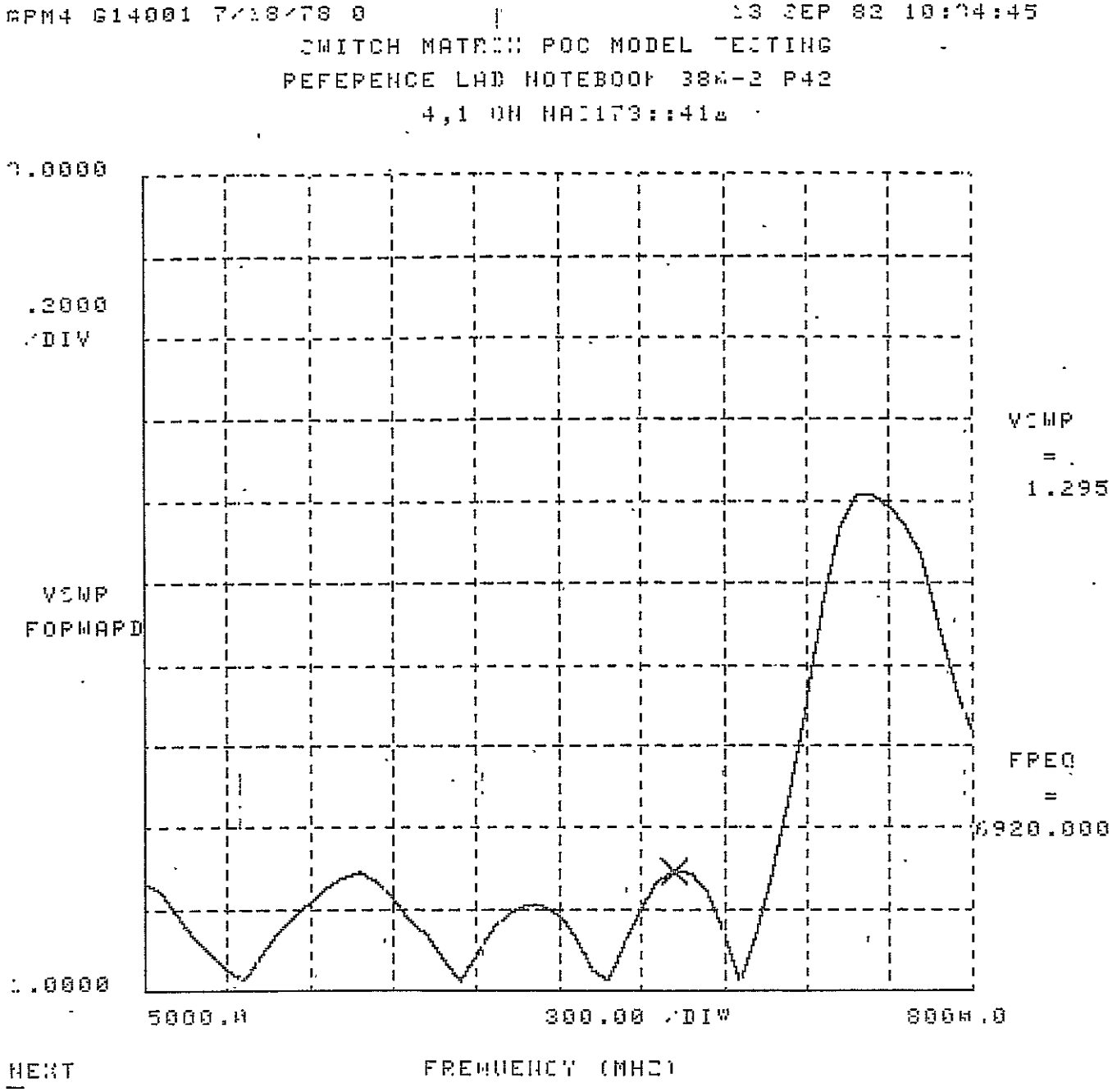

GENERAL ELECTRIC

SPACE SYSTEMS DIVISION

Headquarters: Valley Forge, PA ☐Huntsville, AL ☐Lanham, MD
☐Houston, TX ☐Sunnyvale, CA ☐Beltsville, MD
☐Palmdale, CA ☐Bedford, MA ☐Washington, D.C. Area