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NASA-LEWIS Research Center

Cleveland, Ohio

FINAL REPORT

GRANT NAG 3-299

JUNE 25, 1982 TO JUNE 24, 1983

VLSI Technology and Applications

Donald L. Schilling

Professor of Electrical Engineering

Principal Investigator

COMMUNICATIONS SYSTEMS LABORATORY

DEPARTMENT OF ELECTRICAL ENGINEERING

THE CITY COLLEGE OF
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ABSTRACT

This report discusses NMOS, CMOS and Ga As devices. Digital and analog circuits are described. Applications to Communications Circuits are presented.

Introduction

In the 1940's and 1950's vacuum tubes were used exclusively in the design of communications systems. Such systems were relatively of low speed and dissipated significant power. Size and weight were of great concern. In the 1950's transistors started to be used as communications circuits and as a result, digital communications became practical. Size, weight and power consumption dropped as did switching speed. In the 1970's these parameters were reduced once again as IC's became popular.

Today, the latest form of IC, VLSI is being developed. The VLSI system is smaller, faster, and dissipates less power per communication device than any of its predecessors. This report describes VLSI technology and applications to Communications.

1.0 MOS Integrated Circuits

The main characteristics of MOS transistors are reviewed as they are related to digital and analog circuit design [1] [2]. The basic circuits are examined as well as some processing technologies. Finally, state of the art applications are presented.

1.1 Digital MOS Integrated Circuits

1.1.1 MOS Device Characteristics

The basic structure of an N channel MOS transistor is shown in Fig. 1 [3]. It consists of two n+ regions diffused or ion implanted in a P substrate. In circuit operation, the more positive region is called the drain while the other is called a source. The region between the source and drain is called the channel. The conduction through this channel is controlled by the voltage on the gate, which is either metal or polysilicon. A thin layer of dielectric, usually silicon oxide, separates the gate from the channel.

If the voltage of the source terminal is taken as a reference, then V_{DS}, V_{GS} and V_{BB} are the voltages of the drain, gate and substrate respectively. An applied positive V_{DS} allows electrons, when present in the channel, to drift from the source to the drain causing I_{DS} to flow from the drain to the source. In enhancement-type NMOS, electrons are only present in the channel if V_{GS} is positive and larger than V_T where V_T is the threshold voltage of the enhancement-type device. An increase in
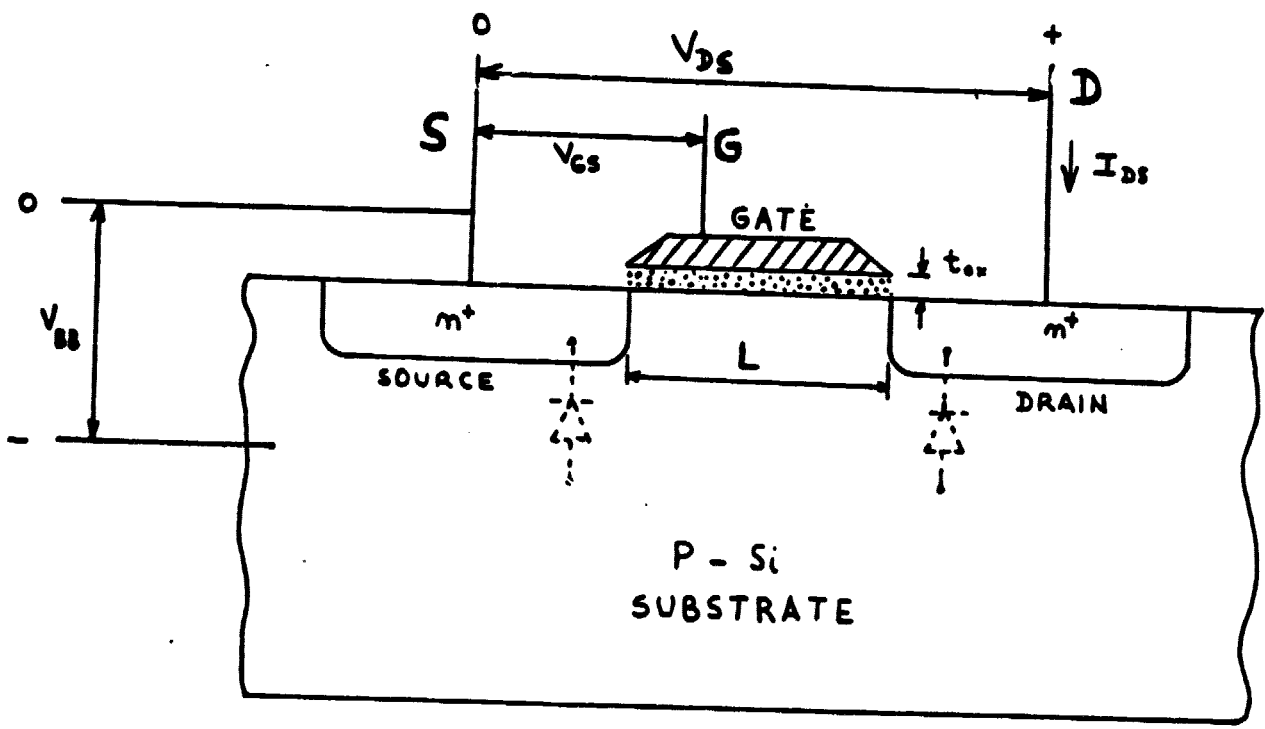
Fig. 1 Cross section of an NMOS transistor

V_{GS} increases I_{DS}. In depletion-type devices, electrons are present in the channel even at $V_{GS} = 0$. This is achieved by ion implanting the surface channel with n-type material. An increase in V_{GS} increases I_{DS}. However if V_{GS} is negative and larger than V_T, where V_T is the threshold voltage of the depletion-type device, the channel is depleted and I_{DS} is reduced to zero.

DC Characteristics

Figure 2 shows two important dc characteristics of the NMOS transistor. The drain current I_{DS} is plotted as a function of the drain voltage V_{DS} for different values of V_{GS} at a given substrate bias V_{BB}; also the drain current I_{DS} is plotted as a function of the gate voltage V_{GS} at a given V_{BB}.

Three regions of operation can be distinguished on the I_{DS} vs V_{DS} characteristic:

1) The off region where $V_{GS} < V_T$ and $I_{DS} = 0$. The value of I_{DS} in this region is much smaller than its value when $V_{GS} > V_T$. Thus the transistor is considered off. However, the small value of I_{DS} in this region could affect the circuit performance as in MOS dynamic memory circuits.

2) The nonsaturation region, where

$$V_{DS} < V_{GS} - V_T$$

$$I_{DS} = \beta [(V_{GS} - V_T) V_{DS} - 1/2 \, V^2_{DS}] \tag{1}$$

I_{DS}

$V_{DS} = V_{GS} - V_T$

Non-saturation Region

Saturation Region

$\rightarrow V_{GS} = 0$ for depletion type

$\rightarrow V_{GS} = 0$ for enhancement type

V_{DS}

I_{DS} vs. V_{DS}

I_{DS}

Depletion type

Enhancement type

V_T

V_T

V_{GS}

I_{DS} vs V_{GS} (V_{BB} fixed)
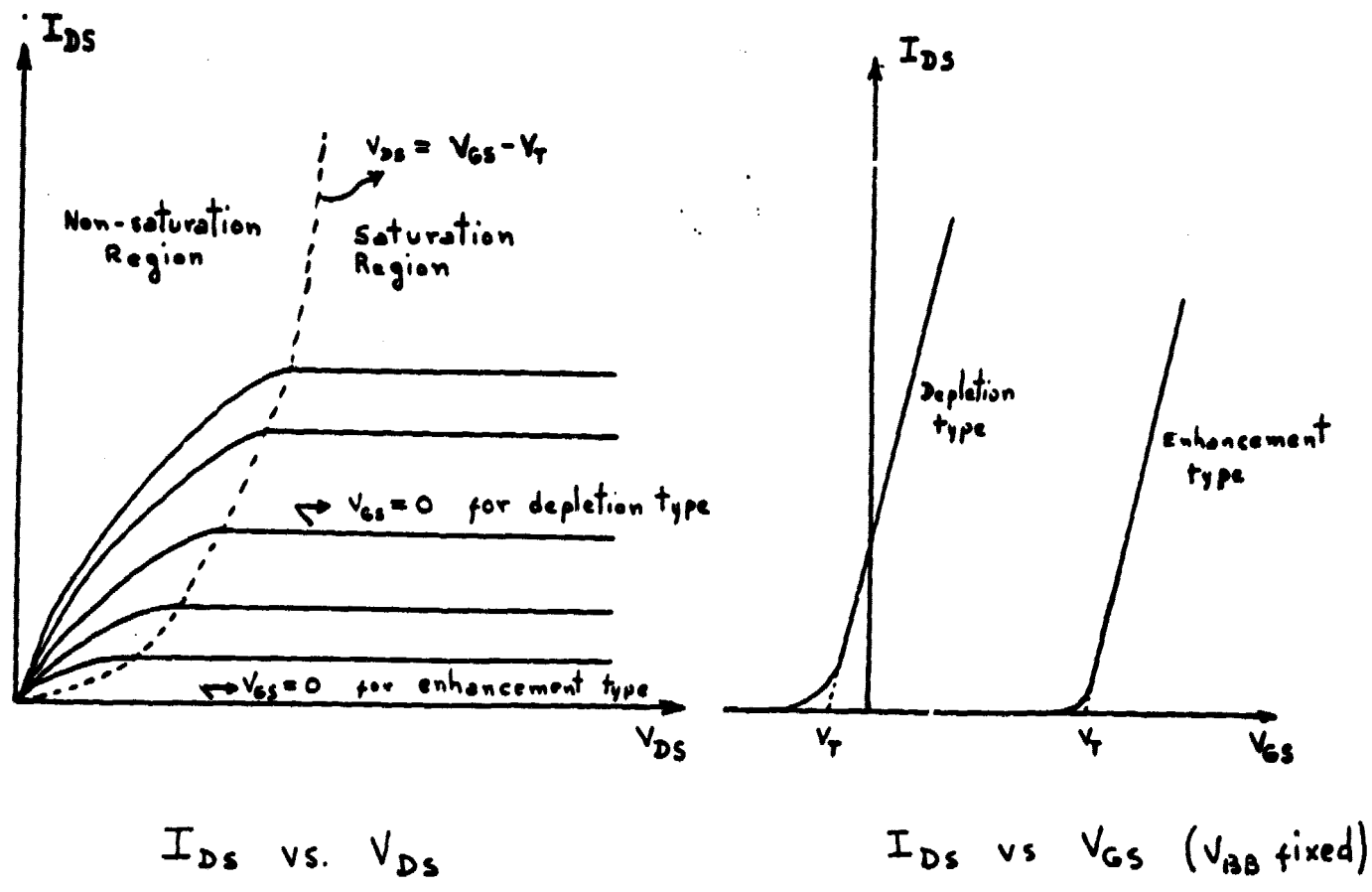
Fig. 2

3) The saturation region,

$$V_{DS} \geq V_{GS} - V_T$$

$$I_{DS} = \frac{\beta}{2} [V_{GG} - V_T]^2 \qquad (2)$$

where

$$\beta = \frac{W}{L} \frac{\varepsilon_{ox} \mu}{t_{ox}} = \frac{W}{L} K' \qquad (3)$$

W = width of the MOS channel

L = length of the MOS channel

ε_{ox} = permittivity of the gate oxide

t_{ox} = thickness of the gate oxide

μ = average surface mobility of carriers

V_T = threshold voltage

C_{ox} = gate capacitance per unit area = $\frac{\varepsilon_{ox}}{t_{ox}}$

The conduction factor $K' \equiv \frac{\varepsilon_{ox} \mu}{t_{ox}}$ is technology dependent and is specified for a given MOS process. K' is a function of temperature because of its dependency on μ .

The geometrical ratio (W/L) is a circuit design parameter. The minimal value of L is determined by the MOS fabrication process. The minimal value of W is usually in the order of the minimum value of L. Increasing (W/L) will increase the drain current for a given set of operating voltages. However, increasing W increases the gate area and the source and the drain diffusion areas and consequently increases the value of the capacitances associated with the gate and with the

source-substrate and the drain-substrate junctions.

The threshold voltage V_T is a function of the MOS processing parameters and the substrate bias V_{BB}. In general, it is also a function of V_{DS}.

Transient Characteristics

The transient performance of a MOS integrated circuit is a function of the total capacitance at the output node. This capacitance C_{out} is the summation of the parasitic output capacitance C_0 and the input gate capacitances of the loading stages C_{IN} [3, 4, 5, 6].

Static NMOS Inverter

The NMOS inverter, shown in Fig 3(a), consists of an enhancement type driver transistor and a load. The load is one of the following: (1) a saturated enhancement-type NMOS device, (2) a nonsaturated enhancement-type MOS device. (3) a depletion-type NMOS device, or (4) a polysilicon resistor. The different loads are shown in Fig 3(a) [1]. Figure 3(b) shows the load lines of the above four loads superimposed on the I_{DS} vs. V_{DS} of the driver. V_0 is the low voltage level representing logical '0' and V_1 is the high voltage level representing logical '1'. The intersection of the load line with the driver characteristic for $V_{GS} = V_{IN} = V_0$, gives $V_{DS} = V_{OUT} = V_1$. Similarly, the intersection of the load line with the driver characteristic for $V_{GS} = V_{IN} = V_1$, gives $V_{DS} = V_{OUT} = V_0$.
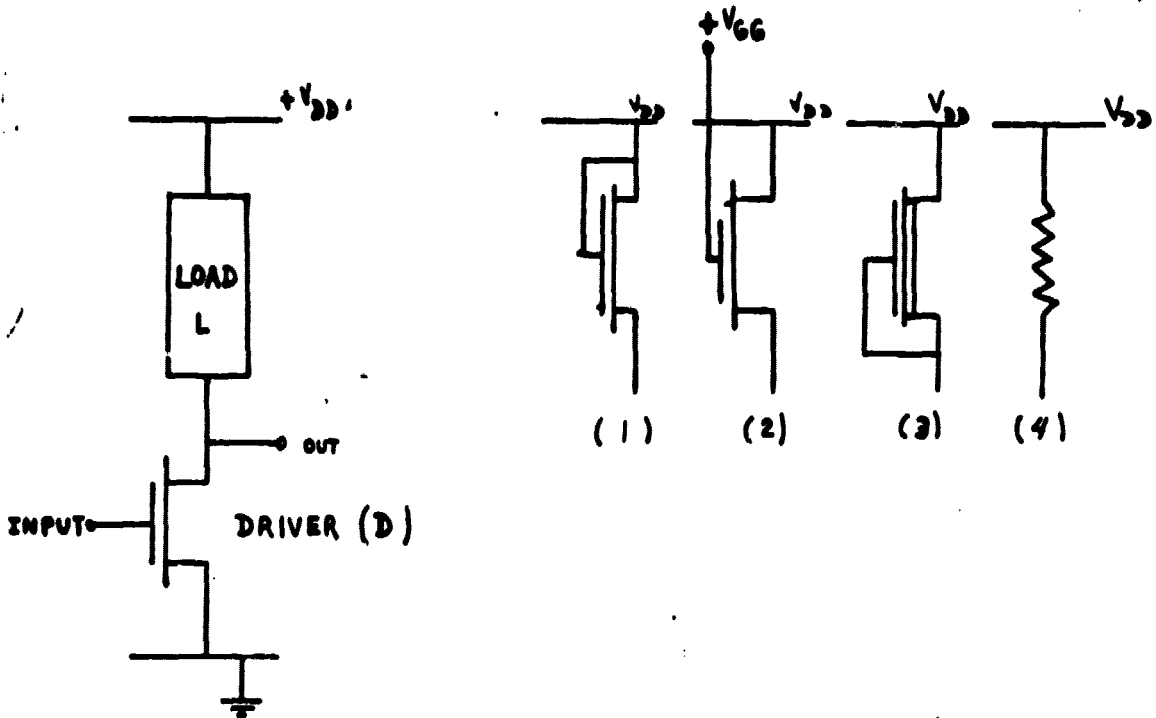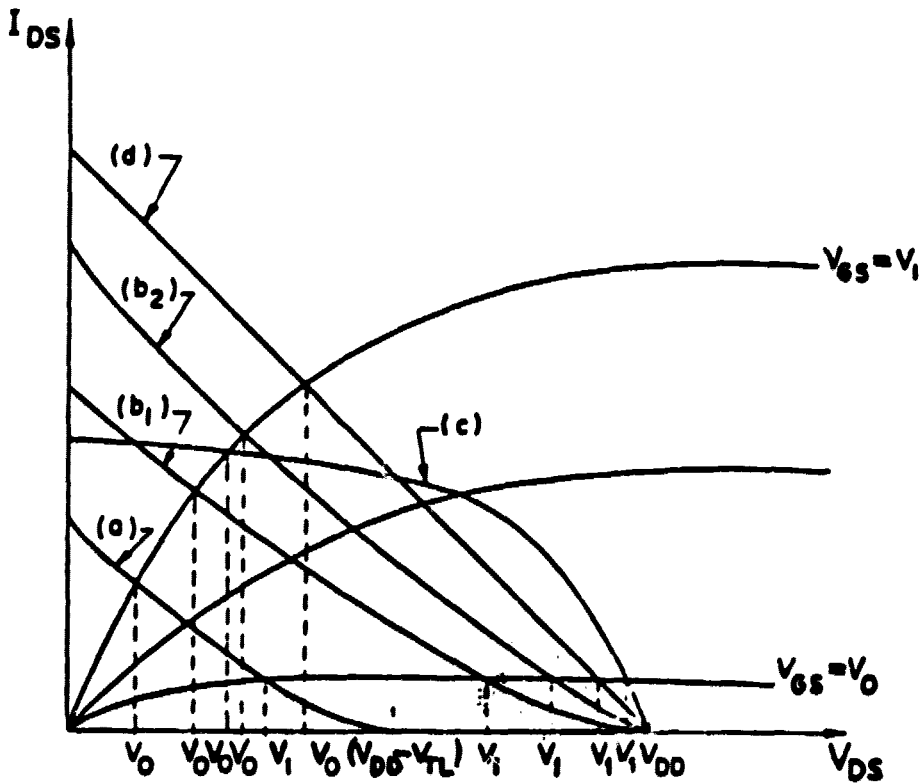
Fig. 3 (a)   NMOS inverter and loads

Fig. 3 (b)   Load lines on I_{DS} vs V_{DS}

DC Performance

Saturated Enhancement-Type Load

This type of load was used in the early digital MOS integrated circuits. This load device operates in the saturation region when it conducts, since $V_{DS} > (V_{GS} - V_{TL})$, where V_{TL} is the threshold voltage of the load device.

(a) When $V_{IN} = V_0$, $V_0 < V_{TD}$, the driver is off, $I \approx 0$ and $V_{OUT} = V_1 = V_{DD} - V_{TL}$, where V_0 and V_1 are defined in the previous section, I is shown in Fig. 3, and V_{TD} is the threshold voltage of the driver.

(b) When $V_{IN} = V_1$, $V_1 > V_{TD}$, the driver is operating in the nonsaturated region ($V_{DS} < V_{GS} - V_T$), the load device is in saturation nd $I = I_0$ and $V_{OUT} = V_0$. I_0 and V_0 are as follows [1]:

$$I_0 = \frac{K' \left(\frac{W}{L}\right)_L}{2} V_1^2 \qquad (4a)$$

$$I_0 = K' \left(\frac{W}{L}\right)_D (V_1 - V_{TD}) V_0 \qquad (4b)$$

$$V_0 = \frac{I_0}{K' \left(\frac{W}{L}\right)_D (V_1 - V_{TD})} \qquad (5)$$

when $V_{out} = V_1$ $P_{DC} = 0$

$V_{out} = V_0$ $P_{DC} = I_0 V_{DD}$

where V_{DD} = power supply voltage (typically = 5v).

Since $V_1 = V_{DD} - V_{TL}$, the saturated enhancement type MOS load is said to introduce "threshold losses". Equation (5) shows

that V_0 is a function of the operating current I_0. V_0 can be reduced (hence increasing the logic swing and the noise margin NM_0) by increasing the ratio $(W/L)_D$ of the driver transistor. This is shown mathematically by manipulating (4) to obtain:

$$\frac{(W/L)_D}{(W/L)_L} \geq \frac{V_1}{2V_0} \tag{6}$$

The threshold voltage V_t of the inverter is $\geq V_{TD}$ [1]. The higher the ratio $[(W/L)_D/(W/L)_L]$ is, the closer V_t approaches V_{TD}.

Nonsaturated Enhancement-type Load

This type of load operates in the nonsaturation region by connecting its gate to V_{GG} where $V_{GG} > (V_{DD} + V_{TL})$ as shown in Fig. 3(b).

(a) When $V_{IN} = V_0$, $V_0 < V_{TD}$, the driver is off, the load is nonsaturated and $V_{OUT} = V_1 = V_{DD} - V_{DS}|_{load}$ where $V_{DS}|_{load}$ is the voltage drop across the load device. If the inverter is driving only MOS gates, then $V_{DS}|_{load} \approx 0$ and $V_1 \approx V_{DD}$.

(b) When $V_{IN} = V_1$, $V_1 > V_{TD}$, the driver is operating in the nonsaturation region, the load is nonsaturated and $I = I_0$ where

$$I_0 \approx K' \left(\frac{W}{L}\right)_L (V_{GG} - V_{TL}) V_{DD}$$

$$\approx K' \left(\frac{W}{L}\right)_D (V_1 - V_{TD}) V_0 \tag{7}$$

and

$$V_O \approx \frac{I_O}{K'\left(\frac{W}{L}\right)_D (V_1 - V_{TD})} \qquad (8)$$

The improved performance of this load, a higher V_1 and improved noise margins, is obtained at the expense of adding the extra power supply V_{GG}.

Depletion-type Load

This type of load is widely used as loads in NMOS logic circuits. It offers a voltage logic level $V_1 \approx V_{DD}$ and an improved transient performance.

a) When $V_{IN} = V_O$, $V_O < V_{TD}$, the driver is off, the load is nonsaturated and:

$$V_{OUT} = V_1 = V_{DD} - V_{DS}|_{load} \approx V_{DD}$$

b) When $V_{IN} = V_1$, $V_1 > V_{TD}$, the driver is operating in the nonsaturation region, the load is saturated and $I = I_O$, where

$$I_O = \frac{K'\left(\frac{W}{L}\right)_L}{2} V_{TL}^2 \qquad (9)$$

$$= K'\left(\frac{W}{L}\right)_D (V_1 - V_{TD}) V_O$$

and

$$V_O \approx \frac{I_O}{K'\left(\frac{W}{L}\right)_D (V_1 - V_{TD})} \qquad (10)$$

Resistive Load

Polyresistors have been used in the design of NMOS static memories. This type of load provides $V_1 \cong V_{DD}$

a) When $V_{IN} = V_0$, $V_0 < V_{TD}$, the driver is off and

$$V_{OUT} = V_1 = V_{DD} - V_{LOAD} \cong V_{DD}$$

b) When $V_{IN} = V_1$, $V_1 > V_{TD}$, the driver is operating in the nonsaturation and $I = I_0$ where

$$I_0 \cong \frac{V_{DD}}{R}$$

$$\cong K' \left(\frac{W}{L}\right)_D \left[(V_1 - V_{TD}) V_0 - \tfrac{1}{2} V_0^2\right] \qquad (11)$$

$$V_0 \cong \frac{I_0}{K' \left(\frac{W}{L}\right)_D (V_1 - V_{TD})} \qquad (12)$$

Transient Performance

The transient performance of a MOS inverter is a function of [7]:

1. The discharging time t_{dis}, which is the time taken by the output node capacitance C_{OUT} to discharge through the driver transistor, from V_1 to V_0 (Fig. 4).

2. The charging time t_{ch}, which is the time taken by C_{OUT} to charge, through the load from V_0 to V_1 (Fig. 4).

Expressions for t_{dis} and t_{ch} are given in [1]. Typical values for t_{ch} and t_{dis}, assuming $V_{DD} = 5v$, $V_{TD} = 0.5v$ and $K' = 25 \mu A/v^2$, are as follows:

1. $t_{dis} \cong 30$ nsec for $V_1 = 5$, $V_0 = .1v$, $C_{out} = 1_{pf}$ and $(W/L)_D = 1$.

2. For saturated enhancement-type load t_{ch} ≈400 nsec for V_1 = V_{DD} - V_{TL} = 5 - .7 = 4.3v, V_o = 0.1v, C_{out} = 1pf and $(W/L)_L$ = 1.

3. For nonsaturated enhancement-type load t_{ch} = 259 ms [1], for V_{GG} = 6v, V_{TL} = .7, V_1 = 4.9v, V_o = .1v, C_{out} = 1pF and $(W/L)_L$ = 1 if V_{GG} increases, t_{ch} will diminish.

4. For depletion-type load t_{ch} ≈62.7 ns for V_1 = 5v, V_o = 0.1v V_{TL} = -2.5v, C_{out} = 1pF and $(W/L)_L$ = 1.

5. For resistive load t_{ch} = $2.2 R_L C_{out}$, for V_1 = $.9V_{DD}$, V_O = $.1 V_{DD}$, C_{out} = 1pf and R_L = 1KΩ t_{ch} = 2.2ns.

Examining the equations in [1] shows that increasing the size of the transistors, load and driving, improves t_{ch} and t_{dis} respectively. However, by increasing the size of these transistors their loading on previous stages and the output capacitance C_{OUT} increases and the overall delay may not improve [8].

NMOS Delay-Power Tradeoffs

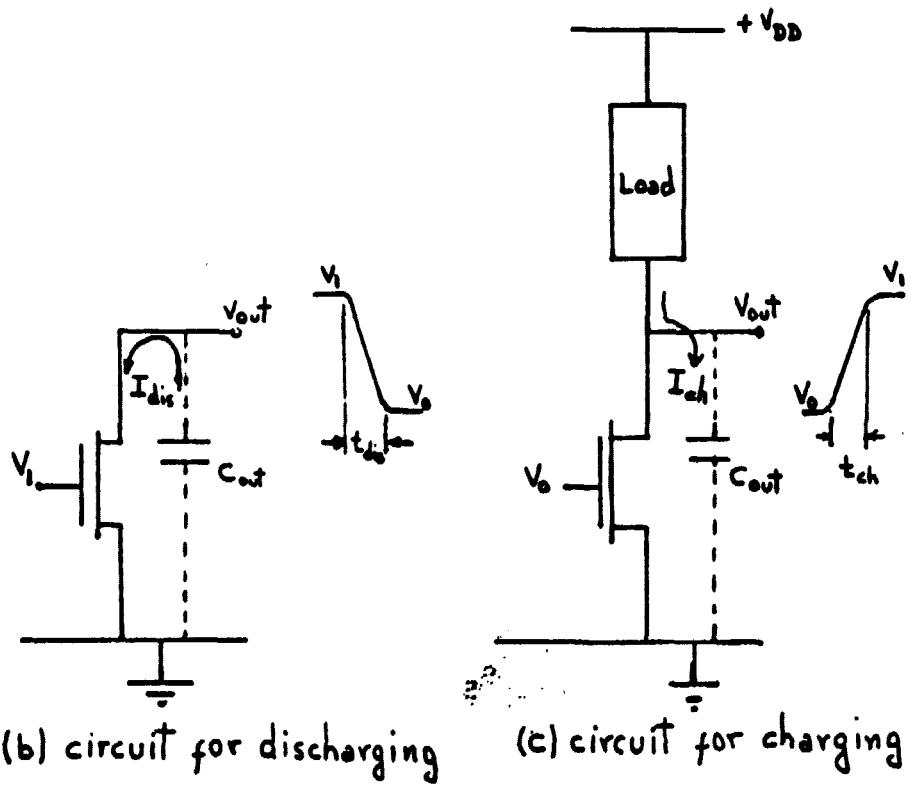The average DC power consumption in a NMOS static inverter is given by:

$$P_{DC}\Big|_{av} = \frac{P_{DC}\Big|_{V=V_1} + P_{DC}\Big|_{V=V_o}}{2} = \frac{0 + I_o V_{DD}}{2} = \tfrac{1}{2} I_o V_{DD}$$

where I_0 is the inverter dc current when the output voltage is low. In addition to this component of power dissipation, there
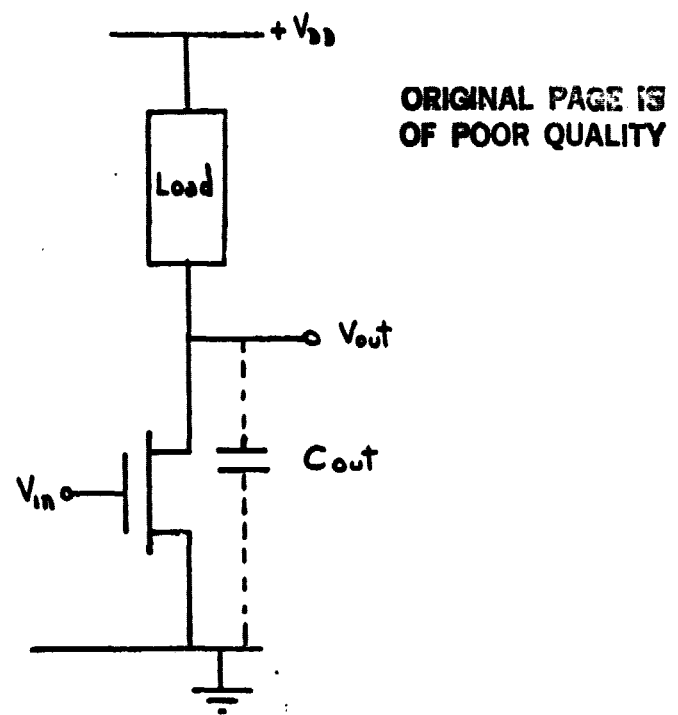
(a) NMOS Inverter

(b) circuit for discharging

(c) circuit for charging

Fig. 4

is a transient power component P_t due to the switching of the output node capacitance C_{OUT}.

$$P_t = C_{OUT} V_{sw} f \qquad (13)$$

where V_{sw} is the logic swing and f is the switching frequency. If $t_{dis} << t_{ch}$ (depletion-type load), the maximum switching frequency $f_{max} \approx 1/t_{ch}$. Thus, the total power dissipation at f_{max} is given by

$$P = \tfrac{1}{2} I_o V_{DD} + \frac{C_{out} V_{sw}}{t_{ch}} \qquad (14)$$

The inverter average delay time τ_D is given by:

$$\tau_D = \frac{t_{ch} + t_{dis}}{2} \approx \frac{t_{ch}}{2} \approx \frac{C_{out} V_{sw}}{2 I_o} \qquad (15)$$

Thus, the delay-power product is given by:

$$\tau_D P = \tfrac{1}{4} I_o V_{DD} V_{sw} + \tfrac{1}{2} C_{out} V_{sw}^2$$

$$= 3/4 \; C_{out} V_{DD}^2 \qquad (16)$$

Therefore the delay-power product is proportional to $C_{OUT} V_{DD}^2$.

1.1.2 Additional Circuit Configurations

Source followers and the push-pull driver are also used in the design of N-MOS digital circuits. Source followers are used to reduce the capacitive loading on a given node while push pull drivers are used to drive high capacitive loads, e.g.,

off-chip loads. Figure 5 shows a static inverter and a push-pull stage. Q_1 is the source follower transistor and it is isolating node 2 from the loading capacitance C_{OUT}. Q_1 and Q_2 operate in the push-pull mode to charge and discharge C_{OUT}. The push-pull operation allows high charging and discharging currents resulting in low switching times.

NMOS transmission gates are used in the design of static and dynamic NMOS digital circuits. It is a symmetrical switch controlled by a voltage applied to its gate. Figure 6 shows a NMOS transmission gate. If the controlling voltage on node 1 is greater than V_T, then nodes 2 and 3 are connected through the on resistance of the NMOS device. If that voltage is less than V_T then the NMOS device is off and nodes 2 and 3 are separated by an open circuit.

1.1.3 Static Logic Gates and Flip-Flops

Logic gates are realized by replacing the driver transistor of the basic inverter with a number of MOS transistors. If they are connected in series, a NAND gate results. If the transistors are connected in parallel, a NOR gate results. Figure 7 shows a NAND gate, NOR gate and a more complex logic gate realized with a series-parallel arrangement.

In designing MOS logic gates, one tries to obtain the same dc and transient performance as that of an inverter. In the case of a NOR gate, a worse situation results if only one of the parallel transistors is on at a given time. Therefore the W/L of
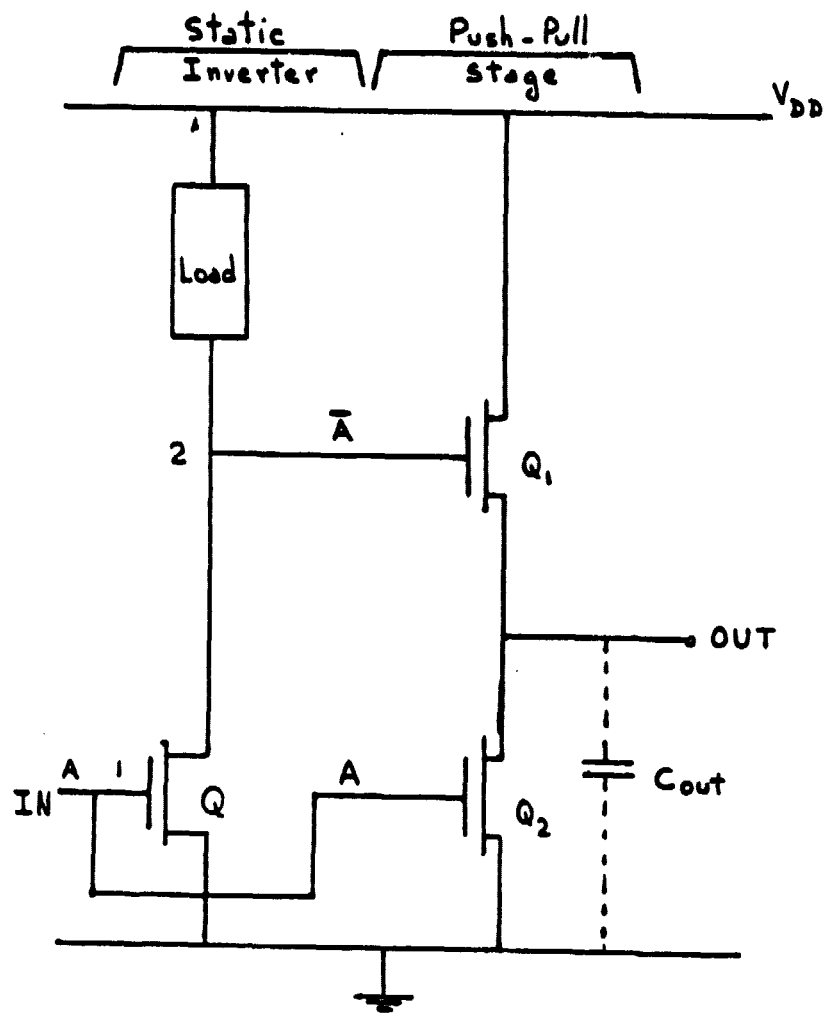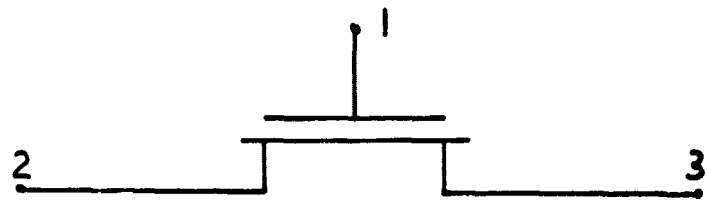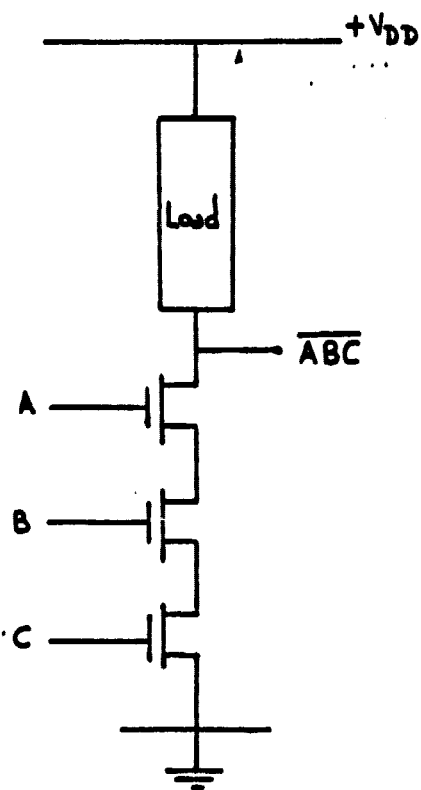
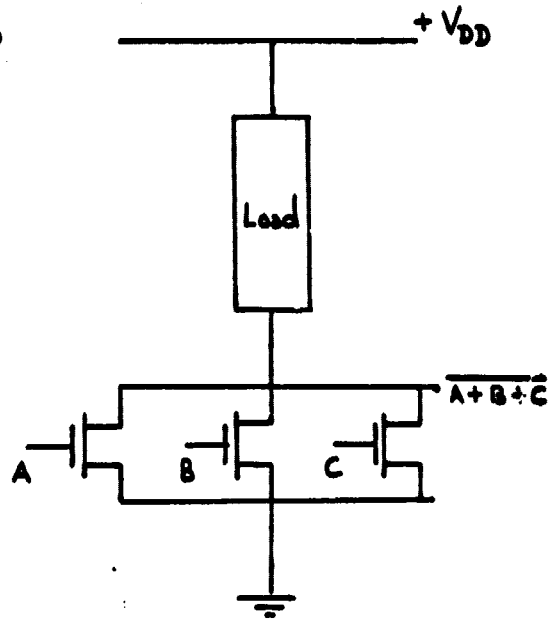Fig. 5   NMOS Push-pull driver

Fig 6.   NMOS transmission gate.

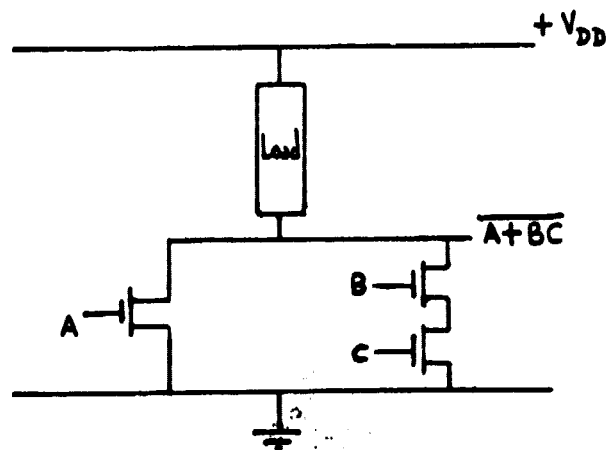(a) NAND gate

(b) NOR gate

(c) a more complex gate.

Fig. 7

the NOR gate drivers is taken to be the same as the $(W/L)_D$ of the inverter driver. In the case of a NAND gate, since the driver transistors are connected in series, the $(W/L)_D$ of the NAND gate drivers is taken to be n times $(W/L)_D$ of the inverter driver (n = number of driver transistors). Consequently, NAND MOS logic gates take more area than NOR gates. On the other hand the n parallel driver transistors of the NOR gate contribute more capacitance to the output node than a single driver. Therefore, if the same transient performance as that of an inverter is required the (W/L) of the load and the driver transistor of the NOR gate has to be increased.

An NMOS static Flip-Flop is shown in Fig. 8. It consists of two inverters connected back to back, and two access transistors Q_3 and Q_4. The circuit has two storage states: (1) V_A is low, V_B is high, Q_1 is on and Q_2 is off; (2) V_A is high, V_B is low, Q_1 is off and Q_2 is on. The state of the flip-flop can be changed by turning on the two access transistors (Q_3 and Q_4), and applying the input and its complement as shown in Fig. 8.

In order to minimize the dc power dissipation of the flip-flop, the load structures are chosen to have high value resistances. The transient performance of the flip-flop is determined by the internal node capacitances C_1 and C_2 and the charging and discharging currents. Most of these currents are provided by the input currents by the input circuits through the access transistors.
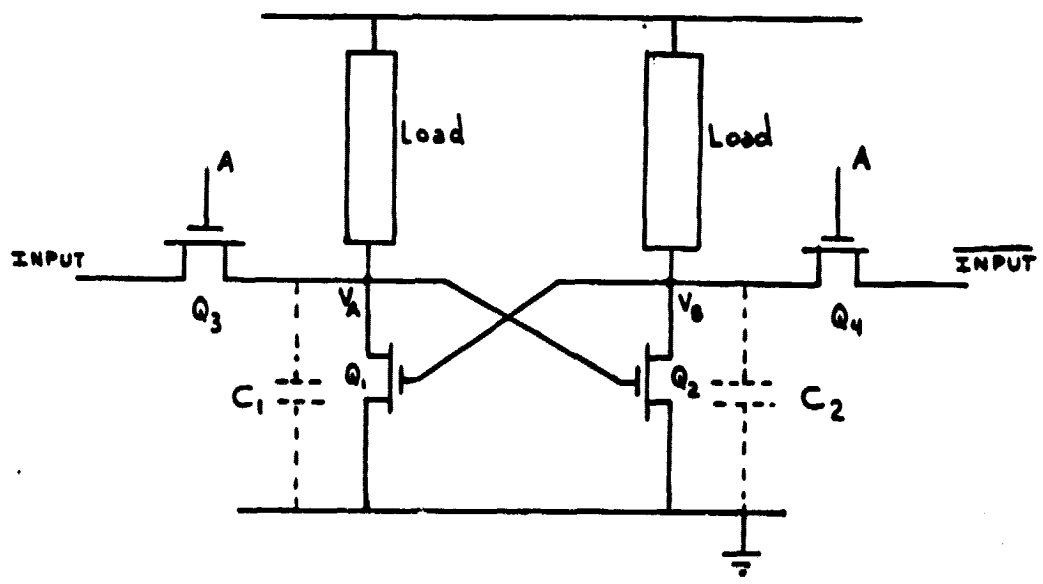
Fig. 8   NMOS static flip-flop

1.1.4 Dynamic MOS Circuits

In general, dynamic MOS circuits offers better performance, consumes less power and occupies a smaller layout area than static MOS circuits. However, dynamic circuits are slower than the static circuits because of the extra time needed to "refresh" the dynamic circuits.

In dynamic MOS circuits, a master clock is used to generate different timing clocks, which are used to control the dynamic operation of the circuit. These clocks are referred to as multiphase clocks [n phase $n\phi$]. The simplest are 2ϕ dynamic circuits but 4ϕ dynamic circuits are commonly used because of practical considerations [5, 9].

Two-Phase (2ϕ) Circuits

Two 2ϕ inverters connected in cascade are shown in Fig 9a, [10]. Each inverter consists of three transistors Q_1, Q_2, and Q_3. Under the control of two nonoverlapping clocks ϕ_1 and ϕ_2, as shown in the timing diagram of fig 9b, three basic operations are performed:

1. Charging a capacitance (C_{OUT}) through a MOS transistor (Q_1) during a first time slot (precharge time: ϕ_1 active).

2. The capacitance C_{out} is discharged through the input transistor Q_2 if the input to Q_2 is "high" or the capacitance C_{OUT} retain its charge if the input to Q_2 is "low".

3. The voltage level on the capacitance C_{OUT} is

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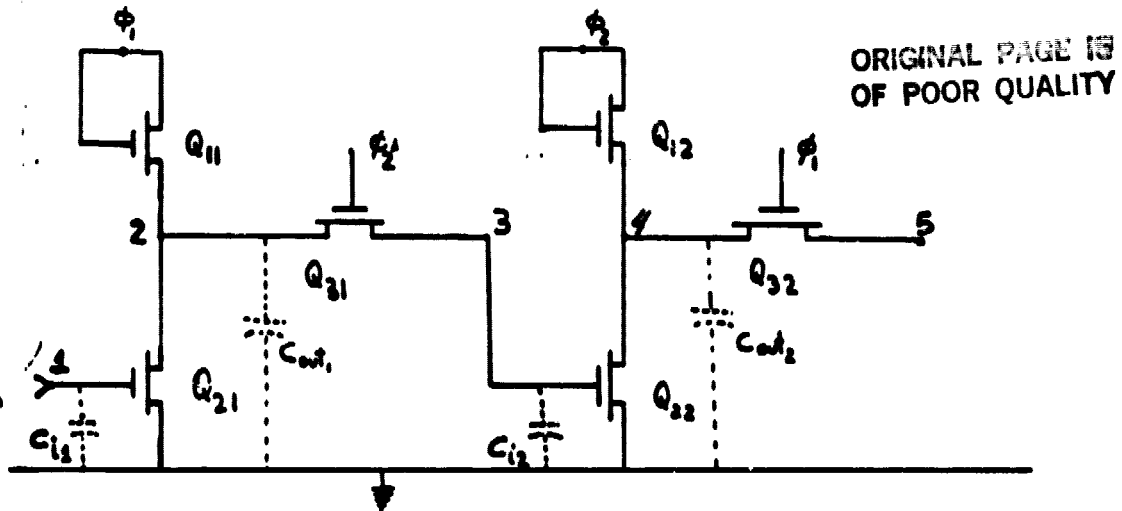
(a) two 2φ inverters connected in cascade
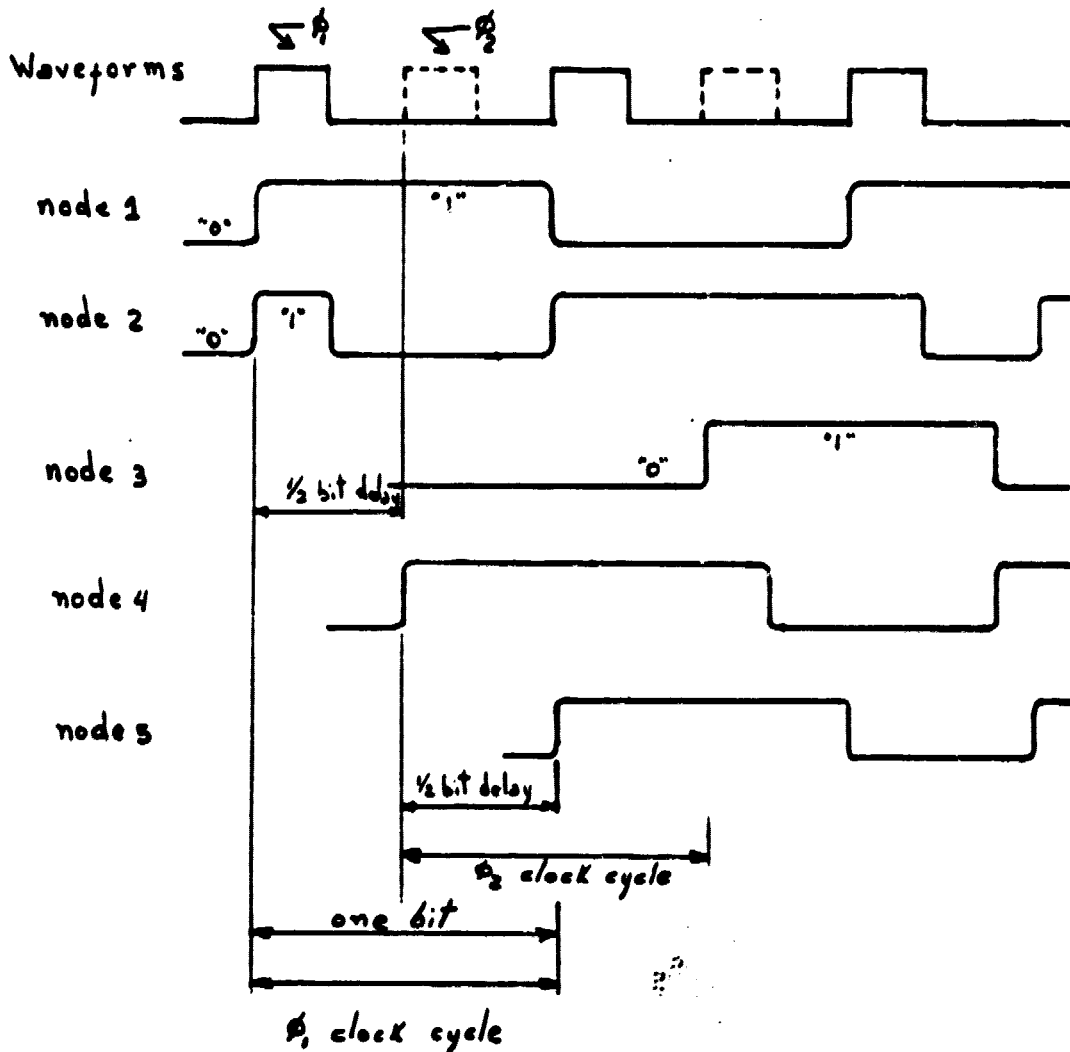
(b) Timing Diagram

Fig. 9

transferred to the input capacitance of the next gate C_1 (sampling time ϕ_2 active).

Figure 10 shows a logic diagram of the two inverters of Fig 9. The first inverter type (ϕ_1/ϕ_2) accepts input at ϕ_1 clock cycles and provides outputs at ϕ_2 clock cycles. The second inverter type (ϕ_2/ϕ_1) accepts input at ϕ_2 clock cycles and provides output at ϕ_1 clock cycles. Consequently, two inverters of the same type cannot be successively connected.

A NAND gate is realized by replacing Q_2 with a series combination of transistors. A NOR gate results if a parallel combination of transistors replaces Q_2. Flip-flops can be realized using such 2 ϕ gates. Figure 11 shows some examples of flip-flops realization.

Four Phase (4 ϕ) Circuits

One disadvantage of 2 ϕ MOS dynamic circuits is the reduction of the voltage representing each logic level during the transfer operation through the transmission gate. This can be overcome by using more than two clocks to control the dynamic operation of the circuits.

Figure 12a shows four 4 ϕ inverters connected in cascade. They are of four types and use 4 ϕ overlapping clocks as shown in the timing diagram of Fig 12b. With reference to the timing diagram, C_1 and C_2 precharge during the time slot 1. During time slot 2, C_1 discharges if IN = "High" or retains its charge if IN = "Low". In this same time slot, the voltage level on C_1 is transferred to the input capacitance of the next inverter. The
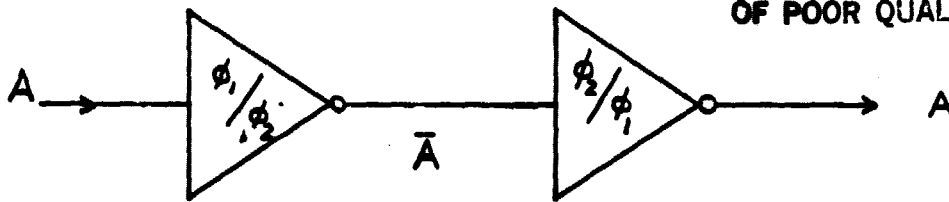
Fig.10. Logic diagram of 2ϕ inverters

Fig.11. Dynamic 2ϕ flip-flops
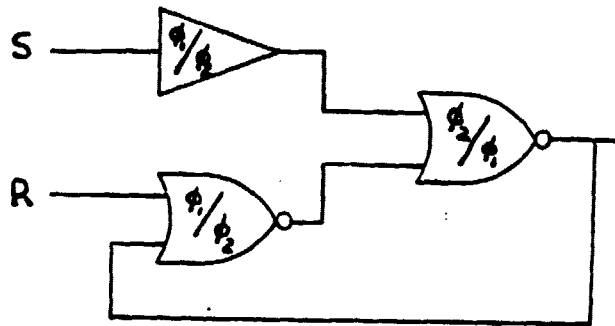
(a) RS Flip-Flop (set dominant)
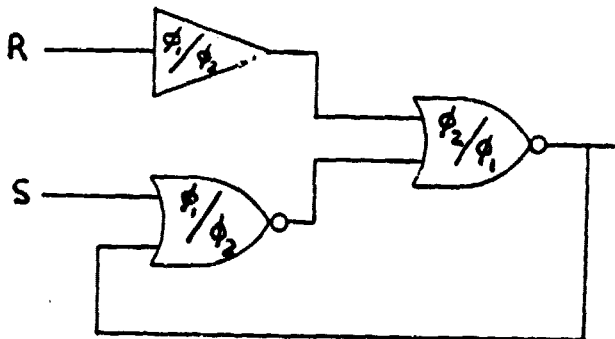
(b) RS Flip-Flop (Reset dominant)
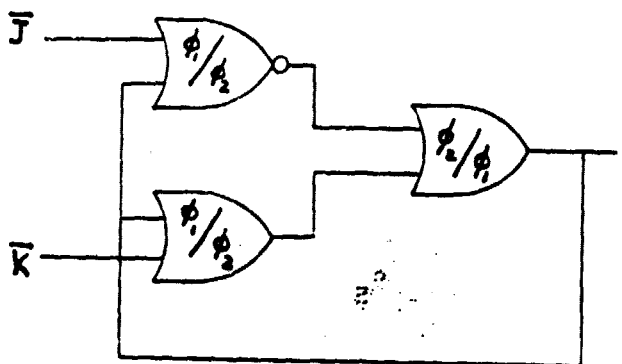
(c) J-K Flip-Flop

timing diagram of Fig. 12b illustrates the operation of this dynamic circuit.

Four-phase NOR circuits are realized by replacing the input transistor Q_{23} with transistors connected in parallel. Four-phase flip-flops are realized using 4ϕ logic gates in a manner similar to the realization of 2ϕ flip-flops using 2ϕ logic gates.

Maximum Frequency of Operation

If τ_1 and τ_2 are the worst case charging and discharging times of the output node capacitances then

$$f_{max} = \frac{1}{K(\tau_1+\tau_2)} \qquad (17)$$

where K is a factor that depends on the clocking scheme. For example K=2 for the two-phase nonoverlapping clock of Fig.9

Minimum Frequency of Operation

The voltage level on a capacitance will deteriorate as the charge in the capacitance starts to leak. Therefore the clock frequency has to be higher than a certain minimum f_{min}, at which ΔV is the allowable deterioration in the high logic level. In a 2ϕ nonoverlapping logic system

$$f_{min} = \frac{I_\ell}{2\Delta V \cdot C} \qquad (18)$$

where I_ℓ is the leakage current at the node and C is the node capacitance.
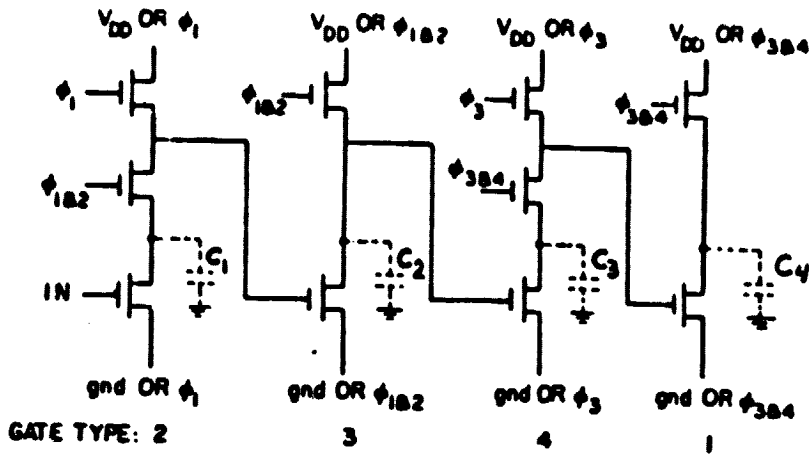
(d) Four 4φ inverters connected in cascade
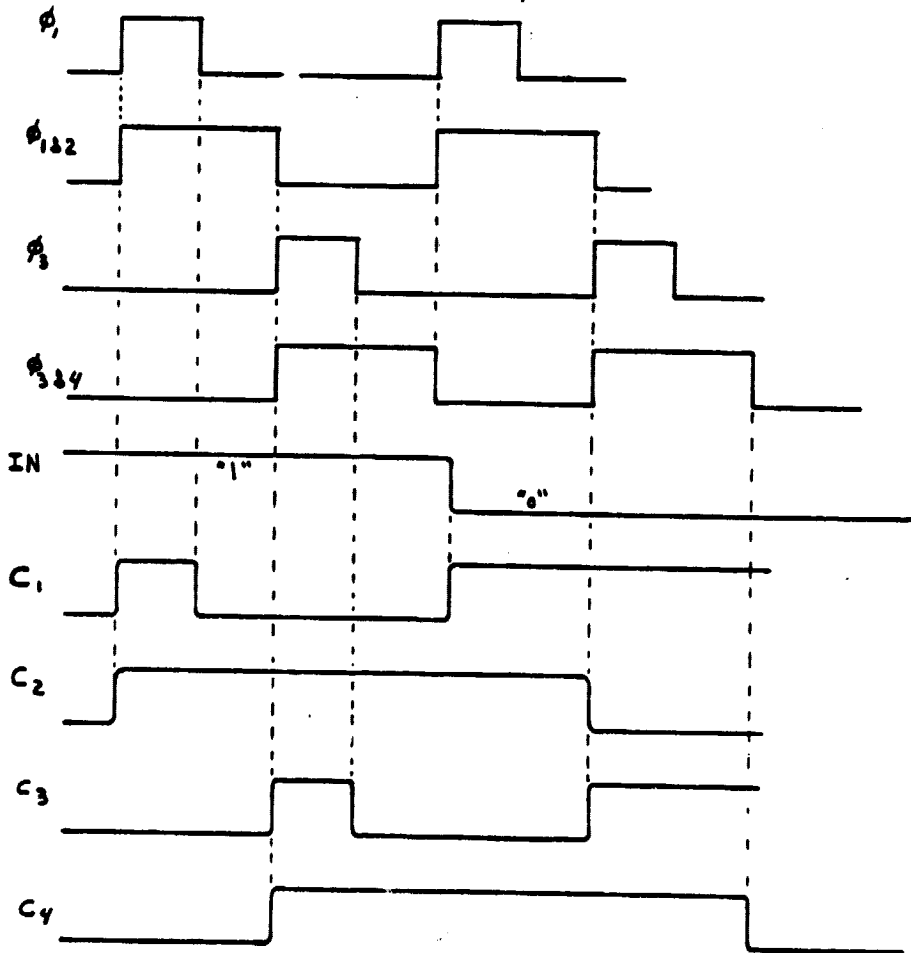
(b) Timing diagram

Fig. 12

1.1.5 Complementary MOS Circuits (CMOS)

An n-channel MOS driver and a p-channel MOS as a load comprises the basic CMOS inverter, as shown in Fig. 13a. CMOS circuits can be fabricated using P-well, N-well or twin-tub CMOS technologies [11]. Figure 13b shows a cross-section of NMOS and PMOS devices in a P-well CMOS technology. Figure 13b also shows the following parasitic diodes: D_1 is the substrate-source/drain junction diode, D_2 is the well-source/drain junction diode, and D_3 is the well substrate junction diode. The three diodes make up a three junction thyrister (SCR) and during circuit operation it may latch-up (SCR turns on). Techniques used to minimize this hazardous circuit operation are presented in [12] and [13].

The CMOS Static Inverter

Figure 14 shows the transfer characteristic and the current I as a function of the input voltage V_{in}. The basic inverter operation is as follows:

1. If V_{in} is a logic "0" (i.e. $V_{in} = V_0$, $V_0 < V_{TN}$, where V_{TN} is the threshold voltage of the n-channel transistor Q_N), Q_N is off. If $V_{in} - V_{DD} < V_{TP}$, where V_{TP} is the threshold voltage of the p-channel transistor Q_P, then Q_P is on. The output voltage V_{OUT} ($V_{OUT} = V_1$) is given by

$$V_{OUT} = V_1 = V_{DD} - V_P \qquad (19)$$

where V_P is the voltage drop across Q_P and is given by

$$V_P = I_P R_P = I_P \frac{1}{\beta_P [(V_{DD} - V_0) - |V_{T_P}|]} \qquad (20)$$
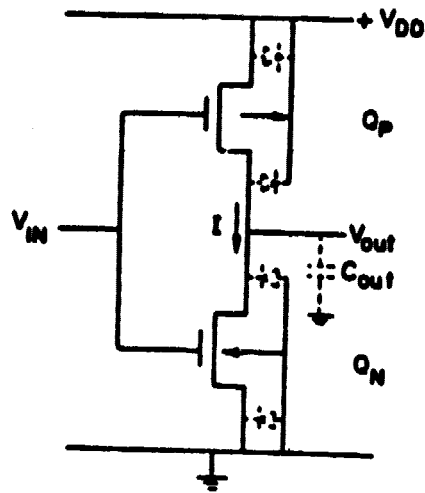
(a) Circuit of a CMOS inverter
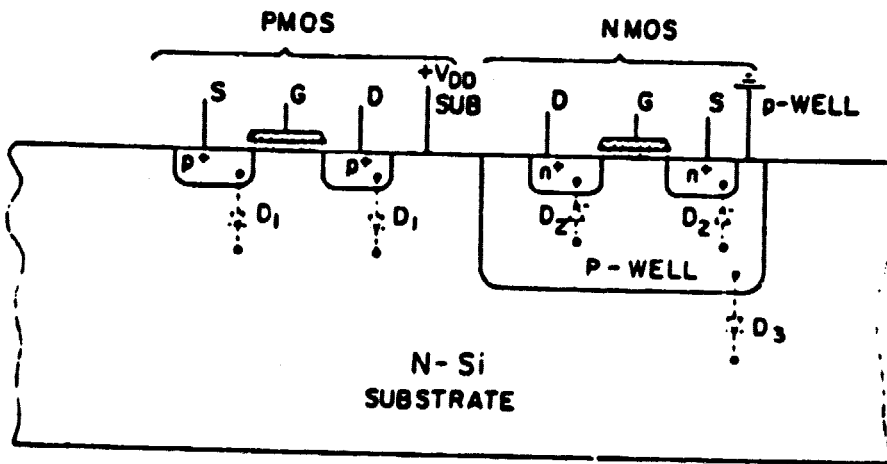
(b) Cross-section in a P-well CMOS

Fig. 13

Transfer Characteristic   I vs. V_{IN}

Fig. 14

NAND

$F = \overline{X_1 \cdot X_2}$
$F = \overline{X_1} + \overline{X_2}$
$\overline{F} = X_1 \cdot X_2$

NOR
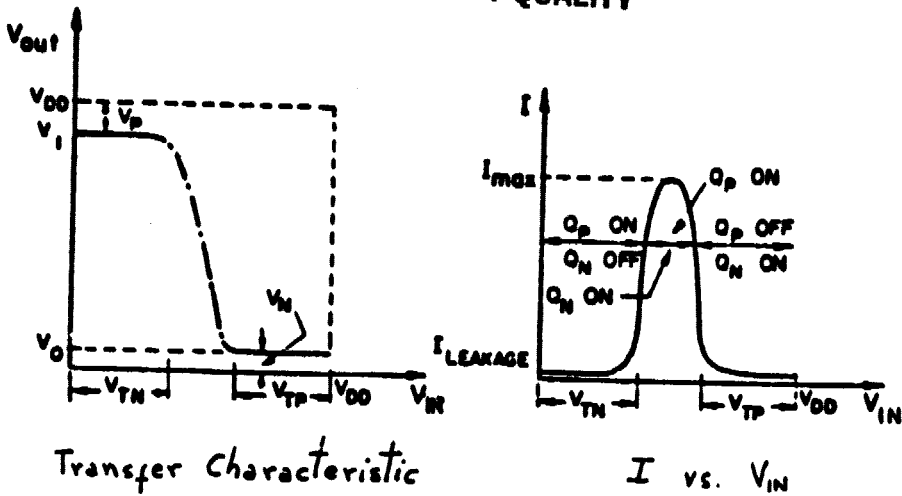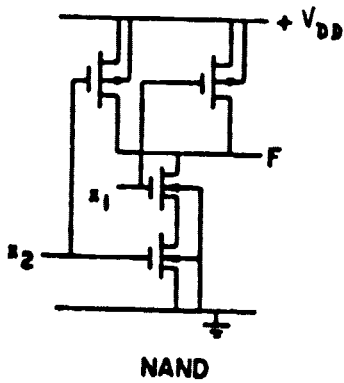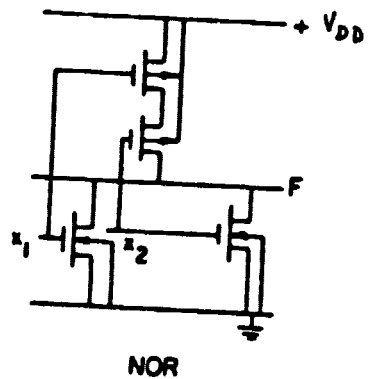
$F = \overline{X_1 + X_2}$
$F = \overline{X_1} \cdot \overline{X_2}$
$\overline{F} = X_1 + X_2$

Fig. 15

where I_P is the current supplied by Q_P to Q_N and to the loads. If the inverter is driving MOS gates, I_P is negligible and $V_1 \approx V_{DD}$. If I_P is not negligible, then by increasing $\beta_P (\frac{W}{L} K')$ it is possible to achieve $V_P \ll V_{DD}$ and, hence, $V_1 \approx V_{DD}$.

2. If V_{IN} is a logical "1" (i.e. $V_{IN} = V_1$, $V_1 > V_{TN}$ then Q_N is on. If $V_1 - V_{DD} > V_{TP}$ then Q_P is off. The output voltage is given by

$$V_{OUT} = V_0 = V_N \tag{21}$$

where V_N is the drop across Q_N and is given by

$$V_N = I_N R_N \approx I_N \frac{1}{\beta_N (V_1 - V_{TN})} \tag{22}$$

where I_N is the current sunk by Q_N from Q_P and from the loads. If the loads are MOS gates then I_N is a leakage current and $V_N \approx 0$ volts. However, if the loads are bipolar circuits, I_N wold be considerable. In this case $V_N = V_0$ can be reduced by increasing β_N.

Since the logic levels can be made close to V_{DD} and ground, the logic swing V_ℓ is of the order of V_{DD}. If symmetrical devices are used, i.e. $\beta_N = \beta_P$, then the threshold voltage of CMOS logic gate V_T is close to $V_{DD}/2$. Therefore, equal noise margins result which are $\approx V_{DD}/2$.

The D.C. power dissipation is a negligible component of the total power dissipation and is given by

$$P_{DC} = V_{DD} I_{leakage} \tag{23}$$

Transient Analysis

The transient parameters of interest are the charging time, the discharging time and the delay through a CMOS inverter τ_D.

The discharging time, t_{dis}, is the time taken for the output capacitance C_{OUT} to discharge through Q_N from an output logic level of $V_1 = V_{DD}$ to an output logic level of $V_O = 0$. It is given by

$$t_{dis} = \tau_N \left[\frac{2}{\frac{V_{DD}}{V_{T_N}} - 1} + \ln \left(\frac{2(V_{DD} - V_{TN})}{V_O} - 1 \right) \right] \tag{24}$$

where

$$\tau_N = \frac{C_{out}}{g_{mN}} = \frac{C_{out}}{\beta_N (V_{DD} - V_{TN})} \tag{25}$$

The charging time, t_{ch}, is the time taken for C_{out} to charge through Q_P from V_O to V_1 and it is given by

$$t_{ch} = \tau_P \left[\frac{2}{\frac{(V_{DD})}{|V_{TP}|} - 1} + \ln \left(\frac{2(V_{DD} - |V_{TP}|)}{V_{DD} - V_1} - 1 \right) \right] \tag{26}$$

where

$$\tau_P = \frac{C_{out}}{g_{mP}} = \frac{C_{out}}{\beta_P (V_{DD} - |V_{TP}|)} \tag{27}$$

The delay through a CMOS inverter τ_D is defined as the delay time between the input and the output waveforms measured at

the $V_{DD}/2$ points for a chain of CMOS inverters or a ring oscilator. This is given by [14]:

$$\tau_D \approx \frac{0.9\ C_{out}}{V_{DD}\ \beta_N} \left[\frac{1}{\left(1 - \frac{V_{TN}}{V_{DD}}\right)^2} + \frac{1}{\frac{\beta_P}{\beta_N}\left(1 - \frac{|V_{TP}|}{V_{DD}}\right)^2} \right] \quad (28)$$

if $(V_{TN}/V_{DD}) << 1$ and $(|V_{TP}|/V_{DD}) << 1$ then:

$$\tau_D \approx \frac{.9\ C_{out}}{V_{DD}\ \beta_N} \left(1 + \frac{\beta_N}{\beta_P}\right) \quad (29)$$

which shows that τ_D is linearly proportional to (C_{out}/V_{DD}).

For $V_{DD} = 5v$, $K' = 25\mu A/v^2$, $\beta_N = \beta_P$ results in $t_{ch} = t_{dis} = 30$ nsec and $\tau_D = 14.4$ nsec for a $C_{OUT} = 1pF$ and a $(W/L)_N = 1$. This compares favorably with the corresponding transient performance of NMOS circuits.

Transient Power Dissipation

The transient power dissipation of a CMOS inverter has two components. The first results from charging and discharging the output capacitance through the finite on-resistance of Q_N and Q_P. This component is given by:

$$P_{t_1} = C_{out}\ V_\ell^2\ f \quad (30)$$

where C_{out} is the total output-node capacitance, V_ℓ is the logic

swing of the gate, and f is the frequency of switching. The second component is due to the fact that the input (and hence the output) voltage waveforms have finite rise and fall times. Therefore current has to be supplied to the inverter circuit during these times, resulting in a power dissipation P_{t_2} which is given by:

$$P_{t_2} = V_{DD} I_{av} \qquad (31)$$

where $I_{av} = \frac{1}{2} I_{max} \dfrac{V_{DD} - (V_{TN} + |V_{TP}|)}{V_{DD}} \quad \dfrac{t_1 + t_2}{\tau}$

$$I_{max} = \frac{V_{DD}}{R_N + R_P} \quad \text{and} \quad \begin{aligned} t_1 &= \text{rise time} \\ t_2 &= \text{fall time} \end{aligned}$$

$$\tau = 1/f$$

However, if t_1 and $t_2 << 1/f$ then $P_{t_2} << P_{t_1}$.

Delay-Power Trade-Offs

Since the main component of power dissipation is P_{t1}, the total power dissipation at the maximum frequency of operation is given by:

$$P = \frac{C_{out} V_\ell^2}{2 \, \tau_D} \qquad (32)$$

where τ_D is the delay time. The delay-power product is given by:

$$\tau_D P = .5 \, C_{out} V_\ell^2 = .5 \, C_{out} V_{DD}^2 \qquad (33)$$

This shows that the delay-power product is proportional to $C_{out} V_{DD}^2$.

1.1.6 CMOS Static Gates

Figure 15 shows a two-input NAND and a two-input NOR. Each input requires a complementary pair. In the case of a NAND gate the n-channel devices are connected in series while the p-channel devices are connected in parallel. But in the case of a NOR gate the n-channel devices are connected in parallel while the p-channel devices are connected in series.

The design of a CMOS logic gate follows that of an inverter. First, an inverter is designed to meet a given dc and transient performance, and $(W/L)_N$ and $(W/L)_P$ are determined. Then $(W/L)_N$ and $(W/L)_P$ of the devices of a logic gate are determined as follows. If a CMOS m-input NAND gate is to be designed to have the same dc and transient performance as that of the inverter, then for the same values of C_{OUT}: $(W/L)_P$ of the NAND gate devices should be ≥ $(W/L)_P$ of the inverter while $(W/L)_N$ should be ≥ m $(W/L)_N$ of the inverter. On the other hand, if a CMOS m-input NOR gate is to be designed to have the same dc and transient performance as that of the inverter, then for the same values of C_{OUT}, $(W/L)_P$ of the NOR gates should be ≥ m $(W/L)_P$ of the inverter, while $(W/L)_N$ should be ≥ $(W/L)_N$ of the inverter. The increase in the size of the NMOS devices in the case of the NAND gate and the increase in the size of the PMOS devices in the case of the NOR gate allows the logic levels V_0 and V_1 to be the same as that of the inverter even if the dc currents are nonzero. CMOS NAND gates are more widely used than NOR gates because a NAND gate consume less silicon area than that of a NOR gate.

This is due to the fact that NMOS devices occupy smaller areas than PMOS devices.

1.1.7 CMOS Transmission Gates

As in the case of NMOS transmission gates, a CMOS transmission gate acts as a switch. It consists of a complementary pair connected in parallel. Figure 16 shows such a gate with the logical variable A as the control input. If A is high, the gate is on and acts as a switch with an ON resistance of R_N and R_P in parallel. If A is low, the gate is off and presents a high resistance between the input and output terminals.

The advantage of using a complementary pair, rather than a single NMOS or PMOS device to realize a transmission gate is that the gate delay time is almost independent of the voltage level of the input variable of the CMOS transmission gate. On the other hand a CMOS transmission gate comsumes more area than a single-channel transmission gate. Thus, if the area is of prime concern, non complementary n-channel transmission gates are used.

1.1.8 CMOS Static Flip-Flops

Figure 17 shows a cross-coupled CMOS static flip-flop. It consists of two inverters and two transmission gates. In one of the states V_A is high, V_B is low, Q_1 and Q_4 are on while Q_2 and Q_3 are off. In the other state V_A is low, V_B is high, Q_1 and Q_4 are off while Q_2 and Q_3 are on. The state of the flip-flop is changed by using the two CMOS transmission gates connected to V_A and V_B nodes as shown in Fig 17.
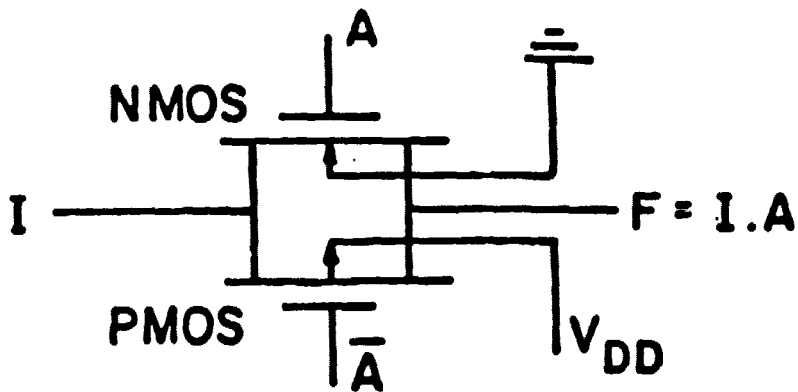
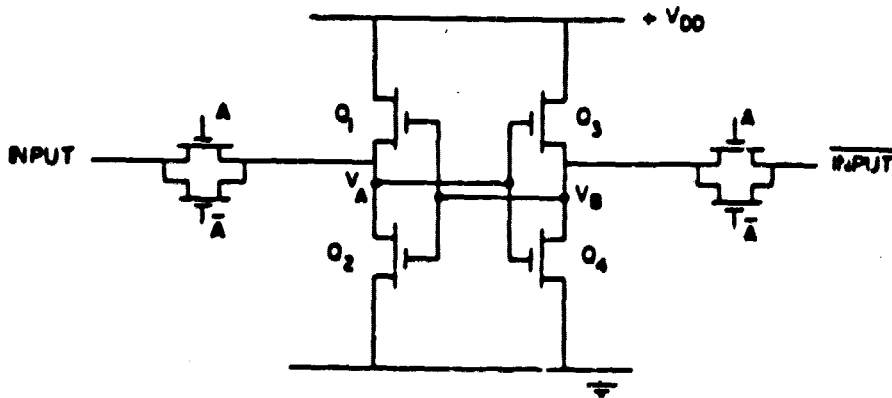Fig. 16   A CMOS transmission gate

Fig 17   A CMOS static flip-flop

A D-type CMOS master-slave static flip-flop is shown in Fig 18a. The master and the slave sections require the presence of a clock to latch up and store the information. Figure 18c shows the flip-flop timing diagram.

1.2 Noise Behavior of MOS Devices

Noise performance is a more important problem in MOS analog circuits than in bipolar circuits simply because the MOS device tends to be noisier than the bipolar device, particularly at low frequencies.

The noise associated with MOS transistors can be split into two parts: thermal noise and 1/f noise. Shot noise does not occur in the MOS device because there are not minority carrier which must jumpt a barrier through a thermal process.

The thermal noise of the MOS transistor arises because of the finite resistance of the channel of the transistor. The flicker noise, or 1/f noise, arises from the presence of extra electron energy states at the boundary between the bulk silicon and the silicon dioxide dielectric. Because of the location of these states in the band gap, they charge and discharge relatively slowly, giving rise to the concentration of the associated noise at low frequencies.

The equivalent input noise voltages can be one to two orders of magnitude larger than in bipolar circuits. This can be reduced by using a large gate area for the input devices [18].
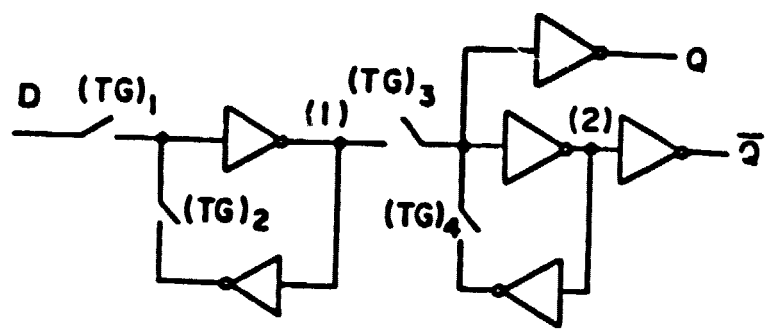
(a) Logic diagram
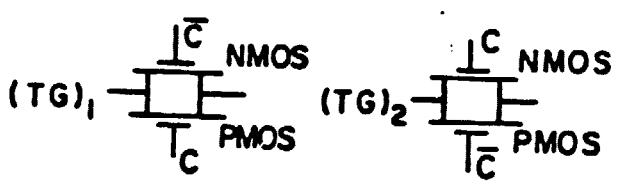
(b) Transmission gates $(TG)_{1,2}$
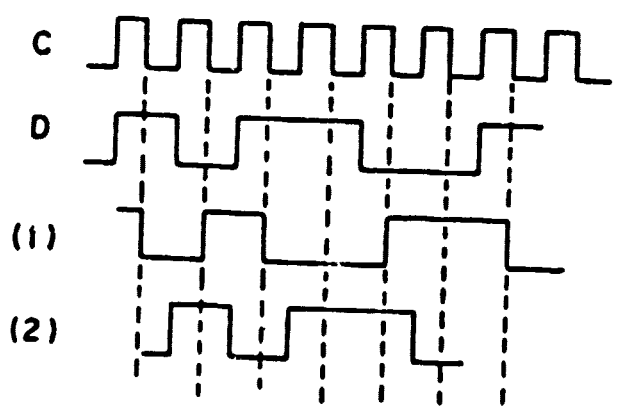
(c) Timing diagram

Fig 18 D-type CMOS master-slave static flip-flop

1.3 Analog MOS Integrated Circuits

The basic dc model and nomenclature used for the MOS transistor was presented in the section "Digital MOS integrated circuits" (p. 1). In all the analog cells presented in this section, the transistors operate in the saturation region. Therefore, operation in this region is assumed for all the results that follow [15].

1.3.1 NMOS Characteristics

Small Signal Characteristics

The change in I_D to V_{GS} is defined as the transconductance g_m and is defined as:

$$g_m \equiv \frac{\partial I_D}{\partial V_{GS}} = \frac{\partial [V_{GS}-V_T]^2}{\partial V_{GS}} \qquad (34a)$$

$$= \frac{2 I_D}{V_{GS}-V_T} \qquad (34b)$$

The transconductance of MOS transistors is much lower than that of bipolar transistors. This is one of the main problems in analog MOS design since it results in a limited voltage gain.

The small-signal model for the MOS transistor in the saturation r jion is shown in Fig. 19, where C_{gd} is the gate-to-drain capacitance, C_{gs} is the gate-to-source capacitance, C_{db} is the drain-to-substrate capacitance, and C_{sb} is the source-to-substrate capacitance. r_{ds} represents the nonzero slope of the I_D-V_{DS} curves and g_{mb} is a transconductance due to the dependence of the threshold voltage V_T on the substrate-to-source voltage [17].

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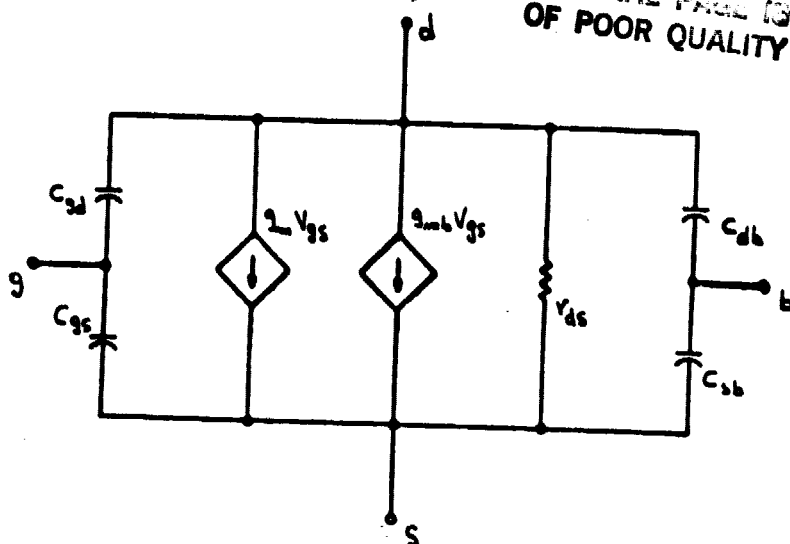
Fig. 19 Small-signal equivalent circuit
for the MOS transistor
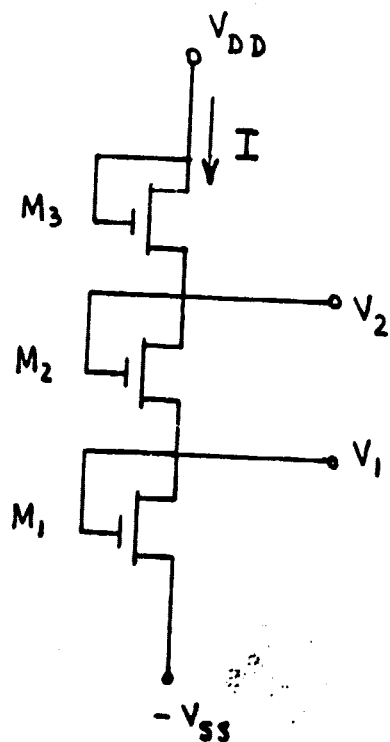
Fig. 20 Voltage divider

1.3.2 NMOS Circuits

In NMOS technology, the lack of availability of complementary transistors and suitable resistors limits the designer's flexibility. For example, the design of operational amplifiers in NMOS depletion load technology is considerably more difficult because of a lack of a complementary device.

Voltage divider- A voltage divider is shown in Fig. 20 . At low frequency and negligibly large r_{ds}, the device behaves like a resistor of value $1/g_m$. A draw-back of this configuration is that the current increases rapidly with increasing power-supply voltages.

Current sources- The design of NMOS current sources follows from n-p-n bipolar current sources. Figure 21 shows a curent source. The small-signal output resistance V_o is equal to r_{ds3} and can be increased by increasing the gate length to reduce channel-length modulation. The current I_o depends on $V_{DD} + V_{SS}$.

Inverters- A simple inverter is shown in Fig. 22 . The low-frequency gain of the inverter is given by

$$A = -\alpha_2 \frac{g_{m_1}}{g_{m_2}} \quad , \quad \alpha_2 \leqslant 1 \quad\quad (35a)$$

where $\alpha \triangleq \frac{1}{1+\lambda}$ and $\lambda \triangleq \frac{\gamma}{2\sqrt{-V_{BS}+2\phi_F}}$

ϕ_F is the Fermi potential and γ is given by

$$= \frac{\sqrt{2\,\epsilon_s\,N_A}\,q}{C_o}$$
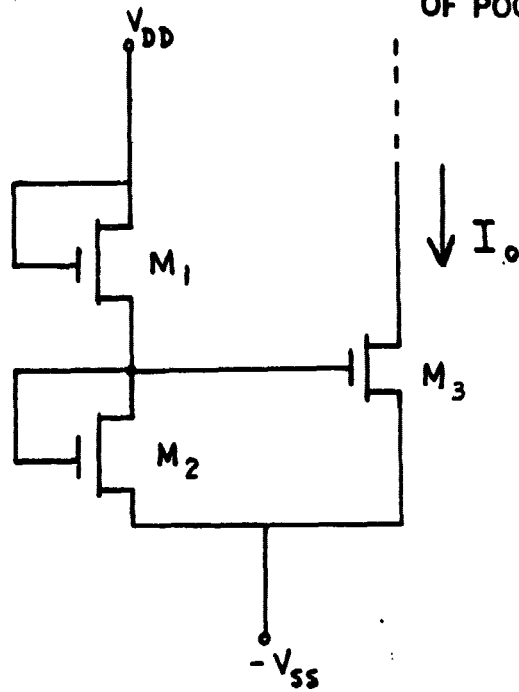
Fig. 21 Current source
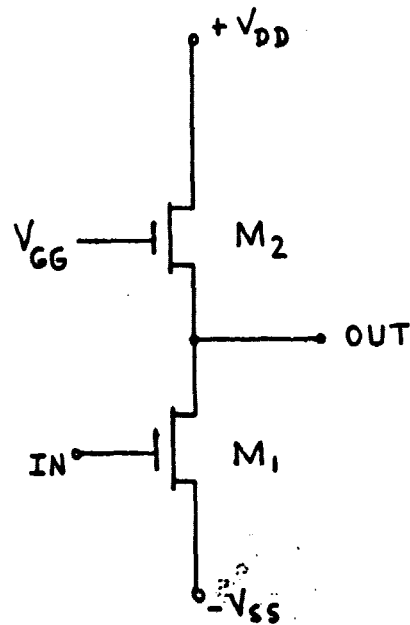
Fig 22 Inverter circuit

Here ε_s is the permitivity of S_1, q the electron charge, N_A the substrate impurity concentration and C_{OX} the gate oxide capacitance per unit area.

The gain of the inverter stage can also be written as:

$$A = -\alpha_2 \sqrt{\frac{(W/L)_1}{(W/L)_2}} \qquad (35b)$$

or

$$A = -\alpha_2 \left[\frac{V_{GS_2} - V_{T_2}}{V_{GS_1} - V_{T_1}} \right] \qquad (35c)$$

If the substrate effect can be neglected ($\alpha = 1$), then the gain becomes purely geometry dependent as can be seen from Eq. (35b).

Cascode Stage – Due to the capacitance C_{gd} an inverter can present a significant load to the stage driving it (Miller effect). In order to eliminate this problem, a cascode stage can be used, as shown in Fig. 23 [15].

Differential Stages [19] – A differential stage is shown in Fig 24. If $(W/L)_1 = (W/L)_2 = (W/L)_3 = (W/L)4$, the differential gain is:

$$A_{d_m} = -\alpha_3 \frac{g_{m_1}}{g_{m_3}} \qquad (36)$$

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The common mode gain is

$$A_{c_m} = - \frac{\alpha_1 \alpha_3}{2 r_{ds_5} g_{m_3}} \qquad (37)$$

Source followers – A source follower stage is shown in Fig 25. The gain voltage is less than unity, even with infinite small-signal load resistance, due to the body effect [15].
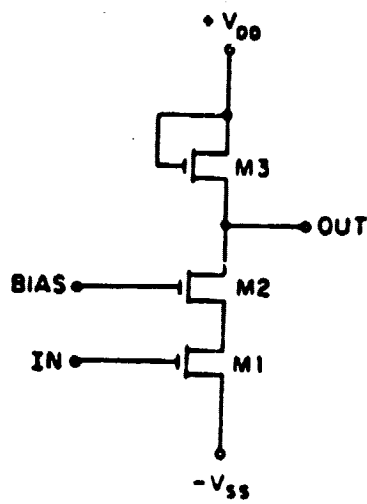
Fig. 23   Cascode stage
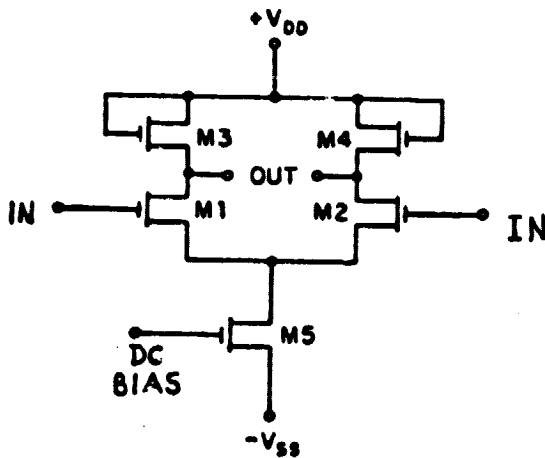
Fig. 24   Differential stage

1.3.3 CMOS

The availability of complementary devices in CMOS, makes the task of the circuit designer easier than designing with single channel MOS devices. For example, the design approaches to the realization of operational amplifiers in CMOS are very similar to those used in bipolar technology. So, the same basic circuit configuration used in bipolar technology is used in CMOS technology [16].

Basic Building Blocks

The CMOS Inverter - The most useful form of CMOS inverter is shown in Fig. 26. It consists of a common-source amplifier with a current source load. m_2 and m_3 form the current source, in which the current source current is determined by the current in the resistor R_1. A DC transfer characteristic is shown in Fig 27. The condition which provides useful voltage gain is that in which both transistors m_1 and m_2 are in the saturated region.

The small-signal voltage gain is the transconductance of m_1 multiplied by the effective output resistance of m_1 and m_2 in parallel [16] and is given by:

$$A_V = \frac{1}{\sqrt{I_D}} \frac{1}{\lambda_1 + \lambda_2} \sqrt{2 \mu C_o (W/L)_1} \qquad (38)$$

as we can see, higher voltage gains are achieved at low values of drain current. However, for a sufficiently low value of I_D, the
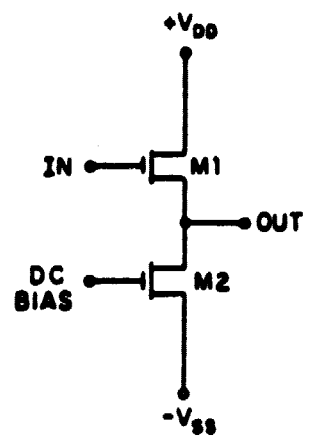
Fig. 25 Source follower stage
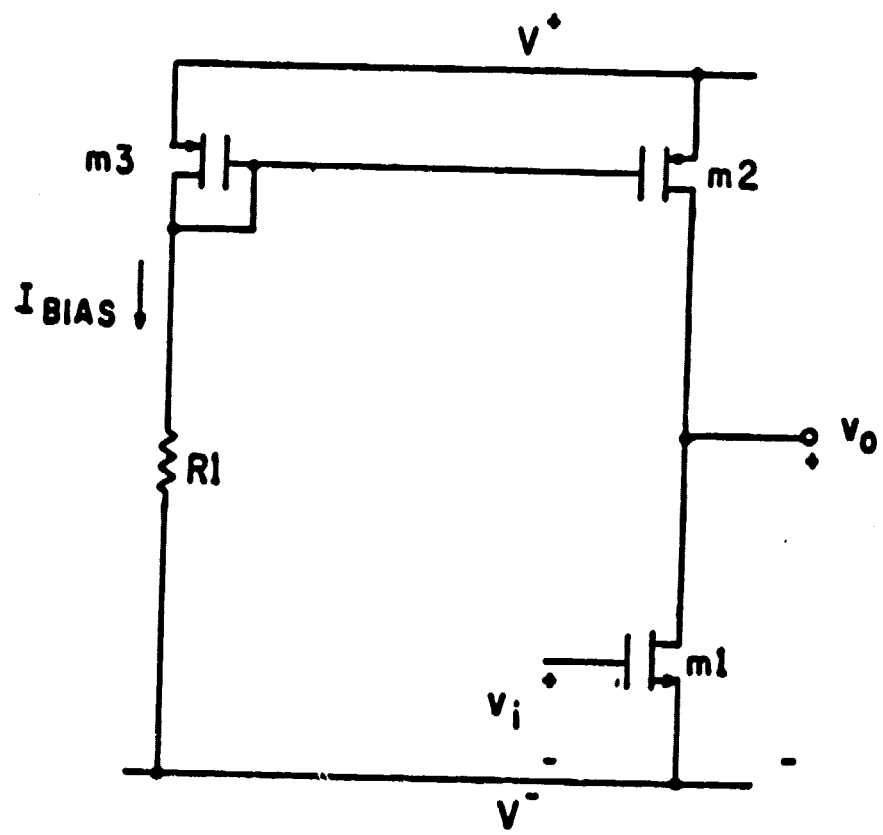
Fig. 26 CMOS inverter with current source load

devices enter the subthreshold region of operation and the voltage gain takes on a constant value. The maximum voltage gain depends on the geometry of the devices and it can lie in the range of several hundred to several thousand.

Difference amplifier- a difference amplifier is shown in Fig. 28. m_1 and m_2 are the differential input devices m_3 and m_4 are the load (current mirror). The gain is given by:

$$A_v = g_{m1} \ (r_{02} // r_{o4}) \qquad\qquad (39)$$

where $g_{m1} = g_{m2}$ and r_o is the output resistance.

Output buffers- As in the case of the bipolar circuits we would have class A and class B operation with CMOS devices. The main drawback of the CMOS devices is that the output resistance is rather high. In order to reduce the output resistance of the buffer an NPN transistor is generally used. This greatly reduces the output resistance since the transconductance of the NPN transistor is much larger than the source follower transistor in the MOS transistor version. Figure 29a and 29b show a source follower output buffer and the improved version. Both of them are class A output buffers.

1.4 Mos Technologies

The oxide-isolated, depletion-load NMOS technology has
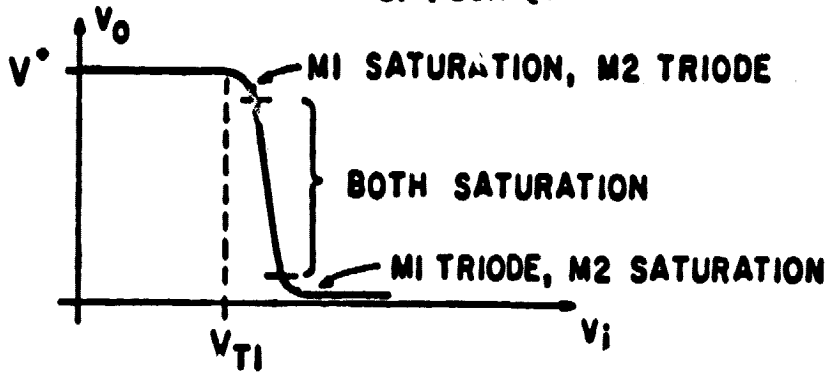
Fig. 27 DC transfer characteristic of the CMOS inverter
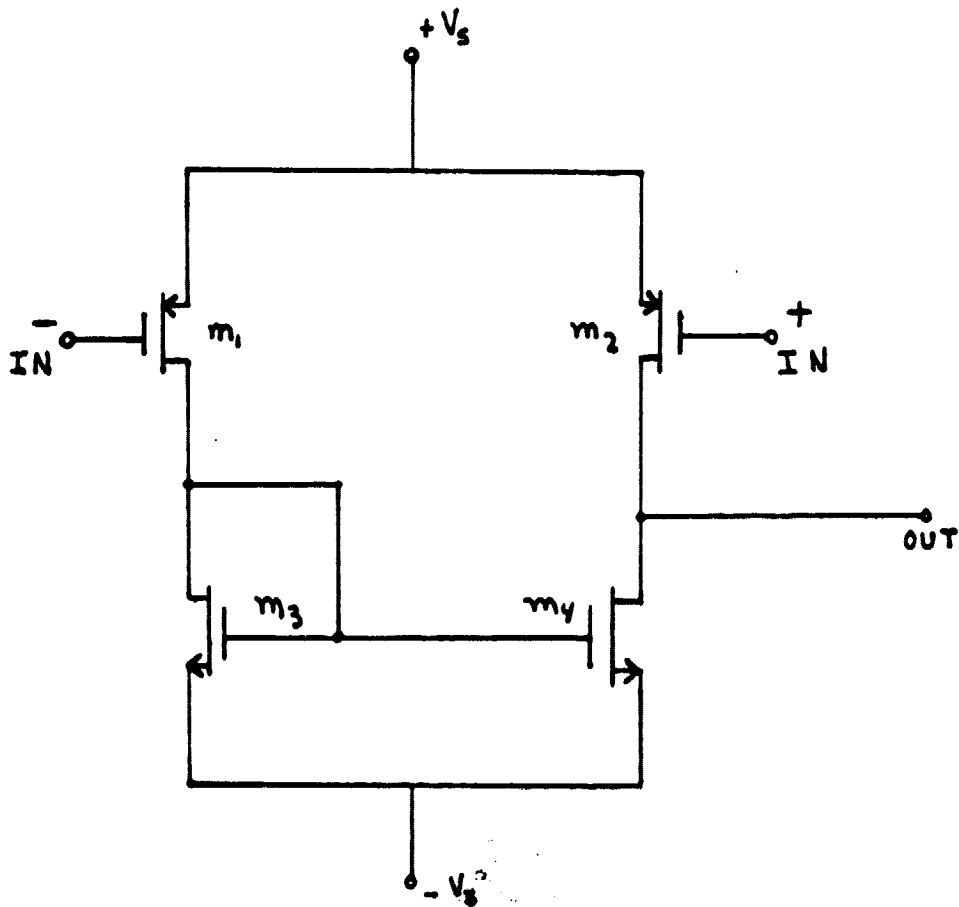
Fig. 28 CMOS Difference amplifier
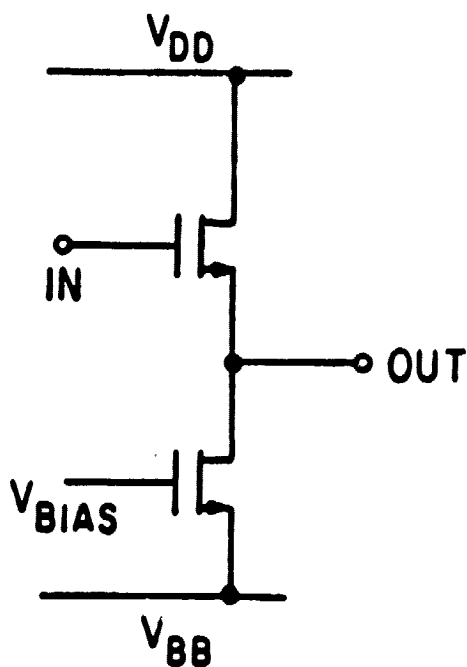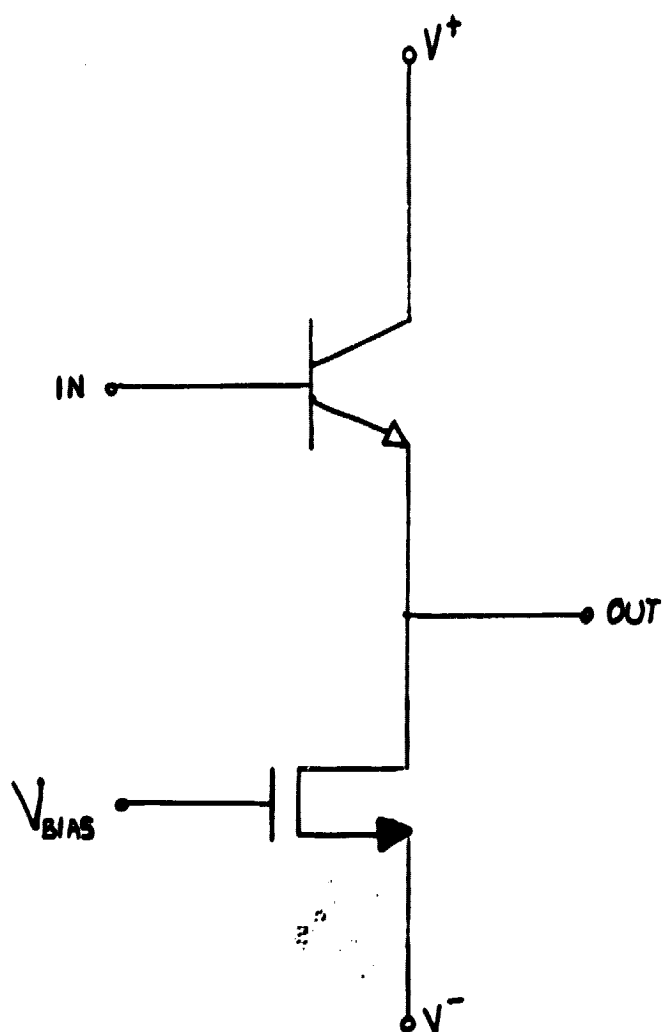
Fig. 29 Output buffers
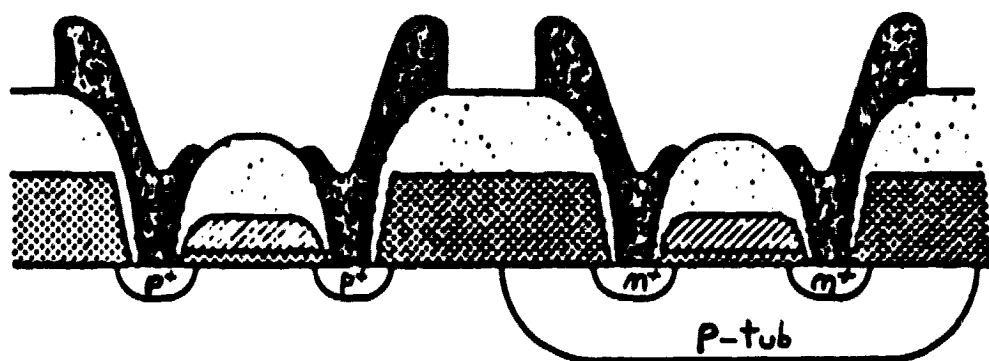
BULK CMOS

Fig. 30 Cross-section of silicon gate bulk CMOS

developed into the industry standard technology. On the other hand there is not an industry standard CMOS technology. Although most of the effort has been on bulk CMOS, silicon-on-sapphire (SOS) and other silicon on insulator (SOI) technologies are still very much alive despite predictions to the contrary.

1.4.1 Bulk CMOS

A cross section of silicon gate Bulk CMOS in shown in Fig. 38. This technology is an extension of the original MOS technology - PMOS. The NMOS device is added to the PMOS process by placing a P-well into the N-type substrate. It is also possible, to have a N-well in a P-type substrate resulting in the so called N-well CMOS technology. Supporters of the l-well technology claim that it should become increasingly appropriate as gate lengths are scaled below 2 microns. On the other hand, supporters of P-well CMOS dispute the speed benefit of the N-well version and cite reduced latch-up immunity as penalty [20], [13]. The arguments are further complicated by the fact that both varieties of CMOS can be constructed in dual-well versions (Twin-Tub CMOS).

1.4.2 Twin-Tub CMOS

In scaling to finer design rules in the classic bulk CMOS process, the doping in the n-substrate has to increase to support voltage in the shorter channel length p-channel transistors. Since the p-tub doping has to be raised proportionately, the n-channel transistor will suffer from excessive source/drain to

p-tub capacitance. In order to avoid these scaling problems, a twin-tub CMOS process was designed [21] to provide separately optimized tubs and consequently a lower capacitance n-channel transistor than the one obtained with bulk CMOS. A cross-section of the device is shown in Fig. 31. The CMOS process is an eight mask process that utilizes lightly doped epitaxy on an n^+ substrate to avoid latchup. The combination of n on n epi and careful I/O layout renders the circuits latch-up free.

The resultant device properties of this technology are well controlled and designed to be scaled smoothly into the improved lithography of the future. One of its properties is the physical symmetry (Fig. 31) which aids in the control of the ratio of current drive per unit gate length for the two types of transistors.

1.4.3 The Isolation Problem

A fundamental requirement of all integrated circuits technologies is the electrical isolation between active transistors. As a matter of fact, the device isolation schemes will play a large role in limiting device switching speed and chip power dissipation. The reduction in lateral feature sizes will achieve higher device packing density but the parasitic resistance and capacitance associated with the interconnects and isolation regions will limit further improvements in the maximum chip operating frequency.

In a typical VLSI chip the relative volume occupied by the isolation regions is 67% while the conducting regions and active

regions occupy 31.5% and 1.5% respectively. It is therefore clear that if we are to increase the packing density of present VLSI chips, it is the development of new isolation schemes that will provide the greatest improvement in chip performance. Improved device isolation approaches will reduce parasitic capacitances and resistances associated with both the active device and the interconnect wiring. This will result in VLSI chips having higher speed, lower power dissipation, lower fabrication cost, increased reliability and higher device packing density than present VLSI chips [21].

All bulk silicon device technologies employ P-N junctions to provide isolation between individual transistors. In the silicon-on-sapphire technology, the silicon between transistors is physically removed, leaving only the insulating substrate between devices. The SOS technology offers a definite performance edge over equivalent bulk silicon technolgies for lateral dimensions down to the order of 1.2 microns. For smaller dimensions than 1.2 microns, both sapphire and silicon substrates allow substantial capacitive coupling (via the substrate) between adjacent conducting regions. Silicon-on-insulator is the alternative device isolation scheme for sub micron design rules.

1.4.4 Silicon-on-Insulator(SOI) [22] [23] [24]

SOI wafers are considered an ideal vehicle for CMOS very large-scale integrated circuits. SOI promises greater speeds and densities than can bulk-type structures because devices can be more tightly packed on the die and have lower parasitic

capacitance. Devices are formed in individual islands of silicon atop an insulating layer so that latchup is completely banished. Both silicon nitride and silicon dioxide layers have been utilized as insulating layers beneath single crystral films of silicon. However, silicon dioxide will be the preferred insulator for the new buried oxide technologies, due to its intrinsically lower relative permittivity. A lower permittivity results in lower substrate capacitive coupling.

1.4.5 N-MOS Process

The schematic cross section of an NMOS device used in the fabrication of a 32 bit CPU chip is shown in Fig. 32. This particular device is produced with an 8-mask silicon gate process. This CPU chip described in [25] contains 450,000 transistors.

Another example of the NMOS process is the one reported in [26] in December 1980. Working with finely scaled-down geometries and advanced processing techniques, a Bell Laboratories team achieved a 40 ps. gate delay in a 19 stage ring-oscillator integrated circuit based on transistors with 0.3 micrometer channel lengths.

Lately [27], it has been reported that at the Laboratoire d'Electronique et de Technolgie de l'Informatique in Grenoble, transistors with channel lengths as small as .15 micron have been produced. For a .25 micron the reported switching speed is 30 picoseconds.
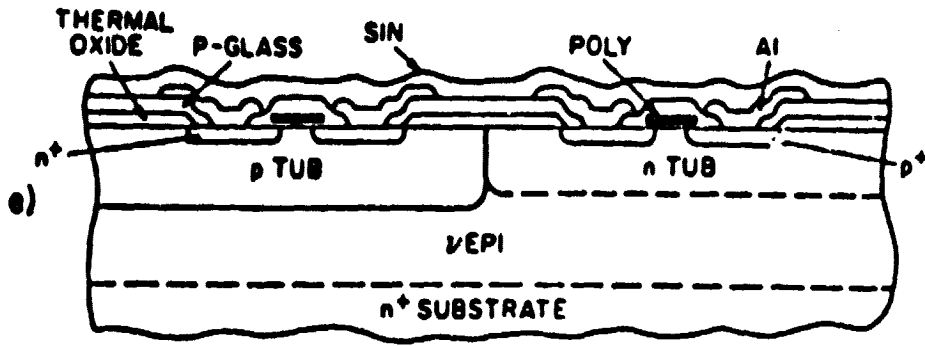
Fig. 31 Cross-section of twin-tub cmos gate.
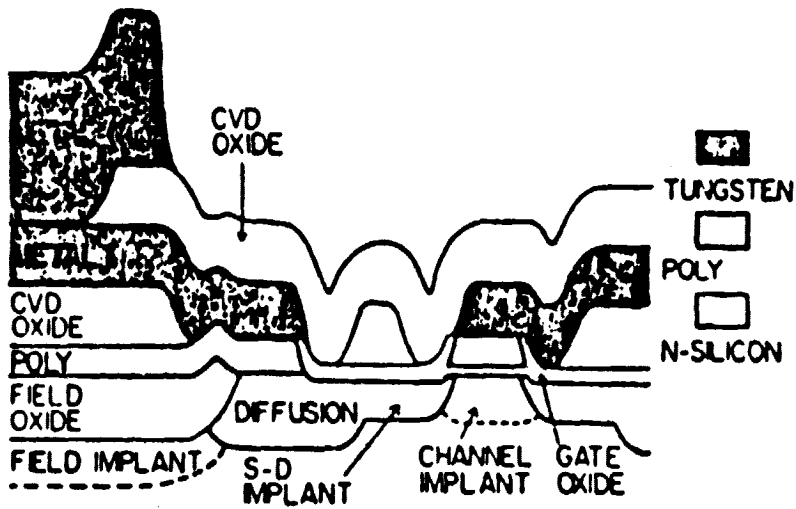
Fig. 32 Cross-section of NMOS device.

N-channel MOS silicon gate process is one of the technologies that are reasonably high in density and scale to submicron dimensions without an explosion in the power per unit area required for its operation. It is this N-MOS technology characteristic that has made N-MOS not only as fast as bipolar but the densest technology available.

1.4.6 Comparison betweeen NMOS and CMOS[28]

If one chooses to compare basic gate speed using identical design rules, the CMOS gate will switch faster than the NMOS gate. In addition to that, in an IC in the standby mode, the NMOS circuit will statistically have half of its gates "on" and will draw orders of magnitude more power than the CMOS IC. Thus, the speed-power product for CMOS is better than the one for NMOS. Furthermore, as technology brings finer-line geometries, the control of the NMOS gate "ratio" (to increase the speed, the ratio of the "ON" resistance of the pullup device to the pull down device should be reduced) will get worse whereas CMOS will be relatively less affected since it is not a "ratioed" logic.

To be fair about the comparison, one should indicate that at maximum NMOS gate toggle rate, the CMOS gate will draw two to four times more current than the NMOS gate (to switch faster, one needs more current). Also the process complexity (cost) of the CMOS process is approximately 20% greater than the NMOS process. It is this cost factor that has made NMOS a mainstream process with enough lead time that there are few CMOS circuits which are

as fast as their N-channel counterparts. However, this is changing because the same scaling principles that have given N-MOS its speed are being applied to C-MOS, and with even more exciting results because of its inherently lower power drain [29] [30].

VLSI densities will encourage the use of more different types of circuitry on one die. CMOS is the only technology of creating all of the following circuits simultaneously on one die: RAM, ROM, Logic, PROM, EPROM, EEPROM, Interface Drivers, Op AMPS, comparators, voltage references, D/A and A/D converters, Audio filters and so forth. In addition one could have automatic and programmable power down on the chip. Certainly, CMOS technology shows great flexibility in application.

1.5 State of the Art Applications

There are many MOS circuits to be reported but we will limit our discussion to the fastest and to applications requiring maximum density as reported lately in the literature. Memory technology demands have driven NMOS development. For example, high speed memories capable of bipolar performance at low power, high packing densities and low cost are in demand to complement advanced logic circuits [31-33]. To meet this need, a fully static NMOS 4K x 1 memory which achieves an adddress access time of under 5 ns was reported at the 1983 IEEE International Solid-State Circuits Confernvce [34]. The device was fabricated using 1 microns X-ray lithograph and the minimum transistor lengths are 0.5 microns to 0.8 microns. The typical power

disssipation, at a supply voltage of 4 volts is 400 mw. At the
same conference, a 4 Kb Bipolar Static ECL RAM was reported. The
device has a typical access time of 3.2 ns with a power
dissipation of 3 W. So, while the bipolar memory is faster by a
factor of less than two, it consumes eight times more power than
the NMOS device [35].

There was an entire ISSCC session in 1983 devoted
exclusively to design of 256 K dynamic RAMs (DRAMS). This
reflects the dominant importance of the MOS memory in both the
market place and as a driver for the continued development of
advanced low defect density processes. In the realization of
high density RAM's, such as 256 K DRAM's, not only smaller cells
are necessary but one needs to provide redundancy characteristics
to improve the yield. The 256K design using the smallest die
size, reported in ISSCC '83, belongs to Nippon Electric Co. [44].
An unusual dynamic - RAM process - two metal wiring levels plus
double polysilicon - coupled with very aggressive 1.3 micrometer
design rules, produces a very small 52,700 mil^2 chip. Redundancy
is not provided, since it is estimated that the yield will be
high enough with that small chip.

A change in the value of a stored bit results in a soft
error. In DRAM technology the Soft Error Rate (SER) is one of
the critical factors related to high density. Since SER depends
on the capacity of the memory cell, poor SER results from
minimization of the die size with the use of conventional
techniques. In the design of the 256K NEC chip, the 1.3 minimum
design rule and 160 A thick oxide have made it possible to

produce a 10.9 x 6.1μ^2 memory cell with storage capacity of over 50 femtofarad. This capacity implies a high reliable sensing and immunity to soft errors.

A comparison of 256K DRAM is shown in Fig. 33.

A 64K N - well CMOS DRAM was reported in ISSCC 83 that shows a superiority over similar NMOS devices [36]. The advantages cited are in the areas of soft error protection, design simplicty, periphery overhead reduction and performance enhancement. These advantages will establish CMOS as the leading technology for future DRAM development.

CMOS static RAM's show their versatility to compete with the involatile memories in a paper presented in ISSCC 83 [37]. A 64 K CMOS static RAM with battery backup is featured as a dense nonvolatile storage. The device access in 80 ns, much faster than any of the electrical eraseable-PROMs to date, and of course, stand by on very low power (15 nw for the entire 64 K array).

At the same conference, reported advances in gate arrays are quite impressive. For example, a high-density 20K - Gate CMOS gate array was presented [38]. It uses 2 micron design rules and the typical gate delay is 1.5 ns for a fanout of 3 and a 3 mm interconnect length. This array was used in the design of a 32b x 32b parallel multiplier resulting in a multiplying speed of 150 ns. with a 300 nw power dissipation at a 5MHz clock rate. Gate arrays are very attractive to the system designer mainly because of the quick turn-around time. As the arrays grow toward 10,000 gates and beyond system designers will find gate arrays

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Company	Nippon Electric	Motorola	Fujitsu	Toshiba	Mitsubishi Electric
Technology (word line/bit line)	double polysilicon (metal-poly/metal)	single or double polysilicon (titanium silicide/metal)	triple polysilicon (poly/poly)	double polysilicon (molybdenum silicide/metal)	double polysilicon (molybdenum silicide-poly/metal)
Design rule (μm)	1.3	2.0	2.5	2.0	2.0
Cell area/capacitance (μm^2/fF)	67/50	84 / (not available)	68/35	77 / (not available)	98/42
Chip area (mil^2)	52,700	71,600	52,900	71,300	73,700
Typical access times (ns) row column nibble cycle	90 (not available) – (not available)	90 50 15 250	<80 35 15 200	94 34 – 260	100 50 25 210
Power consumption (mW) active standby	250 10	225 15	300 15	170 15	250 12
Column-before row-address strobe (CAS before RAS) refreshing	no	yes	yes	no	yes
Redundancy	none	laser; 8 rows, 4 columns	laser; 2 rows, 1 column	laser; 4 rows, 4 columns	laser; 4 rows, 4 columns

Fig. 33   Comparison of 256K DRAM

more attractive if they have memmory as well. Such a feature is included in a 2 ns. CMOS gate array [39]. It has 4,268 gates and a 2,304-bit configurable memory developed by employing a 1.5 micron design rule. The configurable memory can realize many kinds of memory configurations in regard to word depth and bit width by changing the metalization pattern. A control processor for a small computer system was designed as a functional gate array processor [39].

Among the latest circuits for digital communications reported in the literature, there is a 500 MHz Phase Locked Loop NMOS and a NMOS preamplifier for optical fiber receivers. The PLL chip has a NMOS prescaler operating at more than 750 MHz [40]. The Phase Locked Loop chip contains approximately 3000 transistors in a 1.35 x 1.95 mm_2 area. The effective channel length is 1.5 micron and the gate oxide thickness is 470 A. It consumes 150 nw at V_{DD} = 5v. In TV synthesizer tuning systems, the PLL LSI receives the VHF/CATV local oscillator signals directly.

A single-chip NMOS preamplifier for optical receivers was reported in [41]. The amplifier was made with a fineline enhancement/depletion NMOS process resulting in an effective channel length of 0.5 micron. Open loop measurements indicate an average open loop voltage gain of 180 with the single pole rolloff at 170 MHz. The device was tested in a 90 Mb system and optical sensitivity is -37 dBm. These chip receivers are 17 db better at 44.7 Mb than earlier single-chip receivers but the results are 3 dB worse than discrete Ga As/bipolar amplifiers

[42] [43]. This poorer-than-expected noise performance may be due to yet unknown noise sources present in short-channel MOSFET devices.

2.0 Ga As Integrated Circuits

A Viable Technology for High Speed IC's: Ga As.

The Gallium Arsenide (Ga As) compound semiconductor has been used for a long time in the design of microwave circuits such as FET oscillators and low noise amplifiers. More recently, it's superior electronic properties have made it of great interest for ultrahigh-speed logic applications. There are two main reasons for using Ga As rather than silicon in high speed integrated circuits.

1. Ga As electron mobilities are about 6 times higher than those for correspondingly doped bulk silicon.

2. Ga As has semi-insulating properties which reduces parasitic capacitances and allows higher switching speeds.

In order to achieve ultrahigh-speed VLSI, high device transconductance is needed at control voltages only small logic swings above threshold [45], [46]. The transconductance g_m for a FET structure is given by

$$g_m = \frac{\varepsilon \mu}{a} \frac{W}{L_g} (V_{gs} - V_{th})$$

(40)

where ε is the dielectric constant of the semiconductor in a metal-semiconductor FET (MESFET), μ the electron mobility (n-channel), a distance between gate and the channel, W the width of the channel, L_g the gate length, V_{gs} gate-source voltage, and V_{th} is the threshold voltage.

Clearly, to maximize the transconductance, one could

reduce the gate length to shorter and shorter values. Unfortunately taking this course alone places unreasonable pressures on the required lithographic precision and will ultimately prove disastrous to yield. However, one could obtain an equivalent improvement by going to a semiconductor with a higher channel mobility .

2.1 Ga As Digital Circuits

Figure 34 shows a cross-sectional diagram of a typical planar ion-implanted Metal-Semiconductor FET (MESFET) fabricated by localized implantation into a semi insulating Ga As substrate. The Schottky barrier gate field effect transistor (MESFET) is the main active device used in Ga As IC's.

A number of basic circuit designs for logic structures have been realized in Ga As technology. Basic circuits have been demonstrated utilizing normally OFF FET's (Enhancement-Mode) in conjuntion with resistor or depletion loads and Schottky-barrier level shifting diodes. Buffered FET logic (BFL) [47] and Schottky Diode FET Logic (SDFL) [48] gate circuit approaches have been extensively employed for depletion-mode Ga As IC's. A number of circuit approaches for single supply Enhancement-Depletion mode E-D MESFET logic have been proposed and analyzed [49]. The most promising of these circuits at this time is the 3-input NOR gate. This uses source follower logic to obtain the positive OR function, with single diode level shifting and resistor pulldown to drive the output inverter FET.
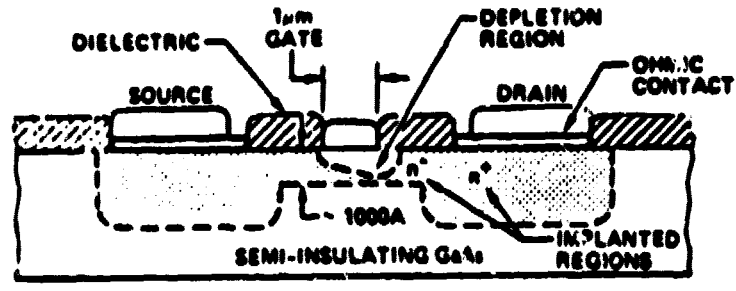
Fig. 34 Cross-section diagram of a planar ion-implanted MESFET
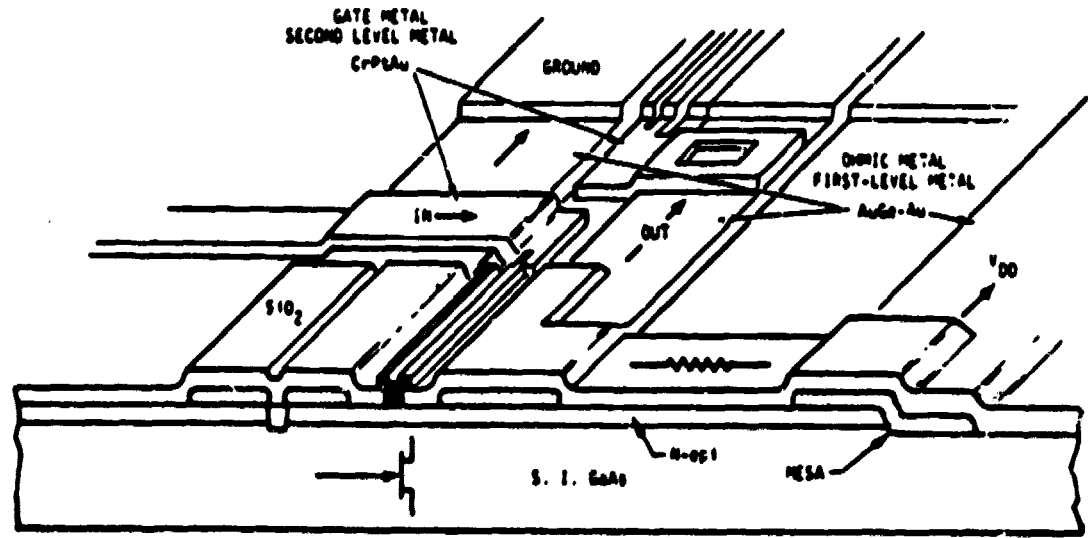
Fig. 35 Enhancement mode Ga As MESFET on epitaxial layers and isolated by mesa etching.

2.2 Technology

There are several fabrication approaches which are currently in use as processing techniques in the Ga As technology. Mesa-Implanted depletion-mode D-MESFET, for instance, is a simple, well developed technology, [47], however, its application is restricted to circuits in which only a single type of device needs to be optimized. Enhancement mode Ga As E-MESFET devices have also been fabricated on eptaxial layers and isolated by mesa etching (see Fig. 35).

Planar fabrication methods similar in concept and appearance to well established silicon IC approaches have been developed. The planar approach employs selective implantation to localize active devices in the semi-insulating Ga As substrate. Planar Implanted enhancement-mode E-JFET fabrication technology [50], [51] uses a junction FET to provide direct-coupled FET logic (DCFL) circuits with resistor loads. Planar Implanted D-MESFET circuits (see Fig. 36) are fabricated as in the planar E-JFET approach by using multiple localized ions implant directly into semi-insulating Ga As substrates [52]. In this way, individual devices can be optimized by using different implants, and the unimplanted Ga As substrate directly provides isolation between devices.

Direct writing electron-beam lithography (EBL), [53]. has been utilized as an alternative to projection optical lithography when submicrometer gate lengths are required in Ga As IC's. One of the advantages of direct-write EBL is the ability to rapidly
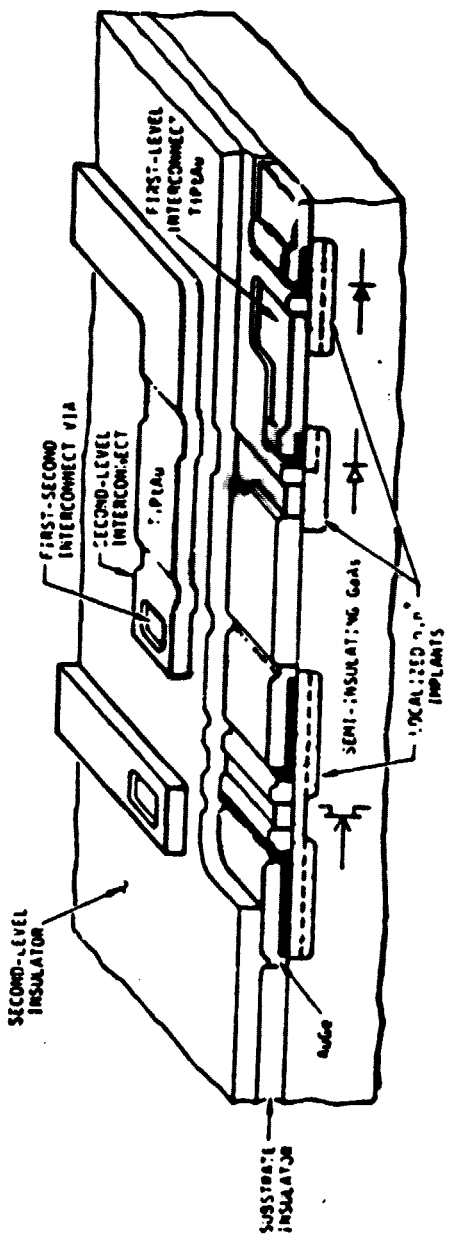
Fig. 36 Planar Implanted D-MESFET

modify circuit and device design to optimize circuit performance. The writing rate of all but the most exotic EBL systems is, however, much too slow to be considered for LSI or VLSI circuit fabrication on large substrates at this time.

2.3 Applications

The commercial application of Ga As IC's is now evolving. The short gate propagation delays and rapid risetimes of Ga As gates make them attractive to designers of high throughput, high clock rate digital signal processors. Ga As digital IC's appear well suited to applications in very high speed instruments, from basic building block components like samplers, counters, and demutiplexers to sophisticated signal acquisition and processing circuits for use in A/D conversion, frequency synthesis, and Gb data link operation. Today, strong development programs exist in Europe and Japan, and applications of Ga As logic into systems are anticipated soon. The Ga As technology drive is somewhat weaker in the U.S.A., with only a handful of US companies anouncing plans to enter the commercial market, while the majority are developing capabilities to satisfy in-house requirements for military equipment. In contrast, the Japanese Government has identified Ga As IC technology as the best approach for implementing fifth generation, high speed computers [54].

An example of an LSI circuit is a multiplier consisting of NOR gate full adders and half adders in a regular array, which forms the binary product of two 8 bit input words. This 8 x 8

multiplier, which also contains D-type flip-flop, latches every input and output bit, required over 1000 NOR gates. The performance observed corresponds to a propagation delay of 150 ps/gate at a full power dissipation of about 2mW/gate. At this speed, a full 16 bit product would be available every 5.25 ns [55].

An active 11.5 GHz frequency translator has been developed using four dual-gate Ga As FETs which achieves carrier and spurious sideband suppresion of more than 20 dB for translation frequency of up to 1 MHz. The circuit can also be used as a high speed APSK modulator with a phase transition time of approximately one nanosecond [56].

Improvements continue to be made in the monolithic microwave IC's. A 60 GHz Ga As FET amplifier, for instance, has recently been designed. The amplifier was tested beyond 60 GHz, to the limits of the fixture it was in. The extrapolation and modeling carried out indicates it will reach about 94 GHz before the gain drops to zero [57].

Using Self-Aligned FET technology, a 1 kb static RAM has been developed, [58], with a resultant access time at 2.0 ns. The speed up is accomplished by the precise control of threshold voltages for the E and D-type self-aligned epitaxial (SAINT) FETs. Gate length and power dissipation are of the order of 0.95 and 459mW respectively.

3.0 Designing a VLSI Chip

Designing a VLSI circuit is complex. A factor that makes VLSI design difficult is caused by the ever-increasing ability of technologists to integrate more components in a single integrated circuit. The maximum number of components in a chip has on average doubled annually for almost two decades. Yet although several more orders of magnitude in complexity are possible before reaching fundamental physical limitations, there is little point in moving to a higher level of complexity when current capabilities are not being used to their full effect. For example, present circuits, with the exception of memories and other very regular circuits, contain a significantly smaller number of components. This has been caused by the increased difficulty of designing such complex circuits [59], [60], [61].

The exponential growth of IC complexity has had a dramatic impact on the time needed to design a circuit. Today most complex chips are still being designed with the same basic method used over 20 years ago. So the time has increased from a few weeks for small-scale IC's (SSI) to tens of man-years for large-scale circuits. After the block diagrams, logic diagrams, schematics, layouts, and of course endless checking, millions of dollars have been invested in a complex IC. So, it is not surprising that the industry must sell vast quantities to recoup its design investment.

It is shown in [62] that the automation of the old design

techniques is not the optimum solution. An alternative method used for dealing with complexity is hierarchical design. As a matter of fact, it has been used in the design of software with great success. However, the introduction of structured design methods is not a simple matter. It requires a change of attitude to design, calls for new concepts to support hierarchical design, and a new generation of Computer Aided Design (CAD) tools. But this design methodology will enable us to go on designing increasingly complex circuits.

The main building blocks in a VLSI design in order of complexity could be the following [63]:

1. Devices (N-MOS transistors, CMOS transistors, etc)

2. Logic Gates (Inverters, Nand, Nor, etc)

3. Signal Flow Blocks (shift registers, etc)

4. Large Logic Arrays (PLA's, etc)

5. Interface Circuitry (To connect Data Bus to System Bus, etc)

6. Data and System Buses (To define signal flow and regularize wiring)

7. Complete Fuction Blocks (RAM's, ROM's, etc)

With these modules, extending from simple devices to whole function blocks one could undertake a regular, structured VLSI design.

4.0 Lithography

Lithography may be defined simply as the transfer of a pattern from a template (mask) to a substrate [64]. The transfer process is considered the pacing feature in the evolution of integrated circuits; and a single lithographic design rule (smallest feature size) is often used as an indicato⁻ of the sophistication of the whole process.

The "lithographic" process could be broken down into the following parts:

1. Mask template fabrication (omitted for e.beam lithography)

2. Exposure and development of a radiation sensitive resist layer (typically a polymer)

3. Transfer of a pattern to an underlying layer

4. Removal of the resist layer.

To pattern a polymeric resist layer (Step:2), one uses one of the following exposure techniques: ultraviolet, deep ultraviolet, X-ray, electrons beams, and ion beams.

Optical lithography will probably reach its limits at .75 microns (stepper machines and deep UV). Below this dimension it is not possible to predict what technology will be the dominant one. Before 1981, it seemed that E-beam would become the dominant technology of the late 80's but a new X-ray system was reported

in 1981. This system [65] was reported as having a potentially higher production throughput than E-beam systems as well as the ability to make the smallest MOS transistors ever reported. There are a number of techniques available within this technology [66-68]:

Contact Printing - It has been the traditional exposure technique with the shadow mask pressed intimately against the photo resist covered wafer. However, the intimate contact produces defects in mask and wafer; so the mask must be discarded after a short period of time.

Proximity Printing - There is no contact between mask and wafer and therefore no yield degradation. On the other hand resolution is not as good as with hard contact printing.

Projection Printing - Reflective optics are used; mask and substrae have same dimensions. The alignment is performed globally over the whole wafer.

Optical Stepper - The stepper approach represents a significant improvement in resolution and alignment precision over the other optical techniques. In this technique a field consisting of one or more die (rather than the whole wafer) is exposed at a time followed by a stage to new alignment site, a realignment, exposure, etc. Of course the throughput goes down and the machines are more expensive as well.
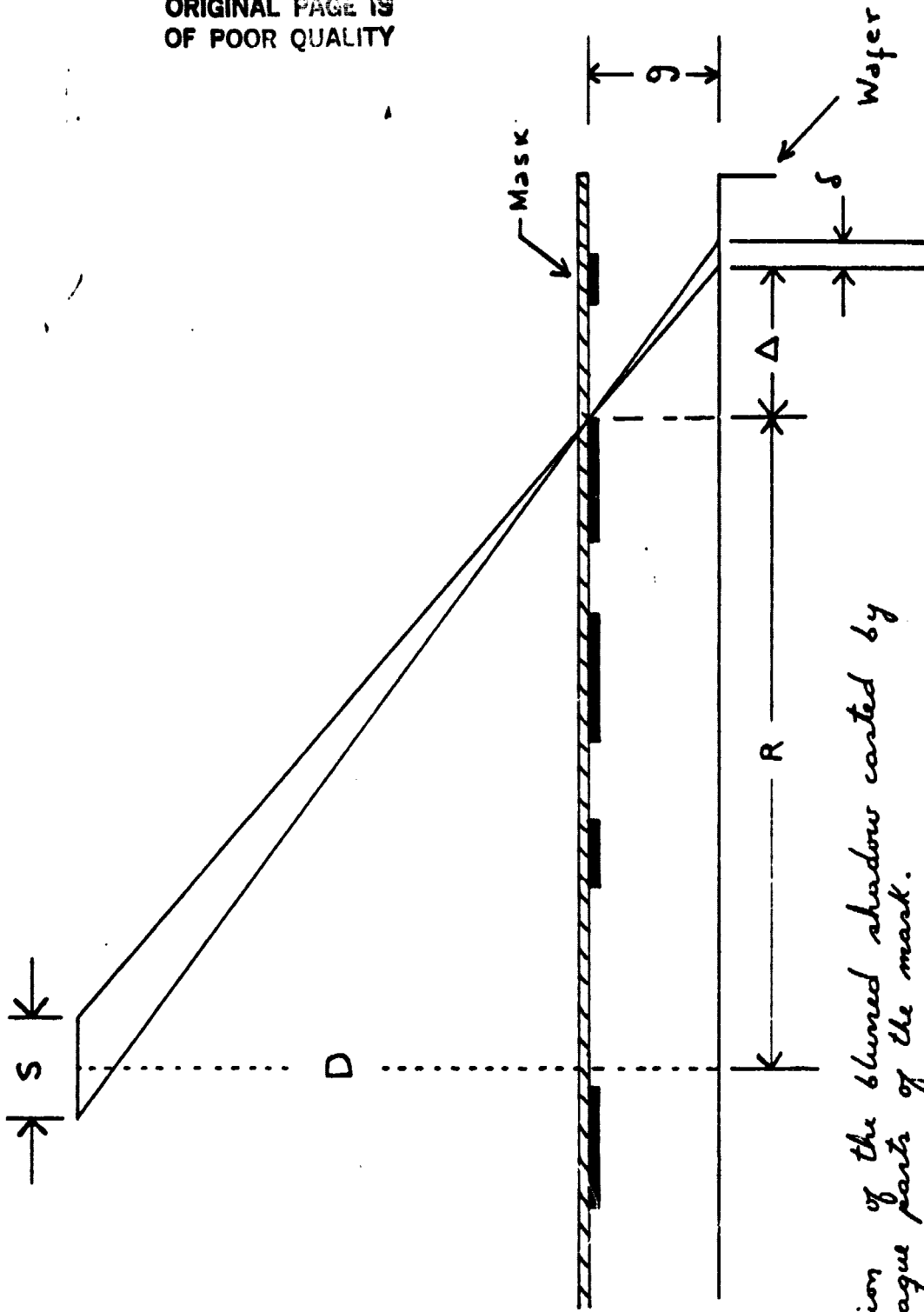
S : dimension of the blurred shadow casted by the opaque parts of the mask.

s : dimension of the X-ray source.

Δ : "runout" $= gR/D$

Fig. 37 X-Ray projection parameters

are longer by an amount   as shown in Fig. 37 at the edge of the wafer [71-72].   This technology is an offshoot of the X-ray approach where approximately 200 Kev protons are substituted for X-rays.   Since the resist is considerabler more sensitive to protons than electrons, the throughput of such a system can be considerably enhanced [73].

Characteristics of Lithography Technologies -   A summary comparison of the alternative technologies is listed in Fig. 38 [64].

5.0 Conclusions

This report summarized the various technologies and their applications to VLSI.   The fabrication of communication systems using VLSI was discussed and an elaborate set of references are presented.

VLSI has a major problem which is power dissipation. This problem affects speed of operation.   Today one finds many digital applications for VLSI.   However, microwave amplifiers, receivers, modems, coders, multiplexes, etc. are also being developed.

It is our opinion that in the near future the engineer will sit at his terminal, design his system using some VLSI language, transmit the design to a fabrication house and receive back the VLSI chip within 1 month.

TECHNOLOGY	ADVANTAGES	DISADVANTAGES	KEY APPROACHES
1. Optical 1:1 Projection	Today's standard High productivity	Confined to 4" wafers Personality of machines limits precision of alignment Alignment is global (across entire wafer), not local (across die) Increased burden put on mask masking as dimensions shrink Theoretical resolution intrinsically less than e-beam, x-ray, ion beam approaches	Expand optical systems to 5", improve precision of mirrors and lenses. Automate and correct for linear distortions. Improve precision of optical elements. E-beam mask making. Use far UV for improved resolution. Use multilevel resist technologies to inhibit reflections, standing waves, etc.
2. Stepper	Demagnifying versions greatly reduce mask technology requirements Alignment can be performed locally to high precision	Throughput low because of necessity to step and to align at each site Trend to large wafers slows throughput further Single large dust particle on mask gives zero yield Theoretical resolution limited by wavelength effects	Improve throughput by faster stepping, faster alignment algorithms, increase of field size, etc. Cover mask with protective out-of-focus plastic sheet (pellicle). Multilevel resists, 2 wavelength exposures.
3. X-Ray Lithography	High intrinsic resolution (100A) Higher throughput than steppers (full wafer exposure)	Slow resists Difficult 1:1 x-ray mask technique "Weak" lab sources Full wafer alignment precludes non-linear local corrections	Custom high sensitivity resists Small stepper masks Plasma sources, synchrotron Stepper x-ray
4. Ion Beams unfocused	Same as x-ray except faster throughput as resist is far more sensitive to ions than x-ray photons Much less proximity effect than electrons because of reduced backscattering in resist and substrate	Beam heating of mask can cause distortions Same mask problems as x-ray Scattering in mask limits resolution	Go to step and repeat to allow smaller masks, local alignment
focused	Same as above plus elimination of masks	Complex optics, source, etc. Both of above at very early research stage	
5. E-Beam	Very high resolution, precision No masks required (less defects) Flexibility in changing patterns in software without hardware (tooling) in masks Many years of research and mask making experience	Slowest of all techniques Patterns affect other closely adjoining patterns (proximity effect) Most expensive Limited scan field (for vector approach) requires piecing fields together	Increase scan speed, data transfer rate, etc. Shape beam to expose whole rectangles, etc. Correct dose of edge regions in software. Expose whole wafer in 1:1 e-beam approach. Hybridize with other techniques e.g., optical for coarse regions

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Fig. 38 Characteristics of Lithography Technologies

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