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This study was intended to prove or disprove the existence of ESD-caused latent failures on semiconductor devices. The parts studied were 3N128 MOSFET and the 54L04 low power TTL integrated circuit. A sampling of each device was stressed by an ESD pulse to various levels of degradation. Life tests were conducted at 25°C and 75°C for 480 hours minimum at each temperature and the results of these tests compared to an unstressed control sample of devices.

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FINAL REPORT

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PREFACE

This Final Technical Report was prepared by Westinghouse Electric Corporation under Government Contract Number F30602-78-C-0281, supplemental agreement P00024. This study of latent ESD failures is a follow-on effort to an earlier study that was part of ESD Task (A6022A3040A40). The efforts reported herein were conducted over the period 20 January 1981 to 16 November 1981. Technical monitoring and coordination of the program was under the direction of Mr. Roy Walker,* IIT Research Institute, Rome, New York.

Although the results of Latent Study I did not positively verify latent ESD failures, there were certain indicators of their existence. Thus, this earlier effort has provided direction for this follow-on study. Several part types showed a propensity for further degradation with time once a certain degree of ESD damage had occurred. The parts in question were damaged beyond the part specification limits by ESD exposure prior to life tests. A part of this effort is to review the data on these severely damaged parts to see if latent failures might occur in certain higher assembly applications. Another indicator of possible latency existed in the few MOSFET devices with gate oxide damage (Most had increased drain to source leakage.). This effort includes a much larger sample of MOSFETS with gate oxide damage. A second part type included in this study is the 54L04 low-power TTL integrated circuit. Samples of 5404 TTL devices and 54S04 Schottky TTL devices were a part of Latent Study I. The sample sizes, including the number of controls, is significantly larger for Latent Study II.

The principal Westinghouse Electric Corporation investigators on this program were Owen J. McAteer and Ronald E. Twist.

*Mr. Walker is presently employed by SAR Associates, Westmoreland, NY.

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1.0 SUMMARY

This study is a follow-on effort to Latent Study I. In this follow-on effort a larger sample of just two part types was used for experimentation in an attempt to end the very controversial question as to whether or not latent ESD failures are a reality. The parts studied were the 3N128 MOSFET and the 54L04 low-power TTL integrated circuit. This follow-on effort also includes a brief review of some pertinent data from Latent Study I on parts that were initially out of specification limits following ESD exposure, then degraded further during 25°C and/or 75°C life tests.

Whereas the existence of latent failures was not felt to have been positively verified by Latent Study I, this latent study provides solid evidence of their existence. The success of this follow-on effort is certainly due to a large degree to information learned during the experience of the first study.

There were latent failures of both types investigated, and the unpulsed control devices were stable during life tests. A review of the Latent Study I data indicates a good likelihood that some of those parts could also be regarded as latent failures in some design applications.

Since this latest effort verifies that latent ESD failures can occur under certain circumstances, static must now be considered a threat to reliability. ESD susceptibility must be minimized and preventive controls must be effective. A further study is recommended in order to gain a better understanding of the types of parts prone to this latent phenomenon.

2.0 INTRODUCTION

The objective of the study is to end the existing controversy as to whether or not latent ESD failures are a reality and to attain an approximate measure of the likelihood of occurrence under normal handling and usage conditions. A latent ESD failure is defined as a failure that occurs in use conditions because of earlier exposure to ESD that did not result in an immediately detectable discrepancy. From a macroscopic viewpoint, a latent failure could occur in several ways:

MAC 1: A device that remains in-specification after ESD exposure but degrades in life to an out-of-specification condition

MAC 2: A device that remains in-specification after ESD exposure and, although it remains in-spec during life, degrades sufficiently to cause a discrepancy at a higher assembly level

MAC 3: A device that goes out-of-specification after ESD exposure but is not detected at the higher assembly level until further degradation occurs with time

The time-dependent degradation associated with the preceding hypotheses might occur in either biased or unbiased conditions at room, ambient or accelerated temperatures.

This study is a follow-on to an earlier study conducted for Naval Sea Systems Command. The initial study did not positively verify the existence of latent failures, but additional analysis of some of the data from that study is included in this follow-on effort.

3.0 SCOPE

The following efforts are included:

3.1 Data Review

Certain data from the initial study were analyzed. Specifically, there were parts that were degraded beyond the part specification limits by the exposure to static and then degraded further during the subsequent life and/or bake tests.

3.2 3N128 MOSFET

Additional tests were conducted on MOSFET devices with emphasis on gate-oxide damage. The earlier study indicated a higher likelihood at latent failures or MOSFET with gate oxide damage. The 3N128 device type was chosen for this evaluation because of availability and high ESD sensitivity.

3.3 54L04 Integrated Circuit

The 54L04 was selected for study because of earlier references[1,2] to subtle degradation not detectable externally until catastrophic. It was, therefore, felt to be a good candidate for latent failure tests.

4.0 TEST DESCRIPTION

The appropriate pin combinations, ESD exposure levels and failure criteria were determined by preliminary engineering tests and evaluation.

4.1 ESD Zapper

An ESD zapper was constructed by following the requirements listed in DOD-STD-1686. A 1.5K ohm resistor and a 100 pF capacitor made up the passive circuit elements. A mercury wetted SPDT relay was used as the voltage switching element (see Figure 1). The resulting ESD pulse was then monitored on a scope and was verified to be repeatable over the entire voltage range used in the study (see Figure 2). The waveform was verified daily and a picture of the waveform was taken weekly. In order to avoid possible stray pulses when the capacitor was recharged, the part was disconnected from the ESD zapper terminals before the relay was de-energized.

4.2 Pin Combinations and Parameters

Pin combinations and polarities for ESD pulsing were chosen to try to affect particular device structures based on previous ESD failure experience on these device types.

The 3N128 MOSFET pin combination used was gate-to-source with the gate positive. The objective was to inflict gate oxide damage, which the initial study had indicated as the most likely site of latent degradation. The parameters used to monitor degradation were I_{GSSR} and V_{GS} (off).

The 54L04 pin combination used was the same combination reported by Freeman and Beall: input (pin 7) to ground (pin 1), with the input negative. The objective was to inflict damage to the base emitter

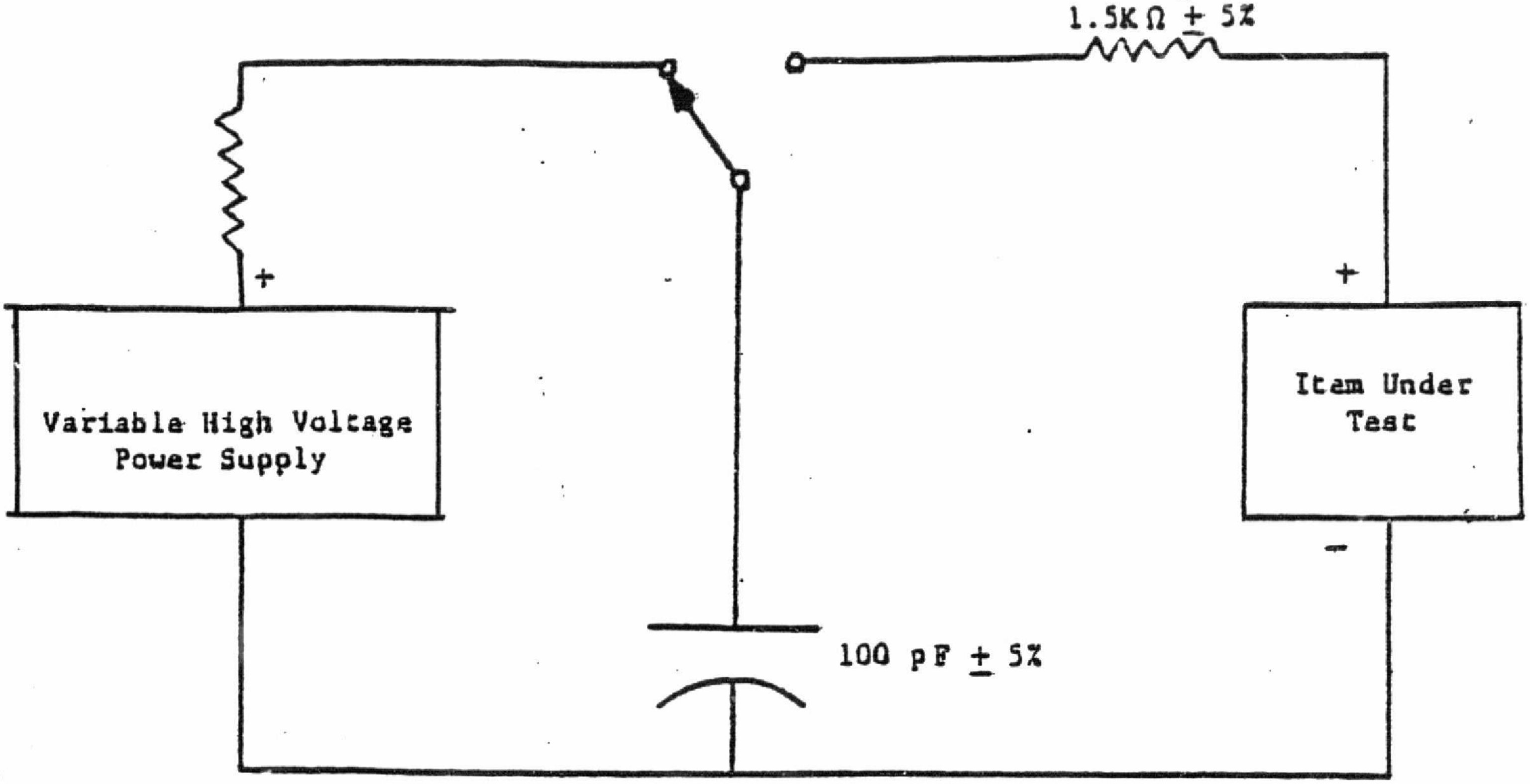

FIGURE 1: ESD TEST CIRCUIT

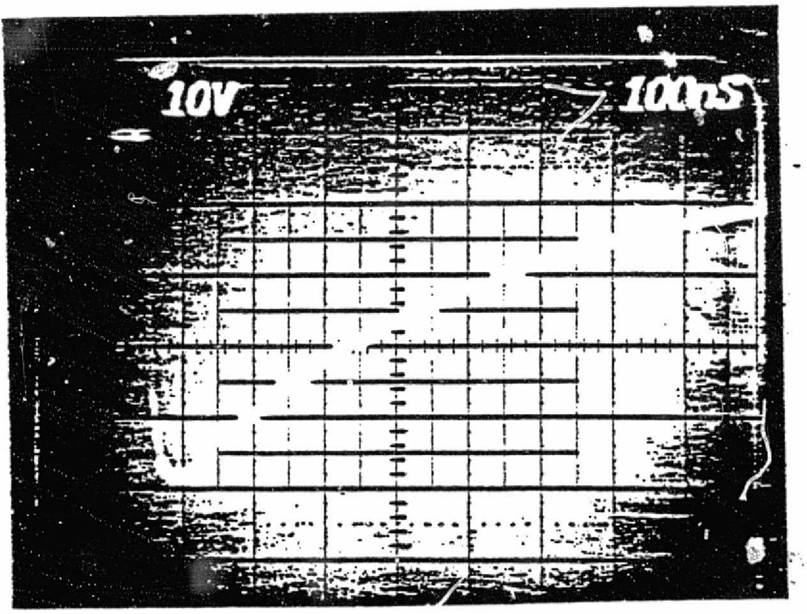

FIGURE 2: ESD WAVEFORM ACROSS 500Ω LOAD

junction of Q2. Damage to this junction would not be detectable until the current gain (beta) degraded to the point that the base bias of Q3 and Q4 was not being switched properly. This results in the output staying at the "high" level. The parameters used to monitor degradation were I_{IH} and V_{OL}.

5.0 TEST CONDITIONS AND FAILURE CRITERIA

The test conditions, specification limits, and failure criteria used for the 3N128 and the 54L04 devices are given in Figure 3. The failure criteria were decided after reviewing preliminary engineering test results. The failure criteria used reflect significant changes due to ESD exposure and are sufficiently wide to rule out measurement error and drift. A Hewlett-Packard Model 425 picoammeter was used for current measurements and a Hewlett-Packard Model 3440A DVM was used for voltage measurements. Series resistance was used for current limiting to prevent further damage during parametric testing.

Extreme care in static handling precautions was taken throughout this study so that unintended exposure to ESD would be avoided. The primary precautionary measures were: grounded wrist straps, grounded "static-dissipative" table tops, and conductive packaging.

Part Type	Test Parameter	Test Conditions	Specification Limits	Failure Criteria
3N128	I_{GSSR}	V_{GS} = 8V V_{DS} = 0V	- 50 pa max	> -25 pa
	V_{GS}(off)	V_{DS} = + 15V I_D + 50 µa	- .5V min - 8V max	- .5V min - 8V max
54L04	I_{1H}	V_{CC} = 5.5V V_{IN} = 2.4V All unused inputs at ground	10 µa max	± 20 na Δ
	V_{OL}	V_{CC} = 4.5V I_{OL} = 2 ma V_{IN} = 2.0V All unused inputs at 5.5V	.3V max	± .050V Δ

FIGURE 3: TEST CONDITIONS AND FAILURE CRITERIA

6.0 ESD PULSE RESULTS

6.1 Test Plan

In Latent Failure Study I, it was observed that most parts experienced an accumulation of damage from exposure to multiple low-level ESD pulses. This often occurs with no apparent parametric shifts until quite suddenly on the n'th pulse. The intent of this study was to test for this phenomenon over a suitable voltage range, as well as exposing a significant number of parts to appropriate single pulse levels. The plan was to then put these pulsed devices on life test and monitor for degradation. The life test sample ideally will include static-pulsed devices with severe, moderate, slight and no measureable damage as well as unpulsed control devices.

6.2 Data Logging

During all pulsing done in this study, detailed daily log sheets were filled out for every part. Dates were recorded. The ESD voltage level was recorded along with a device number which was also marked on the part itself. The number of ESD exposures was recorded. For multiple pulsing, test parameter values before exposure to ESD and after each exposure to ESD were recorded up to 10 exposures or pulses. From 10 to 50 pulses the test parameters were recorded after every 5 ESD pulses. From 50 to 200 pulses the test parameters were recorded after every 25 ESD pulses. Taking parameters measured at 5, 10, and 25 pulse intervals aided in completing the pulsing in a timely manner and was not believed to have affected the results significantly.

6.3 Test Codes

Test codes are used in defining test samples and test conditions throughout this report. The data is coded as follows:

P - Preliminary Engineering Evaluation Devices
M - Multiple Pulse Devices
S - Single Pulse Devices
C - Unpulsed Control Devices

6.4 Preliminary Tests

Latent Failure Study I revealed that the most efficient method of preliminary testing is multiple-pulsing to determine proper voltage ranges for both the single and multiple-pulse samples. The method consists of pulsing a preliminary sample of parts sufficient to approximate the voltage range for obvious damage from a single pulse to no detectable damage from 200 pulses. The preliminary results for the 3N128 (12 samples) are summarized in Figure 4.

Number of Pulses to Failure				
1 pulse level	10 pulse level	50 pulse level	100 pulse level	200 pulse level
200V	2 at 100V	50V	105V	75V
150V				60V
125V				50V
115V				
110V				

FIGURE 4: PRELIMINARY RESULTS ON 3N128

Preliminary results for the 54L04 (30 samples) are given in Figure 5.

MFG.	Number of Pulses to Failure							
	1 pulse level	2 pulse level	5 pulse level	10 pulse level	20 pulse level	25 pulse level	50 pulse level	200 pulse level
T.I.	8000V 7500V 7000V 6000V 5000V	7000V	7000V		6500V	6500V 6000V	7200V 4000V	5500V 5000V
National	3 at 5000V 4250V 4000V 2 at 3500V		3000V 2750V	3250V 2500V		3500V		3000V 2500V 2250V 2000V

FIGURE 5: PRELIMINARY TEST RESULTS FOR 54L04 DEVICES

6.5 Multiple Pulse Tests

Based upon the preliminary test results, the range chosen for the 3N128 was 95V to 115V. The preliminary data might have led to a lower minimum voltage, but we intended to try to inflict measureable damage on most samples. Latent Failure Study I results showed no degradation on parts with no initial measureable damage. The 95V to 115V range was divided into 5 equal steps for variation. Although the intent was to pulse 20 devices at each level, we first pulsed 10 at each level so that the levels could be changed if desired. The selected range gave the desired result as summarized in Figure 6.

The 54L04 multiple pulse sample was made up of 100 parts also; however, there were two manufacturers represented. Since 80% were from National Semiconductor, the preliminary data for National parts was used to set the initial voltage range at 2000V to 5000V. Again, 10 were pulsed at each level to allow for possible change in the range. The results of the first 50 samples pulsed is given in Figure 7.

Since all 10 devices pulsed at 2000 volts withstood 200 pulses and since there seemed to be too many in general that took 200 pulses, the voltage range was raised to 2750V min to 5750V max for the second 50 devices. The results of the second fifty is given in Figure 8.

6.6 Single Pulse Tests

The single pulse levels were determined by taking 90% and 80% of the one pulse level used in the multiple pulse evaluations. This turned out to be 103V and 92V for the 3N128 and 4500V and 4000V for the 54L04.

The 3N128 results at these levels showed significant damage to all devices at 103V and to most devices at 92V. Twenty devices were pulsed at each level.

The 54L04 results were similar: 17 out of 20 initially damaged at 4500 volts and 11 out of 20 initially damaged at 4000 volts.

Voltage Level	Pulses to Failure																			
	1	2	3	4	5	6	7	8	9	10	15	20	25	30	50	75	100	150	175	200
115V	12		1	3	2					1			1							
110V	11	1		1		3					1	1			1					1
105V	6				1	3	1	2	1			2		1	1	1				1
100V	7	1						1		2	4			2			1		2	
95V	6	1									4	1				2	1	1		4

FIGURE 6; MULTIPLE PULSE RESULTS ON 3N128 MOSFETS

Voltage Level	Pulses to Failure						
	1	6	7	8	50	75	200
5000V	5	1	1				3
4250V	7			1			2
3500V	5						5
2750V	1				1	1	7
2000V							10

FIGURE 7: MULTIPLE PULSE RESULTS ON FIRST 50 54L04 DEVICES

Voltage Level	Number of Pulses to Failure							
	1	2	3	4	8	125	175	200
5750V	10							
5000V	7	1					1	1
4250V	9							1
3500V	4			2	1			3
2750	1		1		1	1	2	4

FIGURE 8: MULTIPLE PULSE RESULTS ON THE SECOND 50 54104 DEVICES

7.0 LIFE TEST CONDITIONS

Life tests were conducted at 25°C and 75°C. The life test conditions are given in Figure 9.

Part Type	Life Test Conditions
3N128	V_{GS} = -8V, V_{DS} = 0V, 1 Meg ohm series resistance
54L04	V_{CC} = 5.0V, V_{SS} = 0V, V_{IN} = 0 to 3.0V Peak, F_{IN} = 100KHz, duty cycle = 50%

FIGURE 9: LIFE TEST CONDITIONS

All of the devices of each part type were connected in parallel using appropriate device sockets on PC boards in groups of 16 to 20 devices. These groups of devices were coupled to the indicated supply voltages through series current limiting resistors although particular devices that were severely damaged by ESD had individual current limiting resistors to avoid dropping the overall voltage on a particular group. Individual resistors for each device were not used in order to reduce construction time and expense.

Life tests were conducted at 25°C and 75°C for 480 hours minimum at each temperature. The 25°C life test was selected because this is the most common condition to be encountered in actual usage. Also, a paper by Schwank[3] reported that ESD failures in CMOS devices annealed when exposed to high temperature life test conditions. Test parameter measurements were taken at or near 120, 240, and 480 hours. This interval was felt to be adequate to detect possible intermittencies in the ESD failures. All ESD samples were put on life test regardless of the level of damage since even the severely damaged devices could become latent failures if the damage became intermittent. Life test circuit measurements were made regularly to detect any possible bias voltage changes during the life tests. When at 75°C, the devices were allowed to cool to room temperature under bias before removing power from the devices. Because of the extensive measurement times involved, the life test samples were at room temperature with no bias for approximately 8 hours at each measurement time indicated on the data sheets. Another period of several days when ESD samples were at room temperature with no bias existed between the time the final ESD exposure measurement was taken and the time that the initial life test measurement was taken. Control devices which received no intentional ESD exposures were included in the life test samples.

8.0 LIFE TEST RESULTS

The total sample that was used for the latent failure life test is tabulated in Figure 10.

Device Type	Preliminary Samples (P)	Multiple Pulse Samples (M)	Single-Pulse Samples (S)	Non-Pulsed Controls (C)
2N128	12	100	40	68
54L04	30	100	40	50

FIGURE 10: LIFE TEST SAMPLE

8.1 Non-Degraded Parts

Those devices with no initial degradation in general remained rather stable throughout the life tests. This is particularly true of the 54L04 devices, and it is true of the 3N128 devices where there was definitely no initial degradation. There were some 3N128 devices, however, that, although meeting our accept criteria, had some upward shifts in V_{GS}(off) after ESD pulsing. These devices showing marginal initial degradation include multiple pulsed (200 pulses) samples 54, 57, 58, 75, 87 and 105 and single pulse samples 113, 115, 117 to 120, 123, 125, 128 to 132, 134, 135, 138, 139, 145 to 148 and 150.

Of these, the single-pulsed devices basically remained rather stable after the initial upward shift with no inductions of latent degradation. The multiple pulsed devices on the other hand showed a tendency toward gradual lowering of V_{GS}(off) after the initial upward shift. The data for these is given in Figure 11.

3N128 Device	Initial V_{GS} (off)	Post 200 Zaps	Start 25°C Burn-in	120 hrs. 25°C	312 hrs. 25°C	648 hrs 25°C	304 hrs 75°C	465 hrs 75°C	840 hrs 75°C
54	-1.454V	-4.258V	-2.247V	-3.836V	-3.972V	-4.297V	.946V	.851V	.917V
57	-1.718V	-5.94V	-3.556	4.6V	-4.7V	-4.7V	-2.9V	-2.4V	-2.6V
58	-2.119V	-7.5V	-5.6V	-6.3V	-6.3V	-6.5V	-3.6V	-3.8V	-3.7V
75	-1.533V	-6.2V	-3.7V	-6.1V	-5.2V	-5.4V	-2.8V	-2.6V	-2.6V
87	-1.7V	-6.8V	-6.8V	-5.8V	-6.0V	-6.1V	-2.8V	-2.9V	-2.9V
105	-1.4V	-3.8V	-3.8V	-3.3V	-3.5V	-3.8V	-.752V	-.503V	-.294V

FIGURE 11: MARGINALLY DEGRADED 3N128'S LIFE TEST DATA

First, we must highlight device #105, which has resulted in a definite out-of-specification drift after 840 hours at 75^{o}C. This appears to be a classic MAC 1 latent failure. Device 54 appears to be headed in the same direction, since V_{GS} (off) has already drifted below its initial value. The remainder of the devices could either be heading toward an out-of-specification condition or stability; it is impossible to know without further testing.

8.2 Degraded Parts

The 3N128 initial degradation was usually evidenced by either an out-of-specification V_{GS} (off) or a large (fraction of one picoamp to greater than 10 micro-amps) shift in I_{GSSR}. Of the 64 devices exhibiting high I_{GSSR} after ESD exposure, all devices except five remained quite stable.

Devices 36 and 52 had I_{GSSR} of 36 a and 76 a, respectively, after zap. I_{GSSR} for these devices rose to 58 μa and 220 μa, respectively, at the start of life test, then remained quite stable. Devices 91, 109 and 149 all had > 180 μa I_{GSSR} after zap but showed some improvement during life test.

As far as the 41 V_{GSS} (off) failures are concerned, all either "improved" with time or remained stable. The vast majority of these had shifted to greater than -8.0V, and V_{GS} (off) was decreasing with time.

There was one exception to the general rule worth highlighting. Device 12P shifted from 1.6V to .497V after zap. The specification is .5V min. At the start of the test V_{GS} (off) was .4V. Through the entire life test it gradually improved to .459V.

There were four devices for which V_{GS} (off) was still in-spec but showed some interesting data. Devices 24M, 69M, 70M and 99M all had V_{GS} (off) shifted slightly downward after zap. The change is usually an increase in V_{GS} (off). These devices behaved as tabulated in Figure 12.

3N128 Device	V_{GS} (off) Initial	After Zap	Start 25°C Life	120 hrs 25°C	312 hrs 25°C	648 hrs 25°C	304 hrs 75°C	465 hrs 75°C	840 hrs 75°C
24M	-2.148V	-1.002V	1.016V	.832V	.868V	.887V	.842V	.879V	.877V
69M	2.177V	1.420V	.899V	.904V	.888V	.909V	.870V	.986V	1.012V
70M	2.156V	2.014V	1.605V	1.629V	1.626V	1.604V	1.615V	1.616V	1.520V
99M	2.55V	1.79V	1.79V	1.42V	1.45V	1.47V	1.24V	1.3V	1.2V

FIGURE 12: LIFE TEST DATA ON 3N128's WITH DECREASED V_{GS} (off)

The degraded 54L04 devices experienced either an order of magnitude increase in I_{IH} or a large increase in V_{OL}, although there were a few with lesser changes. The I_{IH} failures either remained stable or improved slightly during life test.

The V_{GS} (off) data showed that 52 devices were catastrophic failures (output stuck high) from the ESD exposure and remained failures throughout life tests. There were 24 V_{GS} failures that improved during life test. But most interesting is the data in Figure 13 showing how 9 devices failed in the stick-high condition during life test. All were National Semiconductor.

8.3 Control Device Behavior

All control devices of both part types were very stable throughout the life tests. There were 68 3N128 MOSFET devices and 50 54L04 devices in the control sample.

54L04 Device	Initial V_{OL}	After Zap	Start 25°C Life	120 Hrs 25°C Life	456 Hrs 25°C Life	696 Hrs 25°C Life	134 Hrs 75°C Life	294 Hrs 75°C Life	648 Hrs. 75°C Life
5P	.4 μa .18V	.33V	.379V	.220V	5V	5V	5V	5V	5V
16P	162 na .166V	.92V	.96V	.96V	1.4V	.85V	5V	5V	5V
27P	139 na .170V	.124V	.146V	5V	5V	5V	5V	5V	5V
43M	170 na .174V	2.7V	2.8V	5V	5V	5V	5V	5V	5V
81M	98 na .174V	.167V	1.4V	2.185V	5V	5V	5V	5V	5V
84M	100 na .173V	.265V	.224V	.218V	3.08V	.275V	5V	5V	5V
133S	94 na .168V	5V	5V	4.8V	2.475V	.349V	5V	4.7V	3.0V
134S	98 na .171V	.209V	.205V	.204V	.229V	.222V	5V	5V	5V
165S	90 na .172V	.260V	.329V	4.968V	4.684V	5V	5V	5V	.382V

FIGURE 13: 54L04 LIFE TEST DEGRADED DEVICES

9.0 DATA FROM LATENT STUDY I

Latent Study I data revealed numerous parts that degraded in time from an out-of-specification condition to a worse condition. The initial out-of-specification condition was usually after ESD exposure. Could these parts possibly have functioned in a higher assembly application while in condition 1, even though out of spec limits, and then cause a malfunction at the higher assembly level after further degradation with time? This would meet type 3 latent failure definition given in section 2.0 Introduction. The parts of interest from Latent Study I are tabulated in Figures 14 and 15.

Part Type	Device #	Parameter Limit	Condition 1	Condition 2
3N170 MOS Fet	99	I_{GSSR} = 10 pa	3.4 na	1.4 na
	26	I_{DSS} = 10 na	70 na	330 na
	51	I_{DSS} = 10 na	12 na	60 na
2N4416 JFET	4	I_{GSS} = .1 na	3 na	11 na
	5	I_{GSS} = .1 na	5.8 µa	8 µa
	12	I_{GSS} = .1 na	15 na	26 na
	34	I_{GSS} = .1 na	50 na	230 na
	11	V_{GS} = -30V	4.3V	.003V
1N5711 Schottky Diode	13	I_P = 200 na	305 na	400 na
	13 (later)		250 na	260 na
	19		.6 µa	1.2 µa
	21		5 µa	17 µa
	25		18 µa	60 µa
	26		220 na	240 na
	28		.05 µa	.4 µa
	32		4.6 µa	11 µa
	34		320 na	400 na
	41		1.6 µa	3.6 µa
	45		360 na	400 na
	30		360 na	440 na
	50 (later)		230 na	250 na
	58		25 µa	46 µa
	78		1 µa	4.2 µa
	79		.6 µa	4.6 µa
	80		1.2 µa	2.4 µa
	84		215 na	250 na
	97		18 µa	23 µa
	103		130 na	290 na

FIGURE 14: LATENT STUDY I, LIFE DEGRADED DISCREET DEVICES

Part Type	Device #	Parameter Limit	Condition 1	Condition 2
5404 TTL Device	8	I_{1H} = 40 µa	230 µa	280 µa
	22		220 µa	390 µa
	40		180 µa	200 µa
	61		120 µa	500 µa
54S04 Schottky TTL Device	2	I_{iH} = 50 µa	540 µa	600 µa
	6		340 µa	600 µa
	8		96 µa	140 µa
	32		500 µa	680 µa
	42		500 µa	660 µa
	45		420 µa	540 µa
	51		140 µa	180 µa
	59		460 µa	560 µa
	64		260 µa	540 µa
	70		540 µa	780 µa
	73		140 µa	380 µa
	92		160 µa	360 µa

FIGURE 15: LATENT STUDY I, LIFE DEGREDED I.C.'S

10.0 CONCLUSIONS

- Latent ESD failures are a reality
- Unit 105 of the 3N128 devices was a classic MAC 1 latent failure
- Unit 12 of the 3N128 devices could be regarded as a marginal MAC 1 latent failure
- 54L04 units 27, 81, 84, 134 and 165 are classic MAC 1 latent failures
- 54L04 unit 5 is a MAC 1 latent failure but somewhat marginal
- 54L04 units 16 and 43 could be MAC 3 latent failures in applications where the original out-of-limits conditions, .92V and 2.7V, respectively, might still permit acceptable operation at the higher assembly level
- 54L04 unit 133 could be regarded as a weak MAC 3 latent failure under the double conditions that:
  - Operation was first monitored after the equivalent of 134 hours' operation at 75°C
  - The unit was in an application where the .349V out-of-limits V_{OL} parameter did not cause higher assembly failure
- A large percentage of ESD-damaged devices are likely to improve during life
- The stable behavior of the significant number of control devices in Latent Study II lends credence to the conclusions that the latent failures were due to ESD and discounts the involvements of some other mechanism

- As for the data from Latent Study I (Figures 14 and 15), one can draw his own conclusions as to whether or not there might be designs with sufficient margin to permit a higher assembly to function in condition 1 and yet fail when condition 2 is reached. We believe that this is certainly possible for some of the devices listed.

NOTE: The 1N5711 devices' increase in I_R leakage can probably be disregarded. Numerous control devices behaved in a similar fashion, so the change is most likely due to a mechanism other than ESD.

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