NASA CR-168076

20 GHz IMPATT TRANSMITTER

BY

J.L. CHAN AND C. SUN

TRW
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16. Abstract

This final report details the engineering development of a solid-state transmitter amplifier operating in the 20-GHz frequency band. The development effort involved a variety of disciplines including IMPATT device development, circulator design, single- and multiple-diode circuit designs, and amplifier integration and test.

The result of this effort is the development of a three-stage IMPATT diode amplifier capable of a 16-W CW output and a 2-dB bandwidth of 117 MHz. Although the figures fall short of the program goals of 20 W and 500 MHz, they represent a significant advance in the state-of-the-art in both device and circuit technologies in K-band frequencies. On the component side, high performance circulators with a 0.2-dB insertion loss and bandwidth of 5 GHz were fabricated. State-of-the-art GaAs IMPATT diodes incorporating diamond heat-sink and double-Read profile were also developed as a result of the program. The diodes are capable of a 2.5-W CW output. A few diodes achieved rf power outputs as high as 3 W. On the circuit side, high gain (up to 12 dB per stage) single-diode multituned circuits capable of 2 GHz and 930 MHz bandwidth were developed as the first and second stages, respectively, of the amplifier. A 12-diode waveguide cavity combiner was developed as the output stage.

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FOREWORD

The work and effort described in this report were the result of a program initiated by NASA/Lewis Research Center (LeRC). Mr. G. J. Chomos, Spacecraft Technology Division, LeRC, was the program manager for NASA.

The work was performed by TRW under NASA Contract NAS3-22492 for a program duration from August 1980 to July 1982. Raytheon was the subcontractor responsible for the development of IMPATT diodes used in the program. The TRW team was under the direction of Dr. C. Sun and consisted of Dr. Y. C. Ngan, Messrs. J. L. Chan, J. Douglass, R. Ebert and G. H. Shimamoto, all of the Millimeter Wave Department, TRW/Electronic Systems Group. The Raytheon team consisted of Drs./Messrs. M. G. Adlerstein, B. D. Lauterwasser, D. Masse, J. W. McClymonds and S. R. Steele, all of Raytheon's Research Division.

Prof. G. C. Dalman served as technical consultant during the period from September 1980 to May 1981, while he was on sabbatical leave from Cornell University. The contributions and directions by Dr. T. T. Fong of TRW are also acknowledged.

ABSTRACT

This final report details the engineering development of a solid-state transmitter amplifier operating in the 20-GHz frequency band. The development effort involved a variety of disciplines including IMPATT device development, circulator design, single- and multiple-diode circuit designs, and amplifier integration and test.

The result of this effort is the development of a three-stage IMPATT diode amplifier capable of a 16-W CW output and a 2-dB bandwidth of 117 MHz. Although the figures fall short of the program goals of 20 W and 500 MHz, they represent a significant advance in the state-of-the-art in both device and circuit technologies in K-band frequencies. On the component side, high performance circulators with a 0.2-dB insertion loss and bandwidth of 5 GHz were fabricated. State-of-the-art GaAs IMPATT diodes incorporating diamond heatsink and double-Read profile were also developed as a result of the program. The diodes are capable of a 2.5-W CW output. A few diodes achieved rf power outputs as high as 3 W. On the circuit side, high gain (up to 12 dB per stage) single-diode multituned circuits capable of 2 GHz and 930 MHz bandwidth were developed as the first and second stages, respectively, of the amplifier. A 12-diode waveguide cavity combiner was developed as the output stage.

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1.0 SUMMARY

This report details the engineering development of a solid-state transmitter amplifier operating in the 20-GHz frequency range. The development effort involved a variety of disciplines including IMPATT device development, circulator design, single- and multiple-diode circuit designs, and amplifier integration and test. The program objective was to develop a transmitter amplifier which would demonstrate the feasibility of providing an efficient, reliable, lightweight solid-state transmitter to be flown on a 30-20 GHz communication demonstration satellite. The work was performed under contract from NASA/Lewis Research Center for a period of two years.

The result of this effort is the development of a three-stage IMPATT diode amplifier capable of a 16-W CW output and a 2-dB bandwidth of 117 MHz. Although the figures fall short of the program goals of 20 W and 500 MHz, it represents a significant advance in the state-of-the-art in both device and circuit technologies in K-band frequencies. On the component side, high performance circulators with a 0.2 dB insertion loss and bandwidth of 5 GHz were fabricated. State-of-the-art GaAs IMPATT diodes incorporating diamond heat-sink and double-Read doping profile were also developed as a result of the program. The diodes are capable of a 2.5-W CW output. A few diodes achieved power outputs as high as 3 W. On the circuit side, high-gain (up to 12 dB per stage) single-diode, multituned circuits capable of 2 GHz and 930 MHz bandwidth were developed as the first and second stages, respectively, of the amplifier. A 12-diode waveguide cavity combiner was developed as the output stage. The output stage utilized commercially available single-drift GaAs IMPATT diodes. The better performance IMPATT diodes developed in the program were not available during the circuit development phase of the program. Although it is believed that the combiner circuit was capable of producing the required output power and bandwidth, however, subsequent measurements showed that due to the wide dispersion of characteristics of the commercial IMPATT diodes, the performance of the output stage was severely compromised.

It is concluded that further work is required on improving the production technique of the IMPATT diodes developed in the program. The purpose is to improve the yield factor of high performance diodes as well as to improve on the uniformity of the diodes. It is also recommended that the existing circuits be modified to accommodate the high performance diodes.

The contents of this report are summarized in the following. Section 2 describes the program objectives, specifications and requirements. Section 3 contains a detailed description of the entire transmitter amplifier. The section discusses the system configuration, individual IMPATT stages and diode bias circuits. Section 4 presents the design methodology, fabrication and performance of IMPATT diodes developed in the program. Section 5 contains discussions on circuit development of the various stages. Also included is key component development, such as circulators and current regulators. Section 6 discusses system integration. The section contains the amplifier schematic and other relevant electrical and mechanical drawings. A physical description and the interface requirements of the amplifier are also given in this section. Section 7 presents, for evaluation, measurement data obtained from functional, noise and environmental tests. Section 8 discusses the overall achievement of the program, the implications of the results, and the assessment of the future development needs. All discussions which are mostly mathematical in nature are presented as appendices in order not to obscure the presentation in the other sections. Finally, all references used for the report are listed at the end of the report.

2.0 INTRODUCTION

This report details the development of a 20-W CW solid-state amplifier operating at 20 GHz. The performance represents a significant advance in the state-of-the-art in both device and circuit technology in K-band frequencies. The development program was conducted over a period of two years, from August 1980 to July 1982. The development effort involved a variety of disciplines including IMPATT device development, circulator design, multiple diode circuit design and amplifier integration and test.

The amplifier development program is one part of a larger effort for the development of a millimeter-wave satellite communication system. Present studies of the growth in communication traffic indicate that the frequency spectrum allocated to fixed service satellites at C- and Ku-bands will reach saturation by the early 1990's. Ka-band with uplink at 27.5-30.0 GHz and downlink at 17.7-20.2 GHz is the next higher frequency band allocated for this purpose. Current plans for development of a satellite system to implement this band include the possibility of a NASA demonstration satellite in the mid-1980's. System studies have identified the use of multibeam antenna systems as a major factor in achieving minimal cost and efficient use of frequency and orbital resource. Such multibeam systems, however, require reliable, efficient, lightweight, solid-state transmitters which have been identified as one of the key areas in which technology development is needed. The amplifier development program described in this report resulted from such a need.

2.1 PROGRAM OBJECTIVES

One objective of the program was to develop a 20-GHz transmitter amplifier which will demonstrate the feasibility of providing an efficient, reliable, lightweight IMPATT transmitter to be flown on a 30/20 GHz communication demonstration satellite. Since high efficiency and high power IMPATT diodes, as well as high quality, reliable circulators were not currently available in the K-band frequencies, it was the objective of the program, also, to develop GaAs double-drift IMPATT diodes and high quality circulators to be used in the transmitter amplifier.

2.2 REQUIREMENTS

Requirements for the amplifier consistent with the program objectives were established and are presented in the following.

General Requirements

The program shall develop a space-flight qualifiable transmitter. The transmitter shall be a three-stage design consisting of a low power input stage, an intermediate driving stage, and a high power output stage. The transmitter shall be capable of continuous operation for a prolonged period. In addition, the transmitter shall be an all-solid-state design incorporating high power and high efficiency GaAs IMPATT diodes of the type developed in the program.

System Requirements

Note: All criteria are specified at maximum output power and for the entire operating frequency band.

RF Output Power

The maximum RF output power of the transmitter at the 1-dB gain compression point shall be no less than 20 W CW. The load shall be characterized by a VSWR of less than 1.3.

Operating Frequency Band

The operating RF band shall be from 19.7 GHz to 20.2 GHz.

RF Power Gain

The transmitter shall have an RF power gain of no less than 30 ±1 dB at the gain compression point.

Gain Variation

The RF gain in reference to various carrier frequencies shall not vary more than ±1.0 dB.

Gain Slope

The rate of change of output power with carrier frequency shall not exceed 0.15 dB over any 1 MHz portion of the operating frequency band.

Phase Linearity

The phase shift at the transmitter output shall not deviate from linear phase shift more than 10 degrees peak-to-peak.

Group Delay Variation

The rate of change of phase shift versus carrier frequency or group delay shall not vary more than 0.5 nsec peak-to-peak over any 50-MHz portion of the operating frequency range.

Harmonic and Spurious Responses

The harmonic output shall be at least 50 dB below the carrier. The spurious output shall be at least 60 dB below the carrier.

AM/PM Conversion

The transmitter phase shift shall not exceed 5 ±1° per dB of input power variation.

DC-to-RF Conversion Efficiency

The ratio $(P_o-P_{in})/P_{dc}$, where P_o is the RF output power, P_{in} is the RF input power, and P_{dc} is the DC input power, shall be no less than 18% for the entire transmitter. The criteria cover both RF circuit and DC circuit efficiencies.

2.2.4 Interface and Installation Requirements

DC Requirements

The transmitter shall require a DC supply with a nominal voltage of 28 V DC. The DC source shall have a voltage regulation of better than 1% and a current capacity of 3 A.

RF Input Requirements

Input Connection - the input port shall accept a WR-42 waveguide with a UG 595/U flange.

Input Frequency - The input signal shall be a single frequency within the range from 19.7 to 20.2 GHz.

Input Power - The power of the input signal shall be 0.02 W CW minimum and shall not exceed 0.064 W CW.

RF Output Requirements

Output Connection - The output port shall accept a WR-42 waveguide with a UG 595/U flange.

Load Requirement - The RF load of the transmitter shall be capable of accepting RF power up to 25 W CW. The load shall have a VSWR of not more than 1.3.

Control and Monitoring Functions

There shall be no control and monitoring functions associated with the transmitter.

Cooling

The cooling of the transmitter shall be achieved by thermal conduction. The transmitter shall be mounted on a baseplate maintained in a temperature range of 0°C to 75°C.

Physical Profile

The transmitter shall be of minimum dimensions and weight such that it is possible to mount the unit in the antenna feed structure.

3. SYSTEM DESIGN

3.1 GENERAL DESCRIPTION

In order to satisfy the gain requirement (≃30 dB) while providing the required bandwidth, a three-stage amplifier circuit was adopted. Figure 3-1 depicts graphically the system configuration. There are six 3-port circulators connected in cascade in the circuit. Three of the circulators are used in conjunction with the one-port IMPATT stages to provide the necessary input and output separations. The remaining circulators are connected as isolators to provide adequate isolation between IMPATT stages and from the signal source. Each IMPATT diode in the amplifier system is powered by its own power supply.

3.2 GAIN DISTRIBUTION

The IMPATT consists of three stages: an input stage, a driver stage and an output stage. The power gain assigned to each stage is shown in Table 3-1. It should be noted that the first stage alone contributes some 54% of the total amplification in the system. A description of the method used for assigning power gain to the stages follows.

The three IMPATT stages are designed to operate in the injection locking mode, that is, each stage operates as a self-excited oscillator with the oscillation frequency synchronized to that of the input signal. The bandwidth of an injection-locked stage is the frequency range in which the oscillator maintains synchronization with the input signal. The injection-locking mode of operation provides, in general, a higher power gain and better DC-to-RF conversion efficiency than the stable mode of operation. In the injection-locking mode, the stage gain is inversely related to the bandwidth of the stage. A first order analysis [1,2] shows that, assuming a single-tuned circuit, the injection-locking bandwidth of a single stage can be determined by:

$$\Delta f = \frac{2f_o}{Q_x} \frac{1}{\sqrt{G}} \qquad (2\text{-}1)$$

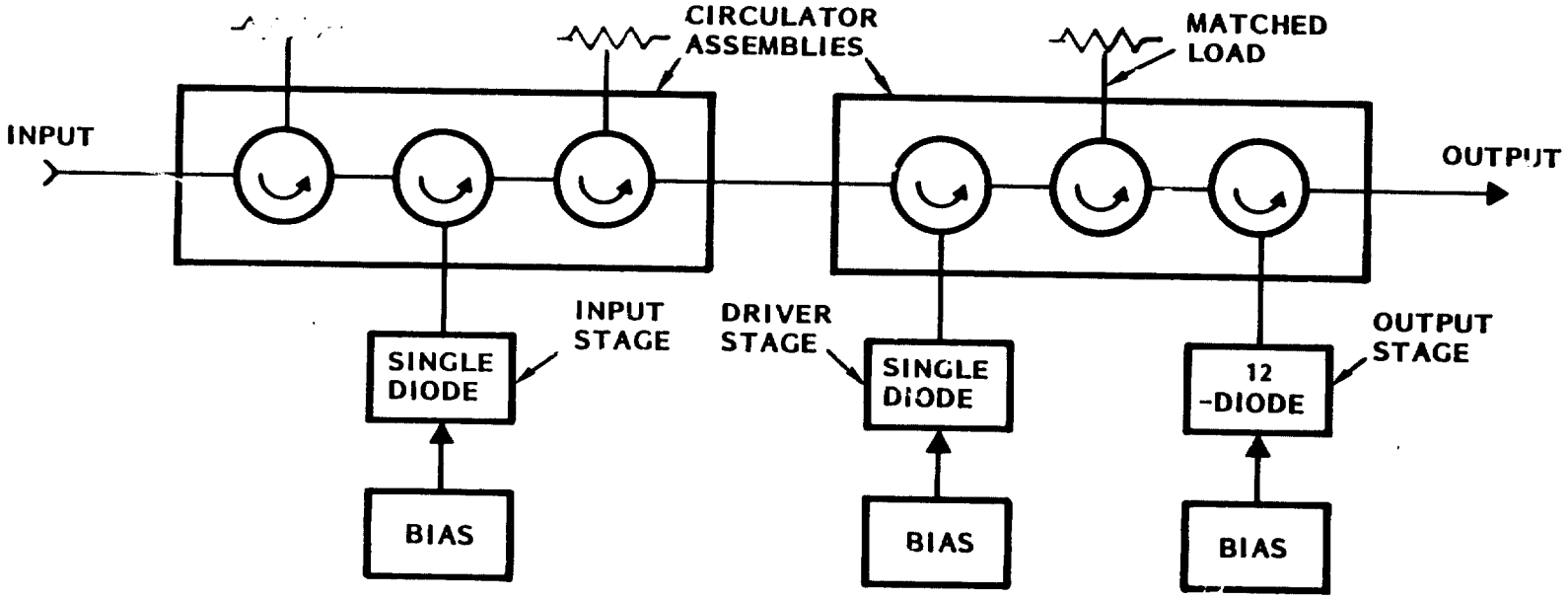


Figure 3-1. Three-State Amplifier Configuration

TABLE 3-1. AMPLIFIER GAIN DISTRIBUTION

	Power Input	Gain (Including Circulator Losa)	Power Output
Input Stage	0.02 W	17.5 (+12.4 dB)	0.35 W
Driver Stage	0.35 W	7.2 (+8.57 dB)	2.52 W
Output Stage	2.52 W	8 (+9 dB)	20.16 W

where Δf = injection-locking bandwidth,

f_o = oscillator free-run frequency,

Q_x = external Q of the oscillator,

G = power gain = P_{out}/P_{in}.

For a wide injection-locking bandwidth, f_o is usually adjusted to situate at the center of the frequency band desired and Q_x and G set to the lowest limits which the design allows. In practice, however, Q_x is limited to 20 or higher. A high circuit Q (Q_x included) is essential in maintaining a spurious-free oscillation in a high power stage. The remaining option is therefore to lower the power gain, G.

By a high power stage one implies that the IMPATT diode(s) is biased at or near its maximum capacity. The output stage is, of necessity, a high power stage. The gain assigned to this stage is 8. Assuming the external Q can be lowered to 25, then, from the first order approximation of Eq. (2-1), the injection-locking bandwidth of this stage is calculated to be 565 MHz. The actual bandwidth, however, was found to be narrower. This was attributed to the fact that the twelve commercial IMPATT diodes used in this stage were of dissimilar characteristics, despite the effort of matching the diodes. Lowering the stage gain further to widen the bandwidth was found not to be the solution. It was found that the increased input power drove the IMPATT diodes into saturation and that the output power actually decreased and appeared to be noisy. It was decided finally that the output stage gain was to remain at 8.

The driver stage is also a power stage. The bandwidth of this stage is more than that of the output stage, the reason being that additional bandwidth is required to ensure spectral integrity at the band edges of the output stage since the latter is synchronized to the driver stage. The gain assigned to the driver stage is 7.2. The gain was not lowered further because a fourth stage would be needed to make up the required system gain. Instead, a multituned circuit was used to provide the additional bandwidth. As shown in Appendix A (see also [3]), a properly designed multituned circuit can provide a superior power bandwidth product as compared to a single-tuned circuit. It should be pointed out here that a multituned circuit is yet to be developed for use with multiple IMPATT diodes.

The input stage is operating as a low-power amplifier. High gain can be provided by this stage without introducing any spurious spectrum. The gain assigned to this stage is 17.5 or some 54% of the total system amplification. On the other hand, an injection locking bandwidth of greater than 800 MHz is required for this stage in order to overlap the operating bands of the driver and the output stages. To provide the necessary bandwidth, a low Q_x of about 10 is needed. Although a low circuit Q is permissible for the low power stage where IMPATT nonlinearity is not profound, it is doubtful that such a low Q_x can be realized in practice. For this reason, a multituned circuit was again adopted for the input stage.

3.3 IMPATT DIODE ALLOCATION

It was the expectation of this program that high power (up to 4 W) IMPATT diodes would be developed by Raytheon, the diode subcontractor, in the early stage of the program to be in time for circuit development. Due to technical difficulties, the IMPATT diodes were not developed until close to the concluding phase of the program; the optimum power achieved then was 2.5 W per diode. A decision was made that commercially available GaAs IMPATT diodes would be used in the amplifier, since the circuit development effort could not be delayed without extending the overall program schedule. The commercial diodes selected were manufactured by the Varian Corporation. The optimum power obtainable from these devices was 1.2 W per diode. (More discussion on diode performance is presented in Section 4.)

To satisfy the power budget shown in Table 3-1, diode allocation for the IMPATT stages was, with the Varian diodes in mind, one diode for the input stage, two diodes for the driver stage, and twelve diodes for the output stage. This allocation provided maximum power extraction from each IMPATT diode while not overloading the device. However, difficulty arose from the driver stage. To combine two diodes in one stage, a relatively high Q ($Q_x \simeq 20$) cavity circuit must be used, as pointed out in Section 5.2. It was found that the cavity circuit suffers from poor gain-bandwidth product and that the driver stage was not able to deliver sufficient power at the band edges to the output stage. Consequently, it was decided that a multiple-tuned, single-diode circuit is necessary to meet the requirements for the driver stage. One problem remained, however. The commercial Varian diode could not provide the required

2.5 W output power in a single-diode circuit; a higher power IMPATT diode was needed. The problem was not solved until the concluding phase of the program, when Raytheon successfully developed the 2.5-W diodes in sufficient quantity. The final amplifier configuration consists, therefore, of a single-diode (Varian) input stage, a single-diode (Raytheon) driver stage, and a twelve-diode (Varian) output stage. Schedule limitations did not allow the refitting of all three stages to use the higher power Raytheon diodes.

3.4 CONSTANT VOLTAGE BIASING

It is well known that in the avalanche breakdown mode, the IMPATT diode behaves very much like a zener diode; that is, as far as the bias supply is concerned, the IMPATT diode acts as a constant voltage device. For this reason, a constant current source has always been used without exception to bias an IMPATT diode. Recently, it was reported [4] that an IMPATT diode operating in the amplifier mode has been successfully biased by a constant voltage source with encouraging results. The report claimed that by using constant voltage biasing, improved amplifier linearity and stability could be obtained while increasing the overall DC-to-RF conversion efficiency. Inspired by the finding, it was decided that constant voltage bias would be tried on the IMPATT stages operating in the injection-locked oscillator mode.

The attempt was successful. Improvement of stability was not noticed. It appeared that for a well-designed circuit, the IMPATT diode is stable with either constant current bias or constant voltage bias. Similarly, improvement of amplifier linearity was not observed since, in an objection locking mode, only the output frequency follows that of the input; the output power remains more or less constant. One distinct advantage was realized, however. The amplifier, when operated under constant voltage bias, offered superior thermal property than when it was under constant current bias. For any reverse-biased semiconductor junctions, Si and GaAs included, the decreased ionization rate at high temperature gives rise to a positive temperature coefficient of breakdown voltage. A good approximation of the breakdown voltage-temperature relationship was found to be:

$$V_b(T_j) = V_b(T_o)\ [1 + \beta(T_j - T_o)] \qquad (3\text{-}2)$$

where T_j is the junction temperature, T_o is the reference temperature, $V_b(T_o)$ is the breakdown voltage at T_o, and β is the normalized temperature coefficient defined by:

$$\beta = \frac{1}{V_b(T_o)} \frac{dV_b(T_j)}{dT_j} \tag{3-3}$$

Rise of the junction temperature, T_j, is caused by external heating (due to rise of the ambient temperature) and internal heating (due to power dissipation in the diode).

When the device is operating under constant current bias, any increase in ambient temperature results in an increase of not only the junction temperature, but also the increase in breakdown voltage. Consequently, power dissipation in the diode is increased, in turn causing the junction temperature to further elevate. This is the well-known thermal runaway phenomenon which can lead eventually to the destruction of the device.

If the device is operating under constant voltage bias, it can be shown (see Appendix B) that the junction temperature actually rises at a slower rate than the rise of the ambient temperature. This action results from the increase in diode breakdown voltage, according to Eq. (3-2), as external heating takes place. Since the diode voltage is kept constant, the diode current decreases. This is followed by a decrease in power dissipated in the diode and by a decrease in junction temperature. Hence, the device is prevented from thermal runaway. It was shown [5,6] that output RF power of an IMPATT diode is proportional to the square of diode current. The price for the thermal protection is thus a graceful degradation of output power with ambient temperature elevation. Appendix B shows that the output power as a function of junction temperature can be expressed approximately as:

$$P_o = k(c_1^2 + d_1^2\Delta T^2 - 2c_1 d_1 \Delta T) \tag{3-4}$$

where k, a, b are constants defined in Appendix A, and $\Delta T = T - T_o$ is the relative ambient temperature. The output power decreases with temperature elevation at a rate equal to:

$$\frac{\Delta P_o}{\Delta T} = 2d_1^2 \Delta T - 2c_1 d_1 \tag{3-5}$$

The output power approaches zero as the temperature differential approaches a cutoff value defined as:

$$\Delta T_c = c_1/d_1 = \frac{V_d - V_b(T_o)}{\beta V_b(T_o)} \tag{3-6}$$

where V_d is the constant bias voltage. At relative temperature, which is equal to or above ΔT_c, the diode current is totally cut off.

In many applications in an extreme thermal environment, a graceful degradation in power with respect to temperature elevation is usually preferred over a catastrophic failure, such as a thermal runaway. It is well known that the failure rate of IMPATT diodes is directly related to the junction temperature and is described by the Arrhenius equation:

$$\lambda = \lambda_o \text{ EXP } (-E/kT) \tag{3-7}$$

where λ = failure rate, λ_o = a constant, E = activation energy, T = temperature, and k = Boltzmann's constant. For example, an increase of 28°C in junction temperature leads to a tenfold increase in failure rate. Similarly, if the junction temperature is cooler by 28°C, the failure rate drops tenfold. The advantage of constant voltage bias is obvious.

4.0 IMPATT DIODE DEVELOPMENT

It was anticipated at the beginning of the program that high power GaAs IMPATT devices would be developed in time to be used in the transmitter. However, due to various technical difficulties, this goal was not realized. Consequently, commercially-available IMPATT devices were purchased so that the circuit development effort could be carried out according to schedule. The commercial IMPATT diodes were manufactured by the Varian Corporation. Section 4.1 contains a description of these diodes together with some test data which are indicative of the diode performance and characteristics.

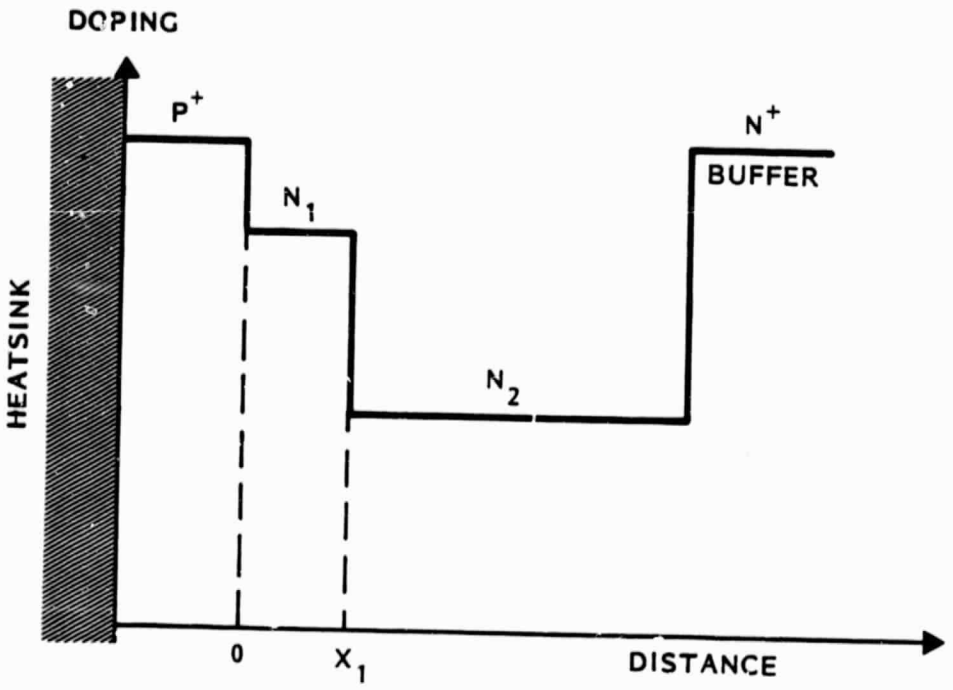
Although commercial devices were used in the amplifier design, effort for developing high performance diodes continued for the duration of the program. Indeed, IMPATT diodes with performance superior to commercial ones were developed near the end of the program. Section 4.2 contains a detailed report on the diode development effort. The report was prepared in whole by the Raytheon Company, the diode subcontractor to the program.

It should be noted that the diode output power figures quoted in the test data in Sections 4.1 and 4.2 were obtained with the test circuit optimally matched to the diode at one single frequency. For a wideband operation, such as the case of the amplifiers, the diode output capability must be degraded. This results from the fact that the power-bandwidth product of a single diode stage is invariant. That is to say, for a maximum output the bandwidth of the stage must be comparatively narrow. Conversely, for a large operating bandwidth, the output power must be lowered. The maximum output power obtainable from the wideband driver stage used in this program is about 1.2 W with the Varian diodes and 2.5 W with the Raytheon diodes.

4.1 VARIAN IMPATT DIODES

4.1.1 Description

The Varian IMPATT diodes were chosen based on the consideration of some desirable features. The diodes utilized a high-low single-drift Read doping profile and GaAs material, resulting in a high DC-to-RF conversion efficiency. A typical high-low doping is shown in Figure 4-1. The diode construction is based on a plated heat sink, high-temperature metallization process on $P^+N^+N^-N^+$ GaAs. This construction has the advantage of high efficiency and resistance to burnout. In summary, these diodes have the following features:



$N_1 = 1.7 \times 10^{17} cm^{-3}$ $\quad X_1 = 0.22\ \mu m$

$N_2 = 1.1 \times 10^{16} cm^{-3}$ $\quad \ell_N = 2.10\ \mu m$

Figure 4-1. Typical 20 GHz P^+ High-Low Simple Drift Read IMPATT Structure

- High CW output - up to 2 W at 20 GHz.
- High efficiency - typically 18%.
- Burnout resistance to circuit mismatches.
- High reliability.

In addition, the Varian diodes were housed in small packages pertinent to mm-wave operations. The small package helps to minimize the effect of the package parasitics from affecting circuit performance. An outline of the Varian diode package is shown in Figure 4-2a. Figure 4-2b contains an equivalent circuit representation of package parasitics. Figure 4-3 shows a calculated small-signal admittance for the P^+ high-low single-drift Read IMPATT structure shown in Figure 4-1. The calculation was based on an operating current density of 2500 A/cm^2 and a junction temperature of 200°C on the diode. A plot of diode impedance (diode resistance versus frequency and diode reactance versus frequency) as seen from the package terminals using Figures 4-3 and 4-2b is shown in Figure 4-4. As can be seen from the plot, the diode contains a negative resistance over a bandwidth of from 15 GHz to 28 GHz.

4.1.2 Test Data

A list of test data of the diode purchased is shown in Table 4-1. The data were provided by the diode supplier. It can be seen that, on the average, the diodes were capable of producing 1.5 W of CW power in the K-band frequency range. Actual usage also showed that the diodes were rugged and resistance to burnout due to circuit mismatch was excellent. However, uniformity of device characteristics such as output power and free-running frequency from diode-to-diode was poor. It should be pointed out that matching of device parameters such as free-running frequency and output power is of prime importance in a combiner circuit. The nonuniformity of the IMPATT diodes is one of the major limiting factors on the transmitter amplifier performance in this program (see Appendix C).

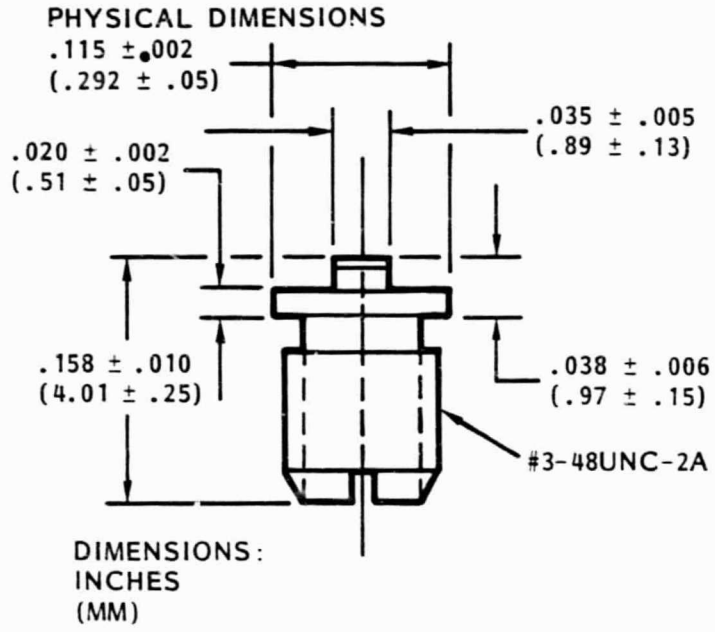


Figure 4-2a. Physical Parameters of Varian Package

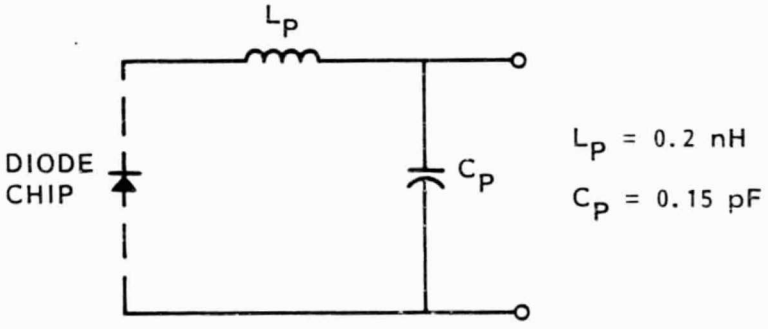


Figure 4-2b. An Equivalent Circuit for Varian Package

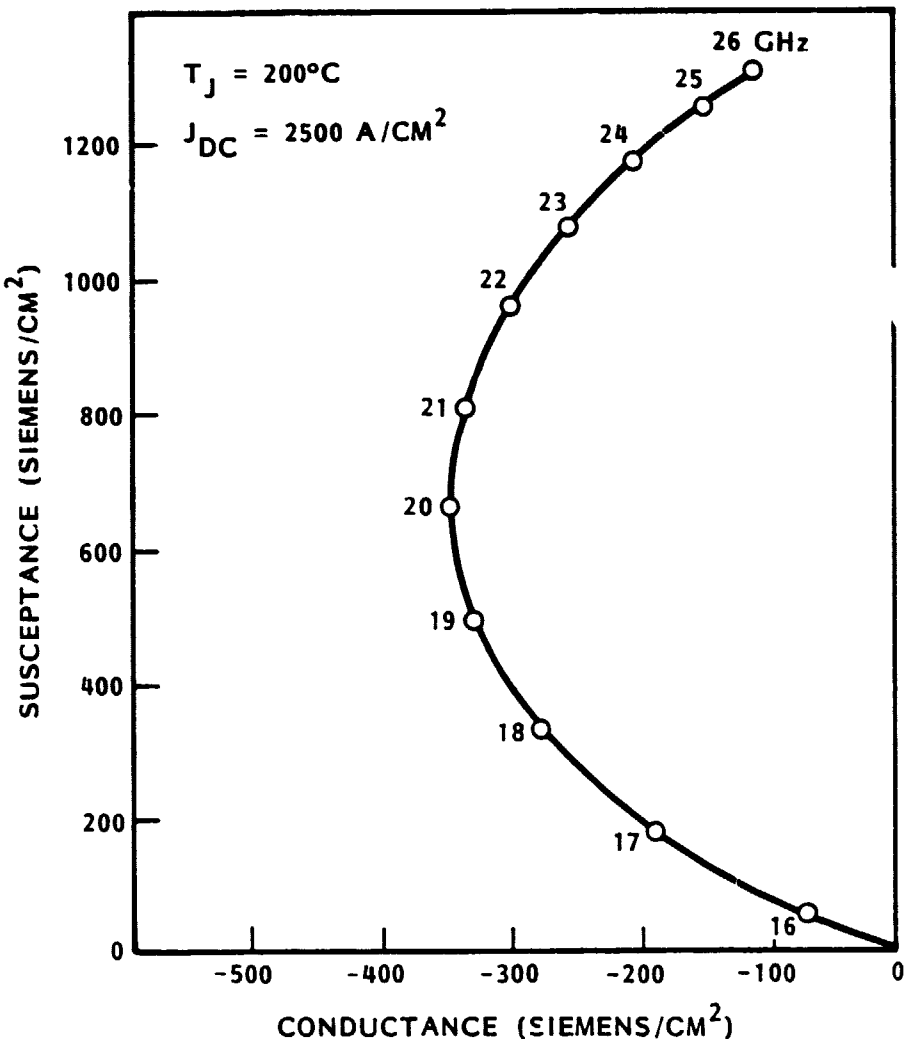


Figure 4-3. Calculated Small-Signal Admittance for P^+ High-Low Single Drift Read IMPATT Structure

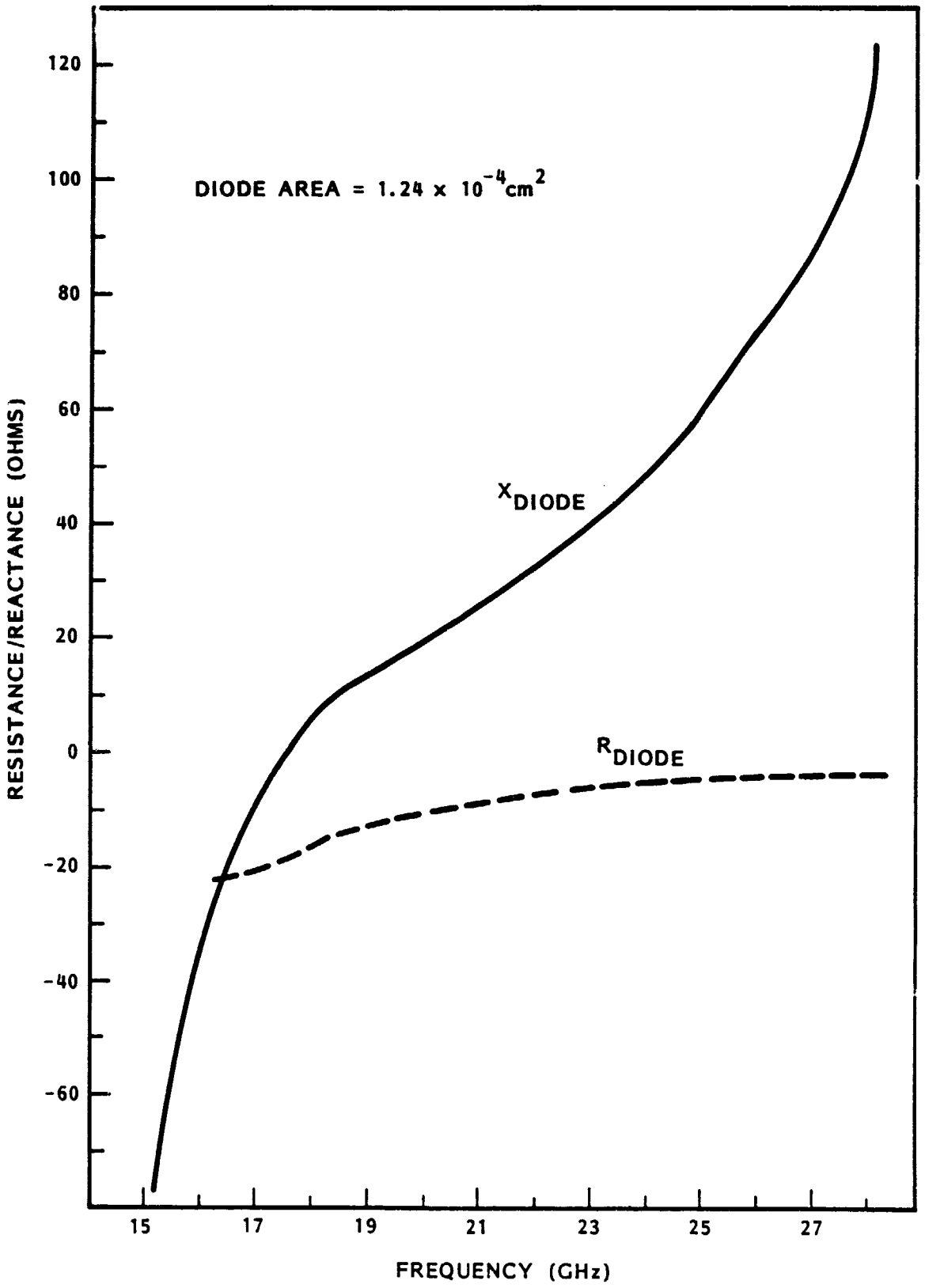


Figure 4-4. Typical Diode Impedance from Package Terminals

TABLE 4-1. TEST DATA OF VARIAN DEVICES

Wafer No.	Serial No.	V_B	V_{op}	I_{op}	Frequency	P_o	Efficiency
R103	3	15.4	27.9	.29	19.85	1.63	20.14
R103	4	16.0	28.4	.29	19.85	1.63	19.79
R103	5	15.4	28.4	.32	20.05	1.74	19.14
R103	6	15.4	29.0	.31	19.0	1.70	18.90
R103	7	15.2	27.8	.32	20.6	1.74	19.55
R103	8	15.2	28.3	.31	19.55	1.82	20.74
R103	9	15.2	21.9	.35	19.55	1.96	19.04
R103	10	15.3	29.0	.40	18.8	2.08	17.93
R103	11	15.2	28.94	.40	19.35	2.0	17.27
R103	12	15.2	28.5	.35	19.40	2.0	19.49
R107	1	12.5	25.1	.47	20.2	2.18	18.5
R107	2	12.0	26.0	.45	19.6	2.08	17.77
R107	3	13.0	25.3	.44	20.45	2.0	17.96
R107	4	15.1	28.0	.36	19.32	2.0	19.84
R107	5	14.6	26.4	.36	19.37	2.08	21.88
R107	6	12.5	25.7	.45	19.0	1.9	16.42
R107	7	12.3	26.0	.4	20.5	1.9	18.26
R107	8	13.0	25.4	.39	20.7	1.86	18.77
R107	9	15.0	27.7	.35	19.69	2.0	20.62
R107	10	15.1	25.9	.36	20.33	2.14	22.95
E1172	1	18.1	30.6	.4	19.0	1.95	15.93
E1172	2	19.0	31.2	.37	19.5	1.66	14.37
E1172	3	17.9	29.5	.42	20.05	1.75	14.12
E1172	4	18.0	30.8	.4	19.0	1.86	15.09
E1172	5	18.4	29.8	.32	20.5	1.66	17.4
E1172	6	18.8	30.9	.41	19.37	1.78	14.05
E1172	7	18.0	31.0	.35	19.6	1.71	15.76
E1172	8	18.4	30.9	.38	19.6	1.66	14.56
E1172	9	19.0	30.9	.37	20.4	1.82	15.91
E1172	10	18.0	30.0	.35	19.6	1.78	16.95

4.2 RAYTHEON IMPATT DIODES

A final report on Raytheon IMPATT diodes prepared by Raytheon Company is attached as Appendix D. The report describes material growth, fabrication, performance, reliability as well as design and modeling of diodes.

5.0 CIRCUIT DEVELOPMENT

As with other amplifier circuits employing two-terminal devices (e.g., IMPATT diodes), the circuit development in this program can be conveniently classified into four areas: input and driver stages, output stage, circulator, and bias regulator. A description of the development of these circuits is presented in the following sections.

5.1 INPUT AND DRIVER STAGES DEVELOPMENT

As indicated in the system considerations in Section 3.2, both the input and the driver stages are single-diode circuits. The two circuits are virtually identical in terms of circuit design and construction, the only difference being that the driver stage uses a higher power diode and a larger bias current. The two circuits will be discussed collectively in this section.

The main requirement of the single-diode stages is a large gain-bandwidth product. To achieve such an objective, the circuit used must provide a suitable impedance locus as seen by the IMPATT diode. An impedance locus is a plot of the circuit impedance as a function of the frequency $Z(\omega) = R(\omega) + jX(\omega)$ in the complex plane with jX as the vertical axis and R the horizontal axis. When the diode impedance as a function of frequency is also plotted on the same complex plane, the intersection of the two loci indicates the oscillation characteristics of the circuit. For example, the impedance locus of an IMPATT diode is a near-straight curve with a moderate slope; the impedance locus of a single-tuned circuit (a circuit with only one resonance) is always a vertical line. The two loci are plotted in Figure 5-1. The arrows on the curves indicate the direction of increasing frequency. The intersection of the two loci is a well-defined point. The output of this circuit has a narrow spectrum with well-defined amplitude and frequency characteristics as indicated in Figure 5-2a. The bandwidth characteristics of a single-tuned circuit are characterized by the rate of change of circuit reactance versus frequency, $\partial X/\partial\omega$ (or circuit susceptance versus frequency, $\partial B/\partial\omega$). A wide bandwidth is characterized by a small $\partial X/\partial\omega$. For a single-tuned circuit, such as the one shown in Figure 5-3a,

$$\frac{\partial X}{\partial \omega} = \frac{2R_L}{\omega} Q_x \qquad (5\text{-}1)$$

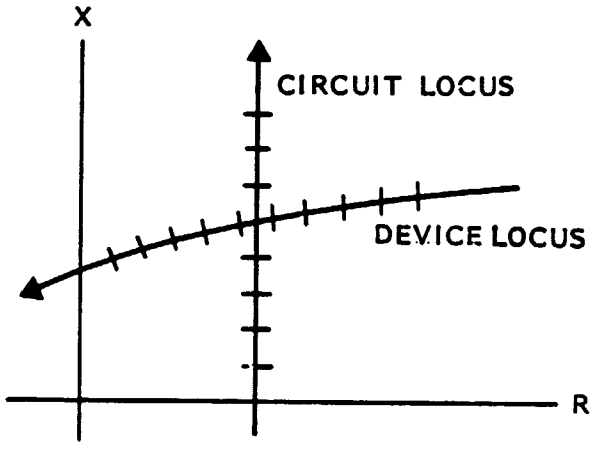
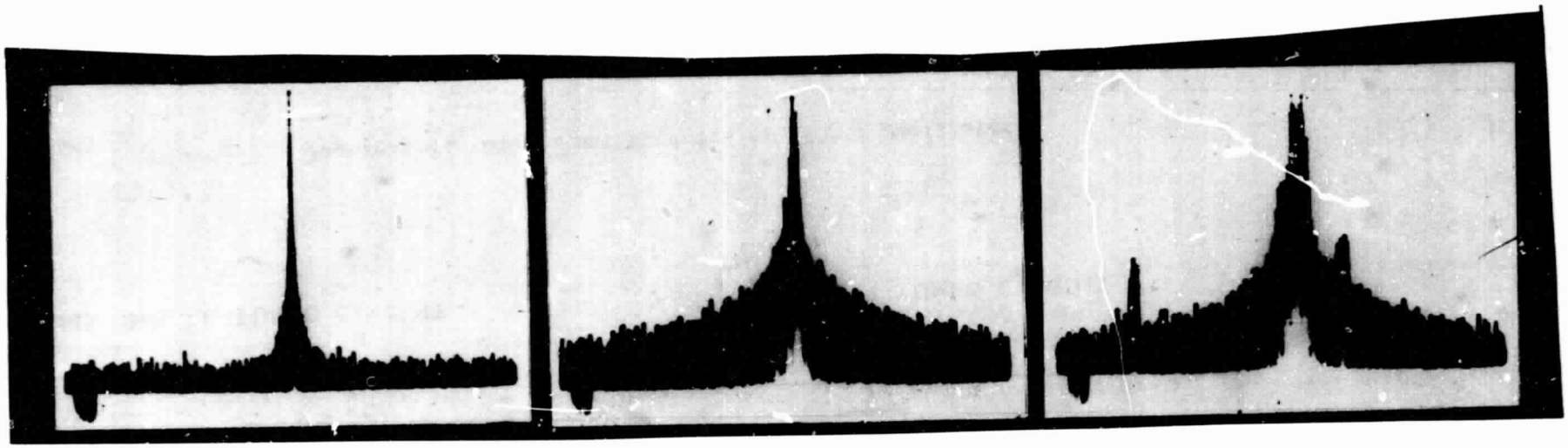


Figure 5-1. Impedance Logic of Single-Tuned Circuits



NORMAL OSCILLATION NOISY OSCILLATION MULTIPLE OSCILLATION

Figure 5-2. Possible Output Spectra of IMPATT Oscillators

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Figure 5-3. Equivalent Circuits of IMPATT Oscillators

where $Q_x = \omega L/R_L = 1/\omega R_L C$ and R_L = load resistance. The injection-locking bandwidth, $\Delta\omega$, of this circuit is [1,2]:

$$\Delta\omega = \frac{2\omega_o}{Q_x} \frac{1}{\sqrt{G}} \tag{5-2}$$

where ω_o = resonant frequency of the circuit and G = power output/power input. It is readily seen that a low Q factor is essential for wideband operations.

All waveguide oscillators are, however, multituned circuits (with more than one resonator). Circuits of this type possess a rather complicated impedance locus as indicated by three possible plots shown in Figure 5-4. The plot, shown in Figure 5-4a, is characterized by a smooth "bump" on the impedance locus centered at the resonant frequency. It can be shown that $\partial X/\partial\omega$ around the "bump" is smaller than the $\partial X/\partial\omega$ of the single-tuned circuit. Using a double-tuned circuit as an illustration, it is shown in Appendix A that the rate of change of reactance versus frequency is

$$\frac{\partial X}{\partial \omega} = \frac{2R_L}{\omega} Q_{eq} \tag{5-3}$$

where Q_{eq} is the equivalent Q-factor defined by

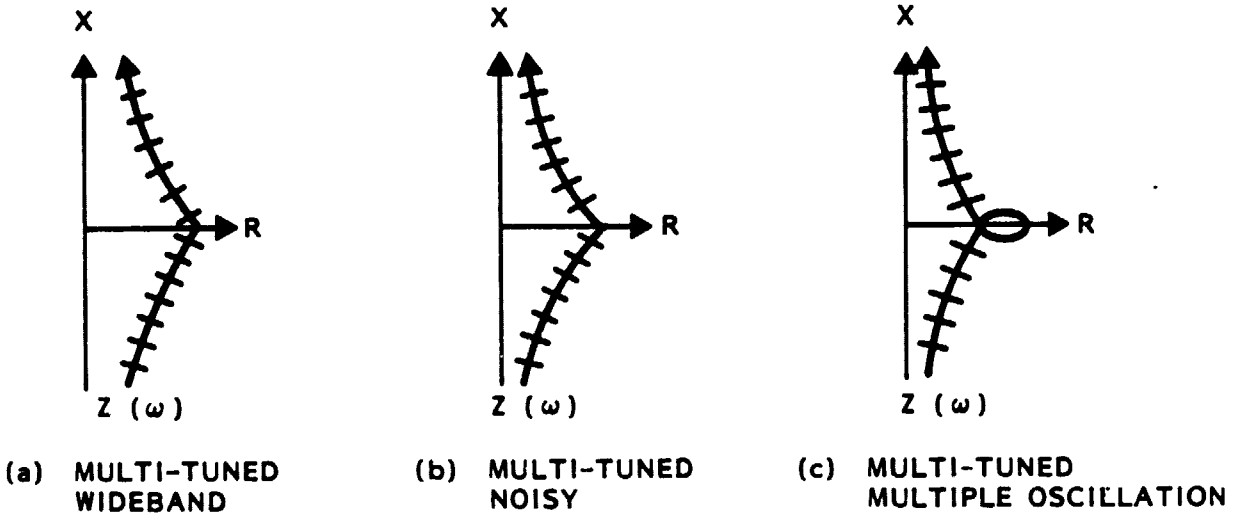
$$Q_{eq} = Q_1 - Q_2 \text{ (double-tuned circuit only)} \tag{5-4}$$

It is readily seen that even the individual Q's, Q_1 and Q_2, are high, the equivalent Q being the difference between Q_1 and Q_2 can be very small. The circuit is thus shown to be capable of wideband operations. In fact, the injection-locking bandwidth in this case is given by [3]

$$= \frac{2\omega_o}{Q_1 - Q_2} \frac{1}{\sqrt{G}} \tag{5-4}$$

with the restriction that Q_1 is larger than Q_2.

In the case of $Q_1 = Q_2$, $\partial X/\partial\omega$ is zero at the resonant frequency and a sharp peak is formed on the circuit impedance locus at the intersection with the diode impedance locus, as shown in Figure 5-4b. Since, at their intersection point, the circuit locus and the diode locus are virtually tangential, oscillation frequency and amplitude are not well defined, and the output has a noisy spectrum (see Figure 5-2b).



(a) MULTI-TUNED WIDEBAND

(b) MULTI-TUNED NOISY

(c) MULTI-TUNED MULTIPLE OSCILLATION

Figure 5-4. Impedance Loci of Multi-tuned Circuits

In the case of Q_1 being smaller than Q_2, the circuit locus forms a loop around the diode locus. It is easily seen that no less than two intersection points would be formed between the two loci. The result is that multiple oscillations would take place (see Figure 5-2c). The objective of designing a multituned oscillator circuit is, therefore, to avoid a noisy or multiple spectrum on the one hand and to achieve a wideband operation on the other. The condition for a multituned circuit such as the one shown in Figure 5-3b to have a clean output spectrum is given by Kurokawa as [3]

$$Q_1 + Q_2 + Q_4 \ldots > Q_1 + Q_3 + \ldots > Q_2 + Q_4 + \ldots \tag{5-6}$$

where the Q's are the Q-factors of the individual resonant circuits.

In microwave circuits (or millimeter wave circuits, for that matter), the determination of Q factors is a very complicated business, since the circuits are made of distributed components and not lumped components. Computer-aided design was employed in order to alleviate the difficulty. The method makes use of a circuit model with parameters which can be identified with those of the actual circuit. A computer program is then used to calculate the circuit properties including the impedance locus. By iterating the various parameters which correspond to actual physical dimensions, a circuit with the proper impedance characteristics can be designed in a relatively short time. The equivalent model was developed by several researchers [7,8] and is shown in Figure 5-5. Based on this model, the various circuit characteristics are defined by:

$$Y' = j \sum_{m=1}^{\infty} \frac{\cos m\pi}{X_m} e^{-mr\pi/b} \tag{5-7}$$

$$Y_{1p} = j \sum_{m=1}^{\infty} \frac{1}{X_m} e^{-m\pi r/b} - j \sum_{m=1}^{\infty} \frac{\cos m\pi}{X_m} e^{-m\pi r/b} = Y_{2p} \tag{5-8}$$

$$Z_{0p} = j \frac{Z_0}{4} \left[k_0^2 - \left(\frac{\pi}{a}\right)^2\right]^{1/2} \sum_{n=2}^{\infty} \frac{\left[\cos \frac{n\pi r}{a} - \cos \frac{n\pi(2d \pm r)}{a}\right]}{\left(\frac{n^2\pi^2}{a^2} - k_0^2\right)^{1/2}} \tag{5-9}$$

$$X_m = \frac{b^2}{4} \frac{n}{k_0 ab} \left(\frac{m^2\pi^2}{b^2} - k_0^2\right) \left(\frac{a}{\pi}\right) \left[K_0 \left(r\Gamma_m\right) - K_0 \left(2d\Gamma_m\right)\right] \tag{5-10}$$

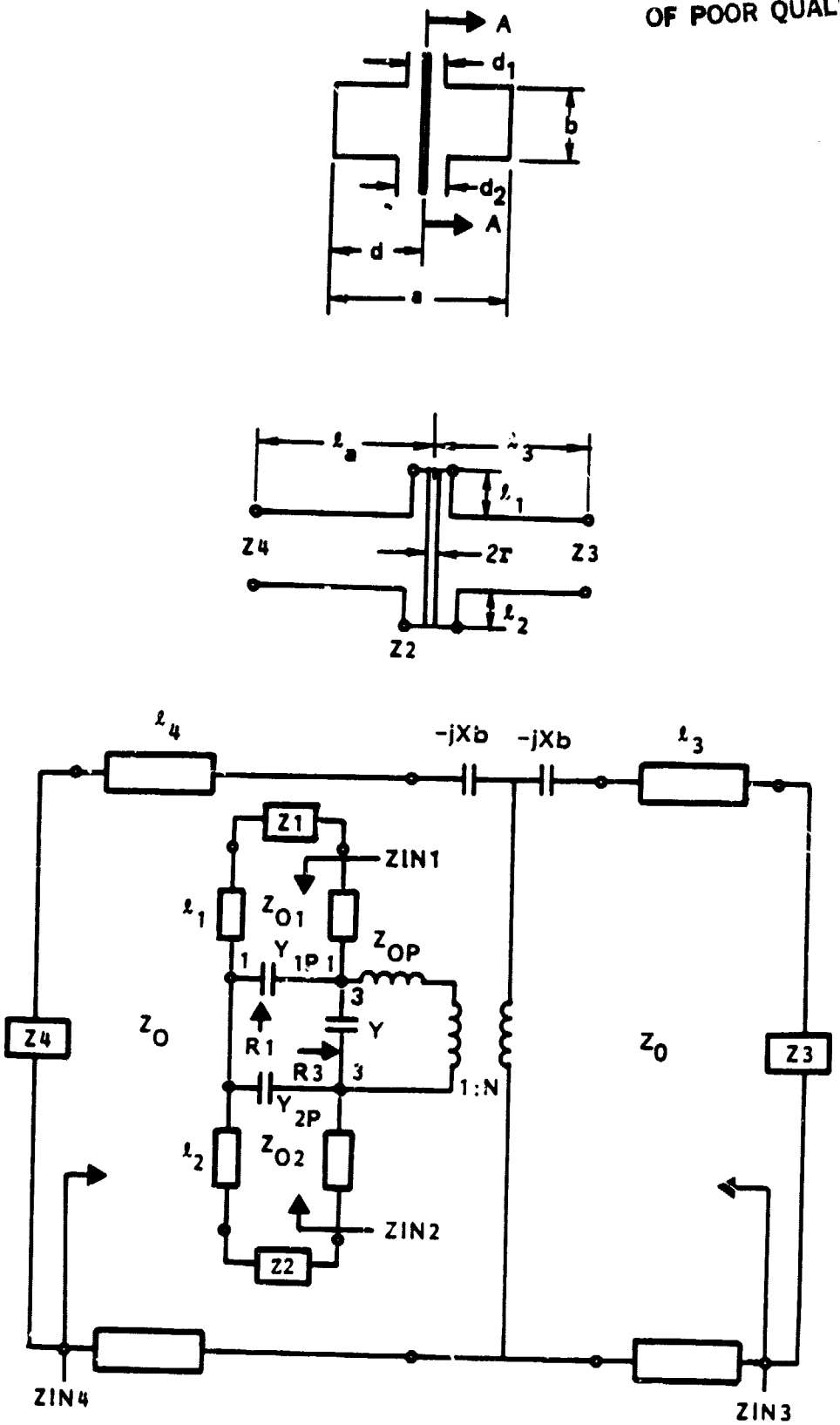


FIGURE 5-5. EQUIVALENT CIRCUIT MODEL OF A COAXIAL-WAVEGUIDE CIRCUIT FOR COMPUTER ANALYSIS

$$X_b = Z_0 \frac{a}{\lambda_g} \left(\frac{2\pi r}{a}\right)^2 \sin^2\left(\frac{\pi d}{a}\right) \tag{5-11}$$

$$N = \sqrt{\csc \frac{\pi d}{a} \csc \frac{\pi(d \pm r)}{a}} \tag{5-12}$$

$$\Gamma_m = \left(\frac{m^2\pi^2}{b^2} - k_0^2\right)^{1/2}$$

where

$$Z_0 = 2\eta \frac{b}{a} \frac{\lambda_g}{\lambda}$$

$$\lambda_g = 2\pi / \sqrt{k_0^2 - \left(\frac{\pi}{a}\right)^2}$$

$$\eta = 120\pi$$

$$k_0 = 2\pi/\lambda$$

K = modified Bessel function of the second kind.

The model was found to have good correlation with measured data. For example, Figures 5-6 and 5-7 show the comparisons between experimental results [9] and the calculated results from the model at X-band frequencies. Figure 5-6 shows the case where the bias port is terminated with a 50-ohm load. Figure 5-7 shows the case where the bias port is short-circuited (RF speaking) 12 mm away from the waveguide. Further confirmation is shown in Figure 5-8 for the driving point impedance at a small gap in the waveguide. The experimental results used in Figure 5-8 are obtained from [10]. The general agreement with the measurement results indicates that the equivalent model is indeed a valid one.

For oscillations to occur, using the IMPATT diode impedance plot shown in Figure 4-4, Section 4, the circuit resistance and reactance must satisfy the following two conditions at the operating frequency band:

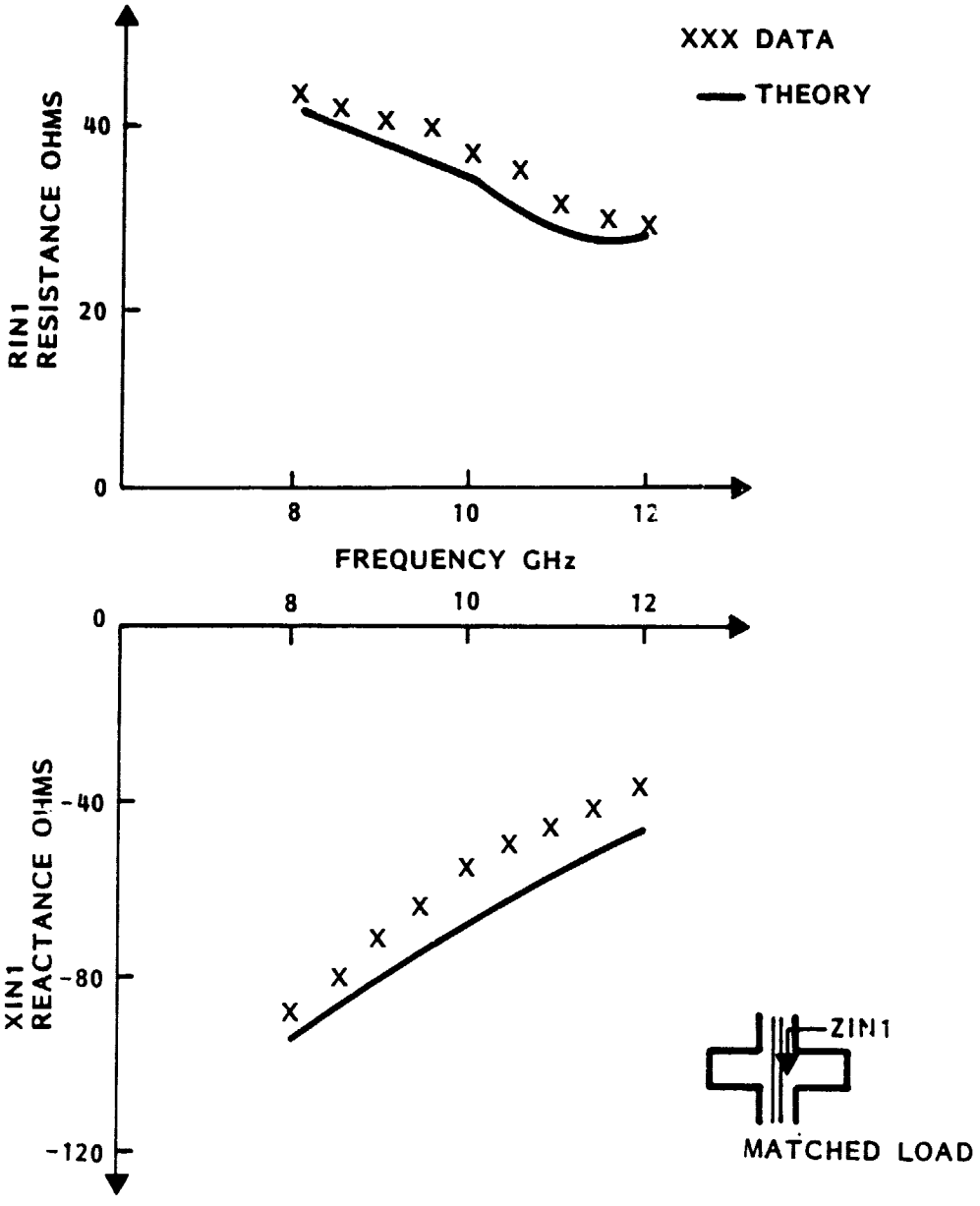


Figure 5-6. Theory and Experimental Comprison for a 50-ohm Load at Coaxial Port

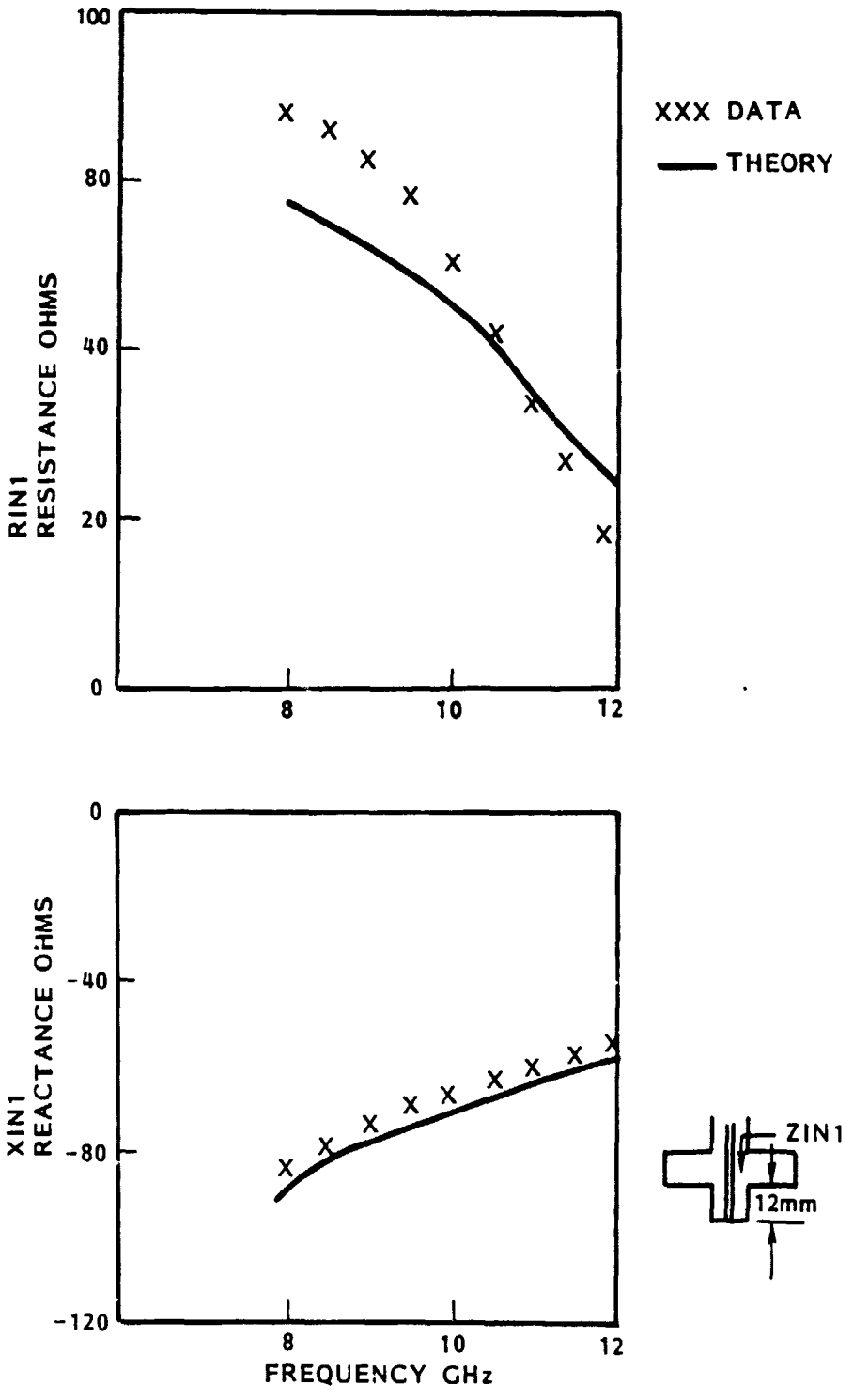


Figure 5-7. Theory and Experimental Comparison for a Short at 12 mm from the Coaxial Entry

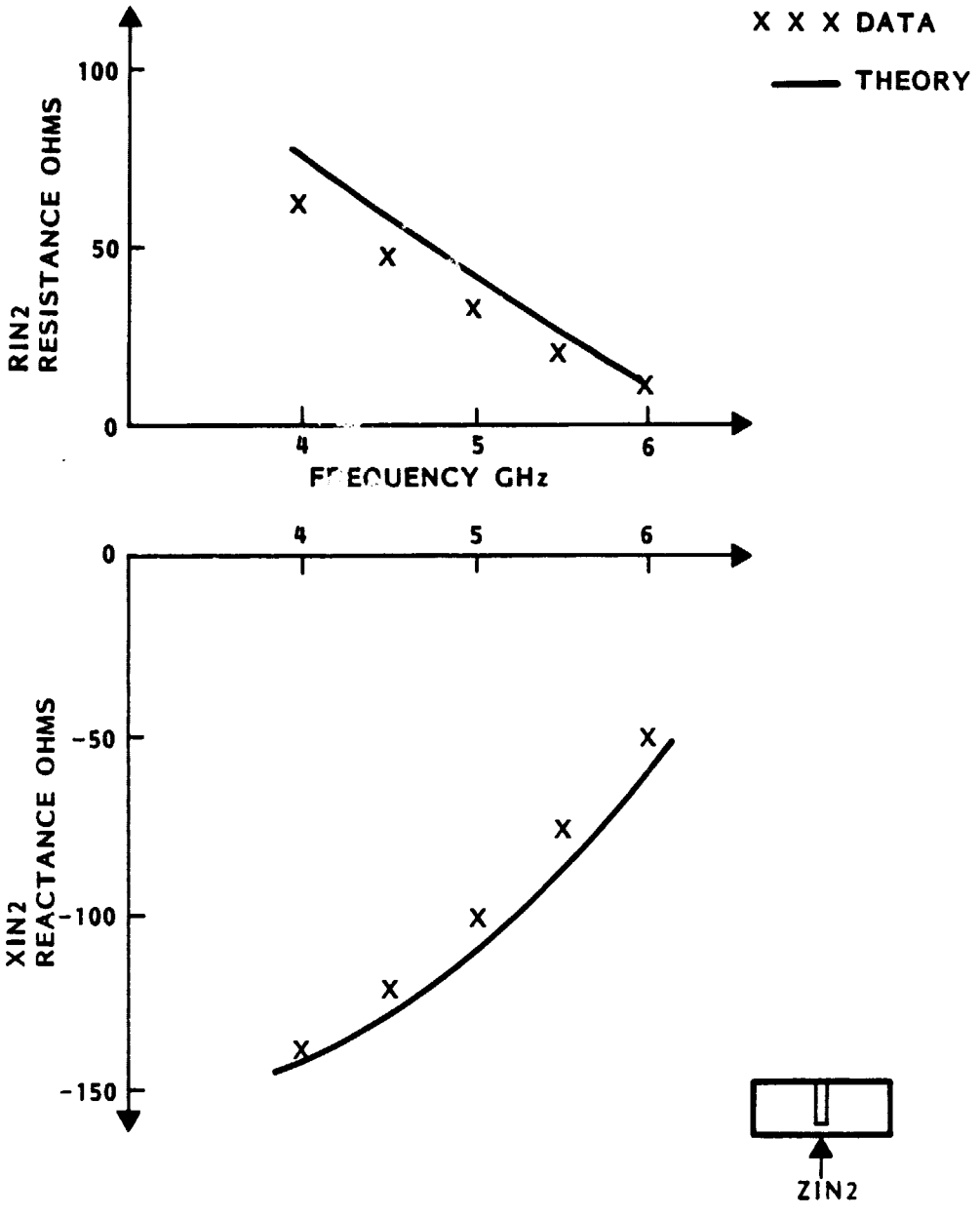


Figure 5-8. Theory and Experimental Comparison for the Driving Point Impedance at the Gap. The Waveguide has a = 1.872", b = .872". The Post is Located at Center with r = .0598" and the Gap is Small.

$$\left| R_{diode} \right| > R_{ckt} \tag{5-13}$$

$$X_{diode} = -X_{ckt} \tag{5-14}$$

A computer program was used to calculate and iterate the various circuit parameters until a suitable impedance characteristic is found. One suitable set of circuit parameters was found to be:

ℓ_1 = .889 mm (.035")	z_1 = 1(matched load)	2r = 1.3 mm (.051")
ℓ_2 = 3.81 mm (.150")	z_2 = 30 ohms	D_1 = 1.4 mm (.055")
ℓ_3 = 25.4 mm (1.0")	z_3 = 1(matched load)	D_2 = 1.33 mm (.523")
ℓ_4 = 5.08 mm (.020")	z_4 = 0 ohms	a = 10.66 mm (.420")
		b = .762 mm (.032")

The corresponding circuit resistance R_{ckt} and reactance X_{ckt} as a function of frequency are plotted in Figure 5-9. Also plotted in the same figure are the diode resistance R_d and reactance X_d from Figure 4-4, Section 4. It is easily seen that both the conditions of Eqs. (5-13) and (5-14) are satisfied. The intersection of X_{ckt} and X_d indicates the oscillation frequency of about 19 GHz. Furthermore, R_{ckt} and X_{ckt} are plotted against each other (the impedance locus plot) as shown in Figure 5-10. It can be seen that the impedance locus is free from loops and sharp peaks, thereby providing a clean single-frequency oscillation.

The final configuration of the single-diode circuit is shown in Figure 5-11 in both construction form and equivalent circuit form. The circuit is a rather conventional waveguide oscillator circuit. By making the circuit parasitics minimum, such as the case of the present construction, the circuit can be shown to be triple-tuned. The three resonators are identified in the equivalent circuit, namely, the quarter-wave transformer, the quarter-wave waveguide short and the quarter-wave choke.

The operation of the circuit is as follows. The IMPATT diode requires a loading resistance of a few ohms. A full-height waveguide, on the other hand, offers an impedance of some 400 ohms. A reduced-height waveguide is therefore used to ease the problem of impedance matching. A two-step transformer is used to match the reduced-height waveguide to the standard full-height waveguide at the output. Since the two-step transformer has a wider bandwidth

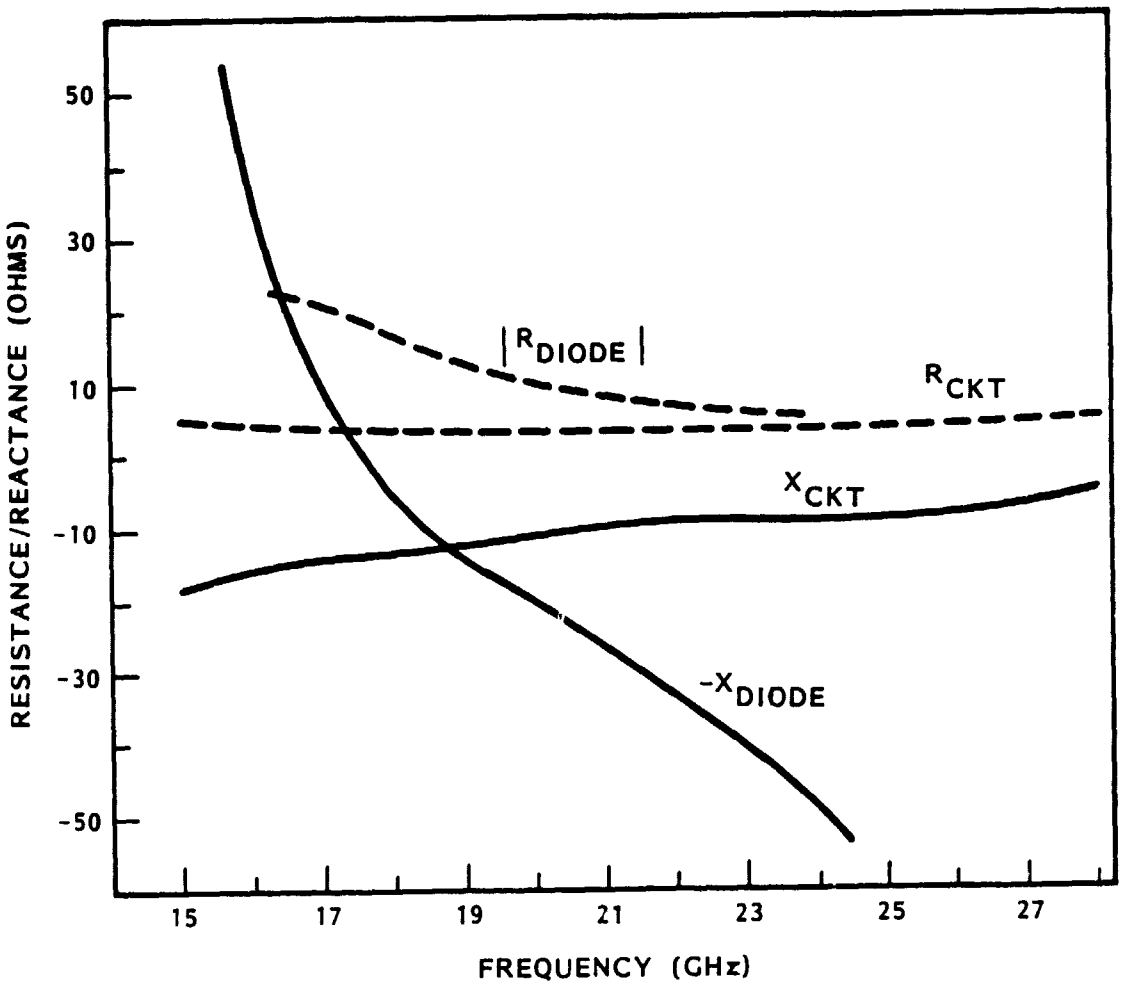


Figure 5-9. R-X Plots of Computer Model

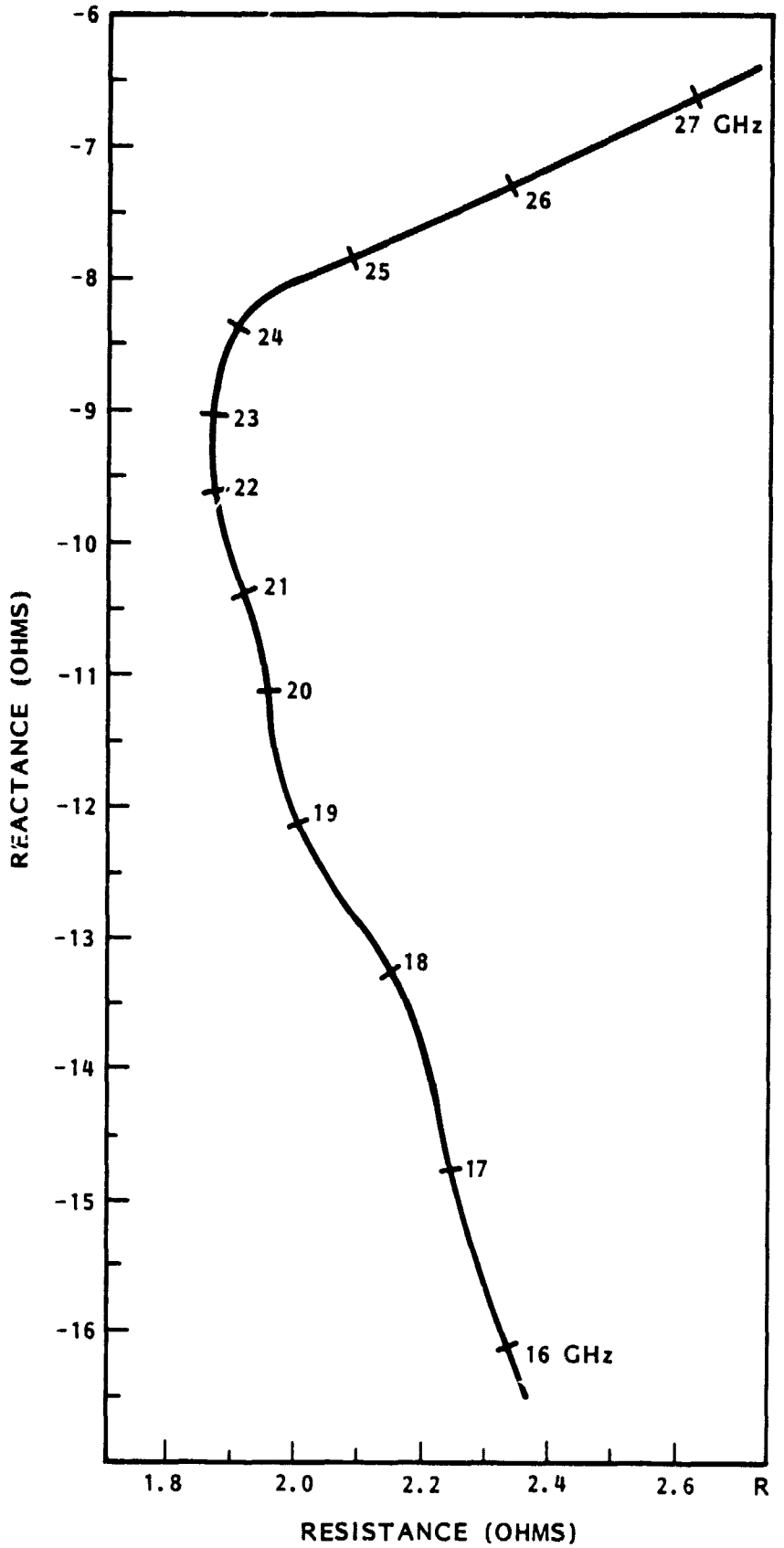
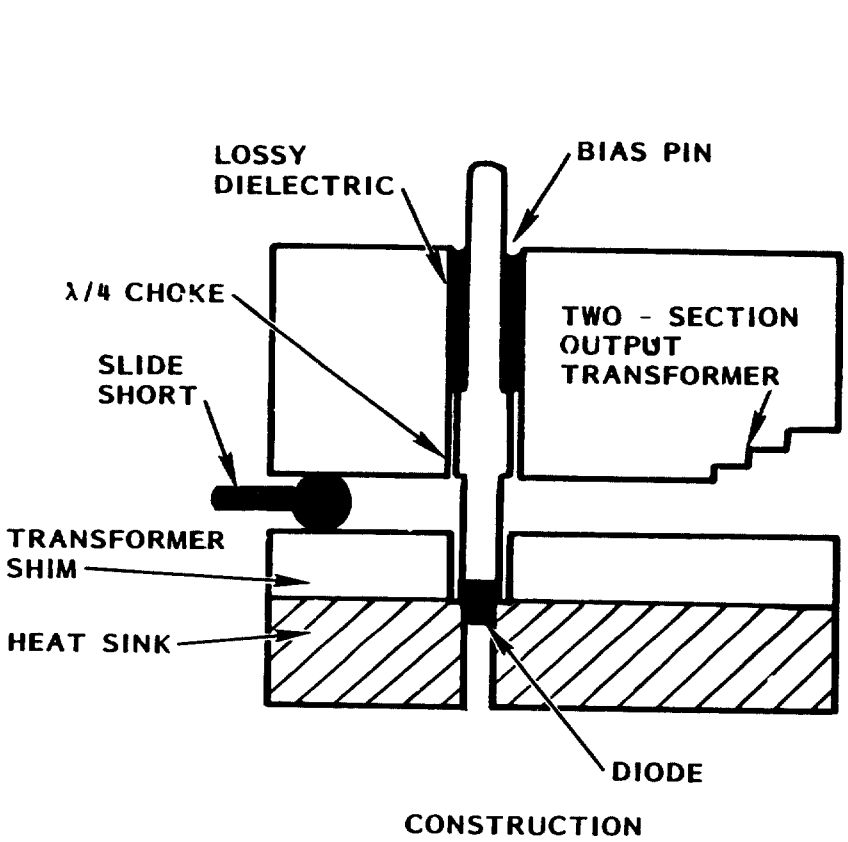


Figure 5-10. Impedance Locus of Computer Model



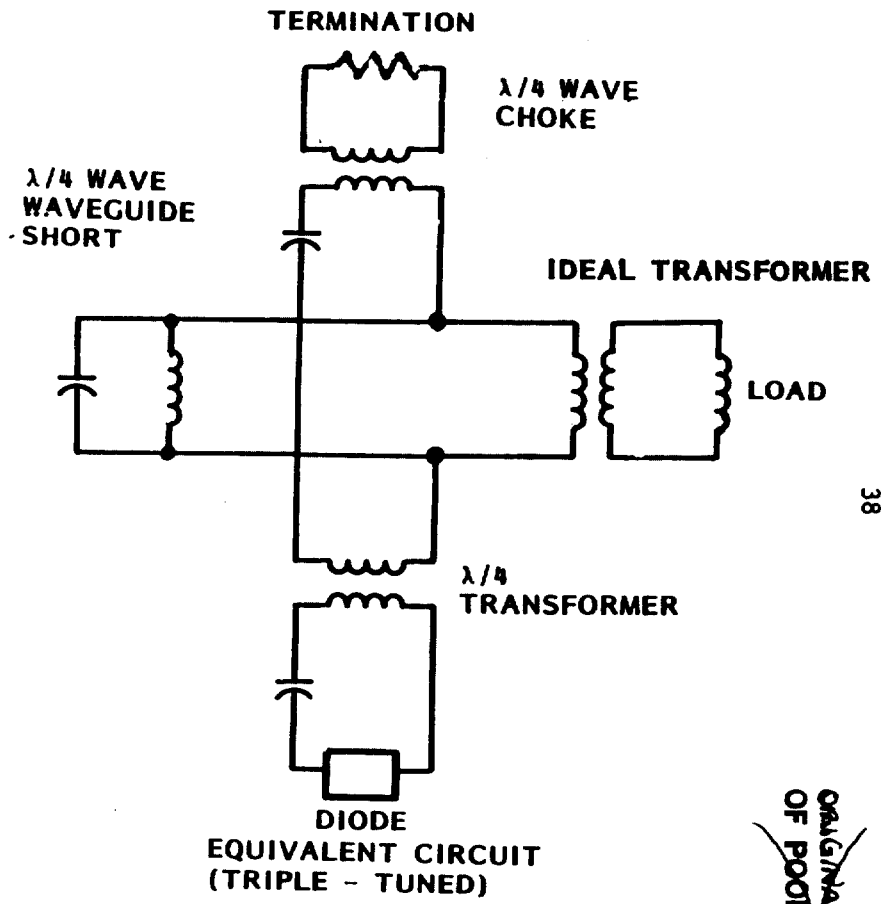


Figure 5-11. Single-Diode Multi-Tuned Oscillator Circuit

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than the operating frequencies, it can be considered as a nonresonant ideal transformer. A single-section quarter-wave transformer, consisting of the bias pin and the transformer shim, is used to match the reduced-height waveguide to the diode. The quarter-wave transformer has the special property that it not only transforms impedances but is also frequency-selective. It acts as a shunt resonator if seen from the high impedance side (from the reduced-height waveguide) and as a series resonator if seen from the low impedance side (from the IMPATT diode). This property is depicted in the equivalent circuit in Figure 5-11. A waveguide short circuit is placed a quarter-wave away from the bias pin in the reduced-height waveguide. The short circuit appears to the diode as an open circuit at the quarter-wave frequency and therefore has the property of a shunt resonator. RF power generated from the diode is shared between the load and the bias termination (formed by the lossy dielectric). A third resonator, the choke, is added to the bias port. The choke is merely a quarter-wave transformer which transforms the relatively low imepdance of the bias termination to an even lower value, thereby allowing most of the RF power to go to the load.

A photograph of the single-diode circuit is presented in Figure 5-12. The RF performance of this circuit is presented in Section 7.6.

5.2 OUTPUT STAGE

Due to the high output power requirement, the output stage is,of necessity, a multidiode circuit. Nonlinear interactions among the diodes impose restrictions on circuit performance. Consequently, the output stage is always the limiting member in the amplifier chain in terms of output power and operating bandwidth. There are two possible approaches to meet the power and operating bandwidth. One is to develop an IMPATT amplifier operating in the stable amplifier mode; the other is to develop an IMPATT amplifier operating in the injection-locked oscillator mode.

Although the stable amplifier mode has the potential of wide operating bandwidth, the circuit requires the use of 3-dB hybrid couplers to achieve power combining. This scheme has the following disadvantages: (a) Because of hybrid losses, the coupler is only capable of combining up to four diodes.

Figure 5-12. Single-Diode Oscillator Hardware

This mandates the use of 6-W IMPATT diodes, which are nonexistent at the present time; (b) stable amplifiers generally have lower gain than injection-locked amplifier (3 dB vs. 10 dB), consequently it is estimated that six amplifier stages would be required in the stable amplifier mode to achieve the 30-dB gain; (c) hybrid-coupled amplifiers are, in general, more bulky than injection-locked oscillators. The larger number of stages also increases the overall size.

In contrast to the stable amplifier mode, the injection-locked oscillator mode offers the following advantages: 12 or more diodes can be combined in a very small volume; due to the high gain of each stage, only three stages are required to achieve the 30-dB gain required in the program. In an injection-locked oscillator circuit, a resonant cavity is used as the medium for power combining. There are basically two configurations of resonant cavities which are suitable for 20 GHz circuits, the cylindrical cavity and the rectangular waveguide cavity. The cylindrical configuration has enjoyed great success at lower frequencies due to its compact size. At 20 GHz, however, the diameter of the cavity is some 1.5 cm (0.45"), making it too small to accommodate the required number of IMPATT diodes. A larger diameter cylindrical cavity is not recommended because of the problem of overmoding; the number of resonant modes within a specific frequency range varies with the square of the cylinder radius. The waveguide cavity, on the other hand, can accommodate a large number of diodes by increasing only the longitudinal dimension of the cavity. This results in a linear increase in the number of resonant modes rather than a quadrate increase as in the case of the cylindrical cavity. Consequently, mode spacing is large and single mode operation is possible. One added advantage with the waveguide cavity is the direct interface with the output waveguide, since the cross-sectional dimensions of the cavity are identical to those of the waveguide. Based on these considerations, the waveguide cavity configuration was adopted for the output stage.

The basic construction of a rectangular waveguide combiner is shown in Figure 5-13. It essentially consists of a number of individual diode modules coupled to a rectangular waveguide through the sidewalls of the guide. The resonant cavity is formed by a short circuit on one end and an iris opening on the other end. The diode module is very similar to those of the input and driver stages. Figure 5-14a shows the construction of the diode module. It differs from the single-diode circuit in three respects.

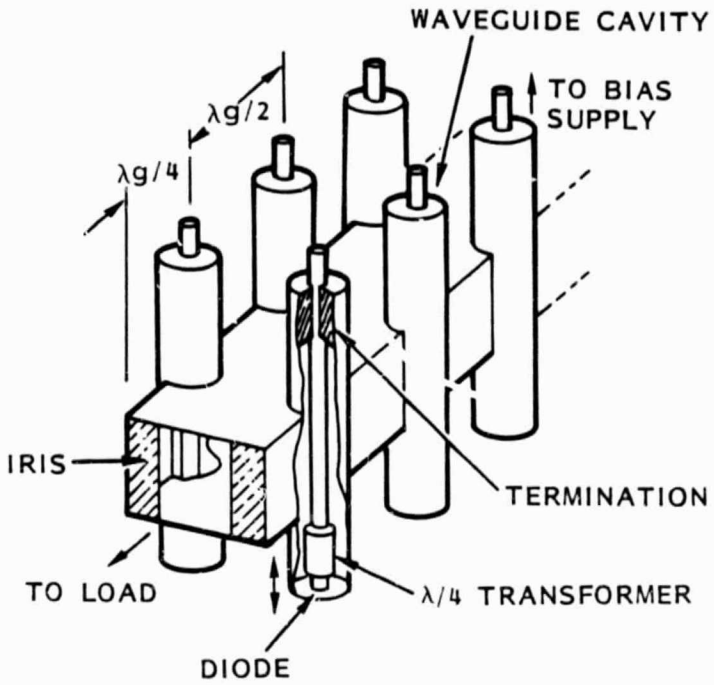

Figure 5-13. Basic Configuration of Waveguide Cavity Combiner

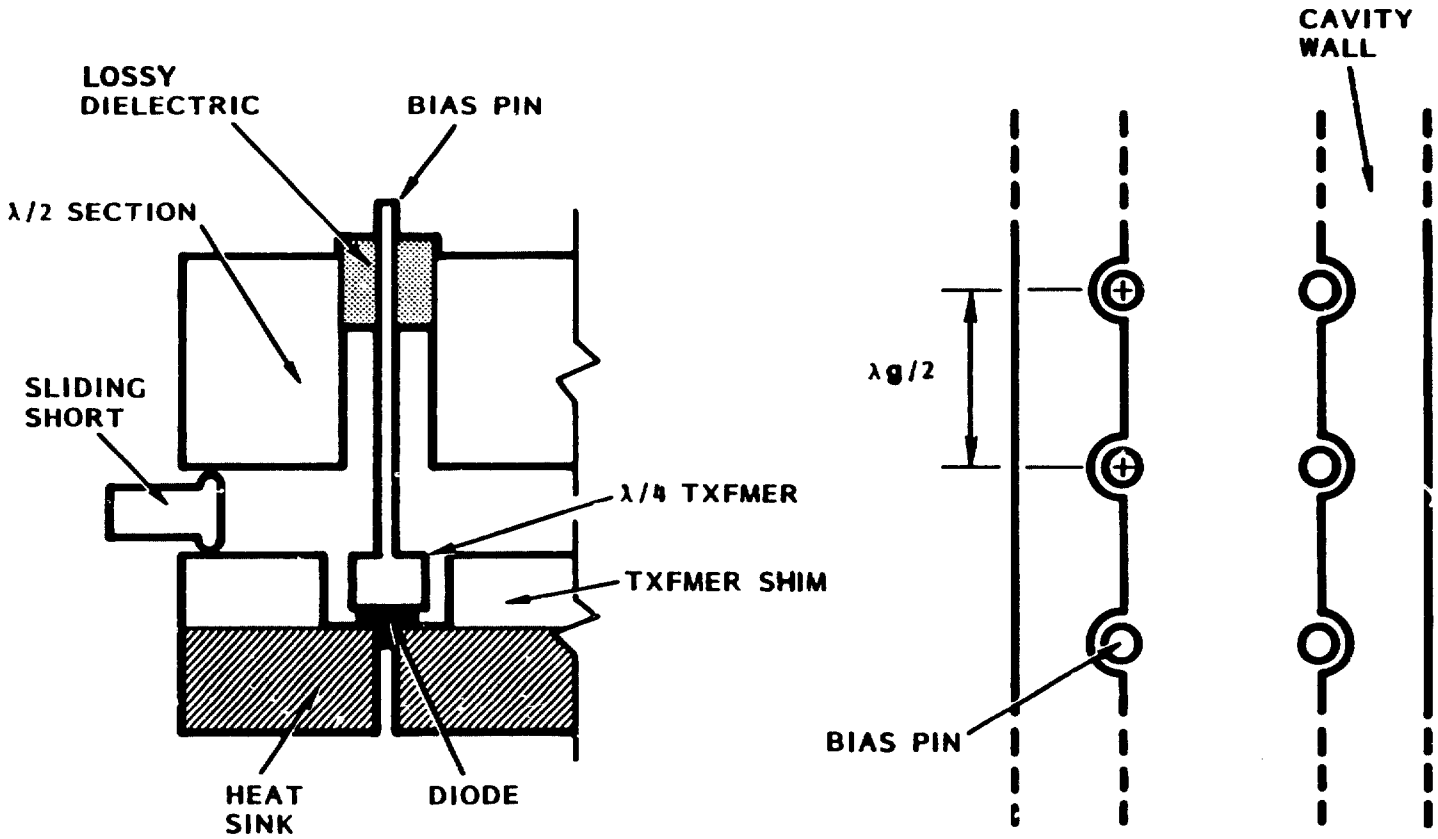

Figure 5-14. Construction of Waveguide Cavity Combiner

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First, the quarter-wave transformer has a step inner conductor; that is, the bias pin is enlarged in the quarter-wave section. This configuration was found necessary experimentally. With a straight bias pin, the gap between the pin and the transformer shim would have been too small to be mechanically practical.

Second, there is no quarter-wave choke in the bias port. Instead, a half-wave section (with air as the dielectric) is used before the bias port is terminated by lossy dielectric (Eccosorb MF124). This arrangement has the merit that at the resonant frequency, the half-wave section behaves as a series resonator and is essentially a short circuit. The diode sees the load and the bias termination in series. Since the bias termination is designed to have a relatively low impedance, most of the RF power is delivered to the load. At spurious frequencies, including subharmonics, the half-wave section exhibits a high impedance, making the oscillation condition for the diode unfavorable. Spurious oscillators and other instabilities are thereby avoided or minimized.

Third, the diode modules are coupled to the waveguide from the sidewalls instead of from the center of the guide. (See Figure 5-10b.) This configuration has the advantage that two diode modules can be placed at the same cross section, thereby cutting the length of the cavity in half.

The actual construction of the 12-diode combiner used on the output stage is shown in Figure 5-15. The individual components are readily identifiable and need no further elaboration. An assembly view of the combiner can be found in Figure 5-16. The measurement data of the unit are presented in Section 7.6.

One design feature of the combiner, which is visible from Figure 5-16, is the bias pin assemblies. The contacts between the IMPATT diodes and the bias pins are very important. Large current, DC and RF, flows through each contact since it is within the low impedance region. Contacts with low ohmic loss are essential for the power performance of the combiner. To maintain a low loss contact, the bias pin must be pressed against the diode package by a large force. A so-called balanced-bridge mechanical configuration was used in the design of the bias pin assembly shown in Figure 5-17. A nonconducting bridge (made of epoxy glass) is seated on the ends of two bias pins. The bridge is

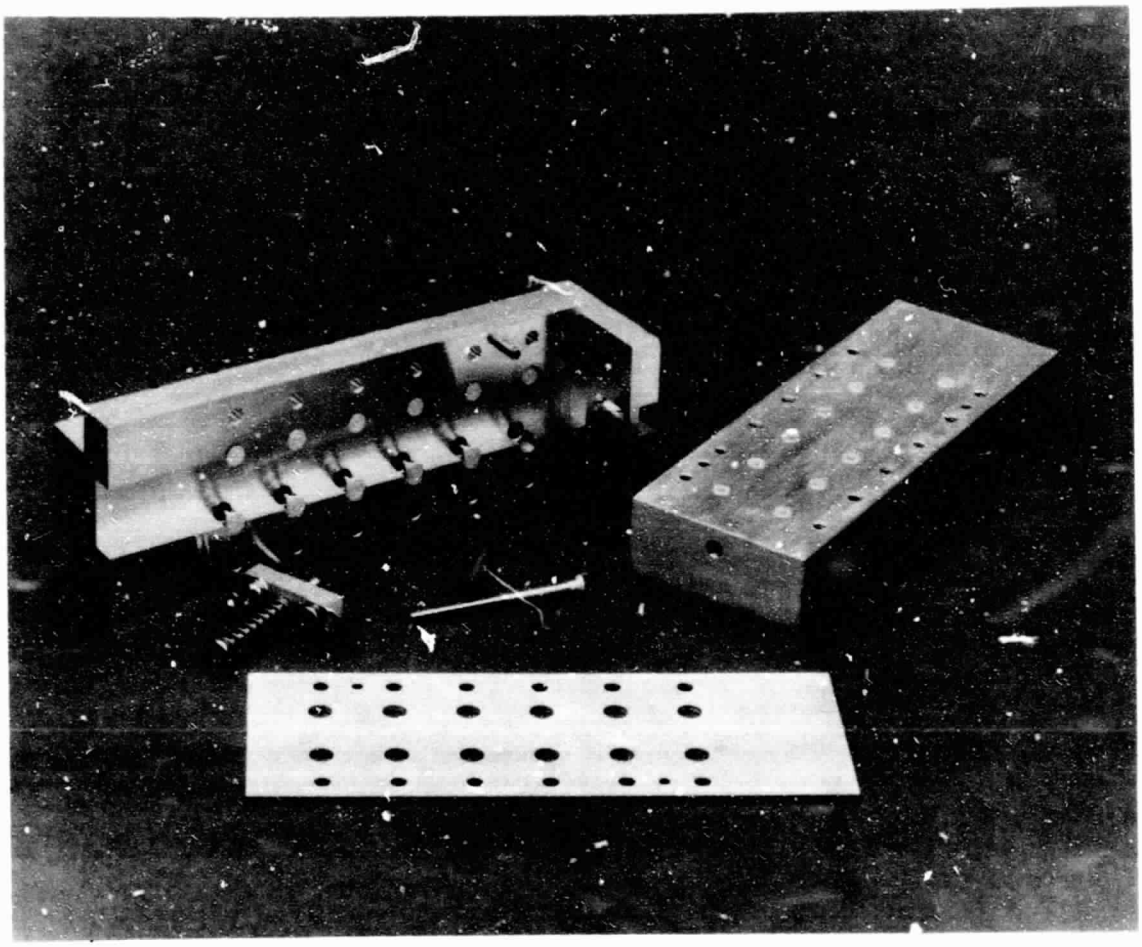


Figure 5-15. Construction of 12-Diode Combiner

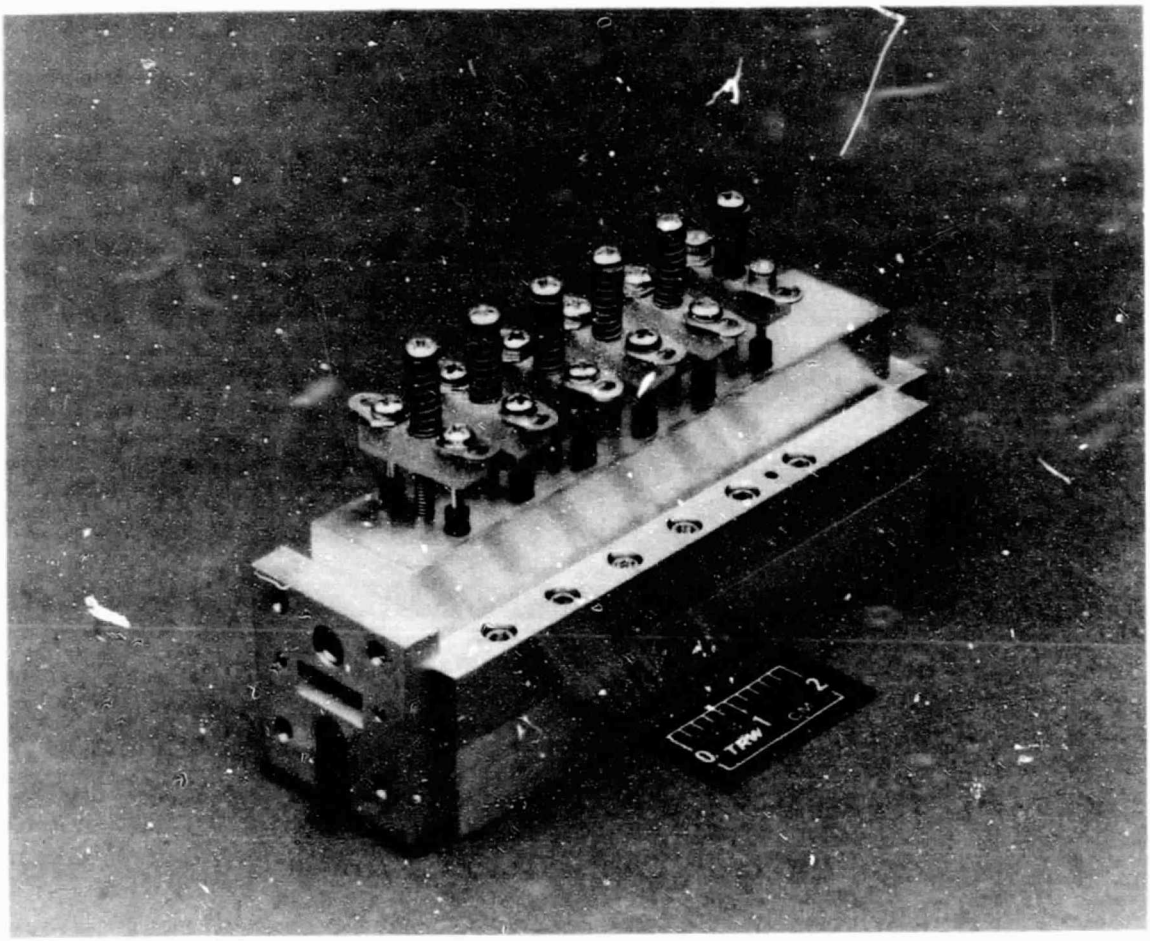


Figure 5-16. Assembled View of 12-Diode Combiner

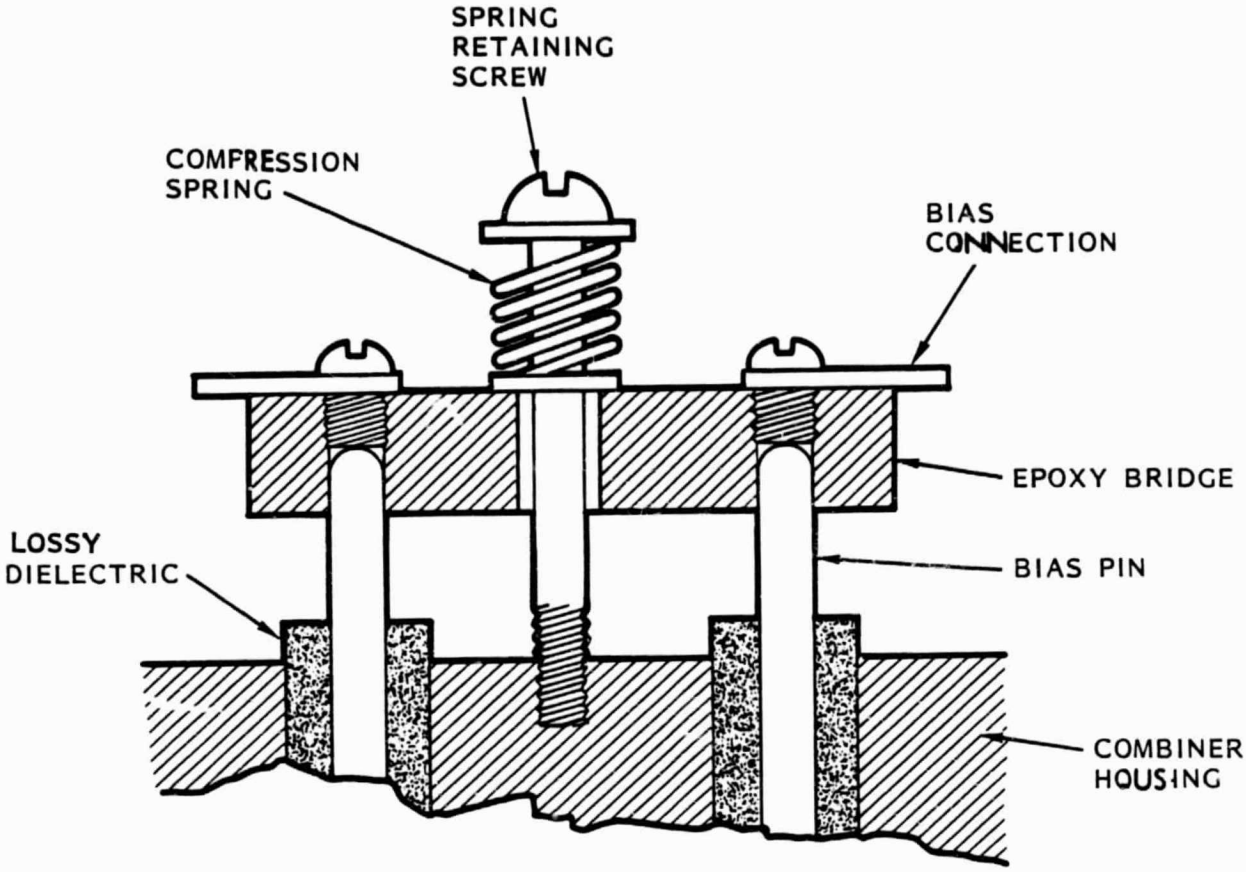


Figure 5-17. Construction of Bias Pin Assembly

being pressed onto the bias pins by a spring situated at the center of the bridge, as shown in the figure. The pressure of the spring is transmitted to the bias pins. By using a suitable spring and with the proper spring compression, precise pressure can be maintained between the diode-bias pin contact.

The equivalent circuit of the output stage is shown in Figure 5-18. With the numerous resonators identified in the figure, the output stage can be classified as a multituned circuit. In actual operations, however, the combiner behaves as a single-tuned circuit. The reason being that, in comparison, the Q of the resonant cavity is so much higher than those of the other resonators that the effects of the latter are all but diminished. This statement was confirmed by experiment that the free-running frequency of the combiner was varied by the adjustment of the waveguide short and the iris (two elements of the waveguide cavity) and, to a large extent, not varied by the alternation of the transformer shim or the half-wave sections. Consequently, the output stage suffers from relatively narrow operating bandwidth as with other single-tuned circuits. Initially, it was believed that by lowering the cavity Q to 25 and the stage gain to 8, the program objectives of a 20-W CW output and a 2-dB bandwidth of 500 MHz can be achieved. During the course of the development, it was found that the wide dispersion of characteristics in terms of output power and free-running oscillation frequency of the IMPATT diodes used is severely limiting the power-bandwidth performance of the output stage. The mechanism behind this limitation process is shown in Appendix C. A high Q resonant circuit was needed to compensate for the variations in diode impedances (due to package and diode chip variations) in order to achieve power combining. Since the Q of the circuit could not be increased without affecting the bandwidth, a compromise was made and both output power and bandwidth suffered.

The test results presented in Section 7.6 show that the output stage falls short of the design objectives by providing an output of some 16 W CW and a 2-dB bandwidth of 117 MHz. It is believed that the power objective of 20 W can be met by the present design. One way is to increase the number of commercial Varian diodes used in the output stage from 12 to 16. The other approach is to refit the output stage with the higher power diodes. Both of

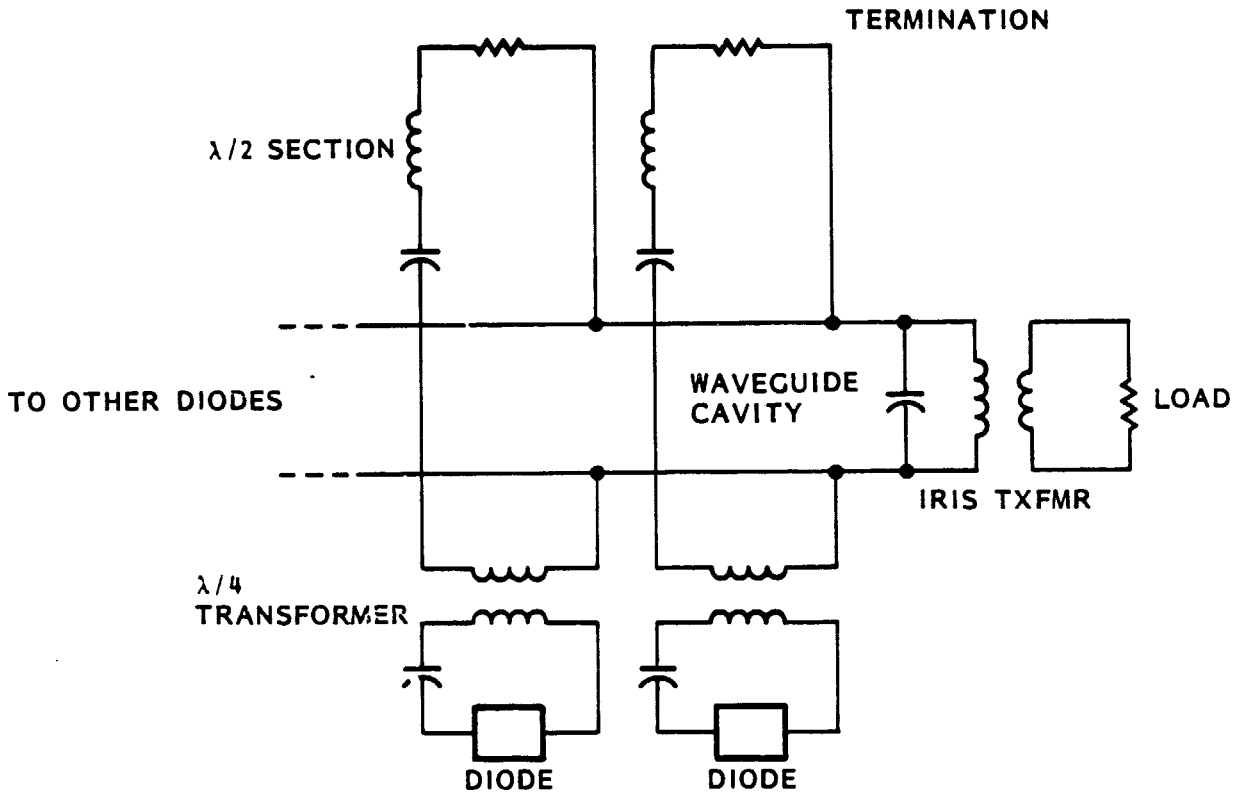


Figure 5-18. Equivalent Circuit of Waveguide Cavity Combiner

these approaches, however, cannot alleviate the bandwidth problem. To solve both power and bandwidth problems, it is believed that still higher power (yet to be developed, 4.5 W per diode) IMPATT diodes should be used.

With the higher power devices, fewer diodes are needed to provide a 20-W output. For example, if 4- to 6-W diodes were used, it would be necessary to combine only four devices at the output stage to satisfy the power requirement. With four devices, not only the problem of diode matching is eased, it is possible also to fine-tune each diode module such that the collective results (i.e., four diodes as a whole) are optimal. It should be noted that the tuning of one diode module in a combiner circuit affects the tuning of all remaining diodes in the same circuit. Consequently, optimization of a circuit which combines a large number of active devices (12 diodes in our case) was proven to be a formidable task. It is expected that a rectangular waveguide cavity combiner using four high power (4 to 6 W) IMPATT diodes is capable of meeting the program objectives.

5.3 CIRCULATORS

One essential component found in most injection-locking oscillators or reflection amplifiers employing IMPATT diodes is the three-port circulator. The circulator decouples the input circuit from the output circuit and, in effect, transforms a one-port network into one with two ports. Since both the input and output signals are transmitted through the circulator, the electrical characteristics of the circulator have a profound influence on the overall circuit performance. The requirements imposed on the circulators are stringent. The circulators must be capable of handling the signal power and have a wide bandwidth (with low SWR) for proper circuit operations and an adequate isolation for input/output decoupling. Moreover, the circulators must have an extremely low insertion loss - in the vinicity of 0.1 dB - so as not to further degrade the relatively poor efficiency of IMPATT devices. TRW has developed and patented such high performance circulators [11].

The development of high performance circulators was initiated at TRW in 1974. A market search had disclosed that even on special order, state-of-the-art circulators were totally inadequate for our purposes and an R&D effort was

initiated to develop a low loss circulator at Ka-band. What appeared at that time as a technically ambitious task resulted not only in a device with performance characteristics far exceeding the original goals, but also led to several significant advances in ferrite component technology. Among these were improvements in analytical design methods and a better understanding of ferrite material applications, resulting in a high degree of control over performance parameters, such as insertion loss, power capacity, and thermal stability. The improvements in structural design resulted in much higher reliability components which totally outperformed, under shock and vibration, the epoxy-bonded, triangular junction designs common to the industry.

Figure 5-19 depicts the simplified construction of a three-port junction circulator. The circulator consists of three TE_{10} rectangular waveguides which are 120° apart and intercept to form a symmetric junction. A ferrite post is placed at the center of the junction. An external status magnetic field H_a is required to bias the ferrite post. Commercially available circulators employ ferrite posts with a triangular cross-section as shown in Figure 5-20a. The triangular geometry was considered to have the potential of offering a wide circulator bandwidth. However, due to fabrication and mechanical alignment difficulties, the wideband potential was never practically realized. In fact, each triangular geometry circulator has to be individually tuned to meet the electrical requirements. TRW, on the other hand, adopted the cylindrical ferrite post as shown in Figure 5-20b. It was found that the cylindrical geometry offers not only superior mechanical properties, but also electrical performance that equals or surpasses that of the triangular geometry. Individual tuning of the TRW circulator is not needed once the proper junction design is completed.

A detailed graphic representation of the TRW circulator junction is depicted in Figure 5-21. The junction consists of two ferrite discs, two dielectric spacers, a septum in the center of the cylinder dividing the junction into two turnstiles, and a dielectric tube enclosing the above parts.

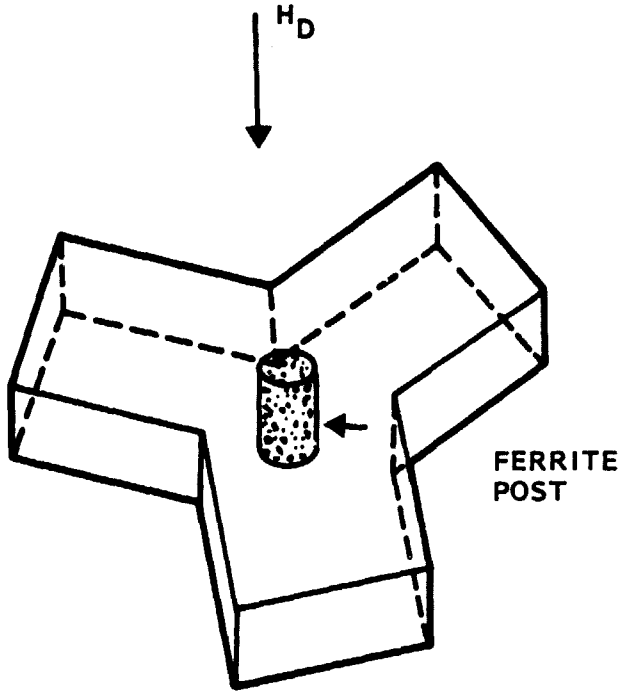
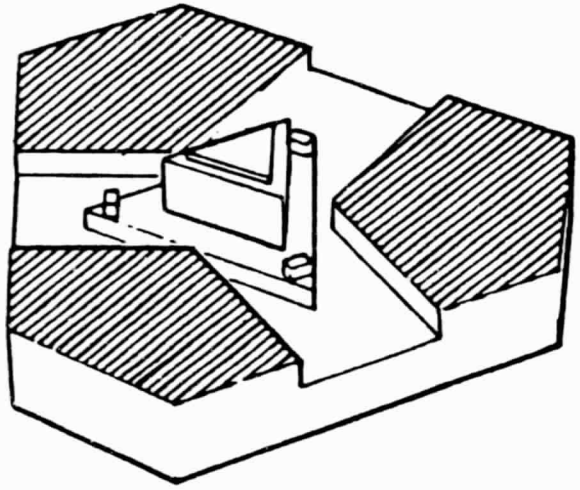
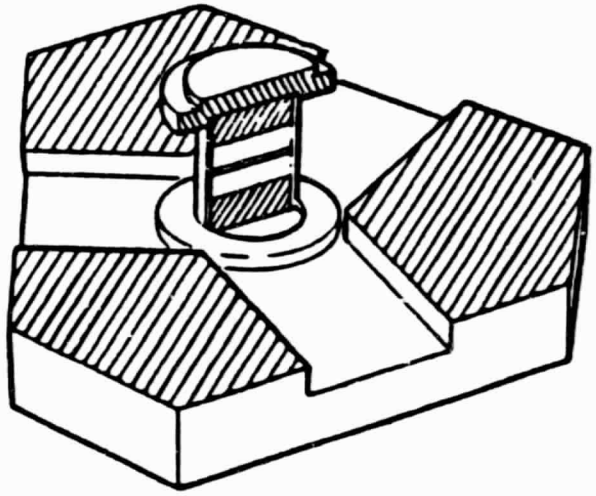


Figure 5-19. Simplified Construction of a 3-Port Circulator



a) TRIANGULAR GEOMETRY

- PARTS DIFFICULT TO FABRICATE AND INSPECT
- ASSEMBLY REQUIRES LOCATING FIXTURES, QUALITY CONTROL OF SIX EPOXIED INTERFACES, CURING OVEN
- ASSEMBLED CIRCULATOR REQUIRES POST-ASSEMBLY TUNING - NO TWO CIRULATORS ALIKE
- DIFFICULT TO QUALIFY UNDER SHOCK AND VIBRATION
- EXPENSIVE LOW RELIABILITY CIRCULATOR



b) CYCLINDRICAL GEOMETRY

- PARTS EASY TO FABRICATE AND INSPECT
- SIMPLE ASSEMBLY
- NO POST-ASSEMBLY TUNING, REPRODUCIBLE AND REPEATABLE
- CIRCULATOR SHOCK AND VIBRATION PROOF
- SIGNIFICANTLY LESS EXPENSIVE, HIGH RELIABILITY CIRCULATOR

Figure 5-20. Comparison of Conventional Triangular and TRW's Cylindrical Circulator Junctions

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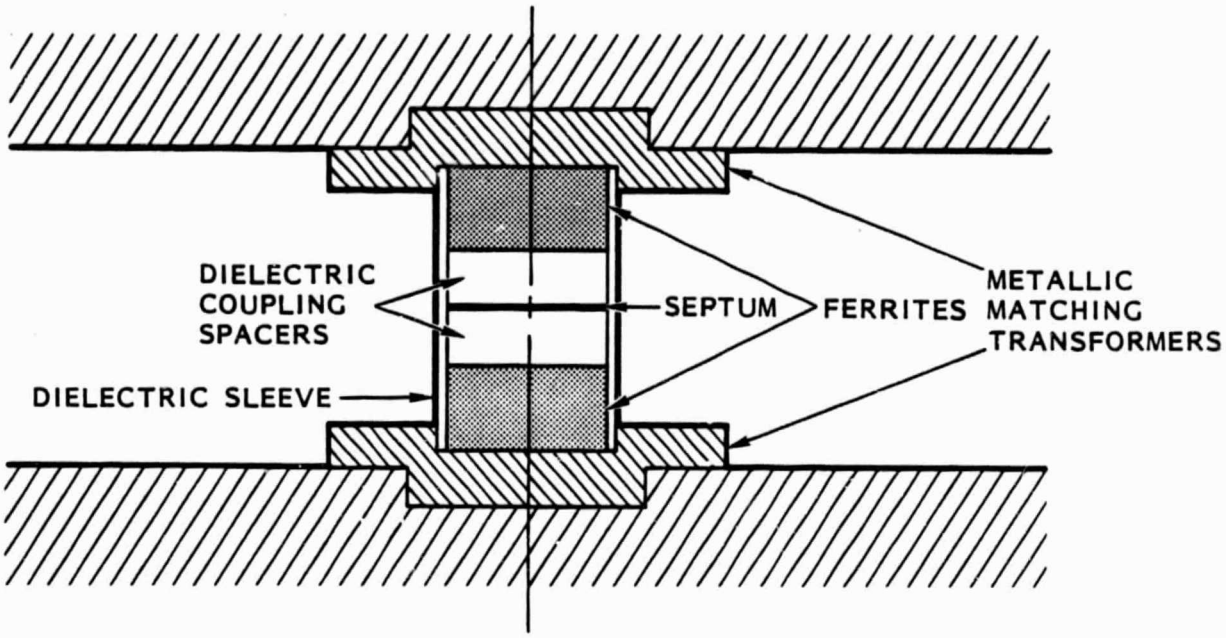


Figure 5-21. Graphic Representation of TRW's Circulator Junction

This junction assembly is nested in metallic transformer discs, which are indexed precisely in the circulator housing formed by three intersecting waveguides. The operation of a junction circulator is best explained with the aid of Figures 5-22a and b. Notice that the symmetric junction formed by the waveguides behaves as a TM_{110} mode cylindrical cavity. When the external magnetic bias H_a is removed and the cavity is excited by the TE_{10} wave from one waveguide, the resulting TM_{110} field pattern is oriented in the direction shown in Figure 5-22a. The pattern orientation is identical to the one when no ferrite post is present. The reason that the ferrite post does not change the pattern orientation is as follows. In the absence of an external magnetic bias, the electromagnetic left- and right-polarized waves existing inside the ferrite have the same propagation constant. The two waves emerge from the ferrite in-phase and no rotation of the cavity field pattern takes place. As shown in Figure 5-22a, the presence of electric and tangential magnetic fields at the waveguide-cavity interface allows the excitation of TE_{10} waves in the two output waveguides.

When the external magnetic bias, H_a, is applied the situation is changed. The two polarized waves in the ferrite no longer have the same propagation constant, resulting in rotation of the mode pattern of the cavity by 30°, as shown in Figure 5-22b. The final outcome is that while one of the output waveguides stays unchanged, the remaining waveguide is isolated (i.e., no output). The cavity field pattern has become such that there are no electrical and tangential magnetic fields at the waveguide-cavity interface to excite the TE_{10} wave in the isolated waveguide.

The bandwidth of a cylindrical circulator is related to its geometry by [12]

$$BW \simeq 3.08\left(\frac{R}{a}\right)^2 \frac{M_s}{1 - \frac{\gamma^2}{\omega_0^2}\left(H_o + \frac{M_s}{2}\right)^2} \qquad (5\text{-}15)$$

where R = radius of ferrite post,

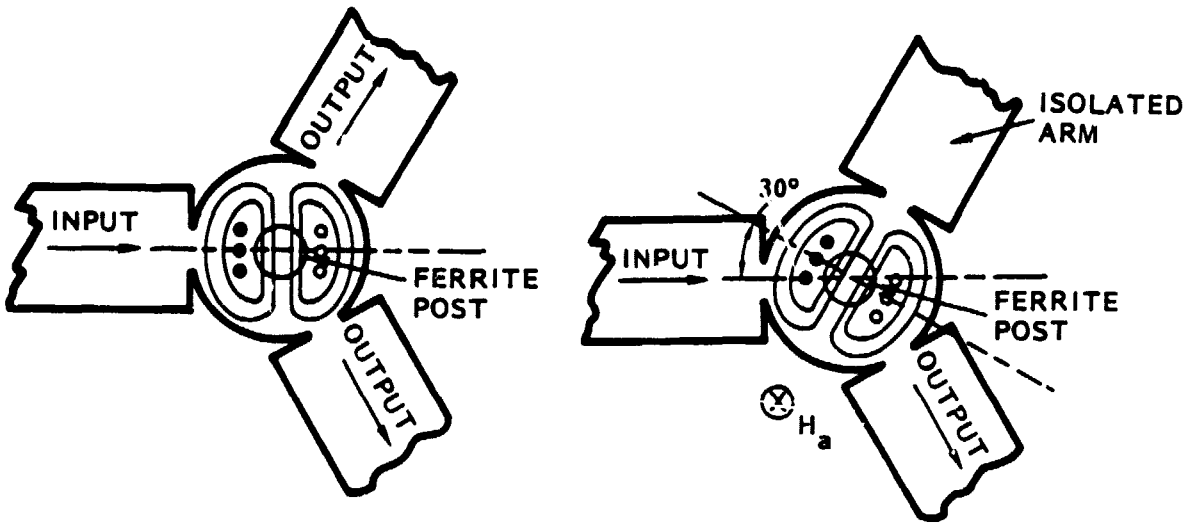
a = radius of cavity,

γ = gyromagnetic ratio of the electron,

ω_0 = center frequency of the passband,

H_0 = external magnetic bias field,

M_s = ferrite saturation magnetization.



a) WITH NO MAGNETIC BIAS

b) WITH MAGNETIC BIAS H_a

Figure 5-22. Field Pattern for H-Plane Waveguide Circulator Using TM_{110} Mode

The upper limit on the circulator bandwidth is, of course, the single-mode bandwidth of the waveguides used.

Figure 5-23 indicates the electrical performance of a K-band TRW circulator. The upper curve represents the VSWR data and the lower curve the insertion loss data. It can be seen that for a VSWR of 1.2, the circulator has a passband from 18 to 23 GHz - a bandwidth of 5 GHz. The insertion loss in the passband is less than 0.2 dB. Tests have shown that the circulator also has an excellent thermal stability; a temperature variation from -21°C to 51°C has little effect on the electrical performance. Figure 5 24 shows the circulator assembly used in the program. The assembly consisted of three circulators in a common housing.

5.4 BIAS REGULATORS

The bias circuit to be used in this program is essentially that of a voltage regulator (constant voltage source). One voltage regulator is needed for each IMPATT diode. Due to their numerous applications, voltage regulators of various capacity and capability have been produced by the industry in IC (integrated circuit) form. These ICs are available in large quantity at low cost.

One regulator suitable for our application in the program is the LM150K, manufactured by the National Semiconductor Corporation. This regulator offers internal current limit, thermal overload protection and safe-area protection to ensure high reliability. The internal circuitry of the regulator is provided in Figure 5-25. The circuit is quite complete. Only three external components, namely a potentiometer, a resistor and a capacitor, are needed to connect the regulator as an adjustable constant voltage source (see, also, Figure 5-25). The IC can operate in a temperature range of -55°C to +150°C. Line regulation is typically 0.005%; load regulation is typically 0.1%. The photograph of a complete regulator assembly is shown in Figure 5-26.

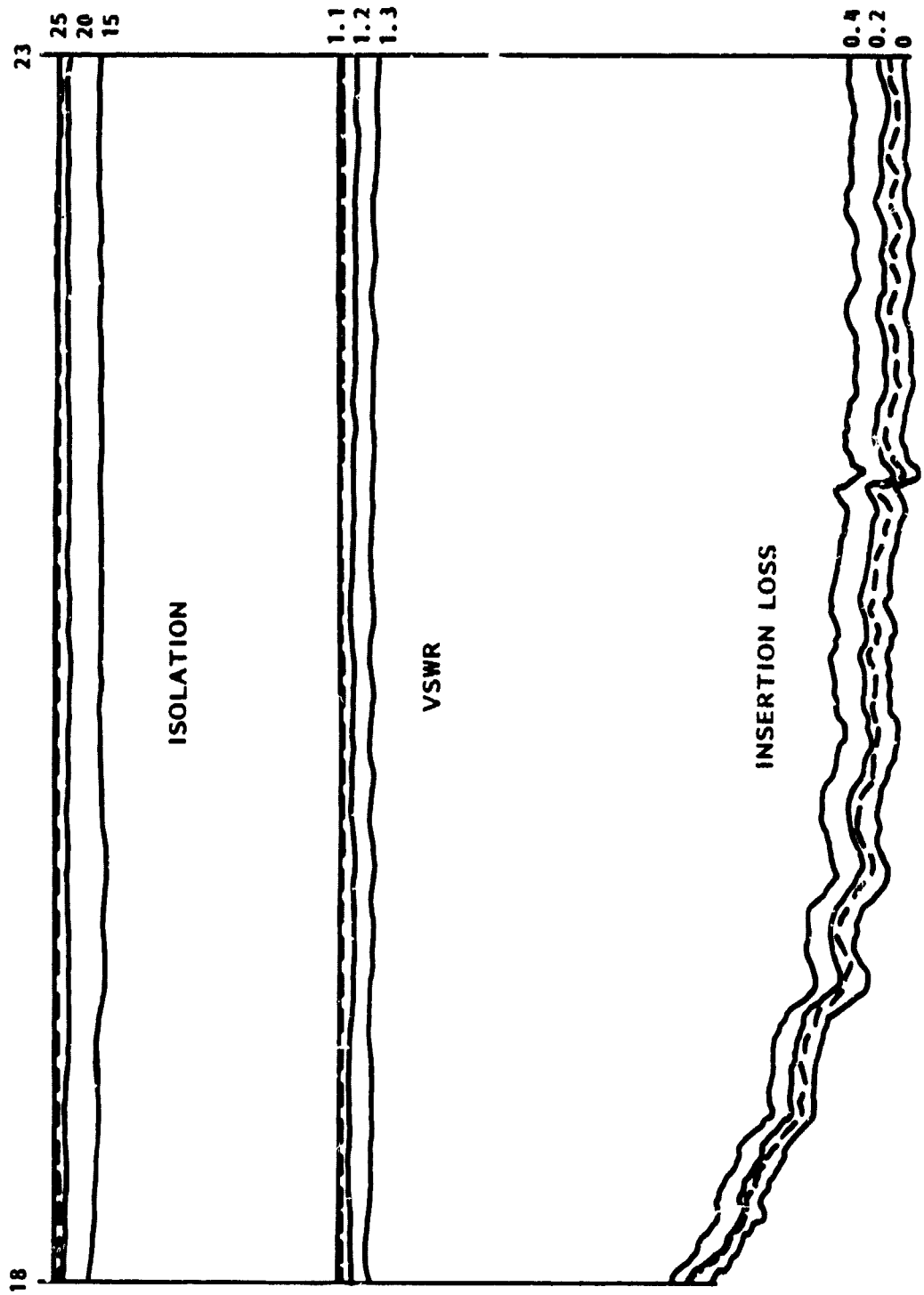


Figure 5-23. Electrical Performance of a 20-GHz Circulator

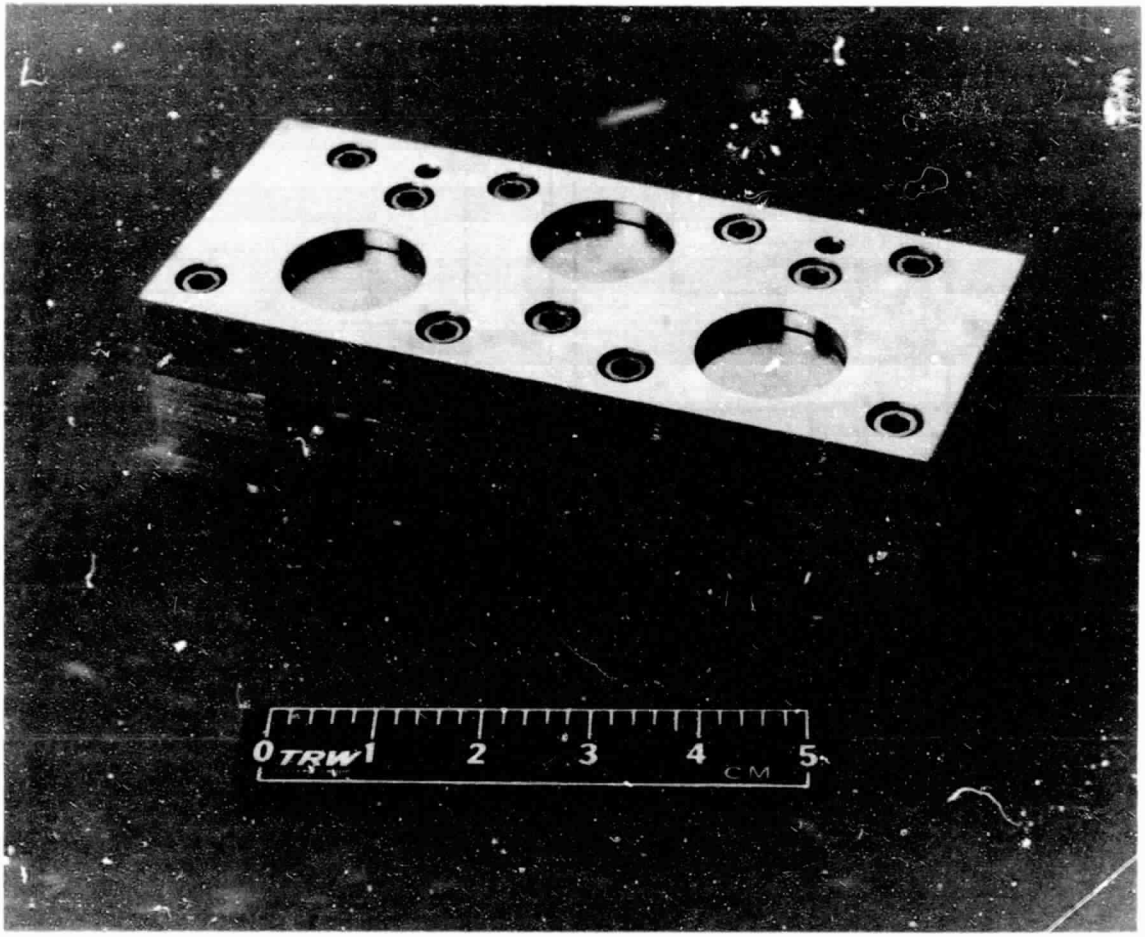


Figure 5-24. Assembly of 3-Junction Circulator Housing

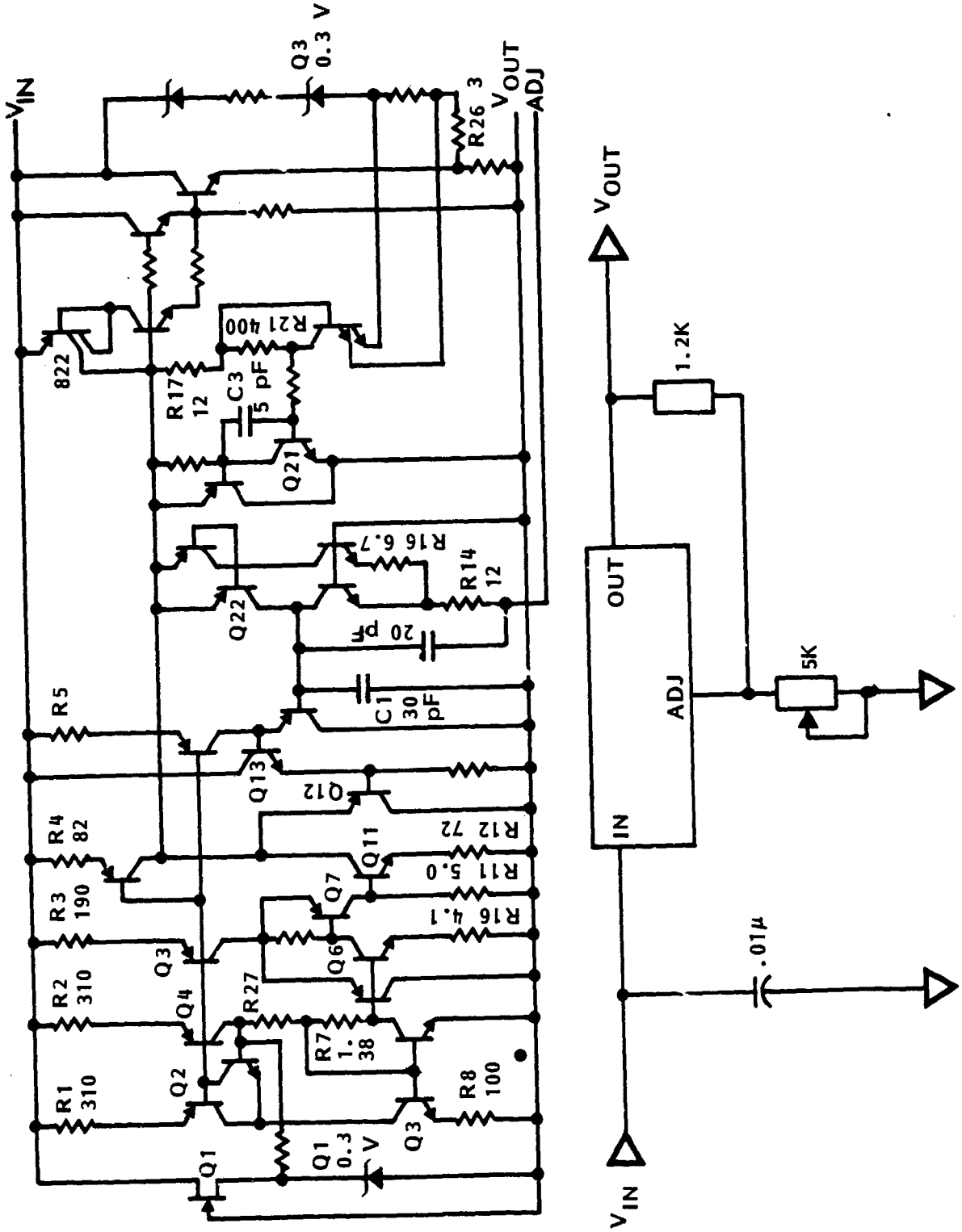


Figure 5-25. Bias Regulator Schematics

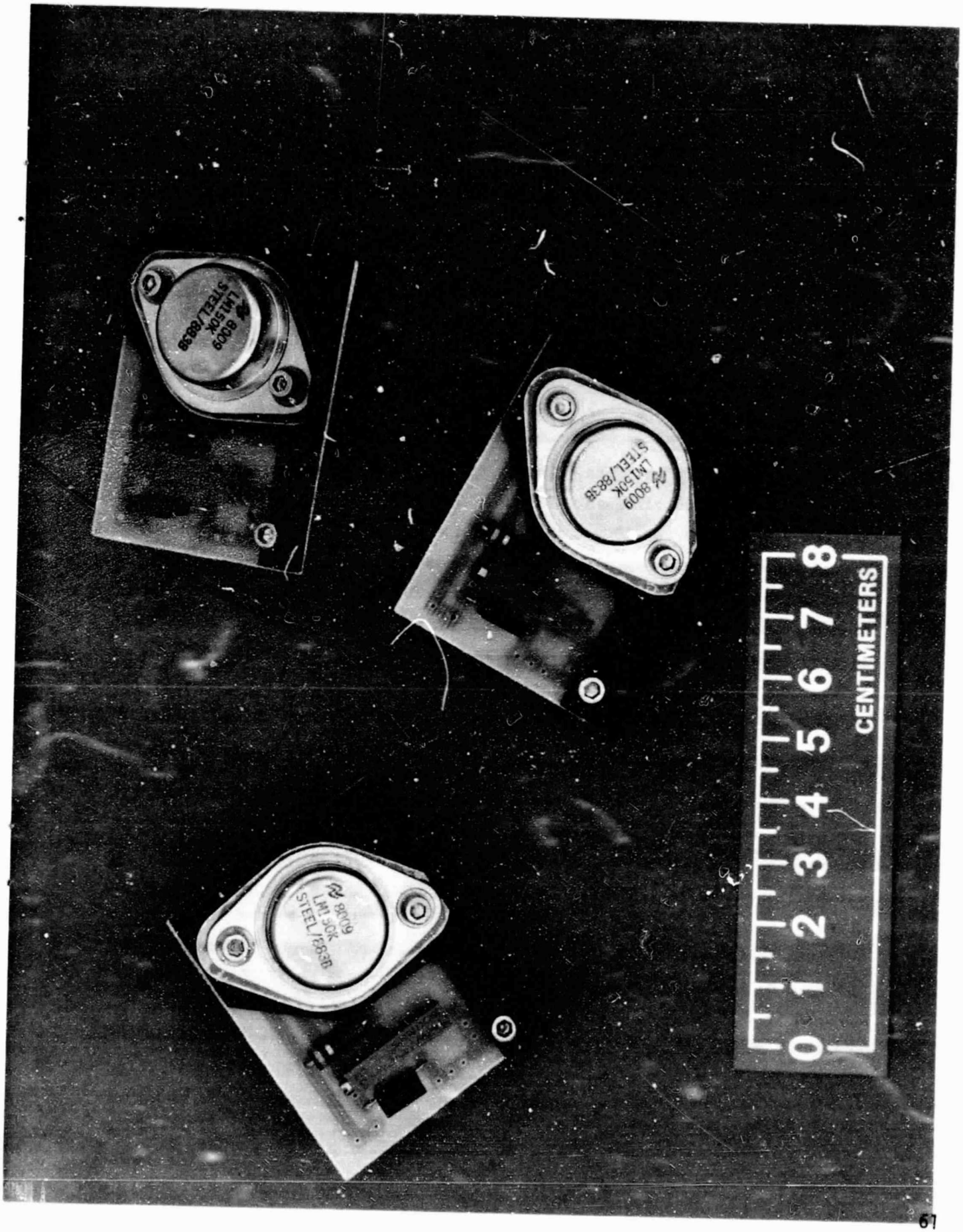


Figure 5-26. Bias Regulator Assembly

6.0 AMPLIFIER INTEGRATION

6.1 SYSTEM SCHEMATIC

The system schematic of the entire amplifier is shown in Figure 6-1. The system consists of two circulator assemblies, three IMPATT stages, fourteen voltage regulators, and one crowbar protection circuit. The circulator assemblies, the IMPATT stages and the voltage regulators have been described in Section 5. The purpose of the crowbar protection circuit is to prevent thermal overloading of the voltage regulators. There are two DC voltages required to power the amplifier; the reason being that there are two types of IMPATT diodes used in the amplifier as explained in Section 3.3. The input stage and the output stage utilize the Varian single-drift diodes, which require a bias voltage of 28 V. The driver stage, on the other hand, utilizes a Raytheon double-drift diode, which requires an operating voltage of 54 V. Consequently, two DC voltages, 60 V and 32 V, are required to power the amplifier. If only the 60-V supply were used, excessive voltage drop would be imposed on the bias regulators for the input and output stages, resulting in an unnecessarily large heat dissipation. The role of the crowbar protection circuit is to become a short-circuit in the event that the +60 V supply is erroneously connected to the +32 V input. When the crowbar circuit is activated, the 5-A fuse blows, thereby removing the power supply from the bias regulators. The schematic of the crowbar circuit is shown in Figure 6-2.

6.2 PHYSICAL DESCRIPTION

All components of the amplifier are attached to a common baseplate by screws. The component layout of the unit can be seen from the photograph of Figure 6-3. The components which are contained in the system schematic (Figure 6-1) are readily identifiable from the photograph and no further elaboration is needed. The advantage of this layout is that only the baseplate is required to be mechanically sturdy and that heat removal can be done through the same baseplate. The baseplate dimensions are 19.8 cm (7.8") wide and 23.4 cm (9.2") long. The entire unit measures 8.53 cm (3.36") tall with the amplifier cover on. A water cooling plate is also provided with the amplifier. The cooling plate is conformal to the baseplate and is 1.90 cm (0.75") thick.

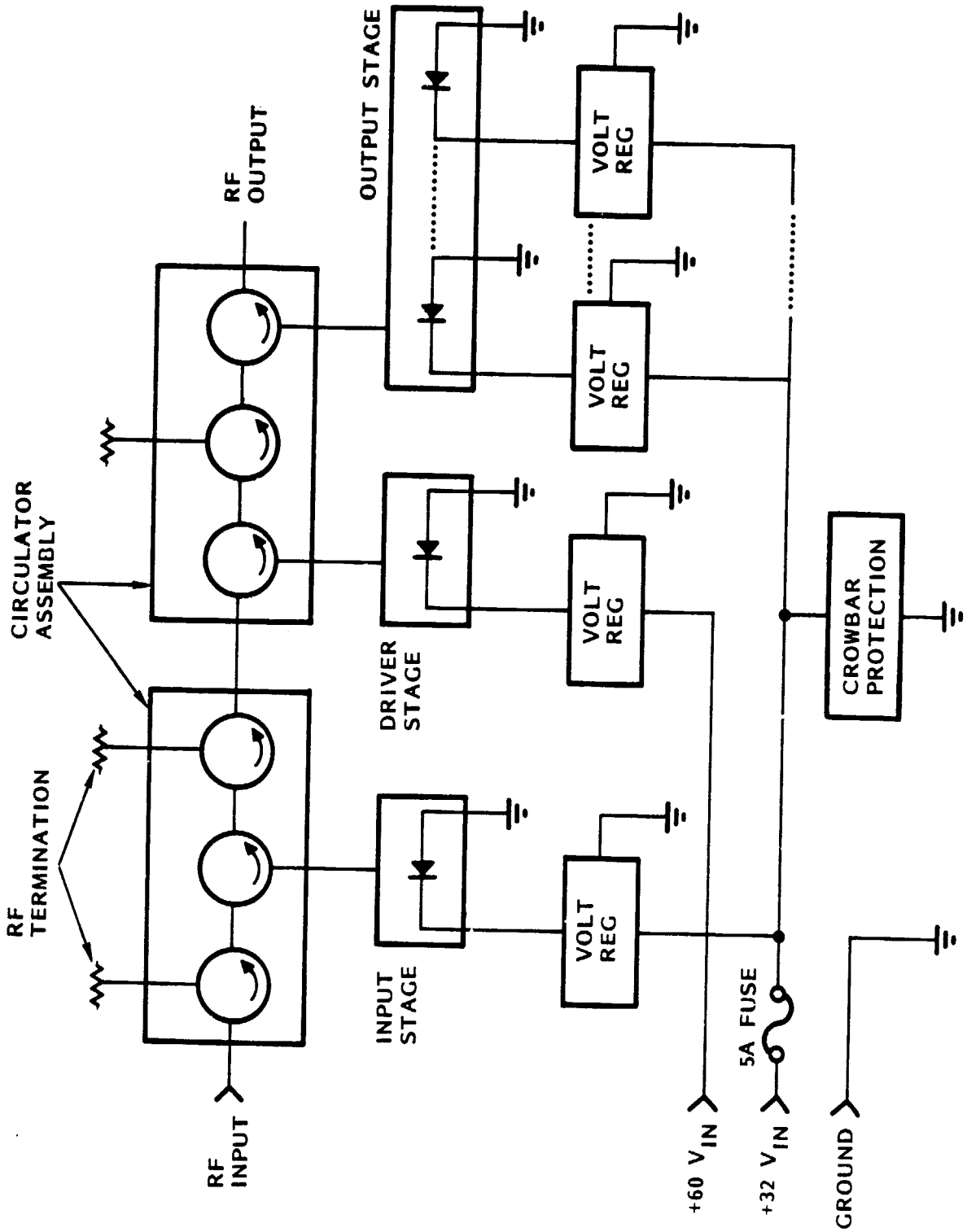


Figure 6-1. IMPATT Amplifier's System Schematic

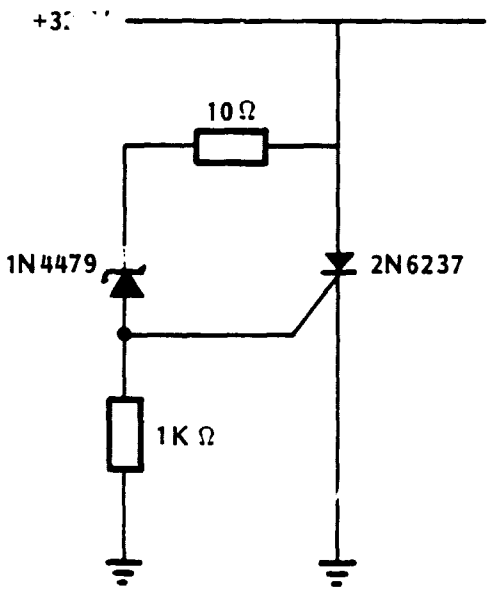


Figure 6-2. Crowbar Protection Circuit Schematic

Figure 6-3. Component Layout of the Amplifier

A photograph of the amplifier unit together with the water cooling plate is shown in Figure 6-4. The unit weighs 3.45 kg (7 lbs., 9.55 oz.) with the cover on. The water plate weighs 2.1 kg (4 lbs., 0.5 oz.).

6.3 INTERFACE REQUIREMENT

Both RF input and output connections are done via a standard WR-42 waveguide with a UG595/U flange. The source and load SWR should not exceed 1.3. The input signal must be of a single frequency within the range from 19.5 to 19.8 GHz (see Section 7.6) and not exceed 0.064 W CW. DC inputs to the unit are connected through standard banana jacks. One jack for the +60 V connection, one for the +32 V connection, and one for the ground connection. The cooling of the amplifier can be done via the water cooling plate provided. Regular cold tap water can be used. Alternately, the amplifier can be mounted onto any structure provided by the user which is conformal to the baseplate of the amplifier and is maintained in a temperature of about 25°C.

6.4 MECHANICAL DRAWINGS

Some relevant mechanical drawings of the various components of the amplifier are shown in this section. A listing of the drawings follows.

Component	Drawing No.	Title
Input Stages	SK-7325-522	K-Band Single Diode Cavity, Top, 0.030 Ht.
	SK-7325-527	K-Band Single Diode Cavity, Bottom
Output Stages	SK-C415-862	Full ht. Cavity Top, 12-diode, Scalloped Sidewall
	SK-C415-863	Diode Block, 12-Diode Cavity
Circulator Assembly	SK-7325-607	3-Junction Assembly, WR-42
Amplifier Housing	SK-C415-934	Amplifier Cover, 20 GHz Combiner
	SK-C415-933	20 GHz 12-Diode Amp. Baseplate
Amplifier Assembly	SK-C415-1099	20 GHz Amplifier Final Assembly

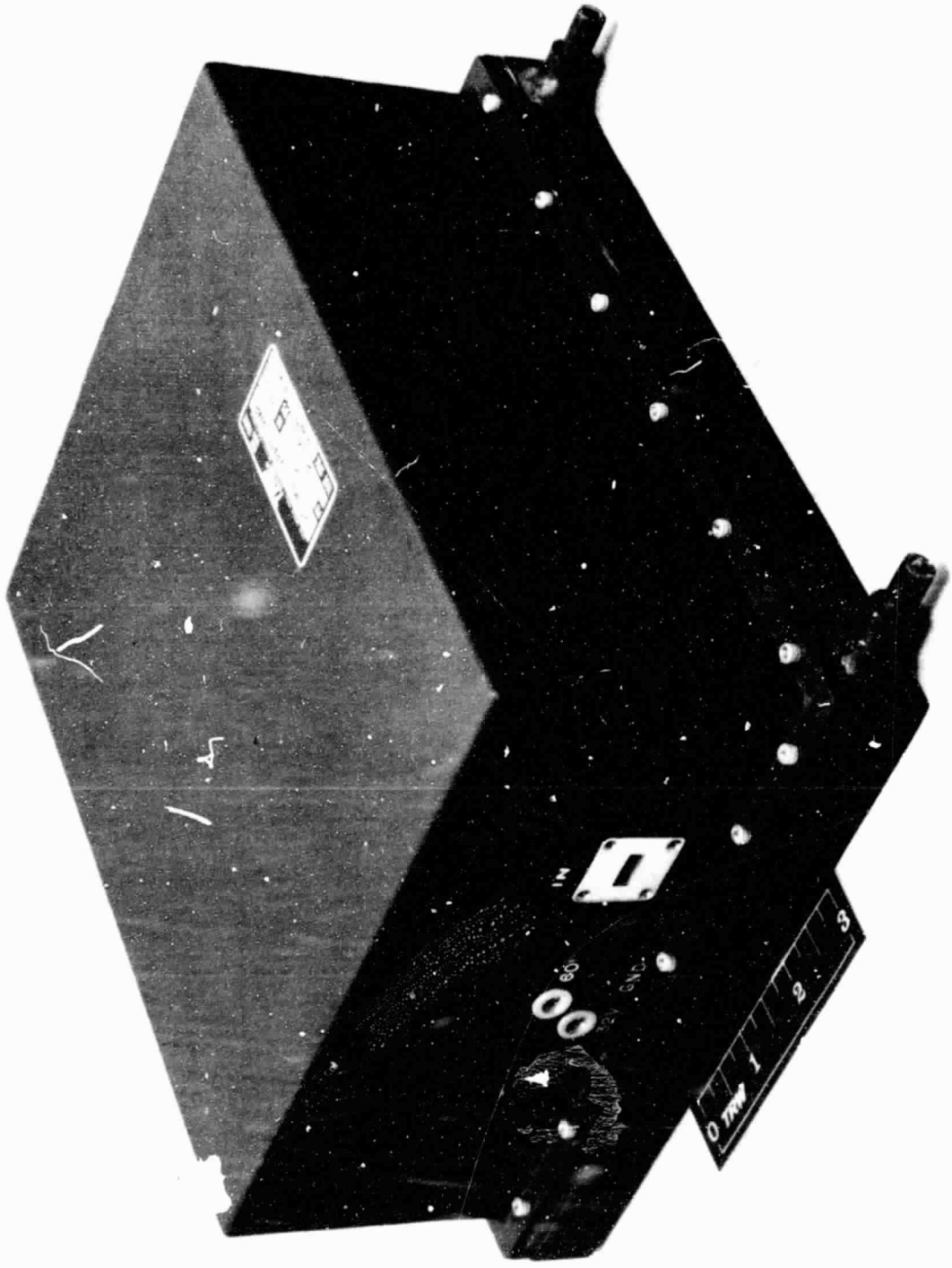


Figure 6-4. Exterior View of Entire Amplifier

SK 7325-522

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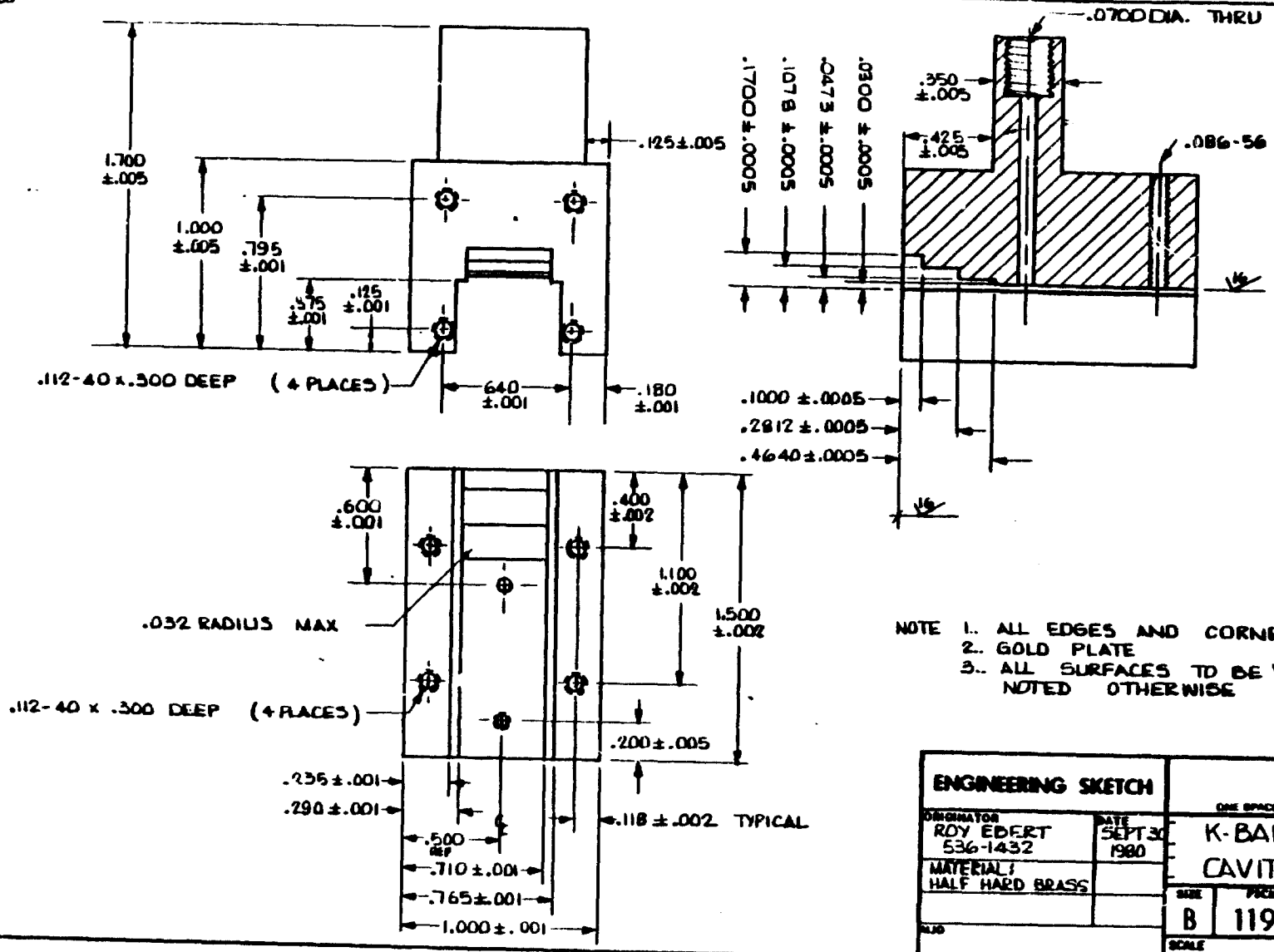

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NOTE 1.. ALL EDGES AND CORNERS TO BE SHARP
2.. GOLD PLATE
3.. ALL SURFACES TO BE 32 EXCEPT WHERE NOTED OTHERWISE

ENGINEERING SKETCH		TRW
ORIGINATOR ROY EDERT 536-1432	DATE SEPT 30 1980	K-BAND SINGLE DIODE CAVITY, TDP .030 HT
MATERIAL: HALF HARD BRASS		SIZE B · PROJ NO. 11982 · SK-7325-522
		SCALE · SHEET 1 OF

SK 7325-527

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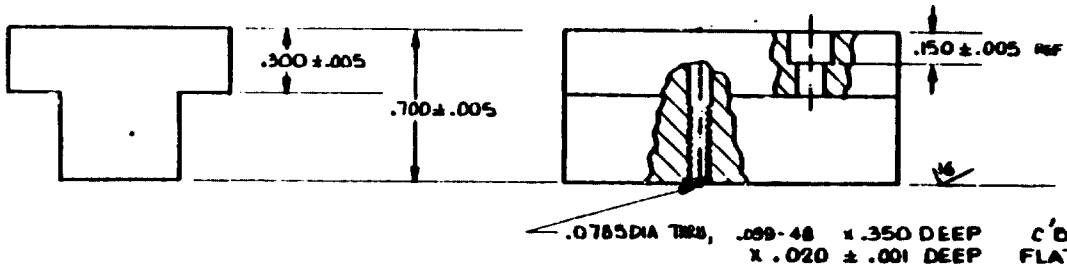
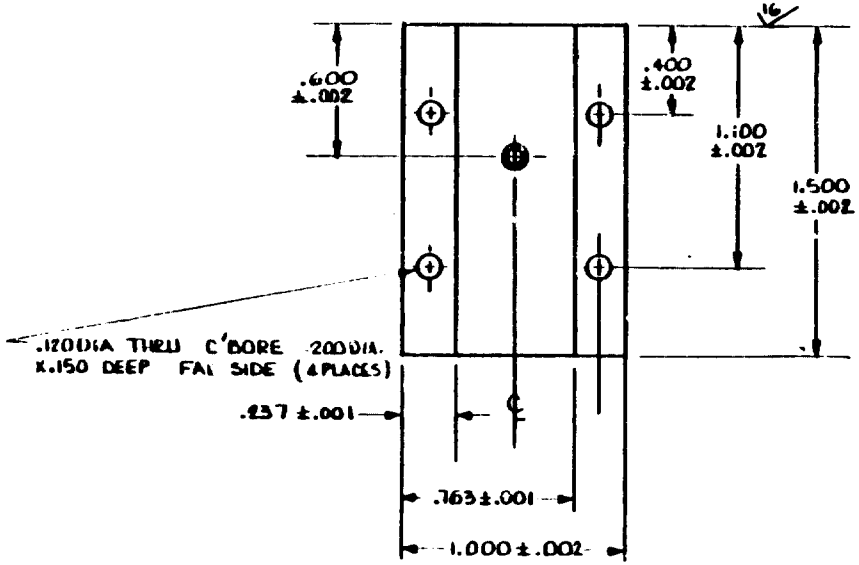
A	CHANGE MATERIAL TO OFHC COPPER	9/16/80	J. Douglas





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2. ALL SURFACES TO BE 32 EXCEPT WHERE NOTED OTHERWISE
3. GOLD PLATE

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DESIGNATOR: ROY EBERT 536-1432	DATE: OCT 1 1980	K-BAND SINGLE DIODE CAVITY BOTTOM
MATERIAL: OFHC COPPER		SIZE: B · PCS NO.: 11982 · SK-7325-527 A
		SCALE · SHEET 1 OF

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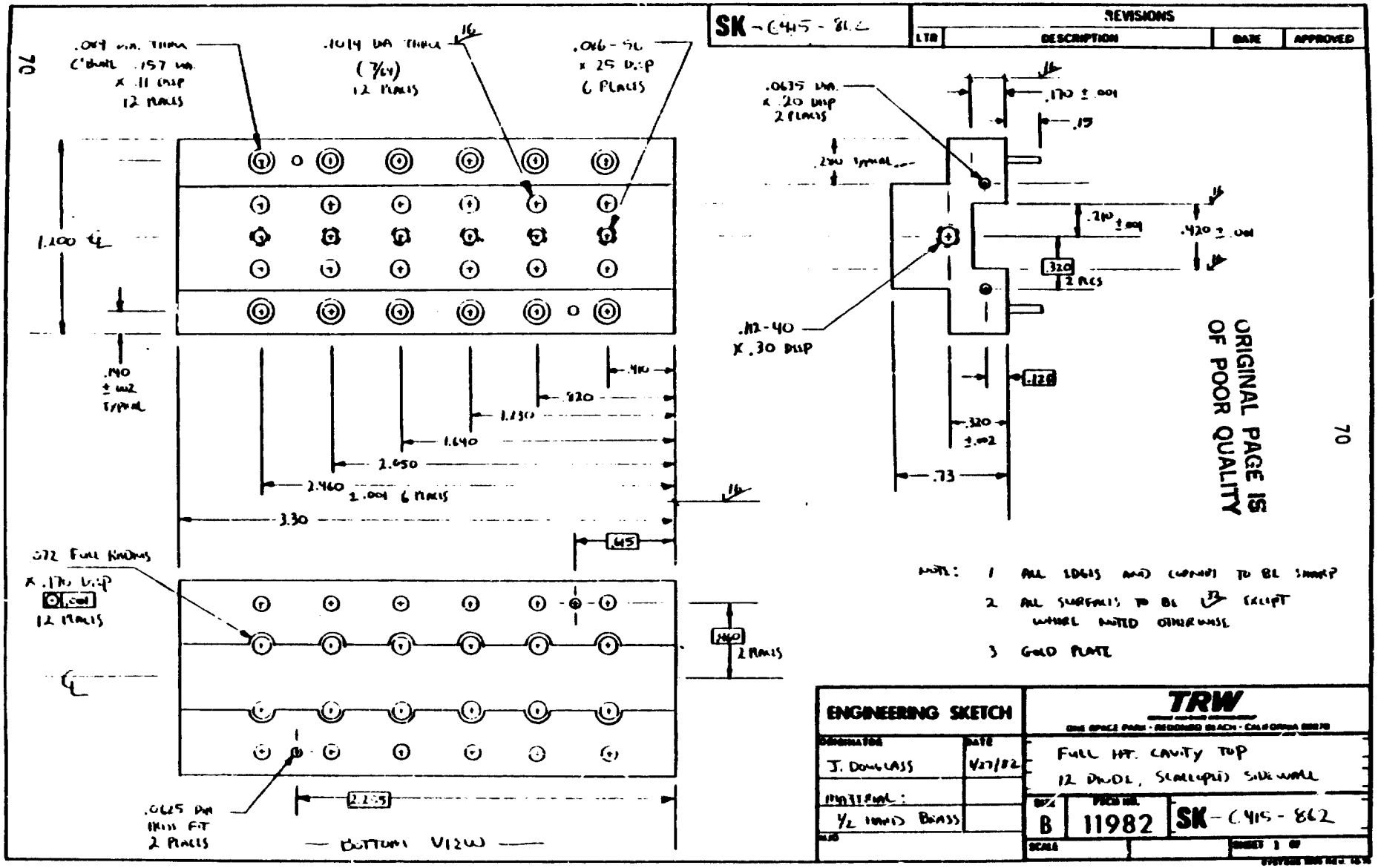
SK-C415-862
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.1014 DIA THRU (7/64) 12 PLACES
.086-56 X .25 DEEP 6 PLACES
1.100
.140 ± .002 TYPICAL
.110
.820
1.130
1.640
2.050
2.460 ± .004 6 PLACES
3.30
.445
.072 FULL RADIUS X .170 DEEP .001 M C 12 PLACES
.240 2 PLACES
.0625 DIA THRU FIT 2 PLACES
2.255
BOTTOM VIEW
.0635 DIA. X .20 DEEP 2 PLACES
.170 ± .001
.15
.280 TYPICAL
.280 ± .004
.420 ± .004
.320 2 PLACES
.112-40 X .30 DEEP
.120
.320 ± .002
.73
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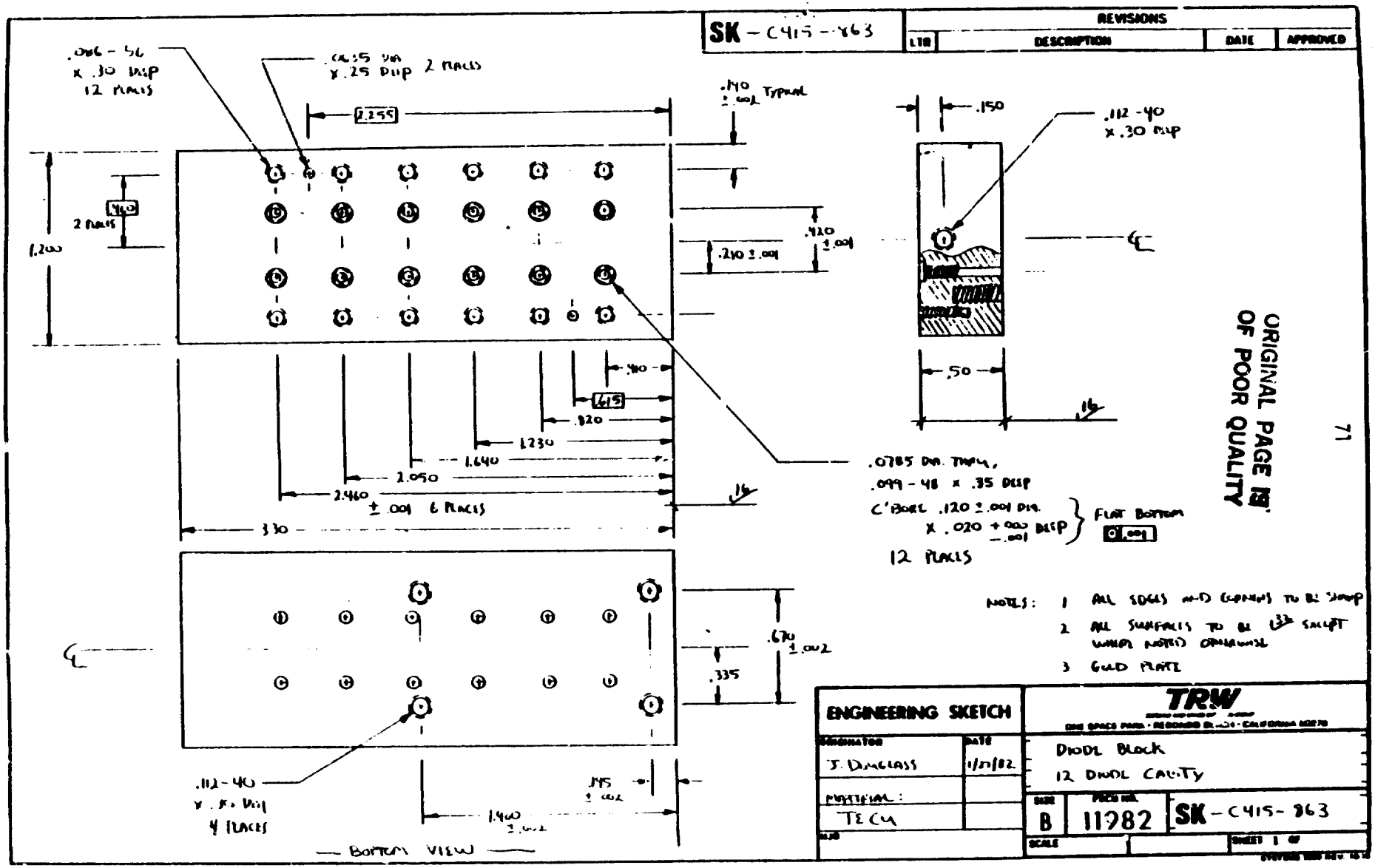
2 ALL SURFACES TO BE 125 EXCEPT WHERE NOTED OTHERWISE
3 GOLD PLATE
ENGINEERING SKETCH
DRAWN BY J. DOUGLASS
DATE 4/27/82
MATERIAL: 1/2 HARD BRASS
TRW
FULL HT. CAVITY TOP 12 DIODE, SCALLOPED SIDEWALL
SIZE B
PART NO. 11982
SK-C415-862
SCALE
SHEET 1 OF
70



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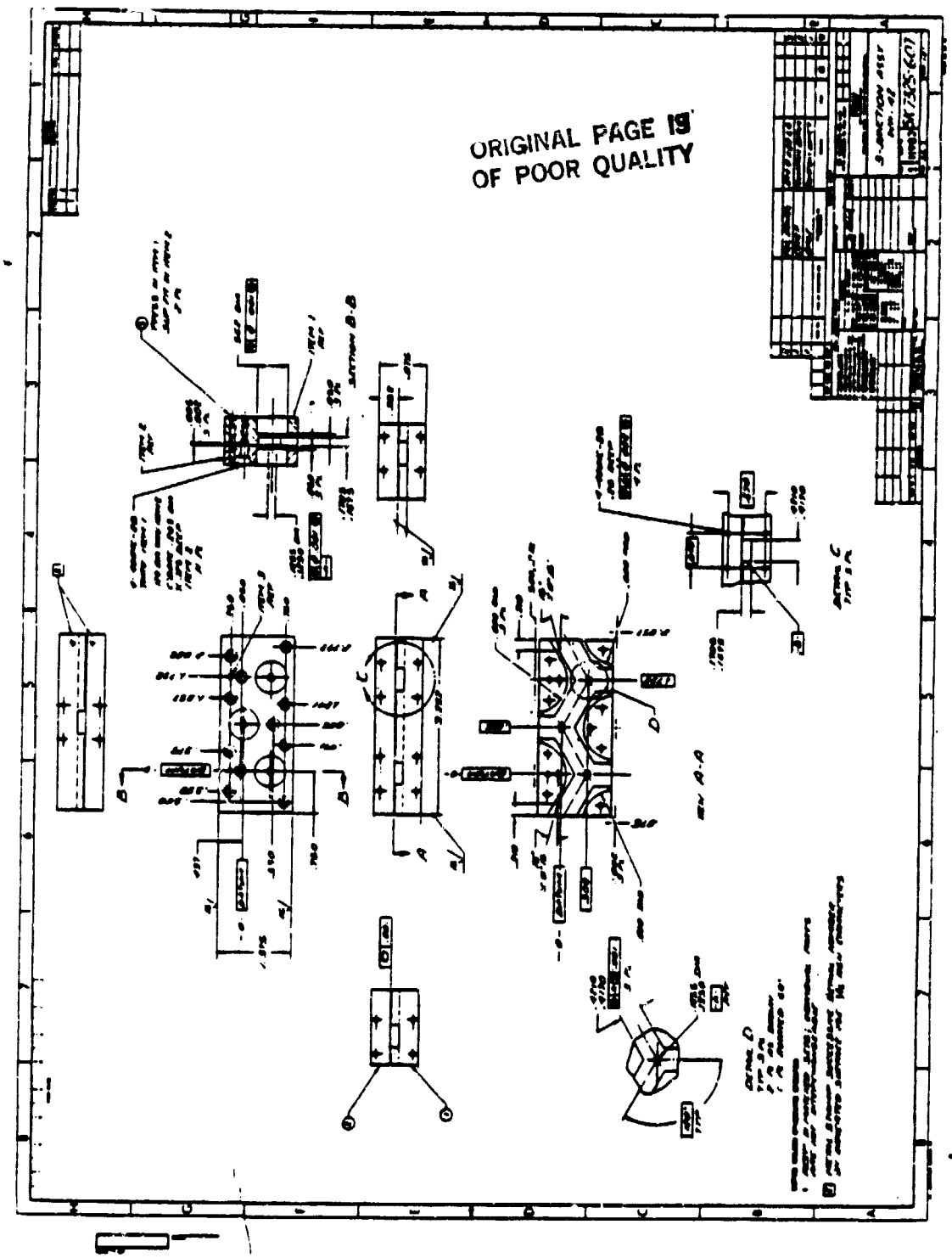
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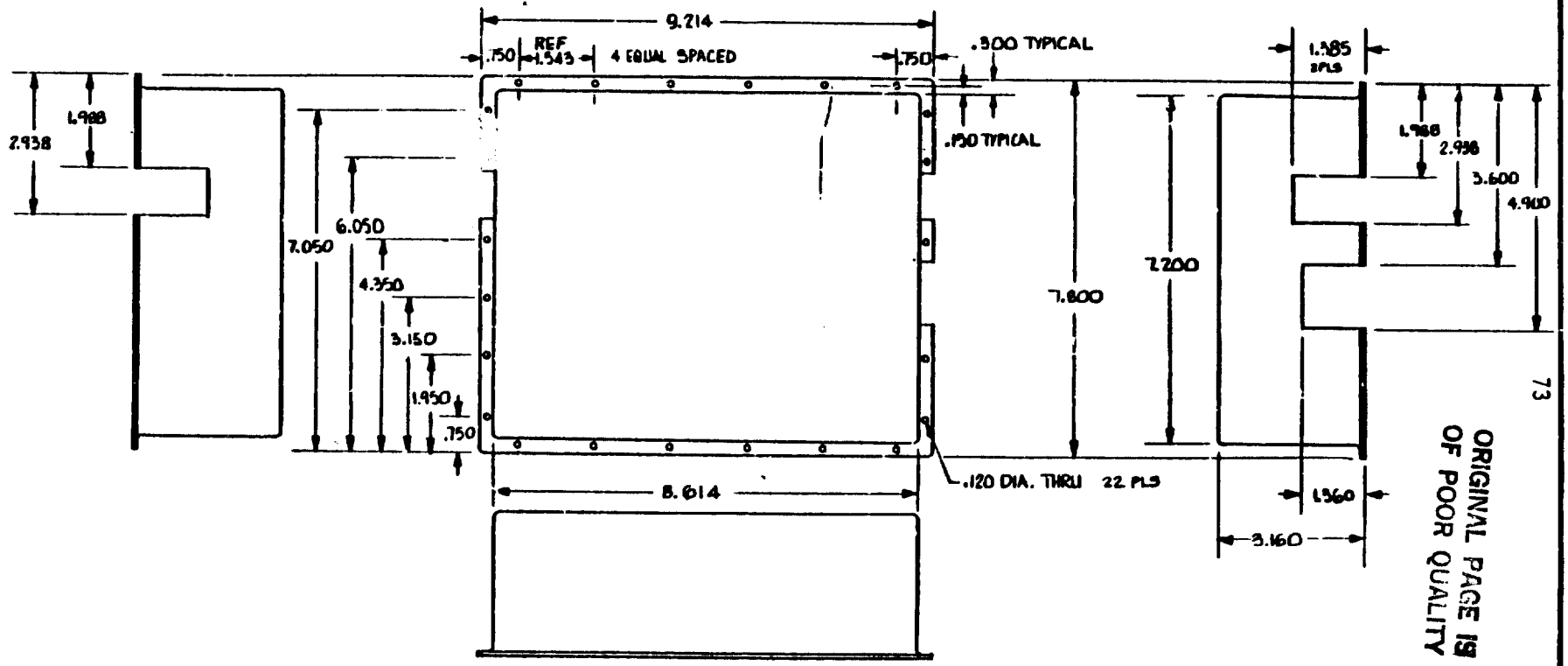

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ENGINEERING SKETCH		TRW ONE SPACE PARK · REDONDO BEACH · CALIFORNIA 90278	
ORIGINATOR ROY EBERT	DATE MAR. 29 '82	AMPLIFIER COVER 20GHZ COMBINER	
MATERIAL: .060 6061 ALUMINUM		SIZE B	FSCM NO. 11982	SK C415-934
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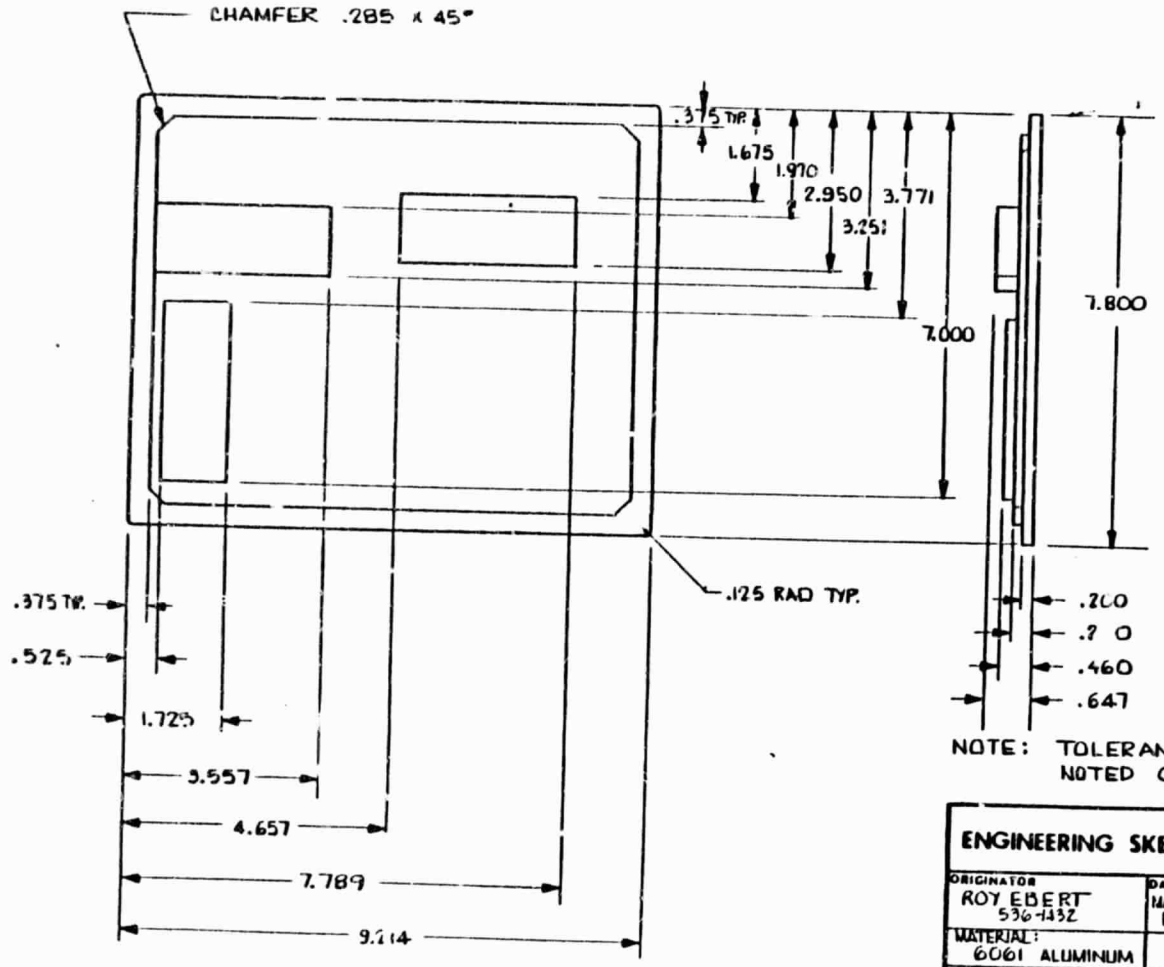

NOTE: TOLERANCES .XXX ±.002 EXCEPT WHERE NOTED OTHERWISE

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ENGINEERING SKETCH		TRW ONE SPACE PARK · REDONDO BEACH · CALIFORNIA 90278	
ORIGINATOR: ROY EBERT 536-1432	DATE: MAR 26 1982	20 GHz 12 DIODE AMP BASE PLATE	
MATERIAL: 6061 ALUMINUM		SIZE: B	FSCM NO.: 11982
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SK C415-933

SYSTEMS 3153 REV 1-78

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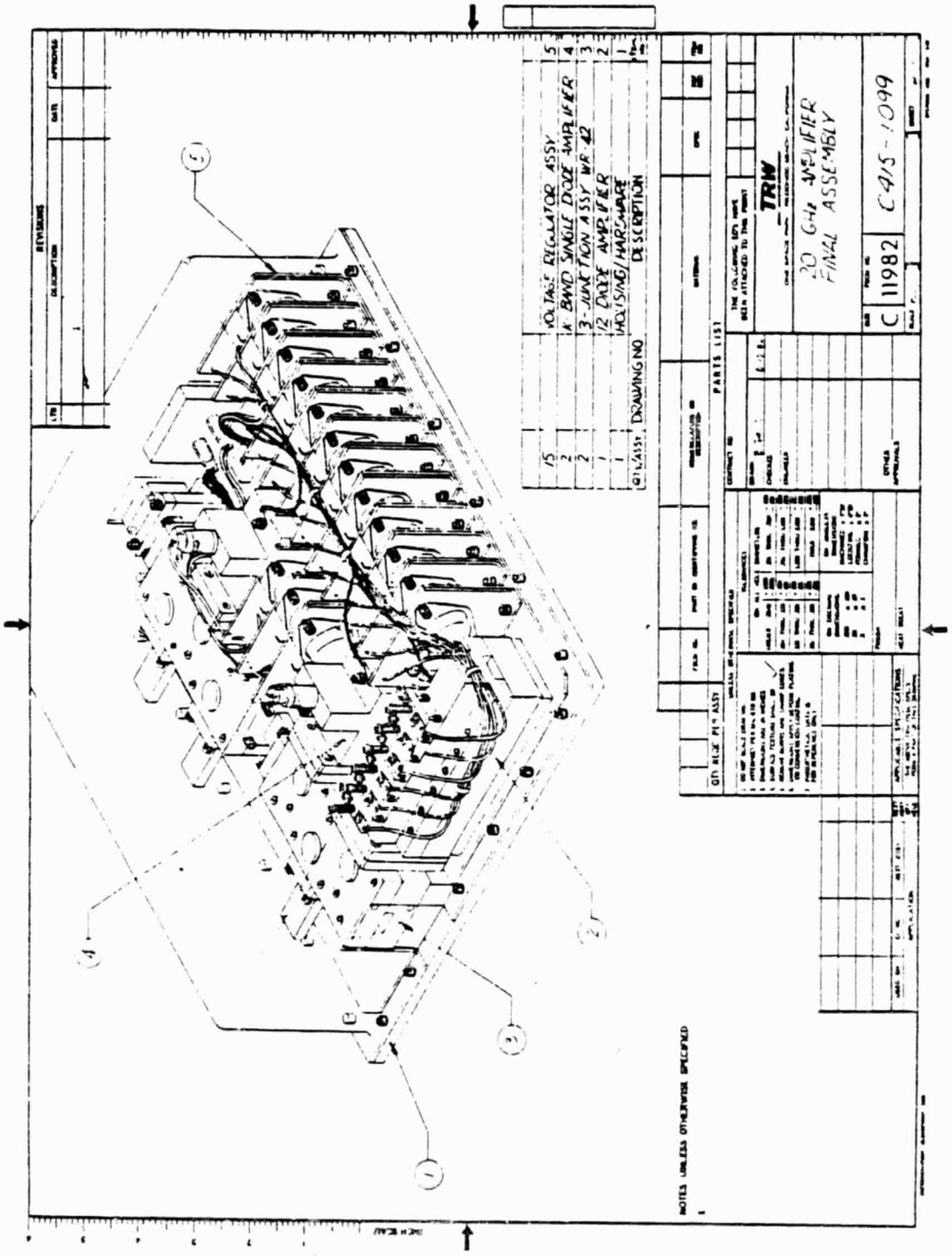


7.0 AMPLIFIER EVALUATION

7.1 TEST OBJECTIVES

The test objectives are to determine whether the POC model is meeting the performance requirements called for by the contract. The requirements are identified in Section 2.2 and are repeated here in condensed form.

RF Output Power	20 W CW Min.
Operating Frequencies	19.7 GHz to 20.2 GHz
RF Power Gain	30 ±1 dB Minimum
Gain Variation	±1 dBm, 19.7-20.2 GHz Maximum
Gain Slope	0.15 dB per MHz Maximum
Phase Linearity	10° P-P Deviation Maximum
Group Delay Variation	0.5 nsec per 50 MHz Maximum
Harmonic Response	-50 dBc Minimum
Spurious Response	-60 dBc Minimum
AM/PM Conversion	5° ±1° per dB of Input Power Maximum
DC to RF Conversion Efficiency	20% Minimum
Overdrive Capacity	+5 dB
Input and Output SWR	1.3 Maximum

7.2 MEASUREMENT IDENTIFICATION

To adequately characterize the POC model electrical performance, seven different measurements (or tests) are required. The seven measurements are listed in Table 7-1. Also listed in the table are the parameters which can be evaluated using data from the various measurements. As can be seen, the parameters in the table identify totally with the specifications listed above. All measurements listed in the table can be grouped into scalar measurements, vectorial measurements, and noise measurements. Consequently, only three different test setups are needed to perform the entire task. The test setup and test methodology are described in a subsequent section.

7.3 TEST AND CORRECTIVE ACTION SEQUENCES

It should be noted that some measurements cannot be performed until other measurements are completed. For example, efficiency measurement is meaningful only when the transmitter is operating properly. The same applies to noise

TABLE 7-1. POC MODEL TESTS/MEASUREMENTS

	Tests/Measurements	Resulting Data for Evaluation
1.	Output Power vs. Input Power	Output Power, Gain of Transmitter
2.	Output Power vs. Frequency	Bandwidth, Gain Variation, Gain Slope
3.	Output Spectrum	Power Levels of Coherent and Noncoherent Components
4.	Efficiency Measurement	Transmitter DC to RF Conversion Efficiency
5.	Output Phase vs. Frequency	Phase Linearity, Group Delay Variation
6.	Output Phase vs. Input Powe	AM/PM Conversion
7.	Noise Measurements	AM/PM Noise Performance

measurements. Figure 7-1 contains a test sequence which shows the proper order of each measurement. Also shown in Figure 7-1 is the corrective action sequence. In the event that the POC model fails to meet the test objective, a diagnosis is performed to determine whether a readjustment or a redesign is necessary to improve the transmitter performance. Upon taking the corrective action, the test cycle is repeated.

7.4 TEST METHODOLOGY

7.4.1 Scalar RF Measurements

The measurements listed as 1 to 4 in Table 7-1 are termed scalar measurements since only the power level and frequency information of the test signal can be obtained. Figure 7-2 shows the test setup. It consists mainly of a variable frequency signal source, a power monitor at the input port of the circuit under test, a power monitor at the output port, and a spectrum analyzer at the output port.

7.4.2 Vectorial RF Measurements

The measurements listed as 5 through 7 in Table 7-1 are vectorial measurements since, in addition to power and frequency information, phase information of the test signal is also obtained. The test setup is basically a network analyzer, as shown in Figure 7-3. The setup contains a variable frequency source and a network analyzer which compares the phase difference between the input and output ports of the circuit under test. Two mixers and one local oscillator are used to downconvert the K-band test signal into a lower frequency signal which the network analyzer can handle.

7.4.3 Noise Measurements

It is well known that all electrical noise in a sinusoidal waveform can be categorized into AM and PM. Although the subject is highly specialized, noise performance is very important in any information transmitting and receiving system. The standard method for both AM and PM noise measurements is the so-called two-oscillator technique. The measuring system is shown in Figure 7-4. The UUT (unit under test) is measured against a reference oscillator of known and superior noise performance. A common frequency source

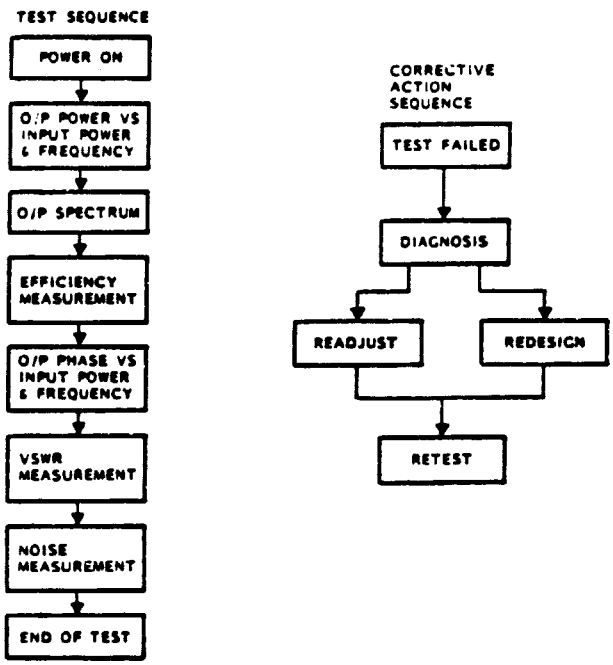


Figure 7-1. POC Model Test and Corrective Action Sequences

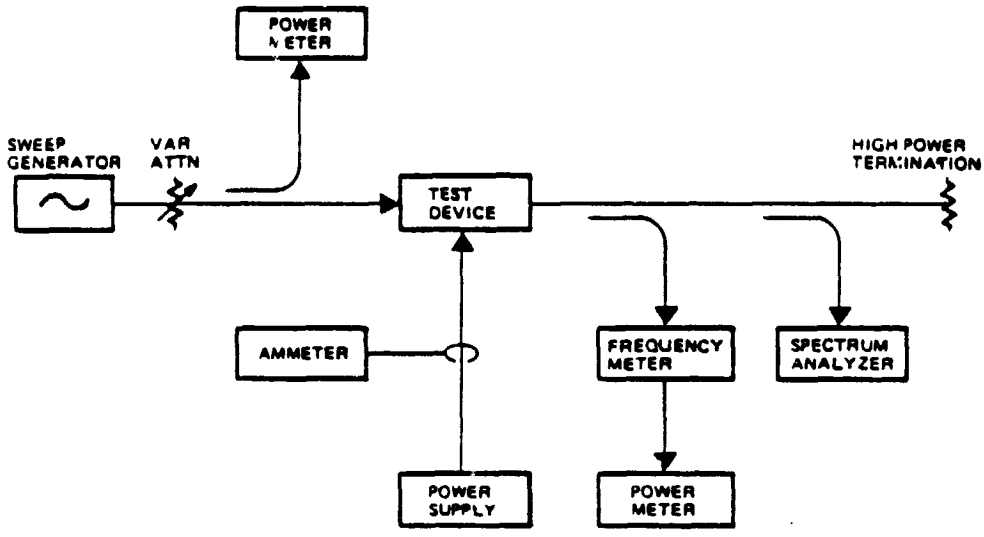


Figure 7-2. Scalar Measurement Setup

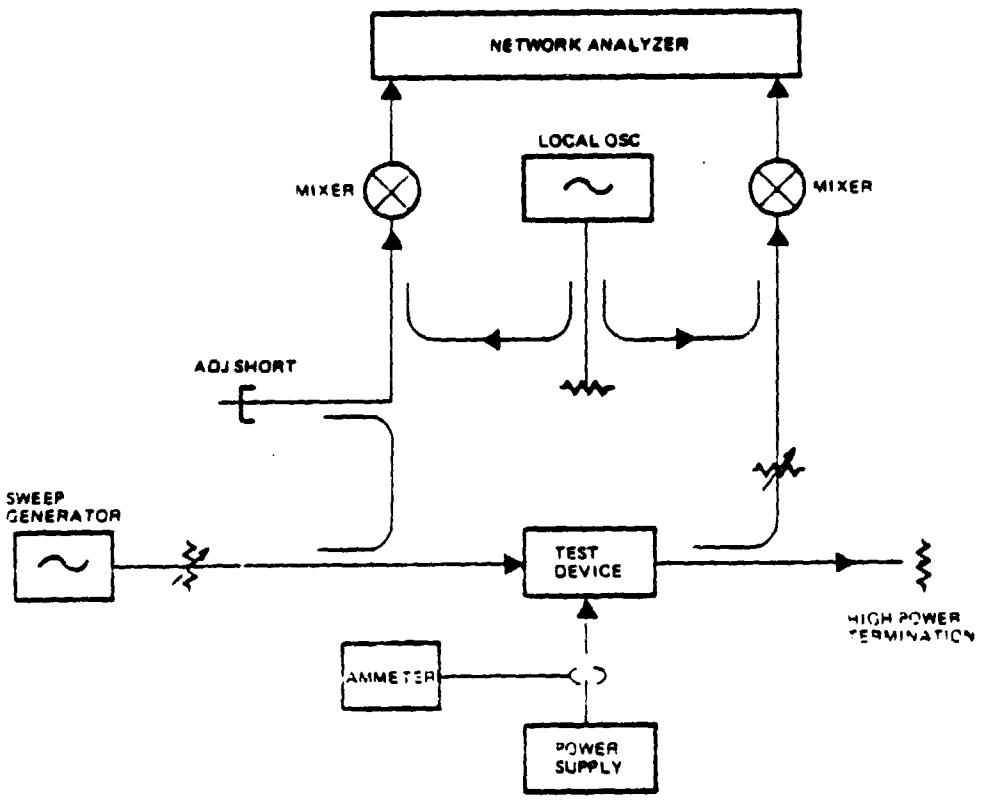


Figure 7-3. Vectorial Measurement Setup

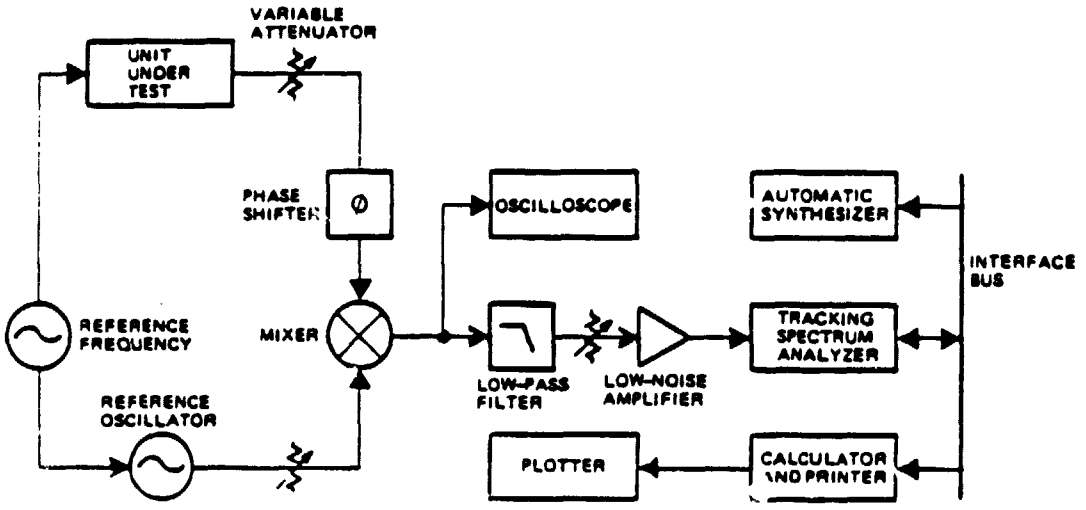


Figure 7-4. Automatic Noise Measuring System - Two-Oscillator Technique

is used to injection-lock the reference oscillator and to excite the UUT. This process assures that the outputs of the UUT and the reference oscillator are coherent. The two outputs are then fed to the mixer. The mixer functions either as a synchronous detector or a phase detector, depending on the phase relationship of the two mixer inputs. When the phase shifter is adjusted to zero, the two mixer inputs are in phase and the mixer acts as a synchronous detector. Any AM noise from the UUT is converted to a fluctuating DC centering around a constant voltage V_o. (V_o is different from zero and is a function of the mixer input magnitudes.) When the phase shifter is adjusted to 90°, the two mixer inputs are in phase quadrature and the mixer acts as a phase detector. Any PM noise from the UUT is converted into a fluctuating DC centering around 0 V. An oscilloscope is used to monitor whether AM noise or PM noise is being measured.

The output of the mixer represents the noise quantity to be measured. A lowpass filter eliminates any power leakage from the mixer inputs. A low noise amplifier boosts the measurement sensitivity by amplifying the mixer output signal.

A spectrum analyzer, desk-top calculator, and a frequency synthesizer automatically evaluate the actual noise power. The synthesizer serves as a local oscillator for the spectrum analyzer, which needs a reference to set the frequencies and bandwidths to be measured. The calculator controls all the operations, stepping from one measurement bandwidth to the next and making 100 measurements at each bandwidth. These are statistically combined in the calculations; the necessary corrections are applied to compensate for equipment characteristics.

7.4.4 Thermal Cycling Test

In order to demonstrate the qualification as a flight hardware, the POC transmitter was subjected to environmental stress, namely, temperature cycling. It should be noted that the thermal cycling test is merely the repeat of some specific electrical test while the POC unit is subjected to temperature extremes. The temperature extremes are chosen from 0°C to +50°C. The tests to be conducted at both of these tempertures are of output power, operating frequencies,

and power gain. The test setup for the measurements is essentially that of the scalar setup with the addition of a thermal plate and a temperature indicator. The additional hardware are connected as shown in Figure 7-5.

7.5 TEST EQUIPMENT IDENTIFICATION

7.5.1 Scalar Test Setup

Variable Attenuator - Hewlett Packard, K382A, 1 required.

High Power Termination - Litton/Airtron, AIL-42-A, 1 required.

Power Supply - Hewlett Packard, 6438B, 1 required.

Current Meter - Hewlett Packard, 6348B, 1 required.

20-dB Coupler - Hewlett Packard, K752D, 3 required.

Frequency Meter - Hewlett Packard, 532A, 1 required.

Power Meter - Hewlett Packard, 432A with K486A sensor, 2 required.

Sweep Generator - Hewlett Packard, 8690B frame, 8696A plug-in, 1 required.

Spectrum Analyzer - Hewlett Packard, 8565A, 1 required.

7.5.2 Vectorial Test Setup

Variable Attenuator - Hewlett Packard, K382A, 2 required.

High Power Termination - Litton/Airtron, AIL-42-A, 1 required.

Power Supply - Hewlett Packard 6438B, 1 required.

Current Meter - Hewlett Packard, 6438B, 1 required.

Sweep Generator - Hewlett Packard, 8690B frame, 8696A plug-in, 2 required.

Mixers, Power Splitter, Adj. Short - Hewlett Packard, K8747A, 1 required.

Network Analyzer - Hewlett Packard, 8410B frame with 8411 A harmonic converter and 8412A plug-in, 1 required.

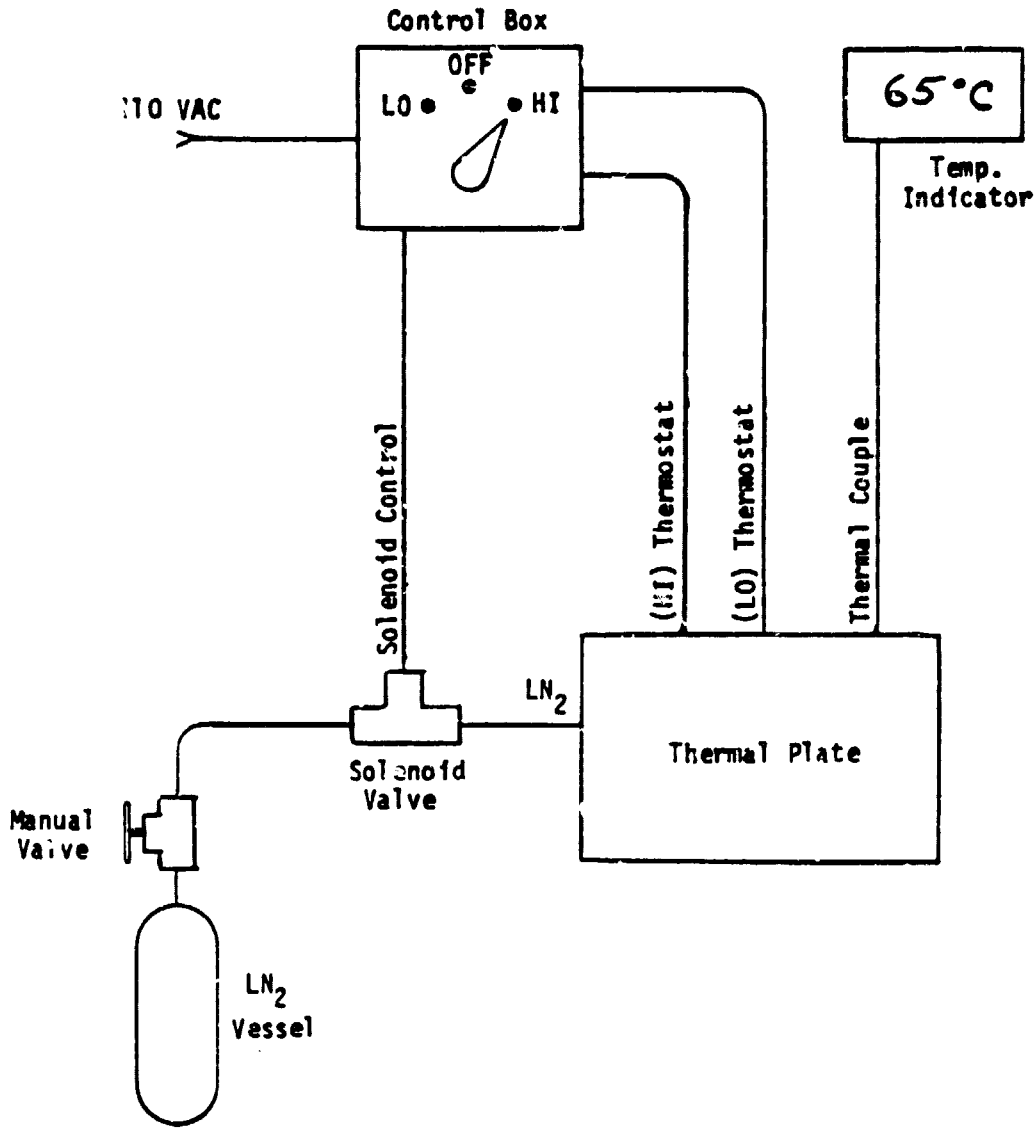


Figure 7-5. Thermal Setup

7.5.3 Noise Test Setup

Variable Attenuator - Hewlett Packard, K382A, 2 required.

Variable Attenuator - Hewlett Packard, 3750A, 1 required.

Reference Oscillator - Hewlett Packard, 8690B frame with 8696A plug-in, 1 required.

Phase Shifter - Waveline 808, 1 required.

Balanced Mixer - MDL, 42MF36-1, 1 required.

Low-Pass Filter - Solar Electronics, 6623, 1 required.

Low-Noise Amplifier - Hewlett Packard, 08640-60506, 1 required.

Oscilloscope - Hewlett Packard, 130C, 1 required.

Spectrum Analyzer - Hewlett Packard, 3571A, 1 required.

Automatic Synthesizer - Hewlett Packard, 3330B, 1 required.

Calculator - Hewlett Packard, 9830B, 1 required.

Printer - Hewlett Packard, 9866B, 1 required.

Plotter - Hewlett Packard, 9862A, 1 required.

7.5.4 Thermal Test Setup

See scalar test setup. Also,

Temperature Indicator - DORIC Trendicator, 400A, 1 required.

Thermal Plan and Control Assembly - TRW Drawing No. SK 7325-613, 1 required.

Miscellaneous - Liquid nitrogen in container, 3/8" dia. stainless steel flexible hose.

7.6 MEASUREMENT DATA EVALUATION

7.6.1 RF Output Power

The RF output power of the amplifier was measured against the RF frequency. Three responses were recorded, namely, (a) the input stage alone, (b) the input and the driver stages in cascade, and (c) the input, driver and output stages in cascade. This arrangement is necessary due to the lack of a power source to drive the driver and output stages. The separate measurements also allow the limiting stage in the amplifying chain to be identified. It can be seen from the measured data that the response of the first stage is much wider and flatter than that of the driver stage whose response is, in turn, better than that of the output stage. Consequently, the response "b" is essentially of the driver stage, and the response "c" is of the output stage.

The responses of the input stage and of the input and driver stages are shown in FIgure 7-6. The response of all three stages in cascade is shown in Figure 7-7. The power output within a bandwidth of 220 MHz (19.555 GHz to 19.775 GHz) can be summarized as follows:

Power Output = min. 0.347 W, max. 0.376 W (1st stage)
= min. 2.24 W, max. 2.52 W (1st and 2nd stages)
= min. 5.75 W, max. 15.49 W (1st + 2nd + 3rd stages)

7.6.2 Operating Frequency

The passband of the amplifier can be read from Figures 7-6 and 7-7. The operating frequencies are:

Operating Frequencies = 18.5 - 20.5 GHz (BW = 2 GHz) (1st stage)
= 19.25- 20.25 GHz (BW = 930 GHz) (1st + 2nd stages)
= 19.555-19.775GHz (BW = 220 MHz) (1st + 2nd + 3rd stages)

7.6.3 RF Power Gain

The power gain information of the amplifier can be extracted from Figures 7-6 and 7-7. The power gains are, with the input level fixed at 20 mW and a bandwidth of 220 MHz (19.555 GHz to 19.775 GHz).

Power Gain = min. 12.4 dB, max. 12.75 dB (1st stage)
= min. 8.1 dB, max. 8.25 dB (2nd stage)
= min. 3.6 dB, max. 8.4 dB (3rd stage)
= min. 24.6 dB, max. 28.9 dB (entire amplifier)

7.6.4 Gain Variation

Gain variation is defined as the difference of maximum gain and minimum gain. The gain variation of the amplifier is, in reference to Figure 7-7:

		Bandwidth
Gain Variations =	±0.5 dB at 19.555 to 19.642 GHz	87 MHz
=	±1.0 dB at 19.555 to 19.672 GHz	117 MHz
=	±1.5 dB at 19.555 to 19.71 GHz	155 MHz
=	±2.0 dB at 19.555 to 19.755 GHz	200 MHz
=	±2.2 dB at 19.555 to 19.775 GHz	220 MHz

C - 2

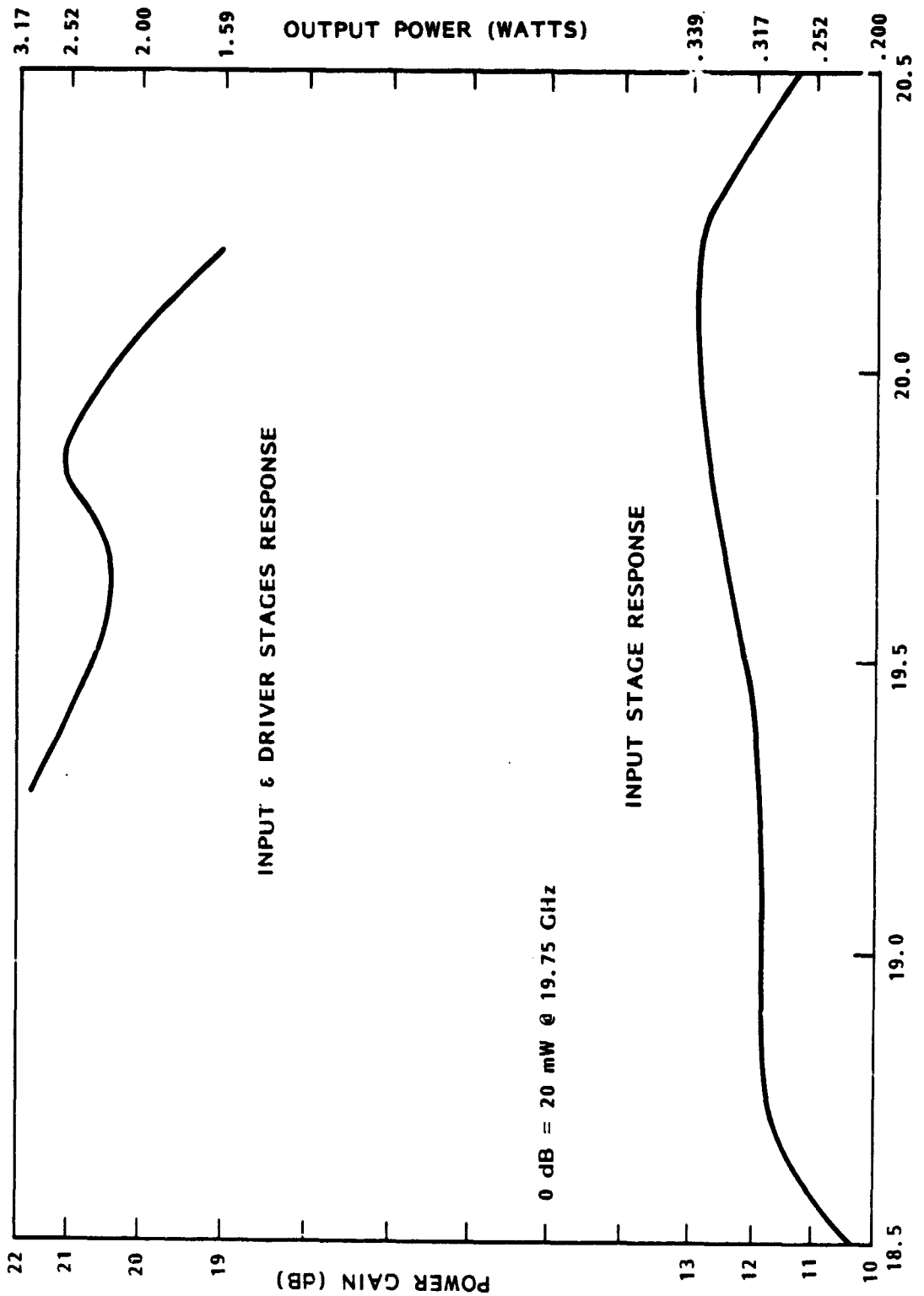


Figure 7-6. Power-Frequency Response of Input and Driver Stages

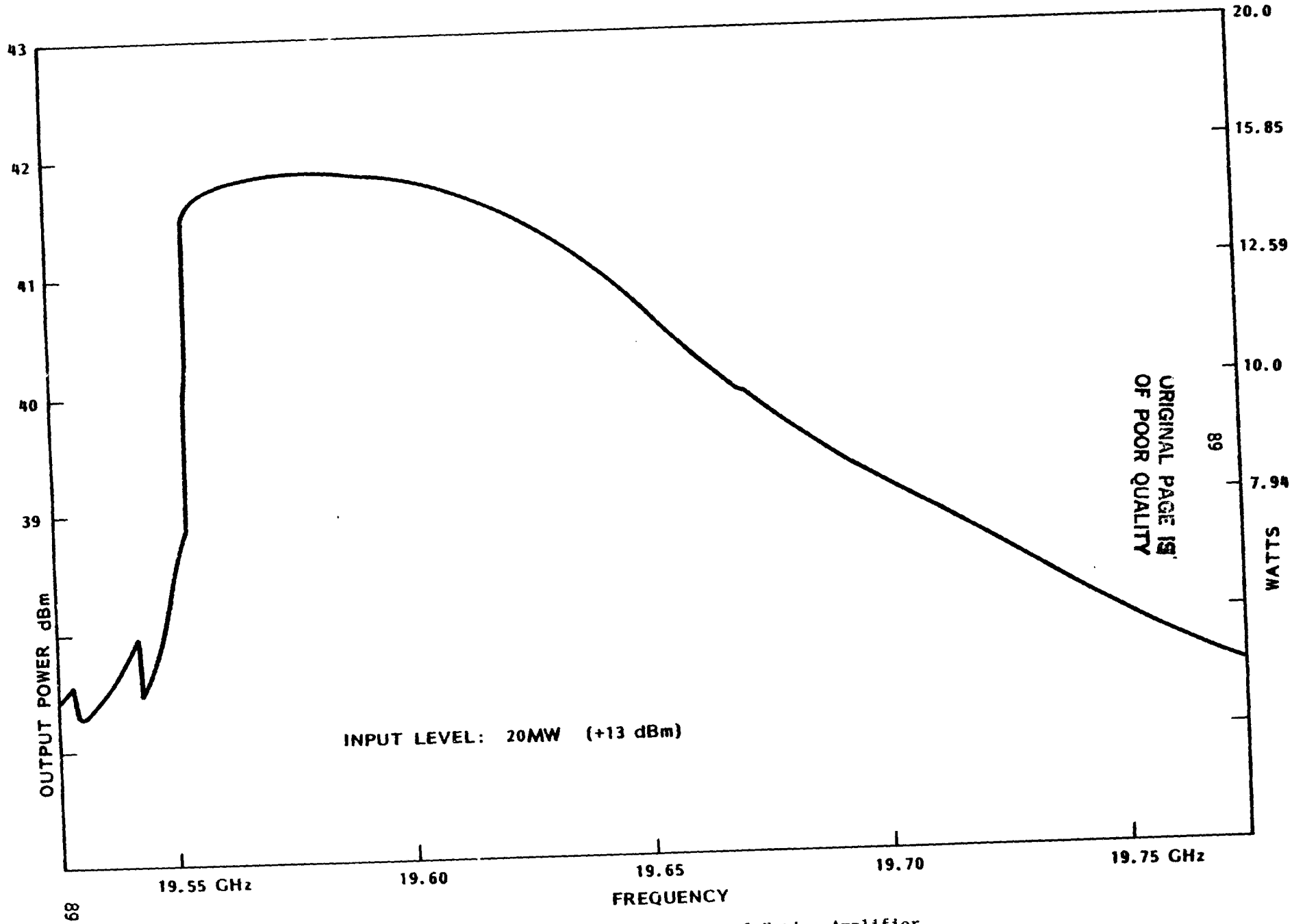


Figure 7-7. Power Frequency Response of Entire Amplifier

7.6.5 Gain Slope

Gain slope is defined as the gain variation per MHz of bandwidth. The maximum gain slope of the amplifier occurs at the lower band edge, as seen from Figure 7-7. The gain slope is found to be:

Gain Slope = 0.038 dB per MHz max.

7.6.6 Phase Linearity

Phase linearity is defined as the deviation of the measured phase response versus frequency from a reference linear phase response (a straight line). The reference line is drawn such that it provides the best least-square fit to the measured curve. Phase linearity is usually expressed as the peak-to-peak (P-P) deviation. Figure 7-8 shows the measured phase response of the amplifier. Notice a peculiarity of the phase response which is a characteristic of all injection locking oscillators. The slope of the response curve changes sign at around 19.598 GHz, the resonant frequency of the combiner cavity in the amplifier. This is due to the fact that for an injection-locking oscillator, the input-output phase relationship is, for a first order approximation, governed by [13]

$$\Delta\Phi = \sin^{-1} \frac{\omega_o - \omega_i}{\Delta\omega} \qquad (7\text{-}1)$$

where $\Delta\omega$ = input-output phase differential,

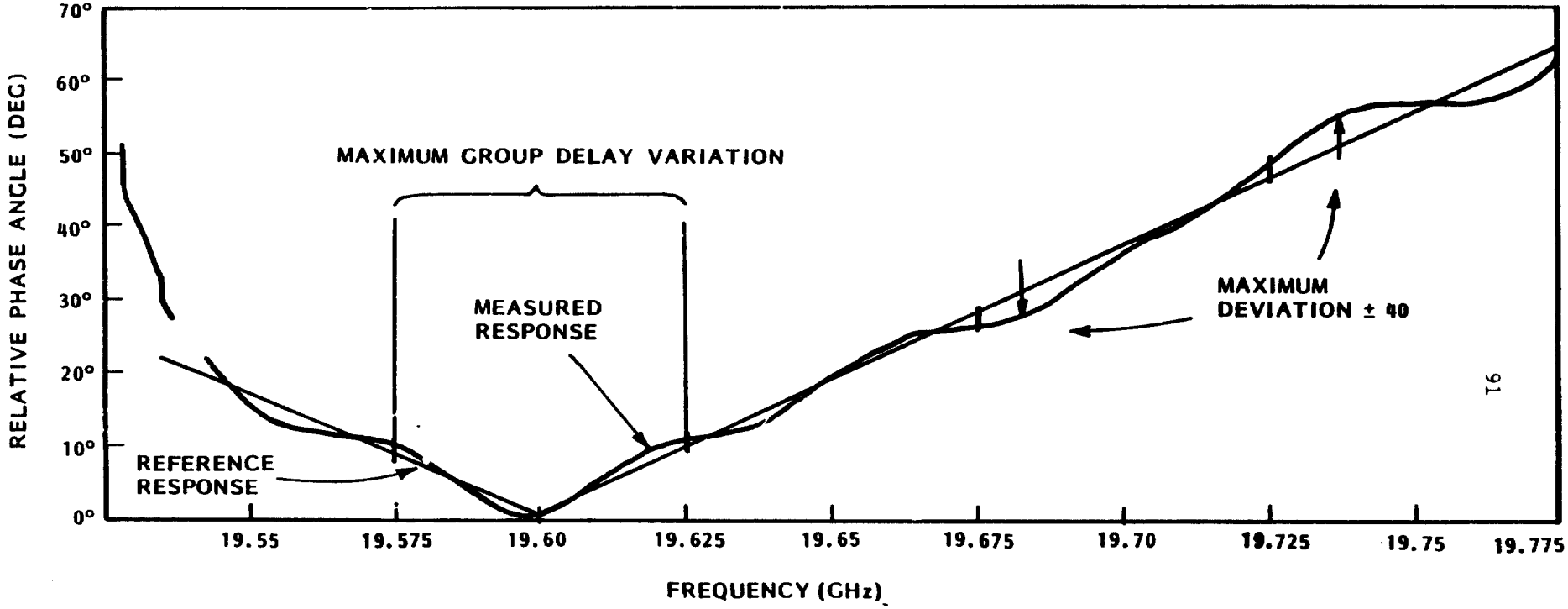
ω_o = resonant frequency of oscillator,

ω_i = injection frequency,

$\Delta\omega$ = injection-locking bandwidth.

The oscillator output leads the input in phase for any injection frequencies below ω_o; the output lags the input in phase for any injection frequencies above ω_o. When this phase characteristic is superimposed on that of the all-pass networks (interconnecting waveguides) and that of the circulators, the result is the response shown in Figure 7-8. The maximum peak-to-peak deviation can be found from the figure to be:

Phase Linearity = 8° P-P max.



Fiugre 7-8. Phase Response of Amplifier at Full Output

7.6.7 Group Delay Variation

Group delay, which has the dimension of time, is defined as:

$$t_d = \frac{d\phi \text{ (in rad)}}{d\omega} = \frac{1}{360^\circ} \frac{d\phi \text{ (in deg)}}{df} \simeq \frac{1}{360^\circ} \frac{\Delta\phi \text{(in deg)}}{\Delta f} \qquad (7\text{-}2)$$

where $\Delta\phi$ = phase variation within Δf,

Δf = a small frequency band within the passband of the amplifier.

Group delay variation is the difference of the maximum group delay and the minimum group delay within a 50-MHz frequency band.

$$\Delta t_d = t_d \text{ (max)} - t_d \text{ (min)}$$

The group delay information of the amplifier can be extracted from Figure 7-8. By dividing the amplifier passband into four 50-MHz segments, namely, from 19.575 GHz to 19.625 GHz, from 19.625 GHz to 19.675 GHz, from 19.675 GHz to 19.725 GHz, and from 19.725 GHz to 19.775 GHz, one can observe the following results:

Group Delays	Frequency	Group Delay Variation
$t_d(max)_1 = 6\times10^{-7}$ sec	19.6125 GHz	$\Delta t_d = 11.5 \times 10^{-7}$ sec per 50 MHz
$t_d(min)_1 = -5.5\times10^{-7}$ sec	19.5875 GHz	
$t_d(max)_2 = 5.24\times10^{-7}$ sec	19.65 GHz	$\Delta t_d = 5.24 \times 10^{-7}$ sec per 50 MHz
$t_d(min)_2 = 0$ sec	19.675 GHz	
$t_d(max)_3 = 6.12\times10^{-7}$ sec	19.725 GHz	$\Delta t_d = 6.12\times10^{-7}$ sec per 50 MHz
$t_d(min)_3 = 0$ sec	19.675 GHz	
$t_d(max)_4 = 6.12\times10^{-7}$ sec	19.725 GHz	$\Delta t_d = 6.12\times10^{-7}$ sec per 50 MHz
$t_d(min)_4 = 0$ sec	10.75 GHz	

It is readily seen that the maximum group delay variation is:

Group Delay Variation = 11.5×10^{-7} sec per 50 MHz

7.6.8 Harmonic and Spurious Responses

A spectrum analyzer was used to scan the output spectrum of the amplifier from 8.5 GHz to 22 GHz. There appeared to be no spectral components, harmonic or spurious, at 60 dB below the output level.

Harmonic and Spurious Responses = better than -60 dBc

7.6.9 AM-to-PM Conversion

AM-to-PM conversion is the process of the input-output phase differential being affected by the change in input level. It is one measure of amplifier linearity. The AM-to-PM conversion characteristic of the amplifier is measured at five frequencies within the passband of the amplifier. The frequencies are 19.555 GHz, 19.60 GHz, 19.64 GHz, 19.68 GHz and 19.725 GHz. The power level of the input to the amplifier was varied from +4 dBm to +16 dBm with 13 dBm being the normal input. The measurement results are presented in Figure 7-9. It is readily seen that the maximum AM-to-PM conversion occurred near the upper band edge at all input levels from +4 dBm to +16 dBm. The maximum conversion ratio is found to be:

AM-to-PM conversion = 2.7° per dB of input, max.

7.6.10 Overdrive Capacity and Dynamic Range of Input Drive

The amplifier was tested with an input range of +5 dBm to 16 dBm (a 3-dB overdrive) and there were no apparent degradations in amplifier performance. Testing at a higher input level was not performed due to the lack of a high power signal source.

Overdrive Capability = better than 3 dB
Dynamic Range = better than 11 dB

7.6.11 Noise Performance

The noise power at the output of the amplifier was measured as dBc (noise power in dB below carrier). The noise output was measured through a 1-Hz window and for a single-sideband bandwidth of 10 MHz. The resulting data is the noise power spectral density, as shown in Figures 7-10 and 7-11. Figure 7-10 shows the spectral density plot for PM noise (noise which appears as

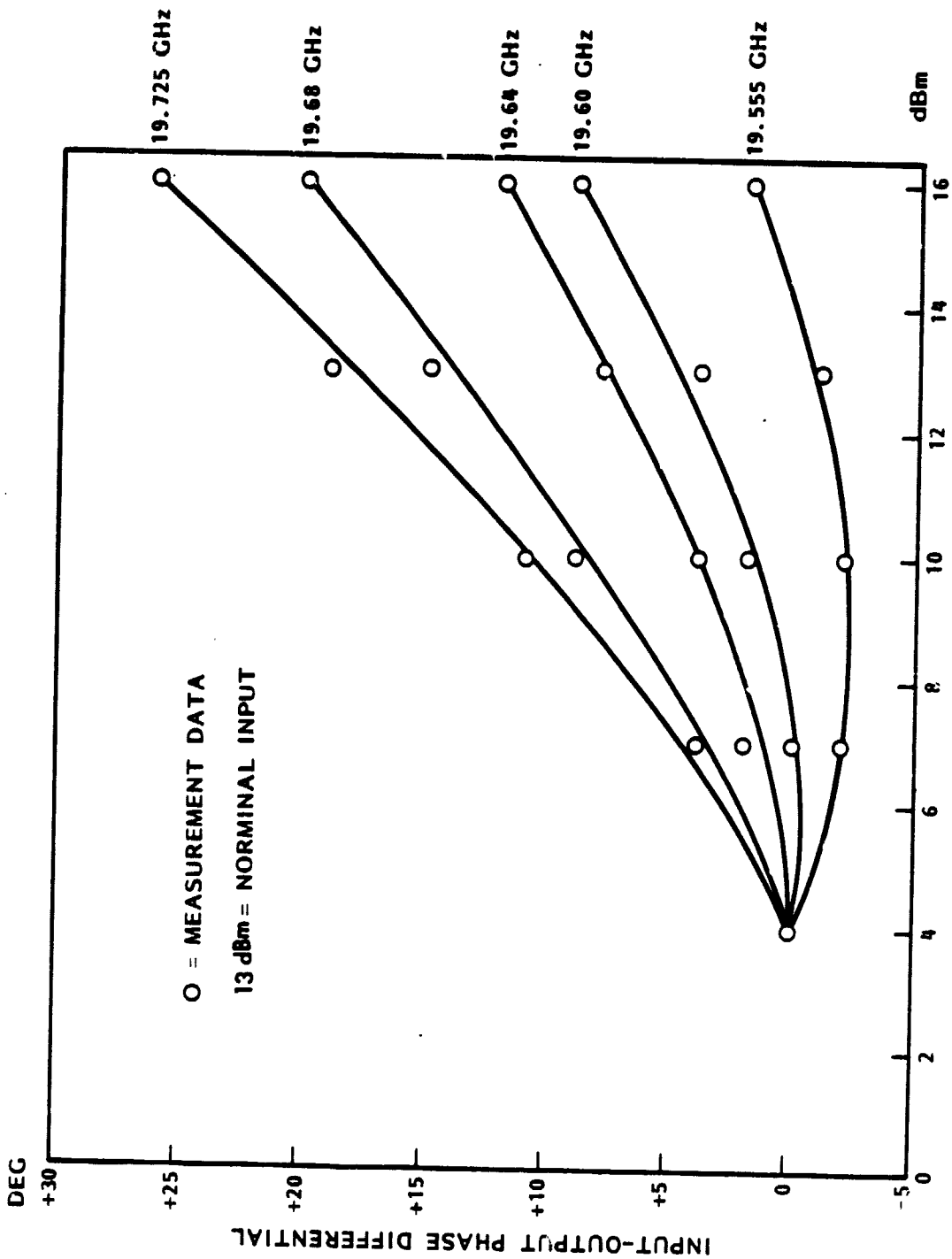


Figure 7-9. AM-to-PM Conversion Characteristic

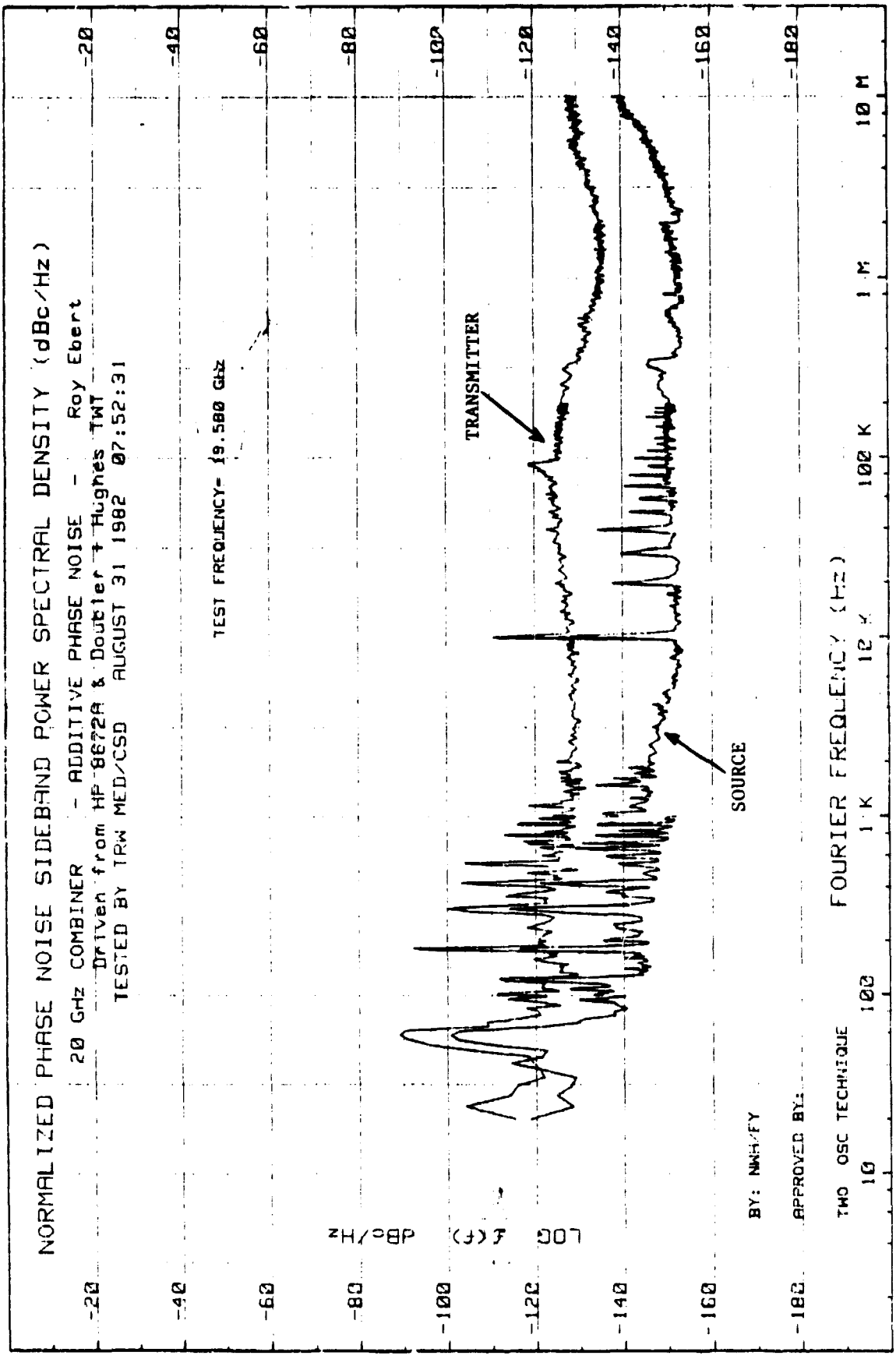


Figure 7-10. Phase Noise Performance of Amplifier

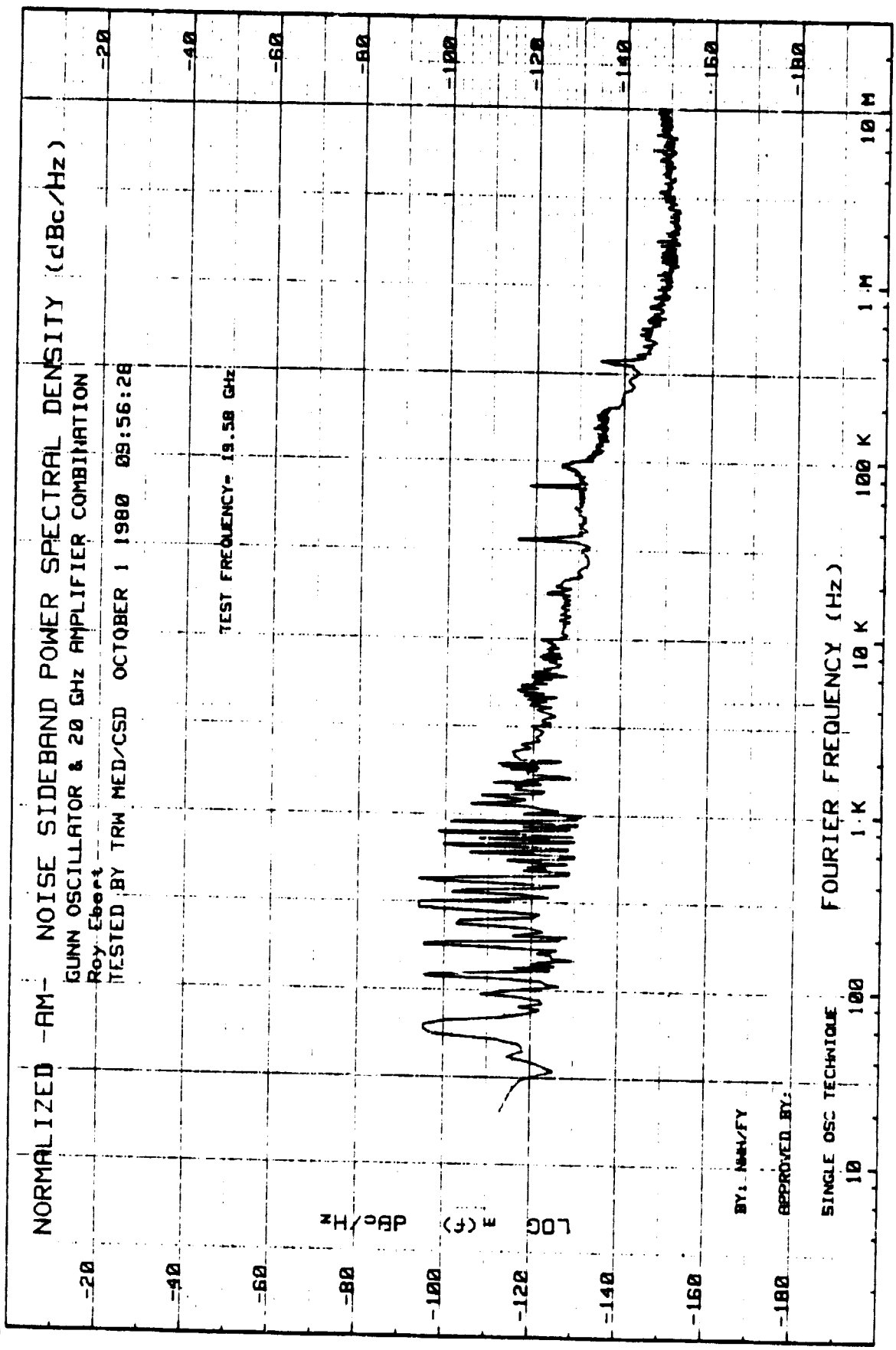


Figure 7-11. AM Noise Performance of Amplifier

phase fluctuation of the carrier). Figure 7-11 shows the spectral density plot for AM noise (noise which appears as amplitude fluctuations of the carrier). Noise performance in terms of AM and PM spectral density is used exclusively to characterize oscillators of which the present amplifier is one.

It can be seen from the figures that both AM and PM noise, measured at 1-kHz away from the carrier, is some -120 dB/Hz below the carrier.

AM Noise ≤ -120 dBc/Hz (1 kHz away from carrier)

PM Noise ≤ -120 dBc/Hz (1 kHz away from carrier)

7.6.12 DC-to-RF Conversion Efficiency

The DC-to-RF conversion efficiency of the amplifier, excluding the bias regulators, can be found from the equation:

$$\eta_o = \frac{100\ (P_o - P_i)}{I_{d1}V_{d1} + I_{d2}V_{d2} + \ldots + I_{d14}V_{d14}} \qquad (7\text{-}5)$$

where P_o = RF output power,

P_i = RF input power,

I_d = IMPATT diode current,

V_d = IMPATT diode voltage.

The overall DC-to-RF conversion efficiency of the amplifier, including the bias regulators, can be found from the equation:

$$\eta_T = \frac{100\ (P_o - P_i)}{I_1V_1 + I_2V_2} \qquad (7\text{-}6)$$

where I_1 = DC supply current, input and output stages,

V_1 = DC supply voltage, input and output stages,

I_2 = DC supply current, driver stage,

V_2 = DC supply voltage, driver stage.

The following data were obtained at band center:

P_i = 0.02 W	I_{d3} = 0.279 A	V_{d3} = 26.3 V
P_o = 15.49 W	I_{d4} = 0.318 A	V_{d4} = 26.8 V
I_1 = 3.61 A	I_{d5} = 0.296 A	V_{d5} = 25.5 V
V_1 = 32 V	I_{d6} = 0.281 A	V_{d6} = 27.7 V
I_2 = 0.504 A	I_{d7} = 0.318 A	V_{d7} = 26.6 V
V_2 = 60 V	I_{d8} = 0.323 A	V_{d8} = 27.3 V
I_{d1}= 0.217 A	I_{d9} = 0.339 A	V_{d9} = 26.8 V
V_{d1}= 26.1 V	I_{d10}= 0.266 A	V_{d10}= 27.6 V
I_{d2}= 0.503 A	I_{d11}= 0.270 A	V_{d11}= 26.6 V
V_{d2}= 54.6 V	I_{d12}= 0.273 A	V_{d12}= 26.8 V
	I_{d13}= 0.300 A	V_{d13}= 26.8 V
	I_{d14}= 0.329 A	V_{d14}=28.3 V

Upon calculations, the DC-to-RF conversion efficiencies are:

η_o = 11.9% (excluding bias regulators)

η_T = 10.6% (including bias regulators)

7.6.13 Input and Output SWR

The SWR (Standing Wave Ratio) of the amplifier was measured at both the input port and the output port. The results are:

Input SWR = 1.5 max.

Output SWR = 1.33 max.

7.6.14 Thermal Cycling

The amplifier was subjected to temperature variations during an operational test. The temperature was varied from 0°C to 50°C in 12 steps with 25.4°C being normal operating temperature. The temperature reading was obtained at the baseplate of the amplifier housing. Three sets of measurements were performed; namely, output power versus temperature, operating frequencies versus temperature, and power gain versus temperature.

Figures 7-12 and 7-13 depict the output power and gain characteristics of the amplifier as a function of temperature. It is readily seen that the output power, as well as the power gain, decreases as the ambient temperature elevates.

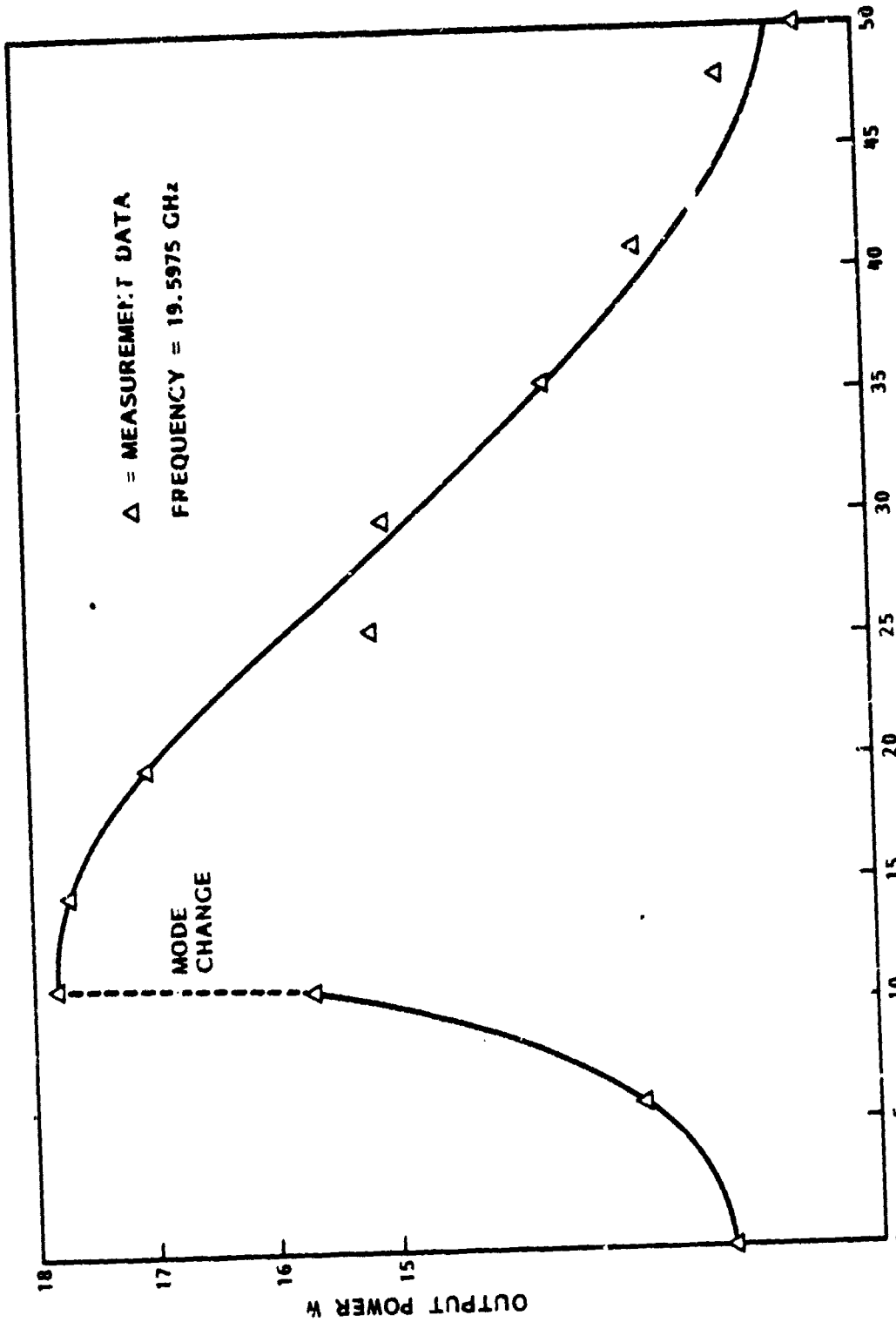


Figure 7-12. Amplifier Output Power Versus Temperature

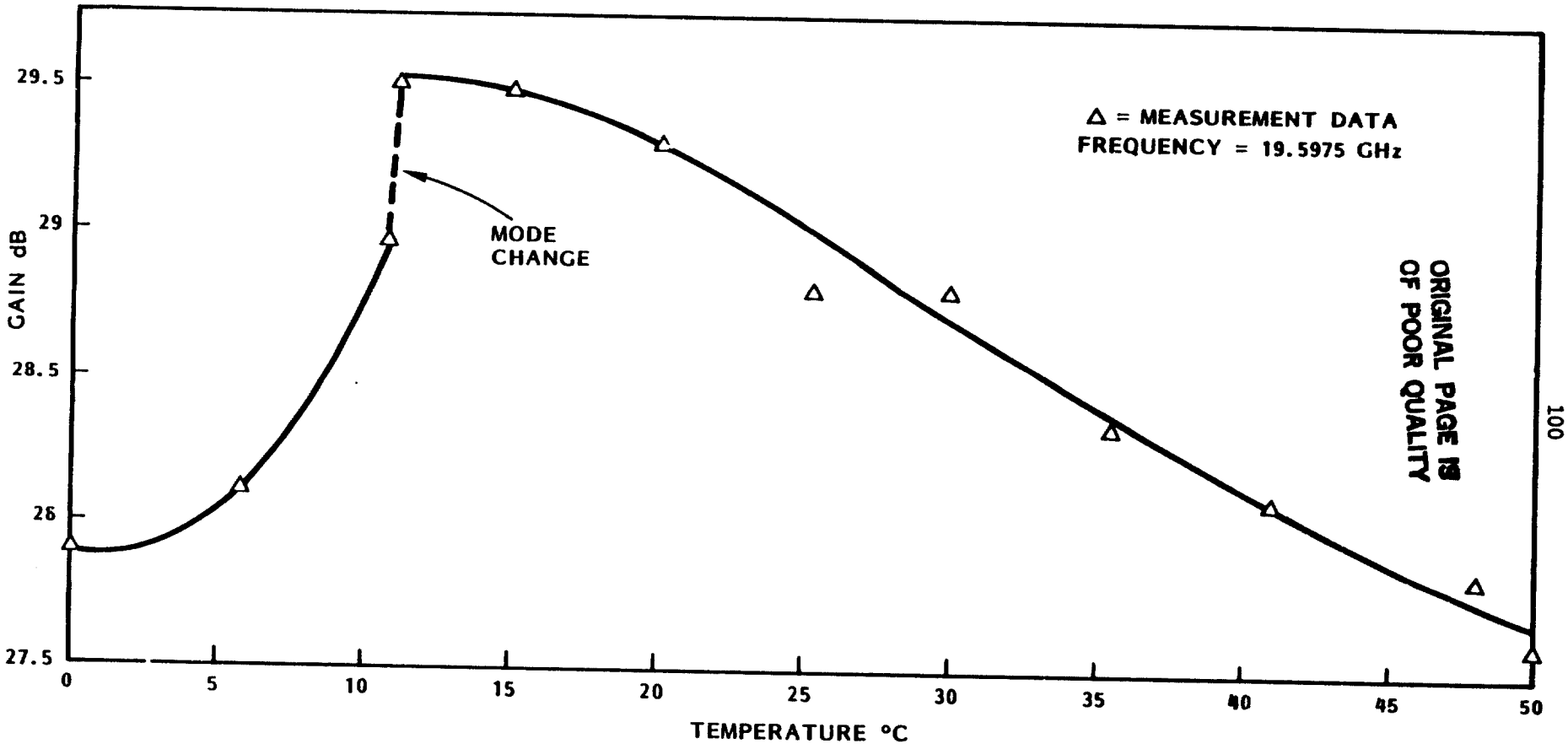


Figure 7-13. Amplifier Gain Versus Temperature

This is a consequence of constant voltage biasing, as mentioned in Section 3. The bias current of the IMPATT diodes decreases with temperature. The benefit of this scheme is that the amplifier is immune from catastrophic failure due to overheating. On the other hand, the amplifier output, as well as power gain, is expected to rise with decreasing temperature due to the increase in bias current with decreasing temperature. However, the IMPATT diodes switched to another mode (an undesirable one) at lower temperatures, as is evident from the figures. Operating at temperatures below 12°C is to be avoided.

Figure 7-14 shows the drift characteristic of the amplifier's operating frequencies. It is remarkable that the operating frequencies drifted little with temperature. In fact, maximum drift occurred at the lower band edge and the drift was only 60 MHz over the temperature range of 0°C to 50°C. This stability is perhaps attributed to the high Q power combining cavity in the final stage of the amplifier.

7.6.15 Summary of Test Results

For the purpose of comparing the program objectives with the performance achieved, the test results together with the technical requirements of the amplifier are listed in Table 7-2.

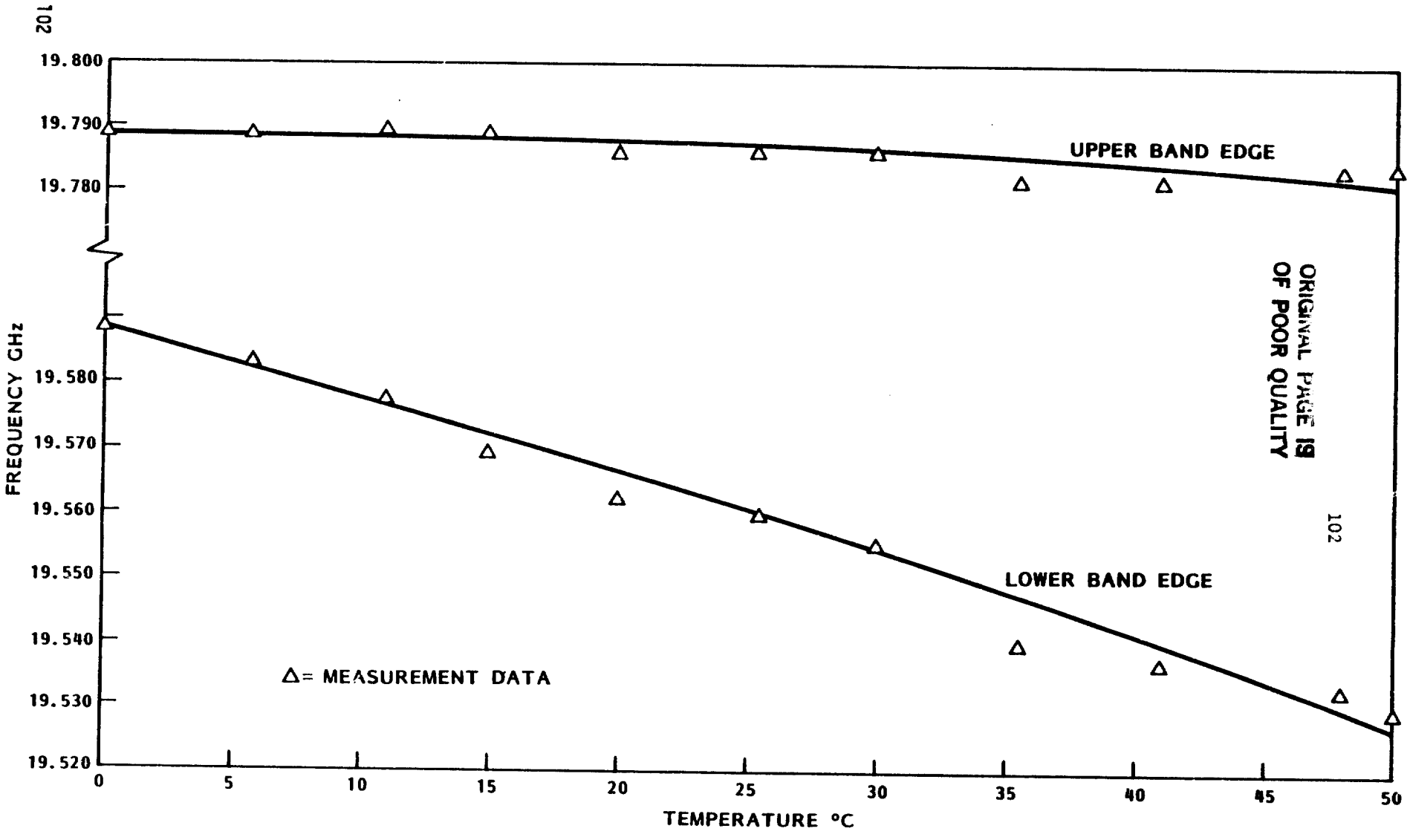


Figure 7-14. Amplifier Operating Frequencies Versus Temperature

TABLE 7-2. COMPARISON OF PROGRAM OBJECTIVE AND PERFORMANCE ACHIEVED

Item	Objective	Achieved
RF Output Power	20 W min.	15.49 W max., 5.75 W min.
Operating Frequencies	19.7 to 20.2 GHz	19.555 to 19.775 GHz
RF Power Gain	30 ±1 dB min.	28.9 dB max., 24.6 dB min.
Gain Variation	±1 dB max.	±2.2 dB max.
Gain Slope	0.15 dB/Hz max.	0.038 dB/Hz max.
Phase Linearity	10° P-P max.	8° P-P max.
Group Delay Variation	0.5 nsec/50 MHz max.	1.15 nsec/50 MHz max.
Harmonic Response	-50 dBc min.	Better than -60 dBc
Spurious Response	-60 dBc min.	Better than -60 dBc
AM-to-PM Conversion	5 ±1° dB max.	2.7°/dB max.
DC-to-RF Conversion Efficiency	20% min.	10.6% (11.9%)*
Overdrive Capacity	+5 dB	Better than +3 dB
Input and Output SWR	1.3 max.	1.15 input; 1.33 output

*Excluding bias circuits

8.0 CONCLUSIONS AND RECOMMENDATIONS

The completion of the 20-GHz IMPATT transmitter program has resulted in the development of a three-stage IMPATT amplifier capable of 15 W of CW output and a 2-dB bandwidth of 117 MHz. The amplifier has met or exceeded some performance objectives, such as gain slope, phase linearity, harmonic and spurious responses, AM-to-PM conversion, and noise performance. On the other hand, the amplifier falls short of meeting the major goals, namely, failing to achieve the required 20 W CW output power and the operating bandwidth of 500 MHz. In the following paragraphs, the major technologies required for the engineering of IMPATT amplifiers will be identified. The degree of maturity of these technologies will be examined and, if deficiencies exist, recommendations for future actions will be provided.

The IMPATT amplifier developed in this program can be accurately linked to five technological disciplines. The performance of the amplifier as a whole is intimately related to the maturity of the devices or components resulting from these disciplines. The disciplines can be identified as (a) IMPATT device technology, (b) single-diode circuit technology, (c) multitdiode circuit technology, (d) bias circuit technology, and (e) circulator technology. As discussed in Section 5 and shown in Section 7.6, the single-diode circuit technology, the bias circuit technology, and the circulator technology are mature and readily available. The performance of the hardware resulting from these technologies has met or exceeded the specifications and requirements of this program. It is concluded that no further work on these discplines is needed. On the other hand, the IMPATT device technology and multidiode circuit technology require further development.

8.1 IMPATT DEVICE TECHNOLOGY ASSESSMENT

As mentioned in Appendix D, up to 4.5 W per diode can be expected from the GaAs diode technology developed for this program. However, yield factor for such high performance devices remains a problem. It is not expected that any performance breakthrough for 20-GHz IMPATT diodes will take place in the near future. This statement is based on the fact that state-of-the-art technologies such as the use of GaAs material, diamond heat sink, double-drift

structure, and double-Read profile have already been incorporated in the development in this program. It seems, therefore, that technological improvement in the near future will be mainly on production refinement. It is recommended that further work be supported on the refinement of production techniques of the 4.5-W diodes developed in this program. The refinement is necessary not only for improving the yield factor for the manufacturing of high-performance diodes, but also for improving the dispersion of electrical characteristics from device-to-device. As is shown in Appendix C, device uniformity is an important factor in obtaining good performance in a combiner circuit such as the output stage of the subject amplifier.

It is not recommended that future work be focused on multimesa devices or any other multichip technologies. Although the multimesa/multichip devices have the potential of providing high output power, it remains to be demonstrated that such devices can be used in wideband, high-frequency (above 10 GHz) circuits. It is believed that the parasitics associated with the large package of these devices are not compatible with the present 20-GHz circuits.

8.2 MULTIDIODE CIRCUIT TECHNOLOGY ASSESSMENT

The test results presented in Section 7.6 have shown that the rectangular waveguide cavity combiner used as the output stage of the amplifier fails to meet the output power and bandwidth requirements of this program. It is believed, however, that output power is not a difficulty and can be accomplished either by increasing the number of Varian IMPATT diodes in the output stage or by refitting the present circuit with the higher power Raytheon devices developed for the program. The main deficiency is due partly to the nonuniformity of the IMPATT devices used and partly to the output stage of the amplifier. The output stage utilizes a single-tuned high Q cavity combiner circuit which is inherently narrow-band.

It was first believed that by lowering the Q of the cavity, the output stage could accommodate a 2.5% bandwidth and a 2-dB power variation (conditions which meet the requirements of the program). However, the unexpected diode nonuniformity demanded a high Q circuit in order to achieve power combining. The solution to the bandwidth deficiency appears to be a tighter control on diode dispersion on the one hand and using the higher power IMPATT diodes on the other. With the higher power devices, fewer diodes are needed

to provide a 20-W output. For example, if 4- to 6-W diodes were used, it would be necessary to combine only four devices at the output stage to satisfy the power requirement. With four devices, not only the problem of diode matching is eased, it is also possible to fine-tune each diode module such that the collective results (i.e., four diodes as a whole) are optimal. It should be noted that the tuning of one diode module in a combiner circuit affects the tuning of all remaining diodes in the same circuit. Consequently, optimization of a circuit which combines a large number of active devices (12 diodes in our case) was proven to be a formidable task. It is concluded that a rectangular waveguide cavity combiner using four high-power (4 to 6 W) IMPATT diodes is capable of meeting the program objectives.

APPENDIX A. THEORY OF WIDEBAND MULTITUNED CIRCUITS

The bandwidth of a tuned circuit is characterized by the rate of change of the circuit susceptance, B (or reactance, X), with the operating frequency, ω. In other words, the bandwidth is a function of the parameter $\partial B/\partial\omega$. A smaller value of $\partial B/\partial\omega$ implies a larger bandwidth. Since $\partial B/\partial\omega$ is related to the Q of the circuit, it can be said that a smaller circuit Q implies a larger operational bandwidth. For a single-tuned circuit, however, the circuit Q can not be lower without limit since some selectivity (frequency determination) must be maintained. The optimum solution in a single-tuned circuit is always a compromise between bandwidth and output power. Consequently, output power always drops at band edged in a single-tuned circuit. In the following paragraphs, it is shown that a multituned circuit, such as the double-tuned circuit used in the analysis, possesses a smaller $\partial B/\partial\omega$ as compared to the single-tuned circuit even if the individual Q's in the former circuit are high.

A single RLC parallel circuit, as indicated in Figure A-1, derives the following:

$$Y_1(\omega) = \frac{1}{j\omega L_1} + j\omega C_1 + \frac{1}{R_1} = j\left(\omega C_1 - \frac{1}{\omega L_1}\right) + \frac{1}{R_1} = jB + G \qquad \text{(A-1)}$$

The rate of change of susceptance with frequency is found to be

$$\frac{\partial B}{\partial \omega} = C_1 + \frac{1}{\omega^2 L_1} = \frac{Q_1}{\omega R_1} + \frac{Q_1}{\omega R_1} = \frac{2Q_1}{\omega R_1} \qquad \text{(A-2)}$$

where

$$Q_1 = \omega C_1 R_1 = \frac{R_1}{\omega L_1} \qquad \text{(A-3)}$$

Now, suppose a second resonator is added across the circuit as shown in Figure A-2, with the stipulation that its resonant frequency is the same as that of the first resonator. $Y_{IN}(\omega)$ then becomes

$$Y_{IN}(\omega) = j\left(\omega C_1 - \frac{1}{\omega L_1}\right) + \frac{1}{R_1} + \frac{1}{R_2 + j\omega L_2 + \frac{1}{j\omega C_2}} \tag{A-4}$$

$$= j\left(\omega C_1 - \frac{1}{\omega L_1}\right) + \frac{1}{R_1} + \frac{R_2 - j\left(\omega L_2 - \frac{1}{\omega C_2}\right)}{R_2^2 + \left(\omega L_2 - \frac{1}{\omega C_2}\right)^2}$$

Since

$$Y_{IN}(\omega) = G_{IN} + jB_{IN} \tag{A-5}$$

we have

$$jB_{IN} = j\left(\omega C_1 - \frac{1}{\omega L_1}\right) - j\frac{\omega L_2 - \frac{1}{\omega C_2}}{R_2^2 + \left(\omega L_2 - \frac{1}{\omega C_2}\right)^2} \tag{A-6}$$

Differentiating with respect to ,

$$\frac{\partial B_{IN}}{\partial \omega} = \frac{2Q_1}{\omega R_1} - \frac{\left[R_2^2 + \left(\omega L_2 - \frac{1}{\omega C_2}\right)^2\right]\left(L_2 + \frac{1}{\omega^2 C_2}\right) - \left(\omega L_2 - \frac{1}{\omega C_2}\right)\left(2\omega L_2^2 - \frac{2}{\omega^3 C_2^2}\right)}{\left[R_2^2 + \left(\omega L_2 - \frac{1}{\omega C_2}\right)^2\right]^2} \tag{A-7}$$

The first term was determined earlier for the case of the single-tuned circuit. In the second term, we substitute for L_2 and C_2 from the relation

$$Q_2 = \frac{\omega L_2}{R_2} = \frac{1}{\omega C_2 R_2} \tag{A-8}$$

Then,

$$\frac{B_{IN}}{\partial \omega} = \frac{2Q_1}{\omega R_1} - \frac{R_2^2\left(\frac{Q_2 R_2}{\omega} + \frac{Q_2 R_2}{\omega}\right) - 2\left(Q_2 R_2 - Q_2 R_2\right)\left(\omega L_2^2 - \frac{1}{\omega^3 C_2^2}\right)}{\left[R_2^2 + \left(Q_2 R_2 - Q_2 R_2\right)^2\right]^2} \tag{A-9}$$

The second term simplifies by inspection so that

$$\frac{\partial B_{IN}}{\partial \omega} = \frac{2Q_1}{\omega R_1} - \frac{2Q_2}{\omega R_2} \tag{A-10}$$

or

$$\frac{\partial B_{IN}}{\partial \omega} = \frac{2}{\omega}\left[\frac{Q_1}{R_1} - \frac{Q_2}{R_2}\right] = \frac{2Q_{equiv.}}{\omega R_{equiv.}} \qquad \text{(A-11)}$$

The significant conclusion, which is evident from this last equation, is that the rate of change of susceptance B with frequency, at least in the vicinity of the resonant frequency, is less for the combination of two circuits than for either circuit separately. This indicates a mutual susceptance compensation and broadbanding action. Allowing qualitatively the possibility of $R_1 = R_2$, we obtain a net $Q_{equiv.}$ of the combination circuit, which is the difference between the two individual Q's, a difference which could be small.

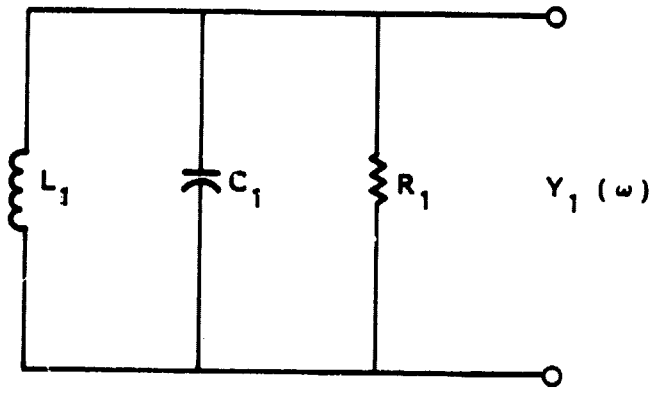


Figure A-1. Equivalent Circuit for a Single Resonator Circuit

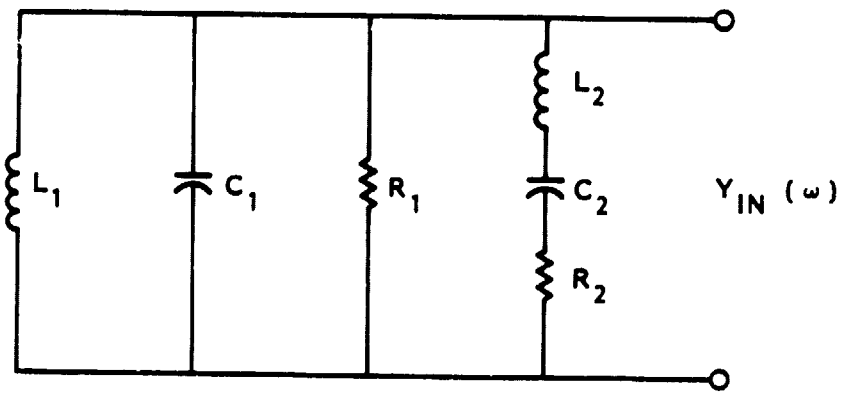


Figure A-2. Equivalent Circuit of a Dual Resonator Circuit

APPENDIX B. THEORY OF CONSTANT-VOLTAGE BIASING

Breakdown Voltage as a Function of Temperature

For any reverse-biased semiconductor junctions, Si and GaAs included, the decreased ionization rate at high temperature gives rise to a positive temperature coefficient of breakdown voltage. A good approximation of the breakdown voltage-tempeature relationship was given as [14,15]:

$$V_b = V_{bo} (1 + \beta(T_j - T_o)) \tag{B-1}$$

where V_b is the device breakdown voltage at a junction temperature of T_j, V_{bo} is the same at a reference junction temperature of T_o, and β is the normlized temperature coefficient defined by

$$\beta = \frac{1}{V_{bo}} \frac{dV_b}{dT_j} \tag{B-2}$$

Notice that the rise of the junction temperature, T_j, is caused by external heating (due to rise of the ambient temperature) and internal heating (due to power dissipation in the diode). Consider first the effect of external heating. Equation (B-1) can be rewritten as:

$$V_b = V_{bo} + \Delta V_b \quad ; \quad \Delta V_b = \beta V_{bo} \Delta T \tag{B-3}$$

where $\Delta T = T - T_o$ is the relative ambient temperature in reference to T_o and T is the ambient temperature. Equation (B-3) states that a change in the ambient temperature in reference to T_o introduces a change in diode breakdown voltage, ΔV_b, in reference to V_{bo}. We shall say that ΔV_b is caused by external heating.

When avalanche breakdown occurs, bias current flows through the device junction. In the case of an IMPATT diode, only a small fraction of the bias power is converted to the RF. The remaining bias power is dissipated at the junction as heat, and as a result, T_j rises. This process causes the voltage across the diode to increase above V_b in a fashion identical to external heating. We shall express the increase in diode voltage in analog to Eq. (B-3) and with the aid of a well-known heat equation:

$$\Delta V_{d1} = \beta V_{bo}\, \theta_t\, (V_d I_d + P_i - P_o) \tag{B-4}$$

where ΔV_{d1} is the increase in diode voltage above V_b due to the internal heating, θ_t is the thermal resistance from the diode junction to the ambience, V_d and I_d are the bias voltage and current, respectively, of the diode, P_1 is the RF injection power, and P_o is the RF output power. Also, during avalanche breakdowns, the space charge of the carriers distorts the electric field profile in the space charge layer, giving rise to a positive electric resistance [16]. This so-called space-charge resistance produces a voltage drop across the diode in addition to ΔV_b and ΔV_{d1}. The voltage drop can be expressed as:

$$\Delta V_{d2} = R_{sc}\, I_d \tag{B-5}$$

where R_{sc} is the space-charge resistance of the diode and can be determined experimentally [14].

For the sake of closed-form solutions, we shall restrict ourselves to a first-order analysis in the next section by ignoring the terms involving P_i and P_o. (Notice that P_o is a function of I_d^2.) The error so introduced is acceptable since only a small fraction of the bias power is converted to P_o. ΔV_{d1} is now expressed as:

$$\Delta V_{d1} \approx \beta V_{bo}\, \theta_t\, V_d I_d \tag{B-6}$$

The total voltage across an IMPATT diode under avalanche conditions can be written as:

$$\begin{aligned} V_d &= V_{bo} + \Delta V_b + \Delta V_{d1} + \Delta V_{d2} \\ &= V_{bo} + R_{sc} I_d + \beta V_{bo}\, \theta_t\, V_d I_d + \beta V_{bo}\, \Delta T \end{aligned} \tag{B-7}$$

A plot of Eq. (B-7) is shown in Figure A-1.

Thermal Properties of C-I and C-V Biasings

With C-I biasing, $I_d = I_o$ = constant, and the diode voltage as a function of temperature, by rearranging Eq. (B-7), can be written as:

$$V_d = \frac{1}{1 - \beta\theta_t\, V_{bo} I_o} \left(R_{sc} I_o + V_{bo} + \beta V_{bo}\, \Delta T\right) = a_1 + b_1\, \Delta T \tag{B-8}$$

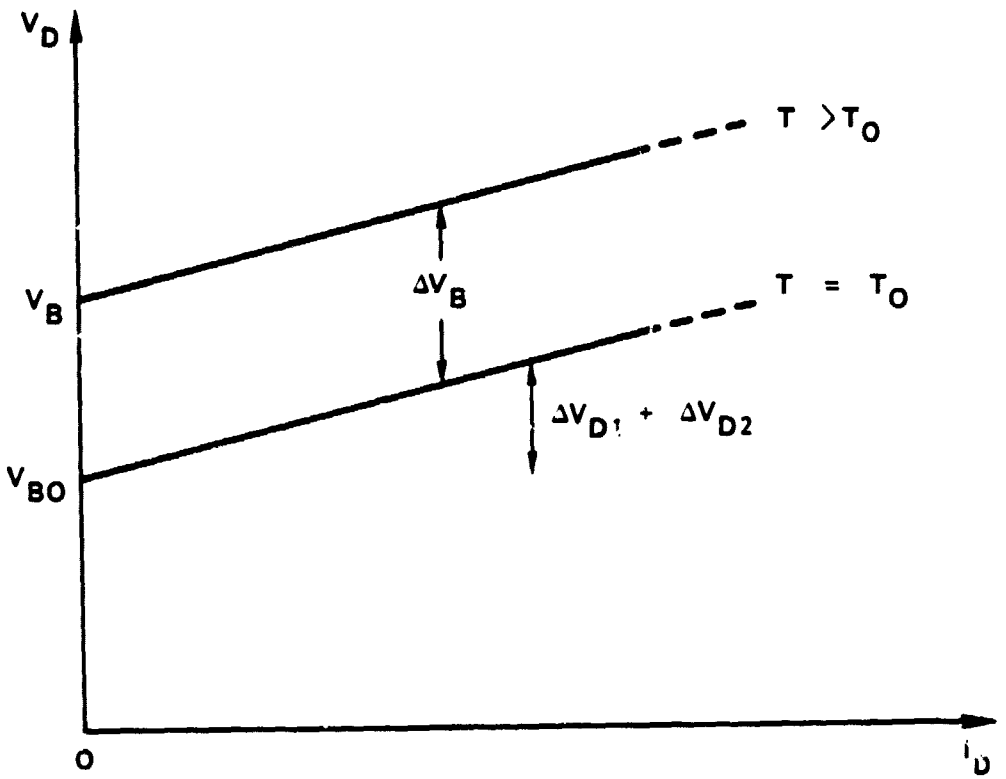


Figure B-1. Diode Breakdown Voltage Characteristic

The junction temperature of the diode is found to be:

$$T_j = \theta_t I_o V_d + T$$

$$= \theta_t I_o (a_1 + b_1 \Delta T) + \Delta T + T_o \qquad \text{(B-9)}$$

$$= a_2 + b_2 \Delta T$$

For practical cases, the parameters a_1, a_2, b_1, b_2 are found to be positive. It is readily seen that with C-I biasing, both diode voltage and junction temperature rise with any temperatures above T_o (i.e., for $\Delta T > 0$) and that there is a possibility of a thermal runaway due to internal heating if the condition $\beta\theta_t V_{bo} I_o = 1$ is met.

On the other hand, with C-V biasing, $V_d = V_o$ = constant, and the diode current and junction temperature can be shown to be

$$I_d = \frac{1}{R_{sc} + \beta\theta_t V_{bo} V_o} (V_o - V_{bo} - \beta V_{bo} \Delta T) \qquad \text{(B-10a)}$$

$$= c_1 - d_1 \Delta T \qquad \text{for } \Delta T \leq \Delta T_c \qquad \text{(B-10b)}$$

$$= 0 \qquad \text{for } \Delta T > \Delta T_c$$

$$T_j = \theta_t I_d V_o + T$$

$$= \theta_t V_o (c_1 - d_1 \Delta T) + \Delta T + T_o$$

$$= c_2 + d_2 \Delta T \qquad \text{for } \Delta T \leq \Delta T_c \qquad \text{(B-11a)}$$

$$= \Delta T \qquad \text{for } \Delta T > \Delta T_c \qquad \text{(B-11b)}$$

Again, the parameters c_1, c_2, d_1, d_2 are found to be positive for practical cases. A new parameter, T_c, which we shall call the cutoff temperature, is introduced here and is defined as

$$T_c - T_o = \Delta T_c = c_1/d_1 = \frac{V_o - V_{bo}}{\beta V_{bo}} \qquad \text{(B-12)}$$

Eq. (B-10) indicates that diode current decreases with elevating temperature. As the ambient temperature reaches T_c, the diode current goes to zero and remains zero for any temperatures above T_c. On the other hand, the junction temperature increases with ambient temperature at a rate d_2. As the ambient temperature goes above T_c, the rate changes to unity. I_d and T_j under C-V bias are plotted against temperatures and are shown in Figures -2 and -3.

Comparison of C-I and C-V Biasing

Although T_j increases with temperature when the diode has either C-I bias or C-V bias, T_j increases with temperature at a slower rate in the C-V case than in the C-I case, as can be seen from the following inequality.

$$b_2 = 1 + \frac{\beta\theta_t I_o V_{bo}}{1 - \beta\theta_t I_o V_{bo}} \quad > \quad d_2 = 1 - \frac{\beta\theta_t V_o V_{bo}}{R_{sc} + \beta\theta_t V_o V_{bo}} \qquad \text{(B-13)}$$

The slower rate is due to the fact that, with C-V biasing, internal heating decreases with elevating temperature. Take a commercial IMPATT diode, HP 5082-0400, for example. The diode parameters were given as follows [17]:

β	$= 1.17 \times 10^{-3}/°C$	V_{bo}	$= 76.1$ V
R_{sc}	$= 31$ ohms	V_d	$= 83.6$ V
θ_t	$= 16°C/W$	I_d	$= 0.05$ A

If this diode were employed, we would have $b_2 = 1.08$ and $d_2 = 0.21$. The diode junction temperature would increase with temperature at a rate of five times faster with a C-I bias than with a C-V bias. The price to pay for this thermal advantage is RF output. With C-V biasing, diode current decreases with temperature at the rate of d_1. Output power is proportional to the square of diode current or

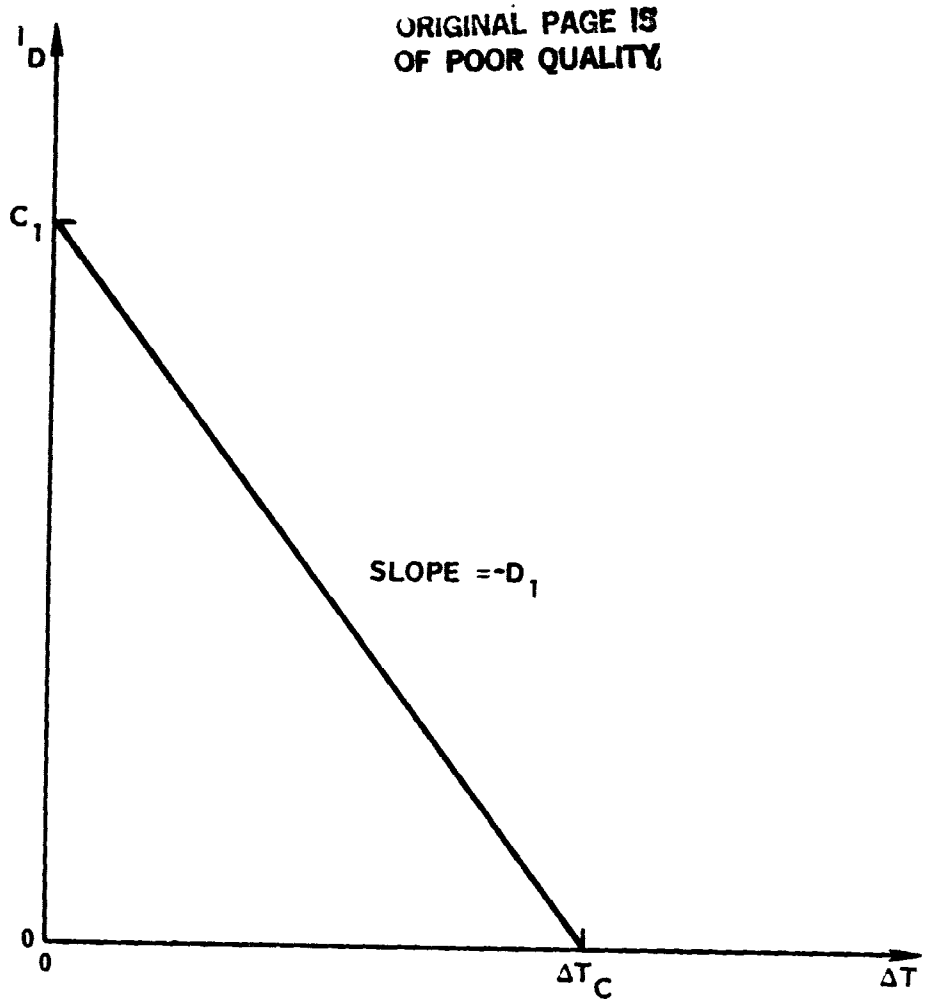


Figure B-2. Diode Current vs. Temperature, C-V Bias

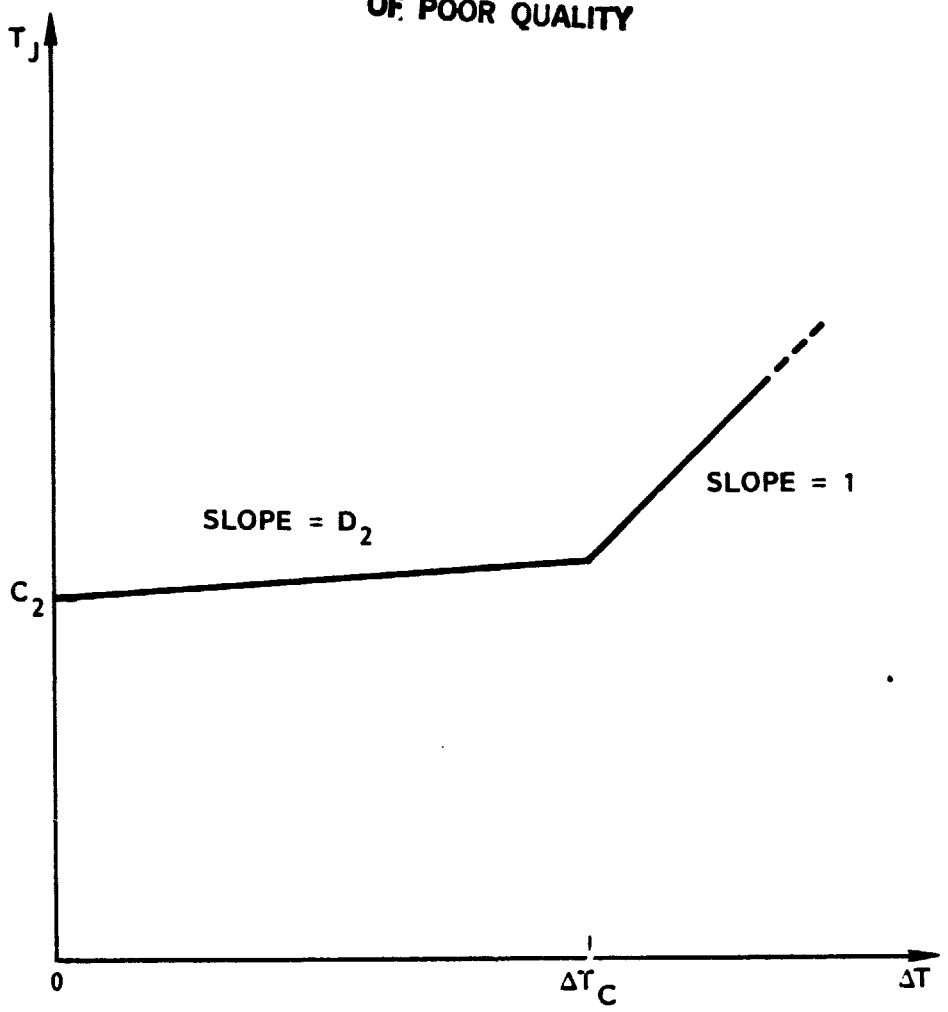


Figure B-3. Diode Junction Temperature vs. Temperature, C-V Bias

$$P_o = k(C_1^2 + d_1^2 \Delta T^2 - 2C_1 d_1 \Delta T) \qquad \text{(B-14)}$$

where k is the constant of proportionality. Output power decreases, therefore, at the rate of

$$\frac{\Delta P_o}{\Delta T} = 2d_1^2 \Delta T - 2C_1 d_1 \qquad \text{(B-15)}$$

APPENDIX C. EFFECTS OF DIODE NONUNIFORMITY

It is of importance to examine the effects of IMPATT diode parameter dispersion on the performance of the IMPATT amplifier, since it is the amplifier which largely determines the overall performance of the communications system. A review of these effects is presented in which it is assumed that the most significant IMPATT diode parameter variation is the maximum power available from the diode. Initially, it has been assumed that this variation in power results principally from variations in the diode area. It is shown that the locking bandwidth and center frequency, as well as the output power, are sensitive to these variations.

In the following paragraphs, a simple equivalent circuit model of a single-diode injection-locking oscillator is discussed. (This will suffice for the purpose of illustrating the effect of diode nonuniformity.) Power output variations due to diode chip area variations are calculated. For simplicity, it is assumed that the oscillator has been adjusted initially for optimum performance using an average diode and that no changes in the oscillator coupling system are made to accommodate diodes of different chip areas. The effects of diode area changes on power, frequency and bandwidths are then calculated. The results of the analysis have shown that the most significant influence of diode chip area variations is on the center frequency of the amplifier. To compensate for this, it will be necessary to individually tune each amplifier to the desired center frequency. The equivalent circuit of the injection-locked oscillator is shown in Figure C-1. Y_e is the electronic part of the diode chip admittance, C_d is the chip capacitance, C_c and L_c are the equivalent capacitance and inductance of the circuit referred to the chip plane, and R_s and G_L are the values of the bias stabilizing resistance and external load conductance referred to the chip plane. Typically, R_s, which is used to suppress subharmonic oscillations, and $1/G_c$, the equivalent circuit losses resistance, are small compared to $1/G_L$. The effect of both of these terms, R_s and G_L, will be neglected to simplify the analysis.

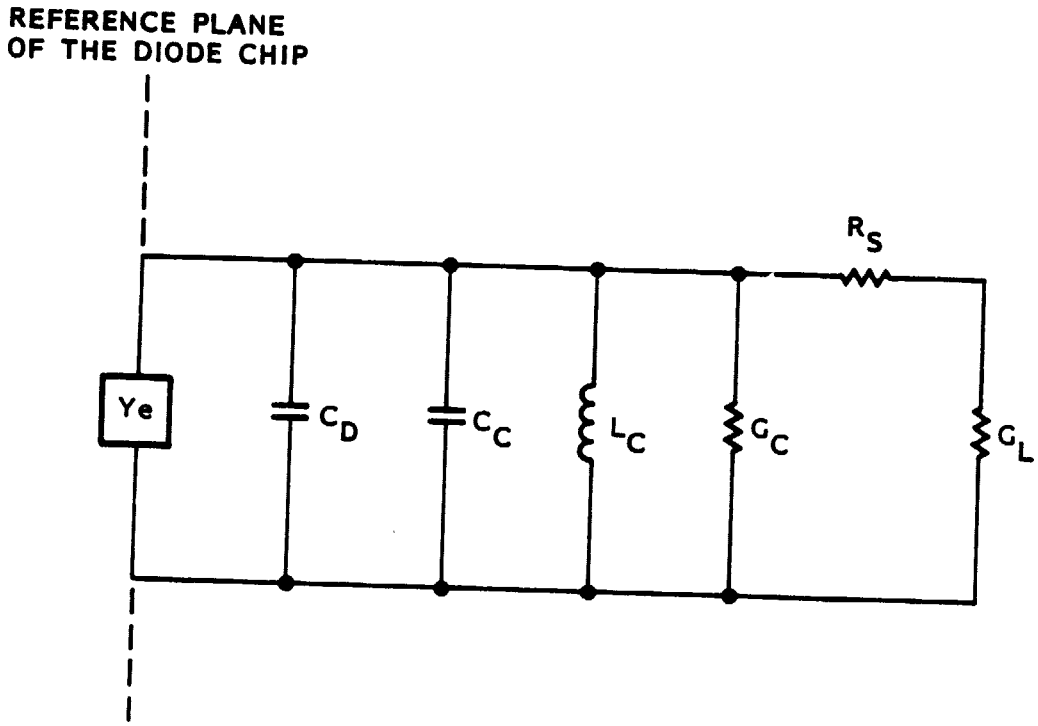


Figure C-1. Equivalent Circuit of the Injection Locked Amplifier

Power Output Variations

The power output of an injection-locked amplifier operating in the free-running oscillator mode is given by

$$P_o = 1/2 \; |-G_e| V_1^2 = 1/2 \; G_L \; V_1^2 \qquad \text{(C-1)}$$

where $-G_e$ is the negative electronic conductance of the diode chip and V_1 is the peak value of the AC chip voltage. For purposes of discussion, a diode with an optimum power of 2.5 W is assumed. It is further assumed that $(-)G_e = (-)20 \times 10^{-3}$ mhos and $V_1 = 15.8$ V under the conditions of optimum power output. It should be noted that the discussion which follows can be modified readily when the actual diode characteristics become available. Near the optimum power operating condition, G_e is assumed to vary as

$$G_e = G_s \left(1 - \frac{V_i^2}{V_m^2} \right) \qquad \text{(C-2)}$$

where G_s is an equivalent small signal electronic conductance and V_m is defined so that when $V_1 = V_m$, $G_e = 0$ (i.e., $P_o = 0$). Solving for V_1^2 and substituting into the P_o equation, we have

$$P_o = \frac{G_L}{2} \left(1 - \frac{G_L}{G_s} \right) V_m^2 \qquad \text{(C-3)}$$

In terms of the two diode parameters, G_s and V_m, the optimum power occurs when $G_L = G_{Lo} = G_s/2$. For this condition

$$V_{1\ (opt)} = \frac{V_m}{\sqrt{2}} \quad \text{(optimum chip voltage)} \qquad \text{(C-4)}$$

and

$$P_{(opt)} = \frac{G_s V_m^2}{8} \quad \text{(optimum power output)} \qquad \text{(C-5)}$$

For the diode assumed, $V_m = 22.34$ and $G_s = 40 \times 10^{-3}$ mhos. Thus

$$P_o = 249.5 \; G_L - 6238.5 \; G_J^2 \qquad \text{(C-6)}$$

A plot of this equation near $G_{L\ (opt)}$ is given as the middle curve of Figure C-2.

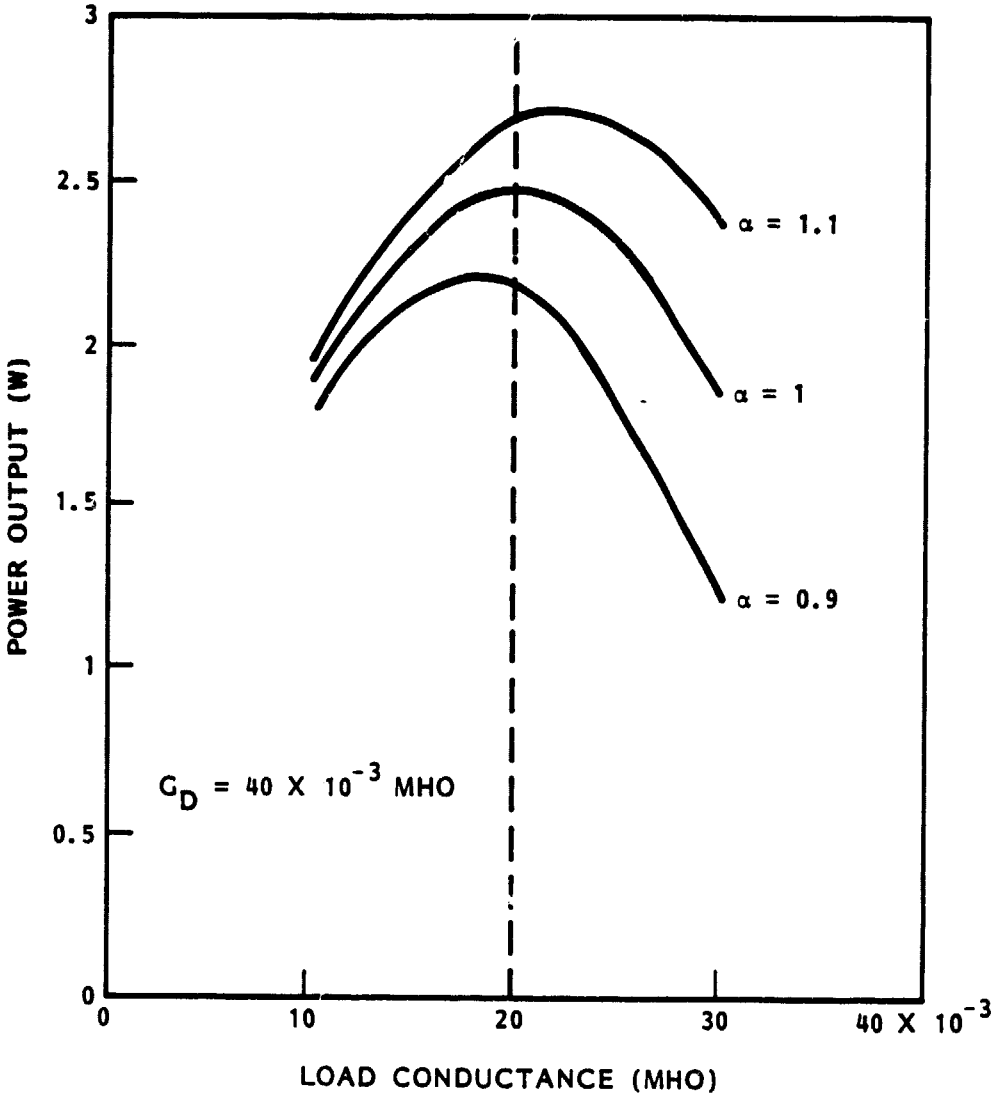


Figure C-2. Output Power Variations Due to Diode Area Variations

If the diode area varies by a factor a, then

$$P_o = 249.5\ G_L - \frac{6238.5}{a}\ G_L^2 \qquad \text{(C-7)}$$

It has been assumed that V_m remains unchanged, since only area variations are considered, and that the new value of G_s is aG_s.

Figure C-2 shows the effect of changes of a from 1.1 to 0.9 (±10% change in area). It is seen that, since the load conductance is assumed constant, the power varies about the nominal 2.5-W value from 2.2 W to 2.7 W.

Oscillator Frequency Variations

The sensitivity of the oscillator frequency to changes in the diode area can be estimated from

$$\Delta f_o = -\frac{f_o}{2}\ \frac{\Delta c}{c} \qquad \text{(C-9)}$$

where Δf_o is the change in f_o, the free-running oscillator frequency, Δc, is the change in capacitance of the diode and c is the equivalent capacitance of the oscillator. It is estimated that the capacitance of the diode chip will be 1.3 pF and the effective capacitance of the oscillator will be 2.0 pF. Therefore, a 10% change in diode chip area will result in $\Delta c = \pm 0.13$ pF so that $\Delta f_o = \mp 650$ MHz.

This calculation shows that the oscillator is very sensitive to changes in the diode capacitance. It is interesting to note that the amplifier design factors which produce large locking bandwidths will also increase the sensitivity to diode capacitance variations. It should also be noted that because of this sensitivity, it will be necessary to provide a frequency adjustment element in each oscillator to maintain a center frequency of about 20 GHz.

Locking Bandwidth Sensitivity

The external Q of the amplifier is given by

$$Q_x = \frac{\omega_o C}{G_L} \qquad \text{(C-10)}$$

where C is the effective capacitance of the oscillator, G_L is the load conductance as measured at the diode chip plane, and ω_o is 2π times the free-running frequency of the oscillator. Assuming, for the average diode, that

$G_L = 20 \times 10^{-3}$ mho, $\omega_o = 2\pi \times 20 \times 10^9$ rads/s, and $C = 2 \times 10^{-12}$F, Q_x is approximately 12.5. For a diode with 10% larger diode chip area, Q_x is 13.4, assuming all other design parameters are unchanged. For a 10% reduction in diode chip area, Q_x becomes 11.75.

The small-signal locking bandwidth of an oscillator is given by

$$f = \frac{f_o}{Q_x} \left(\frac{P_i}{P_o} \right)^{1/2} \qquad \text{(C-11)}$$

where f_o is the center frequency,

Q_x is the external Q,

P_i is the locking power,

P_o is the output power.

Assuming that the nominal values of the amplifier P_i and P_o are 0.25 W and 2.5 W, respectively, the nominal locking bandwidth is, assuming Q_x 12.5, 505 MHz. For a 10% increase in diode chip area, accounting for the power variations and Q_x variations, the locking bandwidth is estimated to be 472 MHz, and for a 10% decrease, the estimated bandwidth is 538 MHz. These results are shown graphically in Figure C-3.

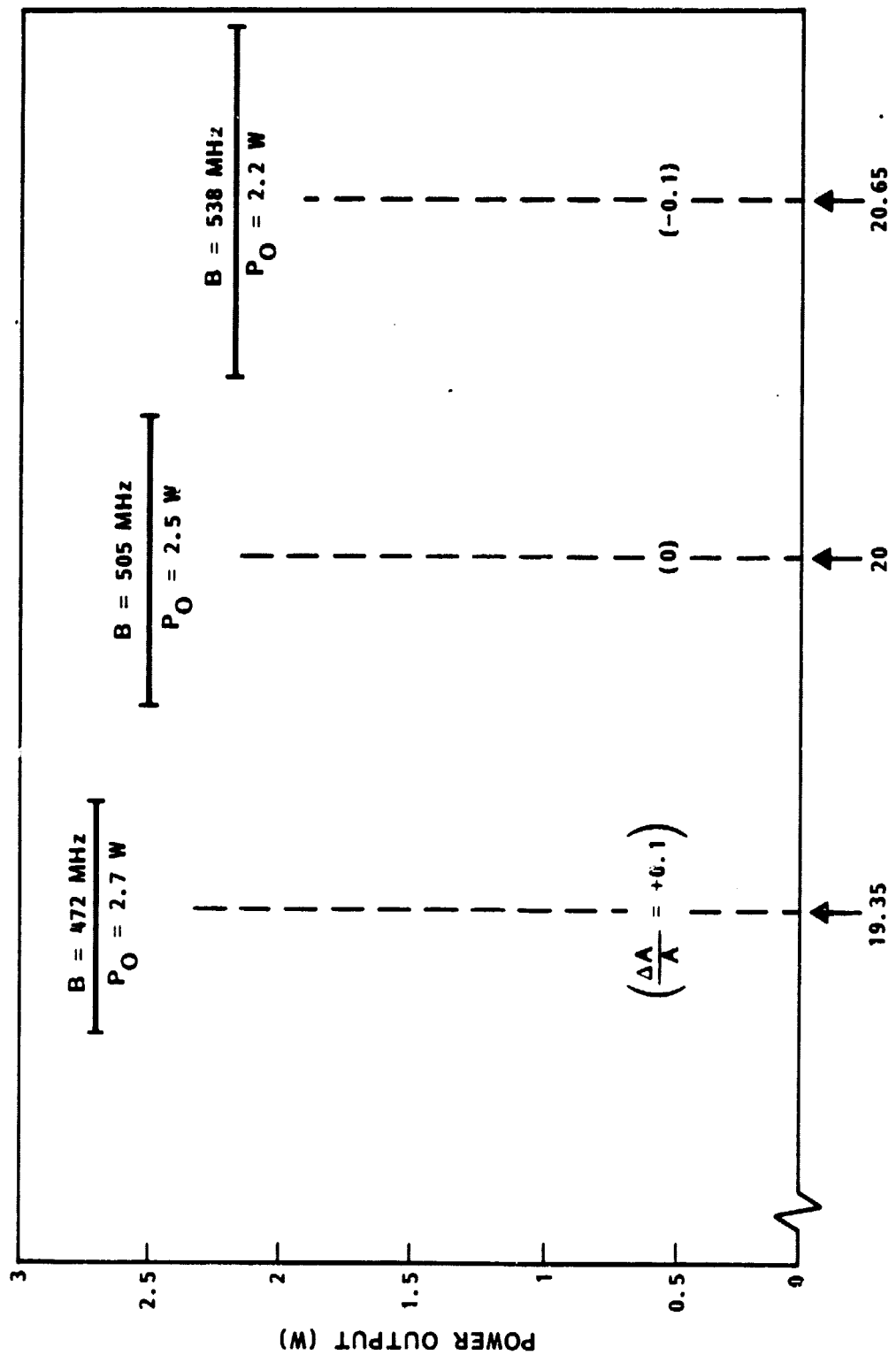


Figure C-3. Center-Frequency and Locking-Bandwidth Changes Due to Diode-Area Variation

APPENDIX D

UNABRIDGED RAYTHEON IMPATT DIODE DEVELOPMENT REPORT

D2

S-3057

20-GHz IMPATT DIODE DEVELOPMENT

by

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Redondo Beach, California 90278

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1.0 INTRODUCTION

This report describes the development of 20 GHz, double-drift GaAs IMPATT diodes carried out at Raytheon Research Division for TRW, Inc., from October 1980 to March 1982. These devices will be used in a proof-of-concept amplifier being developed at TRW for NASA's downlink transmitter of the 30/20 GHz Satellite Communication Program.

During the course of this development, advances were made in material growth, diode fabrication technology and packaging, and circuit design and diode testing. Devices were sent to TRW for evaluation and finally for use in the amplifier.

The diode performance goals for the program were:

Frequency:	20 GHz ± 1 GHz
Power output:	6 W goal, 4 W min.
Conversion efficiency:	25% goal, 20% min.
Maximum junction temperature:	≤275°C

We have demonstrated power levels exceeding 4 W CW and conversion efficiencies greater than 20 percent.

All through this report, the values of power and efficiency are quoted as available at the diode chip. This eliminates the package and circuit effects which vary from user to user. In order to find the power available at the external load, one measures the circuit efficiency defined as the ratio of power in the external load to the total power available at the diode port(s). If the rf circuit is characterized by measuring its S parameters, the circuit efficiency is given by:

$$\eta_{circ} = \frac{|S_{21}|^2}{1 - |S_{11}|^2}$$

This approach to diode and circuit characterization permits to design and predict accurately the performance of oscillators and amplifiers.

A diamond heatsink package was developed to obtain low thermal impedance. We also explored a new technology which gave a quadrimesa geometry to further reduce the thermal resistance.

At TRW's request, in September 1981, we undertook an accelerated diode fabrication program to deliver fifty identical diodes by mid-February 1982. These diodes were to be single-mesa, beam-leaded, and mounted in small EHF packages with diamond heatsinks. Unfortunately, the devices built have a lower conversion efficiency than anticipated. We know the reasons for the degraded performance and have taken corrective action for future devices.

Section 2.0 of this report will describe our efforts to obtain the double-drift, double-Read-profile, epitaxial layers of GaAs required for optimum device performance. In Section 3.0 we outline the diode fabrication technology and the packaging techniques used. The diode performances and the microwave circuit design are given in Section 4.0.

We have performed some preliminary measurements of the reliability of the GaAs IMPATT diode. The results of these measurements suggested some changes in technology, which we have implemented. We have also evaluated the increase in mean time to failure (MTTF) of the improved device. This work is described in Section 5.0. Finally, Section 6.0 describes the diode-modeling techniques used in our laboratory and gives an evaluation of the diode performance limitation.

2.0 EPITAXIAL GROWTH

2.1 Evolution of Doping Profile Specifications

The primary goal of the epitaxial growth effort for this contract was to provide qualified wafers to the processing laboratory for both device fabrication and process development. Qualified wafers are those wafers whose doping profiles meet a particular set of criteria which are detailed in a doping profile specification, the evolution of which is normally a result of both theoretical analysis and practical experience.

At the start of the contract effort, we had no in-house experience with the growth of material for 20-GHz devices. Our experience with devices of higher (40 GHz) and lower (10 GHz) frequency indicated that a double-drift Read structure (Fig. 1) would produce maximum power and efficiency. Scaling up from 10 GHz and down from 40 GHz produced our initial doping profile specifications, K-DDR-1 and K-DDR-2 respectively, given in Table 1.

Our experience with 10- and 40-GHz devices had led us to adopt doping profiles for these devices which are fundamentally different from one another even after scaling the profile parameters to a common frequency. These differences are reflected in K-DDR-1 and K-DDR-2. Specification K-DDR-1, which is a scaled-up version of our X-band, high-efficiency profile, calls for considerably thicker active layers, a much smaller p-spike charge, and hence higher breakdown voltage (V_B ~ 40 V) than K-DDR-2, which is derived from our optimized EHF specification.

A number of wafers were grown and delivered to each of these initial doping specifications. Rather than proceed at that point with additional growth runs without knowing which direction to take, we diverted the K-band reactor to other programs for one month, during which time rf test results on the first growth series became available. The results indicated that K-DDR-2 was the better specification and suggested that even thinner active layers were called for. In addition, concern arose over the importance of series resistance as a

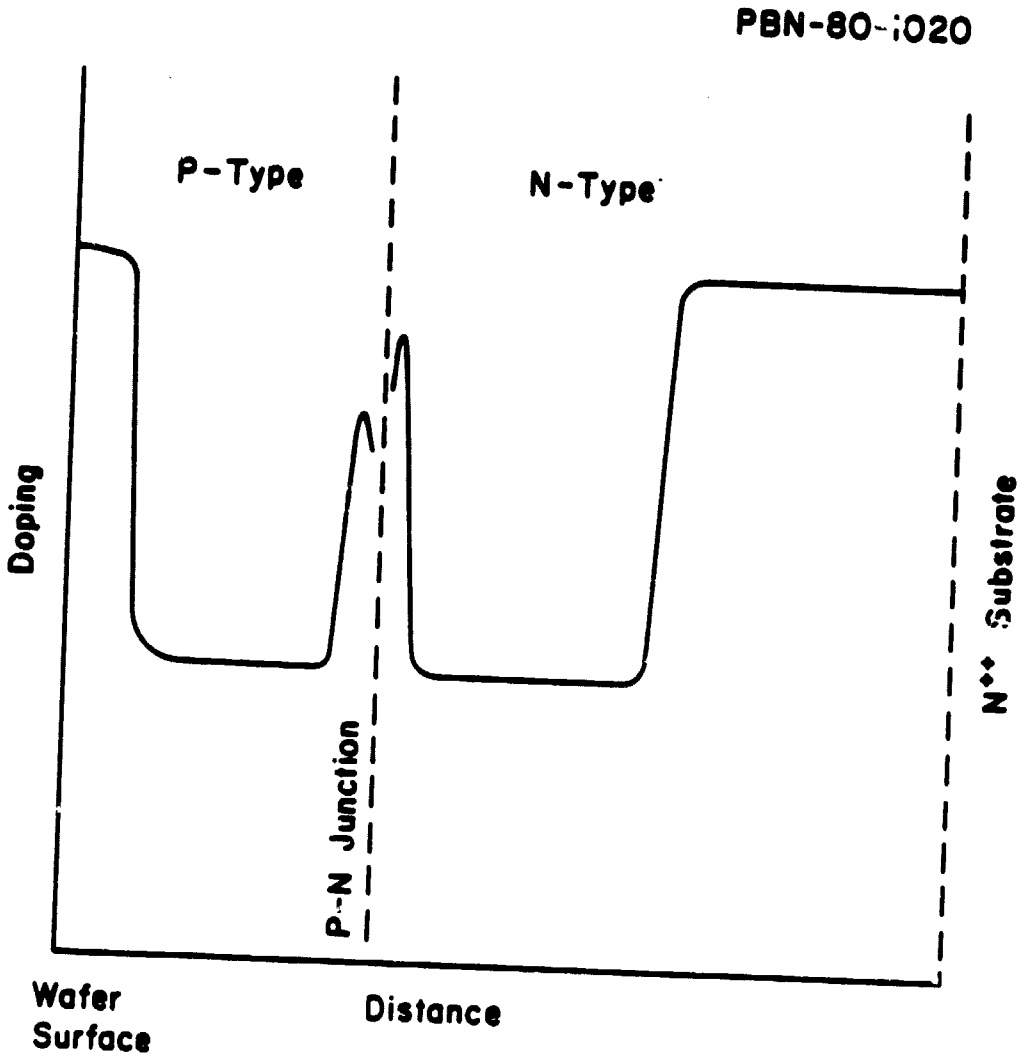


Figure 1. Double-drift Read doping profile.

TABLE 1

INITIAL K-BAND DOPING PROFILE SPECIFICATIONS

Specification No. K-DDR-1

Layer	Thickness (μm)	Doping (cm^{-3})	Q ($\times 10^{12} cm^{-2}$)
n^{++} buffer	6-8	$> 1 \times 10^{18}$	
n active	1.8-2.1	$1.3\text{-}1.6 \times 10^{16}$	
n spike			1.3-1.5
p spike			0.2-0.5
p active	1.3-1.6	$1.2\text{-}1.5 \times 10^{16}$	
p^{++} contact	0.2-0.4	$> 1 \times 10^{18}$	

Specification No. K-DDR-2

n^{++} buffer	6-8	$> 1 \times 10^{18}$	
n active	0.9-1.1	$7\text{-}9 \times 10^{15}$	
n spike			1.9-2.0
spike-to-spike	0.25		
p spike			1.1-1.3
p active	0.9-1.1	$1.2\text{-}1.4 \times 10^{16}$	
p^{++} contact	0.2-0.4	$> 1 \times 10^{18}$	

potential source of performance limitation. The result of these test data and concerns was a new specification, K-DDR-3 (Table 2). As Table 2 shows, K-DDR-3 is quite similar to K-DDR-2, with the exception of the thinner active layers.

Approximately nine months into the contract effort, we undertook a comprehensive review of diode performance as a function of material profile. We found that the diodes fell into three broad performance categories, each of which had distinctive profile features. Table 3 lists these three categories showing typical powers and efficiencies for three specific wafers, one in each group. We found that our best performance diodes had nearly symmetric doping profiles. These findings led to the development of our final profile specification, K-DDR-4 (Table 4).

The principal difference between K-DDR-3 and K-DDR-4 is that the p- and n-spike charges are more nearly equal to one another in K-DDR-4. This symmetry is clearly reflected in Fig. 2 which shows the expected mesa profile (effective carrier concentration vs. total depletion width about the p-n junction) for K-DDR-4. All remaining growth runs for this contract were based on K-DDR-4.

2.2 Reactor Technology

The growth of qualified wafers for device processing is critically dependent upon the ability to carefully control the crystal growth environment. In particular, growth of qualified material with good yield calls for a high degree of reproducibility in the epitaxial growth reactor. One of our standard double-drift IMPATT reactors was dedicated full-time to the growth of K-band material for the duration of this contract. During the course of the contract effort, we made a number of improvements to the reactor and its control system. In mid-1981, we implemented full microcomputer control of the reactor, so that control of all doping network switches, gas flow controllers, and sequence timing was carried out by a computer which in turn was programmed by the reactor technician.

TABLE 2

K-BAND DOPING PROFILE SPECIFICATION

Specification No. K-DDR-3

Layer	Thickness (μm)	Doping (cm^{-3})	Q ($\times 10^{12} cm^{-2}$)
n^{++} buffer	6-8	$> 1 \times 10^{18}$	
n active	0.6-0.9	$0.8\text{-}1.2 \times 10^{16}$	
n spike			1.5-2.5
spike-to-spike	0.15-0.3		
p spike			0.9-1.5
p active	0.6-0.9	$0.9\text{-}1.5 \times 10^{16}$	
p^{++} contact	0.15-0.25	1×10^{18}	$C_o > 600$ pF

$25\ V < V_B\ (1\ mA) < 30\ V$

TABLE 3

COMPARISON OF MATERIAL PROPERTIES

Group	Wafer No.	V_B (V)	X_P (μm)	Na $X10^{16}cm^{-3}$	Qa $X10^{12}cm^{-2}$	Qe $X10^{12}cm^{-2}$	Nd $X10^{16}cm^{-3}$	Xd (μm)	P (W)	η (%)
1	9A-75	31.7	0.85	0.70	1.37	1.58	0.7	0.92	1.99	19.5
2	9A-37	32.8	1.11	1.2	1.00	1.80	3.2	1.30	0.89	13.1
3	9B-19	27.0	0.5	1.3	0.81	2.20	2.3	0.70	0.56	7.4

TABLE 4

K-BAND MATERIAL SPECIFICATION

Specification No. K-DDR-4

Layer	Thickness (μm)	Doping (cm^{-3})	Q ($x10^{12} cm^{-2}$)
n^{++} buffer	6-10	$> 10^{18}$	
n active	0.9 - 1.1	$0.8 - 1.1\ 10^{16}$	
n spike			1.5 - 2.0
spike to spike	0.2		
p spike			1.3 - 1.5
p active	0.8 - 1.0	$0.8 - 1.2\ 10^{16}$	
p^{++} contact	0.15 - 0.25	$> 10^{18}$	
	$23.0 < V_B < 30.0$ V	$C_o > 600$ pf	

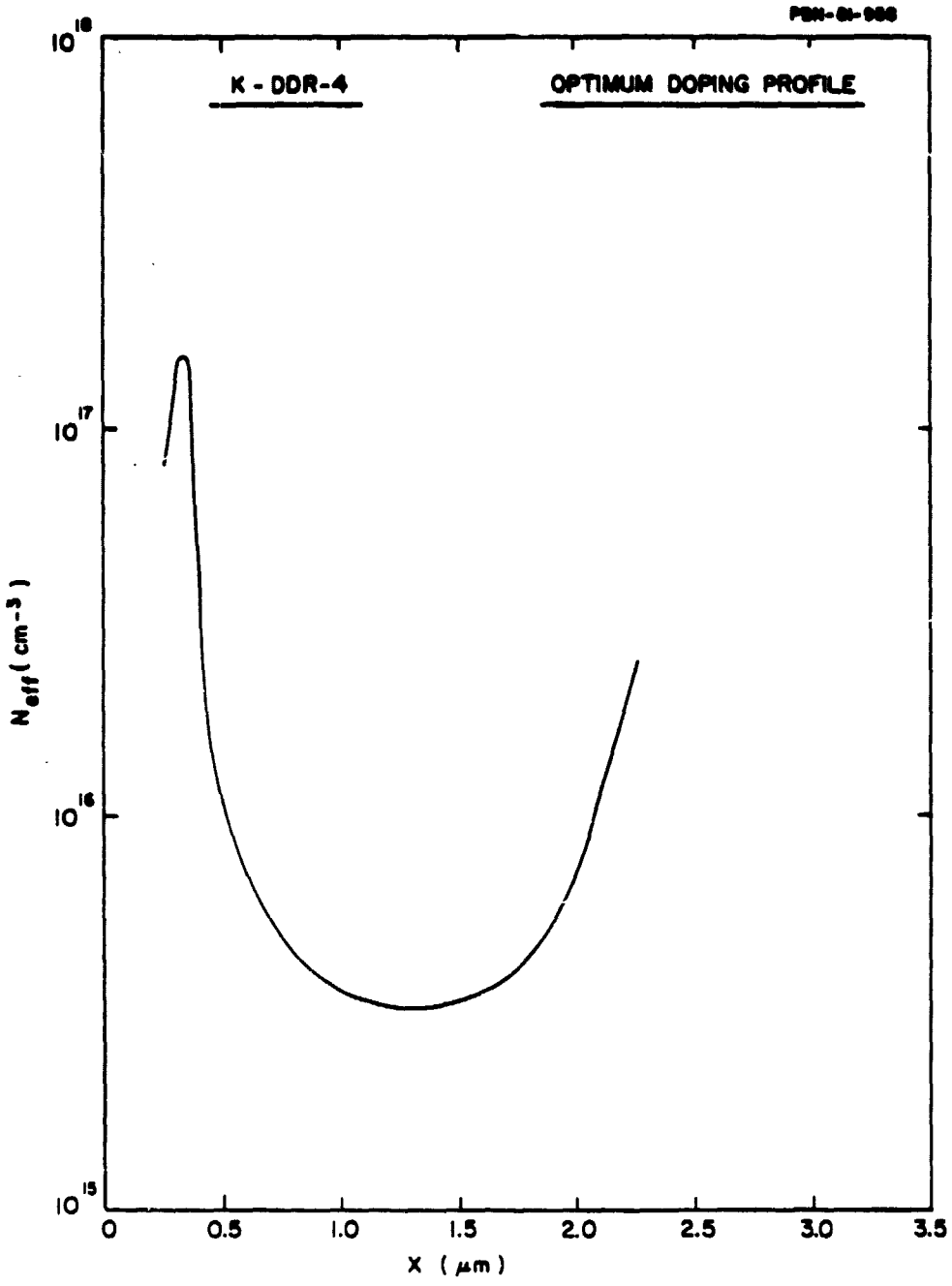


Figure 2. Doping profile of a mesa with specification K-DDR-4.

In addition to implementing computer control, we made several modifications to the p-dopant retort controller in an effort to make temperature control and stability both more responsive and more reproducible.

Finally, efforts were made to assess growth uniformity across the wafer and to improve uniformity. The complex reactions between gas-phase components in the reactor tube are further complicated by temperature gradients and intricate gas-flow dynamics to the extent that the factors governing growth rate and dopant incorporation uniformity are difficult to assess, and even more difficult to control. In fact, wafer nonuniformity remained in the end our most troublesome problem, seriously affecting diode yield. This problem is discussed further in a later section of this report.

2.3 Wafer Deliveries

During this contract effort, a total of thirty wafers were delivered to the processing laboratory for device fabrication. These wafers were grown to the specifications given in Sec. 2.1. Profile characteristics of all delivered wafers are listed in the Appendix.

3.0 DIODE FABRICATION TECHNOLOGY

3.1 Goals and Summary

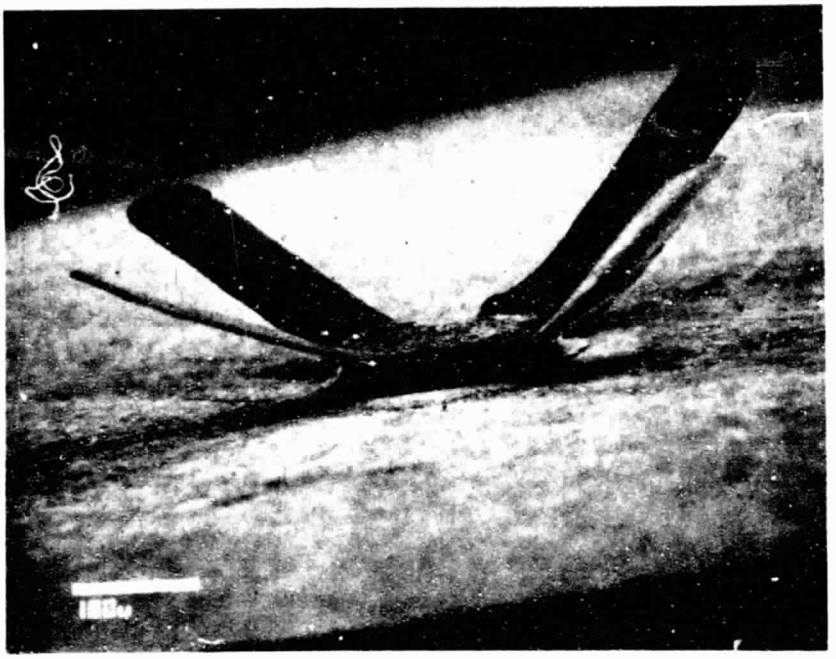
The technology goals of the program were: (1) to implement a fabrication technology which will result in chips that do not have a plated heatsink, that can be mounted on a diamond heatsink, and that have beam leads for bias connection; and (2) to implement a diode fabrication method wherein at least three mesas are interconnected by a beam-lead conductor and are bonded to a diamond heatsink. We accomplished both of these tasks, although the greater emphasis was placed on the first because of dimensional constraints imposed by the EHF package requested by TRW.

Beginning in the eleventh month of the program, we started an accelerated effort to provide chips and packages for a February diode delivery. Ten wafers were processed into 8-mil-diameter, single-mesa, beam-leaded chips, using a metal barrier layer at the p contact for reliability. Profile nonuniformity and problems encountered during processing led to a low chip yield for several of these wafers. The delivery consisted of chips made from wafer 9E-39 (see Fig. 3).

The chips were thermocompression-bonded into EHF-D, diamond-loaded packages, fabricated at Raytheon. Thermal resistances below 12° C per watt were measured on these diodes. Chips were preselected to meet the V_B specification, and etched in the package to meet the C_B requirement. Capping was carried out by soldering using gold-germanium (Au-Ge) preforms.

3.2 Chip Fabrication

Thirty wafers were selected for processing into either single-mesa or multi-mesa chips, as summarized in Table 5. The general process used for each wafer is identified in the second column of the table. The first two digits of the process number designate the frequency band in GHz at which the chips are intended to operate, hence indirectly specifying the overall dimensions of



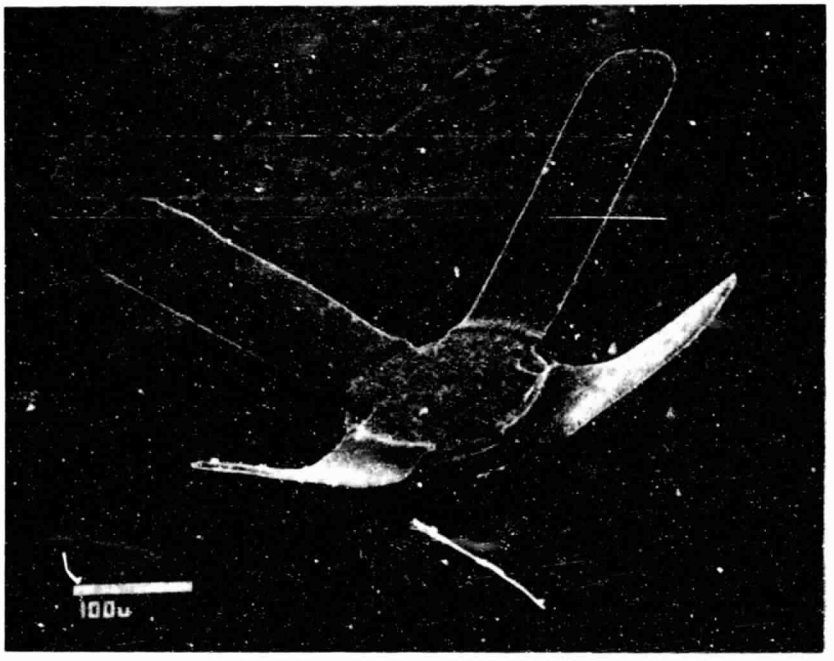


Figure 3. Eight-mil diameter beam-leaded single-mesa chips fabricated from wafer 9E-39 (SEM photographs).

TABLE 5

SUMMARY OF WAFERS PROCESSED INTO CHIPS

WAFER NO.	PROCESS NO.	MESA HEIGHT (μm)	MESA DIAM. (Mils)	BOTTOM CONTACT THICKNESS (μm)	CONFIGURATION	LEADS	TOP CONTACT METAL.	REMARKS
9A-18	20Q402	17-20	4	2[illegible]	Quadrimesa	Preform	Au-Ge	
9A-19	20Q402	17-20	4	25	Quadrimesa	Preform	Au-Ge	
9A-33	20Q402	15-20	4	25	Quadrimesa	Preform	Au-Ge	
9A-35	20S602	15-20	6	25	Single mesa	Preform	Au-Ge	
9A-36	20S603	15-20	6	25	Single mesa	Preform	Au-Ge	Damaged
9A-37	20S603	8-10	6	2	Single mesa	Beam	Au-Ge	
9A-75	20Q402	15-20	4	25	Quadrimesa	Preform	Au-Ge	
9A-93	20S803	8-10	8	2	Single mesa	Beam	Au-Ge	
9A-101	20S803	8-10	8	2	Single mesa	Beam	Au-Ge	Damaged
9A-102	20S803	8-10	8	2	Single mesa	Beam	Pt:Ti:Pt:Au	
9A-103	20Q402	15-20	4	25	Quadrimesa	Preform	Au-Ge	
9A-109	20Q402	15-20	4	25	Quadrimesa	Preform	Au-Ge	
9A-110	20S803	8-10	8	2	Single mesa	Beam	Pt:Ti:Pt:Au	
9A-111	20S803	8-10	8	2	Single mesa	Beam	Au-Ge	
9A-120	20Q402	15-20	4	25	Quadrimesa	Preform	Au-Ge	Damaged
9A-121	20Q402	15-20	4	25	Quadrimesa	Preform	Au-Ge	
9A-151	20S803	8-10	8	2	Single mesa	Beam	Au-Ge	
9A-153	20S803	8-10	8	2	Single mesa	Beam	Au-Ge	
9A-155	20Q402	15-20	4	45	Quadrimesa	Preform	Au-Ge	
9B-09	20S603	8-10	6	2	Single mesa	Beam	Au-Ge	
9B-19	20Q402	15-20	4	25	Quadrimesa	Preform	Au-Ge	
9B-25	20Q407	15-20	4	2	Quadrimesa	Preform	Au-Ge	
9E-29	20S803	8-10	8	2	Single mesa	Beam	Pt:Ti:Pt:Au	
9E-30	20S803	8-10	8	2	Single mesa	Beam	Pt:Ti:Pt:Au	
9E-36	20S803	8-10	8	2	Single mesa	Beam	Pt:Ti:Pt:Au	
9E-37	20S803	8-10	8	2	Single mesa	Beam	Pt:Ti:Pt:Au	Damaged
9E-38	20S803	8-10	8	2	Single mesa	Beam	Pt:Ti:Pt:Au	
9E-39	20S803	8-10	8	2	Single mesa	Beam	Pt:Ti:Pt:Au	
9E-48	20S803	8-10	8	2	Single mesa	Beam	Pt:Ti:Pt:Au	
9E-53	20S803	8-10	8	2	Single mesa	Beam	Pt:Ti:Pt:Au	

the chips. The following character denotes the number of mesas per chip: "S" specifies a single-mesa, "Q" a quadrimesa chip. The next digit designates the nominal diameter of each individual mesa in mils. The last two digits specify the process in more detail: 02 designates a standard plated-heatsink (PHS) process without overlay structures; 03 denotes a beam-lead overlay process; and 07 represents a web multimesa process* without overlay structures. The chip geometries produced by the four processes listed in Table 5 are shown schematically in Fig. 4. The wafers selected for the final diode delivery to TRW used process 20S803 to produce a beam-leaded, single-mesa chip, as shown in Fig. 3.

The yield of acceptable chips from these thirty wafers was partially determined by the smoothness, electrical characteristics, and uniformity of the epitaxial layers grown by the materials laboratory, and partially by consistency and suitability of the processing steps to which they were subjected. Owing to processing difficulties, some wafers produced few or no usable chips.

One troublesome problem which caused several wafers to be damaged occurred during the thinning operation. Wafers were thinned by a lapping operation after they were affixed to a flat support using a wax mounting material. Irregularities in the wafer surface introduced difficulties in the mounting step. If the adhesion between the wafer and the mount weakened during the lapping operation, the wafer became partially or totally dismounted, resulting in over-thinning and some cracking; wafers 9A-93 and 9A-111 experienced this problem. This was especially apt to occur if the original wafer surface was rough or uneven. In the case of wafer 9A-120, for example, the wafer cracked into three separate pieces. Usually, when cracking or overthinning occurred, we were able to salvage most of the wafer, but in a few instances the wafer was irretrievable. Usually, however, chip lots from wafers which became partially or totally dismounted during lapping had a larger than usual incidence of soft breakdown characteristics when packaged.

We spent considerable effort trying to solve this problem. We found that much of our difficulty arose from the quality of the adhesive used. We have

* *Developed under Raytheon funding, patent pending.*

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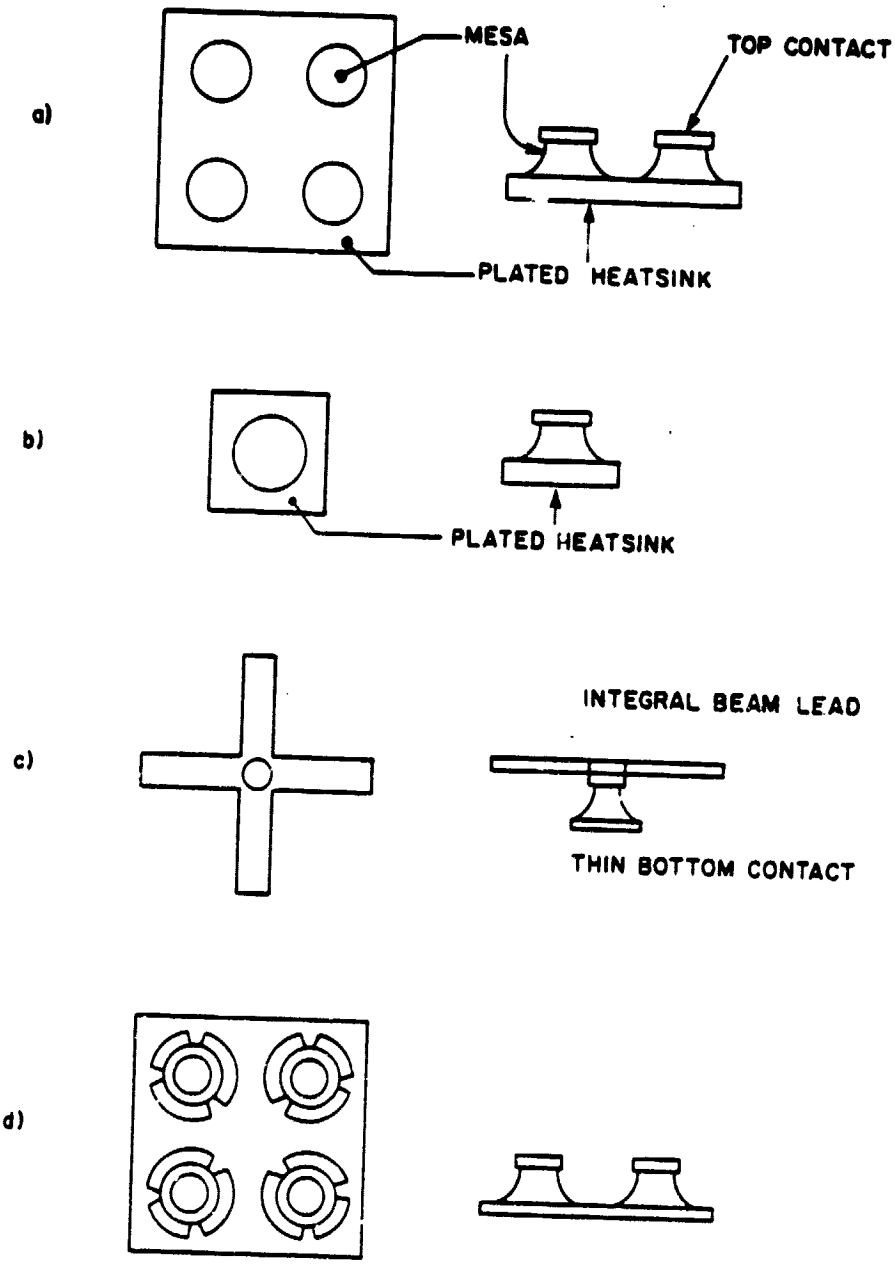

Figure 4. Chip geometries produced by four processes: (a) 20Q × 02; (b) 20S × 02; (c) 20S × 03; (d) 20Q × 07.

recently used a different adhesive, which has alleviated the problem.

A second problem which limited chip yield was over-etching during the mesa definition step, resulting in mesas whose area was too small or whose shape was not optimal. A considerable effort was expended in trying to make this process step more reproducible. In part this effect appeared to be related to the material characteristics of the wafer, and in part to the care taken in the wafer thinning and other preparatory process steps, as well as the care taken in the mesa-definition etch step itself. We found that, with sufficient care, we could minimize this problem for most wafers.

A third problem limiting chip yield was the result of misalignment during multiple masking steps (Fig. 5). This was particularly troublesome for the overlay processes used for the formation of beam leads, as well as in the masking steps used to form the barrier metal contacts (platinum:titanium:platinum:gold – Pt:Ti:Pt:Au) adopted late in the program. This problem was found to result principally from difficulties which the mask aligner operators experienced in indexing the mask to the appropriate wafer detail through the thick layers of resist necessary for the overlay processes. The problem was compounded by the nonuniform wafer thicknesses characteristic of IMPATT diode technology. The deleterious effects of these difficulties were minimized by implementing stringent quality checks at critical points of the process.

A fourth problem, which could arise in any of the prepatterned gold-plating operations, was a deterioration in the effectiveness of the masking resist as plating progressed. This resulted in edge buildup of the gold-plated pattern (see Fig. 6) and in extreme cases fusion of the patterns, as occurred with wafer 9E-29. We found that this effect was enhanced by the ultrasonic agitation used to obtain good throwing power in our gold-plating bath. Resist deterioration was also accelerated at the normal plating temperature of 60° C. The incidence of this problem has been reduced on an experimental basis by the elimination of ultrasonic agitation and by the use of a lower plating temperature.

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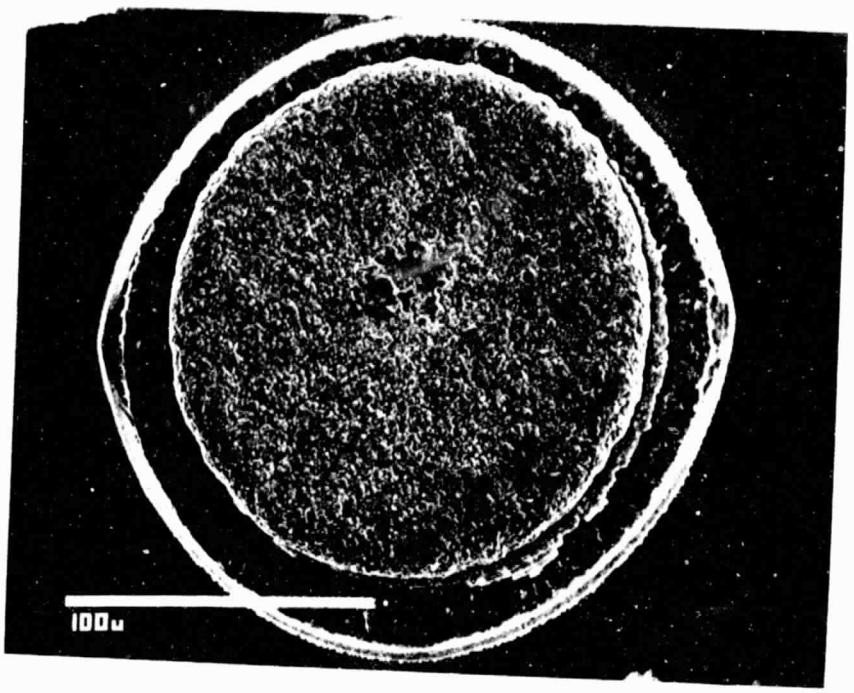

Figure 5. The top of a metallized mesa showing the result of misalignment during photolithography.

Figure 6. Growth of overlay on the edge of the mesa contact and excess gold plating ridge due to resist deterioration (SEM photograph).

A fifth problem arose when we decided to replace the gold-germanium metalization on the top contact with a barrier layer metalization, namely Pt:Ti:Pt:Au. The platinum layers are not easily etched chemically, so we patterned the metalization by lift-off, which required the introduction of several photolithographic steps. Adherence problems arose between the plated gold and the contact metalization, particularly during beam-lead formation. This problem was severe in wafers 9A-102 and 9A-110. It was corrected in subsequent wafer processing by introducing a brief clean-up etch after application of the continuity layer and prior to beam-lead formation.

3.3 Chip Technology Development

3.3.1 Metalization

The standard metalizations used at the beginning of the contract were sputtered Pt:Ti:Au layers on the p^{++} contact and an evaporated Au-Ge alloy on the n^{++} contact.

In the early phases of this contract we evaluated sputtered Ti:Au metalization on the p^{++} contact. This metalization should be easier to etch than the usual Pt:Ti:Au metalization, offering the possibility of eliminating several of the process steps. Analyses showed that neither Pt:Ti:Au nor Ti:Pt:Au metalization demonstrates appreciable gold diffusion into the gallium arsenide after an elevated temperature exposure, but that metalization with Ti:Au only displayed extensive diffusion of gold into the gallium arsenide after the same heat treatment.

A similar trend may be deduced from observations upon our experimental wafer 9A-55. This slice was split into two halves, one metalized in the usual way with Pt:Ti:Au, and the other with Ti:Au only. The two pieces were processed as nearly identically as possible using our overlay process. The resultant chips were thermocompression-bonded into Type 16 packages and subjected to a 200° C vacuum bake and dry nitrogen capping. The half incorporating Ti:Au metalization displayed a much greater incidence of soft reverse breakdowns at t[illegible] one using standard metalization. We

concluded that refractory barrier metals such as platinum were necessary in the metalization to gallium arsenide to prevent gold diffusion, and hence obtain reasonable device reliability.

The Au-Ge alloy contacts also suffer from gold-gallium arsenide interaction. Tests of the reliability of IMPATT diodes have shown that chips with Au-Ge alloy contacts display a disappointing mean time to failure (MTTF). Experiments performed at Raytheon and elsewhere have shown that substitution of metalizations incorporating barrier layers against the diffusion of gold, such as Pt:Ti:Au or Pt:Ti:Ft:Au, results in greatly improved reliability.

Accordingly, after the eleventh month of the program all chips incorporated Pt:Ti:Pt:Au metalization on the n^{++} contact instead of Au-Ge alloy. This change necessitated other changes in processing. The Au-Ge layer had been patterned by etching. This was no longer possible with the Pt:Ti:Pt:Au layers, hence patterning was achieved by liftoff. This process was developed experimentally using scrap wafers prior to use on device-grade wafers. Even so, we experienced difficulties with contact adherence on the first device-grade wafers (9A-102 and 9A-110) processed from this program. These problems were corrected by a brief clean-up etch.

3.3.2 Multimesa chip technology

For any given device there is an optimum area needed to achieve high-power operation. We discuss this problem in later sections on diode design. In general, although heat conduction increases with increasing device area, for a finite series resistance there is a maximum area above which the device performance degrades badly. It is well known that the thermal conductance of chips of a constant area can be increased by the use of extended geometries such as annular rings or multimesas. A further increase in thermal conductance can be achieved on heat spreaders of high thermal conductivity, such as diamonds.

We initially made 26-GHz multimesa chips using our standard PHS technology appropriately scaled for frequency. The 25-μm bottom gold contact

layer, known as the PES, is sturdy enough to support the mesas through the chip fabrication and packaging operations. This thick gold layer, however, interposes an appreciable thermal barrier between the mesa and the diamond heat-spreader and seriously degrades the thermal conductance of the multimesa chip. When the gold contact layer is made thin enough not to affect the thermal conductance appreciably, the chip becomes very fragile and is difficult to handle.

The mesas could be supported by beam leads formed by an overlay process. The beam leads would provide adequate mechanical support without adversely affecting thermal conductance. Implementing this scheme at 20 GHz, however, would greatly reduce the number of chips which could be fabricated from a wafer because of the large area consumed by the beam leads. The same objective can be achieved by an overlay geometry, shown schematically in Fig. 7a, without reducing the number of chips below that obtained using the standard quadrimesa process. After thermocompression-bonding the chips into packages, separate preformed leads are attached in the usual way.

Figure 7b is an SEM photograph of an experimental overlay cross quadrimesa chip made with 6-mil nominal diameter mesas on 12.5-mil centers. The gold bonding layer under each mesa was made 2 μm in thickness and 7 mils in diameter. The four mesas were mechanically supported during processing and packaging by a gold cross, formed by overlay plating on the top contacts of each mesa.

This process, though promising, requires further development. The overlay quadrimesa chips are still quite fragile and difficult to mount. For the particular chip geometry used, the overlay cross appeared to sag in the center of the chip, as seen in Fig. 7b, resulting in a large incidence of shorting after thermocompression bonding to a heat-spreader. This problem could be solved by changing the chip geometry. Specific design changes would require that the top contact heights be increased and the overlay structure be reinforced.

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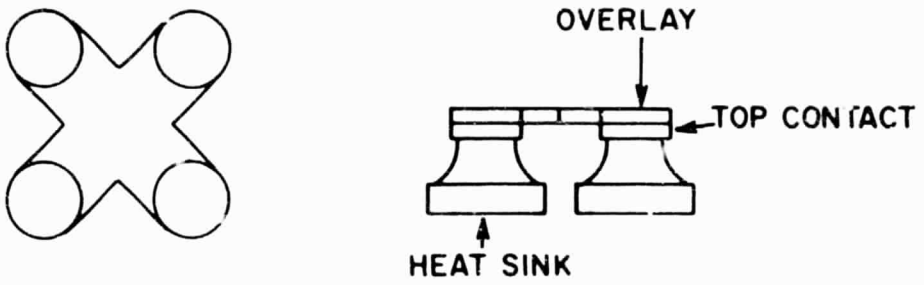

Figure 7a. Four-mesa cross overlay chip, schematic diagram.

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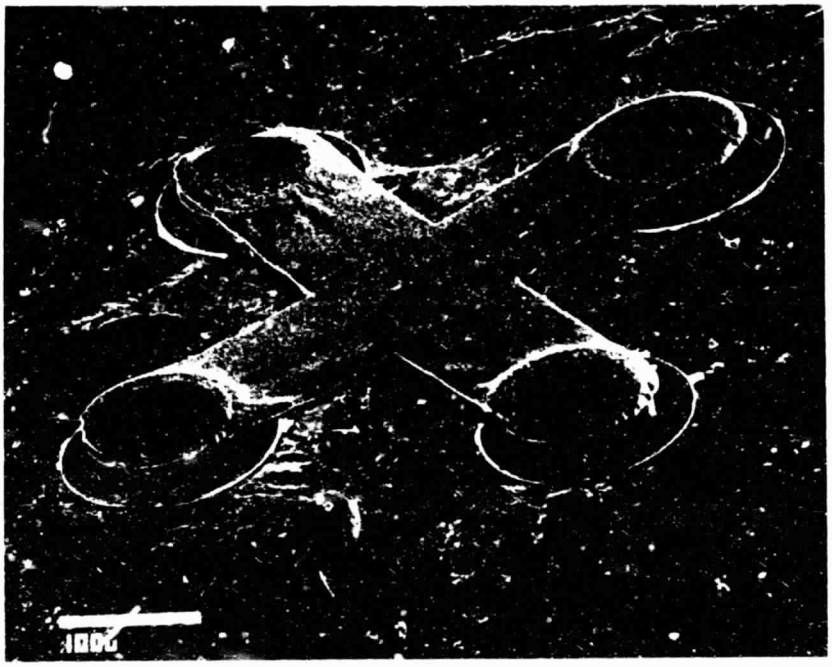

Figure 7b. Four-mesa cross overlay chip (wafer 9A-5. (SEM photograph, 200X).

We overcame this problem with a new chip design, developed under Raytheon funding, designated a "web" multimesa chip.* Each of the mesas is formed as usual upon a gold bonding disc, slightly larger than the mesa base, but only 2 μm in thickness. This chip design has worked very well, yielding excellent thermal conductances when mounted on copper or diamond heat-spreaders. Unfortunately, 20-GHz quadrimesa chips are too large to mount in the EHF packages requested by TRW; hence, this chip could not be used for the device delivery.

3.4 Chip Selection

Diodes intended for use in a combiner must be very similar to one another, in addition to being good individual performers. It is preferable that all chips intended for use in a single combiner be fabricated from the same wafer. To screen wafers for their general conformance to specification and to ensure that individual wafers are sufficiently uniform to give a good yield of chips with similar electrical characteristics, we customarily map the wafer after mesa definition in the chip fabrication laboratory for C_0, V_B, C_{V_M}, and V_M, where C_0 is the junction capacitance at zero bias, V_B is the breakdown voltage at 1 mA, V_M is the voltage at which the breakdown capacitance is measured (and is usually V_B -1), and C_{V_M} is the capacitance at V_M. Forward and reverse I-V characteristics are taken at the same time. Similar measurements were taken in the packaging laboratory on individual chips, and only those chips falling within specified limits were mounted into packages.

Table 6 is a summary of the map data for all wafers reaching the chip stage. Note that most wafers display a rather broad range of V_B values, making it difficult to select chips with closely grouped V_B's. Most of this spread results from variation in material characteristics arising in epitaxial growth. It is also evident that there is a marked difference in the forward I-V characteristics between those wafers fabricated with Au-Ge alloy metalization of the n^{++} layer and those wafers fabricated with Pt:Ti:Pt;Au metalization. Tests

* *Patent pending.*

TABLE 6

SUMMARY OF MAP DATA FROM WAFERS PROCESSED INTO CHIPS

WAFER NO.	V_B @ 1 Ma and 25° C (Volts) MEAN	σ	MIN	MAX	VM (Volts) MEAN	σ	C_{VM} (PF) MEAN	σ	Cφ (PF) MEAN	σ	V_{FWD} @ 10 Ma (Volts)
9A-18	44.0	0.7	43.0	45.0	42.0	1.6	0.59	0.05	3.55	0.19	1.2
9A-19	44.5	1.4	41.9	46.8	42.9	1.3	0.25	0.10	2.98	0.23	1.2
9A-33	37.0	5.4	18.3	41.9	35.5	5.2	0.35	0.13	3.37	0.28	1.2
9A-35	34.7	5.5	18.1	40.6	33.2	5.7	1.16	0.24	9.15	0.71	1.2
9A-36	33.9	3.5	22.2	38.0	32.4	3.9	1.38	0.18	9.69	0.84	1.1
9A-37	32.1	4.6	15.4	36.1	30.2	4.4	1.27	0.36	8.28	0.34	1.2
9A-75	34.5	5.4	20.6	40.9	34.2	4.5	0.49	0.03	3.82	0.21	1.1
9A-93	26.8	2.0	18.2	28.2	26.1	2.3	3.43	0.37	15.99	0.61	1.2
9A-102	32.2	2.2	27.8	34.0	31.0	2.1	2.03	0.12	13.93	0.42	4.4
9A-103	29.6	3.6	21.6	33.6	28.6	3.7	0.64	0.08	4.03	0.31	1.2
9A-109	24.5	3.2	15.2	26.9	23.4	3.2	1.37	0.40	5.73	0.47	1.1
9A-110	32.5	2.0	29.7	34.7	31.4	1.9	2.09	0.19	13.68	0.72	4.5
9A-111	28.7	5.1	16.6	34.0	28.2	5.1	2.04	0.51	12.33	0.70	1.2
9A-120	22.7	3.3	15.2	27.6	21.6	3.8	0.77	0.25	2.90	0.27	1.2
9A-121	21.6	4.0	14.7	26.6	20.9	4.1	0.67	0.25	2.74	0.30	1.2
9A-151	28.8	2.4	18.9	31.8	27.8	2.7	3.11	0.37	14.74	0.56	1.1
9A-153	25.3	1.7	18.6	27.7	24.4	1.7	4.00	0.46	15.61	0.82	1.1
9A-155	27.4	1.6	22.7	29.0	26.1	1.8	0.78	0.15	4.35	0.60	1.2
9B-09	31.6	1.8	25.8	33.2	30.6	1.7	1.37	0.09	8.07	0.81	1.2
9B-19	27.5	0.7	26.2	28.6	26.5	0.7	0.80	0.04	4.71	0.28	1.2
9B-25	26.6	0.9	24.1	28.0	25.5	0.9	0.83	0.11	4.88	0.64	1.2
9E-29	28.0	6.6	19.9	31.6	26.0	3.2	1.99	0.16	19.02	0.82	4.7
9E-30	24.2	6.6	14.8	31.9	23.2	5.3	2.28	0.53	19.16	1.14	3.8
9E-36	33.3	2.9	25.4	36.5	31.3	2.9	1.80	0.07	17.21	0.59	4.3
9E-38	29.6	3.7	22.8	34.7	27.5	3.6	1.98	0.47	17.86	2.77	4.0
9E-39	27.2	4.2	19.8	33.4	24.8	4.1	2.09	0.34	18.34	1.20	5.1
9E-48	33.8	5.2	17.0	39.6	31.6	5.2	1.85	0.25	16.67	0.75	5.2

at other frequencies have shown that this difference does not have a significant effect on diode performance, nor should any be expected, since this metal-semiconductor contact is operated with a polarity opposite to that used for I-V measurement.

The chips were also inspected visually, both in the chip fabrication laboratory and in the packaging laboratory, and those with obvious defects were rejected. The defects included: (1) misshapen or missing contacts or beam leads, (2) foreign material or films on bonding surfaces or mesas, (3) bits of metal, film, or other material which might cause electrical failure, (4) defects in the mesas such as cracks or rough surfaces, and (5) bent metal layers.

3.5 Packaging

We evaluated four major types of packages for this program: the Type 16, the Type 17 (a Type 16 with a short ceramic), the Type 11 (a Type 17 with no capping flange), and the EHF-M package (which also had no capping flange). All of these, except the EHF-M package, accepted our standard 20-GHz quadrimesa chip and its variations. The Type 16 and the Type 17 packages were baked and capped using our standard procedures and equipment. The Type 11 and the EHF-M packages required nonstandard capping procedures because of the absence of a capping flange. The EHF-M package accepted only single-mesa chips. All of these packages had copper heat-spreaders and #3-48 screw thread mounting studs. We also evaluated similar packages, developed at Raytheon, loaded with diamond heat-spreaders. These are identified with the same type of main numbers listed above but have a suffix "-D" appended to the type designation. They are similar to the parent package in the chips which they accept and the procedures used for capping.

Chips with a 25-μm or thicker bottom contact were mounted either by soldering, by using Au-Ge preforms, or by thermocompression-bonding directly to the heat-spreader. The thermal resistance obtained by soldering of these thicker-contact chips was not very different from that obtained by thermocompression-bonding. Indeed, if the surface finish of the heat-spreader was not sufficiently smooth, the thermal resistance obtained by soldering was often

superior to that obtained by thermocompression bonding. Chips with thin (2 μm) bottom contact layers were damaged by soldering, hence they had to be mounted using thermocompression-bonding.

Most wafers were initially screened by fabricating diode-evaluation lots by bonding selected chips into an appropriate copper package. Usually, these screening lots were left uncapped, so that C_{V_M} could be adjusted by in-package etching to optimize performance. Once a wafer yielded promising results, additional evaluation lots were fabricated by methods and in packages which promised to yield the best results.

Of the packages tried, TRW expressed a preference for the diamond-loaded EHF-D package. Therefore, during the last several months of the program, we settled on thermocompression-bonding of single-mesa, beam-leaded chips into EHF-D packages.

All single-mesa, beam-leaded chip lots were initially screened by thermocompression-bonding the chips into EHF-M copper packages. We had the greatest difficulty obtaining high-quality EHF-M copper packages from our vendors. Not only was the lead time between order placement and receipt extremely long but, worse, the product quality was exceptionally poor. The major difficulties were defective ceramics and poor surface finish of both the chip mounting area and the capping metalization. The ceramic cylinders were found to be cracked before or after chip mounting. The poor surface finish of the chip mounting area resulted in seriously degraded thermal resistances. The poor surface finish of the capping metallization sometimes resulted in poor lead bonding and great difficulty in capping. Eventually, we assembled the EHF-M copper packages at Raytheon from parts procured externally. Even then, we had to reject or rework many of the purchased parts before assembly. Given good quality EHF-M copper packages, we rather routinely obtained thermal resistances below 18°C per watt for single-mesa chips etched to a C_{V_M} of 1.25 pF and mounted in the package by thermocompression-bonding.

3.6 Diamond-Heatsink Packages

Throughout the course of the program, we attempted to obtain suitable diamond-loaded packages from various vendors, without notable success. At the same time we successfully carried on an internally funded program to develop a capability for fabricating diamond-loaded packages at Raytheon. We were able to fabricate diamond-loaded EHF-D packages in sufficient numbers to satisfy the delivery requirements of this program.

The EHF-D diamond package, shown schematically in Fig. 8, was fabricated by machining a square recess in an EHF copper stud, dimensioned to be a press fit to a square diamond 1 × 1 × 0.75 mm in size. The metalized diamond was hot-pressed into the recess, and the metalized ceramic is bonded to the center of the diamond.

Using diamond-heatsink EHF-D packages fabricated at Raytheon, we rather routinely obtained thermal resistances below 12° C per watt for single-mesa chips etched to a C_{V_M} of 1.25 pF and mounted in the package by thermo-compression-bonding.

We also experimented with other types of diamond-heatsink packages. Rather early in the program we soldered diamonds onto the pedestal of a Type 16 package. Later we inserted diamonds into a cavity machined in the pedestal of a Type 11 package. The objective of these experiments was to evaluate the performance of multimesa chips bonded to a diamond heat-spreader in a suitable package. Promising results were obtained but further work is required before diodes incorporating these developments can be routinely produced.

TRW provided us with fifty diamond-heatsink pill packages. Upon inspection, we found them to have a rather deep meniscus around the diamond, a problem which we also had during our first experiments with this technology. Since there is a possibility that this meniscus adds a significant series resistance to the diode, and since we did not have this problem with our diamond-loaded EHF-D packages, we used the latter to fabricate the diodes for delivery.

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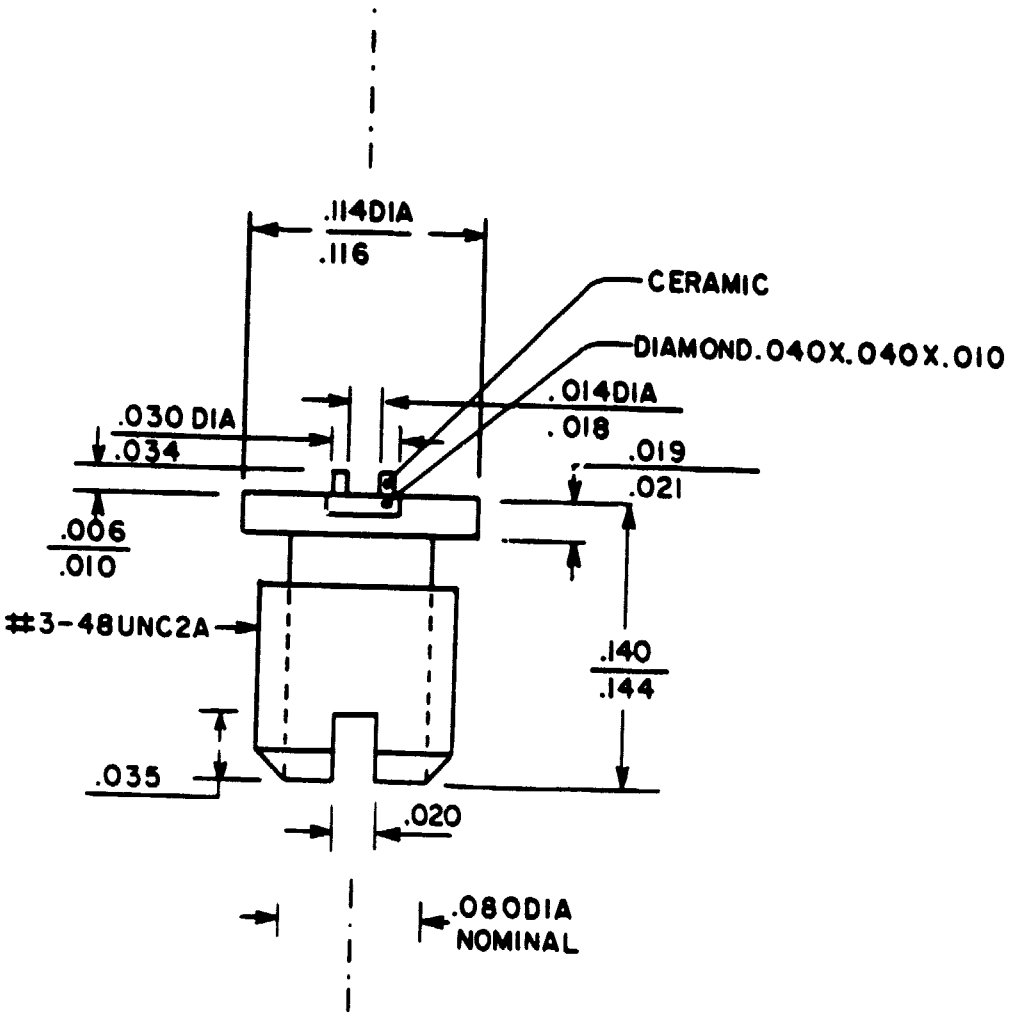

Figure 8. EHF diamond package.

3.7 Capping

We experienced no difficulty in capping diodes incorporating the Type 16 or Type 17 packages. These packages are provided with overhanging capping flanges, which permitted us to cap the diodes using our cap welder. Hermetic seals were assured by using MILSPEC gross and fine leak checks. Diodes were usually baked in vacuum for 44 hours at 225° C to remove adsorbed gases, especially water vapor, prior to capping in dry N_2, and thus improve reliability. The electrical characteristics of the diodes were measured before and after capping to assure that no degradation ensued as a result of the capping process.

Capping of the flangeless Type 11 and Type EHF-M packages proved to be more difficult. Early in the program, capping was carried out by soldering using a 90 percent tin/10 percent gold solder preform with blue flux. We found that this process was not very reliable. A considerable fraction of the diodes failed after capping, either from degraded I-V characteristics, or by mechanical failure of the solder joint between the cap and the package. We spent considerable effort trying to improve this process but with limited success.

Later, we experimented with 20 percent tin-80 percent gold preforms and found that under proper processing conditions a more reliable bond was obtained. However, the preforms we were able to obtain were too thick, giving too large a volume of solder. Commercial vendors were reluctant to provide preforms much thinner than 1 mil in thickness. We attempted to plate up preforms from a commercial gold-tin plating solution using resist masks. We found that the plating solution attacked the resist and became contaminated. Even when we tried plating on dummy samples without resist, using the manufacturer's recommended process, we obtained a plating which upon analysis was found to contain little tin. We contacted the manufacturer for assistance and he has promised to try to resolve the problem.

Using the thicker 20 percent tin-80 percent gold preforms, we were able to get strong joints without flux, using ultrasonic energy to encourage wetting.

In the meantime, we successfully capped EHF-M diodes using 0.025 in. × 0.035 in. gold-germanium annular preforms. This solder is very strong, but wetting is difficult to obtain without some sort of scrubbing. This we obtained by squeezing the molten solder between the cap and the gold-plated metalization of the ceramic. The delivered diodes were capped using this technique.

4.0 DIODE PERFORMANCE AND MICROWAVE CIRCUIT DESIGN

4.1 Introduction

Sample lots of diodes from each wafer processed have been delivered to the diode evaluation laboratory. As part of the routine evaluation tests, we

1. Measured thermal resistance.
2. Measured reverse breakdown voltage (V_B) (at a reverse current of 1 mA).
3. Observed the diode's dc characteristics on a curve tracer. In particular, the abruptness of the breakdown was examined in detail to detect leakage and microplasmas. Their presence was almost always a clear warning of poor rf performance and early burnout.
4. Measured the diode junction capacitance at 0 V bias (C_0) and as near as possible to the breakdown (C_{V_M}). We generally used a voltage $V_M = V_B - 1$ V.
5. Then, for those lots subject to microwave evaluation, we measured the operating frequency, the power output level, and the voltage and current of the dc bias. The conversion efficiency is calculated from this data.

The setup employed in the microwave evaluation of the 20-GHz diodes is shown in Fig. 9. All the components except the cavities, which were fabricated in-house, are unmodified commercial items. We have found that the design of the oscillator cavity structure used in microwave evaluation is critical in obtaining optimized diode performance. In the following section, we discuss the various cavities which were tested during the course of the contract.

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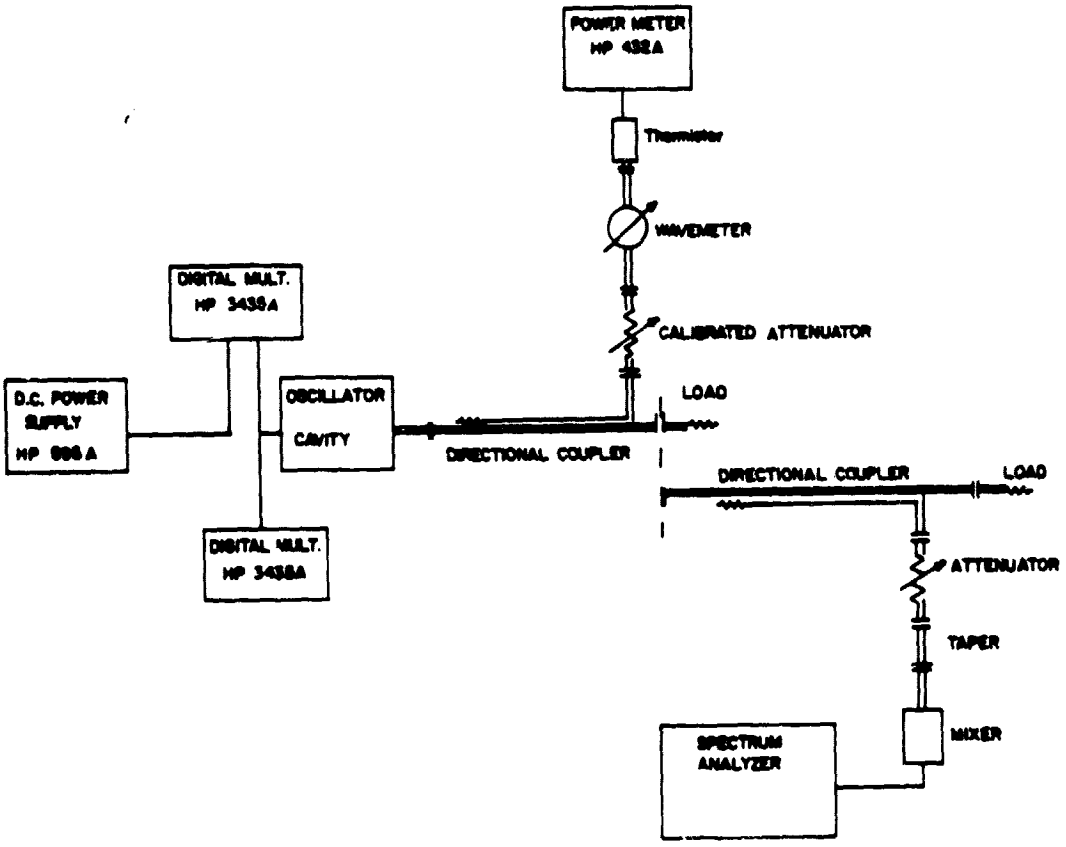

Figure 9. Test set-up for 20-GHz GaAs double-drift diodes.

4.2 20-GHz Test Cavities

Two different types of cavities were designed for the tests of the 20-GHz double-drift diodes. They were all made to operate in a WR 42 waveguide system (0.420 in. × 0.170 in.) which can propagate frequencies covering the range 18 to 26.5 GHz.

A "top hat" circuit was used at the beginning of this contract. It is shown in cross-section in Fig. 10. The E-H tuner is incorporated in the same metal block in order to place it $\lambda_g/4$ away from the diode. The device under test is held in a chuck which can be continually adjusted to obtain the desired position within the waveguide and then locked in place to ensure proper heat conduction between the diode and the cavity heatsink.

In using the "top hat" oscillator cavity, we have found that the diode performance was strongly influenced by the position of the diode and, most important, by the diameter of the bias pin and the impedance of the bias choke. We found early in the contract that the output power from the diodes reached a saturation level which was not caused by excessive junction temperature. The cause of this power limitation is still not exactly known, but it is most likely due to subharmonic oscillations.

Later in the contract a second cavity was designed along the lines proposed by Kurokawa. This circuit is shown in Fig. 11. Much better performance was obtained from it. Figure 12 is a comparison of the power output for the two circuits using the same diode.

When the output power of a diode is stated, it has been corrected for the efficiency of the circuit. In this manner, we obtain the power available at the chip, a quantity independent of the circuit characteristics so that meaningful comparison can be made with different diodes and circuit configurations.

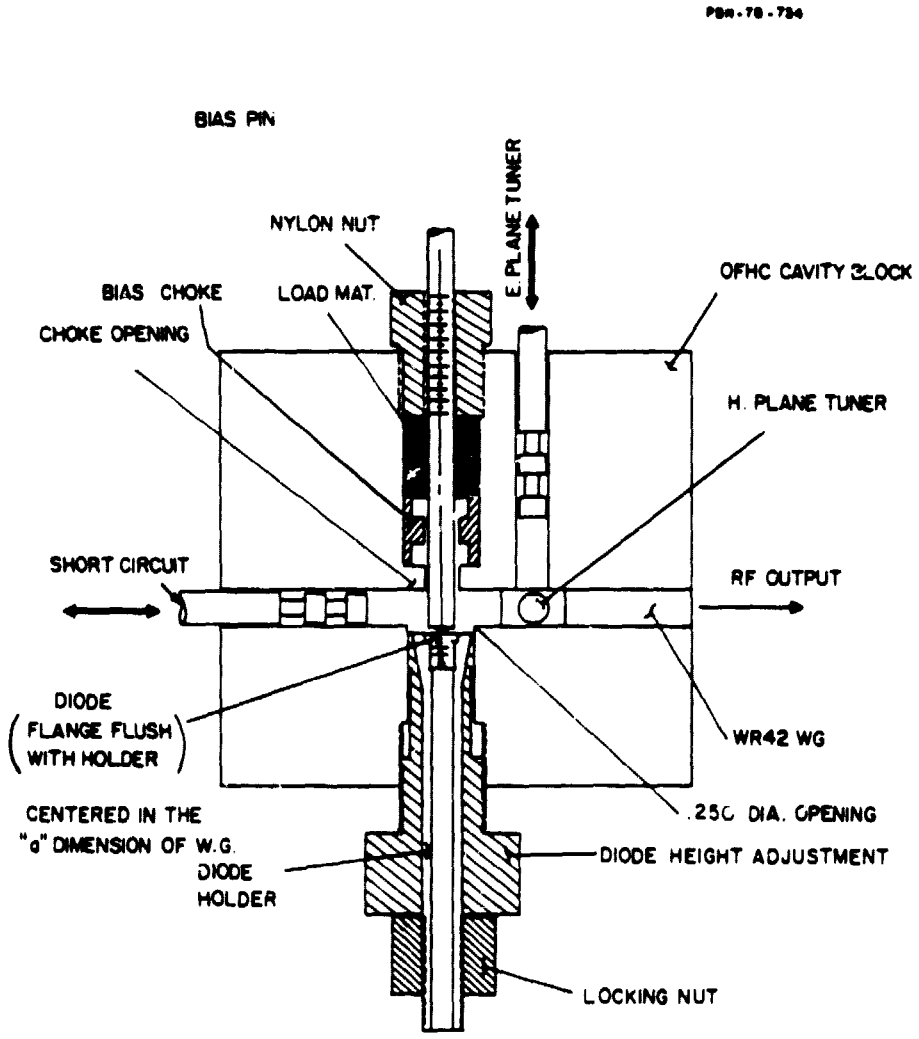

Figure 10. WR42 rf test cavity - top hat.

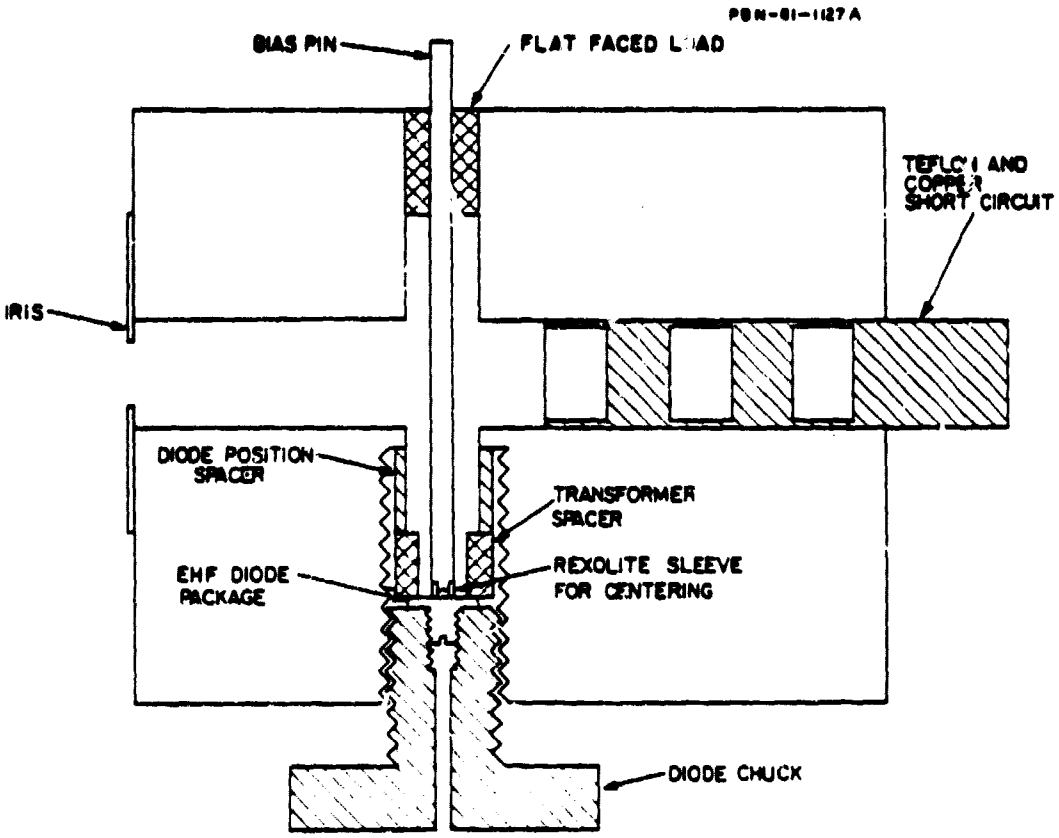

Figure 11. Kurokawa oscillator circuit for diodes in EHF packages.

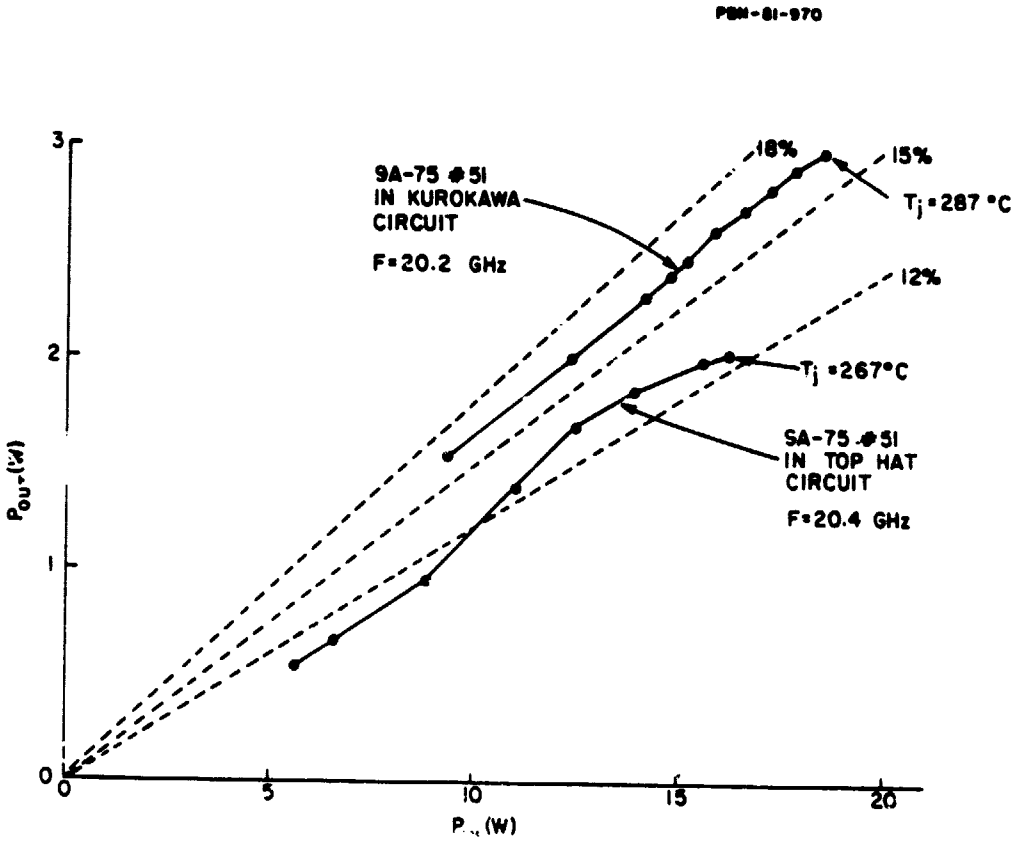

Figure 12. Comparison of the performance of a 20-GHz diode tested in two different circuits.

If the waveguide output of the test circuit is called port 1 and a reference plane in the coaxial line near the diode is called port 2, the efficiency of the cavity is given by:

$$\eta_{ckt} = \frac{|S_{12}|^2}{1 - |S_{22}|^2}$$

For the diodes that were delivered at the end of the contract, the circuit efficiency was about 74 percent. Measurements of circuit efficiency are shown in Fig. 13 for the typical iris sizes used. Table 7 lists the best performance that was obtained from each wafer lot tested.

4.3 Measurements of Diode Parasitics

As Section 6.0 of this report will show, the parasitics associated with the diode can be detrimental to its performance. The series resistance prevents the extraction of the full available power and leads to an optimum diode capacitance, i.e., junction area. The reactive parasitics (inductance of leads and package capacitance) can severely reduce the bandwidth of the circuit in which the diode operates. The diode mount parasitics must also be included. We have devised methods to measure these parasitics so that they can be either reduced or taken into account in the circuit design.

4.3.1 Series resistance

The series resistance of an IMPATT diode is associated with the device's mesa, because of possible undepleted, low-doped residual layers. It is also associated with skin depth effect in high-doped materials and with conduction losses in the leads, packages, and diode mounts (including bias pin contact).

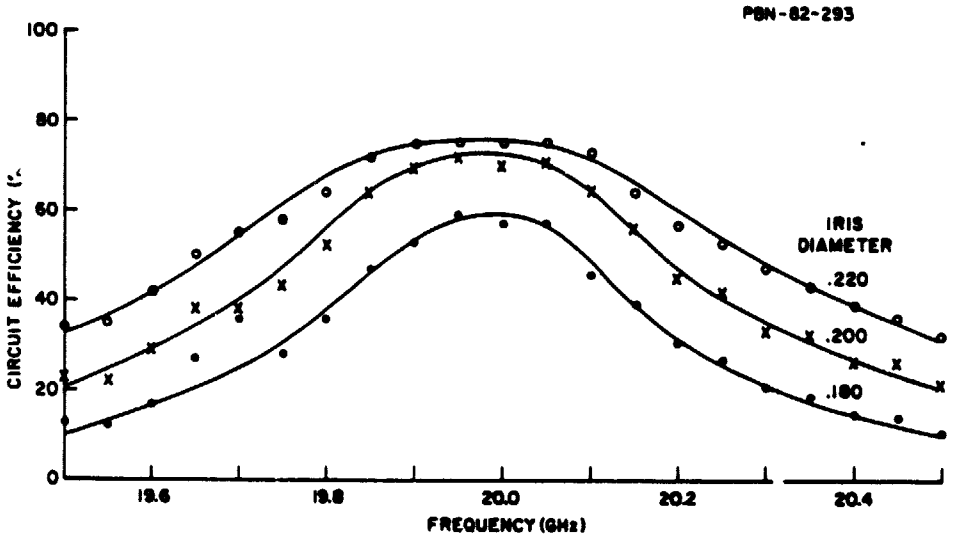

Figure 13. Kurokawa test circuit efficiency.

TABLE 7

SUMMARY OF THE BEST OSCILLATOR RESULTS OBTAINED FROM EACH WAFER

Wafer	P (W)	η (%)	F (GHz)	Mesa Geometry	Heatsink	Circuit*
9A-18	1.17	8.6	19.0	Std Quad	Copper	T.H.
9A-19	0.007	0.04	19.5	Std Quad	Copper	T.H.
9A-33	1.22	9.3	18.2	Std Quad	Copper	T.H.
9A-35	1.46	10.9	18.2	Single	Copper	T.H.
9A-37	0.89	13.1	20.5	Single	Copper	T.H.
9A-75	2.00	19.5	20.4	Std Quad	Copper	T.H.
9A-93	0.74	8.6	19.5	Std Quad	Copper	T.H.
9A-102	1.64	11.8	20.6	Single	Copper	T.H.
9A-103	1.44	9.7	20.9	Std Quad	Copper	T.H.
9A-109	1.7	14.4	21.2	Std Quad	Copper	T.H.
9A-110	1.74	11.5	20.4	Single	Copper	T.H.
9A-111	0.79	8.5	18.4	Single	Copper	T.H.
9A-121	2.4	17.4	20.3	Std Quad	Copper	T.H
9A-153	0.78	7.4	20.1	Single (8 mil)	Copper	T.H.
9A-155	1.39	12.7	21.7	Std Quad	Copper	T.H.
9B-09	1.12	11.7	20.4	Single	Copper	T.H.
9B-19	0.56	7.4	20.6	Std Quad	Copper	T.H.
9B-25	0.90	10.1	20.0	Web Quad	Copper	T.H.
9E-29	2.24	14.2	20.5	Single	Copper	T.H.
9E-30	2.66	15.4	20.4	Single	Copper	K
9E-36	3.19	15.8	19.9	Single	Copper	K
9E-38	2.37	11.2	20.1	Single	Copper	T.H.
9E-39	3.69	14.0	20.2	Single	Copper	K
	4.13	14.4	19.9	Single	Diamond	K (ΔT_j < 250° C)
	5.11	14.5	19.6	Single	Diamond	K (ΔT_j = 275° C)

*T.H. = Top Hat Circuit;
K = Kurokawa Circuit

In a "good" diode, the series resistance is typically 0.1 to 0.2 Ω. In a "bad" diode, it can reach 0.6 Ω. A high series resistance due to an undepleted p-doped layer is thought to be the cause of the low conversion efficiency observed in the fifty diodes delivered to TRW.

We have developed several methods to measure R_s, the series resistance. One method places the diode in a cavity which has either low loss or easily measurable losses. We have constructed two such cavities, one at 1 GHz and the other at 9 GHz. The results obtained in these circuits show that R_s is independent of frequency (at least in the range considered). The results are shown in Figure 14.

In the second method, the complex impedance of the diode and its mount is measured in a network analyzer. A T network is used to represent the transformation between the chip and the measurement plane (Fig. 15). The three elements of the T network are pure reactances. The sum of the diode series resistance and the circuit series resistance (assumed negligible in most cases) is R_L, and the diode reactance is X_L. When Z_{in} is measured for several voltages and with X_L known from low-frequency capacitance measurements, R_L can be calculated. The data at 10 and 17.4 GHz of Fig. 16 were measured by this method, the 1-GHz points by the cavity method.

The third method [6], the simplest to implement, determines the series resistance by measuring the starting current for the diode when it is operated as a power source in an oscillation circuit. The diode bias current is increased from zero, and at each current the circuit tuning is adjusted to establish the current threshold I_{th} where oscillations can be made to occur.

If the circuit is tuned to obtain an external load conductance near zero, the series resistance is given approximately by

$$R_s = \frac{3\alpha'}{\pi \omega^2 C_d^2 \theta} I_{th}$$

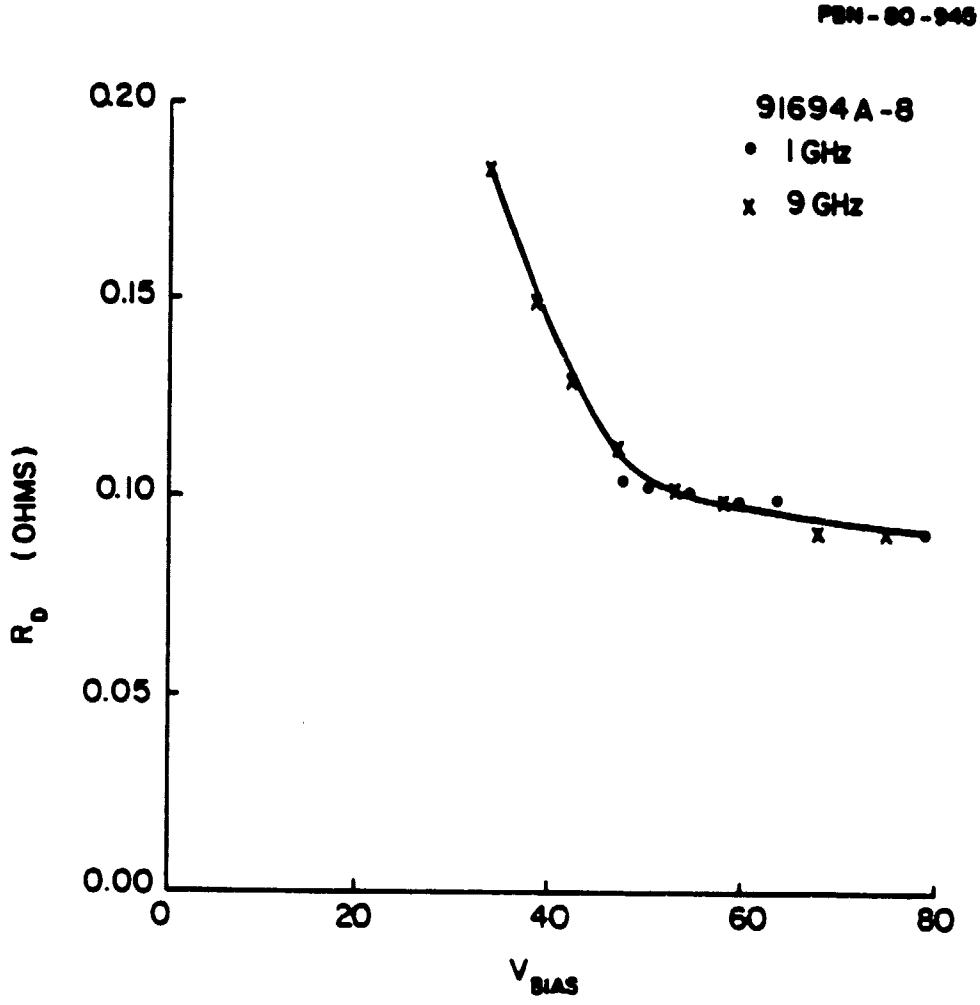

Figure 14. Loss measurements of a diode tested in a 9-GHz and a 1-GHz cavity.

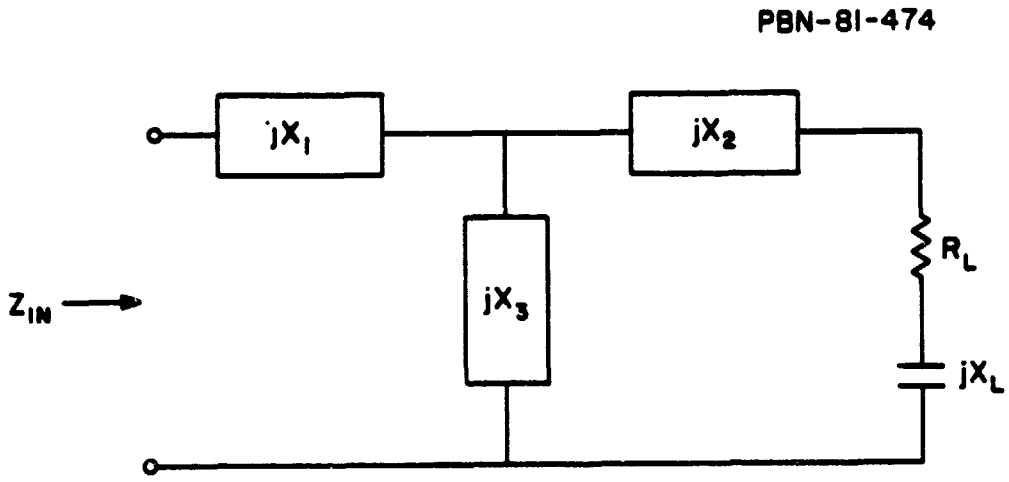

Figure 15. T network used to calculate series resistance.

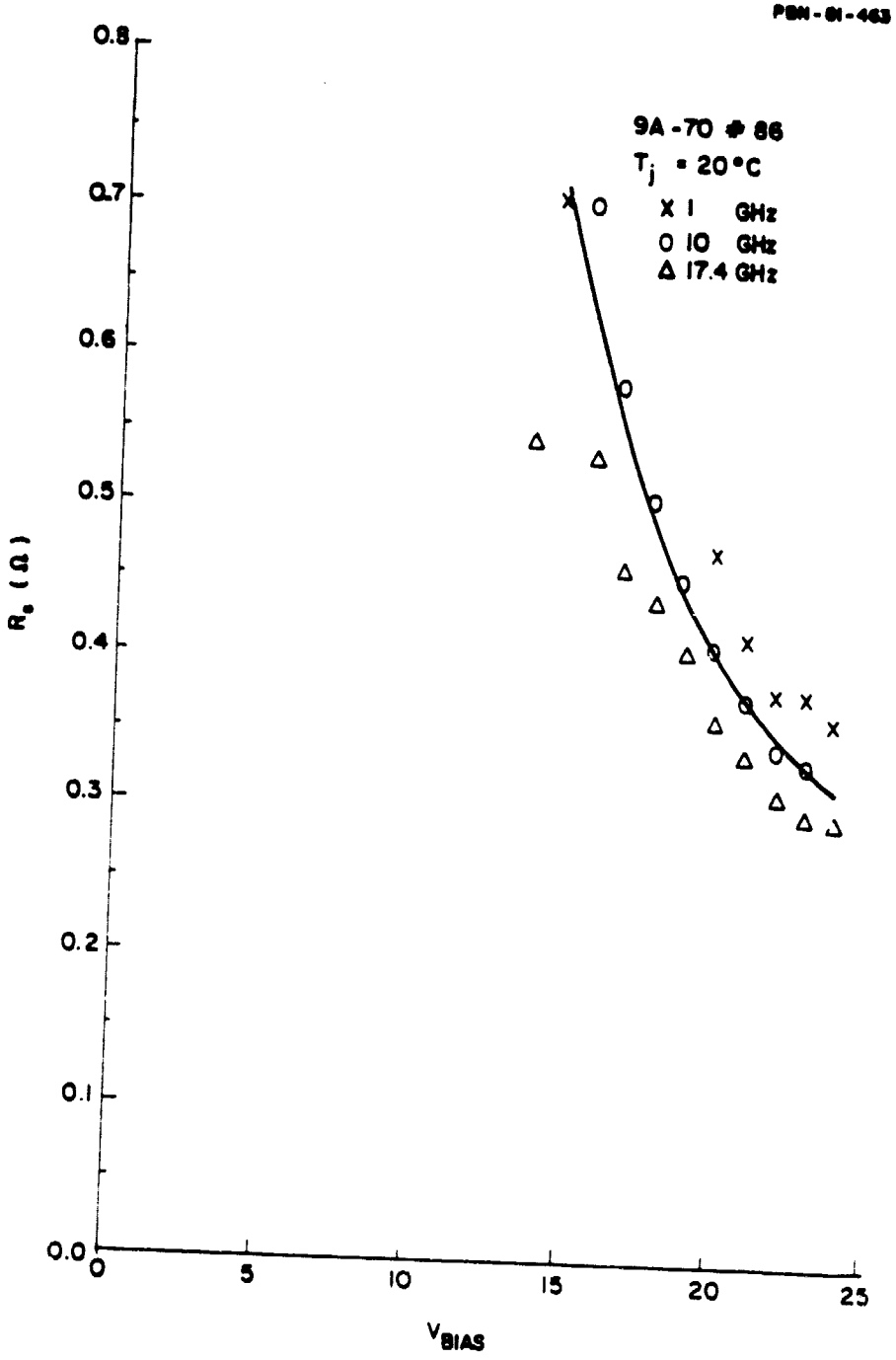

Figure 16. Series resistance of diode 9A-70 #86 vs. bias voltage at three frequencies.

where α' is the first derivative of the ionization coefficient of the material. For GaAs, $\alpha' \underset{\sim}{\sim} 0.22\ V^{-1}$, $\omega = 2\pi f$, with f the frequency of oscillation; C_d is the diode junction capacitance and θ is the drift angle (for an optimized diode $\theta \underset{\sim}{\sim} 0.74\pi$). This method gives results agreeing closely with the others. It has been used routinely in the measurements of the delivered devices.

4.3.2 Parasitic reactances

The parasitic reactances associated with the diode package can severely limit the bandwidth of the circuit in which the device is used, since they form a first step in the impedance transformation. The parasitics associated with the diode mount (bias pin and transformers) should also be included. The equivalent circuit of the diode is given in Fig. 17, together with a drawing of a typical matching structure.

A four-mesa diode with 0.0125 in. center-to-center mesa spacing requires a ceramic inside diameter of 0.050 in., while for the single-mesa chip this can be reduced to 0.014 in. If the parasitics associated with the large package were too great, diodes of the lower thermal resistance could not be used in a broadband amplifier. To test for this limitation, each of the two packages and circuit mount parasitics in a Kurokawa circuit were represented by a double L-network, as shown in Fig. 17. The lumped elements were determined by curve-fitting broadband S-parameters using known transformers. The results are shown in Table 8.

The effect of these parasitic reactances on amplifier bandwidth can be seen from the impedance loci at the reference plane of the diode cap, as shown in Fig. 18. The gain is inversely proportional to the vector separation of the diode and measured circuit locus. For both the large and small packages, the frequency dispersion in this data is dominated by the Kurokawa cavity resonance and not the dispersion due to the package parasitics.

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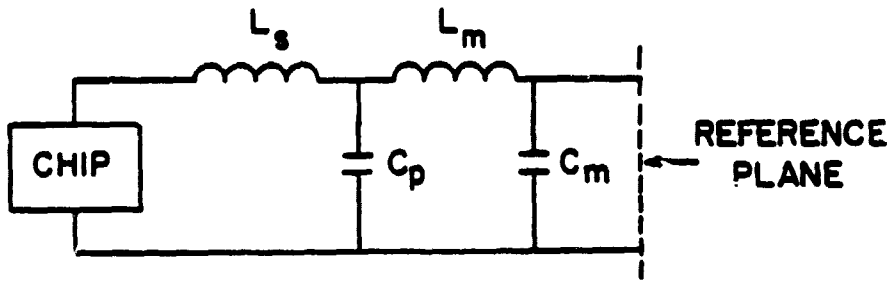

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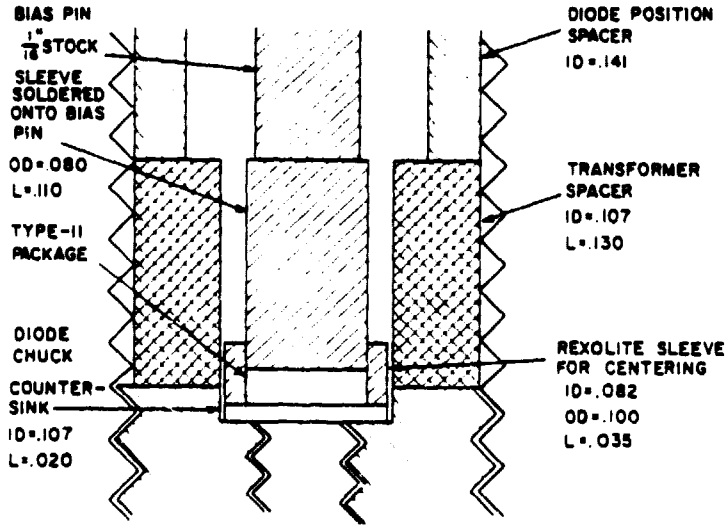

Figure 17. Equivalent circuit and mechanical drawing of a packaged diode in a coaxial mount.

TABLE 8

PACKAGE CHARACTERISTICS

Package Type	OD (mils)	ID (mils)	h (mils)	C_m (pF)	L_m (nH)	C_p (pF)	L_p (nH)
Large (11)	80	50	20	.07	.11	.44	.03
Small (EHF)	30	14	6	.09	.05	.14	.02

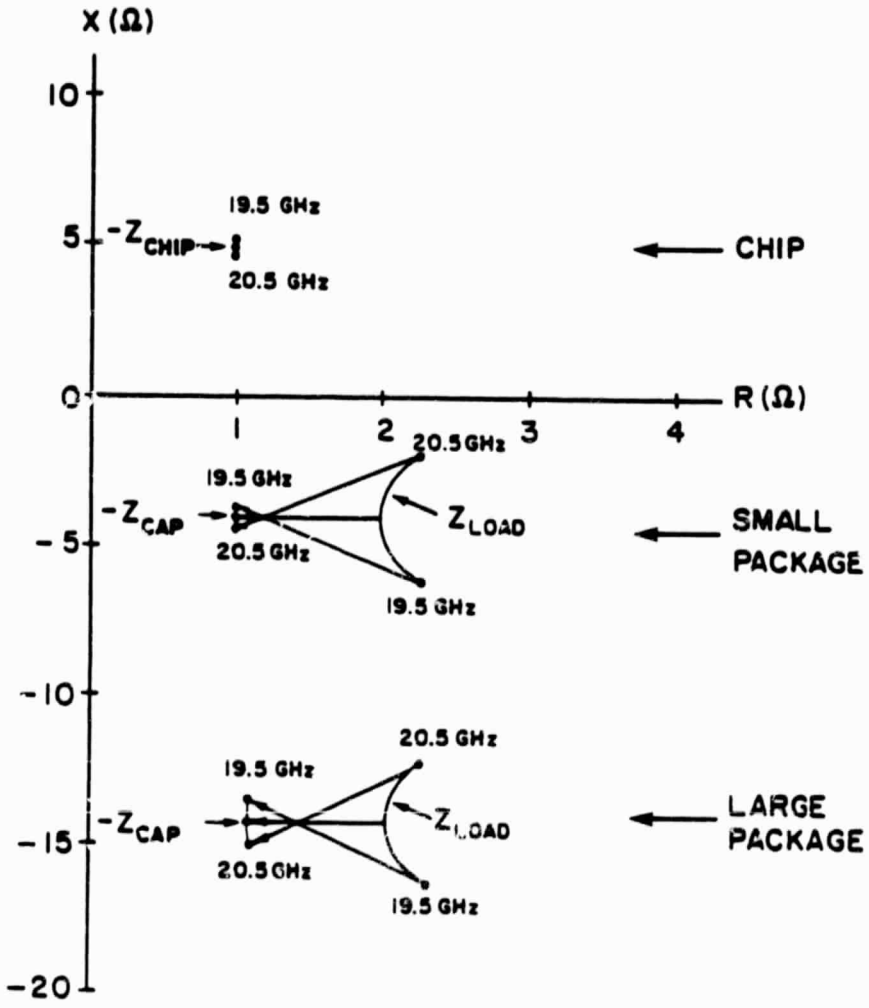

Figure 18. Comparison of the effect of package parasitics on bandwidth for the small and large package.

Indeed, much of the dispersion in the diode characteristic is due to the chip capacitance itself. It is concluded that there need not be a trade off between amplifier bandwidth and thermal design.

4.4 Diode Deliveries

Several diode lots were delivered to TRW during the course of this contract. A first lot of twenty-five diodes was prepared and tested. The average power output for this lot was 1.48 W, ranging from 1.07 to 2.07 W, with a conversion efficiency at an average of 10.6 percent, varying between 6.9 and 15.1 percent. The device junction temperature rises ranged from 111°C to 238°C, showing that they were not pushed to their maximum capabilities. These diodes had four mesas on a thick-plated heatsink, soldered in a Type 16 package.

The second diode delivery of twenty-five diodes was taken from two different wafers: 9A-75 with quadrimesa devices mounted in Type 16 packages with copper heatsinks and 9A-37 made into single-mesa devices with beam leads which were mounted in EHF packages, also with copper heatsinks. The thermal resistance varied from 16 to 18°C per watt for the multimesa diodes, while for the single-mesa diodes we measured a thermal resistance between 20 and 30°C per watt. The average power output for this delivery was 1.6 W (1.37 W minimum, 2.0 W maximum), and the average conversion efficiency was 15.8 percent (12.0 minimum, 19.5 maximum).

The third delivery of diodes was composed of twenty-one quadrimesa chips from wafers 9A-84 and 9A-121. They were soldered in Type 11 packages with copper heatsinks. The average output power of this lot was 1.86 W (1.4 W minimum, 2.4 W maximum) with an average conversion efficiency of 14.4 percent (12.0 minimum, 16.7 maximum).

After the third delivery, the contract effort was redirected by TRW to fabricate fifty diodes, single-mesa with beam lead, with tight tolerances on

the breakdown voltage ($V_B \pm 1$ V) and the junction capacitance ($C_{V_M} \pm 0.05$ pF). The diodes were to be taken from one wafer and thermocompression-bonded to a diamond heatsink in an EHF package. Unfortunately, the material grown for this delivery was not optimum, giving lower conversion efficiency, and we did not have time to go to an additional iteration, if we were to meet our deadline.

Fifty diodes were delivered to TRW as required. The average power gererated at the chip was 3.71 W with a standard deviation σ of 0.21. The conversion efficiency had an average value η = 13.04 percent with σ = 0.72. The diodes were tested in a Kurokawa circuit with an efficiency of 74 percent. The average thermal resistance for these packaged diodes was 9.8°C per watt, with σ = 0.49. The average junction capacitance was 1.30 pF, σ = 0.05, and the average breakdown voltage was 31.67 V, σ = 0.79.

5.0 DIODE RELIABILITY

5.1 Introduction

Device reliability problems can be greatly alleviated by giving appropriate attention to the material growth processes and diode fabrication technology during the diode development effort.

We can efficiently measure operating lifetimes of ten years (approximately 10^5 hours) only through accelerated-stress life testing. This technique applies operating conditions qualitatively similar to those encountered in actual field service to a population of devices under test, but it uses an increased stress level (normally the diodes' operating junction temperature) to induce failures within a relatively short interval. We then use statistical analysis of the failure data obtained under high-stress conditions to project lifetime under ordinary operating conditions.

A particular case may not satisfy all of the assumptions implicit in the use of accelerated-stress life test data for lifetime projections. First, for the projection to be valid, the same failure mode must be dominant over the range of stress levels used in life tests and at the stress level encountered in normal operation. Second, this failure mode must be thermally driven according to the Arrhenius rule. The rate at which the aging process leading to failure proceeds must vary as $\exp[-E_a/kT]$, where E_a is the "activation energy" for the process, k is Boltzmann's constant, and T is the absolute operating temperature. In a given case, however, the failure process may not be one of constant activation energy, and lifetime projections based on this assumption will be invalid.

Certain mathematical techniques can confirm the presence of a single failure mode governed by the Arrhenius rate equation within a particular temperature range. Semiconductor failures produced by a single mechanism have generally shown a log-normal distribution of failure times, with standard deviations, σ, typically 1 to 2 for mature fabrication processes. A plot on

C - 3

probability paper of cumulative percentage of failures vs. operating time at a given temperature yields a straight line if a log-normal distribution exists. The presence, so demonstrated, of a small-variance log-normal failure distribution at a particular operating temperature suggests a single failure mode. However, we need further confirmation, so we observe the variation of the median time to failure (MTTF) and the standard deviation as functions of temperature. If a single failure mode is dominant over a particular temperature range, the failure distribution will remain log-normal with constant standard deviation over this temperature range. Further, the median time to failure will vary as $\exp[+E_a/kT]$ if the Arrhenius rule applies. That is, if log[MTTF] is plotted against 1/T, we obtain a straight line with slope dependent upon the activation energy.

Figures 19 and 20 show how we apply these in a particular case. Figure 19 shows failure data derived from a long-term burn-in on a test lot of GaAs X-band IMPATT diodes. Except for one initial turn-on failure, all failures plotted fall close to a straight line on the probability paper, indicating a log-normal distribution under the test condition used (T_j = 270°C). Further, the absence of a set of "freak" or "sport" failures not characteristic of the main log-normal distribution, together with the relatively small standard deviation, suggests a single failure mode resulting within a mature fabrication process. The linear plot of log[MTTF] against 1/T (Fig. 20) indicates a thermally activated failure mode following the Arrhenius rule. An extrapolation (dashed line) of the experimental data gives values of MTTF at lower temperatures.

Erroneous conclusions can result from extrapolating high-temperature failure data (Fig. 20) to obtain operating lifetime or MTTF data at lower temperatures. While we can verify statistically the presence of a single, dominant failure mode within a given temperature range, statistical analysis alone does not guarantee that this failure mode will still be dominant outside the measured temperature range. Other failure modes, driven by factors other than temperature (e.g., operating current density) may become dominant at lower temperatures.

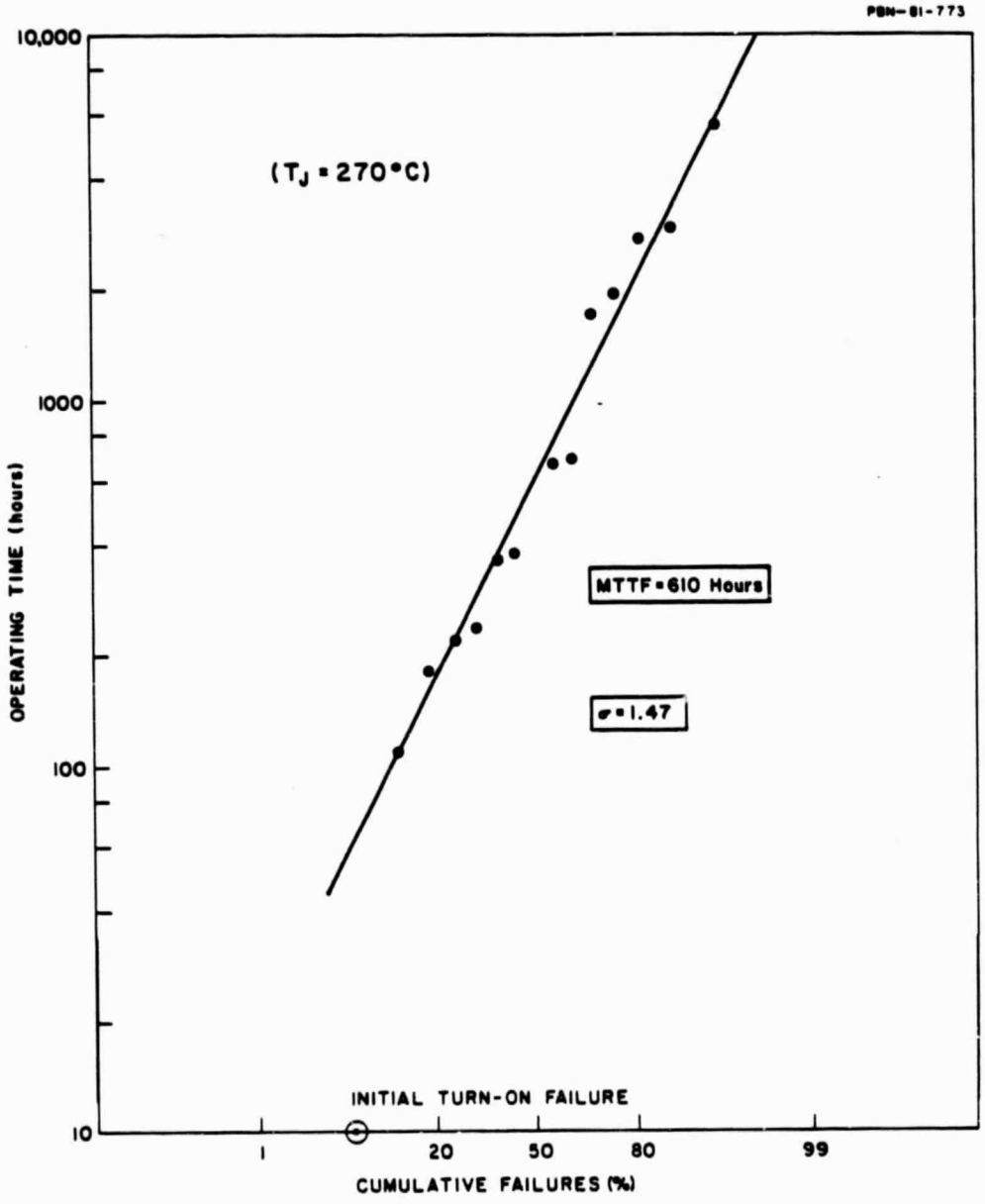

Figure 19. Operating time vs. cumulative failure percentage for test lot of GaAs X-band IMPATT diodes.

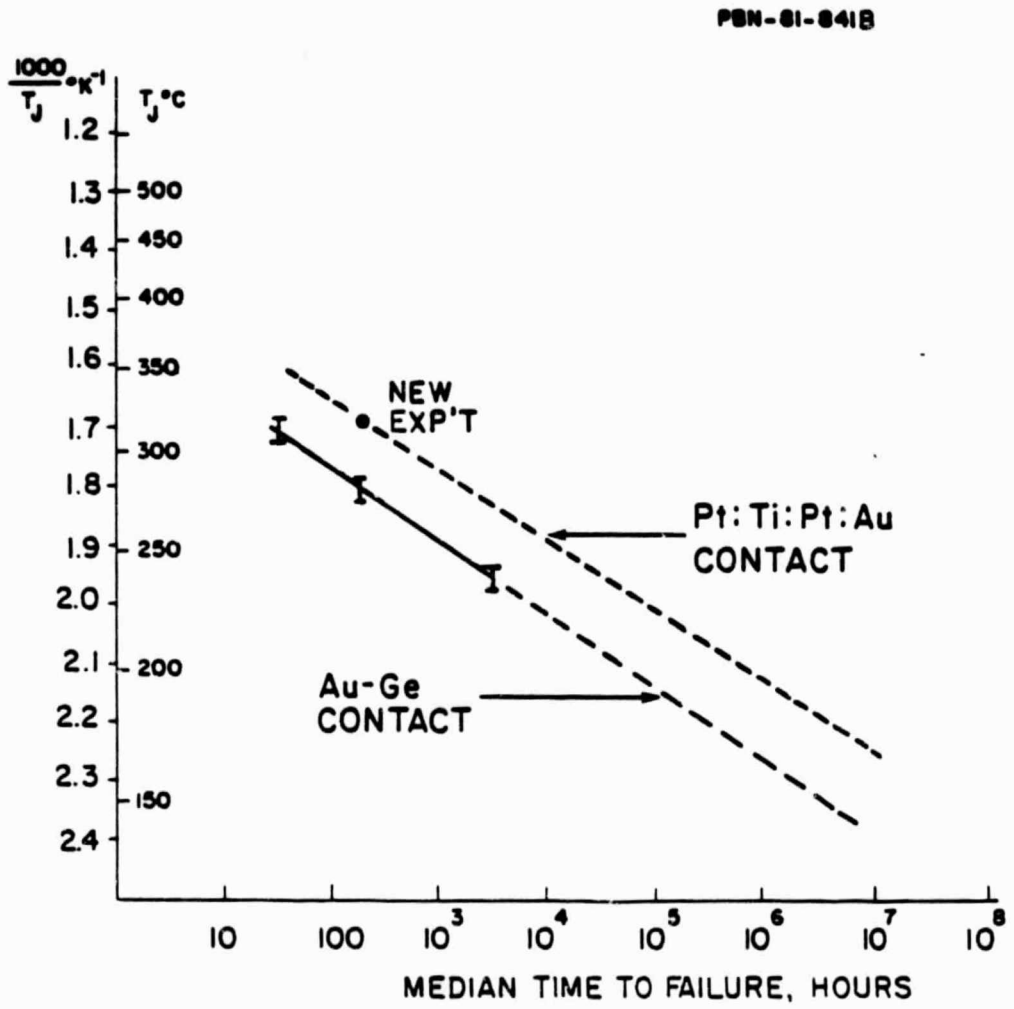

Figure 20. Illustrative data for median time to failure of a test lot of GaAs X-band IMPATT diodes for different operating temperatures. This data is also valid for the 20-GHz diodes.

Extrapolation to obtain MTTF data at lower temperatures is more credible if we complete a physical analysis of failed diodes. If one can show that the same physical process is responsible for failures in the accelerated stress life test as in normal operation, the extrapolation is probably valid.

5.2 Test Conditions for Device Burn-In

Selection of the test conditions to be used for device burn-in is one of the first steps in any reliability study. Ideally, the test conditions should closely approximate those in actual operation. Unfortunately, the cost of building a multiplicity of oscillator or amplifier circuits for use in these tests limits the number of devices which can be evaluated. One must usually be content with a small sample of devices in an rf test along with a larger sample in an alternative (but less expensive) test.

The simplest alternative test involves a high-temperature oven bake of the diodes being evaluated. Large numbers of diodes can be studied at low cost. However, this test is unrealistic in two ways. First, the device is placed at a uniform elevated temperature. In actual operation, significant internal temperature gradients are developed as heat flows from the heat-generating portions of the device to the external heatsink. The pattern of thermal stress in the oven bake is thus very different from that developed in actual operation. Second, certain failure mechanisms (e.g., electromigration of contact metalization), while thermally enhanced, depend on the presence of the electric fields and currents which occur in normal operation. This stress is absent in the oven bake. For these reasons, we do not consider lifetime data derived from oven baking of high-power-density semiconductor devices to be useful for predicting actual operating lifetime.

A second alternative test, a burn-in with dc operating bias applied, represents a good compromise between the conflicting requirements of realistic test conditions and low cost of test implementation. Here, thermal gradients and electric field and current distributions are similar to those in actual operation, especially when the device being tested normally operates at small-signal levels. The IMPATT diode, however, is a large-signal device. In rf

operation, peak fields and current densities exceed those produced by dc bias alone. Further, the flow of rf current may produce additional heating of the device, along with a temperature distribution somewhat different from that generated by the dc bias. One might expect that the dc bias test, because it places slightly smaller stresses on the device, would produce slightly optimistic lifetime data. However, our tests of X-band IMPATT diodes have indicated close correlation between dc and rf burn-in results.

Two techniques are commonly used for setting the stress level in dc burn-in of IMPATT diodes. In the first, one applies normal operating current to the device under test while controlling the heatsink temperature to produce the desired junction temperature. For accelerated-stress life testing, the required heatsink temperature may exceed 200° C. In the second technique, heatsink temperature is fixed or adjustable over only a narrow range, and bias current is increased as necessary to produce the desired junction temperature. In accelerated stress life tests, bias currents and consequently power dissipation levels substantially larger than those used in normal operation may be required to produce the desired junction temperature. Stresses produced by thermal gradients or by the flow of current are then greater at a given junction temperature than those produced by normal bias current with an elevated heatsink temperature. Of the two dc techniques, the first is somewhat more expensive to implement, while the second is likely to produce more pessimistic results. We have generally used the second technique in our reliability testing.

5.3 Reliability Test on 20-GHz Diodes

Twenty diodes (wafer 9A-155, Type 16 package) have been subjected to accelerated-step stress tests. The initial test temperature was 230°C, and each step increased the temperature by 25°C after 24 hours until all the diodes failed. The junction temperature (T_j) was adjusted by varying the dc power applied to the diodes while the heatsink was maintained at a constant 30°C.

The failure data was normalized for T_j = 305°C using an activation energy of 1.9 eV, which we know to be correct for the metalization system used. The

results are shown in Fig. 21. After early failures which would normaily be detected and eliminated during rf tests, the diode population is segregated into two groups. The first one can be removed by burn-in. Subjecting the devices to a temperature of 280°C for 70 hours would eliminate this type of failure. There remain the rest of the diode population for which we can get a mean time to failure (MTTF). The solid curve in Fig. 21 considers the total diode population, while the dashed curve considers only the group after burn-in. An Arrhenius plot of MTTF vs. $1/T_j$ is shown in Fig. 22. At junction temperatures near T_j = 200°C, the MTTF is greater than 10^4 hours. It is interesting to note that this curve reproduces results measured on completely different devices using the same metalization (compare Figs. 22 and 20). The failure mode has been traced to a gallium migration in the region of the Au-Ge contact on the upper side of the diode. By changing the metalization system to include a diffusion barrier (Pt:Ti:Pt), the reliability of similar devices has been improved by at least one order of magnitude (new experiment point in Fig. 20). This new metalization system has been used in all the IMPATT diodes fabricated after concluding the experiments. In particular, all fifty diodes delivered to TRW for inclusion in the P.O.C. amplifiers have Pt:Ti:Pt contacts.

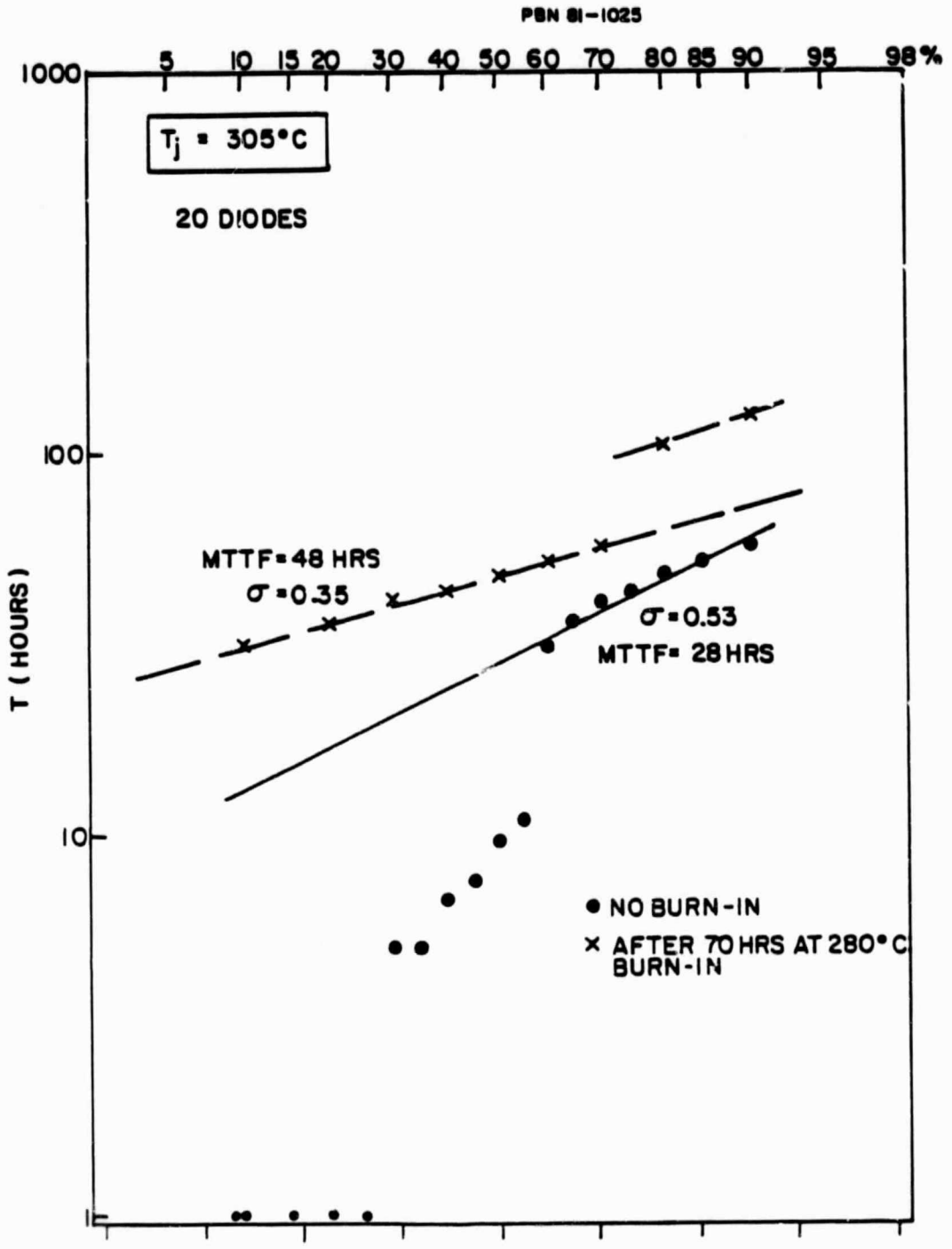

Figure 21. Calculated lifetime of K-band diodes at T_j = 305° C obtained from accelerated-step stress tests.

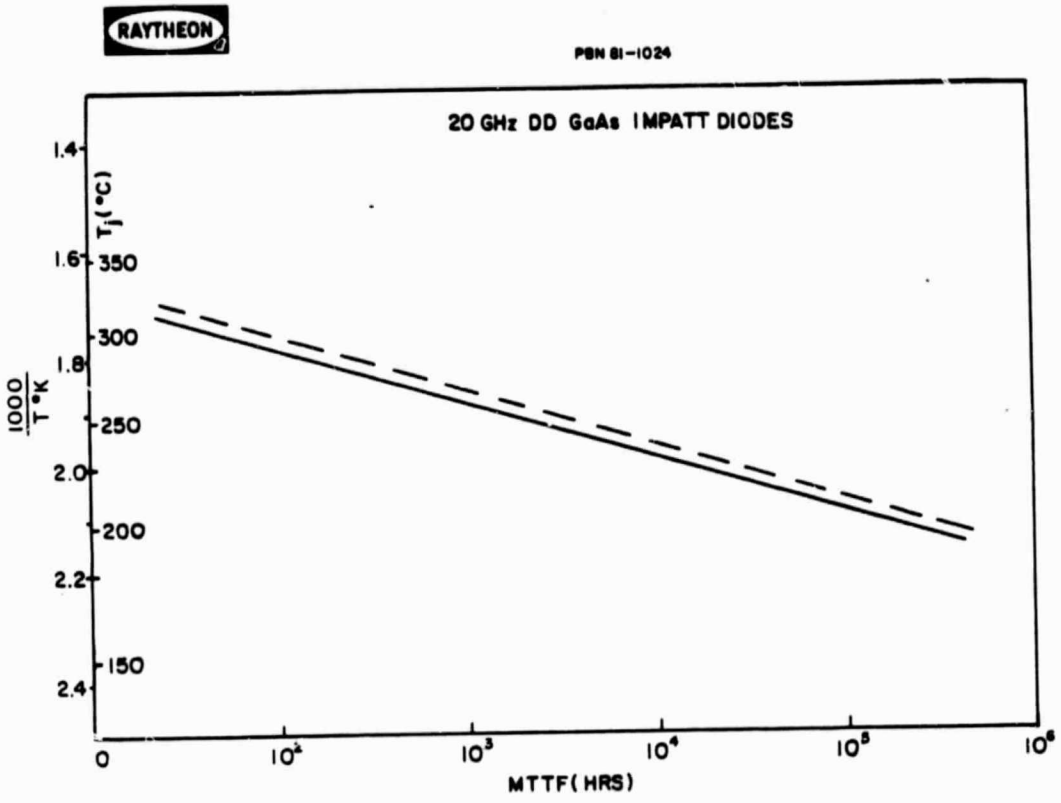

Figure 22. MTTF vs. $1/T_j$ for K-band diodes.

6.0 DIODE DESIGN AND MODELING

6.1 General Model

Our progress toward high power and efficiency has been greatly aided by our ability to model diode microwave characteristics [1],[2] and identify the important parameters which influence device performance. The key elements in achieving high power and efficiency are development of the following:

1. A diode doping profile which permits a high ratio of rf voltage for operating dc voltage prior to rolloff in negative conductance.

2. A material and fabrication technology which results in the lowest possible value of parasitic series resistance.

3. A chip and package design which will result in the lowest possible value of thermal resistance.

These parameters are intimately interrelated. In the sections which follow, we give the major features of our model and show how we can separately measure each of the important device parameters in given wafers and diodes.

Figure 23 shows the simplest diode-circuit combination. The diode is represented by a parallel combination of a negative conductance, G, and a capacitive susceptance, B; in series with this combination is a series resistance, R_s. The circuit, which includes the package parasitics, transformers, couplers, and load, is assumed to consist of a resonating inductance, L, and a load, g_l. The magnitudes of G and B are functions of dc bias, junction area, material parameters, and rf voltage amplitude, V_{rf}.

At sufficiently high V_{rf}, G will decrease with further increase in V_{rf}, so that once an oscillation has started from noise, V_{rf} will grow as long as the net conductance at the load is negative. In the presence of finite R_s, the conductance at the load will be decreased by R_s, and will have an effective value given by

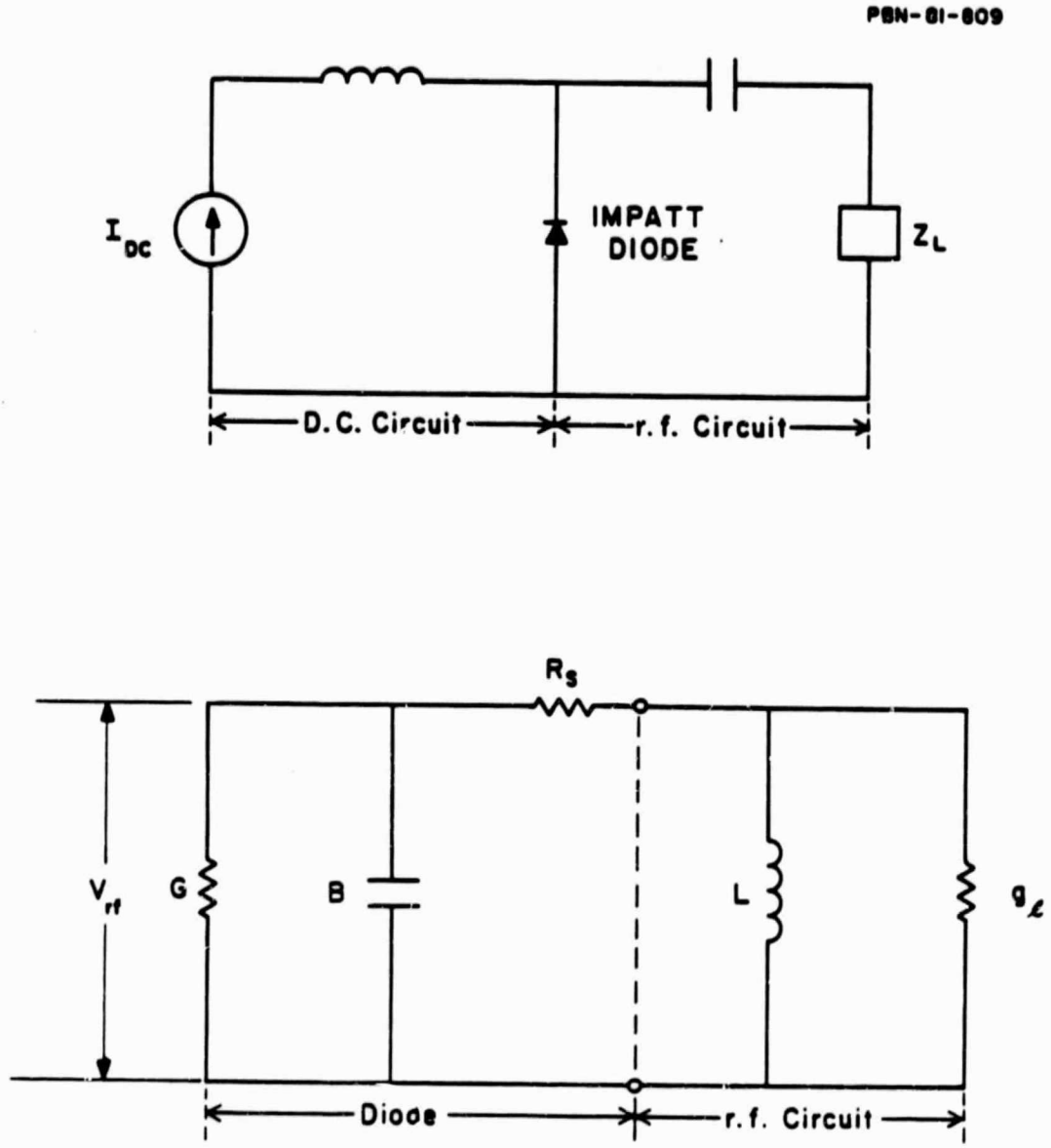

Figure 23. IMPATT diode equivalent circuits.

$$G' = \frac{G(1 + R_s G + R_s B^2)}{(1 + R_s G)^2 + R_s B^2} \approx G + R_s B^2 \ . \qquad (1)$$

The condition for stable oscillation is when

$$G = -g_\ell \text{ and } B = \frac{1}{\omega L} \ . \qquad (2)$$

The power delivered to the load is

$$P_{out} = \frac{1}{2} g_\ell \, V_{rf}^2 = \frac{1}{2} (|G| - R_s B^2) V_{rf}^2 \ . \qquad (3)$$

Equation (3) is basic to our analysis. To determine the output power for any set of material parameters or bias conditions, we must calculate G and B and have knowledge of V_{rf}. For a given bias condition, the relationship between G, B, and V_{rf} determines the optimum circuit tuning, since tuning the circuit while maintaining a constant frequency changes V_{rf} through tighter or weaker coupling. Thus an increase in g_ℓ will not increase P_{out} if V_{rf} drops too much. Likewise, a drop in g_ℓ to increase V_{rf} might give a reduced P_{out}.

Figure 24 shows a typical set of calculated conductance contours for a 20-GHz diode. Superimposed on these curves are sections of the measured curves at various dc bias currents. The locus of points giving constant power output, that is, satisfying Eq. (3), constitutes the set of straight lines on the graph. The oscillator operating point is the intersection of the power contours with the admittance curves. It can be seen that, in the absence of a mechanism limiting V_{rf}, an arbitrarily large power can be obtained. However, there must clearly be a limit to V_{rf}, since it cannot exceed the dc operating voltage of the diode. The experimental contours A through E indicate that there is indeed such a limit. In the range of 20-25 V for the K-band diode, the magnitude of the negative conductance drops precipitously. It can be seen from the figure that the effect of a finite series resistance, R_s, is to reduce the magnitude of $|G|$.

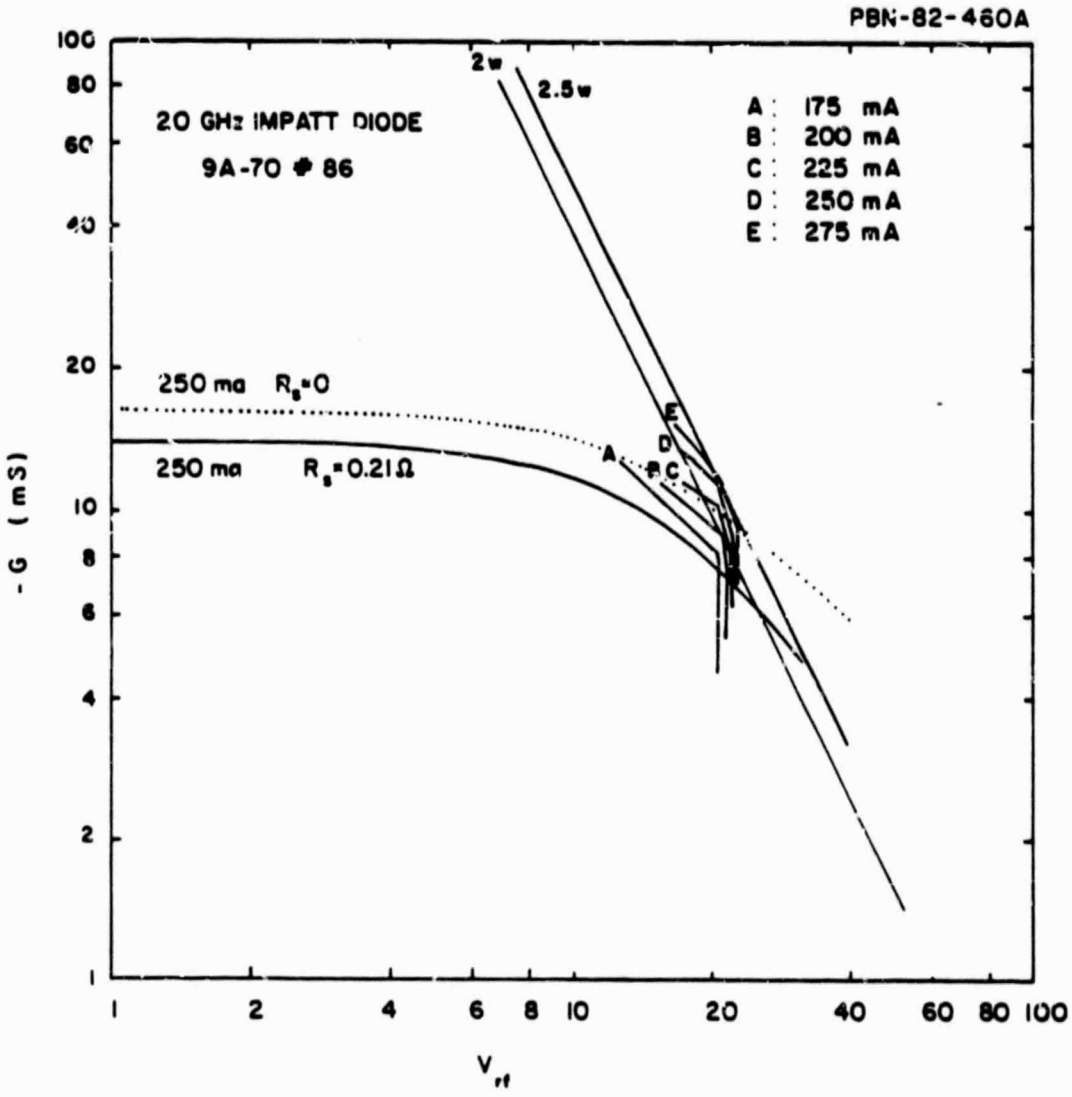

Figure 24. Negative conductance vs. rf voltage for diode 9A-70 #86.

We will later discuss possible causes of a rapid fall-off in $G'(V_{rf})$. One is the eventual domination of the term $R_s B^2$. Pushing the knee in G' to the highest possible value of V_{rf} is one good reason to minimize R_s in the device design. In GaAs K-band devices, the knee in G' occurs well before $R_s B^2$ causes an abrupt decrease in $G'(V_{rf})$; but, as will be shown, the term $R_s B^2$ still significantly reduces G' at typical operating values of V_{rf}.

To calculate G and B as functions of dc bias, rf voltage, material parameters and temperature, we use the Read diode model applied to a double-drift diode [3]. We determine the conduction current at the boundaries of the avalanche zone from the equation

$$\tau_i \frac{\partial I_{ca}}{\partial T} = (\alpha \ell_a - 1) I_{ca} + I_{sat} , \tag{4}$$

where τ_i is the intrinsic avalanche response time in GaAs [4], [5], α is the effective ionization coefficient, ℓ_a is the avalanche zone width, I_{ca} is the conduction current, and I_{sat} is the reverse saturation current. We have measured I_{sat} extensively as a function of temperature in K-band diodes. The results of this measurement will be discussed later in this section in connection with parametric instability. We note here only that at the temperatures of interest, I_{sat} can be neglected compared with the other terms in Eq. (4).

Solving Eq. (4) for the conduction current and adding the displacement current across the avalanche zone capacitance, we obtain the total diode current at the fundamental frequency. The space-charge voltage resulting from the conduction in the drift region is then calculated by twice integrating Poisson's equation with respect to distance. The total diode current and voltage at the fundamental frequency are then

$$I_D = - \frac{I_1(b)}{I_0(b)} I_{dc} + j\omega_0 C_a V_a \tag{5a}$$

$$V_D = \frac{\ell}{\ell_a} V_a - \frac{I_{dc}}{j\omega_0} \left(\frac{I_1(b)}{I_0(b)} \right) \left\{ \frac{1 + F_N}{C_N} + \frac{1 + F_P}{C_P} \right\} . \tag{5b}$$

In Eq. (5a) and (5b), C_a, C_N, and C_P are avalanche, n-drift, and p-drift capacitances, respectively; I_0 and I_1 are modified Bessel functions of order 0 and 1; ℓ and ℓ_a are the total diode length and avalanche zone width, respectively. F_N is defined as

$$F_N = \frac{\exp(-j\phi_n) - 1}{j\phi_n} , \tag{6}$$

where ϕ_n is the n-drift transit angle. A similar expression holds for F_P. V_a is the voltage amplitude occurring across the avalanche zone. The quantity b is defined as

$$b \equiv \frac{2j}{\omega_0} \left(\frac{\alpha'}{\tau_i}\right) V_a , \tag{7}$$

where α' is the derivative of the ionization coefficient with respect to electric field. V_a is the positive frequency amplitude of the avalanche voltage. The real avalanche voltage is

$$V_a \exp j\omega t + V_a^* \exp - j\omega t . \tag{8}$$

The diode admittance is the ratio (V_D/I_D) and can be expressed conveniently as

$$Y = j\omega C \frac{1 - \left(\frac{\omega_R^2}{\omega^2}\right)}{\left\{1 - \frac{\omega_R^2}{\omega^2} C_d \left[\frac{1 + F_N}{C_N} + \frac{1 + F_P}{C_P}\right]\right\}} \tag{9a}$$

where

$$\omega_R^2 = \omega_a^2 h(b) , \tag{9b}$$

$$\omega_a^2 = \left(\frac{3v_s\alpha'}{\varepsilon}\right)\left(\frac{I_{dc}}{A}\right) , \text{ and} \tag{9c}$$

$$h(b) = \left(\frac{2}{b}\right)\left(\frac{I_1(b)}{I_0(b)}\right) . \tag{9d}$$

Here, v_s is the saturated carrier velocity; I_{dc} is the dc bias current; and A, the device area, is determined from the junction capacitance, C_d.

Some discussion of Eq. (9) is in order. Once the transit angles are chosen to maximize the negative conductance in (9a) through the factors F_N and F_P, and the junction capacitance is fixed, the chip admittance will depend only on the parameter ω_R^2. Equations (9b), (9c), and (9d) show that ω_R^2 depends on factors involving the material constants and dc current through ω_a^2 and the rf voltage amplitude through the parameter b, which increases with increasing V_{rf}. The function h(b) decreases with increasing V_{rf}. Expressing Y = G + jB, we find that the conductance changes sign from negative to positive when ω_R^2 exceeds ω^2. Figure 25 is a plot of G and B vs. ω_R^2/ω^2.

6.2 Diode Doping Profile

The diode conductance at a given bias current is established in a Read diode primarily by the dimensions of the active layers. The influence of the doping profile is mainly on the maximum value of V_{rf} which can be achieved prior to conductance rolloff. The profile-related parameter determining diode efficiency is the modulation ratio V_{rf}/V_{dc}. Values in the range 0.35 to 0.61 are obtained experimentally.

The precise mechanisms which limit V_{rf} are not well understood. We speculate that, at the peak of the rf voltage swing, impact ionization in the drift zone can dephase the terminal current. At the lowest terminal voltage reached during the rf voltage swing, carriers can move out of velocity saturation. Our approach to profile design has been to establish an electric field distribution within the diode where the electronic field in the drift zone is midway between these limits.

A schematic representation of a double-Read profile appears in Fig. 26. The electric field control spikes are positioned symmetrically around the junction and spaced by about 0.3 μm. Each of the n-type and p-type drift

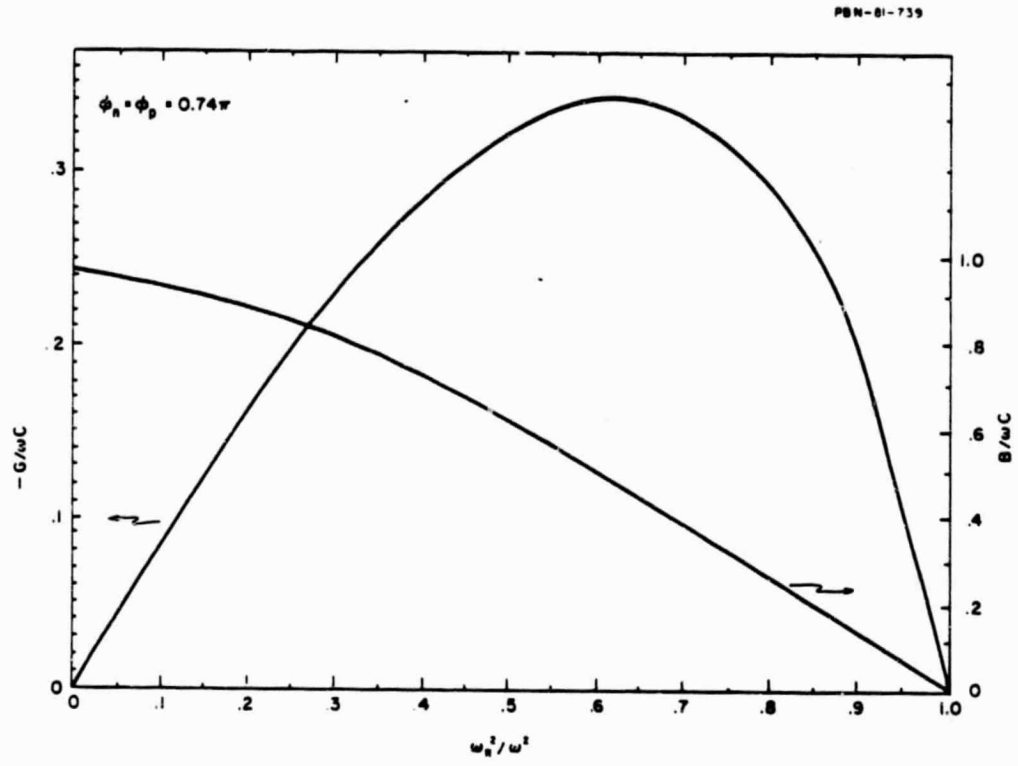

Figure 25. Negative conductance, G, and capacitive susceptance, B, vs. ω_R^2/ω^2.

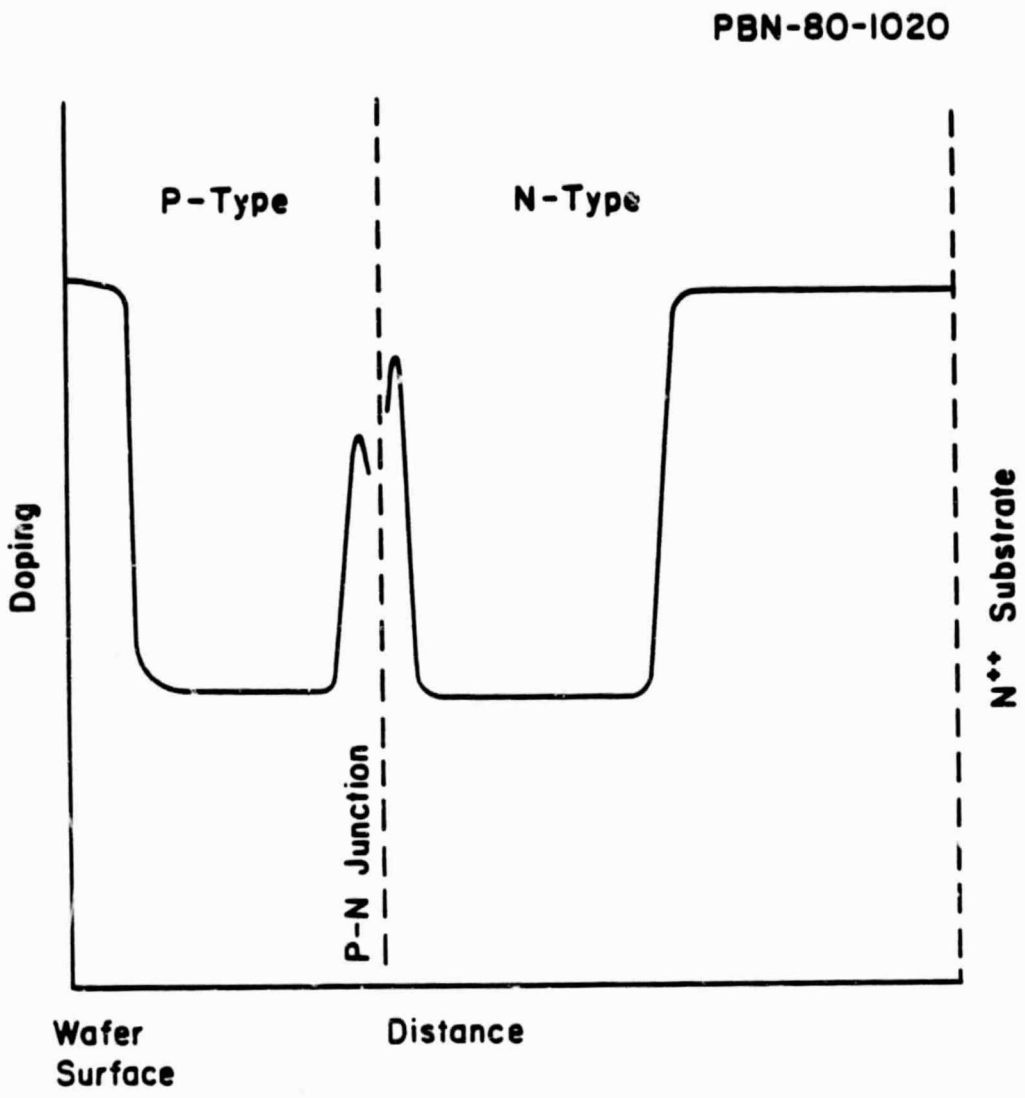

Figure 26. Double-drift Read doping profile.

layers is approximately 0.8 μm wide. The resulting electric field distribution for the model profile is shown in Fig. 27. The change in the electric field distribution, neglecting space charge due to the rf terminal voltage swing, is also indicated. Over the range of terminal voltages shown, the electric field remains nonzero at the drift zone contacts, minimizing the series resistance effects of undepleted semiconductor.

In the model profile shown, the total charge in the p-side field control spike is specified to be smaller than that on the n-side. This was done because p-type undepleted semiconductor would be more detrimental, and high tolerances on Q_p during wafer growth are difficult to achieve (e.g., K-DDR-4). In subsequent profiles, these spikes were taken to be more symmetrical. When we increase the charge in the p-spike, it cannot be made too large or excess series resistance will result from absence of punchthrough conditions. An undepleted layer can result in a specific resistance $R \sim 0.7\ \Omega/\mu m$ in diodes with $C_d = 1.3$ pF.

An example of this is given in Fig. 28. The figure shows the effect of increasing charge in the p spike across a wafer. The series resistance was measured by the threshold method [6] at 20 GHz at room temperature. We believe that the trend toward higher values of R_s at the lower breakdown voltages is due to undepleted p-drift material near the contact. The series resistance is lower for the high-breakdown-voltage diodes. However, since all diodes from this lot had a maximum $V_{rf} \simeq 20$ V, the higher operating voltages for those diodes with higher values of V_B resulted in lower modulation ratios, ~ 0.38, and lower efficiency.

In the next section, we show the relationship between series resistance and thermal resistance in determining diode output power and efficiency.

6.3 Electrical and Thermal Resistance

Excess series resistance can severely reduce diode efficiency even for diodes with a high modulation ratio. This occurs because the circulating

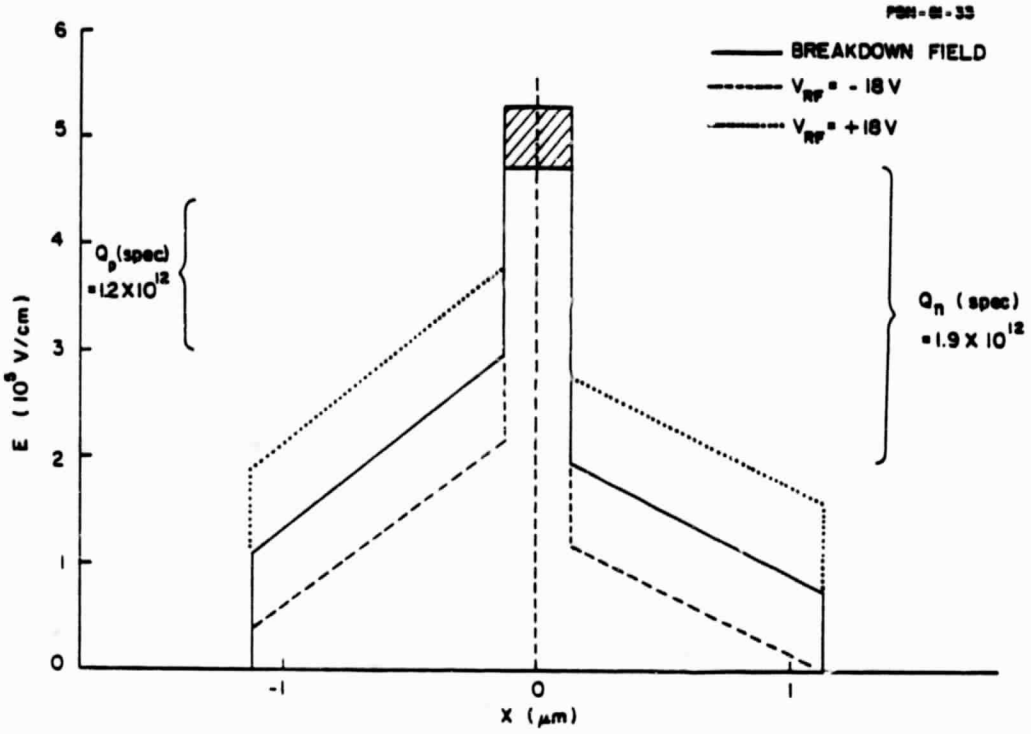

Figure 27. Electric field profile for a diode having the K-DDR-2 doping profile.

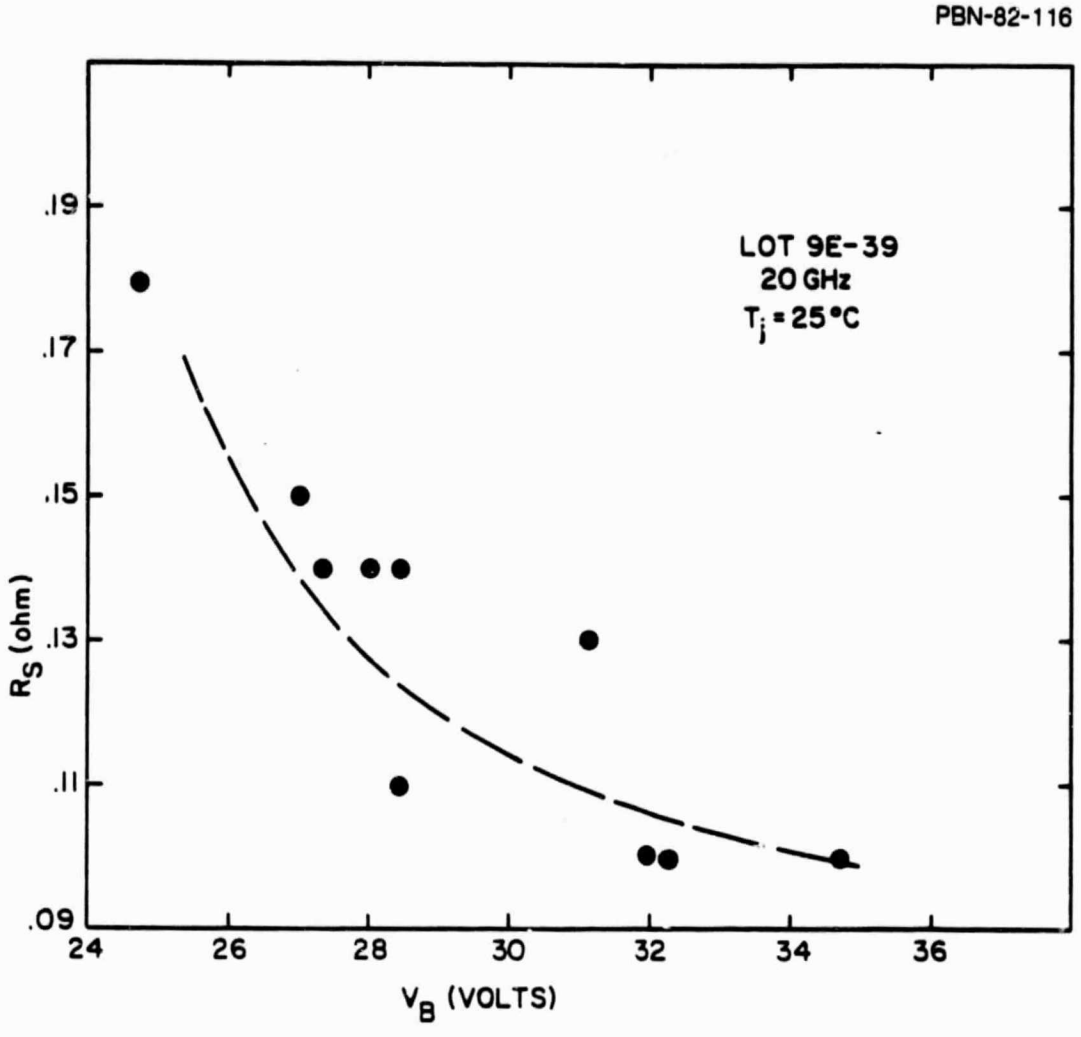

Figure 28. Series resistance vs. breakdown voltage for one diode lot.

reactive current, $B \cdot V_{rf}$, must flow through R_s, producing a power loss $1/2\ R_s(B \cdot V_{rf})^2$. Since $B \approx 2\pi f \cdot C_d$, the effect becomes more severe in large-area, high-junction-capacitance devices for a given R_s. This is illustrated in Fig. 29, where output power vs. junction capacitance is calculated at 225°C for modulation ratio 0.5 and different values of R_s. The terminal resistance is a function of junction capacitance, since $\theta \propto A^{-\frac{1}{2}}$. Hence, as the junction capacitance increases from zero, the dissipated and input power can increase and so does the power output. In the case $R_s = 0$, the power output would continue to increase monotonically. However, for $R_s \neq 0$, the effects mentioned above cause the power to fall eventually. The result is an optimum capacitance, as shown in Fig. 29.

The thermal resistance chosen in the example is characteristic of a beam-leaded single-mesa diode on a diamond heatsink. Higher output power may be achieved using a multimesa diode on diamond, but this approach was not pursued, since such a diode could not be used in the TRW circuit.

To choose an optimum junction capacitance, we used calculated curves such as those of Fig. 29 along with separately measured values of R_s. The diodes delivered during the program had junction capacitance $\sim$ 1.2 pF and R_s in the range of 0.1 to 0.2 Ω.

One of the methods used to determine series resistance is to curve-fit measured output data, as in Fig. 30. This figure shows the sensitivity of the fit to R_s with assumed $\approx$ 0.5 modulation index. The data was taken in a top hat circuit, so that there is some power saturation evident above the 2-W level. The theoretical power curves are most sensitive to R_s in their $P_{out} = 0$ intercept. The slopes of the curves are more closely related to the modulation index. A summary of calculated values of R_s for lot 9A-70 is given in Table 9.

Figure 29 shows that for each value of R_s there is an optimum junction capacitance for maximum output power at T_j = 225°C. In Fig. 31, we plot the set of optimum junction capacitances at T_j = 250°C for four diode thermal designs.

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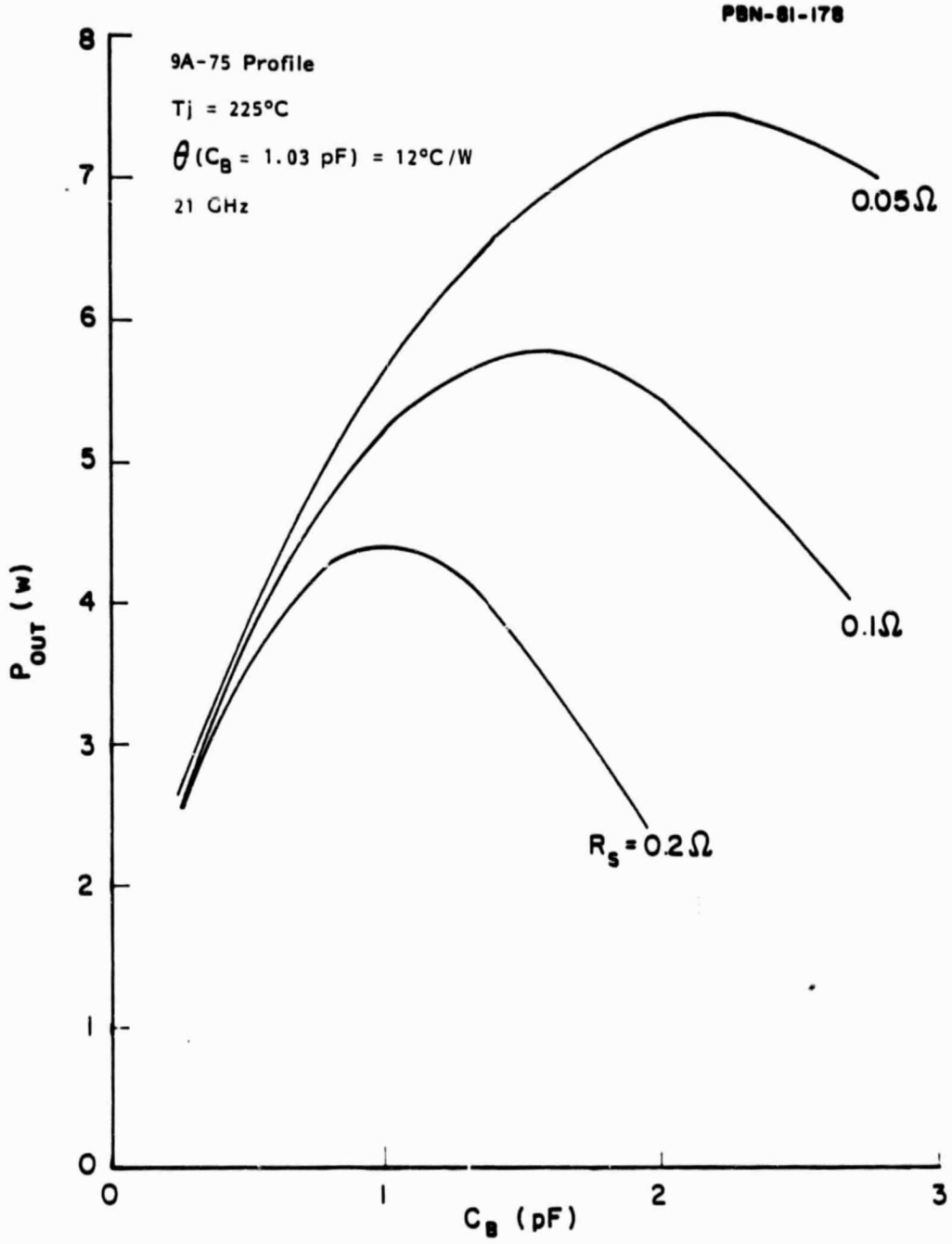


Figure 29. Output power vs. junction capacitance for a K-band diode with low thermal impedance. The diode series resistance is shown as a parameter.

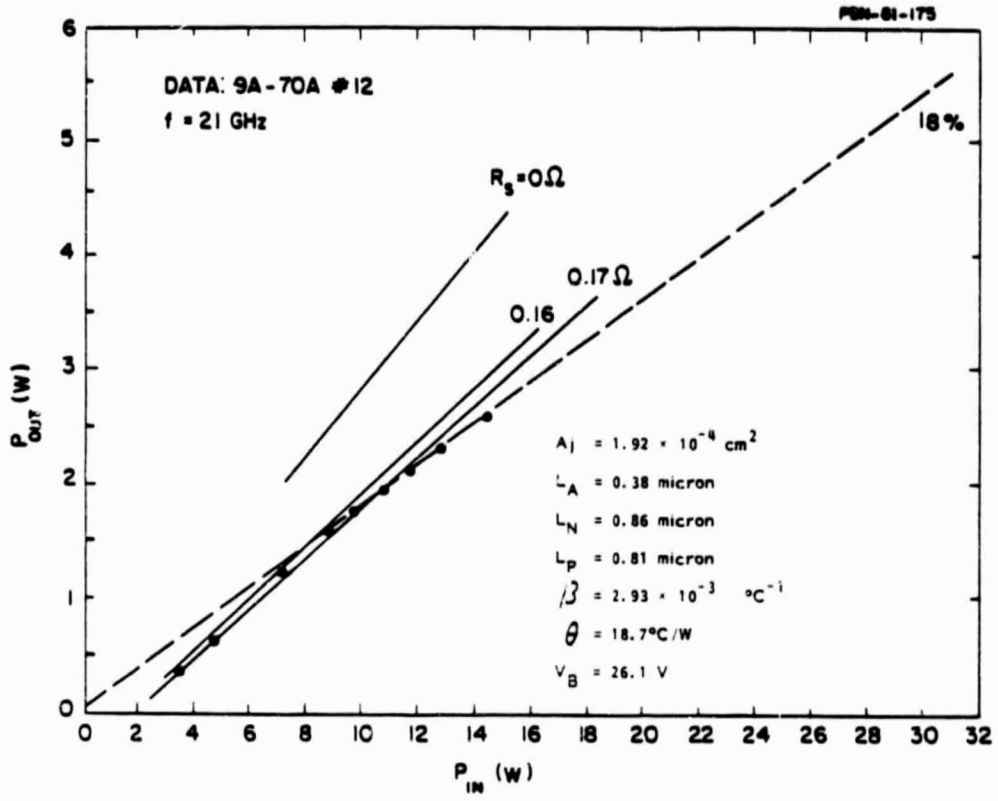


Figure 30. Output power vs. input power for a diode from lot 9A-70. The solid lines are calculated values. The points are measured data.

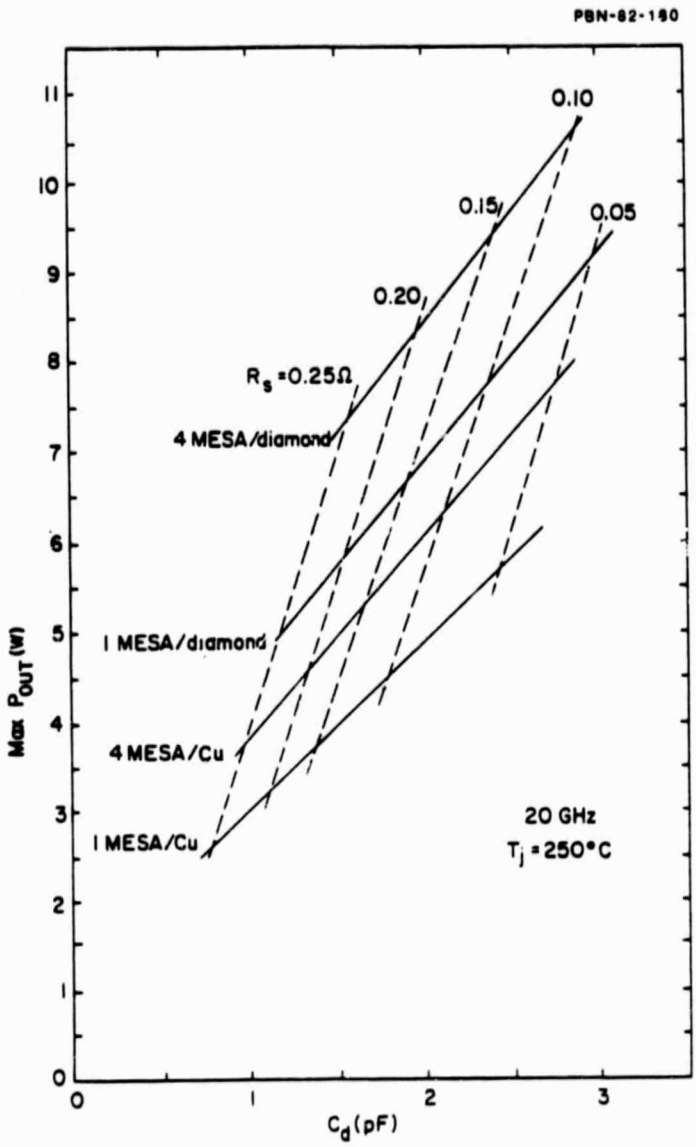


Figure 31. Optimum junction capacitance for maximum output power calculated for four diode thermal designs with series resistance as a parameter.

TABLE 9

SERIES RESISTANCE FROM PERFORMANCE DATA - 20 GHz

Diode No. 9A-70	MEASURED					CALCULATED	
	C_B (pF)	T_J (°C)	P_{OUT} (W)	η (%)	V_{DC} (V)	V_{DC} (V)	R_s (Ω)
35	0.91	180	1.85	19.1	43.0	42.4	0.21
19	0.97	151	1.60	18.3	43.7	43.7	0.18
59	0.99	138	1.67	20.2	41.3	40.6	0.15
12	1.03	189	2.16	19.8	45.2	46.1	0.17
14	1.10	179	2.35	19.3	44.0	44.2	0.16
04	1.14	148	1.60	16.0	44.5	44.3	0.19

The advantage of four-mesa [7] diamond-heatsink [8] chips is evident in Fig. 31. The lower thermal resistances permit larger-area diodes, since the associated higher bias currents increase relative to B^2R_s. For realistic values of $R_s = 0.15\ \Omega$, it can be seen that 9 W CW can be obtained from the four-mesa diamond-heatsink chip. This estimate must be tempered somewhat because of circuit tuning limitations, since it might prove difficult to match a 20-GHz diode with $C_d > 2$ pF. At 1.3 pF, the power output would be about 8 W at $T_j = 250°C$ with 19 percent conversion efficiency. We have again assumed a modulation ratio of 0.5.

As noted earlier, our development effort in this program was directed at a single-mesa beam-leaded device in a small diamond package. With such a chip, a thermal resistance of about 9.8°C per watt was routinely achieved. This is the value expected from extrapolation of our millimeter-wave diode results, as shown in Fig. 32. With such a device, power output of 3.5 to 4.0 W at the chip is obtained at $T_j = 250°C$.

6.4 Parametric Instability

In practical circuits, it is sometimes difficult to use input power levels up to the thermal limits of the diode. This difficulty is due to the onset of subharmonic oscillation and bias circuit instabilities. Either or both of these phenomena have lead to premature power saturation and irregular output spectra at around the 3-W power output level in the top hat circuit.

Subharmonics occur when the device exhibits negative resistance at a frequency ω_1 and ω_2 where $\omega_1 + \omega_2 = \omega$. Subharmonics are often observed in the output spectra of diodes oscillating with relatively high efficiency, but calculations [9] show that their presence can result in substantially reduced power output.

Bias circuit instability occurs when there is negative resistance at very low frequencies that are improperly terminated in the bias circuit. The effects of parametric oscillations are illustrated in the current and voltage

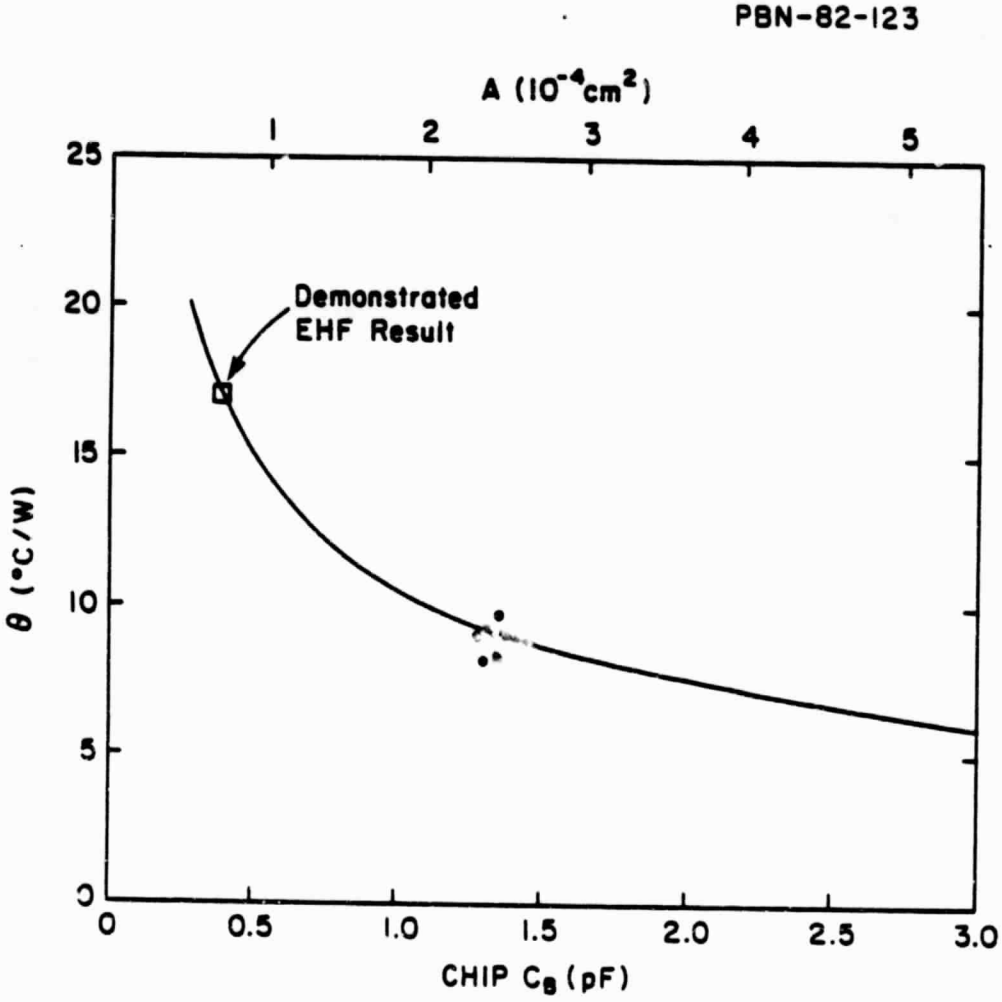


Figure 32. Measured thermal resistance of 20-GHz diodes of lot 9E-39 mounted in diamond heatsink packages.

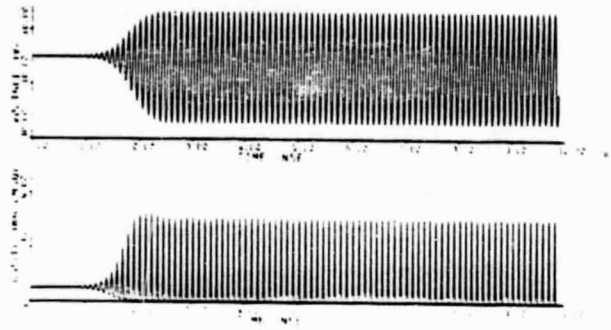
waveforms of Fig. 33 [9]. In normal oscillation, the current and voltage reach a clean steady-state value following a few rf cycles. When a subharmonic is present, alternate cycles have underdeveloped current amplitudes. Bias circuit oscillation can give a modulation envelope which severely reduces the time average (output) power.

Subharmonics can sometimes be reduced or eliminated by increasing the bias circuit capacitance, but there is then the problem of inducing bias circuit oscillations which result in modulation of the rf waveform with a low frequency envelope (1-100 MHz), thereby greatly reducing the average output power.

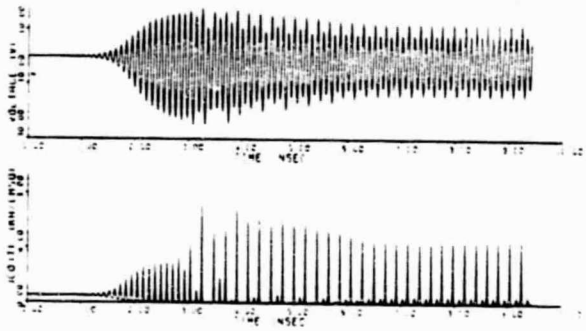
In the output spectra of 20-GHz diodes, we observed that low-frequency, broadband components increased strongly near the power saturation bias levels. The increase in baseband noise and observation of bias circuit oscillations at about the same input power level suggest that improperly terminated negative resistance may be occurring at frequencies from 40 MHz upwards. Analysis of the operating voltage of diodes oscillating below the power saturation threshold shows positive dc space charge resistance with $R_{sc} \sim 20\ \Omega$. The positive value of R_{sc} would be expected to persist to frequencies much higher than 40 MHz, that is, to frequencies where transit time effects are still unimportant.

6.4.1 Bias circuit instability

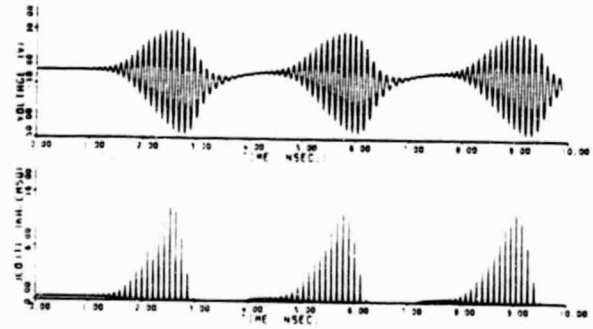
Usually [10], bias circuit instability is associated with a high reverse saturation current, I_{sat}, and a high fundamental frequency rf voltage, V_{rf}. To check whether I_{sat} becomes important at power input levels above power saturation, we made two measurements on typical diodes. Since I_{sat} is a strong function of temperature, and since temperature changes with power input, I_{sat} vs. T was measured as shown in Fig. 34. At temperatures near the operating point, $I_{sat} \sim \exp(E_g/2kT)$, typical of generation current emanating from the active volume of the device. At lower temperature, avalanche multiplication and diffusion current become important and increase I_{sat} above the generation current levels. At 5-V bias, the high-temperature asymptote is reduced, since the device is not fully punched through. The highest values of I_{sat} obtained (near 250°C) were $\sim 10\ \mu A$.



(a) Normal oscillation.



(b) Half frequency subharmonic.



(c) Bias circuit oscillation.

Figure 33. Caiculated diode current and voltage waveforms.

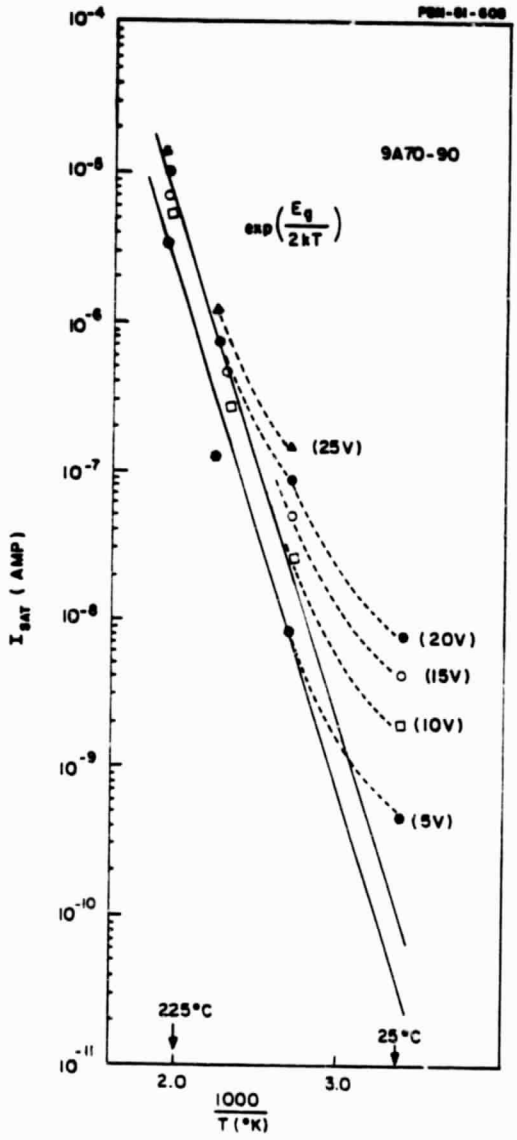


Figure 34. I_{sat} *vs. temperature for a 20-GHz IMPATT diode with bias voltage as a parameter.*

This value was used together with results of pulsed oscillator measurements to conclude that I_{sat} is not a significant cause of bias circuit instability. Figure 35 shows the results of pulsed power measurements on a diode nominally similar to that used for the I_{sat} data.

Three duty cycles (20%, 40%, 60%) and CW are used. At each power input, the temperatures are widely different, with temperature rise scaling roughly in proportion to duty factor. At each temperature, power saturation was observed between 16 and 18 W input levels, even though I_{sat} had a total spread of about four orders of magnitude between the end point temperatures. Furthermore, even in the CW case where $T_j = 306°C$, $(I_{sat}/I_{dc}) \sim 3 \times 10^{-4}$. A criterion for negligible I_{sat} is

$$\frac{1}{\omega\tau} \frac{I_{sat}}{I_{dc}} << 1$$

and this parameter is $\sim 2 \times 10^{-3}$, a value too small to overcome the 20 Ω of positive space charge resistance.

It is significant that at a given input power the efficiency increases with duty cycle. Since input current and hence negative conductance decrease with increasing duty cycle, and since series resistance R_s probably increases with increasing temperature, it may be concluded that the higher efficiency results from greater V_{rf} with higher temperatures. Such effects are also observed fo diodes operating at higher frequencies.

Our understanding of contributions to both the positive and negative space charge resistance remains incomplete, as evidenced by the discrepancy between expected and measured R_{sc}. Table 10 shows the average values of measured, non-oscillating dc space charge resistance for five lots of 20-GHz diodes. Calculated values are $R_{sc} \sim 8$ Ω, assuming negligible change in the breakdown field at the junction due to space charge at the junction.

To confirm that there is indeed negative resistance at baseband frequencies, we conducted a pulsed experiment. The data show that when diodes are oscillating under large-signal conditions at 20 GHz, and the dc bias current

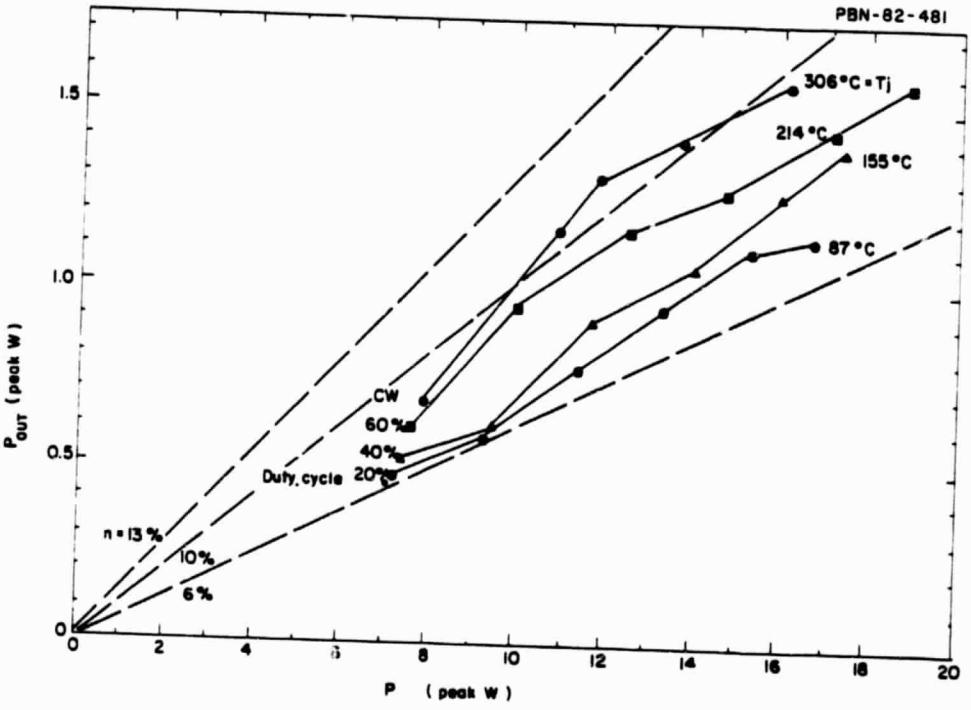


Figure 35. Diode 9A-75 #42 - peak power out vs. power in.

is sufficiently large, there is an incremental dc negative resistance which extends upwards in frequency.

TABLE 10

AVERAGE VALUES OF NON-OSCILLATING DC SPACE CHARGE RESISTANCE

Lot #	Diodes Tested	Average R_{sc} (Ω)
9A-75	19	21.1
9A-70	4	17.3
9A-81	9	15.7
9A-93	4	14.1
9A-111B	3	16.0

It is not likely that this negative resistance is a thermal relaxation effect, since the upper frequency limits of the effect appear to be too high to correspond to a thermal time constant. Furthermore, the negative resistance appears to be uniform for an extended pulse of up to a few microseconds. At present, our feeling is that the negative resistance observed is somehow related to the anomalously high value of non-oscillating space charge resistance of Table 10.

To eliminate the spurious baseband oscillations, we have attempted to characterize and then to modify the low-frequency termination as seen from the diode position in the top hat circuit. Two variations in bias choke arrangements were tried. However, both circuits exhibited power saturation. Attempts to reduce the local capacitance were also unsuccessful in altering the power saturation effect. We finally made progress by operating the devices in a Kurokawa circuit with an entirely different bias circuit arrangement.

6.4.2 Subharmonic instability

As noted earlier, we suspect that power saturation at 20 GHz occurs at a threshold that can be related to subharmonic instability. Measurement of amplifier gain as a function of rf drive at a fixed bias current sometimes

shows a sharp decrease in gain and an associated onset of f/2 subharmonic.

To investigate the connection between these two effects, we have extended the stability analysis of Hines [11] and Schroeder [12] to GaAs double-drift diodes at 20 GHz. The theory has been used to analyze a diode from lot 9A-70 operating into an idealized Kurokawa circuit. The calculation shows that the power levels at which an f/2 instability occurs are comparable to those at which saturation in power output at 20 GHz is observed. This will be shown in detail below.

The model takes the diode operating in an amplifier mode, as shown in Fig. 36. A pump signal is present at angular frequency ω_p and the system is subjected to a perturbation signal at ω_0. The diode is divided into avalanche and drift zones, each with its own shunt capacitance. The avalanche zone is the nonlinear element described by the Read equation

$$\frac{di_{ca}}{dt} = \left(\frac{\alpha\ell - 1}{\tau_i}\right) i_{ca} \qquad (10)$$

The drift zone is connected in series with the avalanche zone and the conduction currents are derived from the differential equation for drifting charge

$$\frac{\partial n(x,t)}{\partial x} + \frac{1}{v_s}\frac{\partial n(x,t)}{\partial t} = 0 ,$$

the definition of conduction current,

$$i_c(x,t) = q\, v_s\, n(x,t)$$

and the boundary conditions that $i_c(0,t) = i_{ca}(t)$. The circuit impedance is $Z_c(\omega)$. The sum of the voltages around the circuit must vanish.

These conditions imply a set of loop currents at all harmonics of ω_p and at frequencies $n\omega_p \pm \omega_0$ where n = 0, 1, 2, ... In the approximation where only ω_0, $\omega_p - \omega_0$ and ω_p are kept as frequencies having finite current

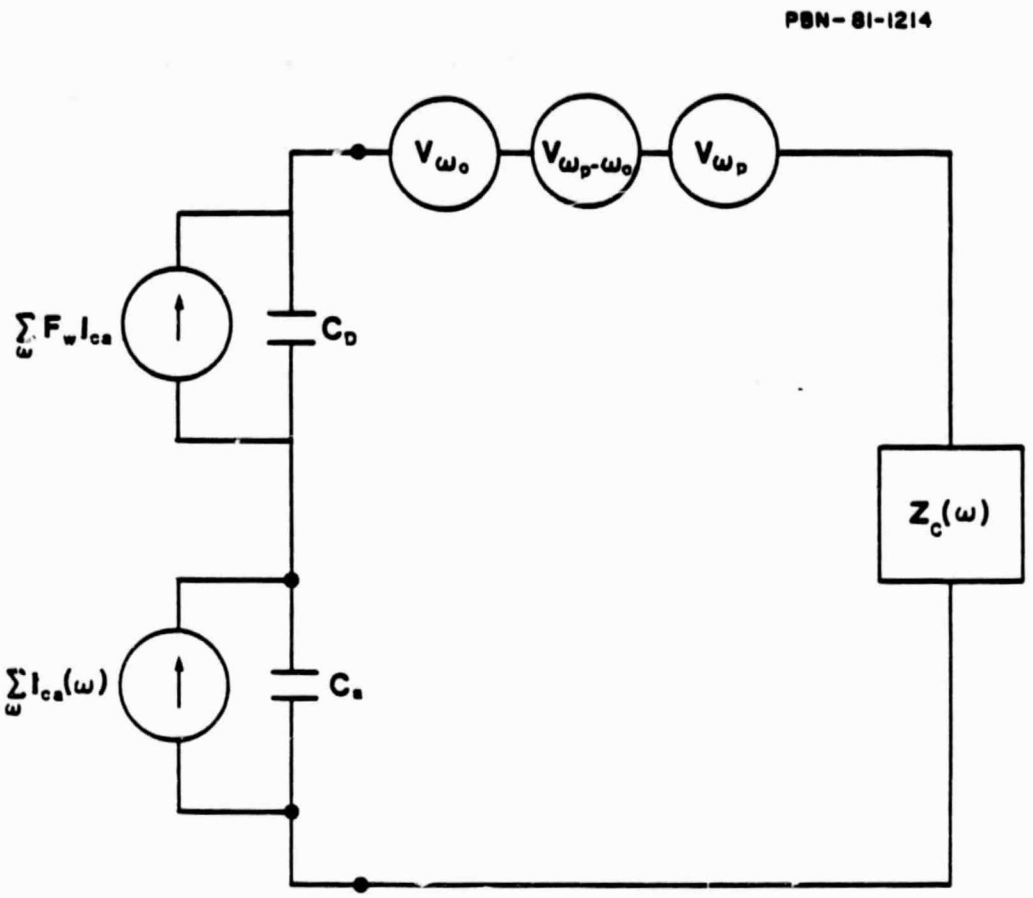


Figure 36. Idealized diode equivalent circuit operating as an amplifier into a circuit with impedance $Z_c(\omega)$. Only three impressed voltages are assumed to be present.

amplitudes, one obtains a solution for these currents in the matrix form

$$\vec{I}_t = [K]\,\vec{V}$$

where $\vec{V}$ is a 3 × 3 excitation vector and [K] is a matrix which contains a resonant denominator which can be simplified to the form [12]

$$D = 1 - |M_1|^2 S(\omega_0)\, S^*(\omega_p - \omega_o)$$

where

$$S_m = S(\omega_m) = 1 + \left(\frac{\omega_m^2}{\omega_a^2 - \omega_m^2} \right) \frac{Z_c(\omega_m) + 1/j\omega_m C_T}{Z_c(\omega_m) + Z_d(\omega_m)}$$

Here, ω_a is the avalanche resonance frequency. C_T is the total diode capacitance. M_1 is the ratio of the conduction current at frequency ω_p to the dc current. $|M_1| \leq 1$.

An instability threshold occurs as a function of M_1 when $D(\omega_0) = 0$ for a real value of ω_0 such that

$$S(\omega_0)S^*(\omega_p - \omega_0) > 1.$$

We have utilized our analytical Read model to calculate $Z_d(\omega_m)$ and an idealized Kurokawa cavity together with a realistic set of transformers and package parasitics to obtain $Z_c(\omega)$. We have then tested for instabilities as a function of dc current. Once values of ω_0 and M_1 are found to give instability, the computer analysis determines the value of fundamental frequency rf voltage at which the instability occurs.

Figure 37 shows the idealized 20-GHz circuit. Figure 38 shows the calculated circuit impedance transformed to the chip plane. As a function of bias current, we find that the only instability present is at the f/2 subharmonic. As shown in Fig. 39, the instability begins at finite V_{rf} at about 250 mA for a 1-pF device. At higher bias current, the threshold 20-GHz voltage drops

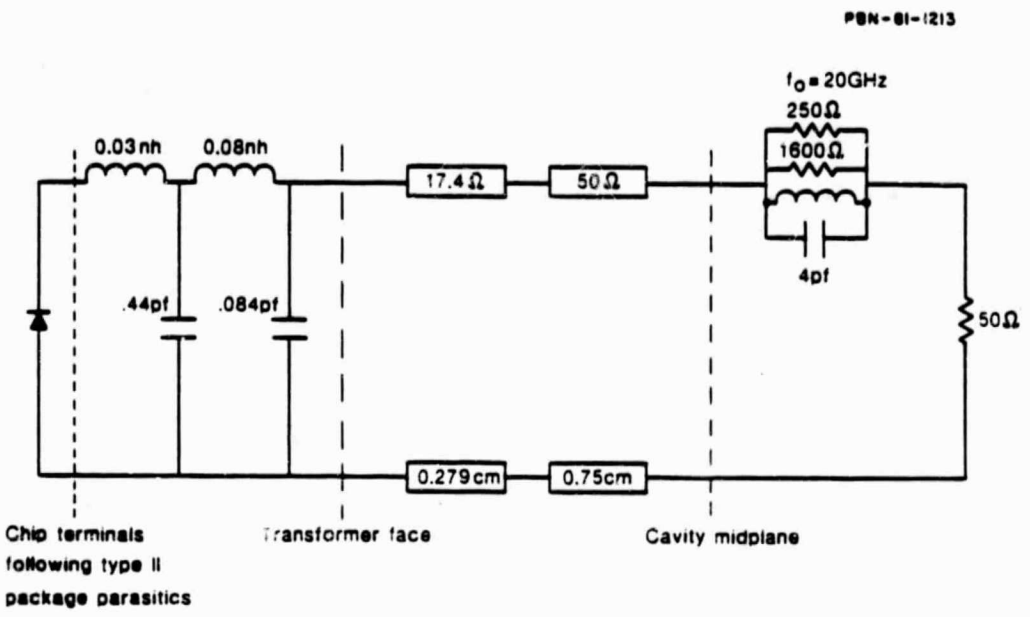


Figure 37. Idealized model circuit.

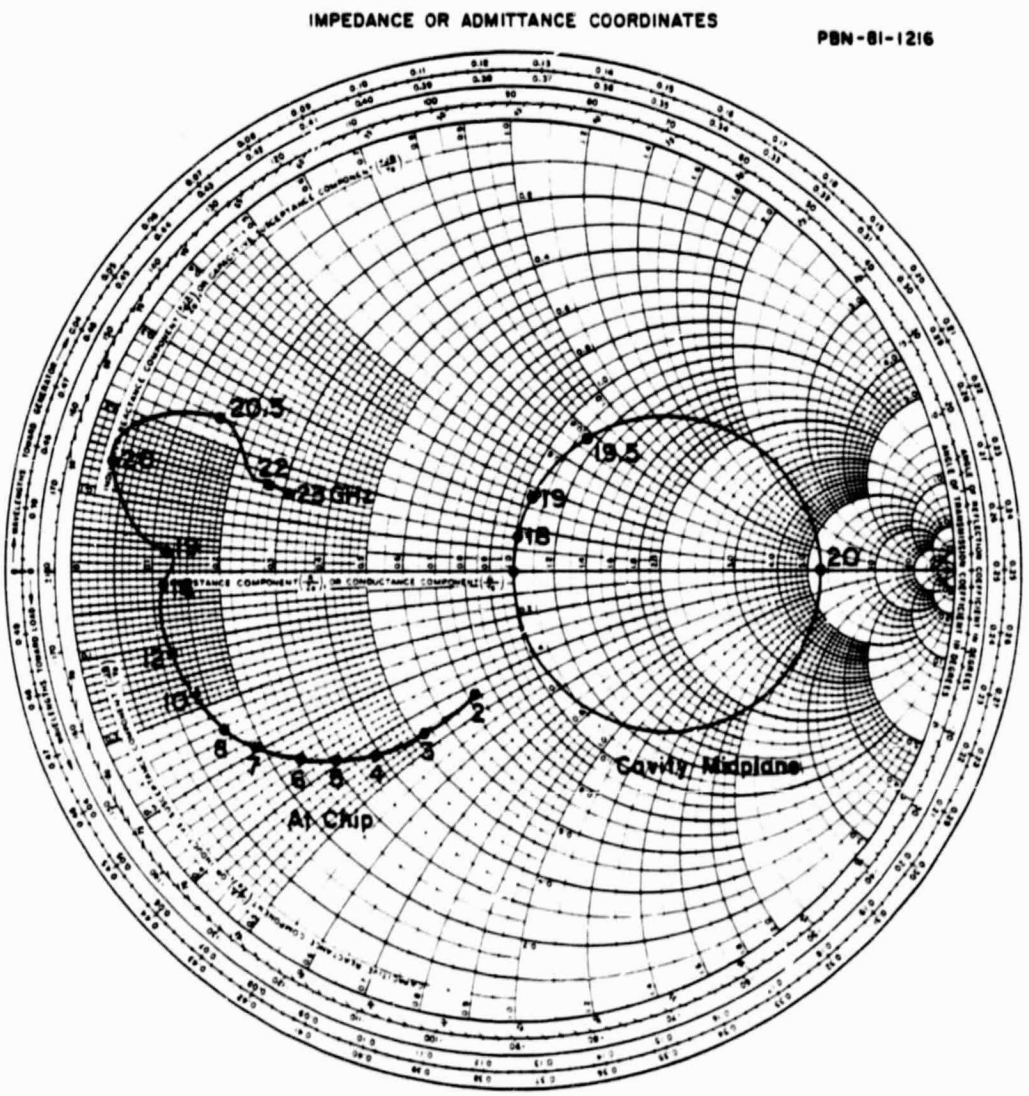


Figure 38. Calculated circuit impedance.

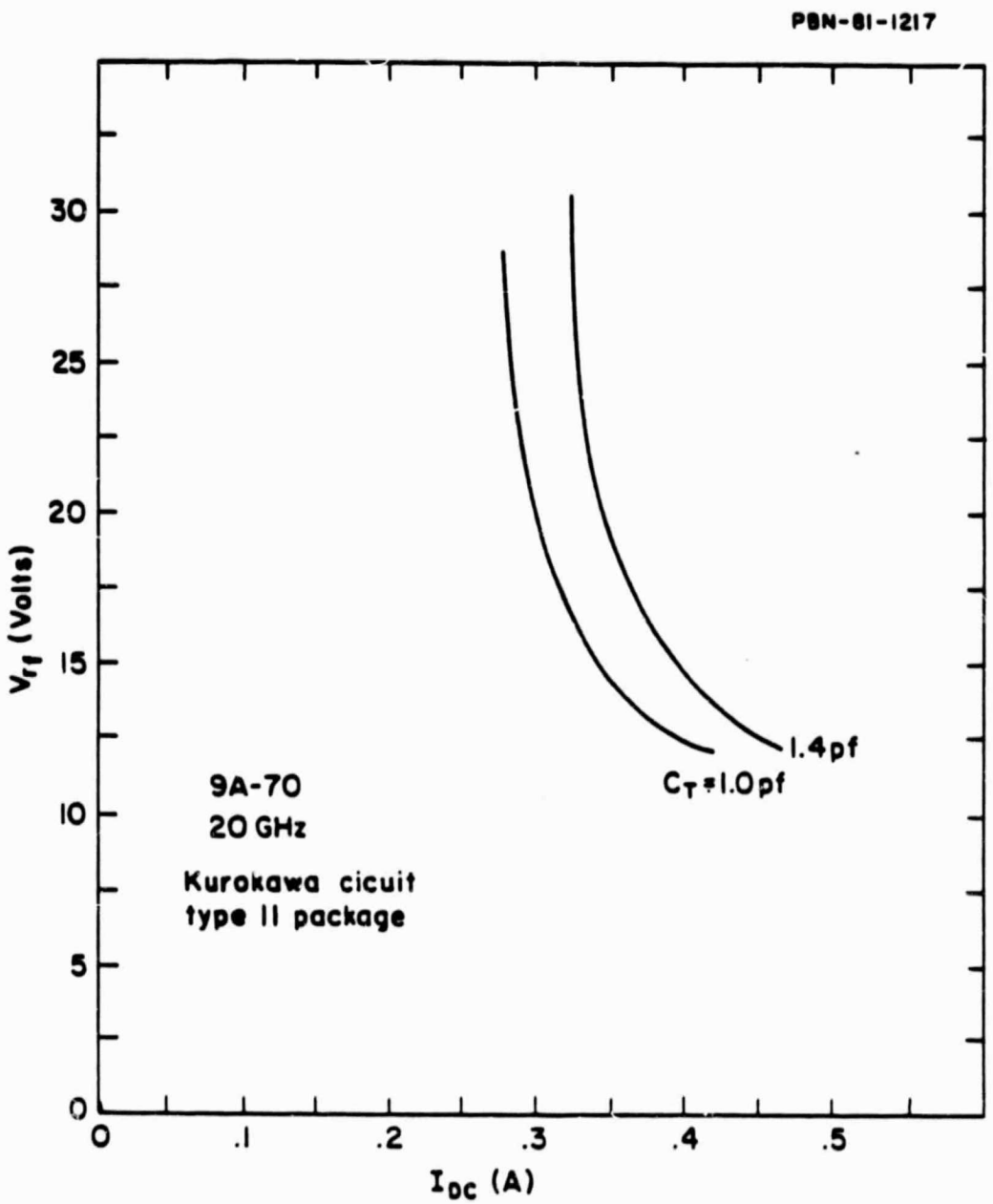


Figure 39. Rf voltage threshold for onset of f/2 subharmonic instability vs. dc bias current.

rapidly, becoming less than 20 V at 300-mA bias current. A larger capacitance pushes these effects to higher current.

In terms of device conductance, and in the absence of losses, the output power is given by $\frac{1}{2} G_D V_{rf}^2$. Thus, we can calculate the output power at the instability threshold, as shown in Fig. 40. Thus, if V_{rf} is fixed by a mechanism other than f/2 instability at low power input, P_{out} vs. P_{in} will increase along a contour of constant efficiency (e.g., 20 percent) until the input induces an instability at f/2. This is shown by the boundary crossing the 20 percent contour. At that point, V_{rf} becomes limited by the instability and there can be a steady decrease in diode efficiency, i.e., an observed power saturation. In this example, the saturation occurs at about 2.3 W for the 1-pF diode and 2.6 W for the 1.4-pF diode. Thus, the theory may describe a basic cause of premature power saturation [9].

To test the validity of the model, it will be necessary to replace the idealized circuit with data obtained by broadband characterization of the real circuit. It is inconvenient to obtain broadband chip admittance data, so that our now generally accepted model could be used with some confidence down to about 2 GHz. Once the stability criteria are shown to apply at 20 GHz, they can be used to synthesize a more stable circuit.

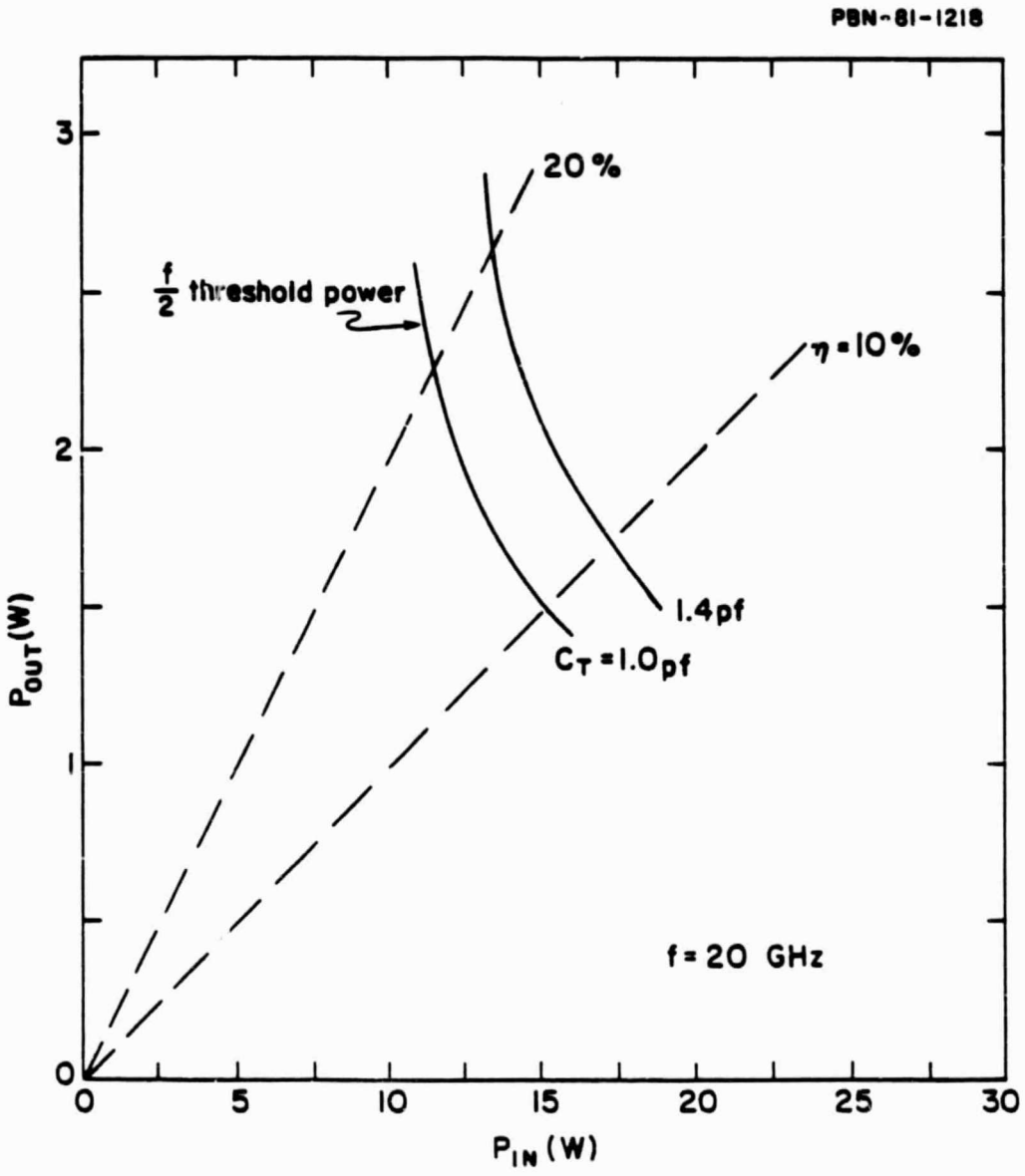


Figure 40. Output power level at f/2 instability vs. dc input power. Power saturation can occur where the diode efficiency line intersects these contours.

7.0 SUMMARY AND CONCLUSIONS

In this report, we have described the results of an 18-month effort which has advanced the state of the art of double-drift GaAs IMPATT diodes operating at 20 GHz. We have demonstrated that power output up to 4 W CW can be achieved with a single device. We have also shown that a conversion efficiency of 20 percent is feasible at this frequency.

Two types of diodes were designed: one, a single mesa with integrated beam leads, can be mounted in the small EHF package; the other is a quadrimesa with thin contact pads suitable for a larger package.

We have fabricated diamond-heatsink EHF packages which yielded devices with low thermal impedances, of the order of 10°C per watt. We expect even lower values, about 6°C per watt, from the quadrimesa geometry on diamond. With such low values of thermal resistance, power output in excess of 6 W should be feasible.

Because of schedule pressures, and under direction from TRW, we built and tested fifty diodes for delivery in the 17th month of the program. The materials grown for that purpose were not optimum, and consequently the conversion efficiencies observed were low, because of the presence of an undepleted p layer. Our next iteration of the material specification will remove this problem. By using a quadrimesa geometry in a diamond-heatsink package, we believe that we can achieve powers in excess of 6 W with efficiencies greater than 20 percent. We have shown from the measured parasitic reactances of the larger package that they should not limit the bandwidth of the amplifier circuit in which the diodes are used.

An important problem which remains to be solved is the elimination of parametric instabilities. They are a strong function of the circuit characteristics. They were observed at relatively low power levels in top hat cavities. By going to a Kurokawa-type cavity, we have pushed the threshold of instabilities to higher levels, but there still remains more work to be done.

Finally, the diode reliability has been improved by refining the contact metalization processes. Mean time to failure (MTTF) exceeding 10^4 hours has been measured on small sample lots using accelerated stress tests. MTTF greater than 10^5 hours seems possible, especially with the multimesa diodes, which can operate at lower junction temperature.

8.0 REFERENCES

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APPENDIX

WAFER CHARACTERIZATION

				N ACTIVE				P ACTIVE			MESA					
Wafer No.	Run Date	Growth Rate (μm/min)	N** Buffer Width (μm)	Width (μm)	Doping (X 10^{15})	N Spike Q (X 10^{12})	P Spike Q (X 10^{12})	Width (μm)	Doping (X 10^{15})	P** Contact Width (μm)	DIA. (mils)	X_o (μm)	C_o (pF)	C_B (pF)	V_B at 1 ma (volts)	Spec. No.
9A 18		0.239	5.98	1.91	12.0	1.43	0.17	1.43	11.0	0.24	23.65	0.31	98	11.5	47.2	K-DDR-1
9A 19		0.267	6.69	2.14	14.0	1.63	0.16	1.61	14.0	0.27	23.65	0.30	107	10.6	41.4	K-DDR-1
9A 33		0.259	15.01	2.07	15.0	1.73	0.57	1.55	12.5	0.26	23.65	0.29	109	42.4	39.2	K-DDR-1
9A 35		0.255	14.78	1.66	12.0	1.62	0.62	1.32	14.0	0.26	23.65	0.29	112	40.4	39.6	K-DDR-1
9A 36		0.252	14.64	1.31	13.0	1.54	0.75	1.12	13.0	0.25	23.65	0.29	108	NA	36.5	K-DDR-1
9A 37		0.251	14.53	1.30	16.0	1.80	1.00	1.11	14.0	0.25	23.65	0.27	115	21.2	32.8	K-DDR-1
9A 75	12/08/80	0.235	14.4	0.92	7.0	1.63	1.45	0.85	8.0	0.40	23.65	0.27	115	12.6	34.0	K-DDR-2
9A 93	01/09/81	0.239	15.54	0.80	12.0	2.40	0.87	0.75	17.0	0.25	23.65	0.25	127	24.8	28.2	K-DDR-2
9A 101	01/21/81	0.257	16.70	0.86	9.0	1.81	1.26	0.75	14.0	0.30	23.65	0.28	113	14.8	32.4	K-DDR-2
9A 102	01/22/81	0.238	15.5	0.78	8.0	1.45	1.45	0.72	16.0	0.40	23.65	0.26	119	16.0	30 ± 2	K-DDR-4
9A 103	01/23/81	0.233	15.1	0.73	8.0	1.4	1.4	-0.8	15.0	0.3	23.65	0.267	118	11.0	26 ± 2	K-DDR-4
9A 109	02/03/81	0.236	15.4	0.80	12.0	2.63	1.67	0.75	16.0	0.40	23.65	0.28	114	25.0	21.0	K-DDR-4
9A 110	02/04/81	0.234	15.2	0.80	8.0	1.43	1.43	0.70	14.0	0.20	23.65	0.27	116	16	29 ± 2	K-DDR-4
9A 111	02/05/81	0.231	15.02	0.75	11.0	1.70	1.48	0.79	8.0	0.30	23.65	0.27	114	16.6	30.4	K-DDR-2
9A 120	02/19/81	0.259	16.84	0.74	17.0	2.42	1.13	0.85	14.0	0.35	23.65	0.28	112	20.6	27.0	K-DDR-2

(continued)

APPENDIX

WAFER CHARACTERIZATION (Continued)

				N ACTIVE				P ACTIVE			MESA					
Wafer No.	Run Date	Growth Rate (μm/min)	N** Buffer Width (μm)	Width (μm)	Doping (X 10^{15})	N Spike Q (X 10^{12})	P Spike Q (X 10^{12})	Width (μm)	Doping (X 10^{15})	P** Contact Width (μm)	DIA. (mils)	X_o (μm)	C_o (pF)	C_B (pF)	V_B at 1 ma (volts)	Spec. No.
9A-121	02/20/81	0.242	14.52	0.72	11.0	2.25	1.58	0.64	20.0	0.30	23.65	0.25	122	19.5	24.2	K-DDR-2
9A-151	04/02/81	0.266	17.29	0.56	11.0	2.04	1.61	0.56	8.0	0.30	23.65	0.27	112	NA	28.6	K-DDR-2-M
9A-153	04/07/81	0.242	15.73	0.65	9.0	2.55	1.48	0.65	15.0	0.30	23.65	0.27	115	NA	25.8	K-DDR-2-M
9A-155	04/09/81	0.238	15.47	0.75	9.0	2.78	1.40	0.75	15.0	0.30	23.65	0.27	111	NA	25.9	K-DDR-2-M
9B-09	05/05/81	0.239	15.5	0.77	8.6	2.18	1.24	0.85	11.5	0.30	23.65	0.32	98	NA	29.1	K-DDR-2-M
9B-19	05/21/81	0.230	15.0	0.69	7.3	2.23	0.81	0.48	13.0	0.27	23.65	0.26	119	NA	27.0	K-DDR-2-M
9B-25	06/03/81	0.235	15.3	0.75	5.2	2.2	2.0	0.7	17.0	0.3	23.65	0.27	118	19	25.0	K-DDR-4
9E-29	10/26/81	0.190	5.5	1.05	8.0	1.83	1.83	1.0	12.0	0.28	23.65	0.18	176	15.0	29.0	K-DDR-4
9E-30	10/27/81	0.213	6.4	1.2	8.2	1.87	1.87	1.13	14.0	0.4	23.65	0.18	174	16.0	28.0	K-DDR-4
9E-36	11/04/81	0.232	7.1	0.94	10.0	1.94	1.94	0.95	10.0	0.3	23.65	0.20	157	14.0	30.0	K-DDR-4
9E-37	11/05/81	0.213	6.4	0.89	9.5	2.05	1.68	1.03	9.5	0.3	23.65	0.19	164	14.0	31.0	K-DDR-4
9E-38	11/06/81	0.201	6.0	0.85	9.6	1.87	1.87	0.95	12.5	0.3	23.65	0.19	168	16.0	27.0	K-DDR-4
9E-39	11/09/81	0.216	6.5	0.90	10.0	2.05	2.05	1.03	12.0	0.3	23.65	0.19	167	17.0	24.0	K-DDR-4
9E-48	11/20/81	0.192	5.8	1.0	8.0	1.83	1.83	1.0	9.0	0.3	23.65	0.20	158	13.0	32.0	K-DDR-4
9E-53	12/02/81	0.225	6.8	1.1	7.0	1.93	1.93	1.1	8.0	0.35	23.65	0.20	154	11.0	34.0	K-DDR-4

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