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HIGH-SPEED DIGITAL SIGNAL NORMALIZATION FOR FEATURE IDENTIFICATION

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Summary

A design approach for high-speed normalization of digital signals has been developed. A reciprocal look-up table technique is employed, where a digital value is mapped to its reciprocal via a high-speed memory. This reciprocal is then multiplied with an input signal to obtain the normalized result. Normalization improves considerably the accuracy of certain feature identification algorithms. By using the concept of pipelining the multispectral sensor data processing rate is limited only by the speed of the multiplier. The breadboard system was found to operate at an execution rate of five million normalizations per second. This design features high precision, a reduced hardware complexity, high flexibility, and expandability which are very important considerations for spaceborne applications. It also accomplishes a high-speed normalization rate essential for real-time data processing.

Introduction

Multispectral imaging systems employed in earth observational satellites generate vast quantities of data at very high rates. All of these data are currently transmitted to the ground regardless of information content or user interest in the scene. This inefficient mode of operation places a considerable burden on the ground processing facilities resulting in high costs and delays in providing users with finished data products. One recognized solution is to introduce intelligence to the sensor by coupling it with an onboard information processing system. This approach would allow useful information to be extracted from raw sensor data prior to transmission.

NASA Langley Research Center is currently addressing the challenging task of processing high-speed data onboard the spacecraft under the Information Adaptive System (IAS) program.[1] The IAS program objective is to investigate algorithms and system architectures and approaches to real-time, spaceborne processing of multispectral image data. The beneficiaries of this technology development would include unmanned remote sensing missions as well as manned operations aboard Space Station.

One particularly useful and potentially complex function under investigation involves the accurate identification of earth features as a function of the spectral characteristics of the image data. The ability to identify features in real time onboard the spacecraft would allow data with little or no information content, e.g. that which contains excessive cloud cover, to be discarded rather than transmitted to the ground. For missions whose objective is to monitor crops and forests; it is desirable to implement an onboard information processing system which can distinguish vegetation from water and bare land. This information could drive a steerable imaging system in an autonomous manner so that only regions of interest are viewed.

Many of the algorithms available for feature identification, such as mean-square distance (MSD) and maximum likelihood (MLH),[2] are computationally complex and time consuming. Therefore, they are impractical to implement in a real-time spaceborne environment where considerations of size, weight and power are essential. Algorithms of the boundary approximation method (BAM) class are more suited to real-time applications since their implementation is much less complex than that of either MSD or MLH. However, MSD and MLH generally offer higher identification accuracy when compared to the BAM. Huck et al[3] have recently developed a BAM type algorithm which involves the normalization of spectral input signals prior to the threshold comparison procedure. Normalization eliminates signal variability caused by atmospheric effects thereby increasing the accuracy of the resulting identification.

The improved accuracy of the normalized BAM approach make it an attractive candidate for implementation in an onboard information processor. However, prerequisite to its acceptance is the development of a technique for high-speed signal normalizaton that fulfills the requirements for speed and reduced hardware complexity. This paper presents such a technique and describes the operation of a breadboard implementation. Results of the breadboard evaluation activity are also presented.

Boundary Approximation Method and Signal Normalization

Figure 1 illustrates the decision flow for a boundary approximation method algorithm using normalized signals. This algorithm utilizes signal ratios and threshold comparisons to identify features in an image. The signals S_1, S_2, and S_3 are radiometrically corrected outputs from a multispectral sensor. They are a measure of the magnitude of the light reflected from the earth surface to the sensor in the 0.67, 0.84, and 1.68 μm wavelengths respectively. Those wavelengths are available from channels 3, 4, and 5 of the Landsat D Thematic Mapper (TM).[4,5] The input signals are normalized and then compared in terms of magnitude with certain previously calculated thresholds. The classification of the incoming pixel is based on the result of the comparisons.

The normalization process reduces signal variabilities caused by variations in the magnitude of the radiance levels common to each spectral channel. The bar chart shown in figure 2 is a result of computer analysis performed to evaluate the effects of signal normalization on feature identification accuracy.[3] These results were obtained on an artificially generated test scene with known feature content. Both normalized and unnormalized identification algorithms were applied to this data and the percentage of correct classifications constitutes the feature identification accuracy. The accuracy of the normalized approach relative to the unnormalized was examined for various imaging conditions. These conditions include the range of visibility which is a function of the atmosphere and sun elevation angle relative to nadir. The radiance variabilities caused by atmospheric effects increase as visibility decreases and at greater sun elevation angle, θ_0. The reason for this is that under these conditions the path that the reflected sunlight has to travel becomes longer. The results indicate that the normalized BAM algorithm improves the accuracy of the feature identification process considerably during unfavorable imaging conditions.

Design Considerations

The major challenge to implementing the normalized BAM in a real-time processing system is the division operation. Division is the most complex and time consuming arithmetic operation and represents a potential bottleneck to any high-speed application. Table 1 presents a comparison between several division algorithms and techniques, in terms of accuracy, flexibility, hardware complexity, and speed. For this comparison, accuracy is related to the extent to which the results obtained from a specific division method agrees with the results of the division performed by a minicomputer software implementation. Further computer analysis is necessary to determine the required precision of the normalization process relative to feature classification accuracy. Flexibility is a measure of how easily an algorithm implementation can be expanded to accommodate increased precision without a major impact on the existing design and operating speed. The hardware complexity relates to the quantity of electronic circuitry needed to implement the algorithm. Finally, speed is an essential quality for this real-time normalization task.

These four categories that characterize each approach are interrelated. For example, as speed and accuracy of the design increases, there is a resulting increase in hardware complexity. The objective of the algorithm selection procedure for signal normalization was to first achieve the necessary throughput (< 500 ns) and then select an approach which provides the best combination of the other design features.

The comparison, restoring and non-restoring division algorithms from table 1, are conventional approaches which are implemented in some digital computers. These algorithms obtain the quotient by repeated operations of subtracting or adding, comparing and shifting. Several hardware implementations of these algorithms were examined and due to the sequential nature of their operation, they were considered too slow to be feasible for real-time applications. Since the throughput of conventional methods for division fell short of the desired performance, high-speed hardware look-up tables were investigated. In a look-up table technique an input value is mapped to a desired output via a high-speed memory circuit. Computations are performed off line from high-speed process, i.e. the desired output values are computed and loaded into memory prior to operational mode.

One approach using this technique is the direct method, where the input signals are applied directly to the address lines of the memory to select a location from which the desired output value is read (figure 3). Using this technique, the speed of the operation is limited only by the access time of the memory. However, the look-up table memory must store all possible results of the normalization and can therefore be excessively large for spaceborne applications.

One method to reduce the required bit capacity of the table is to convert the division into a subtraction by means of logarithm and antilogarithm transformations (figure 4). Instead of storing all possible results, one need store only the approximated logarithms and antilogarithms which usually requires much smaller memories. By using this approach the normalized result will include cummulative rounded errors which were generated from logarithmic approximations. A high error may interfere with an accurate feature classification.

It was desirable to develop an approach to signal normalization which offered the speed of the direct method but with reduced hardware complexity and that also provided acceptable computational accuracy. The reciprocal look-up method was devised to achieve this objective.

Reciprocal Lookup Method

Figure 5 illustrates the reciprocal lookup method (RLM) for signal normalization. In this approach, the normalization is accomplished by multiplying an input signal in the normalization expression by the appropriate reciprocal. The input signals are first summed and then applied to the address lines of a high-speed read-only-memory (ROM). The ROM serves as a lookup table which maps each denominator to the correct reciprocal value. The size of the table in bits is equal to

$$2^N \cdot w$$

where N is the word length of the result of the addition process and w is the length of the reciprocal selected to achieve the desired precision.

The advantage of the RLM is that it requires considerably less storage capacity than the direct lookup approach while maintaining the desired throughput rate. The storage reduction factor of memory required by the direct method to that required by the reciprocal lookup method, is given by:

$$I = 2^{(n-1)(k-1)}$$

where n is the number of signals involved in the normalization and k is the length of the input signals in bits. For example, the direct method requires 128 times the storage of the RLM for an application involving two 8 bit signals. In terms of processing speed, the RLM compares favorably when pipeline design techniques are employed. Pipelining will allow a reciprocal to be determined for the subsequent input signals during the same time the multiplication is performed on the current signals. As a result, the system throughput is limited by the slower of the two pipeline processes rather than by the end-to-end propagation time of data through the entire system. A proof-of-concept breadboard was developed to examine the suitability of the RLM to real-time spaceborne processing. The design and evaluation results are presented in the following section of this paper.

The accuracy of the reciprocal lookup operation is a function of the number of bits used to represent the reciprocal values. An increase in precision will, of course, increase the size of the lookup table ROM; however the speed with which the reciprocal value is read from the table is not effected, since this is a parallel operation. A software model was developed to determine the effect of the precision of the reciprocal on normalization accuracy, and those results are presented in a subsequent section of this paper.

Proof-of-Concept Breadboard and Test Results

Figure 6 is a block diagram of the normalization circuitry and the test support electronics used to evaluate the RLM technique. The purpose of the evaluation was to examine whether the maximum throughput of the design could be achieved while maintaining the accuracy of the computation. A sensor simulator board was developed to serve as a high-speed simulated data source for the tests (figure 7). This board generated two 8-bit signals from high-speed counters, changing at the rate of an external clock of variable frequency. The input-output devices of the MC6800 microcomputer were used to initialize the counters and start the normal operation of the sensor board.

The two 8-bit signals from the sensor simulator were first summed using two 4-bit TTL adders. The 9-bit result of this addition was then input to the address lines of a 512 x 12 read only memory (ROM). The ROM was previously programmed with the reciprocals for the 512 possible results of the addition. A 12 by 12 bit, high-speed multiplier was used to perform the multiplication function which provides the normalized result. The function of the logic analyzer is to collect the output data from the multiplier and display it in an orderly manner for analysis.

The addition, lookup, and multiplication operations have to be performed in an orderly and timely manner. To ensure proper timing of these functions, several control signals were generated. The timing diagram for the operational mode is illustrated in figure 8. New data is presented to the system input at the rising edge of every data clock cycle; therefore, the normalization circuitry must be prepared to accept new data at those times. The control circuitry in figure 6 generates these signals as a function of the input data clock. This circuitry was designed using one-shots or monostable multivibrators. The first one-shot is fired using the rising edge of the data clock and it generates the chip select pulse for the ROM. Subsequent control signals are generated in a similar manner by a chain of one-shots. This approach provided a simple method of generating control signals for the proof-of-concept breadboard. For an actual spaceborne implementation, there is a potential reliability problem due to temperature changes which may affect the pulse widths obtained from the one-shots. Therefore, two other alternatives for control are being considered. The first one involves using a phase locked loop (PLL) configured as a frequency synthesizer (figure 9). This circuit generates a set of signals, nfo, (n-1) fo...fo which can be decoded to control the hardware. The second alternative is to generate a very fast clock and syncronize it with the data clock by means of a simple AND-OR circuit (see figure 10). These two clocks are fed into a shift register and a feedback circuit is used to generate a certain number of pulse trains, each one shifted one clock cycle from the previous one. These pulse trains can be used as the necessary control signals. In a space environment either one of these control alternatives will represent fast, predictable and flexible improvements over the breadboard approach.

The results of the test and evaluation revealed that the RLM breadboard could accommodate, in real time, a sensor which generates new data every 200 ns. The operating speed of the system was limited only by the speed of the multiplier since pipelining was employed in the design. The results of the high-speed breadboard implementation were compared to that of a double precision software implementation of the normalization process to evaluate the processing accuracy of hardware approach. The worst case deviation was 19.92 percent which is a consequence of approximating the reciprocal value to 11 bits in the breadboard RLM. It has been determined via software analysis (see subsequent section) that this error can be reduced to 0.35 percent by expanding the reciprocal lookup table to 16 bits and using a 16 x 16 multiplier device.

Software Analysis for RLM Precision

The major source of error in the RLM normalization approach is the round off associated with representing the reciprocal in fixed point notation. A computer program was developed in the VAX 11-750 system to quantify this error using the maximum precision of the machine in double precision floating point as a baseline for comparison. Figure 11 shows a graph of the error as a function of the number of bits used to represent the reciprocal. Since this is a semilogarithmic plot to the base 10 we can say that the error decreases exponentially with the word length. To accommodate greater precision, the lookup table must be expanded to store increased word lengths and a higher resolution multiplier must be employed. This will have a direct impact on the hardware complexity of the physical electronic circuit. Therefore, a trade off analysis should be performed between the desired precision and the resulting hardware complexity. The RLM approach can be expanded to accommodate greater precision without significant modification to the original design.

Concluding Remarks

An approach to real-time signal normalization for spaceborne applications was presented. The design features a high throughput rate, reduced hardware complexity and can be adapted to accommodate the precision required by the specific application.

After a comprehensive investigation of existing division algorithms, the reciprocal lookup method (RLM) was devised as an alternative approach which is more suitable to the real-time spaceborne processing task. A test breadboard was implemented using off-the-shelf components, and successful operation was demonstrated. The normalization process was executed every 200 ns when pipeline processing was implemented. Software analysis was performed to evaluate the effect of the reciprocal approximation on the result of the normalization. Future implementation of this approach will become more practical in terms of power, size, and speed as the development of high-speed devices continues as a major technology thrust.

ALGORITHM	ACCURACY	FLEXIBILITY	HARDWARE COMPLEXITY	SPEED
COMPARISON	HIGH	LOW	MED	LOW
RESTORING	HIGH	LOW	HIGH	LOW
NON-RESTORING	HIGH	LOW-MED	HIGH	MED
DIRECT METHOD	HIGH	LOW	HIGH	VERY HIGH
LOGARITHMIC DIVISION	LOW	MED	LOW	MED HIGH
*RECIPROCAL LOOK-UP METHOD	MED-HIGH	HIGH	LOW	HIGH

TABLE 1: DIVISION ALGORITHMS COMPARISON

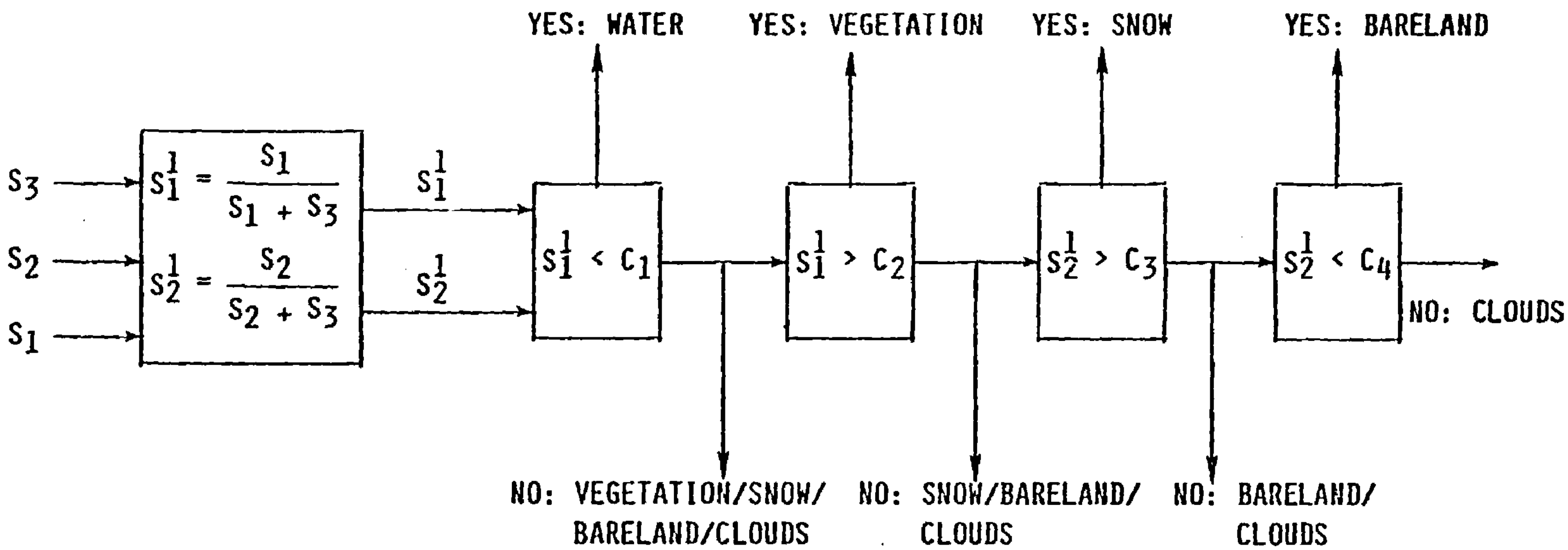


FIGURE 1. <u>DECISION FLOW DIAGRAM FOR A BOUNDARY APPROXIMATION METHOD USING NORMALIZED SIGNALS</u>

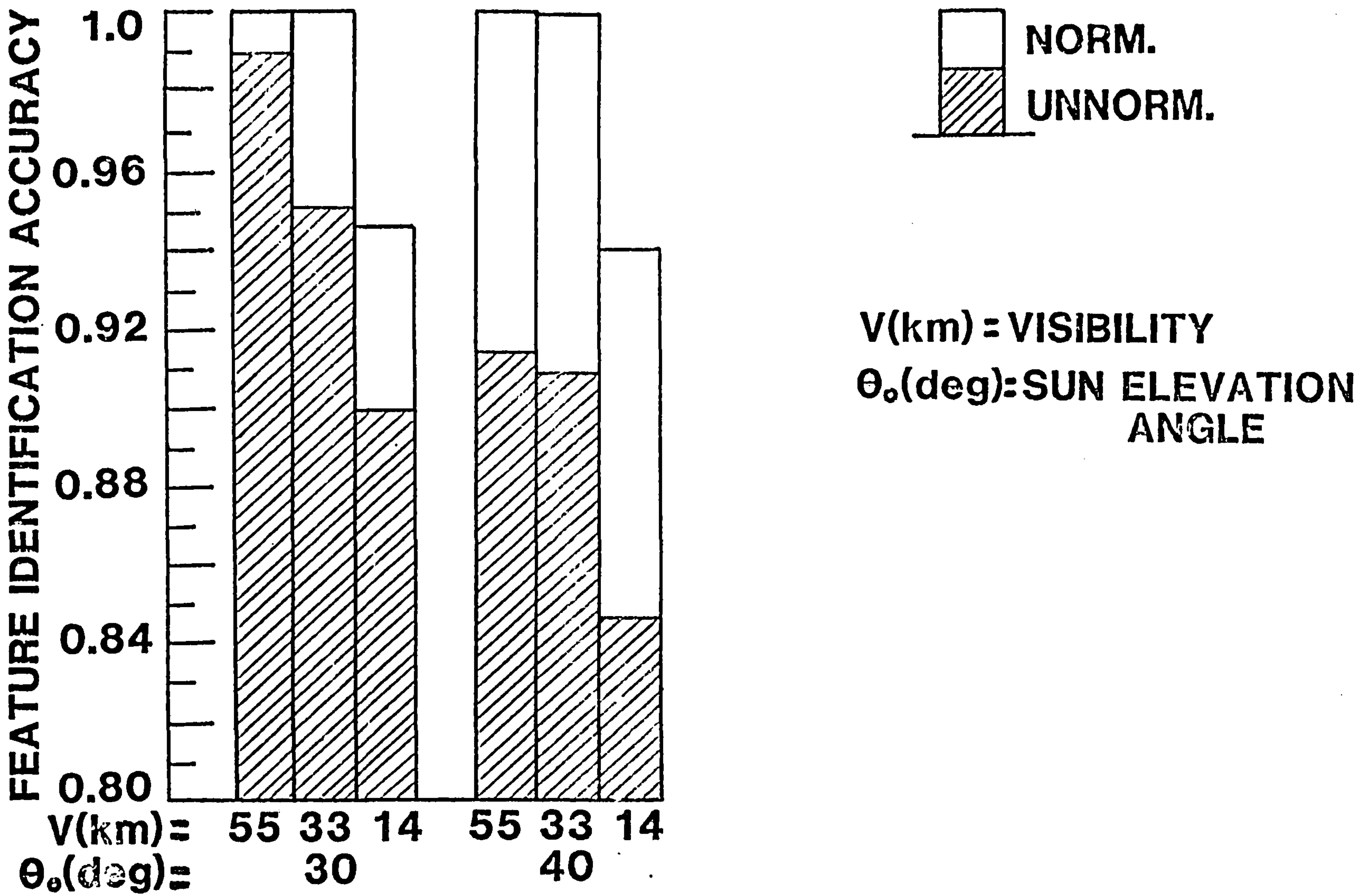


FIGURE 2. BOUNDARY APPROXIMATION METHOD ALGORITHM ACCURACY

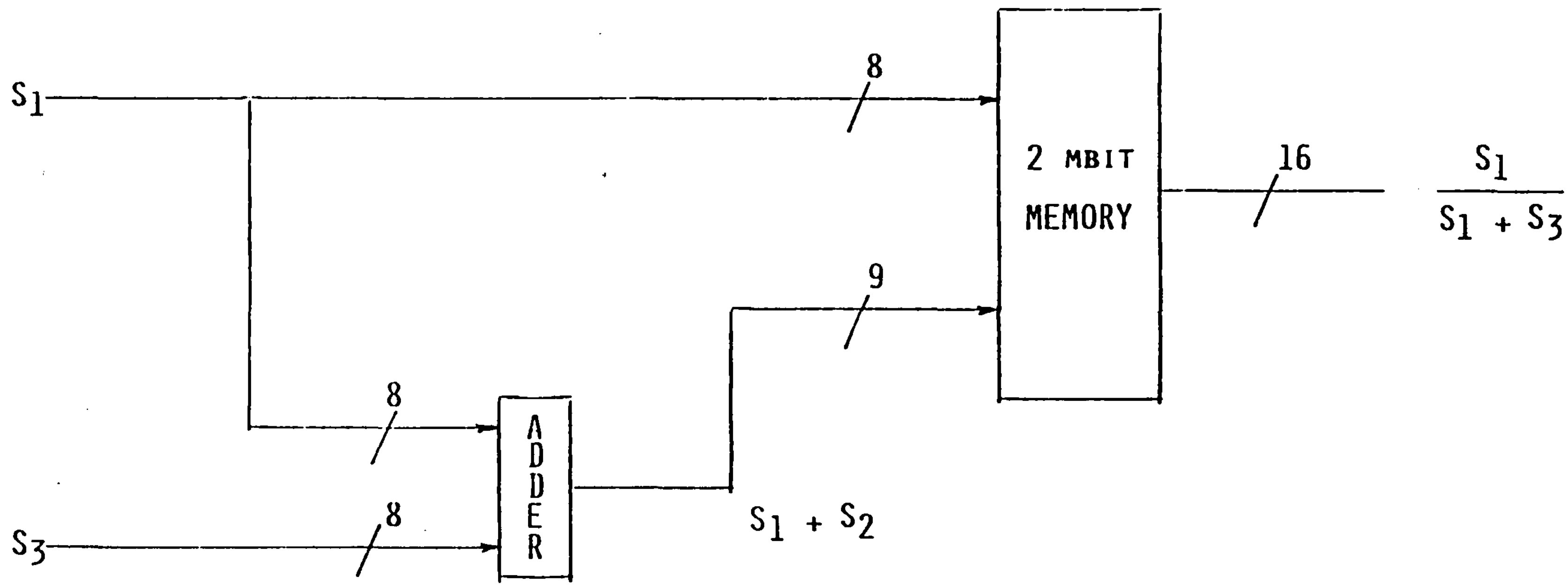
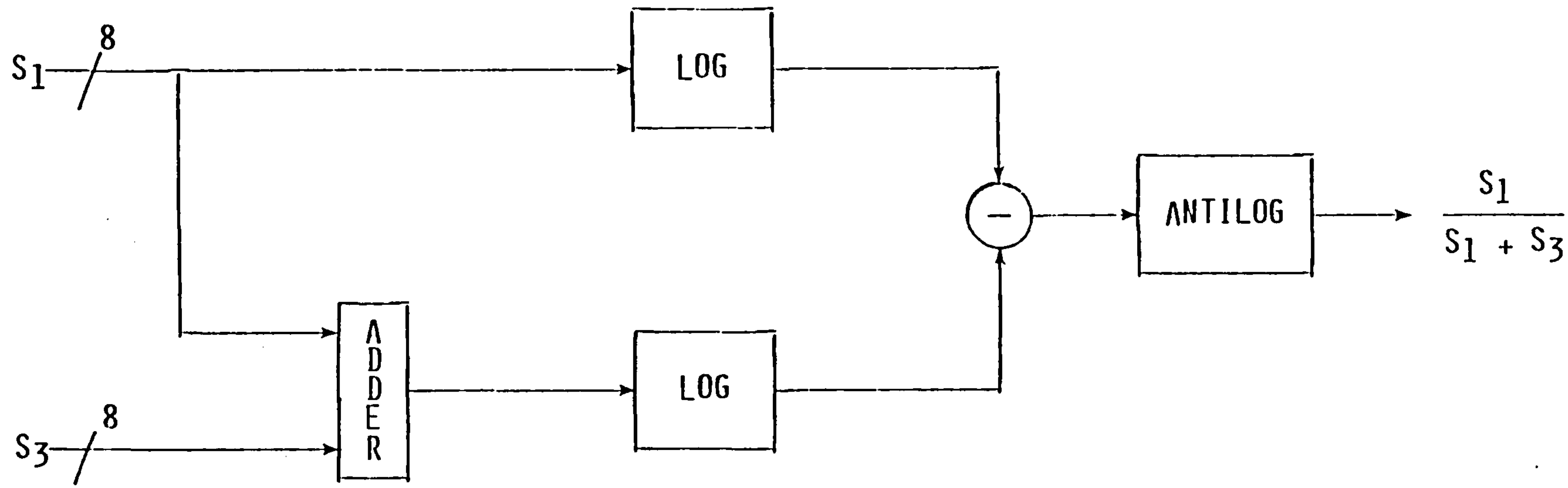


FIGURE 3. LOOK-UP TABLE DIRECT METHOD



• A/B = ANTILOG (LOG A - LOG B)

FIGURE 4. LOOK-UP TABLE NORMALIZATION USING LOGARITHMIC TRANSFORMATIONS

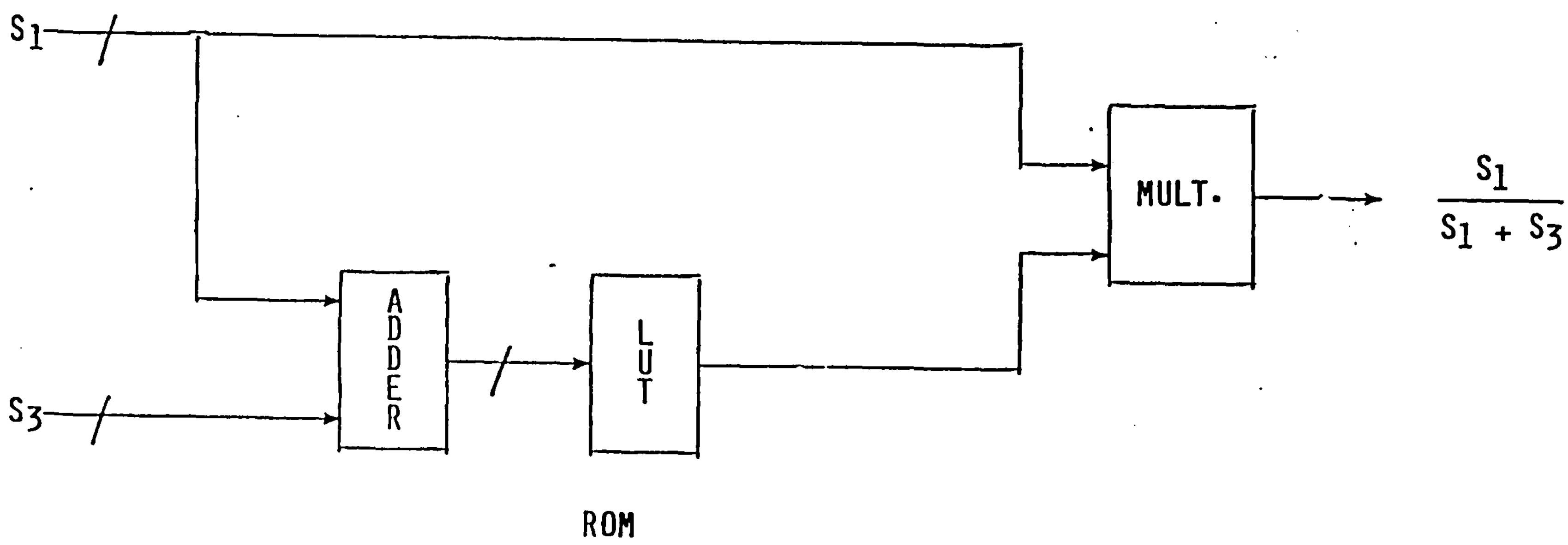


FIGURE 5. RECIPROCAL LOOK-UP METHOD

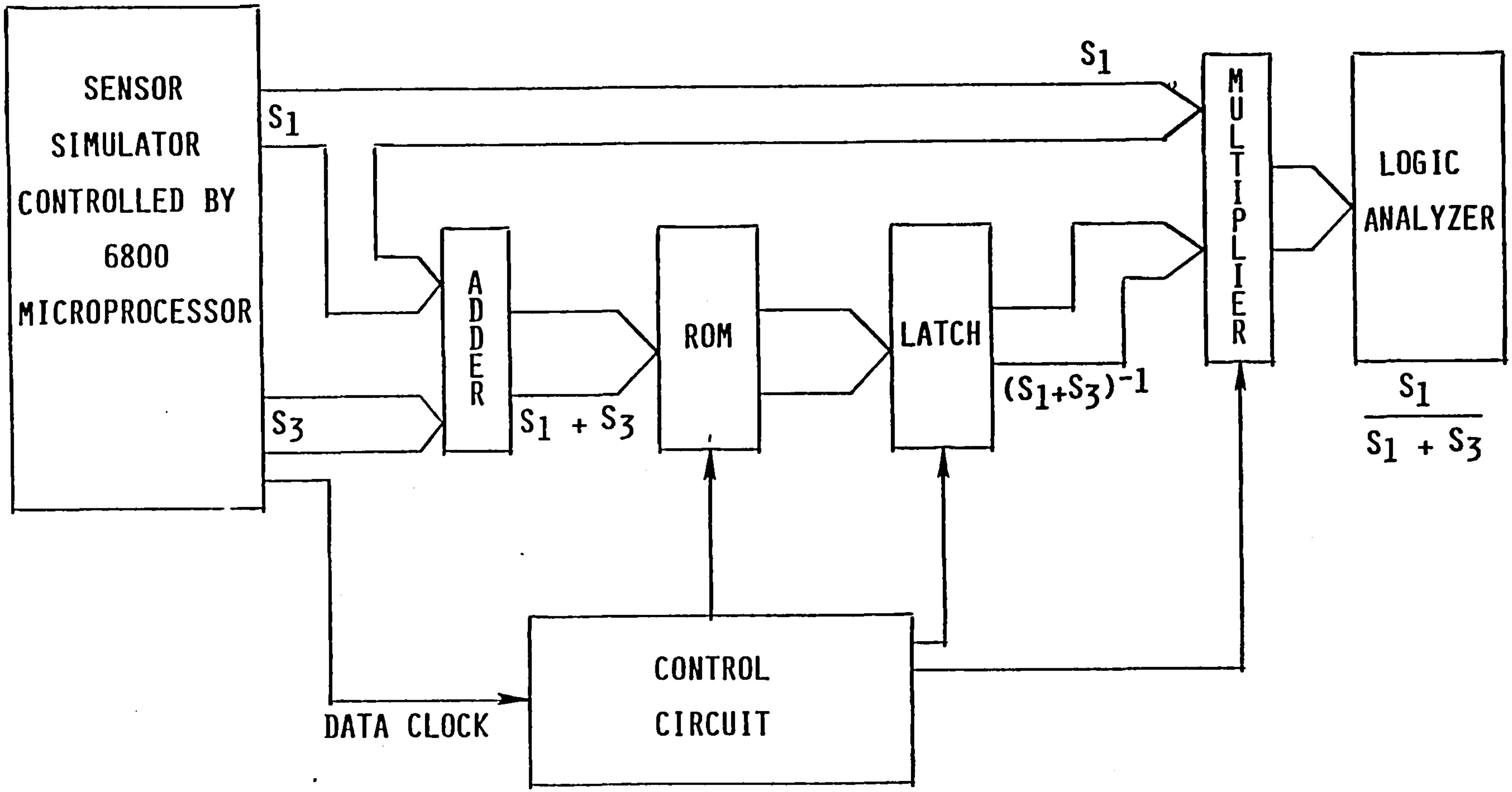


FIGURE 6. LABORATORY IMPLEMENTATION OF THE RECIPROCAL LOOK-UP METHOD

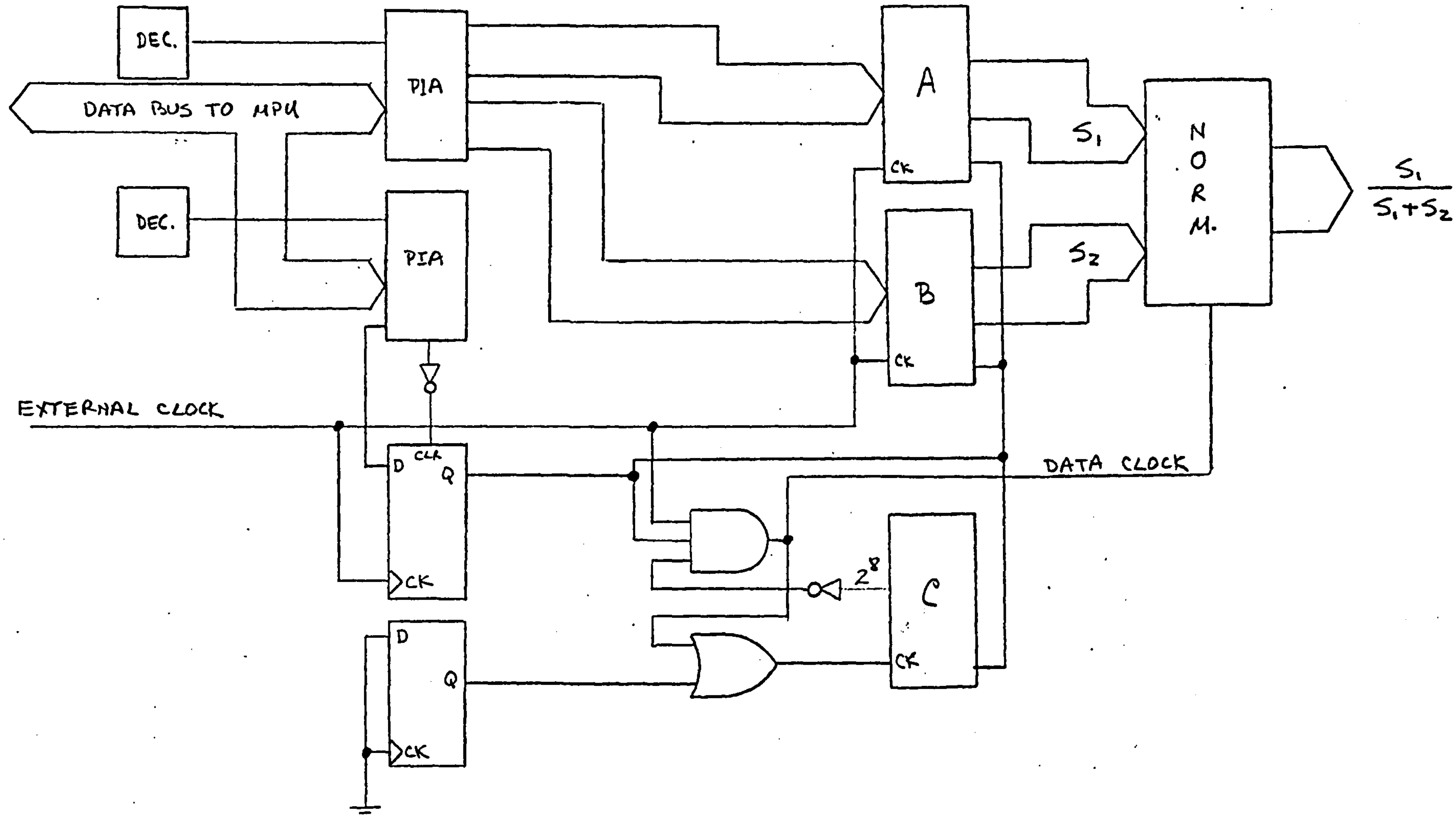
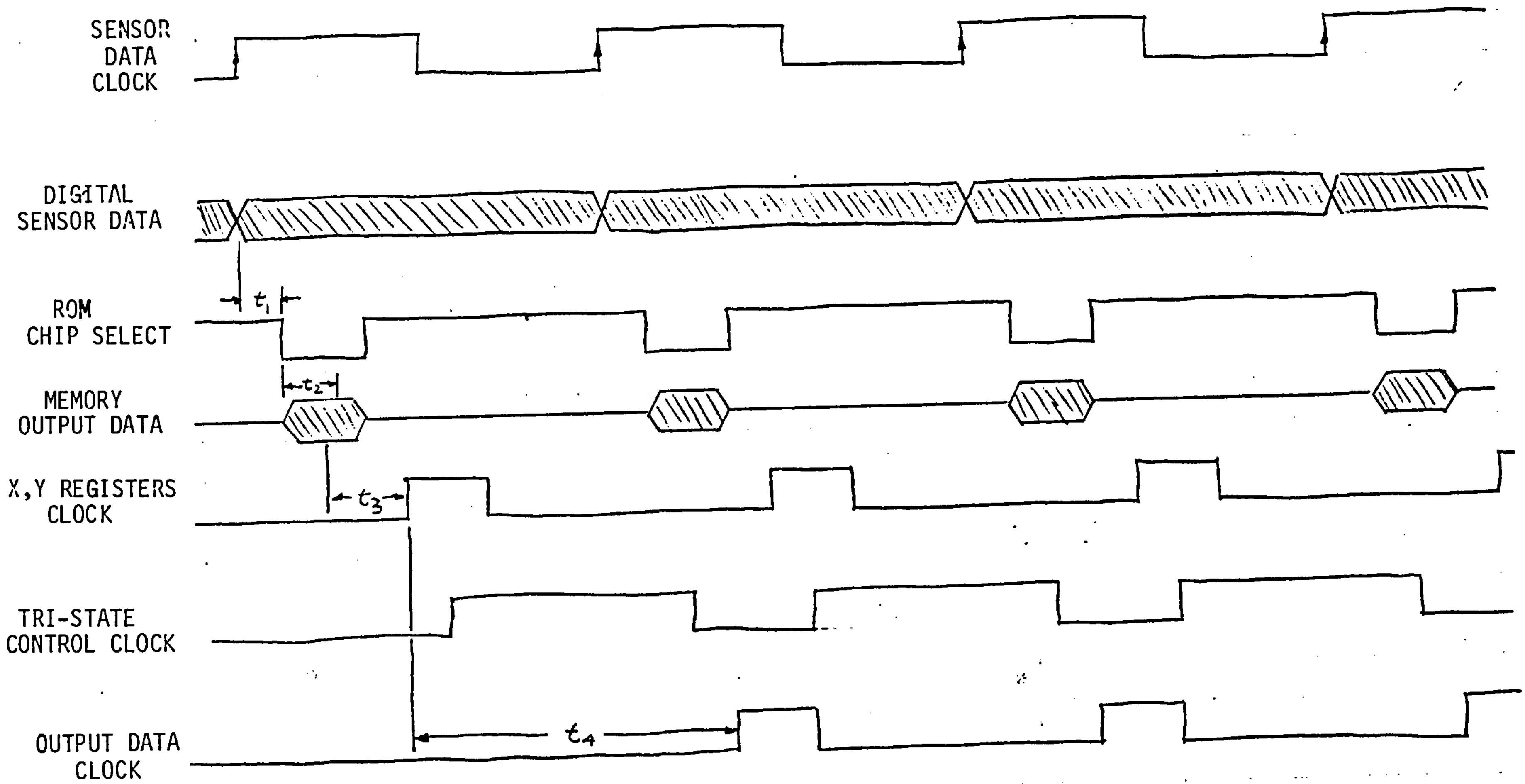


FIGURE 7. SENSOR SIMULATOR BOARD DIAGRAM



$t_1 \rightarrow$ add time
$t_2 \rightarrow$ memory access time
$t_3 \rightarrow$ memory output data latched time
$t_4 \rightarrow$ multiply time

FIGURE 8. SIGNAL TIMING DIAGRAM FOR THE NORMALIZATION BOARD

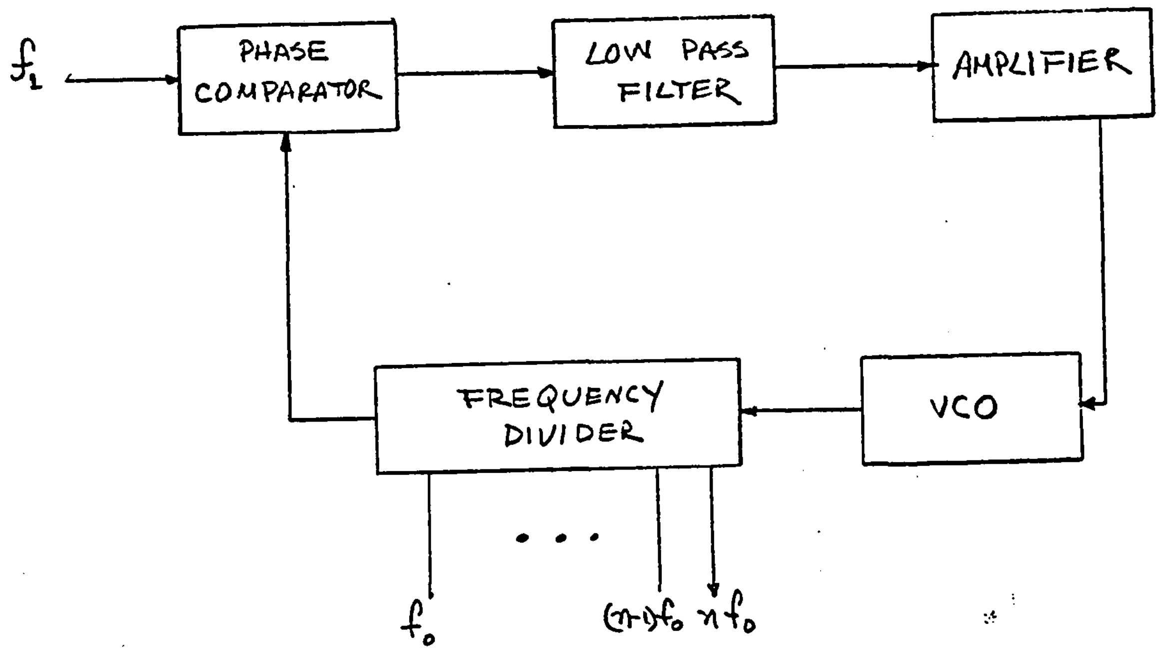


FIGURE 9. FREQUENCY SYNTHESIZER USING A PLL

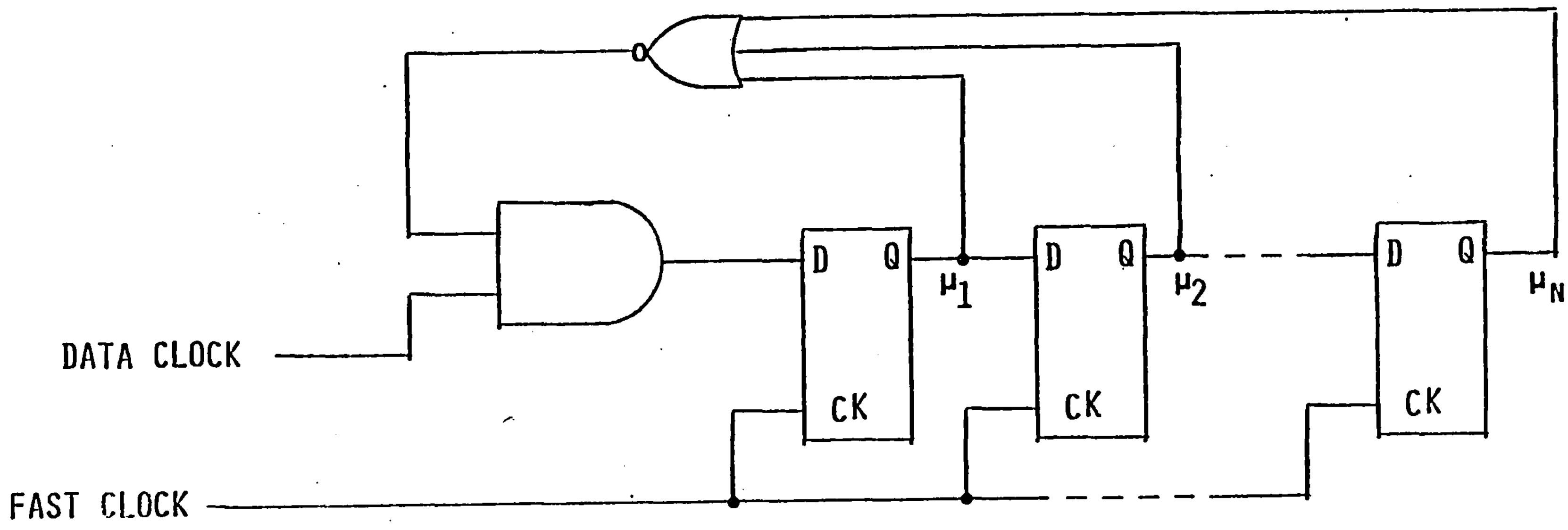


FIGURE 10. PULSE TRAINS GENERATOR USING A SHIFT REGISTER

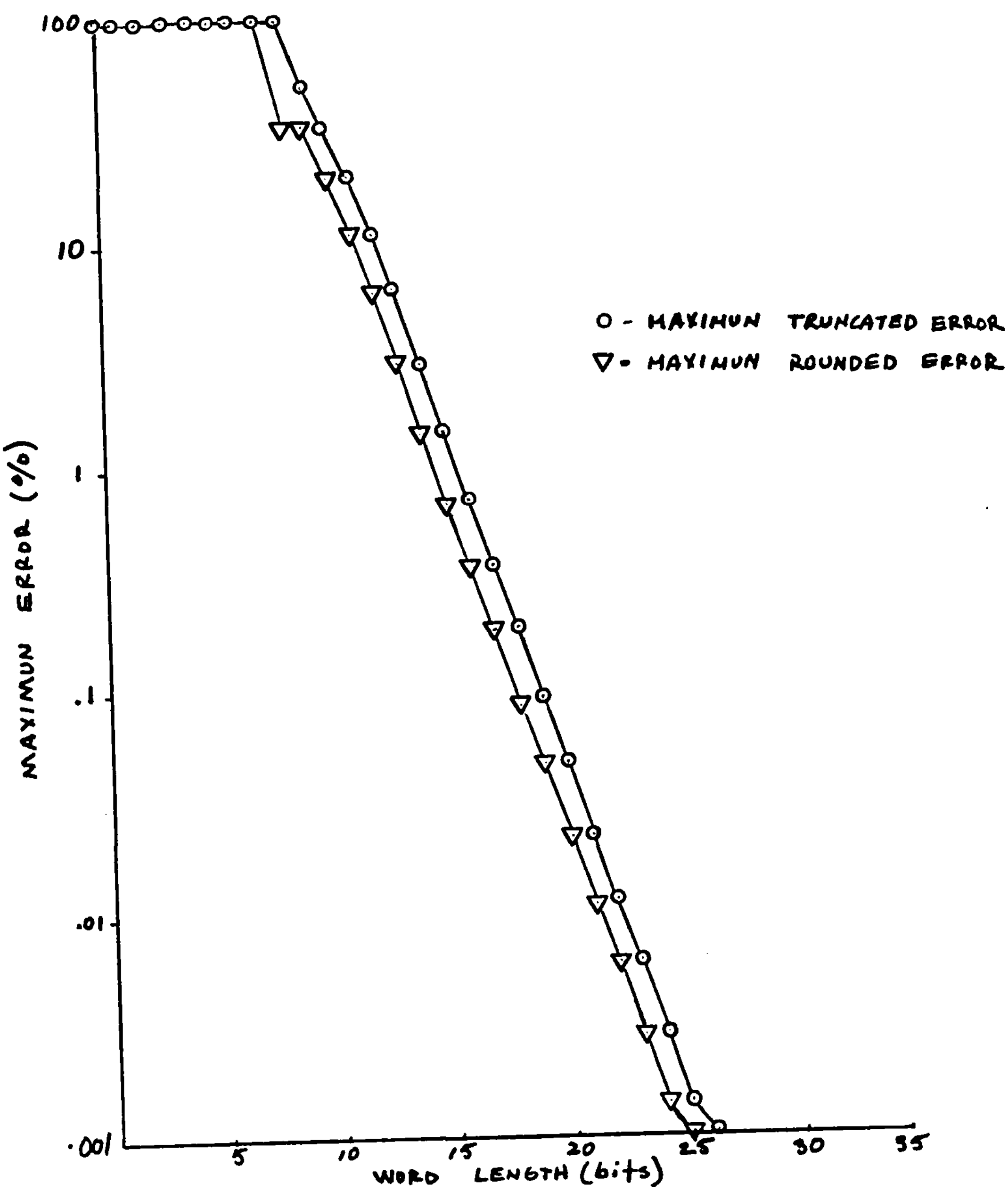


FIGURE 11. <u>MAXIMUM NORMALIZATION ERROR AS A FUNCTION OF THE PRECISION OF THE RECIPROCAL</u>

References

1. Meredith, B. D.; Carney, P. C.; LaBaugh, R. J.: "Laboratory System for Demonstrating Spacecraft Processing of Multispectral Image Data." Optical Engineering, Vol. 22, No. 2, March/April 1983.

2. Haralick, R. M.: "Automatic Remote Sensor Image Processing." Digital Picture Analysis, Ed. A. Rosenfeld, Sringer-Verlag (1976).

3. Huck, F. O.; Davis, R. E.; Fales, C. L.: "Study of Sensor Spectral Responses and Data Processing Algorithms and Architectures for Onboard Feature Identification." NASA-Langley Research Center, SPIE's Technical Symposium, May 3-7, 1982.

4. Slater, P. N.: Remote Sensing: Optics and Optical Systems, Addison-Wesley Publ. Co., London, 1980.

5. Salomonson, V. V.: "Landsat D, A Systems Overview." Proceedings of the Twelfth International Symposium on Remote Sensing of the Environment, Vol. II, Environmental Research Institute of Michigan, April 20-26, 1978.

6. Hwang, K.: "Computer Arithmetic: Principles, Architecture, and Design," John Wiley and Sons, Inc., 1979, pp. 206-208.

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15. Supplementary Notes

16. Abstract

A design approach for high-speed normalization of digital signals has been developed. A reciprocal look-up table technique is employed, where a digital value is mapped to its reciprocal via a high-speed memory. This reciprocal is then multiplied with an input signal to obtain the normalized result. Normalization improves considerably the accuracy of certain feature identification algorithms. By using the concept of pipelining the multispectral sensor data processing rate is limited only by the speed of the multiplier. The breadboard system was found to operate at an execution rate of five million normalizations per second. This design features high precision, a reduced hardware complexity, high flexibility, and expandability which are very important considerations for spaceborne applications. It also accomplishes a high-speed normalization rate essential for real-time data processing.

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