An EPROM-Based Function Generator

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A circuit is described to produce arbitrary time-dependent voltage functions derived from digital information stored in EPROMs. While this circuit is designed to be used as a modulator of the microwave pump source for a solid state low noise maser, it can be readily adapted for other applications

I. Introduction

Although there are many published descriptions of circuits to generate specific (sinusoidal, logarithmic, etc.) or arbitrary waveforms using electrically programmable read-only memory (EPROM) and digital-to-analog converter (DAC) devices, this report presents an implementation that is somewhat unique in that (1) it can be controlled and monitored externally by a computer through parallel ports, and (2) it can be programmed to hold a particular output, or to sweep over any portion of the output function without sweeping the entire range. These special features make this circuit particularly useful as a voltage source for the frequency modulation of an IMPATT oscillator, which is used as a microwave pump for the solid state masers used in the DSN as very low noise amplifiers. Since the waveform is determined by the operating characteristics of an individual maser, the use of an EPROM allows the waveform to be readily modified. The discussion of this particular application will be the subject, however, of another TDA report. In this report we describe the circuit and its operation.

II. Circuit Design and Description

The circuit described here provides a periodic voltage of amplitude from 0 to 10 volts, with 12-bit resolution, utilizing readily available components. In addition to the two requirements described above, this circuit is designed to provide an output symmetrical about one-half the total period.

Figure 1 shows a block diagram of the circuit. The symmetrical output is achieved by controlling a 12 bit up/down counter to count up continuously from a low value (low limit) to a high value (high limit) and then reversing direction (i.e., count down) until the low limit is reached again. This linear digital sweep produced by the counter is used as the address for the EPROM, whose output is then tied to the DAC where the output voltage is produced. (The output can be held constant by setting the high limit and the low limit equal to each other.)

Figure 2 shows the schematic for the clock oscillator, the low and high limit comparators and logic providing the up/down control, and the command decoder providing the external control. A brief description of each section is presented here.

A. Clock

The clock signal is generated by a (74C14) Schmitt trigger oscillator and is buffered by another Schmitt trigger. This signal is steered by the counter control logic to provide the count up and count down clocks for the binary counter. The clock frequency used in this application is 2 MHz, which at 32 point/period provides an output frequency of 60 kHz (2000 kHz/32).

B. Counter Control Logic

High and low limits supplied by the data bus are stored by hex latches (74C174) when enabled by the command decoder,

and compared to the EPROM address as provided on the counter bus. Cascaded 12-bit magnitude comparators (74C85) provide low/high limit signals to the up/down counter controller circuit, which when enabled on the positive clock transition drive the bidirectional binary counter. The logic insures that the counters start at known value and begin sweeping in the proper direction.

C. Command Decoder Circuit

Commands provided on the control bus are decoded by Intel (8205) 3 bit to 8 line decoders to provide four commands. U24 provides a card type select decoder, U23 a unit select, and U22 provides a command select. As implemented here, the command syntax is as follows.

bit	7	6	5	4	3	2	1	0	
	0	0	1	0	0	0	x	x	
	x	x	x	.	.	.	.	.	card type, 0 - 7
				x	x	x	.	.	unit number, 0 - 7
							0	0	run
							0	1	load low limit. hold
							1	0	load high limit, hold
							1	1	load low and high limit, hold

This syntax was chosen so that the command byte can be generated in software by ORing with masks.

Figure 3 shows the schematics for the binary counters, the EPROMs, the DAC, and output stages, which we describe here briefly.

D. Binary Counter

The binary up/down counter consists of three 4-bit presettable up/down counters (74C193) cascaded with the clear inputs disabled. A load high and low command causes the twelve bits on the data bus to be loaded simultaneously into the high and low comparators and the binary counters. The quality signals from both comparators prevent the clock signal from appearing at the count up or down clocks. Thus the address on the EPROM is a fixed value, and the output of the DAC will be held at the corresponding fixed voltage. In this manner the function can be swept through point by point by the external computer. If, however, the load high and low command is followed by a load low (or high) command. the binary counter and the low (or high) comparator are loaded with new data to be found on the data bus. Only one of the low (or high) comparators now shows equality, and the steering logic will cause the counters to ramp up (or down) starting at the low (or high) address entered. (There is nothing to prevent low value to exceed the high value. The counter will increase from the low value entered, wrap around the zero, and continue to increase *until the high value is reached, then reverse its direction.)* Since the EPROMs used here are Intel 2716 (2048 x 8), only the eleven counter bits 0 to 10 are used to provide the addressing. However, all twelve bits are used by the control logic.

E. EPROM

Two EPROMs are addressed in parallel to provide 16-bits of output data. Since the DAC chosen is a 12-bit converter, four of the data lines of the second EPROM are not used.

F. DAC and Output Stage

The DAC used here is the Analog Devices HDD1206SM, which has an integral sample and hold circuit to minimize the effects of switching transients, and is sufficiently fast to provide satisfactory operation at 2 MHz. Uniform switching transients are observed, and are measured to be less than 3×2^{-12} of the output with settling times less than 100 ns. Two op amps provide level shifting and buffering at the output, and two potentiometers allow for adjustments of offset and gain for 0 to 10 volt output.

III. Comments

The clock frequency is determined by the choice of R1 and C1. The command of the circuit at the bus can be modified at U22-U24. Alternately, the circuit can be hardware controlled by connecting the lines at U22, pins 1, 2, and 3 to a rotary switch. Straightforward modifications to the steering logic providing the load counter, count up clock, and count down clock will allow this circuit to sawtooth in either direction. In order to use 2732 EPROMs, the bit 11 output from the binary counter would be used to address the EPROMs. The overall performance of this function generator is dominated by that of the DAC. Adaptation of this circuit to more demanding specifications may dictate the use of a higher performance DAC. U21 is used here only as an active pull up for U6, U11, U14, U23, and U24, and four of the hex inverters in U30 are unused. The capacitors C5 through C26 denote by-pass capacitors for each IC.

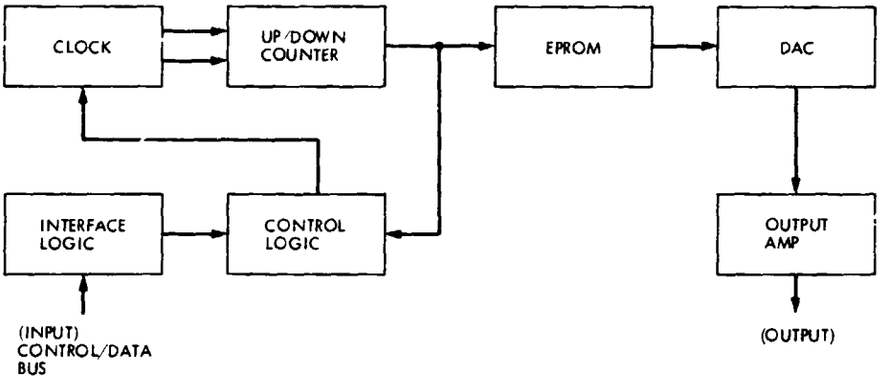

Fig. 1. The block dia- control logic, which is derived from a command on the bus, causing the up/down veep between two limits, also derived from the bus. The counter provides the EPROM, the output of which is converted to the desired analog signal by the ut stage provides scaling and buffering.

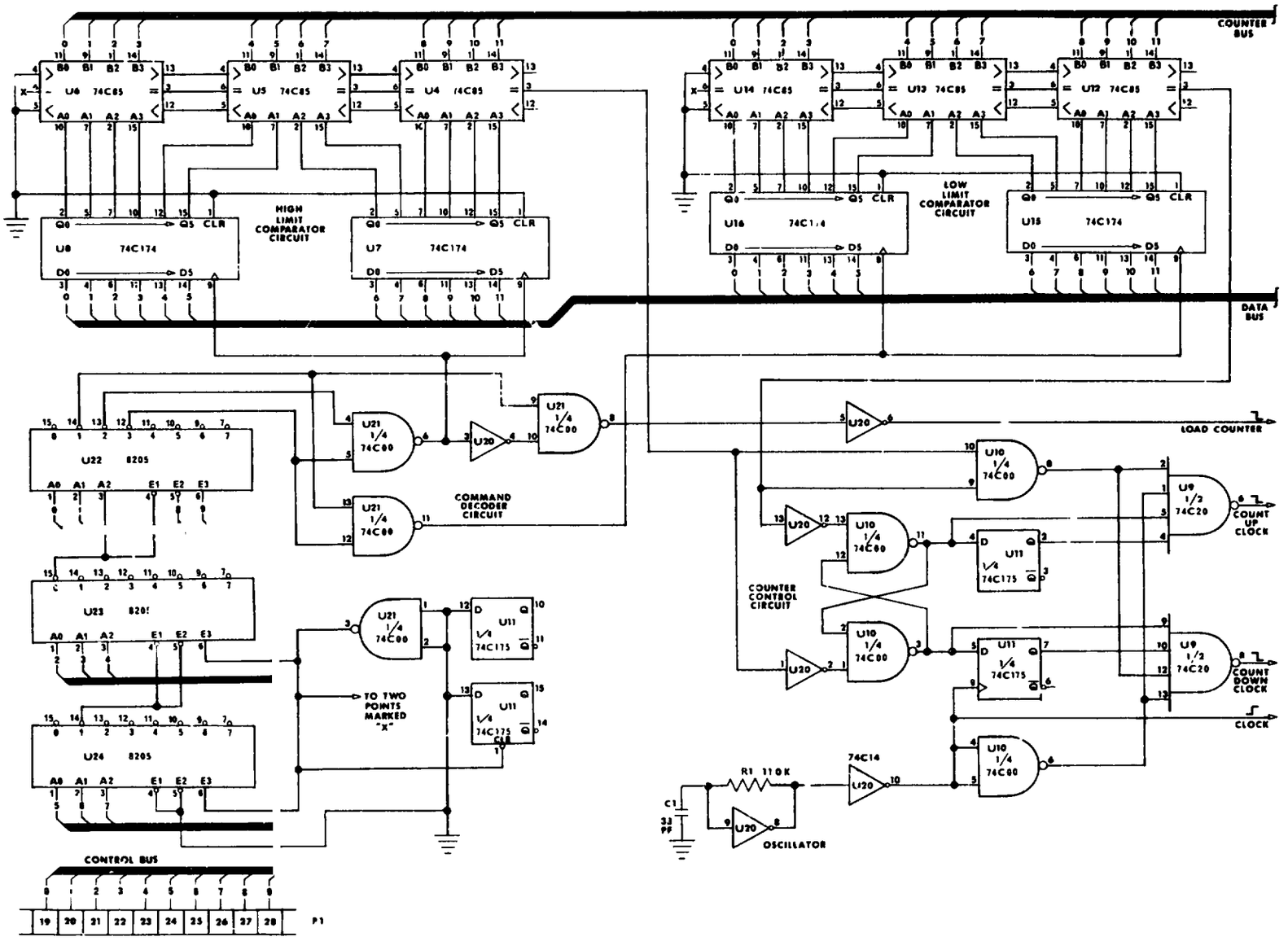

Fig. 2. Schematic of the command decoder and steering logic providing a linear up/down binary sweep, and thus an output waveform with even symmetry about half its period.

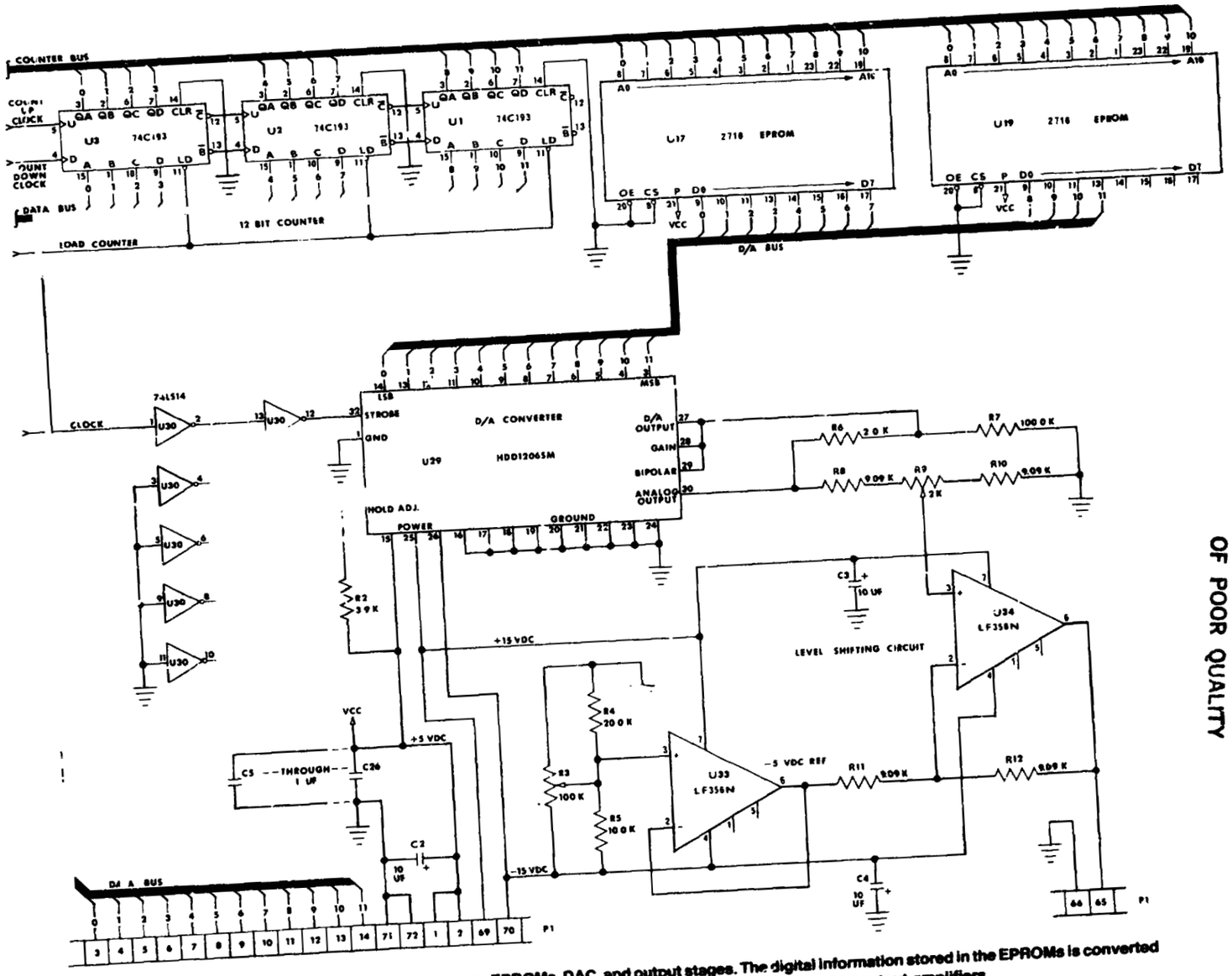

Fig. 3. Schematic of the binary counters, EPROMs, DAC, and output stages. The digital information stored in the EPROMs is converted to an analog signal by the DAC, and is scaled and buffered by the output amplifiers.