DEVELOPMENT & FABRICATION

OF A

HIGH CURRENT, FAST RECOVERY POWER DIODE

Allen-Bradley Company
Power Transistor Components
800 West Carson Street
Torrance, CA 90502

Contract Final Report No. CR-168196

Prepared for
National Aeronautics & Space Administration
NASA-Lewis Research Center
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1. Report No.	2. Government Accession No.	3. Recipient's Catalog No.
CR-168196		

4. Title and Subtitle	5. Report Date
Development and Fabrication of a High Current, Fast Recovery Power Diode	October 1983
	6. Performing Organization Code
7. Author(s)	8. Performing Organization Report No.
Albert H. Berman, Vilnis Balodis, Darrell C. Devance, Charles E. Gaugh, Eric A. Karlsson	
	10. Work Unit No.
9. Performing Organization Name and Address	
Allen-Bradley Company Power Transistor Components 800 West Carson Street Torrance, CA 90502	11. Contract or Grant No. NAS3-23280
	13. Type of Report and Period Covered
12. Sponsoring Agency Name and Address	Contract Final Report
National Aeronautics & Space Administration Lewis Research Center Cleveland, OH 44135	14. Sponsoring Agency Code

15. Supplementary Notes

Project Manager, Arvle Sundberg, Space Propulsion and Power Division, NASA-Lewis Research Center, Cleveland, Ohio

16. Abstract

A high voltage (V_R = 1200 V), high current (I_F = 150 A), fast recovery (< 700 ns) and low forward voltage drop (< 1.5 V) silicon rectifier has been designed and the process developed for its fabrication. For maximum purity, uniformity and material characteristic stability, neutron transmutation n-type doped float zone silicon is used.

The design features a hexagonal chip for maximum area utilization of space available in the DO-8 diode package, PIN diffused junction structure with deep diffused p^+ anode and a shallow high concentration n^+ cathode. With the high temperature glass-passivated positive bevel mesa junction termination, the achieved blocking voltage is close to the theoretical limit of the starting material. Gold diffusion is used to control the lifetime and the resulting effect on switching speed and forward voltage trade-off. For solder reflow assembly, trimetal (Al-Ti-Ni) contacts are used.

The required major device electrical characteristics have been achieved. Due to the trade-off nature of forward voltage drop and reverse recovery time, a compromise had to be reached for these values.

17. Key Words (Suggested by Author(s))	18. Distribution Statement
neutron transmutation doped silicon - gold diffusion - float zone silicon - theoretical voltage limit - positive angle bevel - high temperature glass passivation V_F versus t_{rr} trade-off	Unclassified - Unlimited

19. Security Classif. (of this report)	20. Security Classif. (of this page)	21. No. of Pages	22. Price*
Unclassifed	Unclassified		

* For sale by the National Technical Information Service, Springfield, Virginia 22161

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1.0 SUMMARY

The objective of this work was to develop a fast recovery 1000 volt, 150 ampere silicon diode as specified by NASA Contract NAS3-23280, dated March 12, 1982.

To meet the specifications of this contract, a PIN diffused structure was used. A positive bevel mesa structure with glass passivation was used for junction termination. This structure produced reverse blocking voltages close to the theoretical limit of the starting material.

Gold diffusion was used for lifetime control, a change from the previous work, NASA Contract NAS3-22539, which used electron irradiation. Gold diffusion resulted in faster switching speeds for a given forward voltage.

Metallization used for contacting the anode and cathode areas were of a tri-metal composition, which allows solder reflow assembly.

The devices were encapsulated in DO-8 diode packages. Processing details and device electrical performance are presented in the following sections.

2.0 INTRODUCTION

The NASA requirement in avionic systems for electrical power beyond the ten kilowatt level requires the use of a fast-switching, high voltage, high current transistor.

The use of a fast switching, high voltage, high current power transistor necessitates a fast switching, high voltage diode with equivalent power capability of the transistor.

The reverse recovery time of the diode would have to be shorter than that of the transistor by a factor of two in order to protect the transistor.

Diodes with these characteristics are used in snubber networks, as freewheeling diodes in inverter circuits and as rectifiers in high frequency power conversion equipment.

This combination of fast switch speed and high voltage required by the NASA specification is in the realm of the state-of-the-art of power semiconductor device fabrication.

The NASA requirement for such a high voltage, fast-switching diode is also a requirement for the industrial electronics market.

Specific applications are in electric vehicle motor drives, and both AC and DC motor controllers. The 1000 volt capability of the diode will have an application in industrial motor controllers where the bus line voltages are 480 volts. At the present time, two fast switching low voltage parts must be used in series to achieve the 1000 volt requirement and speed requirement at the expense of switching efficiency.

Diodes fabricated under this contract will be utilized in AC motor controller inverter circuits operating from 480 volt lines.

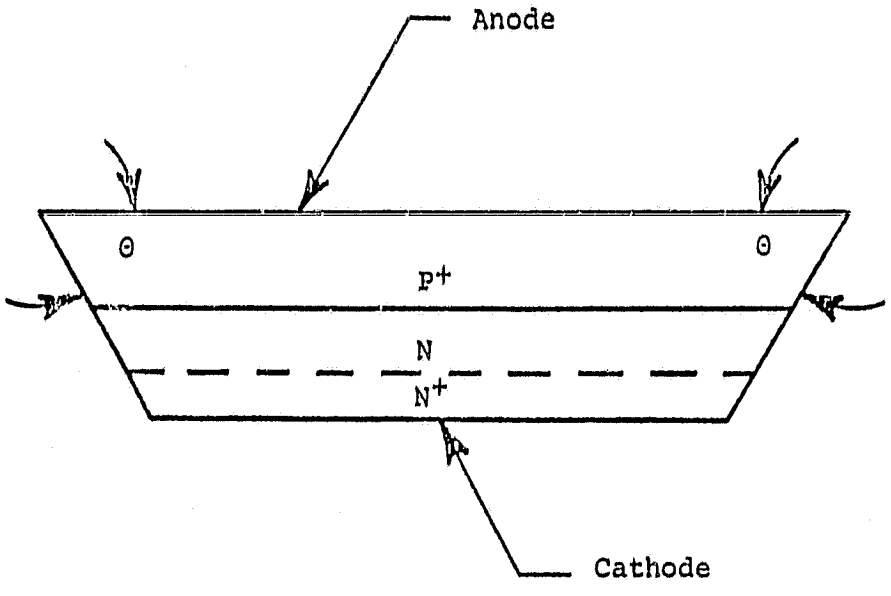
3.0 DEVICE DESIGN

3.1 Structure

The device is fabricated from 35 Ω cm thermal neutron transmutation n-type doped, float zone silicon. Float zone silicon exhibits high minority carrier lifetime and low oxygen and carbon content. Neutron transmutation doping involves the nuclear conversion of silicon atoms into phosphorus dopant atoms by exposing (intrinsic) silicon to a flux of thermal neutrons in a nuclear reactor core. The nuclear reaction is $Si_{14}^{30} + n \rightarrow P_{15}^{31} + e^-$. The silicon isotope Si_{14}^{30} absorbs a thermal neutron and becomes Si_{14}^{31}. Si_{14}^{31} is unstable and emits an electron to become P_{15}^{31}. This technique allows the fabrication of n-doped float zone silicon of extreme homogenity, i.e., small radial variations and reduced striations (resistivity microvariations); a result impossible by any of the other growing and doping methods. Low resistivity variations across the wafer minimizes the wafer thickness required as a function of the resistivity and the intrinsic layer minority carrier lifetime.

Terminating the p-n junction with a glass-passivated positive bevel moat allows the use of material with a relatively low resistivity level. The use of this material improves the trade-offs between blocking voltage, forward voltage drop and switch time.

The diode junction structure consists of a deep diffused P^+ anode and a shallow, high concentration N^+ cathode. See Figure 1. The structure allows for higher carrier injection into the low concentration intrinsic layer from both the anode and the cathode.



Θ = positive bevel angle

Figure 1 Surface Structure

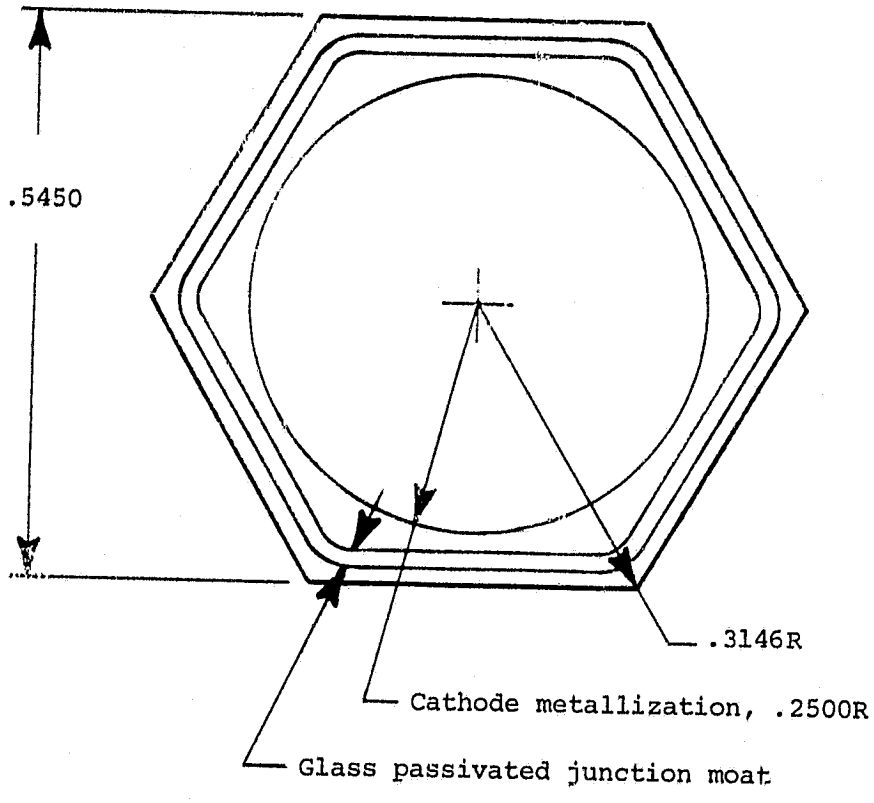


Figure 2 Surface Geometry

High level double injection provides a lower on-state potential (V_F) than either single injection or low level bipolar injection. The P^+-N junction terminates on a positive bevel wall of a moat that also defines the junction area of the device. High temperature hard glass, deposited in the moat during wafer processing, provides the required junction passivation.

Another factor affecting the forward voltage drop (V_F) is the active area of the device. To maximize the device area within the limits of a DO-8 package, a hexagonal geometry is employed. The contact is circular, and the moat is hexagonal. See Figure 2. The entire area within the moat will be active. The current density at 150 amperes is 150 A/1.53 cm^2 = 98.0 A/cm^2.

3.2 Voltage Requirements

From previous device design calculations and diffused junction impurity profile evaluation data, as reported in NASA Report Number CR-165411, the following parameters have been established to fabricate the device:

ρ_B = starting material resistivity = 35 Ω cm

N_B = background impurity conc. = 1.5×10^{14} atoms/cm^3

Nop = anode surface impurity conc. = 2.5×10^{19} atoms/cm^3

X_{jp} = p^+ anode junction depth = 140 μ

d = depletion layer width @ 1250 V = 92 μ

a = grade constant of the p^+ layer = 1.29×10^{17} atoms/cm^3

The positive bevel structure has been proven superior to planar and negative bevel structures. In a planar junction structure, premature breakdown can occur at the surface, leading to a concentration of current at

the edge and reducing the surge current capability of the device. Beveled structures exhibit considerably reduced surface fields as compared to bulk fields, resulting in uniform bulk breakdown.

The positive bevel angle forms a structure of decreasing cross-sectional area going from the heavily doped P^+ anode to the lightly doped N intrinsic region. As a first order approximation, the surface field of a positive bevel junction is reduced by a factor of sin θ; therefore, as the bevel angle is reduced, so is the peak electric field as it shifts into the lightly-doped region. The breakdown voltage of a positive bevel junction approaches the true bulk breakdown of a device. Using the previously established physical parameters, the maximum field, E_m, and the bulk breakdown voltage, V_B, are calculated.

Maximum field:

$$E_m = \frac{4 \times 10^5}{1 - 1/3 \log_{10}\left(\frac{N_B}{10^{16}}\right)} \text{ V/cm} \qquad [1]$$

$$N_B = 1.5 \times 10^{14} \text{ atoms/cm}^3$$

$$E_m = 2.49 \times 10^5 \text{ V/cm}$$

Breakdown voltage for a graded junction:

$$V_B = \frac{4E_m^{3/2}}{3}\left(\frac{2\varepsilon s}{q}\right)^{\frac{1}{2}} (a)^{-\frac{1}{2}} \qquad [2]$$

where

ε_S (semiconductor permittivity) = 1.06×10^{-12} F/cm

$\varepsilon_S = K\varepsilon_O$

K (dielectric constant of Si) = 12

ε_O (permittivity of space) = 8.85×10^{14} F/cm

F = 1 coulomb/V

therefore

ε_S = 1.06×10^{-12} coulombs/V cm

a (grade constant of P^+ layer) = 1.29×10^{17} atoms/cm^4

q (electron charge) = 1.6×10^{-19} coulomb

V_B = 1689 V

This analysis assumes that the breakdown voltage is not limited by intrinsic region thickness. To minimize forward voltage drop, it is important to optimize the intrinsic region thickness. This was done, using the experience gained during the work on NASA Contract NAS3-22539. For a more detailed discussion of voltage design considerations, refer to Section 3.2 of the final report for the above mentioned contract, Report Number CR-165411 (June 1981).

3.3 Reverse Recovery Time

Investigation of previous discussions and specifications of reverse recovery time has revealed that an error was made and propagated. In the proposal for this contract, RFP3-435433, an equation for t_{rr} as a function of recovery charge and current fall rate is derived:

$$Q_R = \tfrac{1}{2} t_{rr}^2 \left(\frac{dI_F}{dt}\right)$$

This equation is incorrect. The error was made as follows:

The equation

$$Q_R = \int_o^{t_{rr}} I(t)dt$$

is basically correct. Because t_{rr} is JEDEC defined as the time to recover to 10 percent of the maximum reverse current, the true equation is:

$$Q_R = \int_o^{t} I(t)dt, \text{ where } t = \text{time to recover to static reverse leakage current}$$

Because $I(t) = 0.1\ I_{RM}$ (REC) and falling at $t = t_{rr}$, errors introduced by assuming the first equation are typically only a few percent. The author(s) of the above referenced proposal next assumed:

$$I(t) = \left(\frac{dI_F}{dt}\right) t$$

This was then integrated to yield:

$$Q_R = \int_o^{t_{rr}} \left(\frac{dI_F}{dt}\right) t\ dt = \tfrac{1}{2} t_{rr}^2 \left(\frac{dI_F}{dt}\right)$$

The error is that $I(t) = \left(\frac{dI_F}{dt}\right) t$ only to time t_1 (See Figure 3) because $\left(\frac{dI_F}{dt}\right) t$ is fixed by the test circuit, assuming $I(t) = \left(\frac{dI_F}{dt}\right) t$ implies that $|I(t)|$ is a linearly increasing function of time through $t = t_{rr}$. For $I_R(t)$ to decrease from I_{RM} (REC) to $0.1\ I_{RM}$ (REC), the JEDEC definition of t_{rr}, it obviously must decrease at some time, a requirement that cannot be satisfied by a linearly increasing function. The problem can be illustrated by considering a typical reverse recovery wave form as shown in Figure 3.

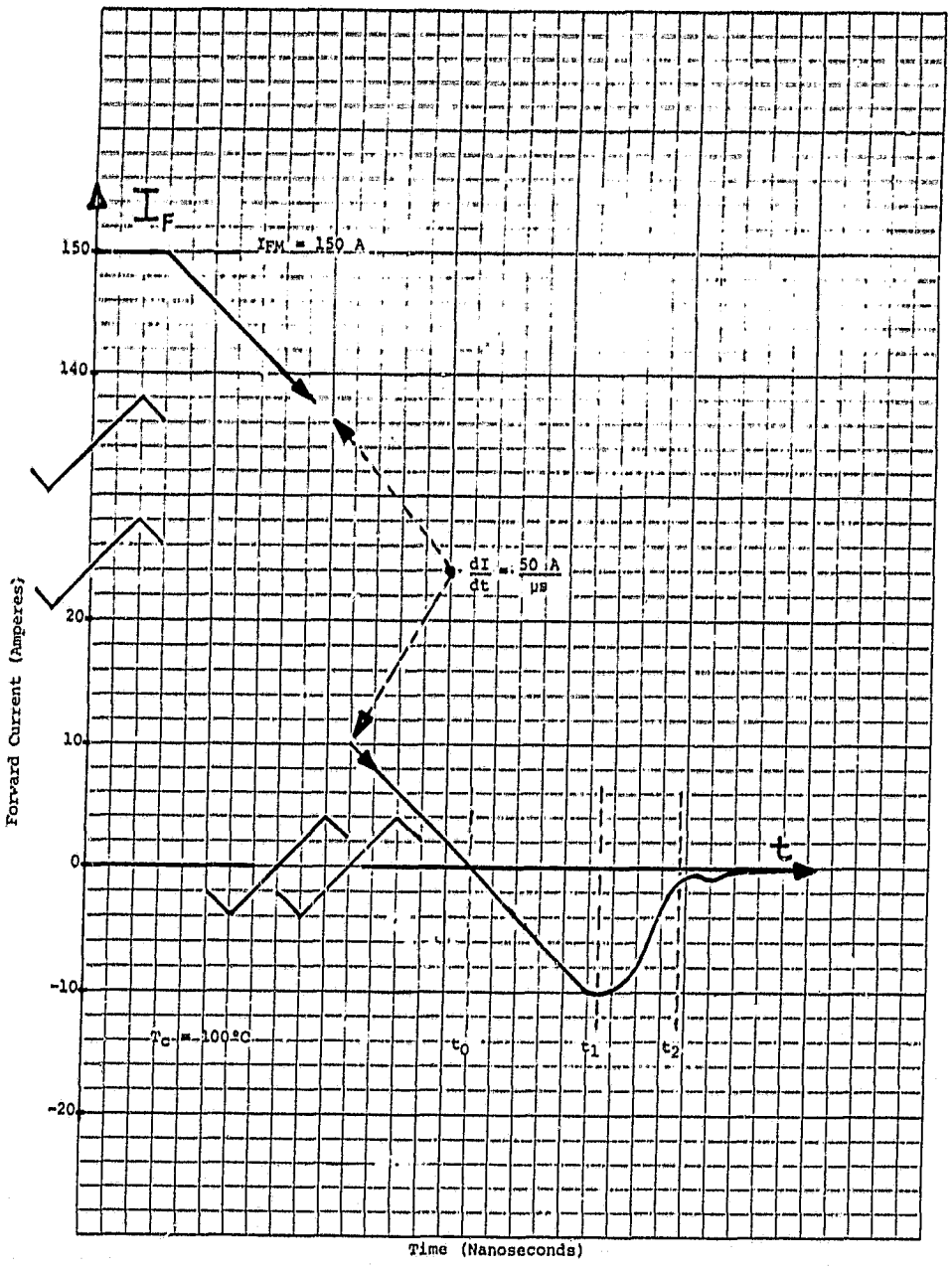


Figure 3 Reverse Recovery Waveform

Because $\frac{dI}{dt}$ is fixed by the test circuit until the peak reverse recovery current is reached ($t = t_1$), $I(t) = \left(\frac{dI_F}{dt}\right) t$ is true until $t = t_1$. It is only after $t = t_1$ that the recovery characteristics of the device are measured. Before this, the waveform is fixed by the test circuit. The assumption that $I(t) = \left(\frac{dI_F}{dt}\right) t$ for all times (as was done) is equivalent to assuming instantaneous recovery at $t = t_1$, or $t_{rr} = t_1$.

Because of this mistake, t_{rr} on the statement of work for this contract (NAS3-23280) was specified as 200 nanoseconds. Given the fall rate dI/dt = 50A/μs, and peak reverse recovery current I_{RM} (REC) = 10 amperes,

$$\frac{10\ A}{50\ A/\mu s} = 200 \text{ nanoseconds}$$

This is the time to reach the peak reverse recovery current and is fixed by the test circuit (t_1 on Figure 1). The true reverse recovery time must be larger than the 200 ns because the time from t_1 to t_2 must be added to the 200 ns determined by the circuit.

Correct equations describing the reverse recovery time involve solving the time-dependent diffusion equations describing the minority carrier distributions. These have been solved for a test circuit simpler than the JEDEC circuit [3,4]. The resulting transcendental equations for the simpler circuit are soluble only by numerical analysis (computer). Derivation and analysis of the corresponding equations for the JEDEC circuit is beyond the scope of this work.

One of the goals of this contract was to minimize the reverse recovery time while keeping the forward voltage drop below a maximum value. Exact equations were not needed to pursue this. Initial work experimented with electron radiation for minority carrier lifetime control, but gold diffusion was later selected because it has the best trade-off between forward voltage drop and reverse recovery time [5].

Table I

Typical t_{rr} Values

Typical t_{rr} values for the lots used for the final 50 unit shipment are presented below. Conditions: I_F = 150 amperes, T = 25°C, $\frac{dI}{dt}$ = 50 A/μs, JEDEC circuit.

LOT NUMBER	UNIT NUMBER	t_{rr} (NANOSECONDS)
26-II	1	653
	2	680
	3	654
	5	574
	6	644
27	4	658
	6	648
	9	700
	11	661
	12	646
28	1	690
	4	668
	5	606
	7	680
	8	633

When comparing these values to those achieved with the previous 50 ampere diode (Contract NAS3-22539), several factors should be kept in mind:

(1) Reverse recovery time is roughly proportional to $\frac{I_F}{I_R}$ [5, 6]. $\frac{I_F}{I_R}$ for the 50 ampere diode was $\frac{50}{5} = 10$. $\frac{I_F}{I_R}$ for the 150 ampere diode is $\frac{150}{10} = 15$. Thus, if construction was similar, one would expect 50 percent larger t_{rr} for the 150 ampere part simply due to the test circuit current specifications.

(2) Current fall rate for the 50 ampere diode was 25 A/μs, but for the 150 ampere diode is 50 A/μs. As mentioned, t_1 for the 150 ampere part is 10 A/(50 A/μs) = 200 ns. For the 50 ampere part, t_1 = 5 A/(25 A/μs) = 200 ns also. The stored charge removed during time t_1 is the area between the waveform and the X-Axis (Figure 3). For the 50 ampere diode, this is ½(200 ns) (5 A) = 5×10^{-7} coulombs. For the 150 ampere diode, ½(200 ns) (10 A) = 10^{-6} coulombs. The ratio of cathode areas for the 150 A/50 A devices is $(.2500/.1345)^2$ = 3.45 times more area for the 150 ampere part. Stored charge is proportional to the device area, so although the 150 ampere device has 3.45 times more area, only twice as much charge is removed during time t_1. This means time t_2 will be longer for the 150 ampere part because it will have proportionately more charge left to remove during the recovery period from t_1 to t_2. The effect of fall rate on t_{rr} is not considered in the literature because of test circuit differences, but our measurements have shown that the difference in t_{rr} may be as much as a factor of 3 when comparing a 50 A/μs rate to a 25 A/μs rate.

(3) It has been shown in theory and by experiment that storage time increases with diode diameter until very large diameters are reached [6]. The basic reason for this is that the diode sidewalls act as surface recombination sites, reducing excess carrier lifetime. If the device thickness is kept constant, as is the case in our work, then as the diameter is increased, proportionately less sidewall area is available for recombination. Another way to look at this is that as the diameter is increased, proportionately more charges are located far enough away from the sidewalls that they are more likely to recombine in the bulk than at the sidewall surface.

The overall effect of these factors was that the desired device characteristics were not achievable by a simple scale-up of the previous 50 ampere part. Development of a gold diffusion process to replace electron radiation as a lifetime control method delayed delivery of the final units, but the device performance that resulted was much closer to the desired characteristics.

3.4 Forward Voltage Drop

The forward voltage (V_F) drop across a PIN diode is the sum of five terms: the potential across the cathode intrinsic interface, V_o, the potential across the anode intrinsic interface (the p-n junction), V_1, and the drops through the cathode, intrinsic and anode regions, V_N, V_i and V_P.

$$V_F = V_o + V_1 + V_N + V_i + V_P \qquad (1)$$

The drops through the heavily doped cathode and anode, V_N and V_P, are small relative to the other terms and may be neglected for this estimation. From reference [9], equations 8 and 11:

$$V_o = \frac{1}{2\Theta} \ln (JdN_o^+/2N_{io}^2 qD) \qquad (2)$$

and

$$V_1 = \frac{1}{2\Theta} \ln (J_g P_o^+ N_o^{+2}/2N_{io}^4 qD) \qquad (3)$$

where Θ = q/KT = 38.6 volts^{-1}

J = current density = 98.0 A/cm^2

q = the electron charge = 1.6 x 10^{-19} coulomb

D = the diffusion coefficient of charge carriers

= 6.5 cm^2/s

d = the cathode width = 15 micrometers

g = the anode width = 150 micrometers

P_o^+ = the anode thermal equilibrium carrier concentration

= 1.5 x 10^{19} carriers/cc

N_o^+ = the cathode thermal equilibrium carrier concentration

= 2.5 x 10^{19} carriers/cc

N_{io} = the intrinsic carrier concentration

= 1.5 x 10^{14} carriers/cc for 35 Ω -cm silicon

The sum of (2) and (3) gives the total drop caused by the junctions.

$$V_j = V_o + V_1 = \frac{1}{\Theta} \ln (JN_o^+ (gdP_o^+ N_o^+)^{\frac{1}{2}}/2N_{io}^3 qD) \qquad (4)$$

V_j = 0.703 volts for the given conditions

The ohmic voltage drop through the intrinsic region is the integral of the electric field in the region

$$V_i = \int_o^W E(x)dx = \frac{J}{2Q\mu}\int_o^W \frac{dx}{N(x)} \qquad (5)$$

since the current $J = 2q\mu N(x) E(x)$

where μ = the carrier mobility = 250 $cm^2/V \cdot s$.

Equation (5) gives $V_i = 0.317$ V.

Therefore, the forward voltage drop at 150 A is

$$V_F = V_j + V_1 = 1.02 \text{ V}. \qquad (6)$$

This is less than the specified 1.5 volts at 150 A. This allows a margin for increase due to the effects of gold diffusion. A discussion of these effects follows in the next section.

3.5 Trade-Offs

Several of the electrical characteristics of this device are coupled. Improvement of one characteristic unavoidably degrades another.

Forward voltage drop and the reverse blocking voltage both depend on the intrinsic layer thickness. Increasing the intrinsic layer thickness will increase the reverse blocking voltage (to a point, when the breakdown voltage is no longer depletion width limited), but also increases the forward voltage. As mentioned in Section 3.2, intrinsic layer thickness has been optimized to produce the minimum forward voltage drop achievable while simultaneously satisfying the reverse blocking voltage requirement.

Trade-offs that result in more serious electrical limitations exist between forward voltage drop, reverse leakage current, and reverse recovery time.

When gold is diffused into the silicon lattice, two major effects take place. The first is that by introducing recombination centers, carrier lifetime is reduced. This has a direct effect on the reverse recovery time and on the reverse leakage current. Details of these effects follow. The other effect is that of carrier removal, which increases the resistivity of both the n and p-type regions [3]. Forward voltage drop is proportional to the resistivity, so it increases with increasing gold concentration.

To examine the trade-off between reverse leakage current and reverse recovery time, the following equations are reproduced from Peference [1]:

$$\text{Reverse leakage} = J_R = q\sqrt{\frac{D_P}{\tau_P}}\,\frac{n_i^2}{N_D} + \frac{qn_iW}{\tau_e} \qquad \text{[Equation (50), p.91]}$$

$$\text{Reverse recovery time} = t_1 + t_2 \approx \frac{\tau_P}{2}\left(\frac{I_R}{I_F}\right) \qquad \text{[Equation (89A), p.110]}$$

The first term in the expression for reverse leakage is called the diffusion term, the second is the generation component. In these expressions,

q = unit electronic charge

D_P = p-carrier diffusivity

τ_P = p-carrier lifetime

n_i = intrinsic carrier concentration

N_D = donor concentration

W = depletion region width

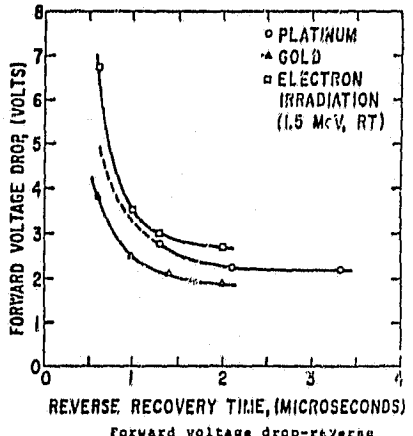
τ_e = effective lifetime (holes and electrons)

I_R = reverse current (fixed by test circuit)

I_F = forward current (fixed by test circuit)

For silicon at room temperature, the generation component of the reverse leakage dominates [4]. Given this, it can be seen that a decrease in carrier lifetime will result in a linear increase in reverse leakage accompanied by a linear decrease in reverse recovery time.

As it was, the limitation imposed by the forward voltage drop turned out to be more severe than that imposed by the reverse leakage specification. Thus gold diffusion processing was targeted to produce units with forward voltage drops close to the specification limit (1.5 V @ 150 A). Because the gold-diffused devices have the best trade-off between forward voltage drop and reverse recovery time of any lifetime control technology known [7], these devices should represent the state-of-the-art in terms of recovery time and forward drop for devices fabricated from silicon. A comparison of forward voltage drop versus reverse recovery time for the various methods of lifetime control is reproduced from the work [7].



Forward voltage drop-reverse recovery time trade-off curves for gold diffused, platinum diffused and electron irradiated silicon.

4.0 WAFER PROCESSING

The processes and major processing steps are outlined in Figure 4.

4.1 Diffusions and Oxidation

Spin-on liquid boron or a high temperature boron nitride planar source is used for p^+ deposition, followed by high temperature drive-in diffusion.

The n^+ cathode layer is formed by liquid source phosphorus ($POCl_3$) deposition and drive-in diffusions. The initial oxidation utilized a pyrogenic oxidation system. All of these processes are in routine use at Power Transistor Company.

4.2 Lap and Polish

The p^+ layer is removed from one side of the wafer by mechanical lapping, thereby exposing the original starting material. The required intrinsic layer thickness is also established at this time. To provide adequate surface finish for subsequent moat and cathode geometry formation, the surface is chemically polished. (Figure 4, C).

4.3 Gold Diffusion

After lap and polish, the n^+ cathode layer described in 4.1 is fabricated, (Figure 4, D). Oxide is then removed from the anode p^+ layer, and a thin (less than 100 angstroms) layer of gold is deposited on the anode by electron beam vacuum evaporation.

The gold is diffused into the silicon in a high temperature diffusion tube, and any excess gold is removed with aqua regia.

4.4 Positive Angle Bevel

The positive angle bevel is formed during the moat etch. Standard photoresist masking and silicon etching techniques are used. The moat is formed by etching through the n^+/n cathode region and some distance into the p^+ anode layer (Figure 4, E). Since the angle of the bevel determines the field at the junction, and therefore, the breakdown voltage of the device, close control of the etch process is essential.

4.5 Glass Passivation

After the mesa formation, the junction is exposed to contamination in subsequent processing steps. To prevent this as well as ensure future reliability during the high current, high voltage temperature glass passivation is performed to seal the mesa junction.

The glass, suspended in a binder, is deposited in the freshly etched and cleaned moat. In a two-step operation, the binder is burned off and the glass fired at temperatures in excess of 700°C to fuse the glass to the walls of the mesa (Figure 4, F).

Relative to the 50 ampere device, the 150 ampere device requires a considerable increase in area, therefore, the junction periphery in the moat is also increased. The relatively deep moat, coupled with the extended length, required some adjustments to the glass process to prevent cracking.

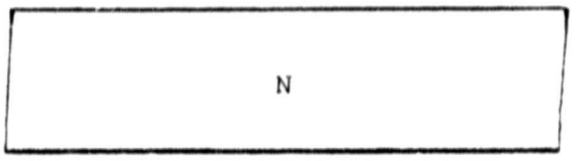
4.6 Metallization

A metallization process that is compatible with glass-passivated junctions and provides solderable contacts to cathode and anode was developed under NASA Contract Number NAS3-22539 and reported in the final report NASA CR-165411. The same process is used for this device.

The metallization consists of a trimetal system - aluminum, titanium and nickel. A sintered aluminum layer established low resistance ohmic contact to the silicon surfaces of anode and cathode. Nickel forms the top layer of the trimetal system and provides solderable contact required for solder reflow assembly. A thin layer of titanium is used as a barrier to prevent nickel from diffusing through the aluminum during the metal sintering step.

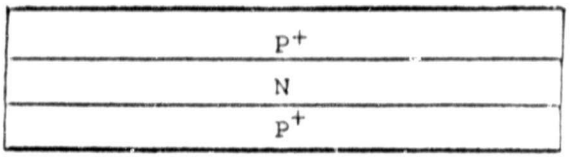
Starting material wafer, neutron doped N-type silicon

A



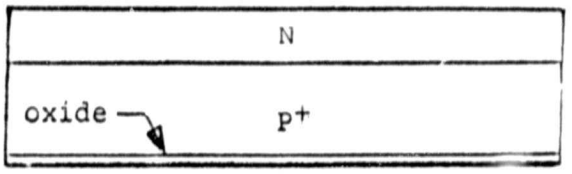
Boron deposition and drive in diffusion to form anode P^+ layer

B



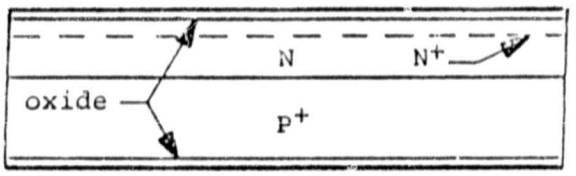
Single side lap & polish oxidation and oxide removal from cathode side

C



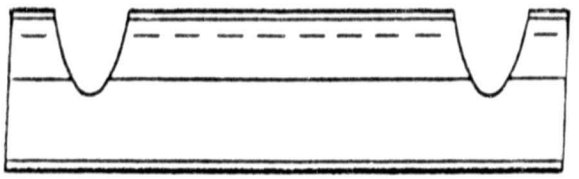
Phorphorus deposition and drive-in diffusion to form N^+ cathode layer

D



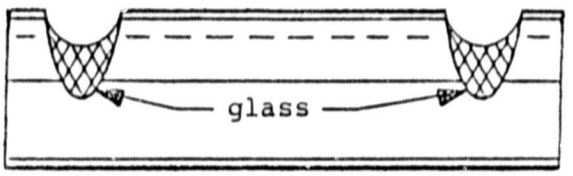
Photoresist mask, oxide and moat etch to form positive angle bevel

E



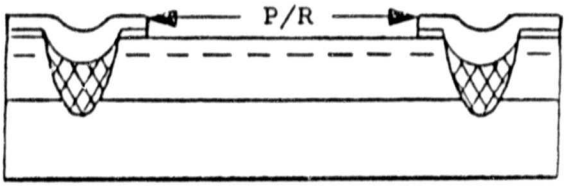
Hard glass passivation of the P/N junction in the moat

F



Contact photoresist and oxide etch to define anode and cathode areas

G



Anode and cathode three layer metallization

H

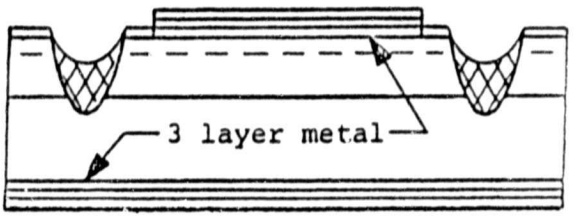


Figure 4 Process Sequence Outline

5.0 ENCAPSULATION

5.1 Package

The device is encapsulated in a JEDEC standard DO-8 assembly, Drawing Number 50-0047, utilizing a soft solder reflow process and hermetically sealed by a resistance welded cap. A ceramic to metal seal cap is used to provide sufficient surface insulation between cathode and anode terminals.

The specifications of the assembly components are detailed in the following drawings:

DO-8 stud - 50-0083

DO-8 cap - 50-0082

Solder-clad moly tab - cathode - 50-0084-2

Solder-clad moly tab - anode - 50-0084-1

Internal lead - 50-0085-2

External lead - 50-0109

5.2 Assembly

In a one-pass solder reflow process, the die is mounted on the nickel-plated stud platform and the internal lead attached. Solder-clad molybdenum preforms form the metallurgical bond between the nickel-plated assembly components (Figure 5).

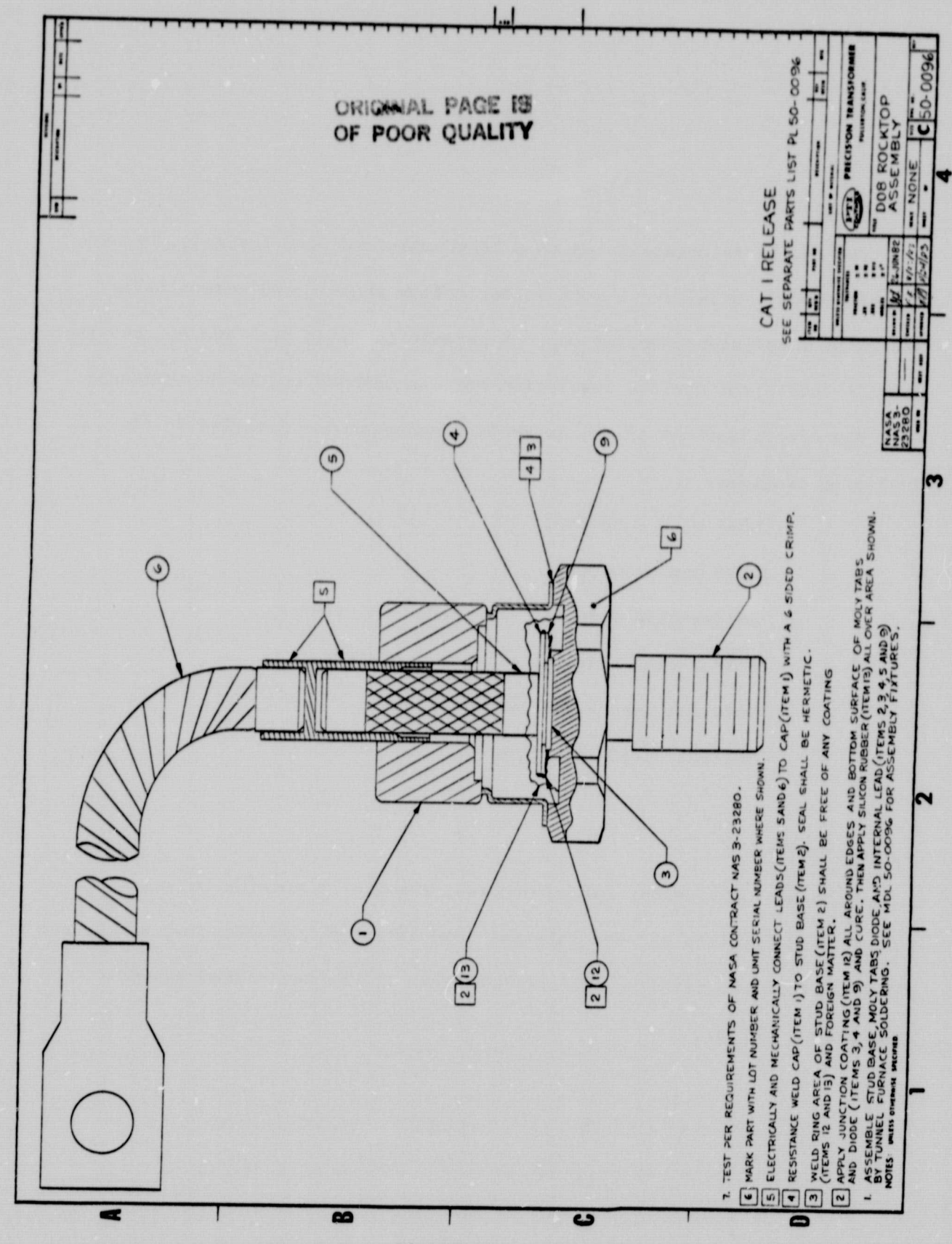


Figure 5

Assembly Drawing 50-0096

ITEM	QUAN.	PART NUMBER	DESCRIPTION	VALUE / TYPE NO.	VENDOR PART NO.	VENDOR NAME
1	1	50-0082	CAP - D08 ROCKTOP			
2	1	50-0083	STUD BASE - D08 ROCKTOP			
3	1	50-0084-1	MOLY TAB, ROUND, SOLDER CLAD			
4	1	50-0084-2	MOLY TAB, ROUND, SOLDER CLAD			
5	1	50-0085-2	LEAD, INTERNAL, D08			
6	1	50-0109	LEAD, EXTERNAL, D08			
7						
8						
9	A/R	40-0002-630	DIODE, PHOTORESIST MASK - TURNING POINT			
10						
11						
12	A/R		SEMICONDUCTOR JUNCTION COATING		V-131	VISILOX
13	A/R		SILICON RUBBER		3140 RTV	DOW CORNING
14						
15						
16	REF	50-0047	POWER DIODE - D08 ROCKTOP			

DRAWN BY	DATE	ENGINEER	DATE	CHIEF ENG.	DATE	NEXT ASSEMBLY	TITLE
WZ	29 JUN 82	E.K.	8/23/83	WSJ	8/24/83	—	D08 ROCKTOP ASSEMBLY

		MODEL NO.	USED ON		DWG NO	REV
	SHEET OF	CAT 1 RELEASE	NASA NAS3-23280	PL	50-0096	

pti-12

Figure 5a: Parts Lists for Figure 5

Power Transistor Co.
800 West Carson Street,
Torrance,California,90502.
(213) 320-1190

PART #_____ ASSEMBLY LOT TRAVELER LOT #_____

INPUT_____ NASA 150A HIGH VOLTAGE DIODE DIFF LOT #_____
REFLOW FURNACE PROCESS

DATE

PROCESS PROCESS SPEC. NO.	QUANTITY IN	 OUT	OPR	DATE	PROCESS INSTRUCTIONS AND CONTROL
DIE MOUNT					Fixtures: Dwg. No. 50-0092; 50-0093; 50-0094 Assembly parts: Dwg. No. 50-0083; 50-0084-1 & -2; 50-0085
REFLOW FURNACE					Profile: 515/505/450/350 Gas flow: 60/80/60 Belt speed: 11.2cm/min
VISUAL INSPECT					Check for continuous solder fillets
ELECTRICAL INSP.					Checks for shorts Dead shorts Qty=_____
HIGH VOLT. COAT					Visilox V-131 Use syringe
VACUUM BAKE					T=150°C; t=12hours Min. Vacuum >20in Hg
2nd PASSIVATION					Dow Corning 3140 RTV
CURE					Room temperature Overnight
BAKE					T=150°C; t=2hours
CAP					8 CFM N2; CAP DWG. No. 50-0082 1hour prior to capping
HEX CRIMP					

Figure 5b Assembly Lot Traveler

The reflow process assembly is performed in a belt furnace. After the assembly furnace pass, the glass passivated moat region of the die is coated with Visilox high voltage junction coating number V-131. Prior to capping, Dow Corning RTV 3140 is applied for additional insulation and protection against possible weld arcing during capping.

The assembly is completed into a hermetically sealed unit by resistance welding the cap to the DO-8 stud. This operation is performed in a dry nitrogen ambient, achieving inert conditions inside the encapsulation cavity. Gross leak test is performed for 100 percent of the devices. A braided external lead is crimped to the cap to provide convenient connection to the cathode. An Assembly Lot Traveler is shown in Figure 5b.

5.3 Thermal Ratings

Junction temperature is determined by the total power dissipation in the device P_T, the ambient or case temperature T_C, and the thermal resistance Θ_{JC} from junction to case.

$$T_J = T_C + \Theta_{JC} P_T$$

The basic equation for the conduction of thermal energy is:

$$Q = \frac{KA}{L} \Delta T = \frac{KA}{L} (T_1 - T_2)$$

where Q = heat flow/unit of time

K = thermal conductivity constant, W/cm, °C

A = area of thermal path, cm^2

L = length of thermal path, cm

T_1 = temperature of heat source, °C

T_2 = temperature of heat sink, °C

rewritten

$$Q = \frac{T_1-T_2}{L/KA} = \frac{T_1-T_2}{\Theta}$$

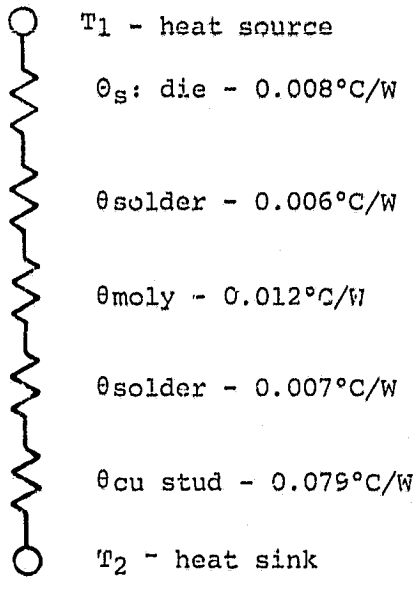
and $$\Theta = \frac{L}{KA}$$

The thermal spreading is taken into consideration by applying the following equation for circular-geometry:

$$\Theta circle = \frac{L}{K\pi(r^2 + rL)}$$

where r = radius of the circle

The equivalent thermal resistance diagram below shows the thermal conductive path considered and the calculated theoretical values of each thermal resistance element.



This consideration is limited to a situation in which heat from the device is removed by conduction to a heat sink only. The cooling of the device by convection and radiation from the device enclosure above the heat sink to the air is negligible and therefore neglected in the calculations. The resulting theoretical junction to case thermal resistance, θ_{JC} is 0.11°C/W.

6.0 TEST

6.1 Test Plan

1. Expose all diodes to 3000 A nonrepetitive peak surge current.
2. Screen on Tektronix 576 curve tracer for:
   a. I_R = 100 μA MAX. @ 800 V
   b. V_F = 1.51 V MAX. @ 150 A
3. Serialize and trademark.
4. Read and record reverse recovery time at T_C = 100°C.
5. Read and record forward voltage at I_F = 150 A.
6. Read and record DC blocking voltage at T_C = 25°C and T_C = 150°C.
7. Read and record maximum reverse current at rated V_{RRM} and T_C = 25°C and T_C = 150°C.
8. Select deliverable diodes that meet the "specifications".
9. Select samples and generate characteristic curves for:
   a. Capacitance versus reverse voltage.
   b. Forward voltage versus forward current.
   c. Reverse current versus reverse voltage as a function of temperature.

The required specification read and record data of the deliverable diodes is tabulated in Table II. The test equipment and procedures of the tests are discussed in the following paragraphs.

6.2 Nonrepetitive Peak Surge Current, I_{FSM}

As a potentially destructive test I_{FSM} has been performed to screen all devices prior to serializing and performing any other tests. All devices were exposed to over 3000 A half-cycle to insure compliance with the 3000 A requirement.

The major components of the 3000 A peak surge tester are: thumb-wheel transformer selecting switch, diode and power transistor module firing circuit, ten transformers with a high current secondary, a .01 Ω current sensing resistor, and an oscilloscope - connected as shown in Figure 6.

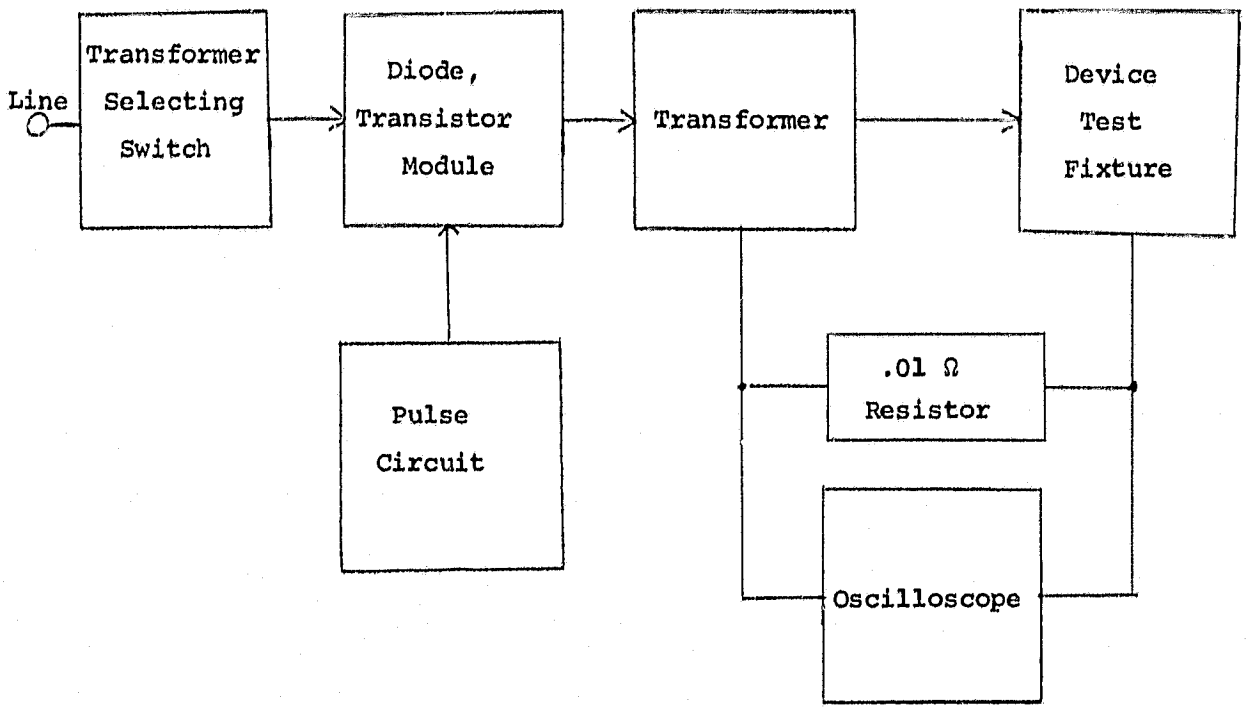
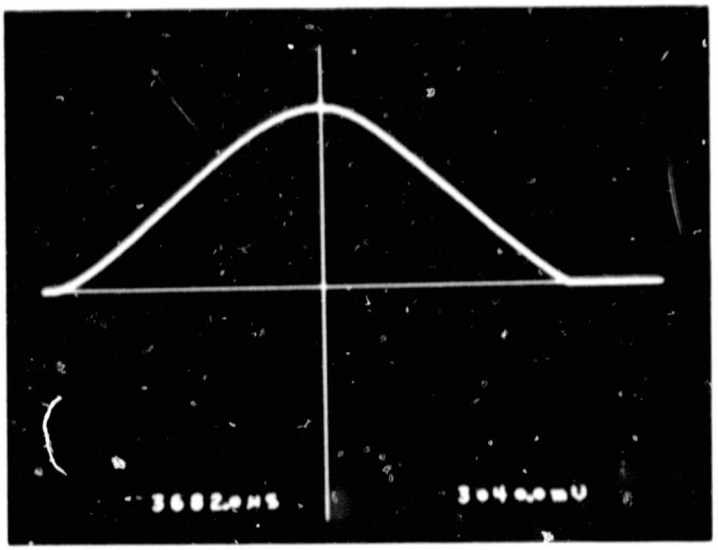
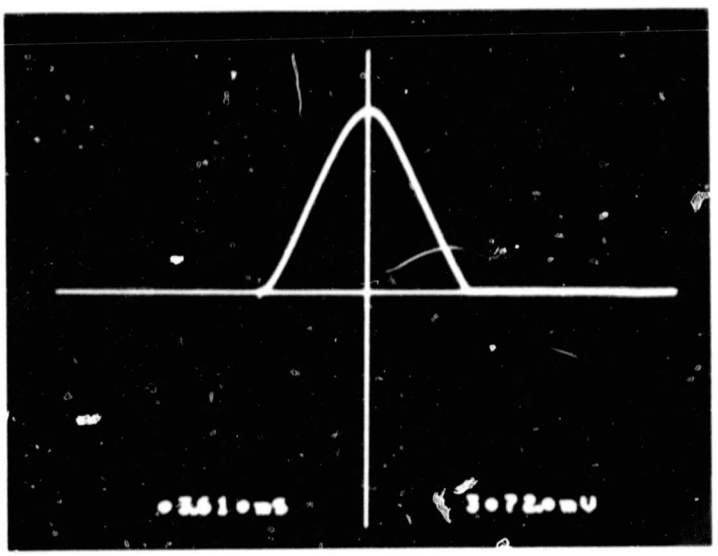


Figure 6
Test Circuit Block Diagram



Scale: 1 mV = 1 A



Scale: 1 mV = ? A

Figure 7 Peak Surge Current Pulse

The device under test is clamp-held in a safety test fixture, while a high current pulse, triggered by the SCR firing circuit, is applied. The amplitude of the current pulse is determined by observing the voltage pulse across the noninductive one milliohm resistor in series with the diode, as displayed on the oscilloscope. See Figure 7. The variac is adjusted for the required pulse amplitude.

Following the high current surge test, a survivor screening test was performed using a Tektronix 576 curve tracer. At room temperature the diodes were tested for:

$$I_R = 100\ \mu A\ MAX\ @\ 800\ V$$

and $$V_F = 1.51\ V\ MAX\ @\ 150\ A$$

Units that passed the series of tests were serialized for the subsequent read and record tests.

6.3 Reverse Recovery Time, t_{rr}

The reverse recovery test was performed in a JEDEC type test circuit.

The current through the diode is reduced at a rate of 50 A/μs. When the sign of the current through the diode changes, the zero reference line is established. The measurement of the reverse recovery time is made from that point (t_0) to its maximum negative value (t_1) and to the approximate point where the reverse current has returned to 10 percent of its maximum value, I_{RM} (REC.).

The diodes were stabilized at 100°C in an oven. Using the reverse recovery test circuit, set at I_{FM} = 150 A and dI/dt = 50 μs, the t_{rr} was read on a custom fabricated digital readout t_{rr} tester and recorded for each unit.

6.4 Forward Voltage, V_{FM}

A Tektronix Model 576 curve tracer with a Model 176 pulsed high current adapter was used to measure the forward voltage drop at I_F = 150 A. A typical V_{FM} characteristic trace is shown in Figure 8 , as displayed on the Tektronix 576 curve tracer.

6.5 DC Blocking Voltage, V_R

The blocking voltage at 25°C, 500 μA and at 150°C, 5 mA was read on Tektronix 576 curve tracer.

6.6 Reverse Current, I_R

Utilizing Tektronix 576 curve tracer in the Leakage Mode, the reverse leakage current was recorded for V_R = 800 V at T_C = 25°C and for V_R = 800 V and 1000 V at T_C = 100 °C.

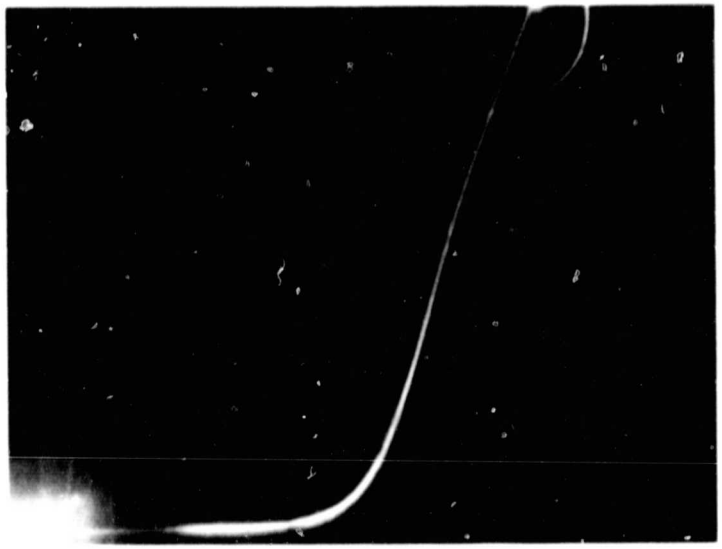
All high temperature characteristics were read and recorded with the devices heated in an oven and stabilized at the required elevated temperature.

Lot – Device Number	V_F @ 150 A Volts	V_R @ 500 μA T_C = 25°C Volts	V_R @ 5 mA T_C = 100°C Volts	I_R @ 800 V T_C = 25°C μA	I_R @ 100°C mA 800 V	1000 V	t_{rr} From 150 A $\frac{dI}{dt}$ = 50 A/μs Nanoseconds T_C = 25°C	T_C = 100°C
26-1A	1.45	1160	790	40	5.2	6.8	600	816
26-1	1.42	1120	980	75	3.9	5.2	653	886
26-2	1.28	1160	1000	50	3.3	5.0	680	916
26-3	1.44	1080	970	70	4.0	5.4	654	895
26-5	1.50	1300	850	50	4.8	5.7	574	822
26-6	1.42	1120	1040	50	3.8	4.8	644	858
26-8	1.32	1200	1030	60	3.6	4.7	658	884
27-4	1.48	1150	1030	60	3.7	4.8	658	926
27-6	1.50	1250	1040	40	3.7	4.7	648	906
27-9	1.40	1120	1080	50	3.4	4.2	700	959
27-11	1.48	1220	1075	50	3.2	4.4	661	891
27-12	1.50	1100	1030	40	3.9	4.8	646	886
27-13	1.44	1200	1065	50	3.6	4.5	679	943
27-14	1.44	1120	1035	50	3.3	4.6	680	946
27-15	1.46	1160	1020	60	3.5	4.9	691	952
27-16	1.49	1180	1080	50	3.4	4.3	697	967
27-17	1.48	1240	950	60	4.1	5.7	628	876
27-18	1.47	1120	1000	80	3.7	5.0	690	945
27-21	1.40	1250	1060	60	3.5	4.4	678	938
27-23	1.44	1120	1040	60	3.5	4.5	668	950
27-28	1.38	1210	940	50	4.2	5.8	651	906
27-29	1.50	1220	960	60	4.3	5.5	657	922
28-30	1.30	1150	920	70	3.5	4.8	695	959
27-31	1.46	1040	1025	40	3.8	4.8	675	960
27-32	1.46	1200	1040	40	3.7	4.8	678	970
27-34	1.46	1040	980	40	4.0	5.3	648	949
28-01	1.35	1280	1085	20	3.6	4.4	690	942
28-04	1.28	1200	1005	20	3.5	5.2	668	905
28-05	1.44	1180	900	25	4.6	5.9	606	845
28-07	1.40	1320	1050	20	3.6	4.5	680	929
28-08	1.40	1320	990	20	4.1	5.1	633	861
28-09	1.44	1220	975	20	4.2	5.4	662	919
28-10	1.50	1450	1040	25	4.1	4.5	668	921

Table II Delivered Test Data

Lot - Device Number	V_F @ 150 A Volts	V_R @ 500 µA T_C = 25°C Volts	V_R @ 5 mA T_C = 100°C Volts	I_R @ 800 V T_C = 25°C µA	I_R @ 100°C mA 800 V	1000 V	t_{rr} From 150 A $\frac{dI}{dt}$ = 50 A/µs Nanoseconds T_C = 25°C	T_C = 100°C
28-11	1.34	1250	1085	15	3.8	4.5	691	960
28-12	1.42	1450	1060	20	3.7	4.5	693	965
28-13	1.50	1350	965	20	4.4	5.4	580	836
28-15	1.50	1200	1030	30	3.7	4.6	621	828
28-16	1.32	1280	840	15	4.8	6.2	695	952
28-18	1.46	1400	1000	25	4.3	5.0	648	885
28-20	1.40	1380	1050	15	3.8	4.6	684	959
28-21	1.42	1360	1030	20	4.0	4.8	652	892
28-50	1.42	1320	1120	40	3.6	4.1	674	937
28-51	1.32	1160	1105	30	3.2	3.9	684	944
28-52	1.32	1130	1050	40	3.5	4.5	695	903
28-53	1.36	1300	1120	35	3.4	4.0	699	986
28-55	1.40	1200	1200	30	3.3	3.7	697	982
28-56	1.36	1220	1105	30	3.4	4.1	691	961
28-57	1.50	1380	1040	35	4.1	4.7	665	908
28-58	1.32	1200	1070	30	3.3	4.1	690	973
28-60	1.42	1160	1010	40	3.9	4.9	652	896
28-61	1.40	1240	1150	35	3.3	4.9	694	974
28-62	1.48	1040	840	60	4.9	6.5	619	822
28-63	1.50	1040	860	45	4.6	6.4	621	835
28-65	1.48	1360	1100	40	3.8	4.5	655	914
28-66	1.40	1070	1030	35	3.7	4.6	634	889
28-67	1.44	1160	1140	40	3.4	4.1	682	944

Table II Delivered Test Data (Cont'd)



Scale: 200 mV/Division Horizontal
20 A/Divison Vertical

Faint trace is hysteresis loop.

Figure 8 Forward Voltage Curve

7.0 ELECTRICAL PERFORMANCE

7.1 Characteristic Curves

Five devices, Numbers 7, 8, 10, 13 and 18 were chosen as typical and three characteristic curves were generated for each device: Forward Voltage Drop Versus Forward Current (Figures 9-13), Reverse Leakage Current Versus Reverse Voltages at Six Temperatures (Figures 14-18), and Capacitance Versus Reverse Voltage (Figures 19-23). Average leakage current of the five units versus temperature is plotted (Figure 24).

V_F versus I_F was plotted from 100 mA to 200 A using a Tektronix Model 576 curve tracer with a Tektronix Model 176 pulsed current adapter.

The leakage current versus reverse voltage curves were generated by heating the diodes in an oven, stabilizing and then measuring the leakage at 200, 400, 600, 800, 1000 and 1200 volts on a 576 curve tracer. The electrical fixturing in the oven did not include heat sinks. Because of this, onset of thermal runaway was observed when leakages above 15-30 milliamperes were generated. To prevent permanent device degradation, leakage values at 125°C V_R = 1000, 1200 V and 150°C V_R > 200 V were not measured. Thermal runaway should not result if the devices have proper heat sinking. By plotting the average leakage current of the devices at 800 volts against temperature on a semi-log graph, a straight line results. This indicates the leakage increases exponentially with temperature. See Figure 24.

Capacitance was plotted against reverse voltage by using a Boonton Model 72BD capacitance meter and a Hyland high voltage power supply. The resulting curve is a straight line on logarithmic graph paper. The capacitance plot was terminated at 300 volts due to the maximum limitations of the test equipment.

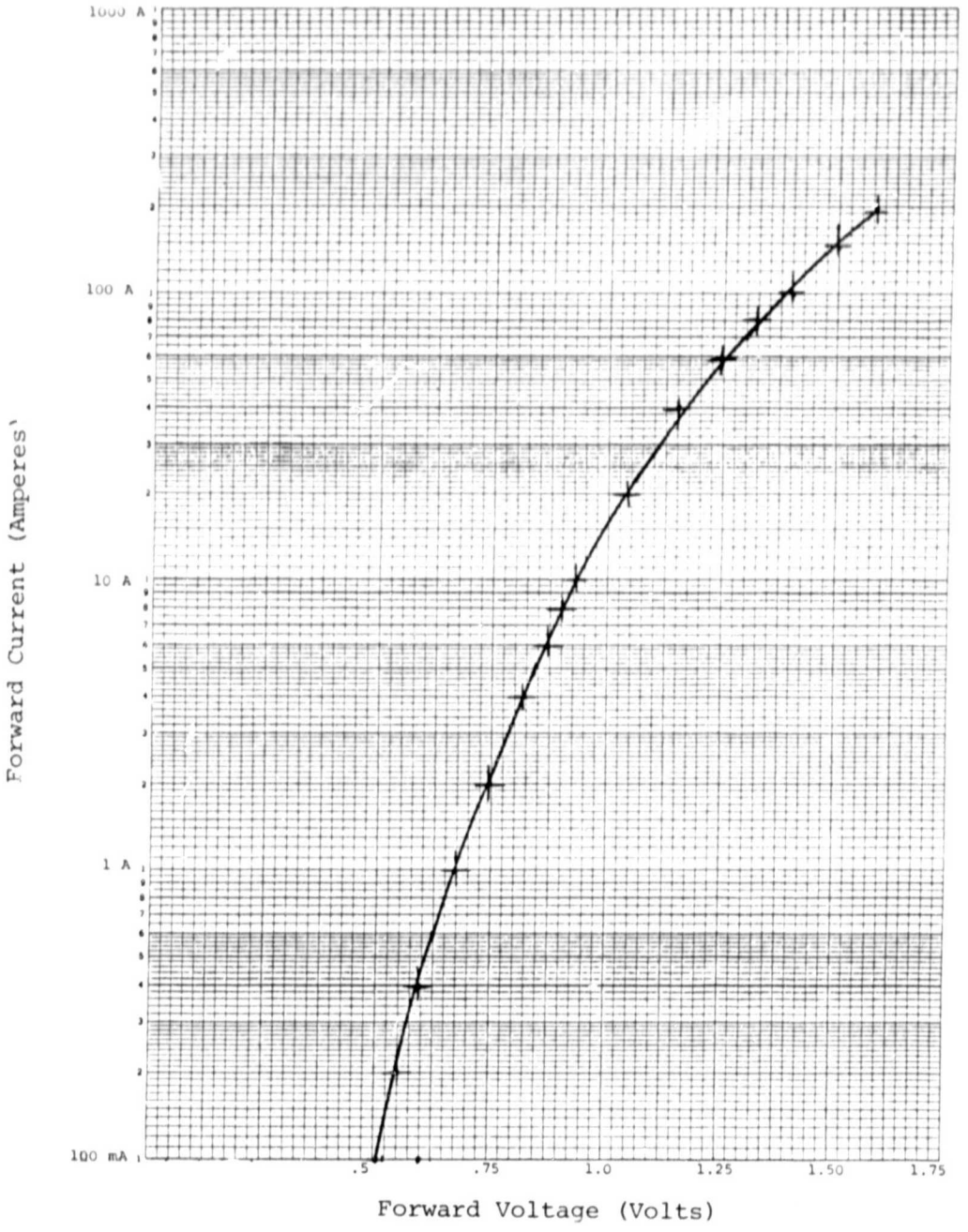


Figure 9 Device #28-7 Forward Characteristic Curve

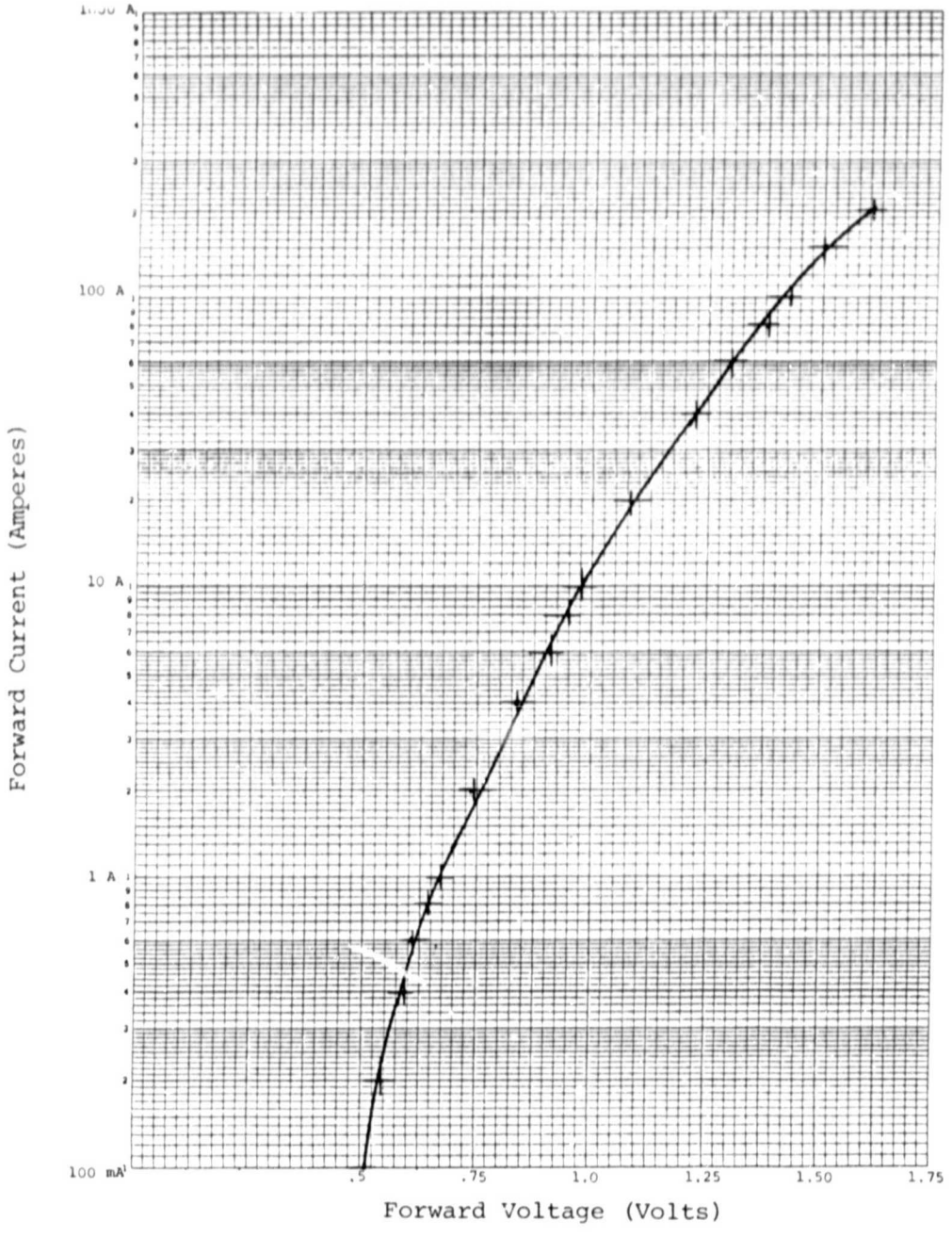


Figure 10 Device #28-8 Forward Characteristic Curve

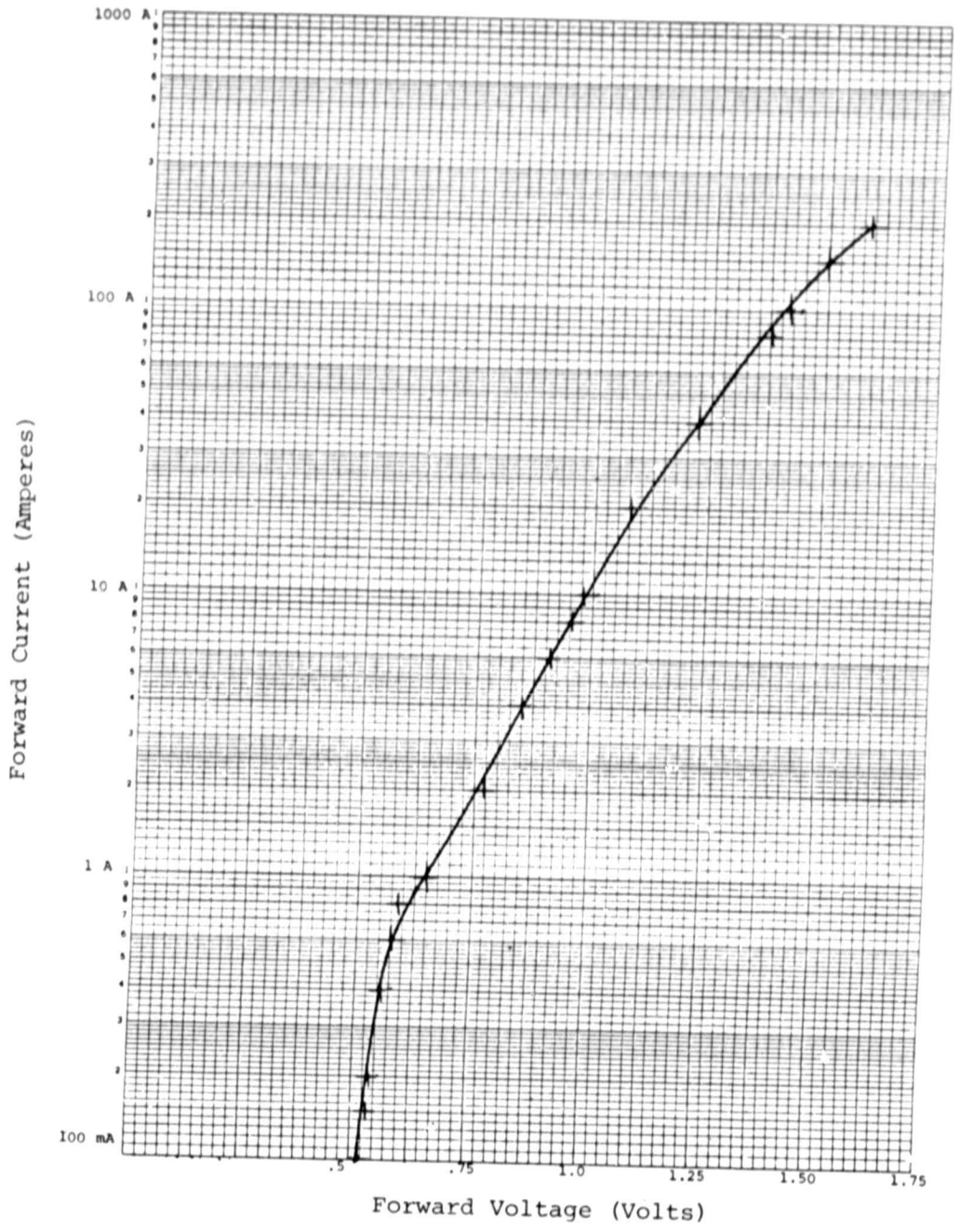


Figure 11 Device #28-10 Forward Characteristic Curve

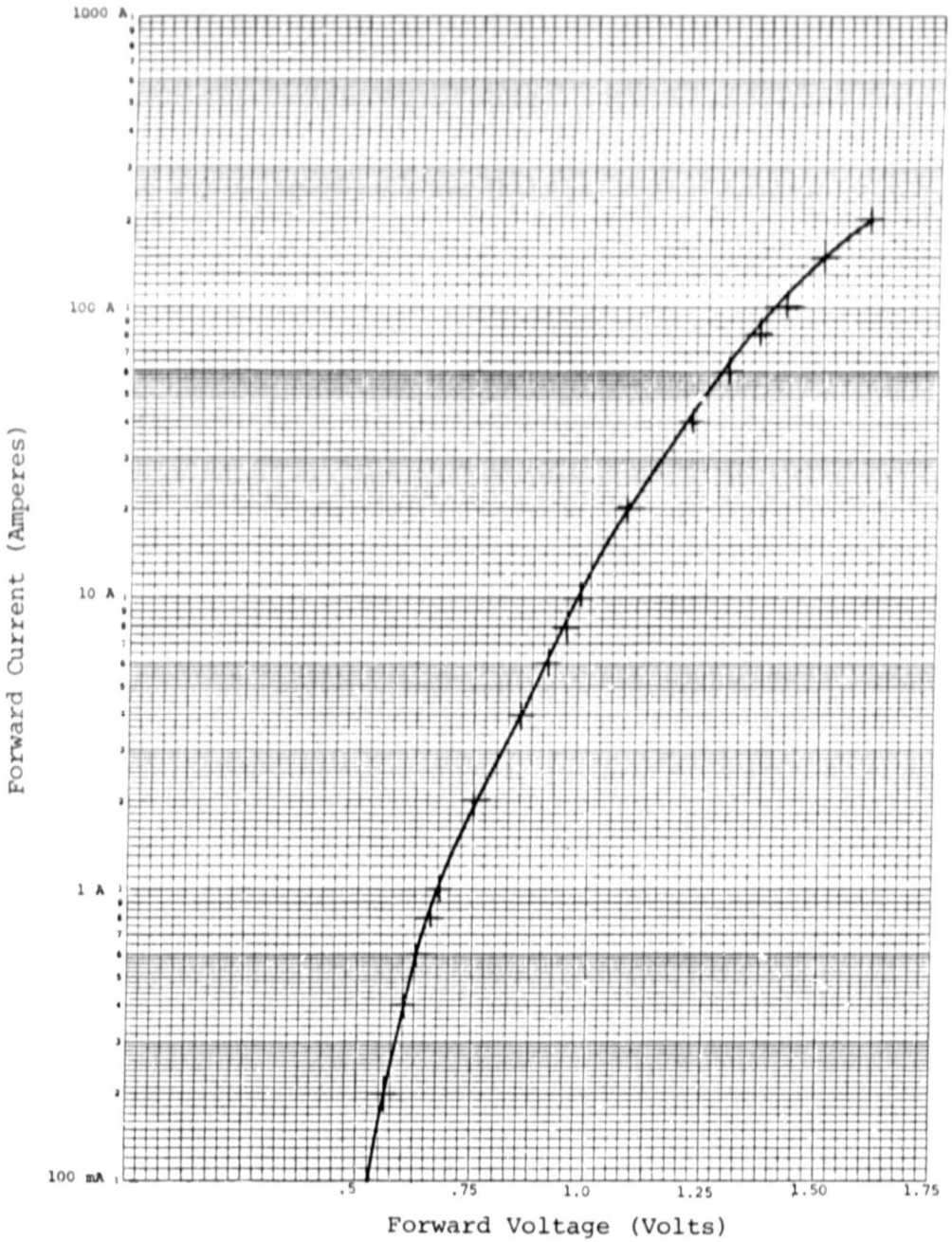


Figure 12 Device #28-13 Forward Characteristic Curve

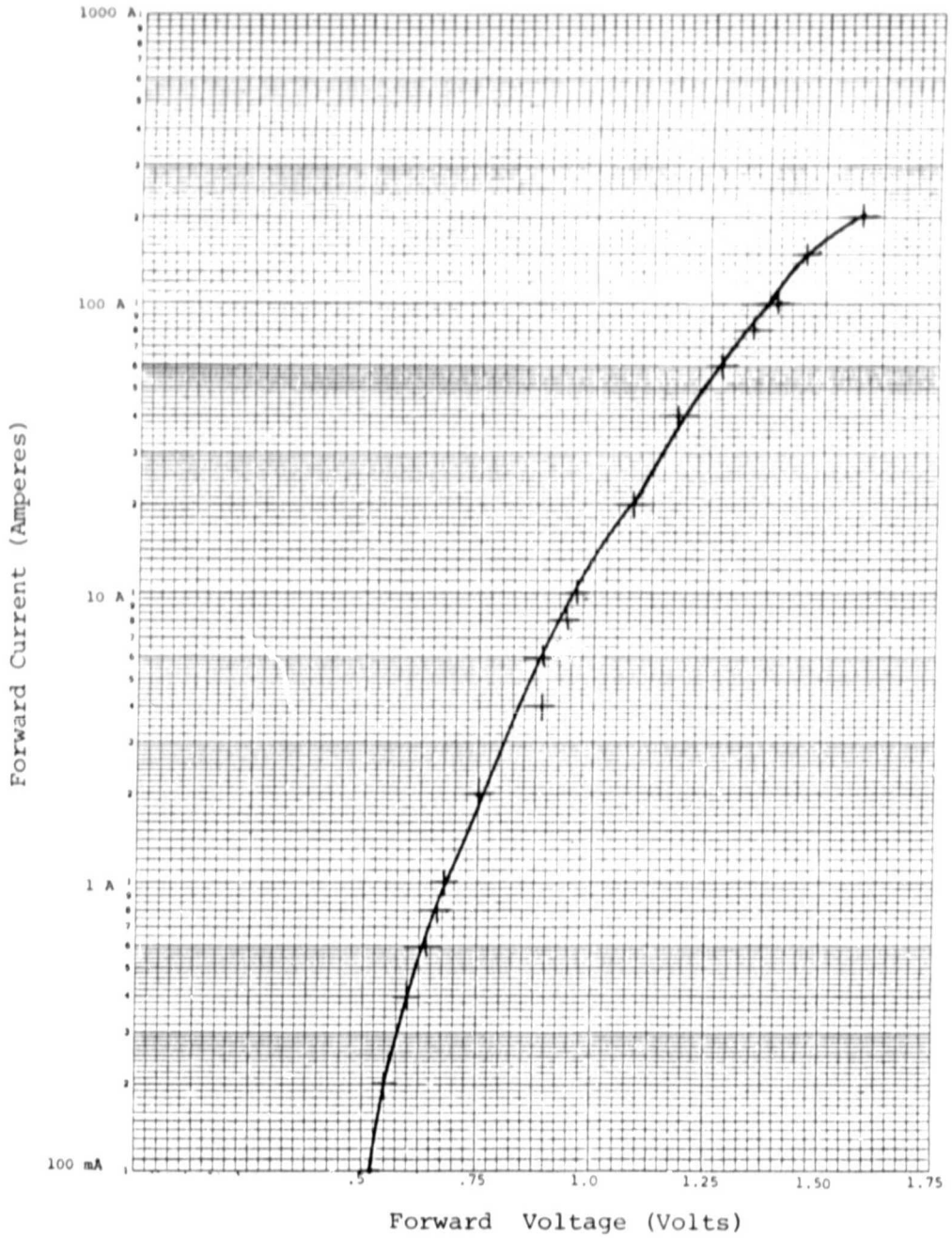


Figure 13 Device #28-18 Forward Characteristic Curve

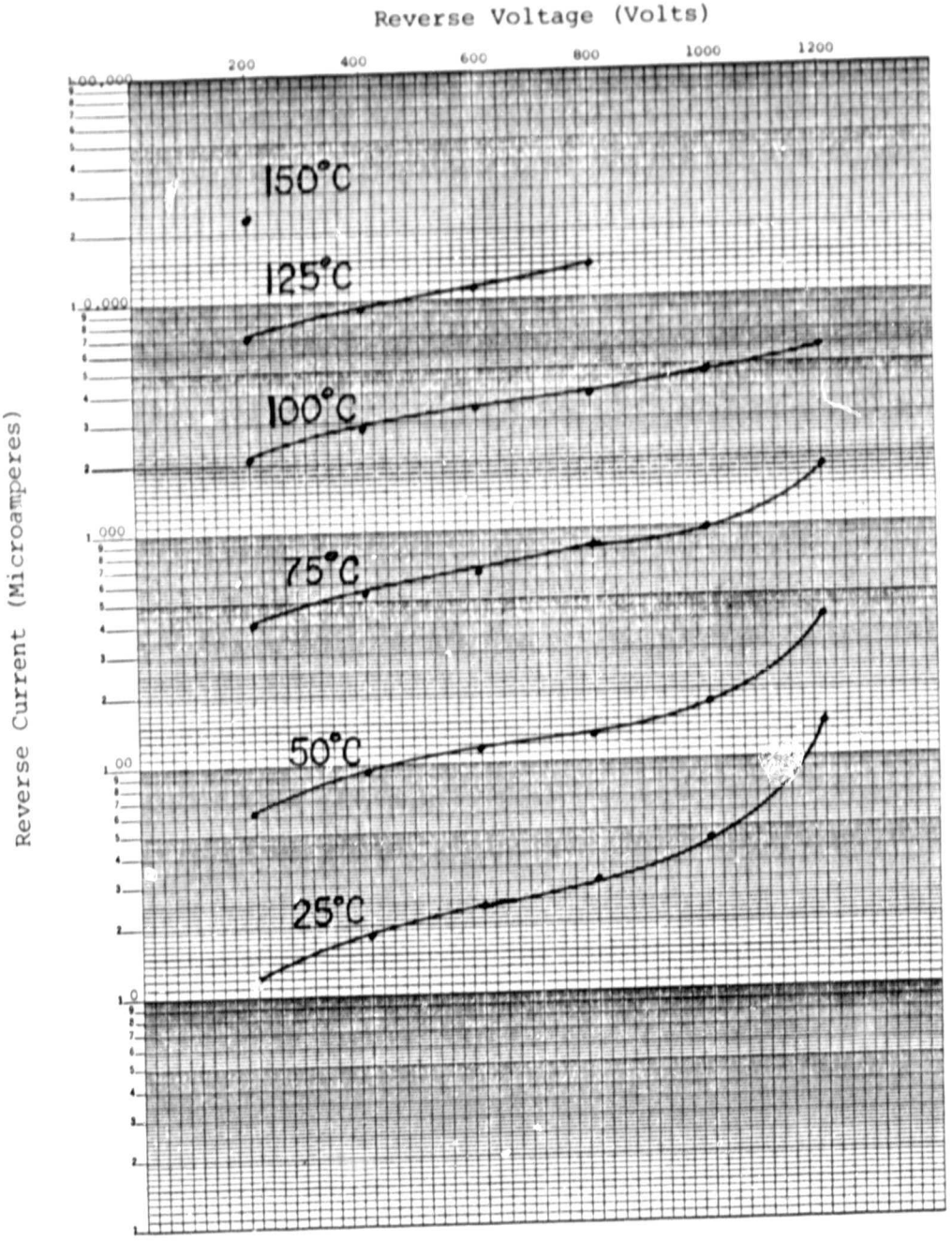


Figure 14 Device #28-7 Reverse Leakage

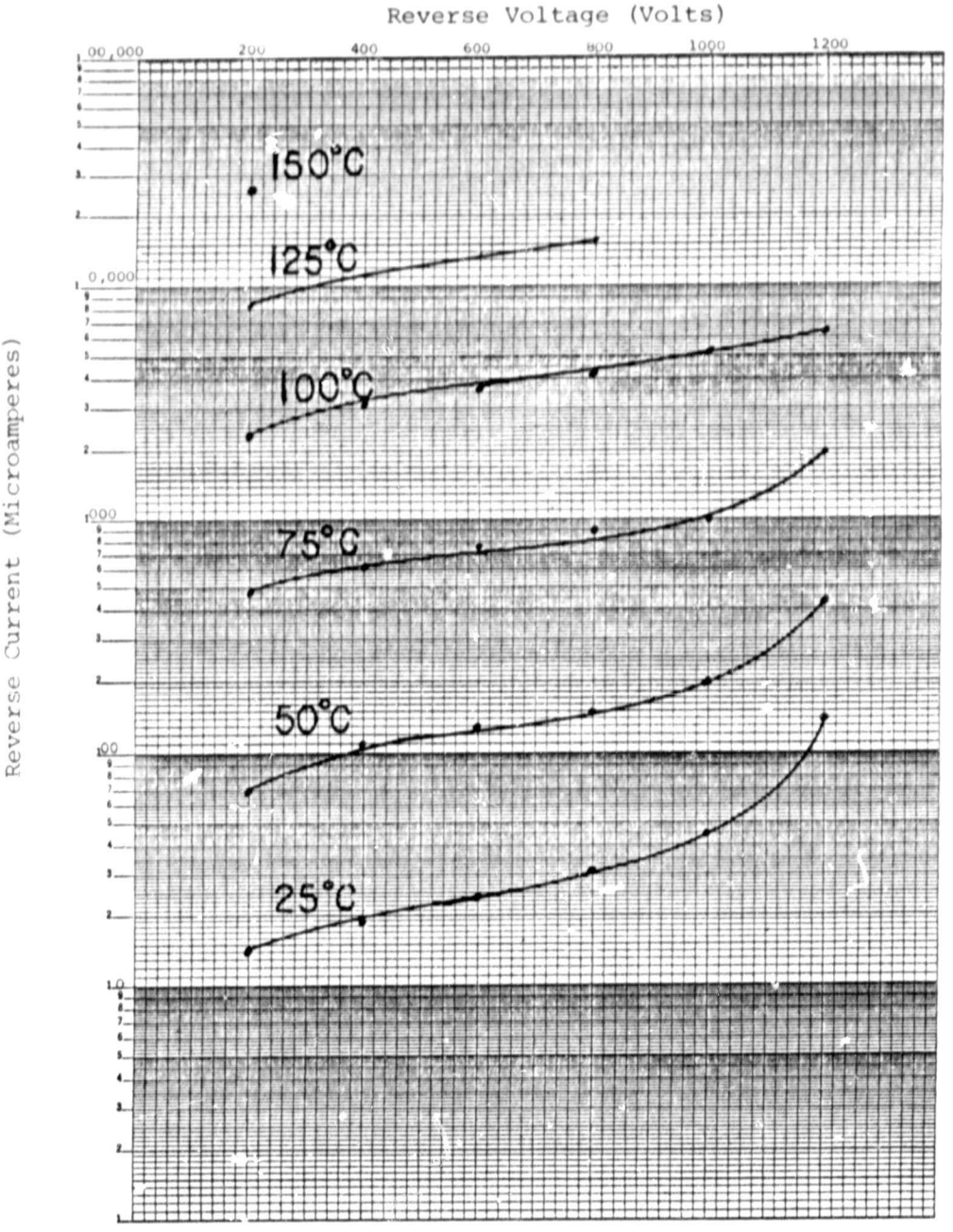


Figure 15 Device #28-8 Reverse Leakage

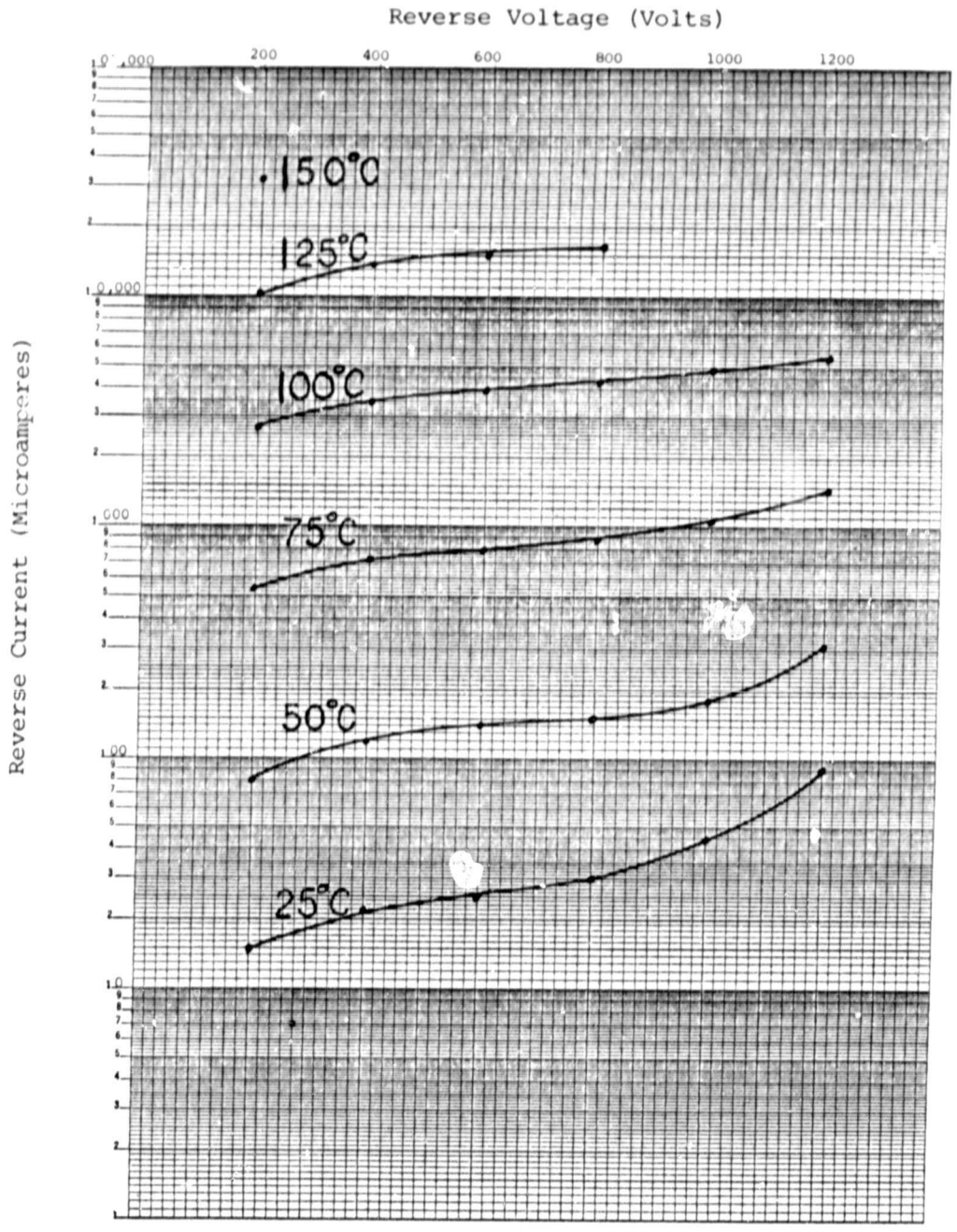


Figure 16 Device #28-10 Reverse Leakage

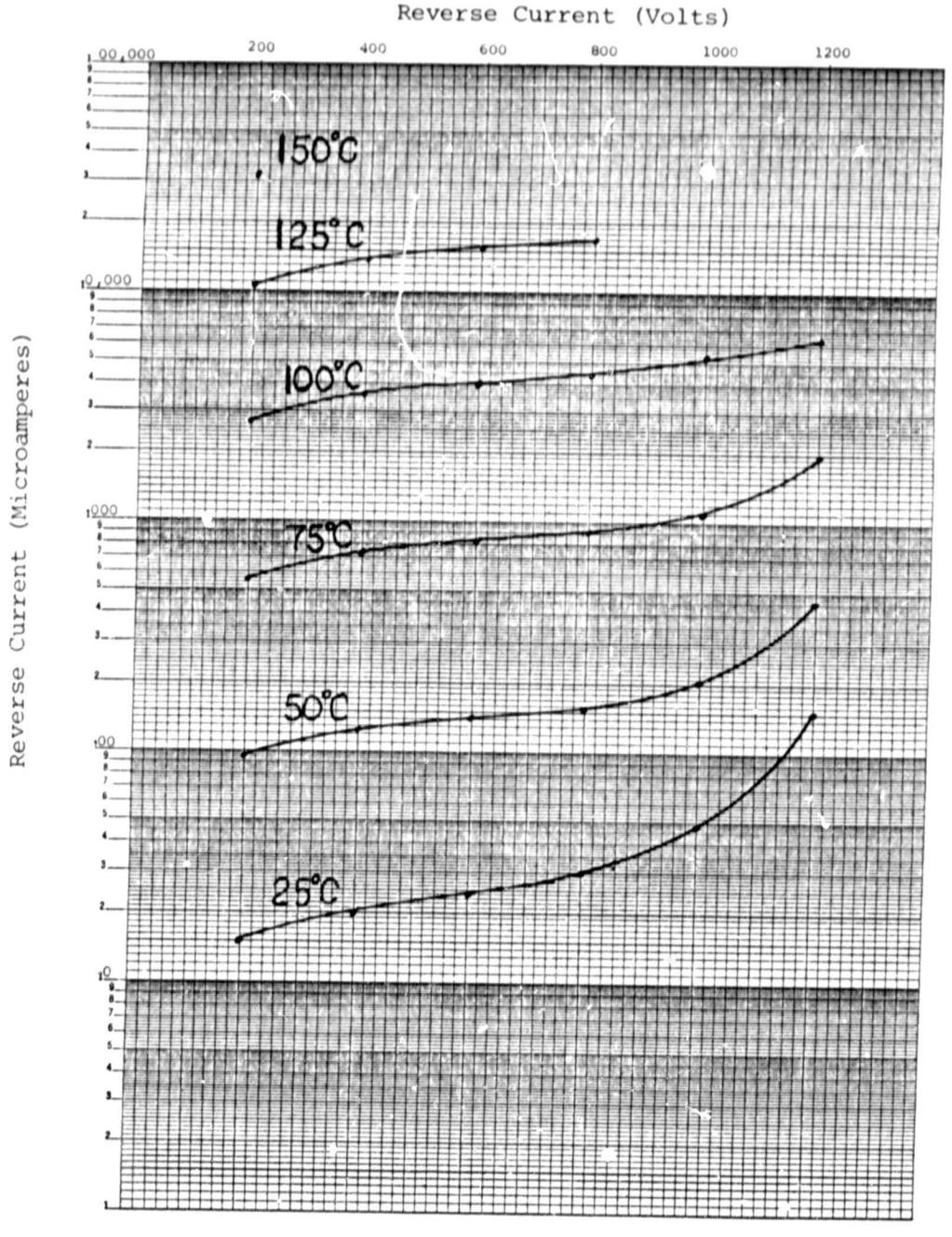


Figure 17 Device #28-13 Reverse Leakage

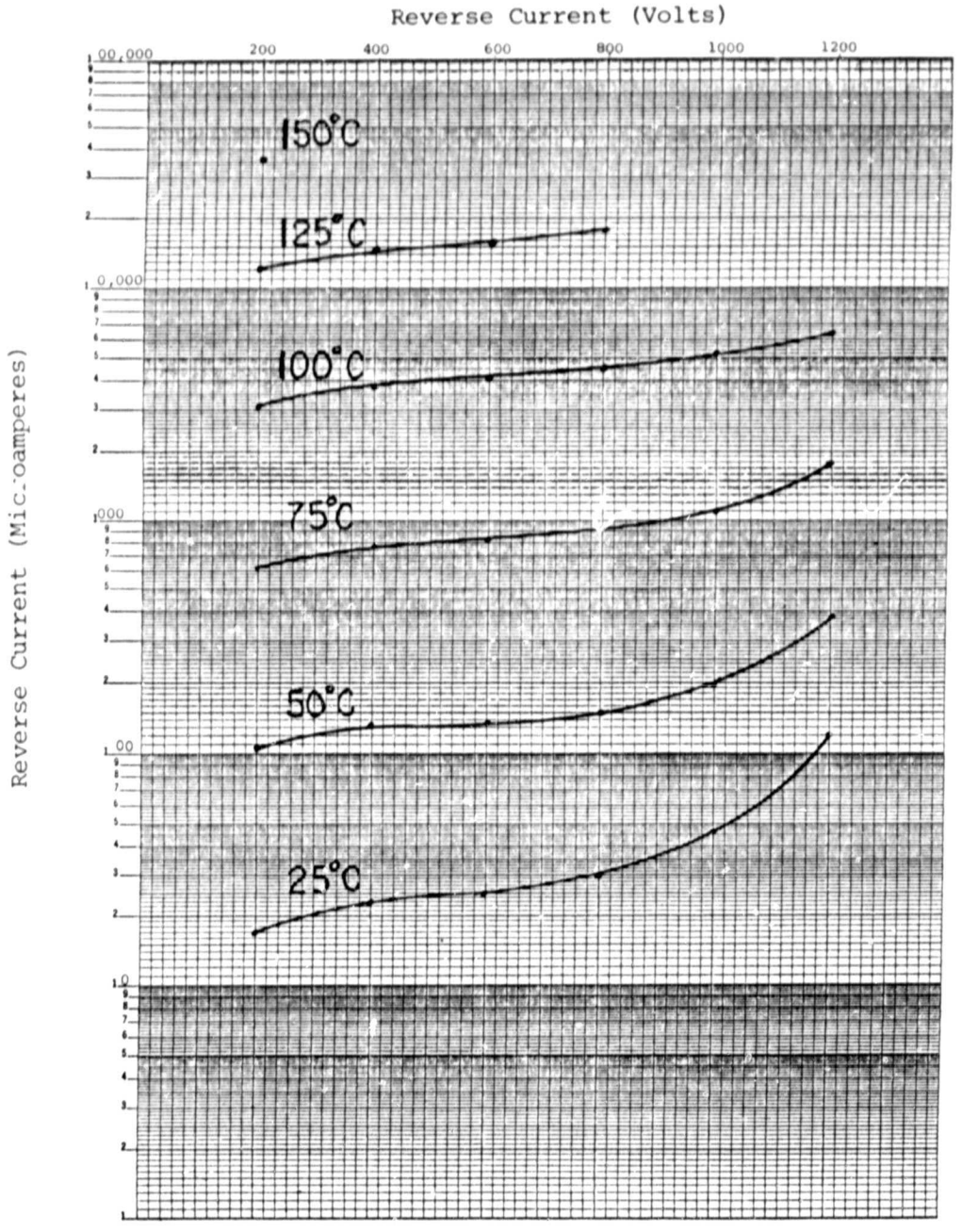


Figure 18 Device #28-18 Reverse Leakage

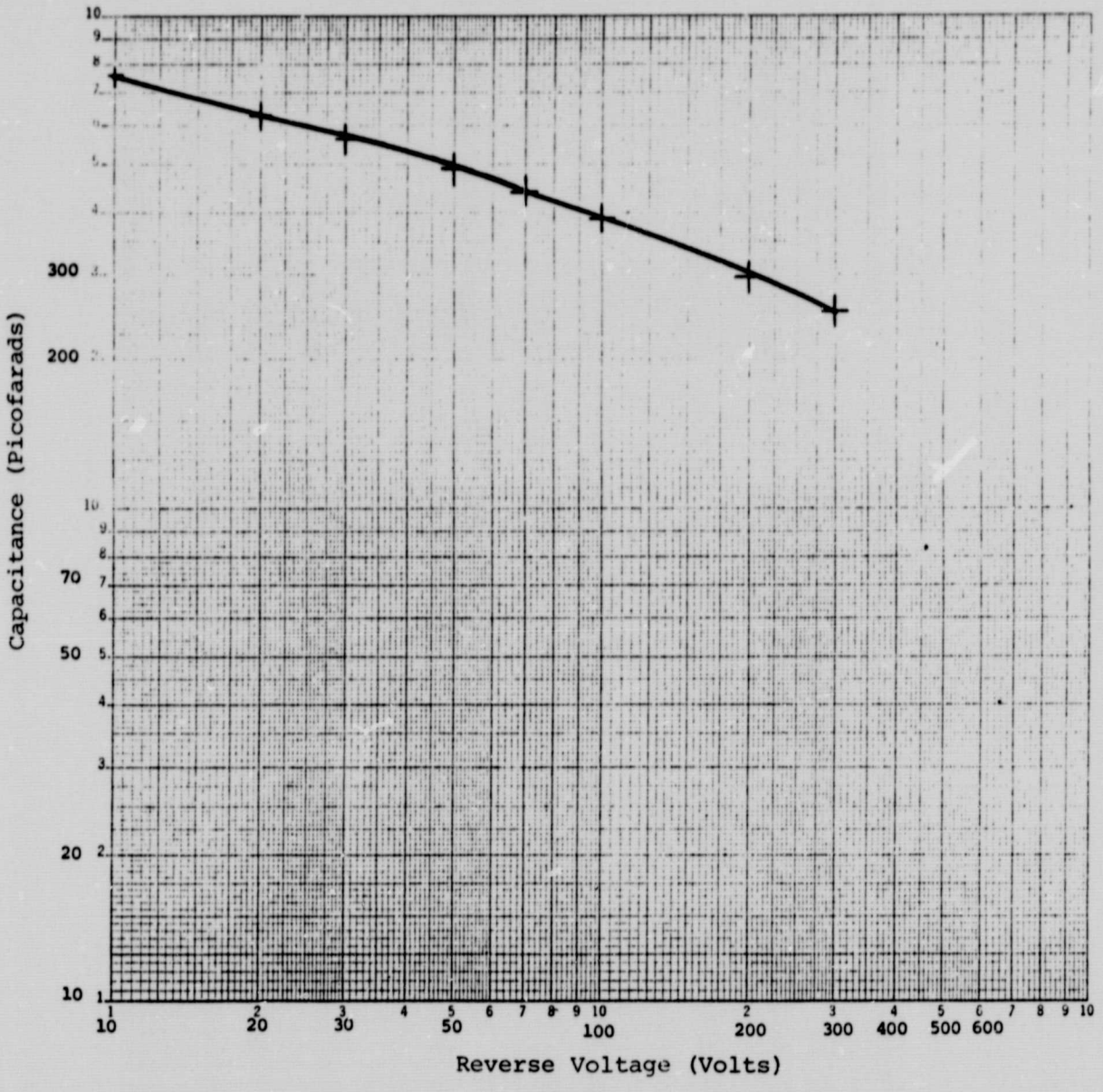


Figure 19 Device #28-7 Capacitance Versus Reverse Voltage

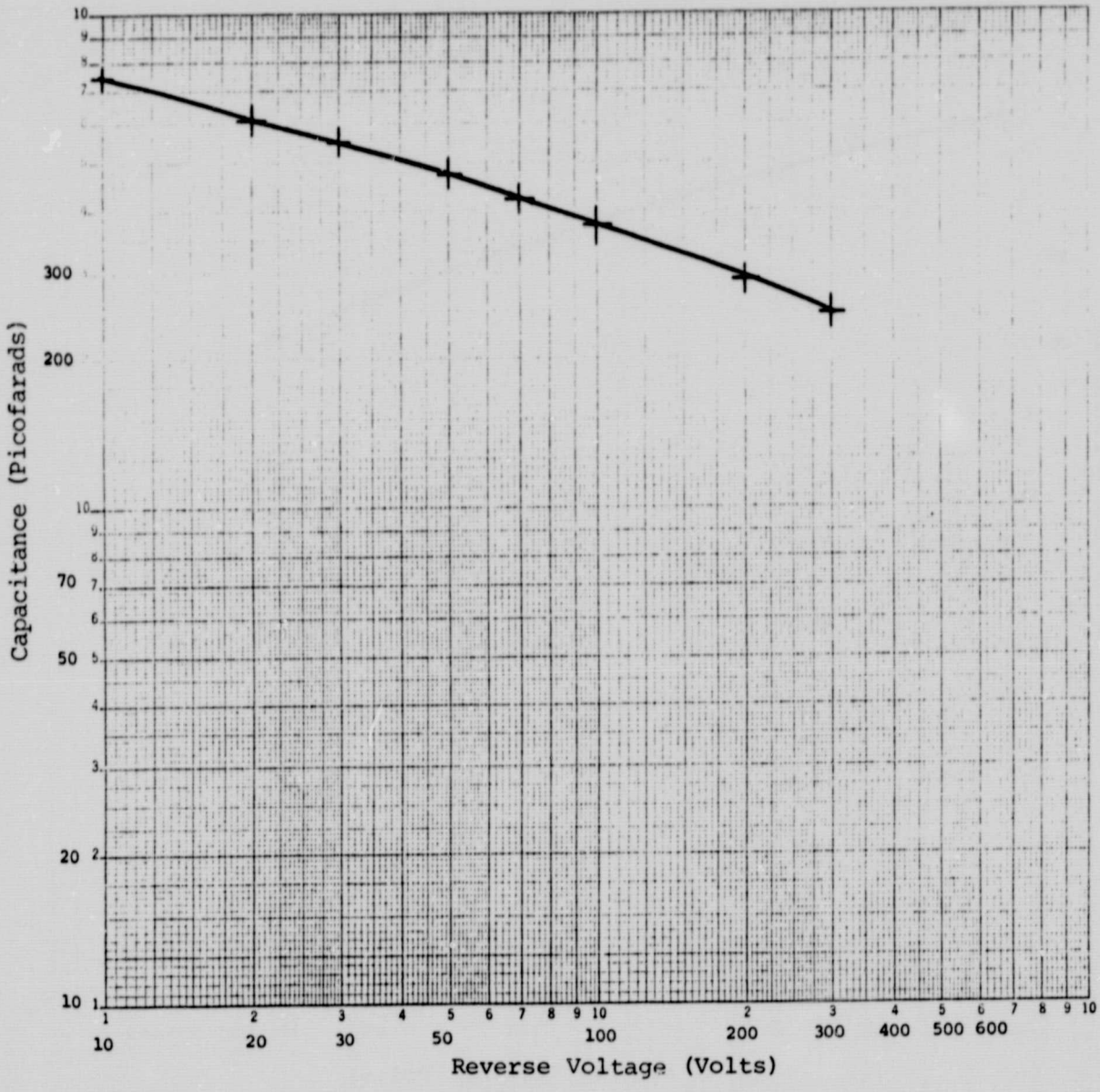


Figure 20 Device #28-8 Capacitance Versus Reverse Voltage

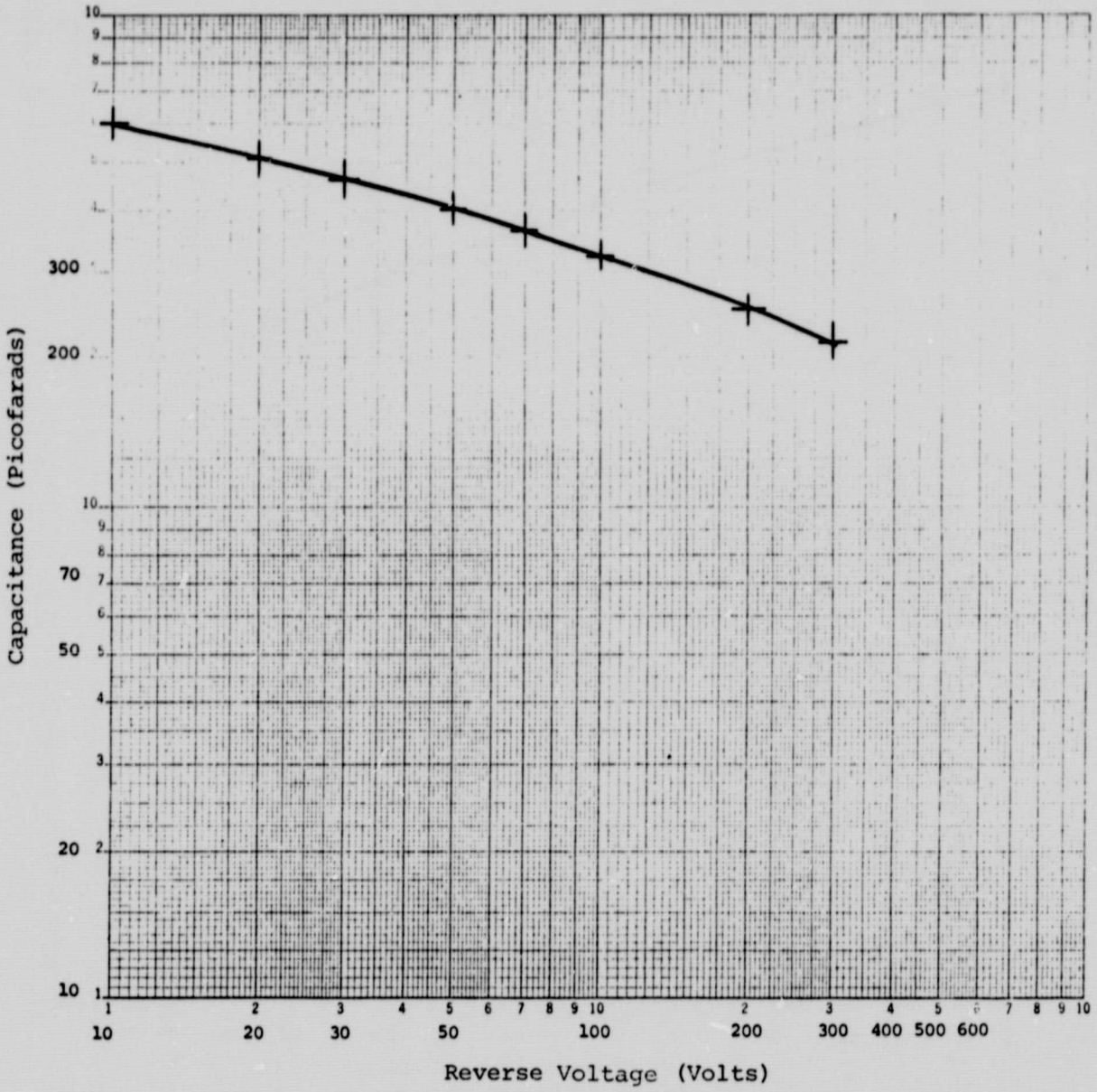


Figure 21 Device #28-10 Capacitance Versus Reverse Voltage

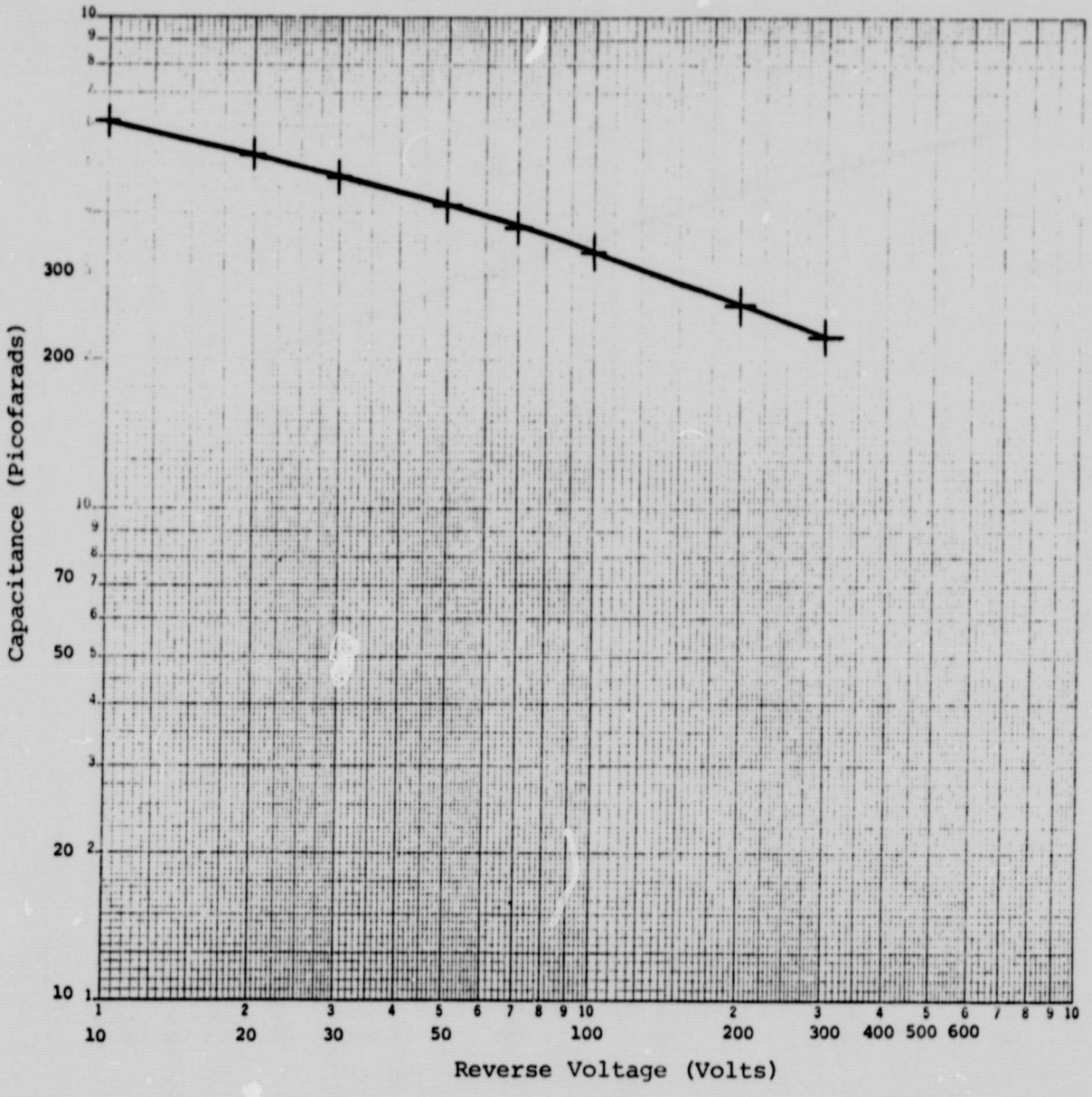


Figure 22 Device #28-13 Capacitance Versus Reverse Voltage

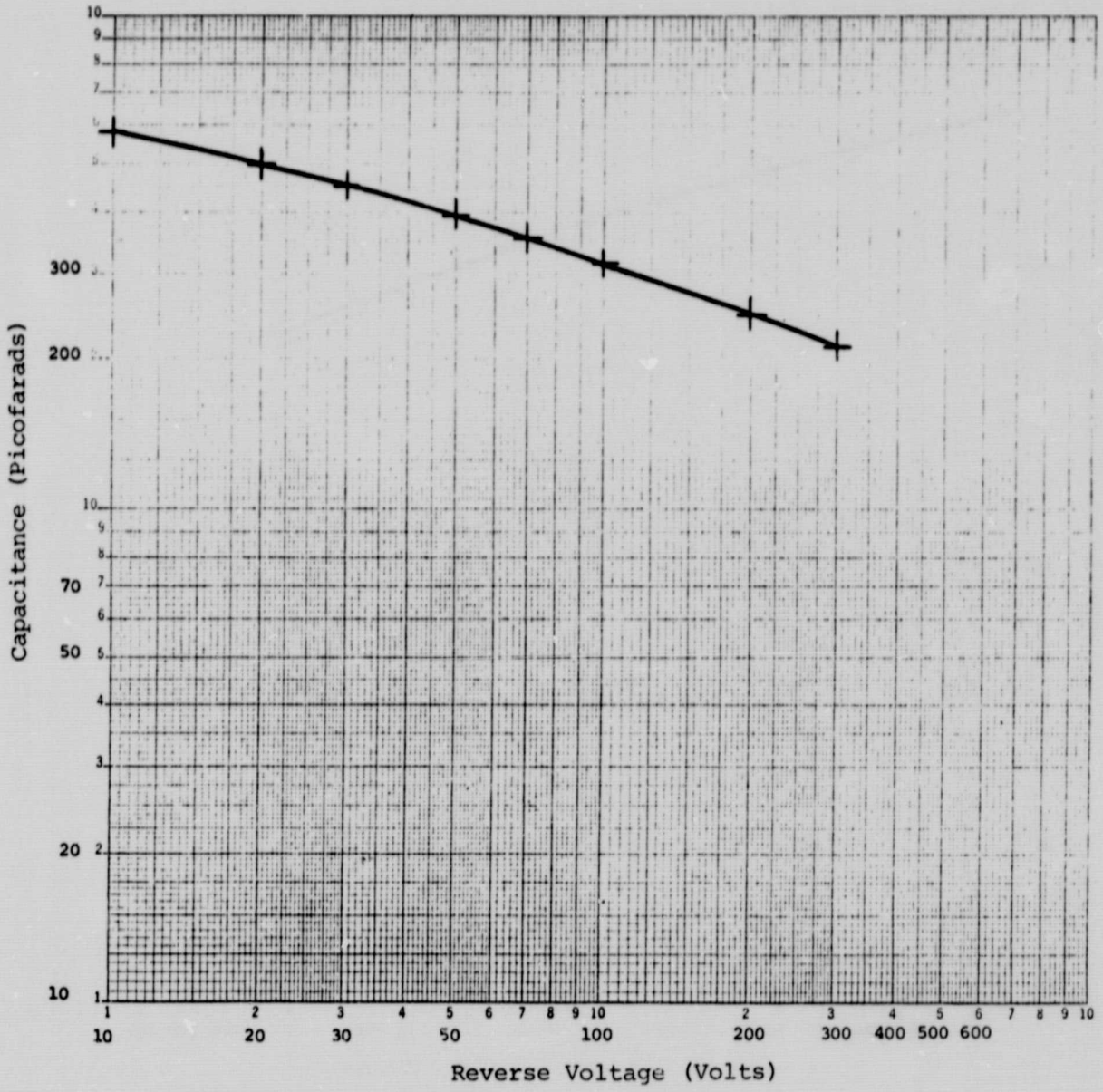


Figure 23 Device #28-18 Capacitance Versus Reverse Voltage

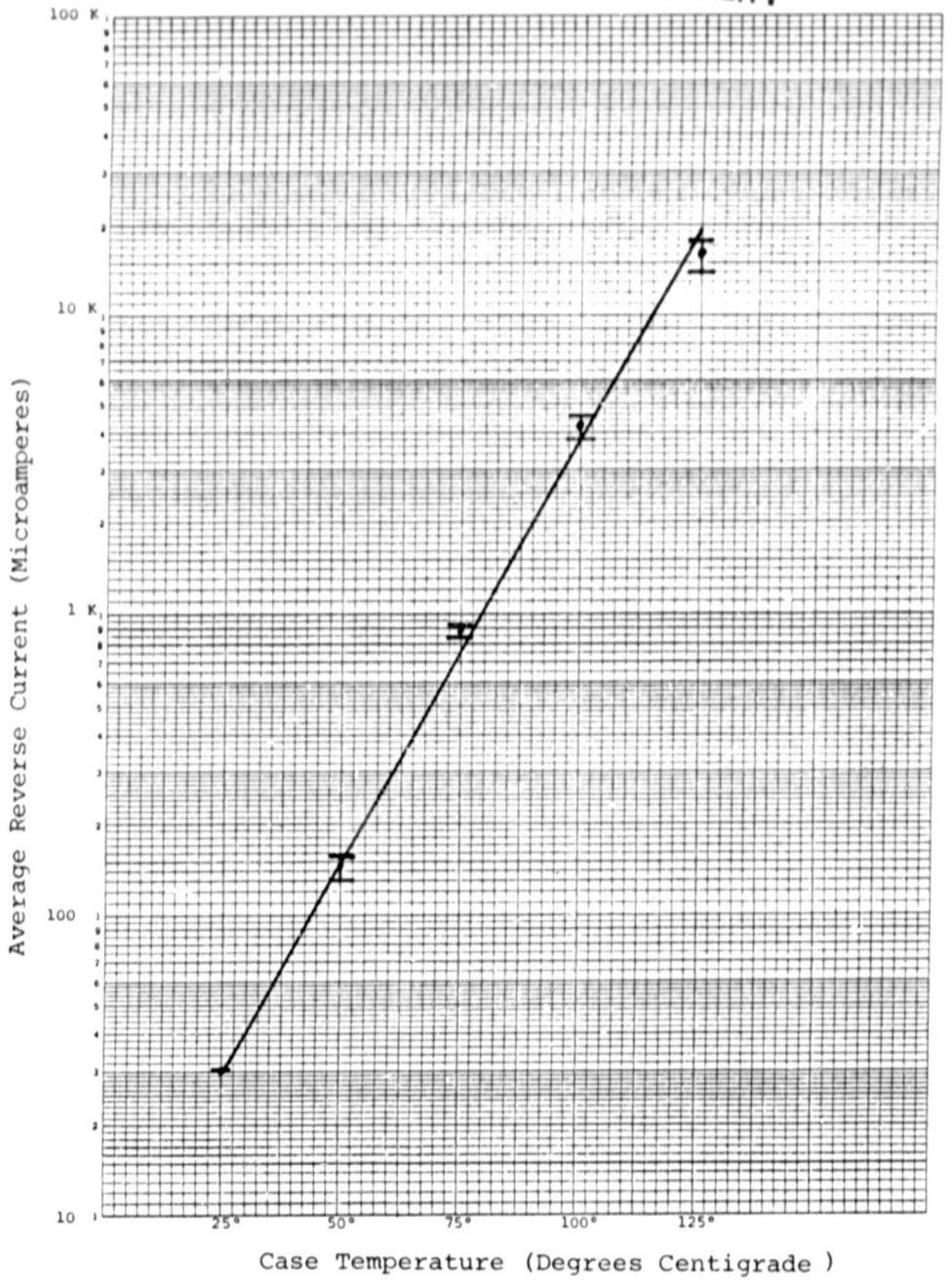


Figure 24 Reverse Leakage Versus Temperature

8.0 CONCLUSION

For Power Transistor Company, this contract was a continuation of the device design and process development work for high voltage, high current, fast recovery rectifiers, initiated with the development of the 1200 volt, 50 ampere diode under NASA Contract NAS3-22539. Although the approach to the basic design of the 150 ampere device was a scaled-up version of the 50 ampere device, several major device design process modifications, adjustments and improvements were implemented.

Assembly

The stranded and braided cable anode internal lead improves the current carrying capability as well as provides sufficient flexibility during the final capping and crimping operations.

Replacing solder preforms with solder-clad moly tabs reduced the number of piece parts to be handled and resulted in more reliable solder reflow contact.

Process

To achieve the required electrical characteristics, a gold diffusion process was developed and replaced the electron irradiation as the means for lifetime control in silicon. The following advantages have been gained

by this process:

- improved t_{rr} versus V_F trade-off
- more uniform switching characteristics
- more uniform reverse current characteristics
- no lifetime annealing effect during high temperature assembly
- in-house process control
- reduced cost

Although the reverse leakage current levels have increased as the result of gold diffusion, they are still well within the specified limits and are stable.

Areas of further device and process development have been identified at PTC and the experience gained during this contract work promises to yield significant improvements in the device performance.

The contract extension granted by NASA allowed PTC to pursue successfully the necessary process development for the completion of this contract.

9.0 ACKNOWLEDGEMENTS

Editor: Vilnis Balodis

Contributors: Albert H. Berman

Darrell C. Devance

Charles K. Gaugh

Eric A. Karlsson

Barbara G. Maddalena

Guin Troutman

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11.0 APPENDIX

SYMBOL	CHARACTERISTICS WITH TEST CONDITIONS	VALUE	UNITS
V_{RRM}	Peak Repetitive Reverse Voltage, T_J = 150°C	800 to 1000	Volts
V_R	DC Blocking Voltage, T_J = 150°C	800 to 1000	Volts
V_{RSM}	Peak Non-Repetitive Reverse Voltage, T_J = 150°C	$\geq$ 1.25 V_{RRM}	Volts
I_{RRM}	Max. Reverse Current at Rated V_{RRM}, I_F = 50A Forward Current T_J = 25°C T_J = 150°C	 0.10 7.5	 Milliamps Milliamps
I_F	Average Forward Current at T_C =100°C	150	Amps
I_{FSM}	Non-Repetitive Peak Surge Current (1/2 cycle surge current at 60Hz under load)	3000	Amps
V_{FM}	Forward Voltage at Rated I_F = 150A	1.5	Volts
T_J	Operating Junction Temperature Range	-65 to 200	°C
T_{STG}	Storage Temperature Range	-65 to 200	°C
$R_{\theta JC}$	Thermal Resistance Junction to Case	0.5	°C/W
t_{rr}	Reverse Recovery Time, T_C = 100°C I_F = 1.0A to V_R = 30 Vdc I_{FM} = 150A, dI/dt = 50A/μsec (JEDEC)	 50 200	 nsec nsec
$I_{RM(REC)}$	Peak Reverse Recovery Current I_{FM} = 150A, dI/dt = 50A/μsec (JEDEC)	10	amps

11.1 Specifications for fast recovery, high voltage power diode - Case temperature = 25°C unless otherwise specified