NASA CONTRACTOR REPORT

NASA CR-170908

LIGHTNING MAPPING SENSOR STUDY

By V. Norwood
Hughes Aircraft Company
Electro-Optical and Data Systems Group

Final Report

July 1983

Prepared for

NASA - Marshall Space Flight Center
Marshall Space Flight Center, Alabama 35812

TECHNICAL REPORT STANDARD TITLE PAGE

1. REPORT NO.	2. GOVERNMENT ACCESSION NO.	3. RECIPIENT'S CATALOG NO.
NASA CR-170908		

4. TITLE AND SUBTITLE	5. REPORT DATE
LIGHTNING MAPPING SENSOR STUDY	July 1983
	6. PERFORMING ORGANIZATION CODE
7. AUTHOR(S) V. Norwood	8. PERFORMING ORGANIZATION REPORT #
9. PERFORMING ORGANIZATION NAME AND ADDRESS Hughes Aircraft Company Electro-Optical and Data Systems Group	10. WORK UNIT NO.
	11. CONTRACT OR GRANT NO. NAS8-34942
12. SPONSORING AGENCY NAME AND ADDRESS National Aeronautics and Space Administration Washington, D.C. 20546	13. TYPE OF REPORT & PERIOD COVERED Contractor Report
	14. SPONSORING AGENCY CODE

15. SUPPLEMENTARY NOTES Final Report
Technical Monitor: Hugh Christian, Atmospheric Sciences Division, Systems Dynamics Lab., Marshall Space Flight Center

16. ABSTRACT

This study provides a technology assessment to determine how a world-wide, continuous measurement of lightning could be achieved from a geostationary platform. Various approaches to the detector sensors are presented.

It was first determined that any existing detector chips would require some degree of modification in order to meet the lightning mapper sensor requirements. The elements of the system were then analyzed, categorized, and graded for study emphasis.

The recommended approach for the lightning mapper sensor is to develop a monolithic array in which each detector cell has circuitry that implements a two-step photon-collecting method for a very high dynamic range with good measurement accuracy. The efficiency of the array is compatible with the use of a conventional refractive optics design having an aperture in the neighborhood of 7 to 10 cm.

17. KEY WORDS	18. DISTRIBUTION STATEMENT
Lightning Mapper Optical Sensors Satellite Sensor	Unclassified-Unlimited G. F. McDonough Director, Systems Dynamics Laboratory

19. SECURITY CLASSIF. (of this report)	20. SECURITY CLASSIF. (of this page)	21. NO. OF PAGES	22. PRICE
Unclassified	Unclassified	78	NTIS

MSFC - Form 3292 (May 1969)

For sale by National Technical Information Service, Springfield, Virginia 22161

ACKNOWLEDGMENT

The work reported herein was supported by the National Aeronautics and Space Administration, Marshall Space Flight Center, Systems Dynamics Laboratory, Atmospheric Sciences Division, under NASA Contract NAS8-34941 and under the sponsorship of Dr. James C. Dodge, Mesoscale Atmospheric Processes Program Manager, NASA Headquarters, Washington, D.C.

Special thanks are given also to Dr. H. J. Christian (scientific monitor of this study) and other NASA and university lightning research team members who provided technical advice and input to the final documentation.

CONTENTS

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (cont.)

LIST OF ILLUSTRATIONS (cont.)

LIST OF TABLES

INTRODUCTION AND SUMMARY

The lightning mapping sensor study was conducted along the lines described in Section 1.8 after the requirements for optics, focal plane array, and processing were allocated according to the systems analysis described in Sections 1.1 through 1.7.

It was first determined that any existing detector chips would require some degree of modification in order to meet the lightning mapper sensor requirements. The elements of the system were then analyzed, categorized, and graded for study emphasis as shown in the following table.

Study Emphasis by Elements

ELEMENT OR FUNCTION	FEATURES	STATUS OR DIFFICULTY
PRIMARY OPTICS	16^{o}, f/1.5, 5 to 15 cm VISIBLE, 10 Å	CONVENTIONAL
AFT OPTICS	NONE OR BEAMSPLITTER OR OPTICAL REDUCER	CONVENTIONAL
FPA	0.5×10^{6} DETECTORS, SAMPLE RATE 1000/SEC MINIMAL GAPS 2×10^{5} DYNAMIC RANGE	NOT AVAILABLE; DEVELOPABLE FROM STATE-OF-ART TECHNOLOGIES MAJOR STUDY TASK
BACKGROUND REMOVAL	BACKGROUND 100 TIMES MINIMUM SIGNAL	WHERE AND HOW MAJOR STUDY TASK
EVENT DETECTION MEASUREMENT I.D. (TIME POSITION) FORMAT FOR TRANSMISSION	SIGNIFICANT DATA 15×10^{-4} TIMES DATA SAMPLED INITIALLY	CONVENTIONAL COMPONENTS LESSER STUDY TASK

The recommended approach for the lightning mapper sensor is to develop a monolithic array in which each detector cell has circuitry that implements a two-step photon-collecting method for a very high dynamic range with good measurement accuracy. The efficiency of the array is compatible with the use of a conventional refractive optics design having an aperture in the neighborhood of 7 to 10 cm.

Lightning events are separated from the wide range of cloud-reflected sunlight by means of analog filtering circuits that are located off the focal plane in the signal processor.

The stages following the background-removal filters isolate events data from the very much greater amount of inconsequential data so that the signal processor can be reduced in power and size.

1. SENSOR SYSTEM REQUIREMENTS AND ANALYSIS

1.1 SENSOR SYSTEM REQUIREMENTS

Column 1 in Table 1-1 lists the requirements or recommended ranges on parameters provided by MSFC as guidelines for this study. The next column shows the values that are derived from the first column.

1.2 SIZING THE SENSOR

The key to the selection of the instantaneous field of view, sampling time, aperture size, and detector noise requirements lies in the signal-to-noise and background equations; see Figure 1-1. First, the sensor must be sized to ensure that the signal exceeds the photon uncertainty by a ratio corresponding to the required signal to noise, or;

$$\text{Signal} \geq \left(\frac{S}{N}\right)_{RQ'D} [\text{Signal} + \text{Background}]^{1/2}$$

Substituting and solving for the term G, which includes all of the sensor sizing elements except T, yield

$$G = \left(\frac{S}{N}\right)^2_{RQ'D} \frac{J + TN'}{J^2}$$

Re-inserting this expression into the equations for S and B leads to a determination of how the photon uncertainty will compare with the levels of noise electrons that can be achieved for the types of detectors under consideration.

$$[S + B]^{1/2} = K^{1/2} [J + TN']^{1/2} = \left(\frac{S}{N}\right)_{RQ'D} \frac{J + TN'}{J}$$

Table 1-1. Requirements and derivative parameters

Study Basis	Auxiliary or Derived Values	Consequence/Report Reference
Full disk coverage from three geostationary satellites	FOV 16°	(Section 1.3)
Intensity and position of lightning events day and night	Incident solar irradiance reflected from clouds used to calculate maximum background 99 $\mu w\ cm^{-2}\mu^{-1}$ on Lambertian scatterer of reflectance 0.8	Isolating events from background received major attention in study. Aspects are summarized in Section 1.7 and discussed in detail in Sections 2 and 3.
Spectral band is 10 Å at 8683 Å	Available filters will allow 0.5 transmission	Other spectral lines could be used if NASA so specifies. Since the responsivity peaks in region of 8000 Å either the NI or OI lines can be accommodated.
Minimum signal is -1σ of peak radiant energy/flash population from NASA U-2 measurements	4.7×10^{-6} joules m^{-2}sterad^{-1} in band	These conditions combined with the required S/N lead to a maximum signal-to-minimum noise ratio of 10^4, which is discussed in Section 1.
Maximum signal is 10^4 times minimum signal	4.7×10^{-2} joule m^{-2}sterad^{-1} in band	
Resolution is 10 to 20 km	From 977 to 489 detectors across array	Emphasis here was shifted from user needs to optimization for sensor effectiveness, such as background removal. The analysis is described in Section 1.5.
Sampling interval is about 1 msec	Determines number of signal lines needed to read out the FPA and also the processing rates (especially A/D encoder difficulty)	Section 1.4
Measurement accuracy must be better than 50% for lowest-signal, highest-background case	Background levels must be estimated with accuracy of better than 0.5%, and optics must be made sufficiently large to collect enough signal photons to dominate photon noise	Since calculations show that the need to control false-alarm rates for signal processing reasons imposes a more severe S/N requirement than the accuracy requirement does, accuracy does not dictate aperture sizing.

Charge carriers generated by lightning events,

$$\text{Signal} = \underbrace{JA\alpha^2\tau_o\tau_f\tau_a\mathscr{R}\frac{1}{q}}_{G}$$

Sensor characteristics and constants G

and by background,

$$\text{Background} = \underbrace{N'A\alpha^2\tau_o\tau_f\tau_a\mathscr{R}\frac{1}{q}}_{G}$$

where

J = energy in pulse in band, joules m^{-2} $sterad^{-1}$

N' = radiance from cloud - watts $m^{-2}sterad^{-1}$

A = aperture area, m^2

α^2 = instantaneous field of view, sterad

τ_o = primary optics throughput = 0.7

τ_f = filter transmission = 0.5

τ_a = aft optics transmission = 1 or 0.5

$\mathscr{R}$ = responsivity = 0.2 ampere/watt

q = charge on electron = 1.6×10^{-19}

T = sample time

Figure 1-1. Equations and symbols for signal/(background)$^{1/2}$ calculations.

These values of charge carriers caused by photon uncertainty are plotted in Figure 1-2 with solid lines for three values of T. For each position along the abscissa it is assumed that the combination of sensor parameters that make up G has been selected to ensure the signal/photon noise ratio indicated. For any signal-to-noise margin that will ensure a reasonable false alarm rate (see Section 3.3), the photon noise exceeds the expected detector noise value which are in the region of 100 equivalent electrons and are shown by a dotted line.

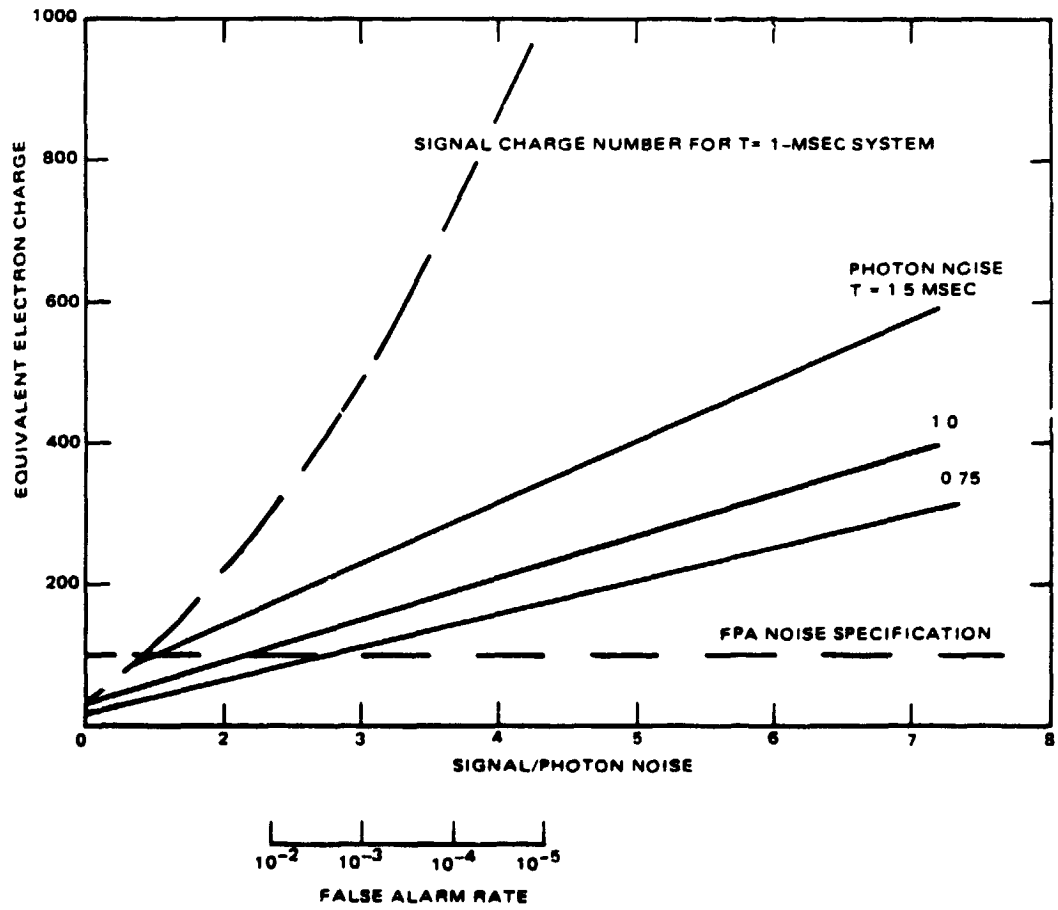


Figure 1-2. Signal and noise carrier numbers for systems sized for indicated S/N levels.

For each margin, we then calculate the number of carriers caused by signal alone without background. These numbers have been plotted on the same graph with a dashed line for the nominal sampling interval of 1 msec. The expression for signal only is

$$S = \left(\frac{S}{N}\right)^2_{RQ'D} \left(1 + \frac{TN'}{J}\right)$$

Not shown here is the number of the maximum background carriers which can be reconstructed by squaring the photon noise values. The signal is generally not dependent on T; however, in this case D has been adjusted to admit enough signal to ensure the indicated margin over background which entails a T dependency.

SENSOR PARAMETERS

Each signal level derived to provide a given margin implies a family of sensor parameters. Substituting (see Table 1-1) values of minimum required signal imbedded in the worst-case reflecting cloud described above leads to the following relationship:

$$A\alpha^2\tau_o\tau_a\tau_f\mathscr{R}\frac{1}{q} = \left(\frac{S}{N}\right)_{RQ'D} \frac{4.72 + 252T \text{ (in msec)}}{(4.72)^2} 10^6$$

Using expected values for throughput (0.7) a responsivity of 0.2, and a spectral filter transmission of 0.5, we calculated two sets of curves for diameter versus IFOV under two circumstances, i.e., (1) when the detector dimensions match the focal plane dimensions with no additional aft optics elements; (2) when an additional loss of 0.5 is incurred in making the match because an adaptor or beamsplitter is required; see Figure 1-3. The several approaches to detector array design require different aperture sizes and different elements in the aft optics train. Points corresponding to the three most promising types of arrays and sensor configurations are spotted on the appropriate

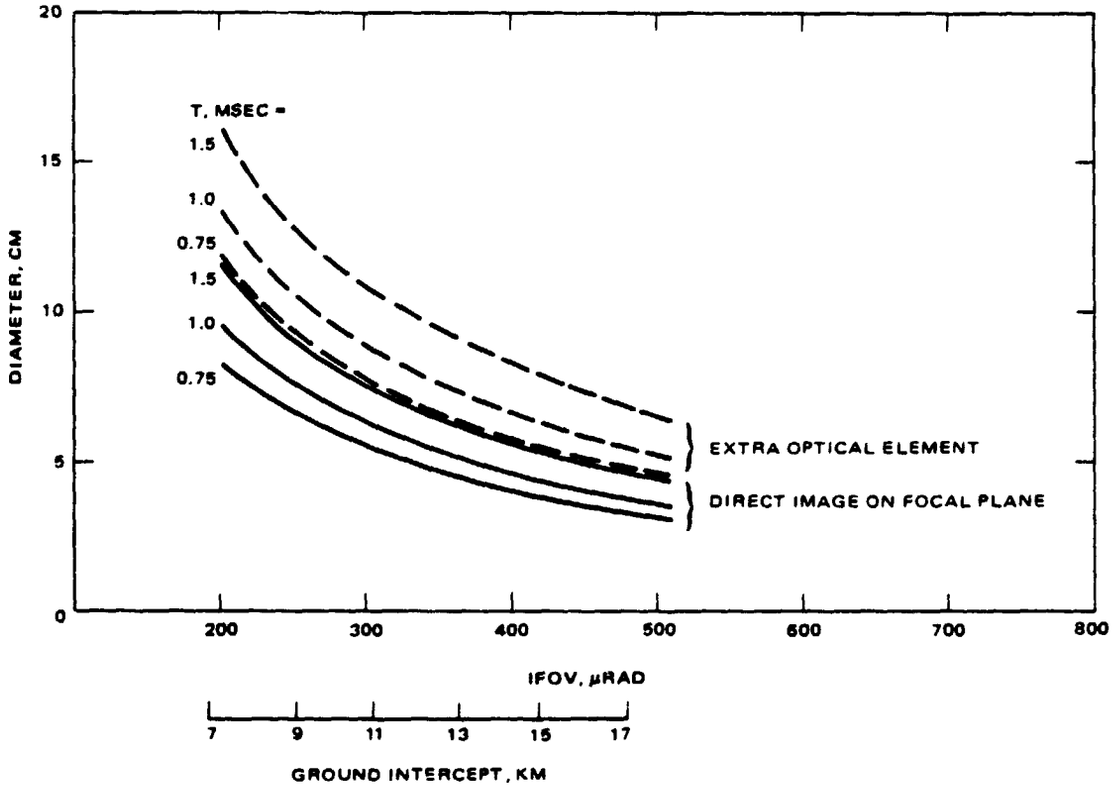


Figure 1-3. Diameter required for three sample times and two optics systems; versus IFOV event fills IFOV.

curves: A - A monolithic array design with a dual-gain collector for very large dynamic response and off-chip background removal; B - A modified CCD array with background removed off-chip; C - A monolithic array designed for background removal at each detector cell. The reasons for the mismatch and the proposed solutions are given in Sections 1.4 and 1.6, respectively.

The more recent experiments from the Shuttle lightning sensor indicate that weak events may not fill the larger resolution elements. Figure 1-4 shows the demands on aperture size if the minimum event level has the same cloud-top radiance but extends over only 100 km^2. In this case, the aperture must be increased as the detector intercept angle is increased. The smallest aperture is achieved when the IFOV just corresponds to the extent of the minimum event.

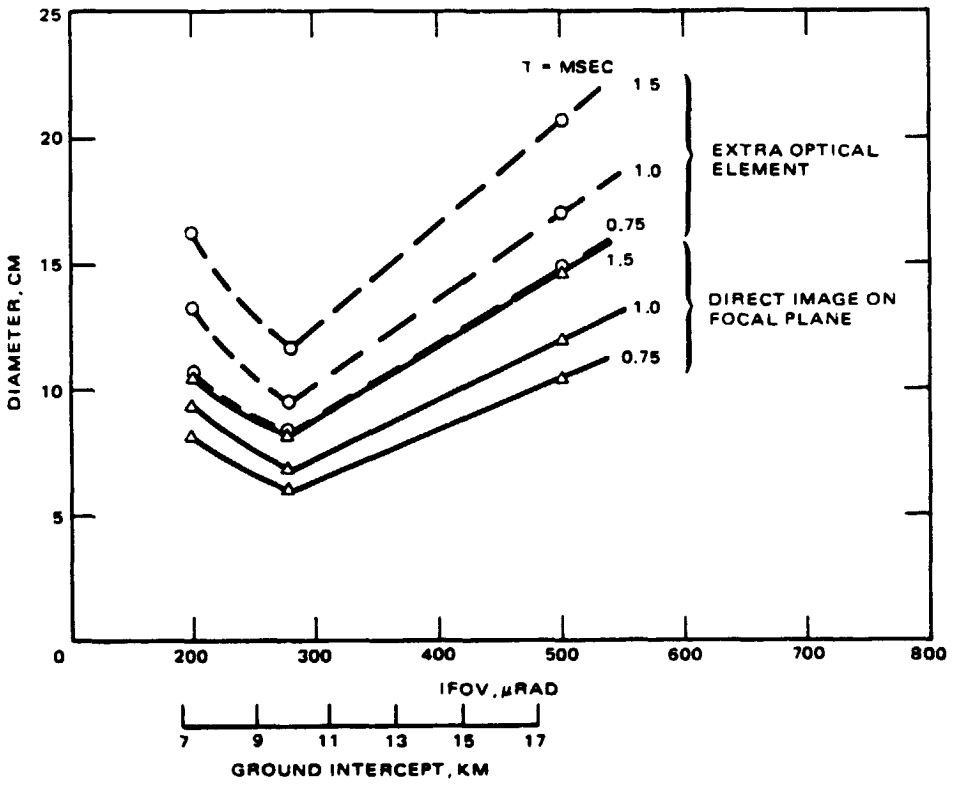


Figure 1-4. Diameter versus IFOV – event fill only 100 km^2 (280 $\mu rad)^2$.

1.3 VIEWING GEOMETRY

In order to view the entire equator from three geostationary satellites, it is necessary to calculate angles of the viewing triangle shown in Figure 1-5. The half-angle at the satellite for viewing one-sixth of the equator is

$$\theta_c = \sin^{-1}\left[\sin\theta_o \frac{a_e}{\left[(a_e + h)^2 + a_e^2 - 2(a_e + h)\, a_e \cos\theta_o\right]^{\frac{1}{2}}}\right] = 8.07^o$$

The discrepancy between the projected intercept of an IFOV at the nadir and at the rim caused by range alone will be ten percent. The intercepted patch

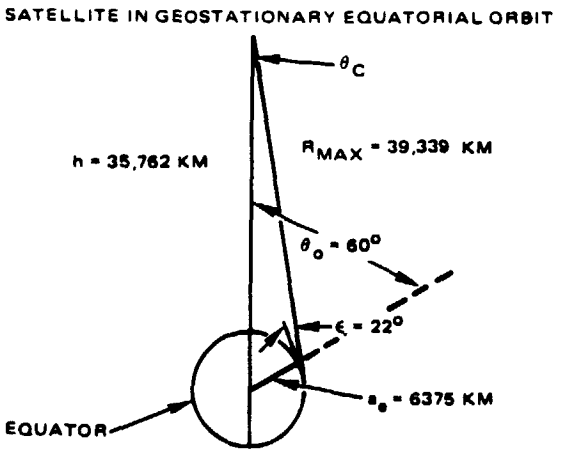


Figure 1-5. Half-angle for FOV needed to view entire equator with three satellites.

along the ground or along a cloud top in the radial direction will be 2.94 times larger because of the intercept angle. Using the nominal value of intercept, which is 15 km at nadir, the 419-μrad-square instantaneous field of view (IFOV) will intercept a patch at maximum range that is 16.5 km wide and 44 km long.

The assumption of Lambertian scattering implies essentially equal background return from clouds (for the same incident solar angle) regardless of the position in the field of view since the scattering is a function of sin ϵ, and the area is increased by sin ϵ^{-1}.

1.4 FACTORS AFFECTING SELECTION OF SAMPLING INTERVAL

The primary difficulty in using sampling intervals that are shorter than 1 msec is that the number of leads required to address the array grows since transit times are more or less limited for state-of-the-art devices operating at ambient temperature. Although for the designs under study, more leads could be handled than the number shown, the examples given are based on good design density practice. The desire to arrange all feed lines around the perimeter has led to the arrangements shown and restricts the total number of lines used.

Reducing the time between samples to less than 1 msec would ease the problem of saturation by large signals since more pulses would be split among the samples. For example, at 1-msec sampling, 45 percent of the pulses must be split, whereas with 0.5-msec sampling, 90 percent must be split.

The dual-gain integrator array described below can handle pulses of almost any size expected whereas the CCD design may be limited. Should this design be pursued, the question of sampling time should be reopened.

Under full sunlight conditions, increasing the time between samples would decrease the signal-to-noise ratio for pulses at the minimum level. There would be a slight advantage in the nighttime scenes since weak pulses would be less likely to be divided or made weaker. The advantages in terms of signal processing equipment are proportional to the sampling rate, but no dramatic improvement can be realized.

In general, it would be good sampling practice to increase the sampling rate to the highest level that can be economically supported until some factor forms a demarcation. In this case, the number of leads that can be accommodated provides such a demarcation, and the interval is about the 1 msec shown.

1.5 GENERAL PRECEPTS FOR SELECTING CHIP SIZE AND NUMBER OF DETECTORS/CHIP

The goal for the detector array design is to limit the maintenance and signal readout lines to the outer edges. In this way, gaps in the imaged region can be made inconsequential. Ideally, the array would have no more than two chips spanning at least one of the dimensions, and it should be possible to restrict the lines to one or two edges. In this way, all lines could be restricted to the outer perimeter of the array. It should be observed that several of the types of arrays that were studied satisfy this condition.

Because of feedline considerations, one would elect to have as few chips as possible; hence, large chips are desirable. In general, the maximum chip size is limited to a dimension that can be handled at all stages of processing and to one that can be cut from a boule with a high yield. A maximum dimension of 0.8 inch was selected to be compatible with present state of chip design.

The size of an individual cell varies according to the complexity of circuitry that must be included in the cell area. For the mapping application, it is not necessary to provide completely contiguous photosensitive areas. If only a portion of the area intercepted by the IFOV is photosensitive, for example 25 percent, the aperture diameter can be increased to recover the signal level required; in this case, the diameter must be doubled. It is essential that the energy incident on the reduced area be a good representation of the entire cell space, which requires a judicious blurring of the focused region. It can be seen from the following optics discussion that some aperture requirements may be incompatible with some detector sizes, an incompatibility that may necessitate the use of additional optical elements with an attendent reduction in throughput. The decreased throughput will in turn entail even larger apertures.

Since the arrays studied had cell dimensions ranging from 25 to 100 μm, chips could have as many as 400 cells across or as few as 180 cells after readout circuit space has been provided. Table 1-2 lists the number of detectors and chips that could be used for three representative sizes.

Table 1-2. Effect of cell size and IFOV(α) on FPA

Center-to-Center Cell Size, μm	For α = 280 μrad, 972 cells across	For α = 419 μrad, 648 cells across
25	Array of 2 x 2 chips requires leads at perimeter only	Array of 2 x 2 chips requires leads at perimeter only
50	Array of 3 x 3 chips requires leads into interior	Array of 2 x 3 chips requires leads at perimeter only
100	Array of 5 x 5 or more chips requires leads into interior	Array of 4 x 4 chips requires leads into interior

The three examples shown that involve leads into the interior of the array require some type of optical splitter if large gaps are to be avoided. One such arrangement is shown in the following discussion of optics.

Hybrid arrays are an option that would permit small, contiguous photosensitive areas to be used in combination with very complex specialized readout circuitry. This type of array was abandoned because monolithic designs can include circuitry having sufficient sophistication for the mapper application, and they offer long-range economies and greater reliability compared with those characteristics of hybrid designs.

1.6 OPTICS CONSIDERATIONS

The requirements for the primary optics, i.e., a 16^{o} field of view, a 3- to 15-cm aperture in a very narrow spectral band, can be easily met with conventional refractive optics provided that the f/No. is not too small. Some combinations of very small detectors with the larger optics lead to a mismatch between the focal plane dimensions and the detectors. For example, a 25 μm (0.001 inch) cell intercepting 419 μrad in an f/1.3 system would allow an aperture of only 4.6 cm. Figure 1-3 shows that such a combination could be used if the supposition that the radiance fills a 15-km cell prove to be correct. If only 100 km^2 is illuminated, it would be necessary to increase the aperture to 10 cm; this increase could be accomplished by (1) using a 54.4-μm (0.0022-inch) detector; (2) developing special optics having f/0.6, (3) using an optical fiber bundle adaptor. The first option is compatible with a new design under the guidelines described above, the second is not practical and the third is feasible and inexpensive. Since a fiber bundle causes an additional transmission loss in the neighborhood of 0.5, the optics must be enlarged another 40 percent to compensate for this loss. The larger optics increases the dimension discrepancy by requiring a longer fiber bundle, but the procedure does converge since most of the loss occurs at the boundaries rather than in the length.

Some array designs described above involved cell sizes so large that the 600 to 900 elements required could not be spanned by two chips. Having more than two chips involves interior feed lines and large dead strips across the field of view. Figure 1-6 shows one approach to eliminating the blank strips. A beamsplitter of this type is regarded as state of the art although the added complexity and vulnerability of alignment to vehicle launch loads mitigate against its use. The splitter can be in the form of a partially mirrored plate or be imbedded in a cube. Either can be used with a wide angle refractive system of the Petzval type. The cube splitter would conserve space and give a more nearly balanced signal at the two focal planes.

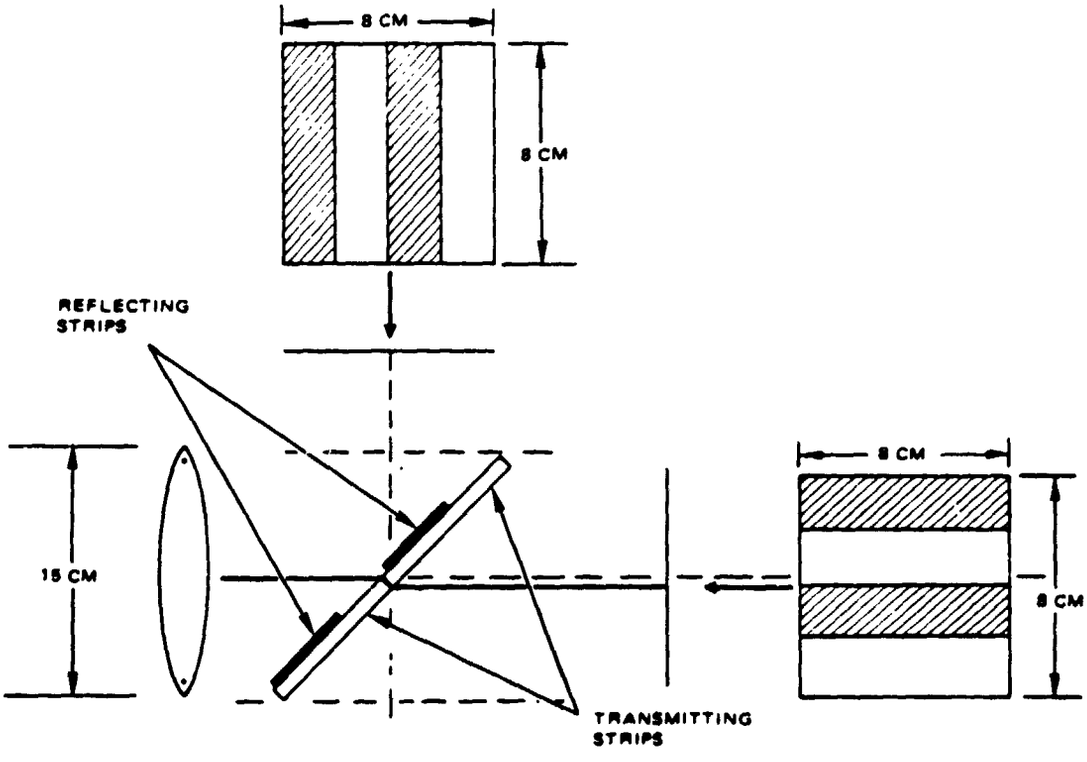


Figure 1-6. Beamsplitter for large-cell detectors (0.004 inch).

Figure 1-7 shows the optics elements to be added for the range of detector cell sizes that were considered.

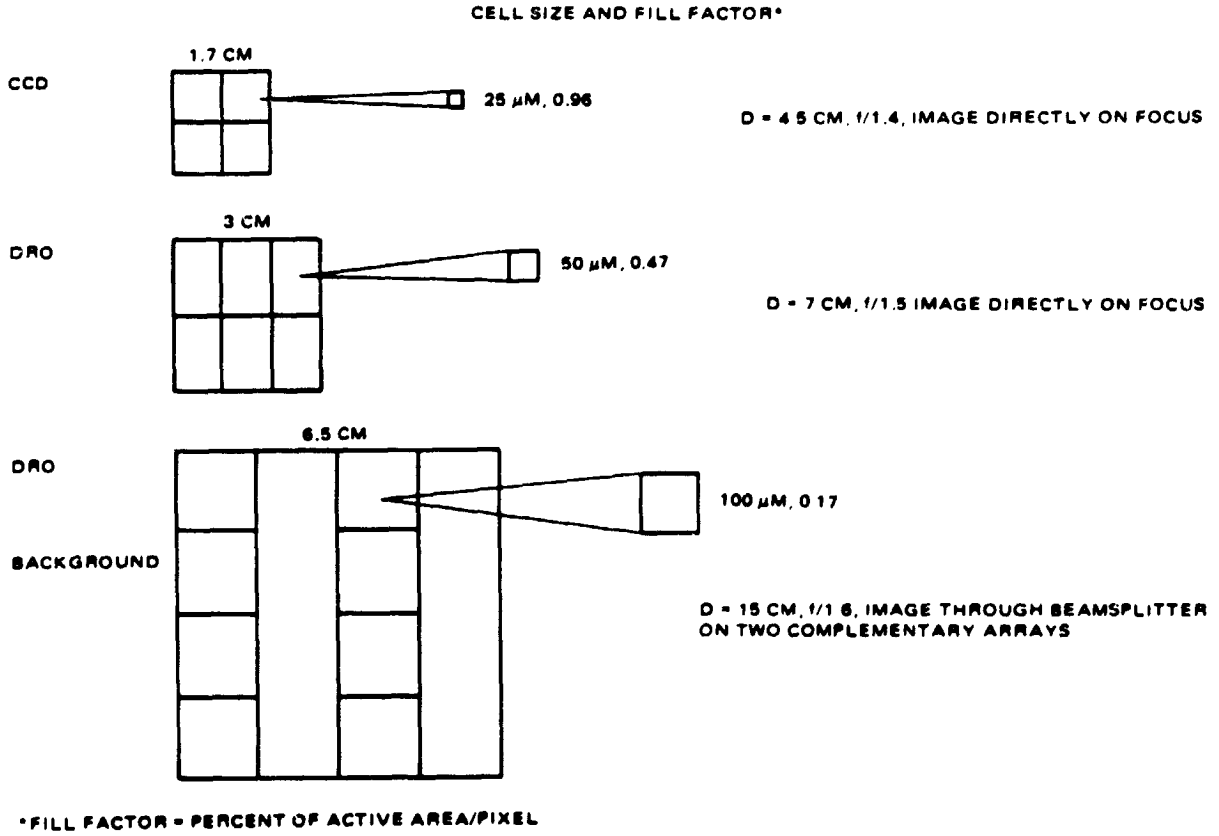


Figure 1-7. FPA effect on optics.

Optical Filter

A price quotation has been obtained for a dielectric spectral filter based on conventional design; the price and delivery time reflect this conventionality. The following are characteristics that accompanied the quotation.

Width	10 Å ± 2 Å
Center point	+2 Å, -0
Minimum transmittance	0.4 ± 0.1

Out-of-band rejection	10^4
Diameter	2 inches

No further effort was devoted to the filter since these tolerances indicate that this will not be a critical item. Experience with specialized metal oxide filters has shown that a higher transmittance could be obtained at a higher price. This option would be pursued if other parameters, such as fill factor, made the transmittance critical.

Optical Fiber Bundle Adapter

The optical fiber bundle adaptor has made it possible to consider sizable mismatches caused by reasonable f-numbers (≥1.5) and convenient detector cell dimensions. Such a bundle consists of 16 to 25 more fibers than detector cells. Transition factors can be made as large as 4 to 1 for the linear dimension; the following characteristics were quoted for a factor of 1.45

Number of fibers/detectors:	5 x 5
Transmittance:	0.6
Blemished fibers:	$25/10^6$
Numerical aperture:	1 (60^o)
Path length variation:	0.02-inch systematic (outside fibers are longer)

For the lightning mapper application, the larger end would be at the focal plane. An emersed bundle, filter, and FPA assembly would provide the best combined transmittance.

The preferred FPA designs, both CCD and DRO, appear to be compatible with the calculated apertures. If greater sensitivity were desired or if the performance of a component should fall short of that predicted, the fiber bundle could be used to permit a significant aperture increase. The prices quoted for this precision device are modest.

1.7 BACKGROUND-REMOVAL APPROACHES

The daytime background consisting of sunlight reflected from clouds has been reduced by spectral filtering, minimum practical detector intercept, and sampling time to the extent that the lowest lightning signal required has an amplitude of about 0.01 of the background. It is not feasible to use simple pulse-to-pulse differencing to subtract background because the pulse widths of the events vary from 0.5 to 3 msec which means that pulses can be split among samples and also there is the possibility that two pulses may occur in consecutive samples. Subtracting subsequent pulses would eliminate these two categories systematically. Hence, a more sophisticated temporal comparison must be made which is implied below by the phrase temporal analysis.

The following is a list of the methods considered during the study; a brief paragraph describes the status of each.

1. Spatial Comparison of Adjacent Pixels. This method requires that adjacent detectors receive cloud-reflected energy that match within 0.25 percent and have responsivities matched to a similar or better level. This method can tolerate no cloud variation or edges, and the responsivity calibration is clearly impractical.

2. Spectral Band Comparison. The lightning event occupies such specialized spectral lines that the cloud return in an adjacent band was considered as a method for estimation and removal. Since separate detectors must be involved, the same calibration matching to within 0.25 percent described above would be required and would entail the same difficulties. Other factors that make this method unattractive are the greater array complexity (yield penalty) and the optics which grow in size and in the number of elements.

3. Digital Processing of Successive Samples (Temporal). This technique was studied (see Section 3.2) but was abandoned when it was found that the analog-to-digital rates were excessive.

4. Analog Processing of Successive Samples (Temporal). Techniques of this kind were studied (see Figure 3-5); one, involving a recursive filter, has been selected as the preferred approach.

5. A-c Coupled Detector Cell. Several such cells were devised, and one was carried to the point of being exercised in a computer simulation. Good discrimination proved to require such a complex circuit that the fill factor was reduced to six percent.

1.8 OVERVIEW OF STUDY

Figure 1-8 shows the study effort in skeleton form. The crux has always been perceived as the decision to remove the cloud background with a "smart" array or to use an array in as close to existing form as possible and assign

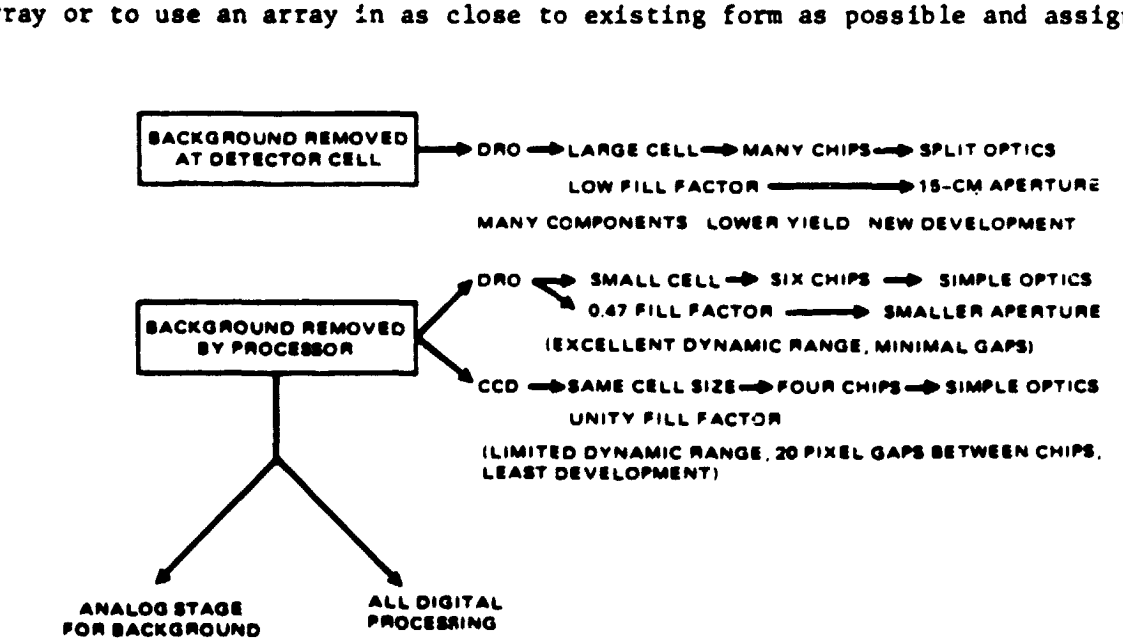


Figure 1-8. Study outline and preferred approach.

the background-removal task to the processor. Early in the study, two facts became apparent, i.e., (1) that digital processing was very power-consuming and that many analog-to-digital devices would be required if all of the data required encoding; (2) that no off-the-shelf array or chip could be sampled quickly enough to form a building block.

Since a major adaptation or a new design seemed necessary, effort was focused on cells capable of background removal. The sequential nature of the lightning pulses described in Section 1.7 led to the need for increasingly complex circuitry to achieve a good estimate of the background. At the same time, a suitable analog circuit was devised for background removal in the signal readout lines off-chip. In retrospect, it is realized that background removal in each cell requires a replication of the circuitry that is proposed here for off-chip removal, but instead of one circuit for each readout line (about 200), one circuit per cell or about 420,000 would be needed. In addition, since the size of the cell grew, the number of chips increased and thereby complicated the optics with beamsplitting. Also the ratio of active area to focal plane area diminished to the extent that larger optics were required. The complexity of chip and optics has more than counterbalanced the additional signal processor circuitry.

Having elected to remove the background in the processor, we now turn to the array options. One approach is to modify an excellent CCD silicon array described earlier with 32 parallel readout lines so that 1-msec sampling is possible. Because the existing array has a limited charge capacity, an alternative design was sought that could meet the extended dynamic range requirements. A modification of an available design was devised that offers a splendid dynamic range and uses a combination of techniques, each of which has been demonstrated. This proposed design also permits an array to be assembled without more than two pixel gaps between chips. A schedule has been established that will allow feasibility to be demonstrated before a major program is initiated.

2. FOCAL PLANE ARRAY TASK

2.1 SCOPE OF FPA STUDY

The array design task was directed toward developing a detecting element that could perform background removal on-chip and also toward developing an efficient design that would depend on the processor for background removal. In this way a comparison could be made between the two different systems approaches. Combined detector and readout noise were to be kept low so that relatively small optics can be used. The requirements that make off-the-shelf designs inadequate are the very high readout rate and the high dynamic range, that must be achieved while maintaining a very low noise at the small signal level.

Theoretically, the integration time can be reduced to a number close to the transfer time; however, the number of parallel readout lines that can be located along the chip edge is limited by the chip dimension, which in turn is limited according to the yield and cell size considerations described previously.

Table 2-1 shows the requirements allocated to the FPA which were derived from the sensor system requirements. The cell size dimensions, quantum efficiency and number of chips are in the nature of guidelines. It was assumed

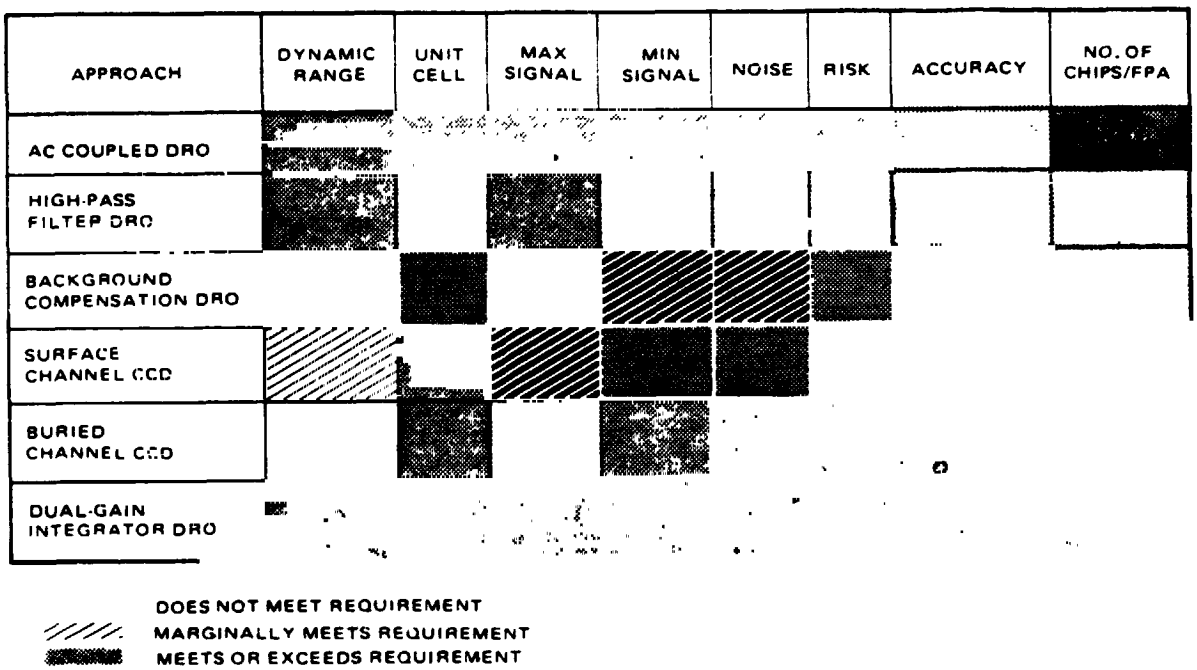
Table 2-1. Focal plane requirements. Above values served as guidelines to design approaches

Noise	$\leq 100\ e^-$
Active area/pixel	$\geq 15\%$
Chip abutting gap	≤ 2 pixels
Cell size	25 to 100 μm
Dynamic range	$>10^4$ (10^6 is a goal)
Quantum efficiency	>30%
Sensor chips/focal plane	4 to 6

for the initial analysis that the optics would be sized to adapt any cell dimension in the range from 25 to 100 μm (1 to 4 10^{-3} inch). The number of pixels across the array should be in the order of 648. The focal plane array is then divided into a number of sensor chips which are of manufacturable size and can be abutted sufficiently closely to give minimum gaps between chips. It is important that the unit cell size be large enough to accommodate the required readout circuit and small enough to give the required pixel count (pixel area = unit cell area) consistent with full earth disc coverage (Section 1.5). The unit cell fill factor, which is the ratio of photo-active area to total area, should be maximized to maintain the required signal level above total noise. Six circuit designs were considered in an effort to meet these requirements. Three approaches (the a-c coupled direct readout (DRO), the high-pass filter direct readout, and the background compensation direct readout) provided background removal on focal plane while three approaches (the surface channel CCD, buried channel CCD, and dual gain integrator direct readout) left background removal to the signal processor electronics. The performance of these six circuits is summarized in Table 2-2. Note that the simplest circuit providing background removal (a-c coupled DRO) suffers from inaccuracy. More complex circuits designed to improve accuracy suffer from a large unit cell size, higher noise and increased risk. Circuits which relied on the signal processor to remove the background were challenged to provide both a large dynamic range and low noise. All six approaches were designed to use silicon detectors and to provide a 648 pixel matrix with good responsivity uniformity (<3 percent variation). Cooling is not recommended because thermal noise is not the dominant factor and the optics can be sized to insure a signal to noise of 4 for the 100 to 250 noise electrons predicted for the various designs.

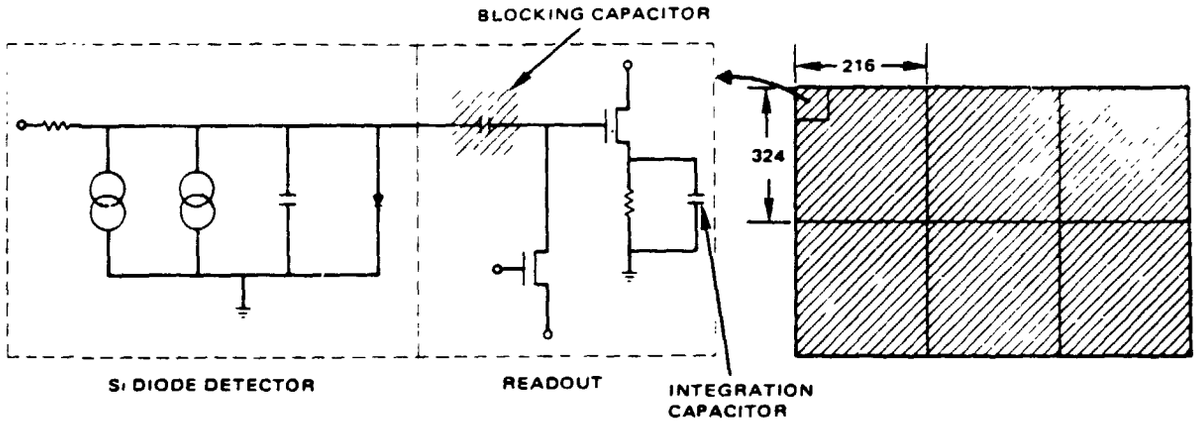
A readout time of 1 msec was used; however, all circuits considered can operate at least three times faster. One means of obtaining greater temporal resolution for specialized regions would be to manufacture a smaller, steerable array utilizing the same circuitry. Another means would be to use the signal processor to address a small subsection of the matrix at a faster rate while ignoring those portions of the matrix that show no sign of lightning activity.

Table 2-2. Performance summary. Eight design/performance criteria are used to compare the various approaches.



2.2 METHODS FOR REMOVING BACKGROUND SIGNAL ON-CHIP

The a-c coupled direct readout is shown in Figure 2-1. A blocking capacitor stops dc background current while passing ac lightning pulse. The energy in the pulse is integrated on a simple MOSFET integrator. This type of circuit provides a low risk, low noise approach with a high (10^6) dynamic range. The entire circuit (detector and readout) can fit in a $(45\ \mu m)^2$ unit cell. If 216 x 324 pixels are allotted per sensor chip a 0.982 cm x 2.1 cm sensor chip results. This is within manufacturing capabilities using the 10X (magnifying) aligner. The unit cells fit in a 1.0 x 1.8 cm block with the decoder size of 0.01 x 1.8 cm and pads of 0.3 x 0.982 cm (see Figure 2-2). A 3 x 2 sensor chip array forms the focal plane with the necessary 648 x 648 pixel matrix. This design uses 54 output lines from the decoder/multiplexer which is well within manufacturing capabilities. The penalty for the simplicity



a. Unit cell

- 0.17 FILL FACTOR
- LOW RISK
- RESET SENSITIVE (NOT BACKGROUND STABILIZED)
- PULSE INTEGRAL INACCURATE
- LOW NOISE (<100 e^-)
- PULSE INTEGRAL INACCURATE
- HIGH DYNAMIC RANGE (10^5)
- ON-CHIP BACKGROUND SUBTRACTION

b. Focal plane array

- $(50\ \mu M)^2$ UNIT CELL
- 0.002 CM X 2.1 CM SENSOR CHIP
- 216 X 324 PIXELS/SENSOR CHIP
- 54 OUTPUTS/SENSOR CHIP

Figure 2-1. Circuit diagram and focal plane array configuration for a-c coupled direct readout.

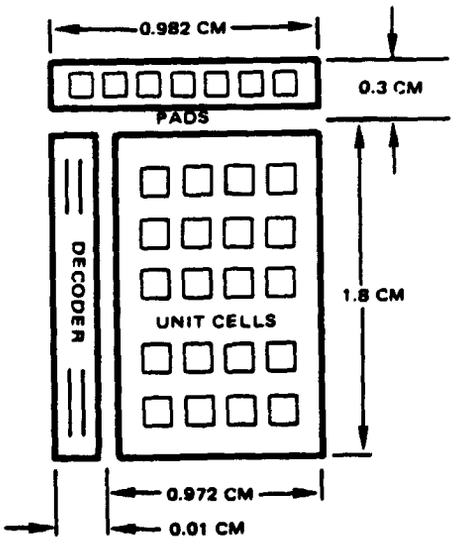
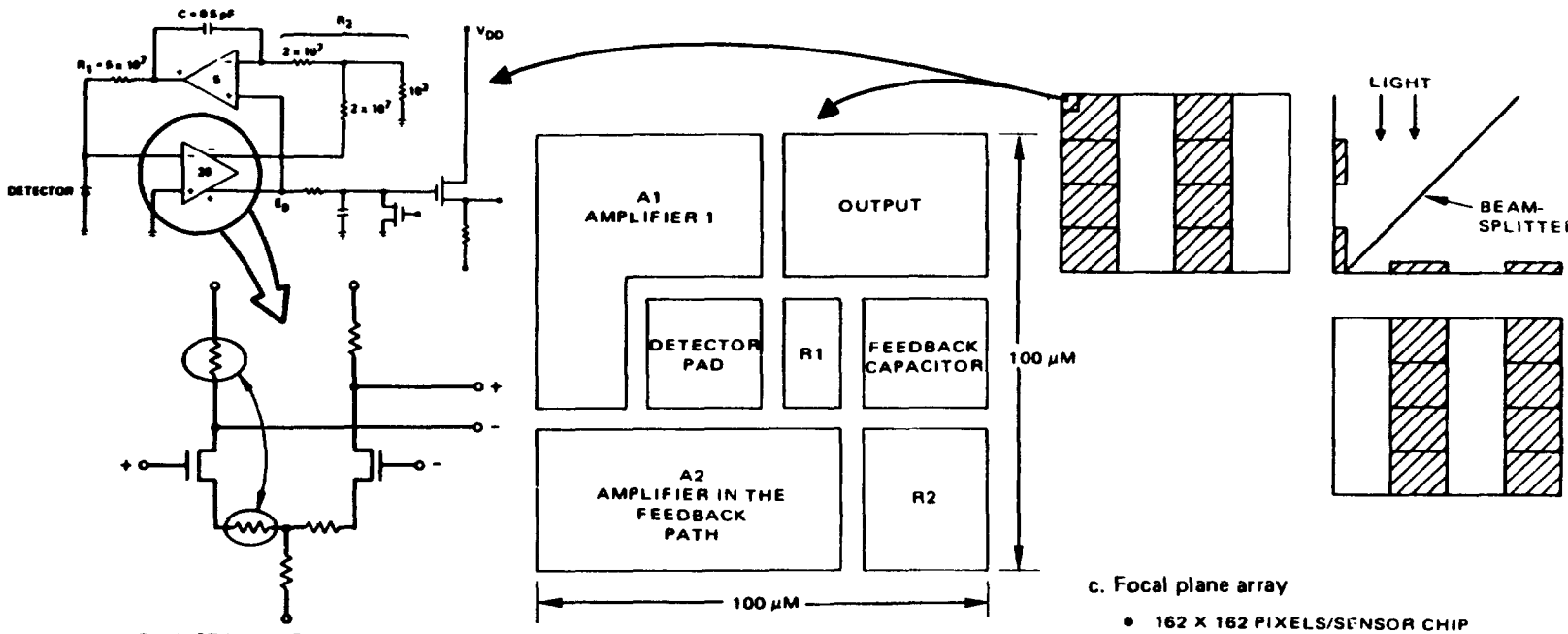


Figure 2-2. Geometry of a sensor chip showing areas devoted to unit cells, decoder/multiplexer, and pads for electrical connections.

of the circuit is that some performance goals are not met. The accuracy of the energy integral of the lightning pulse suffers because the background generated charge, although blocked by the blocking capacitor does affect the initial reset value since this charge is integrated on the blocking capacitor. A second source of inaccuracy was discovered in a computer simulation of the circuit operation. For weak lightning pulses, charge is lost from the integration capacitor resulting in an energy integral that varies with the temporal position of the event relative to the sampling interval. The magnitude of this error could be as much as 30 percent of the actual energy integral which was still within requirements for low signal levels. It cannot be over emphasized that the deficiency of this circuit is due to its extreme simplification and to the desire to keep reasonable component values (e.g.; resistance, capacitance). The number of components was kept to a minimum. This is important in a monolithic design since any area used by the readout is taken away from the photosensitive area. Note that the unit cell fill factor (ratio of detector area to total unit cell area) was 0.17, again within specification. Also because there are few components this direct readout design has low noise (about 100 noise electrons). Even with the unit cell fill factor of 0.17 this low noise permits a signal to noise ratio greater than ten for the minimum signal and the selected aperture.

In an attempt to solve the problem of the background sensitivity of the previous circuit an improved high pass filter was designed. The circuit shown in Figure 2-3 illustrates this design. While the design eliminated the sensitivity to background levels during reset, the problem of an inaccurate integral of pulse energy remained. This was due to charge decay on the integration capacitor. The design uses operational amplifiers and a voltage divider network (R_2) to provide excellent low frequency (background) rejection while keeping component values within manufacturable limits. Because the design uses more circuit components, the noise level is increased to 350 noise electrons. In addition, the unit cell size must be increased in size to 100 μm to accommodate all circuit components (Figure 2-3b). The area left for the detector using a monolithic approach would be only 6.25 percent of the unit



a. Circuit diagram

- MANY COMPONENTS
- HIGH TO MODERATE RISK
- PULSE INTEGRAL INACCURATE
- HIGH NOISE (350 e^-)
- DYNAMIC RANGE (10^4)
- ON-CHIP BACKGROUND SUBTRACTION
- BACKGROUND STABILIZED

b. Unit cell layout

- 0.0025 FILL FACTOR
- $(100\ \mu M)^2$ AREA

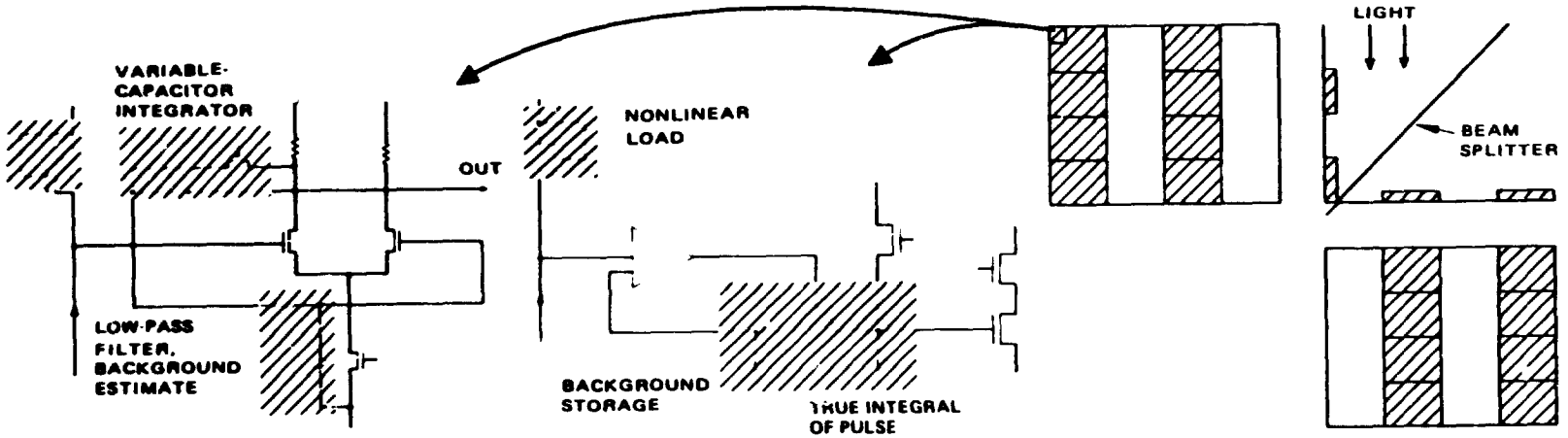
c. Focal plane array

- 162 X 162 PIXELS/SENSOR CHIP
- 1.62 CM X 1.62 CM SENSOR CHIP
- TWO SIDE PAD OUT
- ALIGNMENT
- 11 OUTPUTS/CHIP

Figure 2-3. Circuit diagram, unit cell configuration, and focal plane layout showing beamsplitter for direct readout with high-pass filter. Detail shows the gain-stabilized amplifier. Gain is determined by the ratio of the circled resistors.

cell, hence a hybrid rather than monolithic array is recommended for this design. This approach uses separate detector and circuit pads that are bumped to form interconnections at each unit cell. Although this stacking permits almost unity fill factor, the larger cell size required for the circuitry above allows only 162 x 162 pixels/sensor chip (the largest manufacturable chip is 2.1 by 2.1 cm). Full earth coverage would require a 4 x 4 sensor chip matrix to form the focal plane. Electrical access to the interior sensor chips of this matrix causes large gaps between chips because space must be left for the 54 leads. An optical design which eliminates this problem is shown in Figure 2-3c. This gives full earth coverage and permits electrical input/output pads to be located on both sides of the chip. The optical design for this approach was described in Section 1.6 of this report. The number of outputs from the multiplexer for this design is eleven. Care was taken in the circuit design to reduce sensitivity to temperature and process variations (e.g., gain stabilized amplifier Figure 2-3a). The predicted dynamic range of this design is 10^4 which is slightly below specification. Because of the large number of components per unit cell and the problem of alignment in the optical design and detector hybridization the risk is assessed to be high to moderate.

Two circuit designs which address problems encountered in the previous design are shown in Figure 2-4. Both require the large unit cell $(100\ \mu)^2$ and optical design previously discussed (Figure 2-4c). The number of components has been greatly reduced. The calculated unit cell fill factor of 0.17 allows a monolithic approach. Figure 2-4b illustrates a design which uses a non-linear load to increase dynamic range, a variable capacitor integrator to provide automatic gain control for improved dynamic range and a low-pass filter to give a running estimate of the background. One problem with this design is that the lightning strokes themselves are averaged and included in the background estimate. A large stroke may contaminate this estimate and affect estimation for subsequent pulses. The circuit shown in Figure 2-4a attempts to eliminate this problem by using the lightning pulse to open a switch which equilibrates signal stored on two capacitors. Thus, pulses which have been



a) CIRCUIT (2)

- ON-FOCAL PLANE BACKGROUND SUBTRACTION
- NONLINEAR DETECTOR LOAD
- AUTOMATIC GAIN CONTROL
- MODERATE NOISE (250 e^-)
- MODERATE COMPLEXITY
- MODERATE TO HIGH RISK
- PULSE CONTAMINATES BACKGROUND ESTIMATE

b) CIRCUIT (1)

- ON FOCAL PLANE BACKGROUND SUBTRACTION
- ACCURATE PULSE INTEGRAL
- NONLINEAR DETECTOR LOAD
- HIGH DYNAMIC RANGE (10^6)
- MODERATE NOISE (250 e^-)
- MODERATE COMPLEXITY
- MODERATE TO HIGH RISK

c) FOCAL PLANE ARRAY

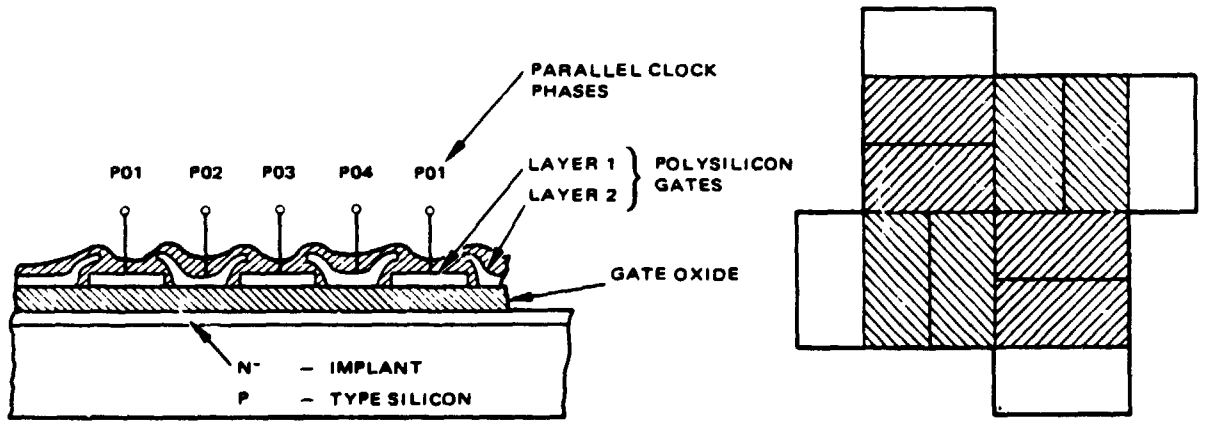
- 0.17 UNIT CELL FILL FACTOR
- (100 M)^2 UNIT CELL

Figure 2-4. Two circuit designs for direct readout with background compensation. The focal plane array configuration is the same as in Figure 2-3.

added into the background estimate are subtracted as well and an accurate integral of energy results. Both circuits have moderate complexity and noise (250 noise electrons). The combination of optical complexity, and moderate number of circuit elements puts this design into the moderate to high risk category. These two circuits are the best candidates for removing background on the focal plane.

2.3 CHIP DESIGNS THAT DO NOT SUBTRACT BACKGROUND SIGNALS

The following designs all depend on the signal processing circuits for background removal. Figure 2-5 shows the buried channel CCD design which is based on the MADAN focal plane array and uses four-phase buried channel CCD elements. Since the CCD gates themselves form the PIN Si diode detector, a 0.96 fill factor results. The buried channel design provides moderate noise



a) UNIT CELL CROSS SECTION

- 0.96 FILL FACTOR
- MODERATE NOISE (250 e^-)
- LOW RISK
- LIMITED DYNAMIC RANGE (4×10^3)

b) FOCAL PLANE ARRAY

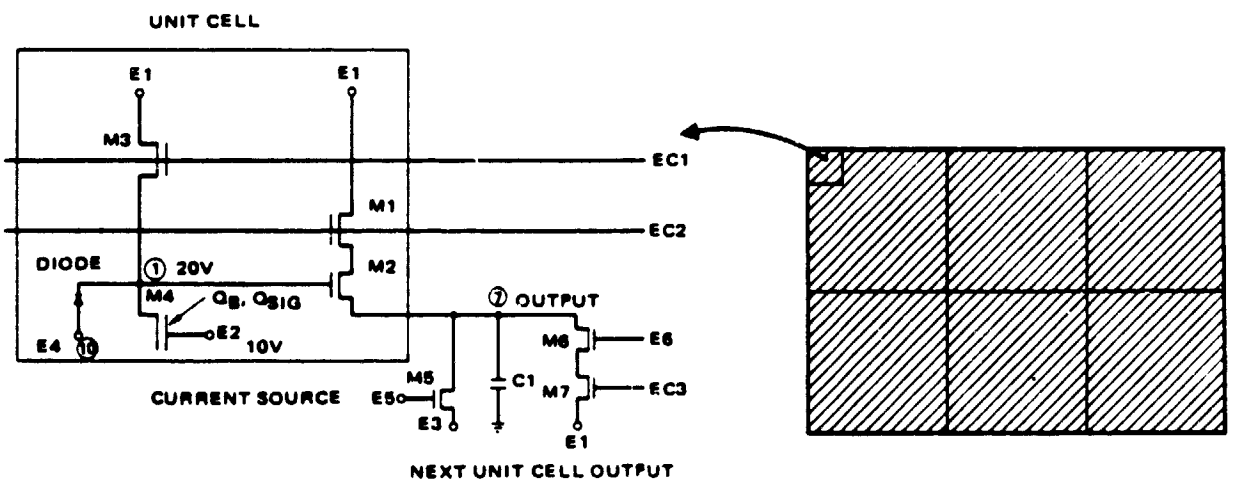
- 2 X (162 X 324) PIXELS/SENSOR CHIP
- $(25\ \mu M)^2$ UNIT CELL
- 0.92 CM X 1.12 CM SENSOR CHIP
- 32 OUTPUTS/CHIP

Figure 2-5. Unit cell of buried channel CCD design shown in cross section. Four-phase clocking is used, and three gates form actual detector. Focal plane array consists of four sensor chips. Each chip is fabricated in two parts.

(250 noise electrons) and because of the high fill factor, signal to noise exceeding 20 is achievable even at the lowest signal levels. A disadvantage of the buried channel is that charge capacity of the CCD is reduced resulting in a dynamic range of 4×10^3. Because of the small unit cell size of the CCD only four sensor chips of 324 by 324 pixels are required to fill the focal plane (Figure 2-5b).

A surface channel CCD design (not shown) would be similar to the buried channel design (Figure 2-5a) except the charge transport would occur at the Si/SiO_2 interface. This results in a higher charge capacity so that dynamic range will be increased to 10^4 at the cost of higher noise (1000 electrons). Thirty-two multiplexed outputs would be used for each 0.92 by 1.12 cm circuit chip to permit complete sampling every millisecond.

The circuit design shown in Figure 2-6 meets or exceeds all performance requirements. The focal plane array shown in Figure 2-6b is the same as that



a) **UNIT CELL**
- HIGH DYNAMIC RANGE (10^6)
- 0.47 FILL FACTOR
- LOW NOISE (100 e^-)
- OUTPUT VOLTAGE 20V
- LOW RISK

b) **FOCAL PLANE ARRAY**
- 216 X 324 PIXELS/SENSOR CHIP
- (50 μM)^2 UNIT CELL
- 0.982 CM X 2.1 CM SENSOR CHIP
- 54 OUTPUTS/CHIPS

Figure 2-6. Unit cell circuit diagram and focal plane array layout for dual-gain integrator direct readout.

described in Figure 2-1b. The entire circuit fits in a 45 by 45 μm unit cell. The sensor chip of 216 by 324 unit cells is shown in Figure 2-2. A fill factor of 0.47 is achieved because charge generation occurs under a large MOSFET gate as in the CCD design, while other MOS components are few and small in size. The DRO approach is expected to restrict the noise electrons to 100. At small photon flux levels, photo-generated charge "sees" only the small diode capacitance C, at node 1; since $V = Q/C$, a nominal gain results. Since at higher photon flux levels, the photon charge "sees" the full diode plus MOSFET capacitance $C_2 > C$, $V = Q/C_2$, which results in a smaller gain. The point at which the gain change occurs ($Q > Q_S$) can be preset. The design accepts a large dynamic range (10^6) with accuracy that scales for the two levels. A variation of this design is presently in use, hence the risk is estimated to be low. This last design was judged to be the preferred approach and will be discussed in more detail.

2.4 DESIGN DETAILS AND PREDICTED PERFORMANCE FOR RECOMMENDED FPA

Figure 2-7 shows the response of a typical PIN photo diode such as that formed by the gate of a MOSFET. The expected responsivity at optimal bias is 0.2 ampere/watt at 8683Å. Should NASA decide to use the 7774Å line, the bias could be changed to provide essentially the same responsivity.

An expanded circuit diagram is shown in Figure 2-8. Photons incident on the M4 MOSFET gate E2 or the diode E4 are swept to the diode node 1 by the potential difference between Node 1 and E2, in this case 10 minus 20 volts or 10 volts. When sufficient charge has accumulated in the diode capacitance well to equal 10 volts, the MOSFET well is accessed and begins to accumulate the rest of the charge on its capacitance. Thus the gain of the transduced voltage switches from one value to another at a preset charge quantity.

After integration, the voltage corresponding to the photo-generated charge is read out using MOSFET M2 and the storage capacitor (diode and MOSFET M4) is reset using MOSFET M3. The timing diagram for this operation is shown in Figure 2-9. Note that valid signal levels are available for 0.5 μsec every 1 msec on 54 output leads for each chip. This allows an adequate sampling aperture for the processor.

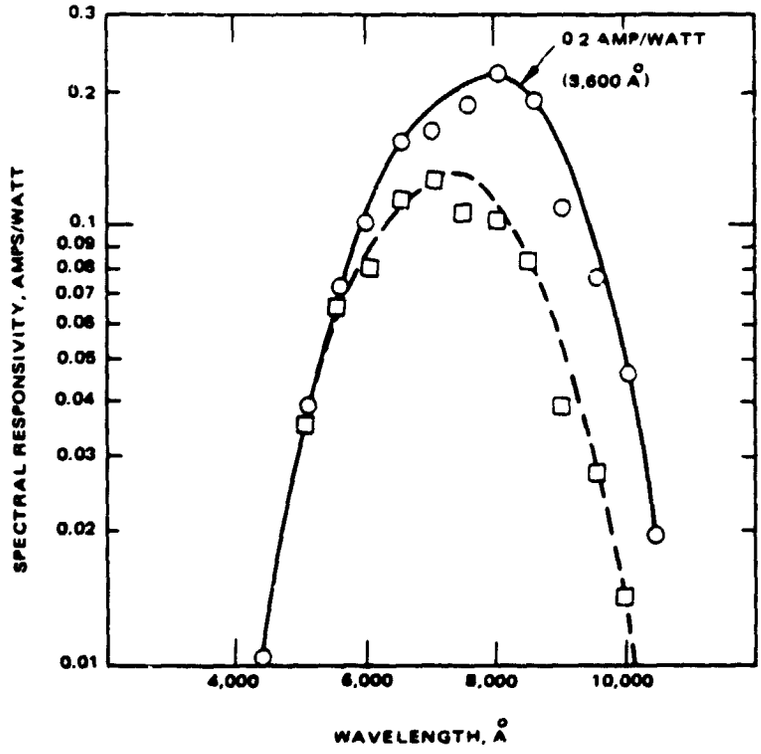


Figure 2-7. Spectral response of PIN diode at two bias values. Graph represents actual experimental data.

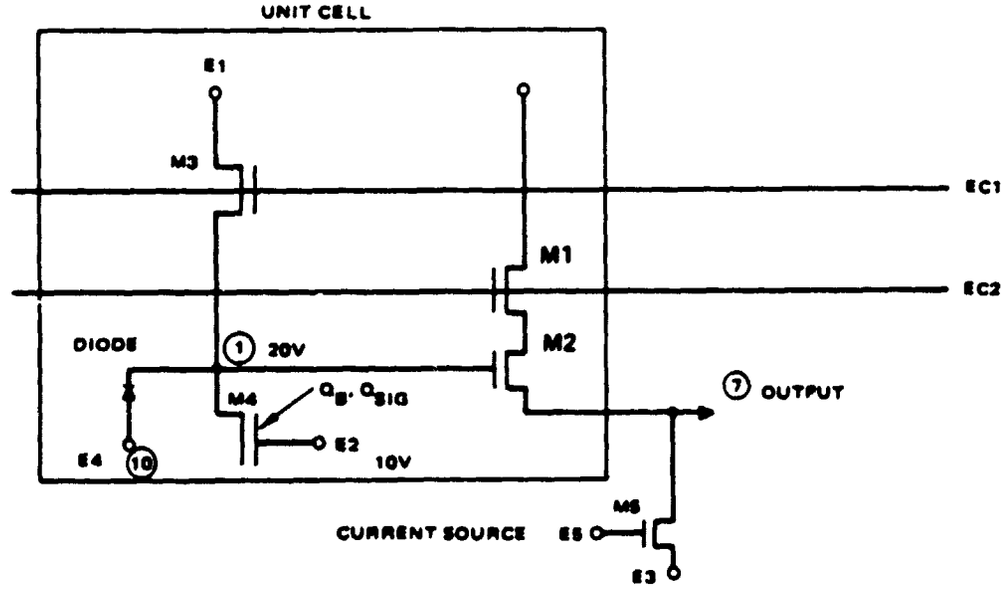


Figure 2-8. Unit cell circuit diagram for dual-gain integrator direct readout.

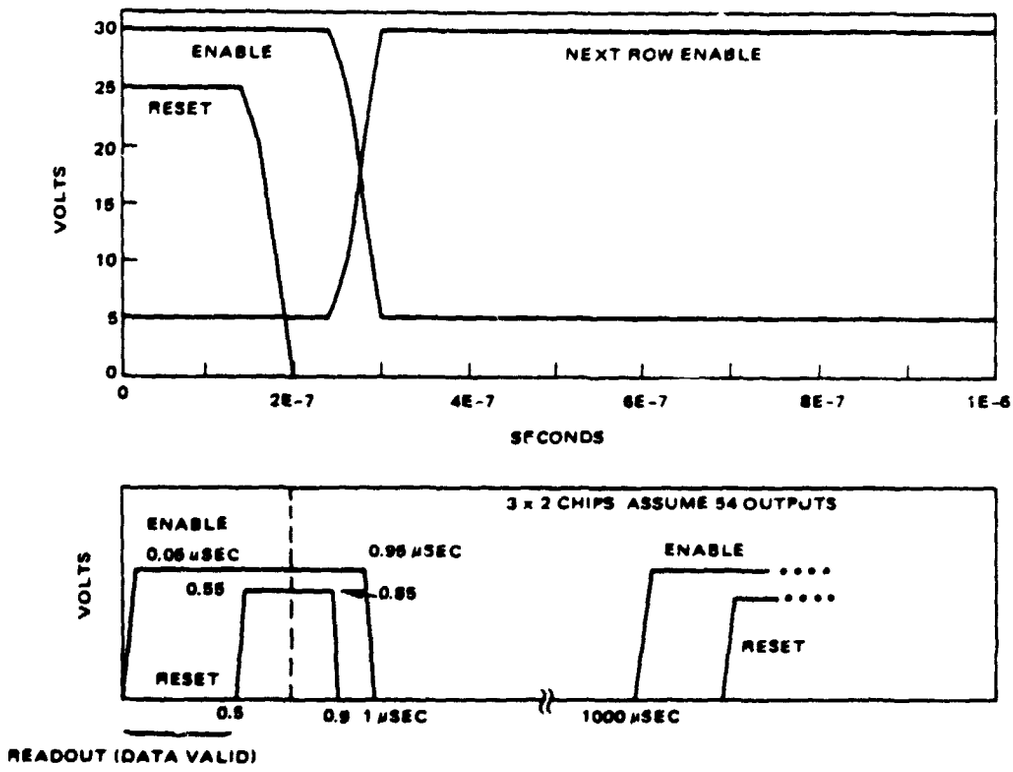
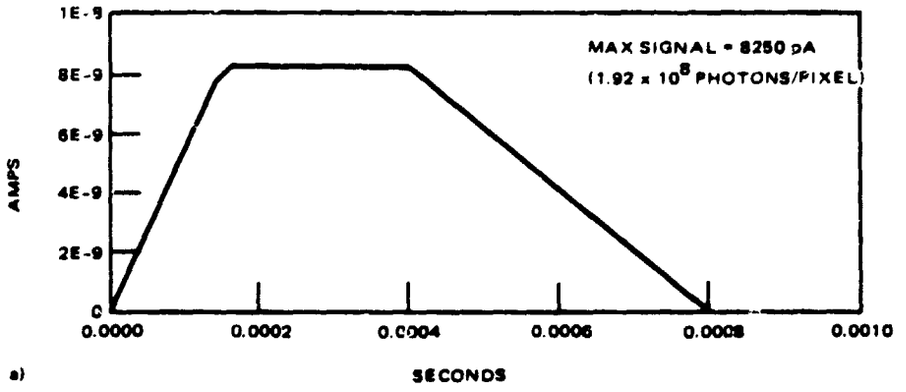
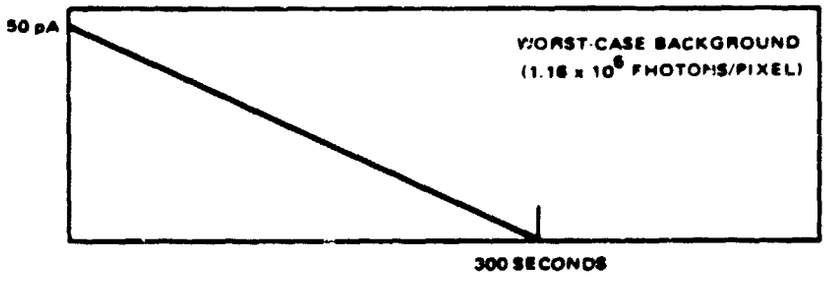


Figure 2-9. Timing diagram for reset and enable operations.

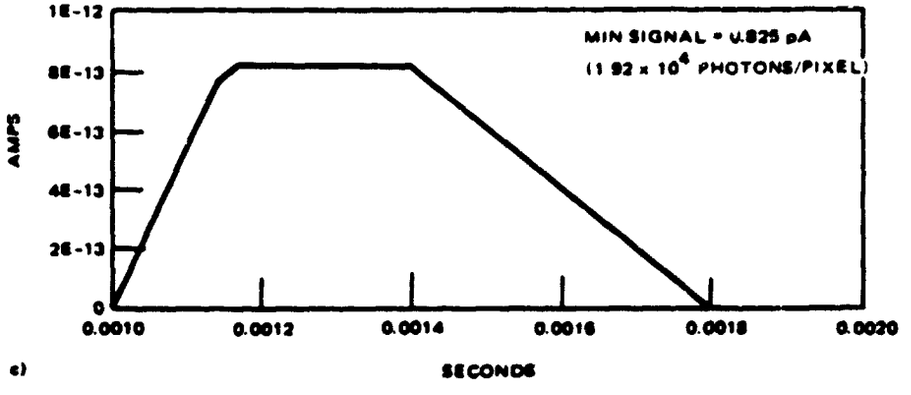
Figure 2-10 shows the expected input current characteristics produced by the maximum and minimum lightning strokes as well as the worst-case background of a fully illuminated cloud filling a pixel. Photon levels and temporal characteristics were calculated from early data and are subject to later revision (maximum and minimum signal levels of 1.92×10^8 photons/pixel and 1.92×10^4 photons/pixel are revised later in this report to the more accurate values of 1.65×10^8 photons/pixel and 1.65×10^4 photons/pixel, respectively, as shown in Table 2-3). These input signal characteristics should be construed as approximations to specified inputs. The circuit can accommodate a fairly significant departure from this illustration. Using a cloud velocity of 72 km/sec to represent a relatively fast change, it was calculated that a cloud edge would take 600 seconds to traverse a pixel, which would cause the current ramp shown



a)



b)



c)

Figure 2-10. Input signal characteristics assumed for analysis purposes.

Table 2-3. Comparison of two preferred readout approaches against selected performance requirements

Parameter	Requirement	Dual Gain Integrator DRO	CCD
Noise equivalent photons	To detect minimum signal	709 ph (100 e^-)	868 ph (250 e^-)
Maximum detectable signal	1.65×10^8 photons	6.18×10^8 photons	3.47×10^6 photons
Minimum detectable signal	1.65×10^4 photons	(709 x S/N) photons	(868 x S/N) photons
Dynamic range	1.28×10^4	8.72×10^5	4×10^3
Maximum background	9.05×10^5 photons	–	–
Minimum detectable signal at maximum background	1.65×10^4 photons	(1190 x S/N) photons	(1290 x S/N) photons

in Figure 2-10b (note that the worst-case background flux of 1.16×10^6 photons/pixel is later corrected to 9.05×10^6 photons/pixel in Table 2-3).

Figure 2-11 illustrates the output voltage at the detector produced by the worst case scenario. In Frame 1 (T 1) the maximum stroke occurs during the worst-case background producing the largest expected signal. In Frame 2 (T 2), the smallest signal occurs superimposed on the worst-case clutter. Frames 2 and 3 (T 3, T 4) are reference frames to simulate the change in voltage produced by the worst-case background alone (ΔV). The challenge is to accurately measure the small signal of Frame 2 after accommodating the large signal in the immediately preceding frame. Figure 2-12 is an expansion of Frame 1. The ordinate gives the output voltage at the detector node 1, and time is shown along the abscissa. For reference the temporal signature of the maximum signal has been superimposed on the graph. The magnitude of this signal does not correspond to the x axis (see Figure 2-10). Figure 2-12

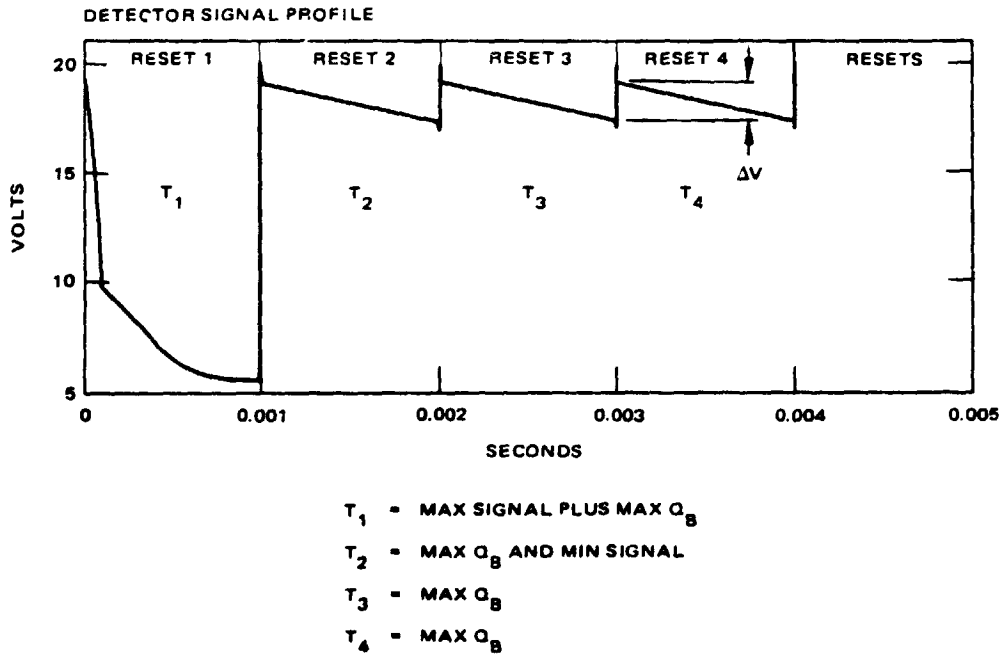


Figure 2-11. Simulation of four-frames of circuit as seen at detector node under indicated irradiance levels.

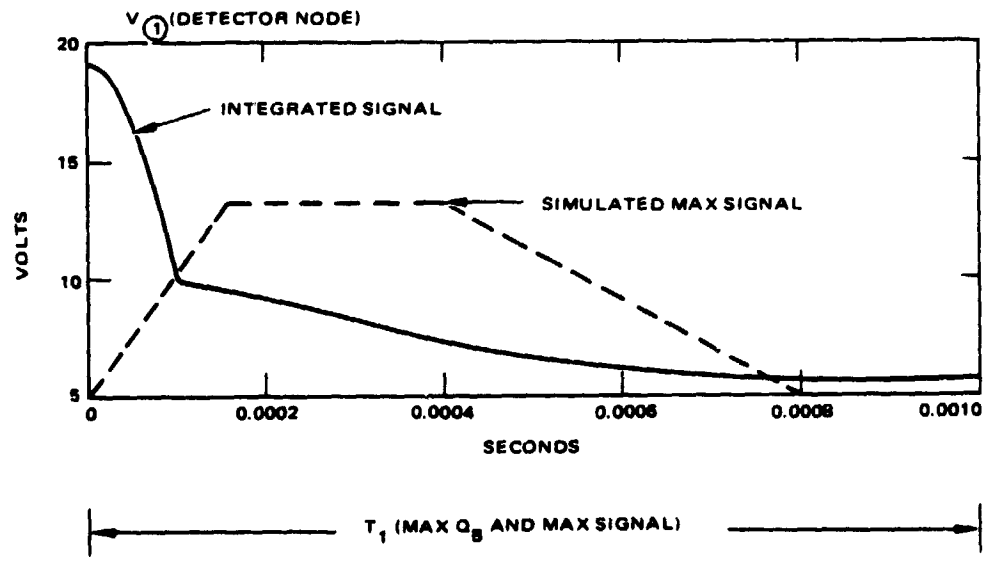


Figure 2-12. Expansion of frame one in Figure 2-11, showing detector output voltage. Input signal strength is included for reference. The area under the dashed curve corresponds to the charge quantity at which the gain switch occurs.

illustrates the gain (slope) change which oc. s at the preset value of 10 volts. Initially, the slope is steep, implying a high gain. When the preset change quantity Q_s has accumulated on the diode capacitance (shaded area under dashed curve), the gain switch occurs. The subsequent shallow slope implies a much smaller gain as the rest of the charge accumulates under the MOSFET (M4) gate. By the end of the input (0.8 msec), the slope is zero, indicating that the circuit has stopped integrating charge. This novel dual gain approach provides high sensitivity for the detection of small signals, while also providing high dynamic range for the measuring of large signals.

Figure 2-13a shows the output voltage at node 7 produced by the four frame simulation (See Figure 2-11). The time scale is expanded in Figure 2-13b

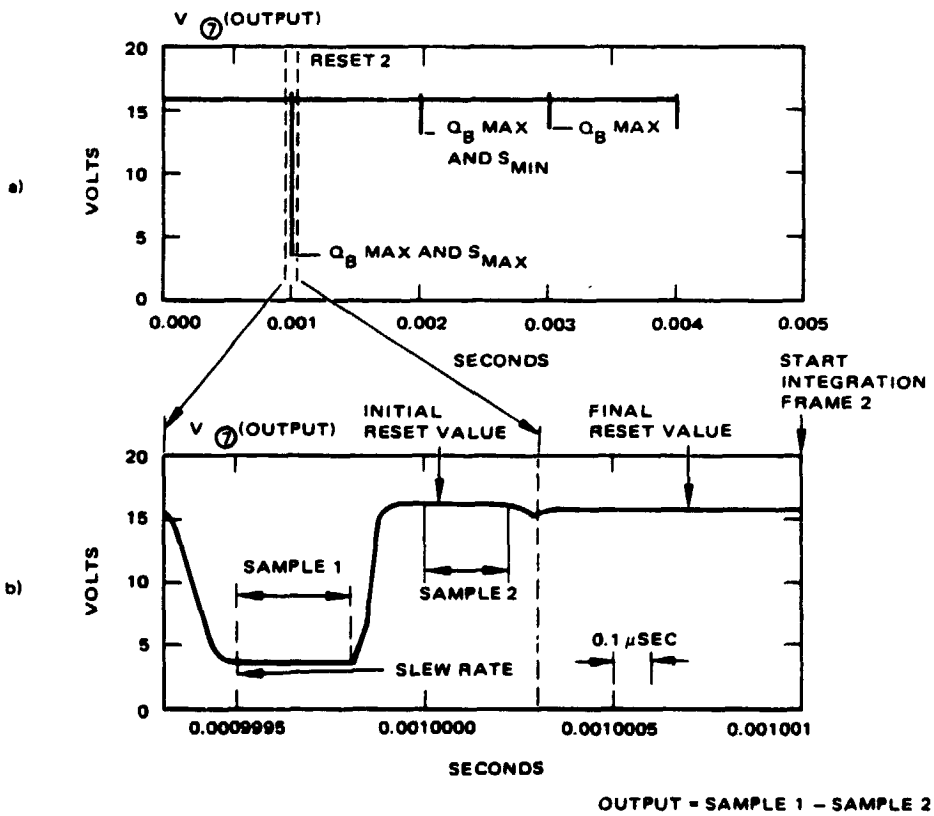


Figure 2-13. Four-frame simulation of output of source follower MOSFET.

to show how a signal proportional to the charge integral is extracted. Once the circuit has slewed up to a stable voltage, a sample is taken anywhere in the interval labeled sampling. The slew rate can be increased to allow a broader sampling aperture at the cost of increased power consumption. The capacitor is reset and a second sample taken in the interval "Sample 2." The difference between these two voltage levels is proportional to the integral of the photogenerated charge. In this example the difference is about 12 volts. A slight transient occurs as a MOSFET switch closes (see Figure 2-9) and the circuit settles down to a final reset value read to start integration in the next frame.

Figure 2-14 shows both the detector Node 1 and the output Node 7 in the presence of the minimum signal plus maximum background and with maximum background only. Note that reset 3 corresponds to the integration which occurred in Frame 2 and reset 4 to Frame 3. The voltage corresponding to the minimum signal at the input is the difference between the voltage values in Figure 2-14a and 2-14b (or 2-14c and 2-14d at the output). The difference between Figures 2-14a and 2-14b is plotted in Figure 2-15 as a function of time. The signal (Figure 2-10c) produces a 15 mV voltage swing at the detector in 0.8 msec. The level can be detected with conventional signal processing electronics.

Figure 2-16 shows the actual mask layout of the circuit, illustrating relative component sizes. The M4 plus D1 area form the detector giving the 0.47 fill factor. The circuit easily fits into a $(45\ \mu m)^2$ unit cell.

Table 2-3 compares the DGI-DRO and the CCD. The noise-equivalent photon number is that number of photons incident on a pixel which produces a signal just equal to the noise. For example, 868 photons incident on the CCD unit cell would produce 250 electrons in the detector. Since the CCD itself produces an estimated 250 noise electrons, this gives a signal-to-noise ratio of unity. Similarly 709 photons incident on the DGI-DRO would produce 100 electrons, which equals the number of noise electrons for the DGI-DRO device. It is important to note the effect of fill factor because, although the CCD has 2.5 times the noise of the DGI-DRO, the incident photon flux needed to produce a S/N of unity is only 1.22 times as great because the large CCD fill factor

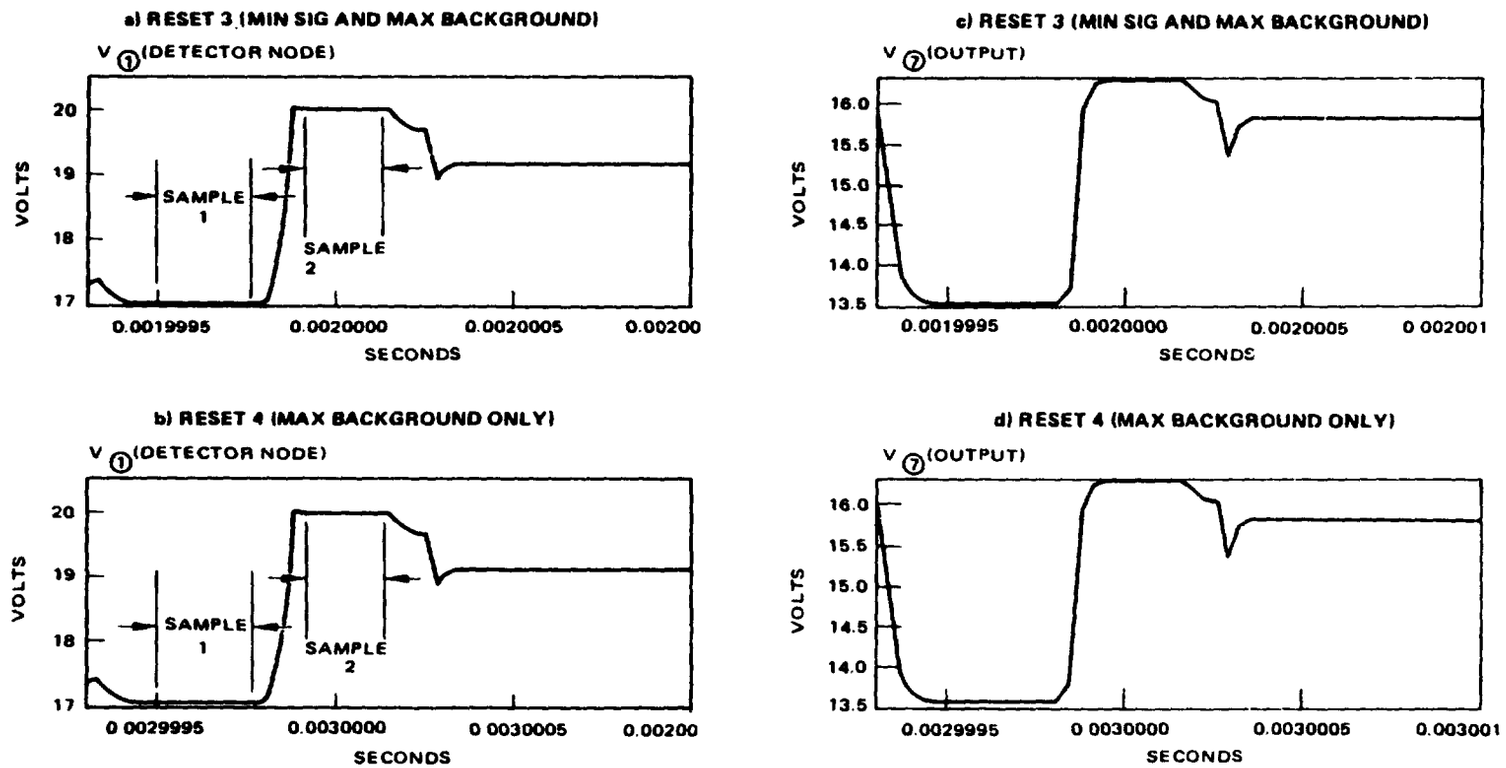


Figure 2-14. Graphs showing detection of minimum signal under maximum background conditions.

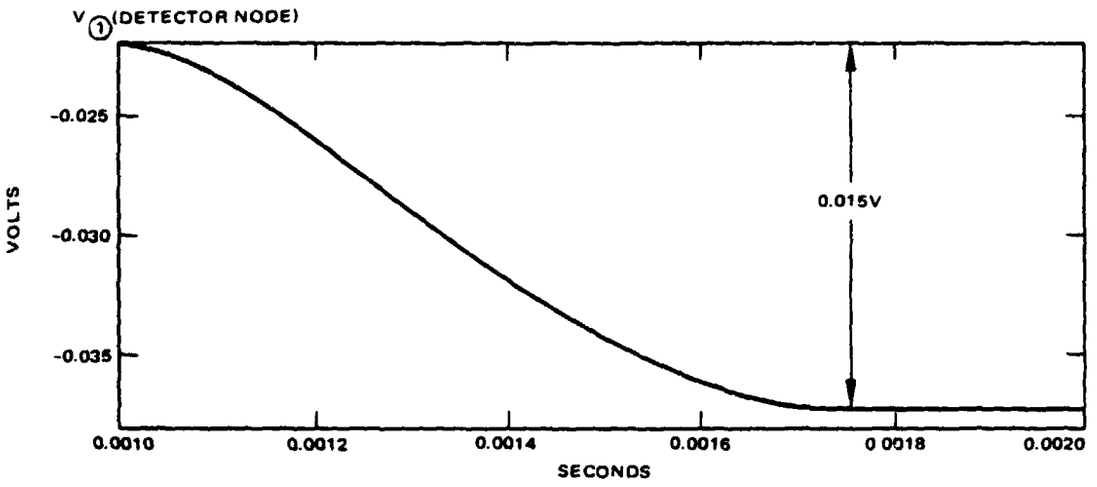


Figure 2-15. Graph showing difference between Frames 2 and 3 in Figure 2-11 and illustrating extraction of minimum signal under maximum background conditions. (cf. Figure 2-14)

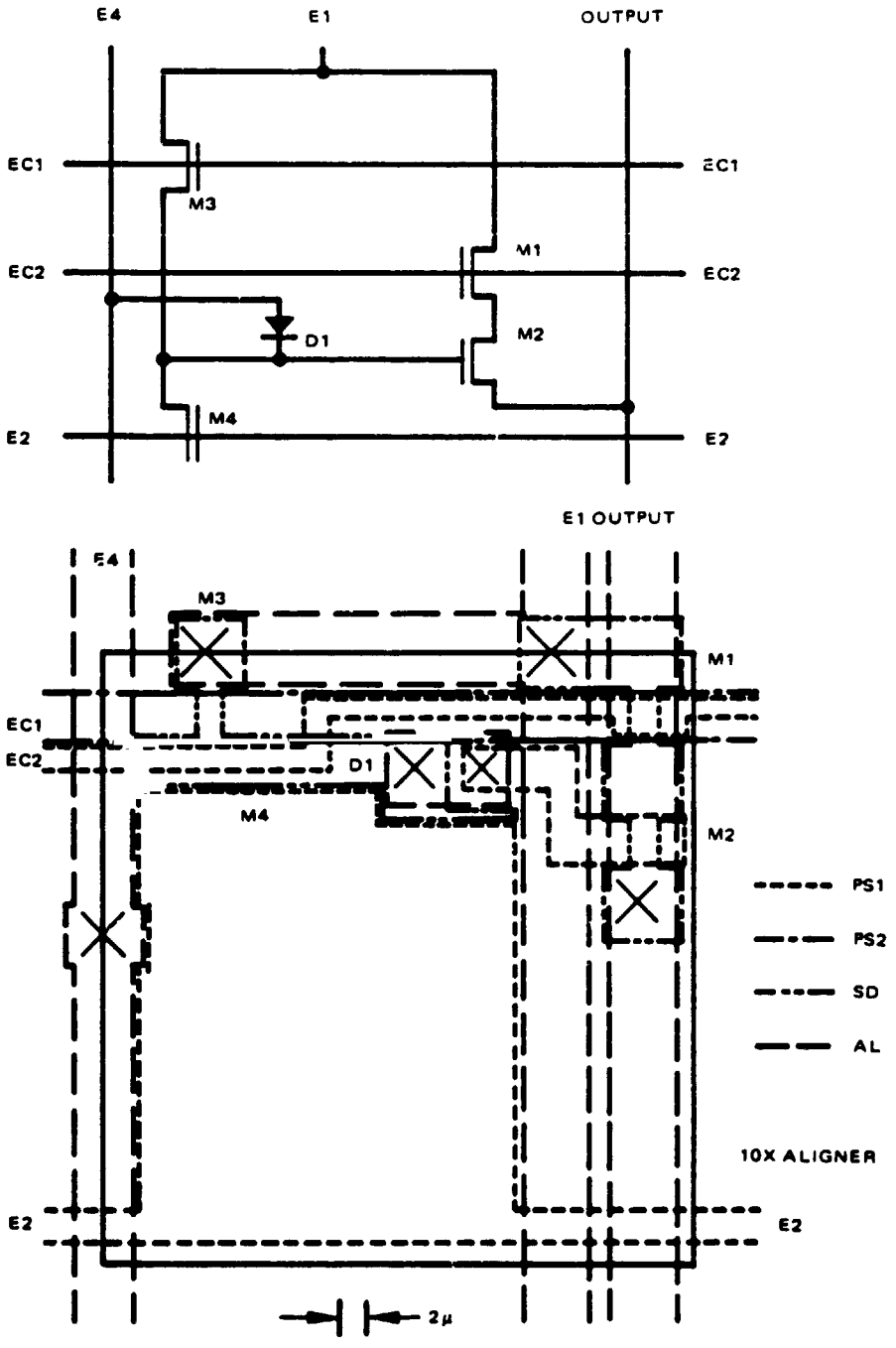


Figure 2-16. DGI-DRO unit cell layout design (50 μm x 50 μm unit cell) Layout is shown below circuit diagram for component identification.

(0.97 as opposed to 0.47 for the DGI-DRO) allows for the more efficient collection of incident photons. A quantum efficiency of 0.3 was used to estimate the conversion ratio of electrons produced for each incident photon. The maximum detectable signal is the number of photons which would fill or saturate the capacitor (CCD bucket) of the DGI-DRO (CCD). Total charge capacity, fill factor, and quantum efficiency are used in the calculation. The minimum detectable signal is determined by choosing a signal to noise ratio which gives an acceptable false alarm rate and multiplying this by the number of noise equivalent photons. Dynamic range is defined here as the ratio of the maximum signal to the minimum signal. Since the detection limit occurs at a signal-to-noise ratio of unity and is ultimately limited by read-out noise, the dynamic range described above is equivalent to the maximum detectable signal divided by the noise equivalent photons. For the worst case background model, the photon noise caused by the background dominates the internally generated noise so that the minimum detectable signal is larger than for the night or low background operation. Calculations shown in Table 2-3 assumed that a stroke filled the instantaneous field of view of the detector. For events which do not fill the pixel footprint or which spill into adjacent pixels, the requirements values in column one must be correspondingly adjusted. Based on this study we feel that the DGI-DRO exceeds all requirements in Table 2-3 by a factor of at least three.

2.5 REVIEW OF EXISTING FOCAL PLANE ARRAY TECHNOLOGIES FOR LIGHTNING MAPPER

The preceding sections have described the application of new, low risk technology to the lightning mapper problem. This approach was adopted only after considering existing technologies which would represent off the shelf solutions to the focal plane design. These considerations are discussed in the following sections and are included for completeness although the results are negative.

Figure 2-17 shows the basic approaches available in focal plane array technology. The hybrid approach involves fabrication of separate diode detector and readout arrays and then mating them using indium bump

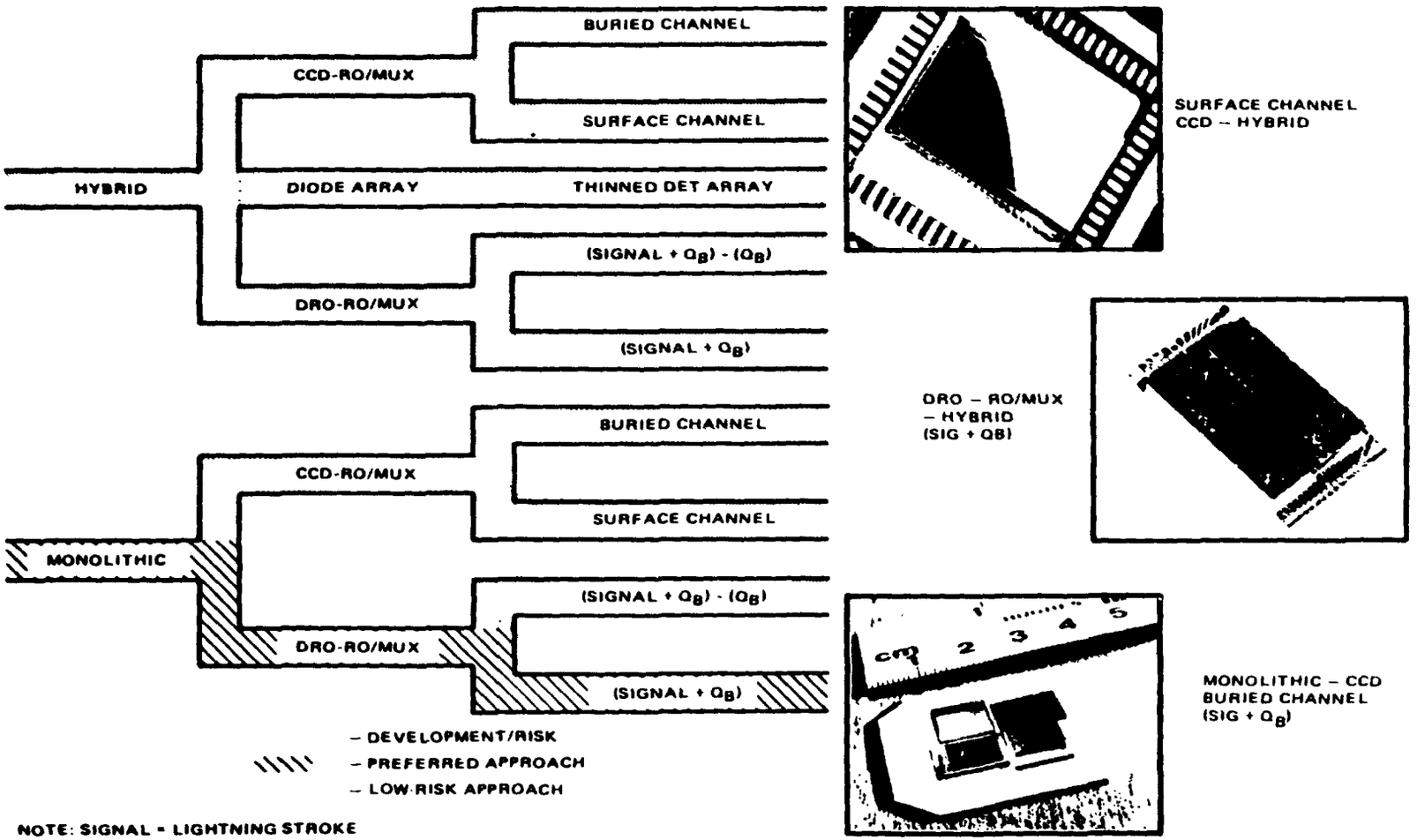


Figure 2-17. Focal plane array techniques studied for lightning mapper application.

interconnect technology. Both buried and surface channel CCD hybrid focal planes have been fabricated using this technique. Because of the nature of the CCD readout, background subtraction cannot be done on a local pixel to pixel basis although global background subtraction schemes have been devised. The direct readout with multiplexer (DRO-RO/MUX) wherein pixels can be addressed on an individual basis, offers the flexibility to do background subtraction on or off focal plane as shown in Figure 2-17. The major drawback of the hybrid approach is that the detector array must be fabricated on a thick substrate to maintain structural integrity during the bump interconnection process. After interconnection the diode array must be thinned to permit photon penetration through the diode material to the active junction. This thinning process is currently in use, however experience indicates a reduction in yield with attendant increase in cost and/or risk. The monolithic approach in which the detector is fabricated in the silicon substrate along with the readout circuit offers an inherently lower risk approach. In this case, noise considerations rule out the surface channel CCD, while the lowest risk, buried channel CCD approach, offers the benefit of proven technology at the expense of some performance.

2.6 TECHNOLOGY BACKGROUND IN RELATION TO RECOMMENDED FPA DESIGN

Hughes has an existing technology base which allows us to pursue a low risk program designed to produce the focal plane described in Section 2.4. Our confidence that we can and will meet the design goals is based upon the combined experience described below.

Table 2-4 provides a brief summary of the review of existing readout technologies highlighting the advantages and disadvantages of each. Figures 2-18 through 2-21 are photographs of devices that show the established manufacturing capability of Hughes Aircraft Company. Figure 2-22 is a historical perspective of design improvements at Hughes which resulted in low noise readouts. (Note that the lightning mapper noise requirement as shown on the graph is easily met by DRO designs.)

Table 2-4. Focal plane study issues

Method	Advantages	Disadvantages
Structure		
Hybrid	Unity fill factor Detector and readout optimized separately Bump interconnection involves low risk	Thinning of detector required after hybridization
Monolithic	Simple processing No thinning required	Pixel fill factor may be as low as 47 percent
Conclusion: Monolithic structure provides low-risk, high-performance sensor chips.		
Background removed		
On chip	Reduce complexity of processor	Complex unit cell Large cell size (100 μm) Beamsplitter required 16 chips needed for focal plane
Off chip	Simple unit cell (25 to 45 μm) 4 to 6 chip focal plane Simple optics	Added complexity for processor
Conclusion: Off chip approach offers low risk with high performance. Processor complexity is quite acceptable.		
CCD		
Buried channel	Low noise <110 electron charges 324 by 324 array available	Low dynamic range (4×10^3) No background-removal method known with 25-μm pixel

Table 2-4 (cont.)

Method	Advantages	Disadvantages
CCD		
Buried channel	Proven performance Radiation hardened	
Surface channel	45 by 90 array available Proven performance	Low dynamic range ($<10^4$) No background removal method known with 25-μm pixel High noise
Conclusion: Buried channel CCD preferred to surface channel CCD because noise is lower. Other factors essentially equivalent.		

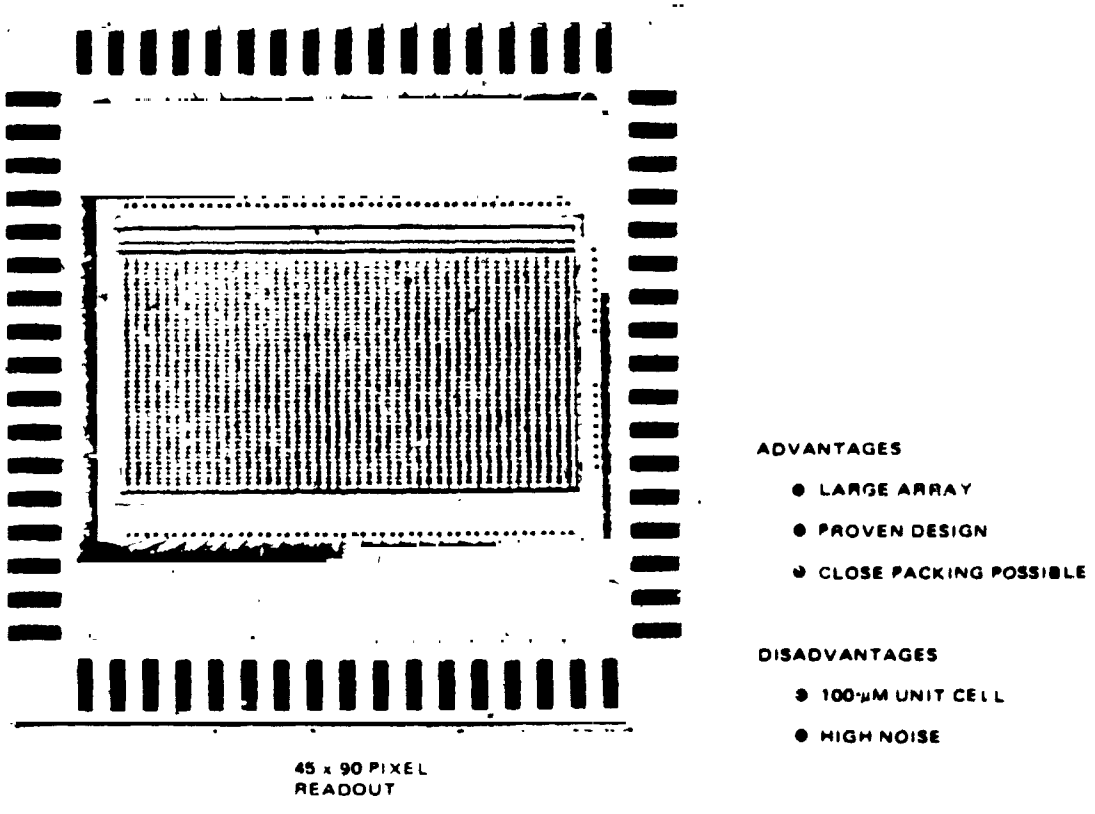


Figure 2-18. Surface channel CCD direct injection.

2 x 128 PIXEL
READOUT

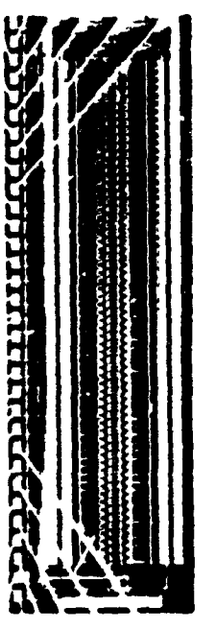
ADVANTAGES

- T_i = 1 MSEC
- 10^5 DYNAMIC RANGE

DISADVANTAGES

- NOISE 100 NOISE ELECTRONS
- REQUIRES LARGE UNIT CELL SIZE 3 x 20 MILS FOR COMPLEX CIRCUITS

Figure 2-19. Synthetic T/A unit cell.



10 X 64 PIXEL
READOUT

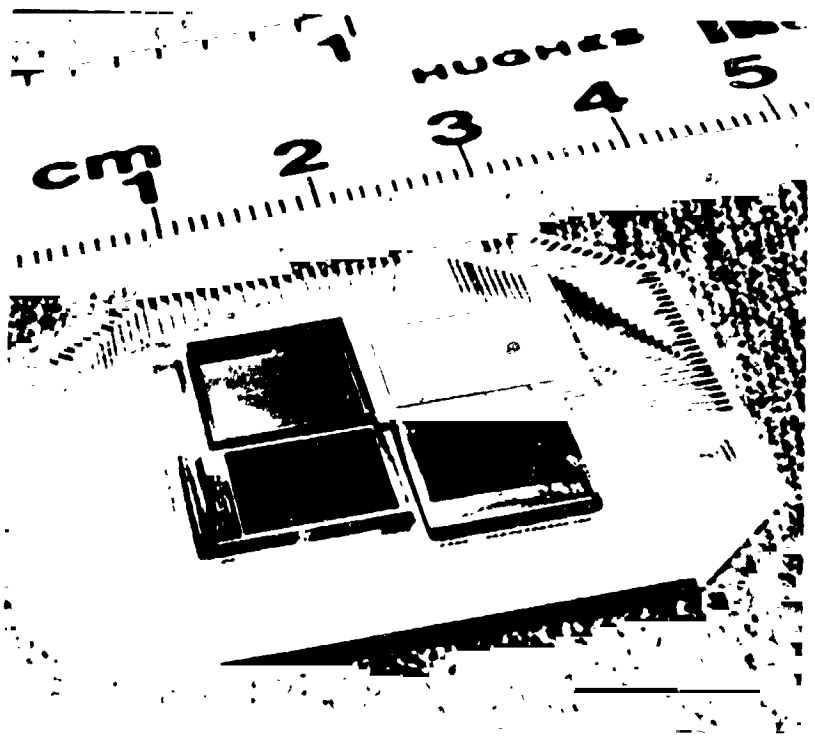
ADVANTAGES

- LOW NOISE
- SIMPLE HIGH-YIELD DESIGN
- SMALL UNIT CELL

DISADVANTAGES

- LOW DYNAMIC RANGE < 10^4

Figure 2-20. Direct integration DRO.



ADVANTAGES

- DEMONSTRATED DESIGN
- SMALL UNIT CELL
- LOW NOISE

DISADVANTAGES

- LOW DYNAMIC RANGE $< 10^4$
- CHIP-ABUTTING GAPS ARE EXCESSIVE

Figure 2-21. Monolithic buried channel CCD.

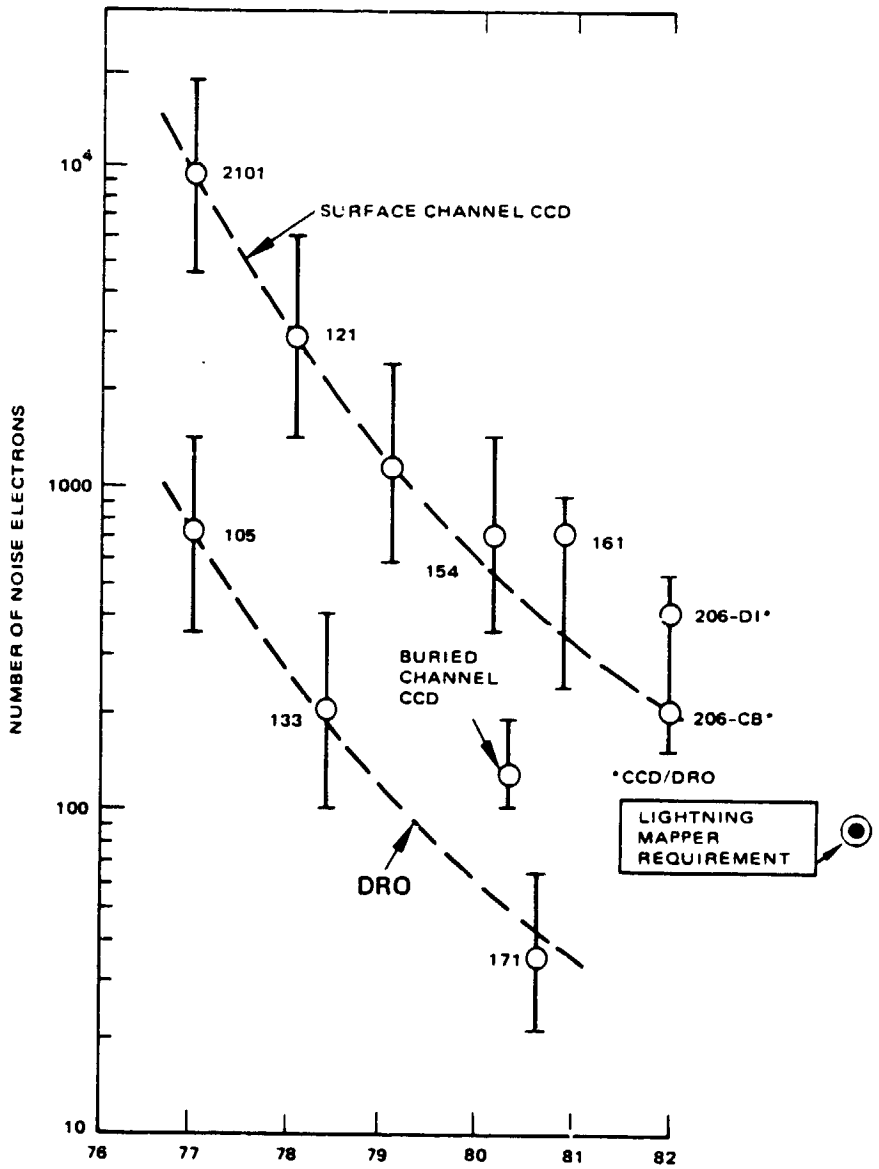


Figure 2-22. Focal plane readout/multiplexer performance history.

The two focal plane alternatives recommended as a result of the study are summarized in Table 2-5. The packaging and assembly of the buried channel CCD is shown in Figure 2-23 while that of the DRO is shown in Figure 2-24. Either packaging design is judged to have a low risk factor. The CCD is presented as an alternative or back-up technology to the preferred DRO approach.

Table 2-5. Study conclusions regarding FPA alternatives

Parameter	CCD Visible Imager	Modified SFD-DRO Visible Imager
Pixel size Sensitive area	25 μm x 25 μm (96% of pixel)	50 μm x 50 μm (47% of pixel)
Chip size	324 pixels x 324 pixels	325 x 216 pixels
Chips/FPA	4	6
Dynamic range	5×10^3 (1×10^4 required)	1×10^5 to 1×10^6
Data output lines	32 per chip (128 total)	54 per chip (324 total)
SNR (min signal and max Q_B)	6 (BLIP)	6 (BLIP)

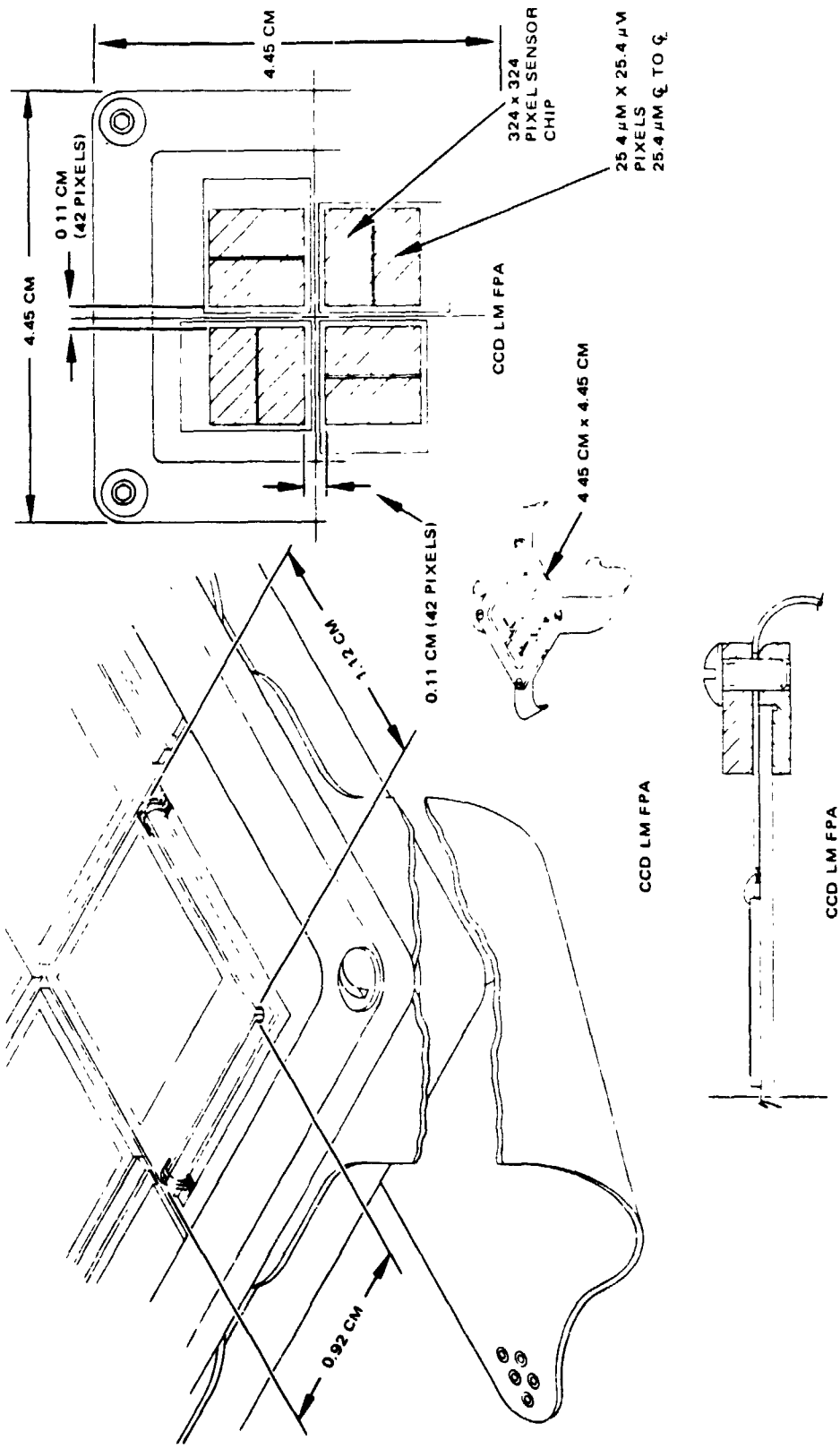


Figure 2-23. Buried channel CCD for lightning mapper focal plane assembly.

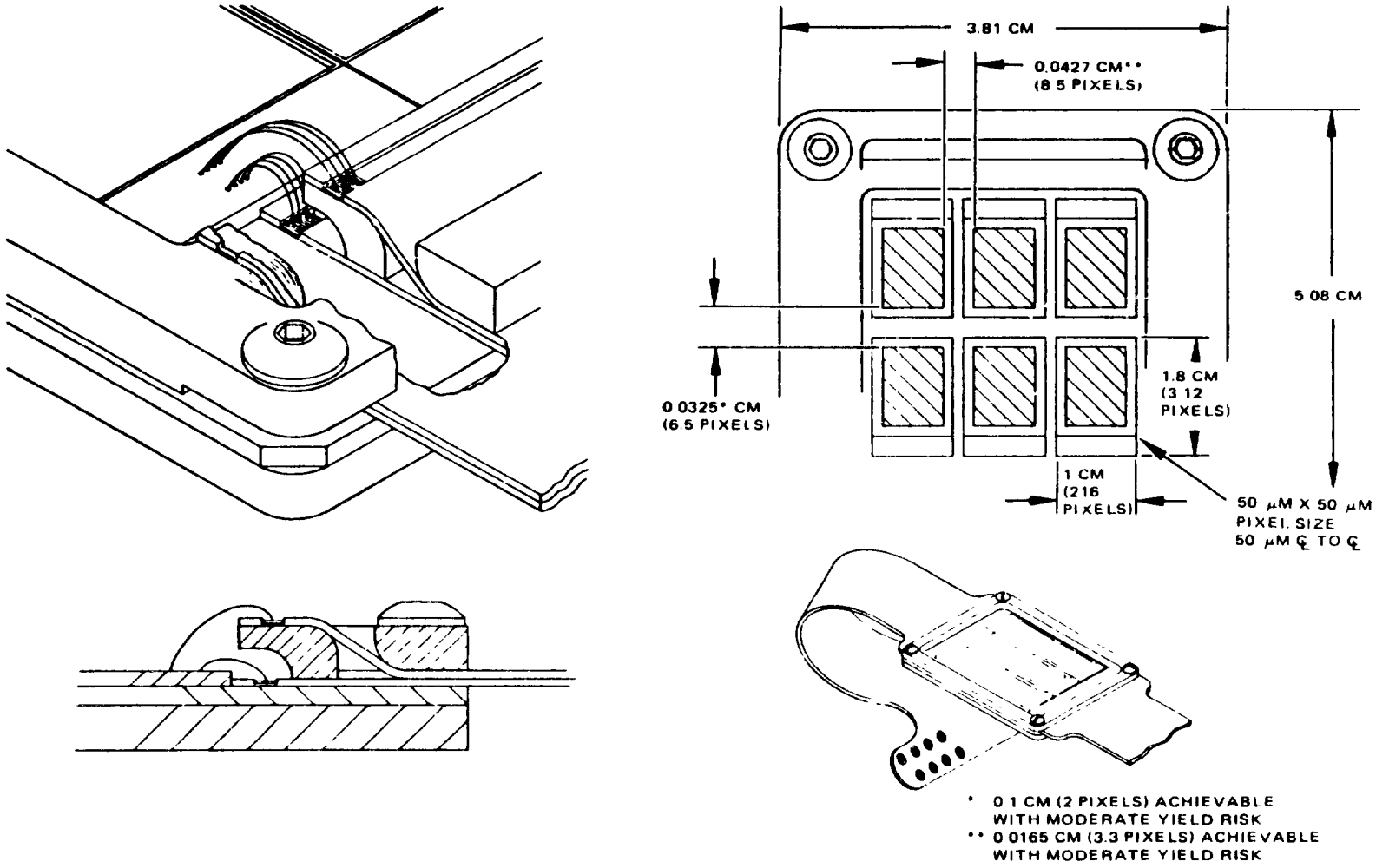


Figure 2-24. Modified SFD-DRO for lightning mapper focal plane assembly.

3. SIGNAL PROCESSOR TASK

3.1 SCOPE OF PROCESSING TASK

Initially we considered the functional requirements for a complete lightning sensor/mapper system and allocated them between the space and ground segments of the system.

Basically, the purpose of space segment data processor is to reduce the volume of data for transmission to ground by identifying the lightning events while preserving the required scientific characteristics.

Ground segment processing can then be made completely flexible to serve a variety of scientific needs which may involve different coordinate systems and correlation of events with a number of different data bases.

The study reported here concentrated on defining an architecture for the on-board processor which was compatible with other components of the space sensor and which would be relatively inexpensive to implement, while still meeting the space segment processing requirements indicated in Figure 3-1.

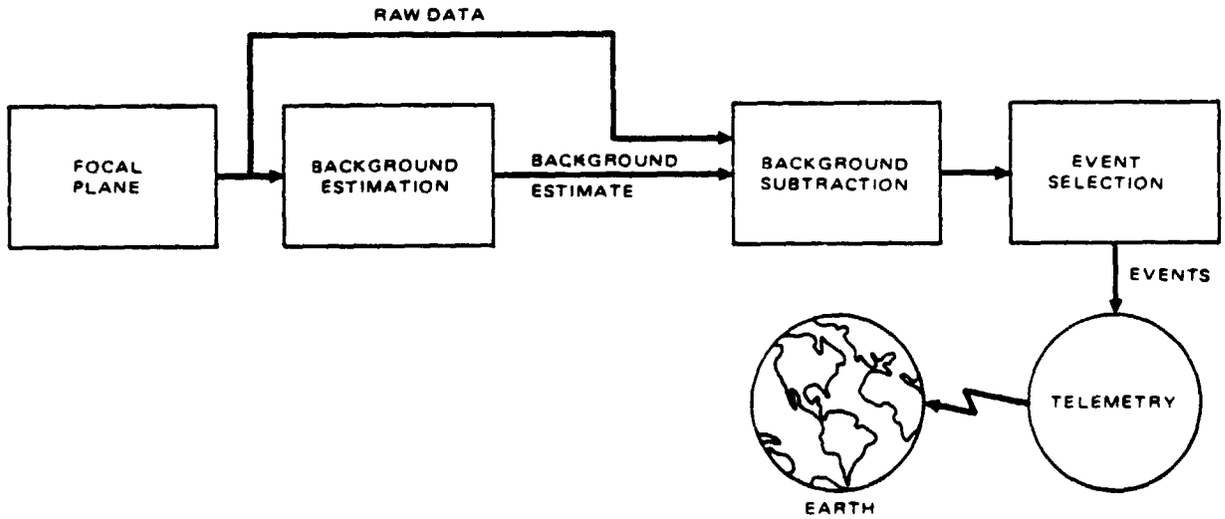


Figure 3-1. On-board data processing tasks.

The first task, estimating the background, was found to be the most challenging because solar radiation reflected from cloud tops may be one hundred times larger than the smallest signal of interest. Ideally the background estimate should be obtained through the same sensor element (focal plane pixel) that collects the data to avoid the need to calibrate all 400,000 sensor elements to within 1 percent. This implies using the time history of each pixel intensity to form a background estimate unique to that pixel. The problem then becomes one of preventing a large lightning event from increasing the background estimate so that smaller subsequent events are measured incorrectly or lost completely. Proposed solutions to the background estimation problem are discussed in Section 3.2.

Given that good background estimates have been found, they are then simply subtracted from the raw data to obtain signal estimates for each pixel. This process is straightforward, the only difficulties being the high data rates involved (400,000 pixels x 1 sample/msec = 400 million samples per second) and the large range of data values (five orders of magnitude).

The resulting signal estimates are thresholded to determine probable lightning events which are then selected and queued for transmission to earth. The first decision that must be made with regard to implementing the on-board data processing tasks is when to convert analog data to digital form. The data originate in analog form from the focal plane and it is possible theoretically to perform all data processing in analog form even through the data transmission link. This extreme approach would eliminate the need for any analog to digital conversion circuitry on-board.

On the other hand, digital processing offers potentially greater accuracy, guaranteed precision, and broader functional capabilities. Since digital processing becomes more attractive as data rates decrease, and since digital pulse code modulation is the preferred telemetry technique, it is apparent that near-focal-plane processing may be done in analog, the data converted at some point, and the remainder of processing done digitally.

Figure 3-2 shows that postponing analog-to-digital conversion until after the lightning events have been selected reduces the converter power requirements by a factor of ten. This estimate is based on our survey of analog to digital

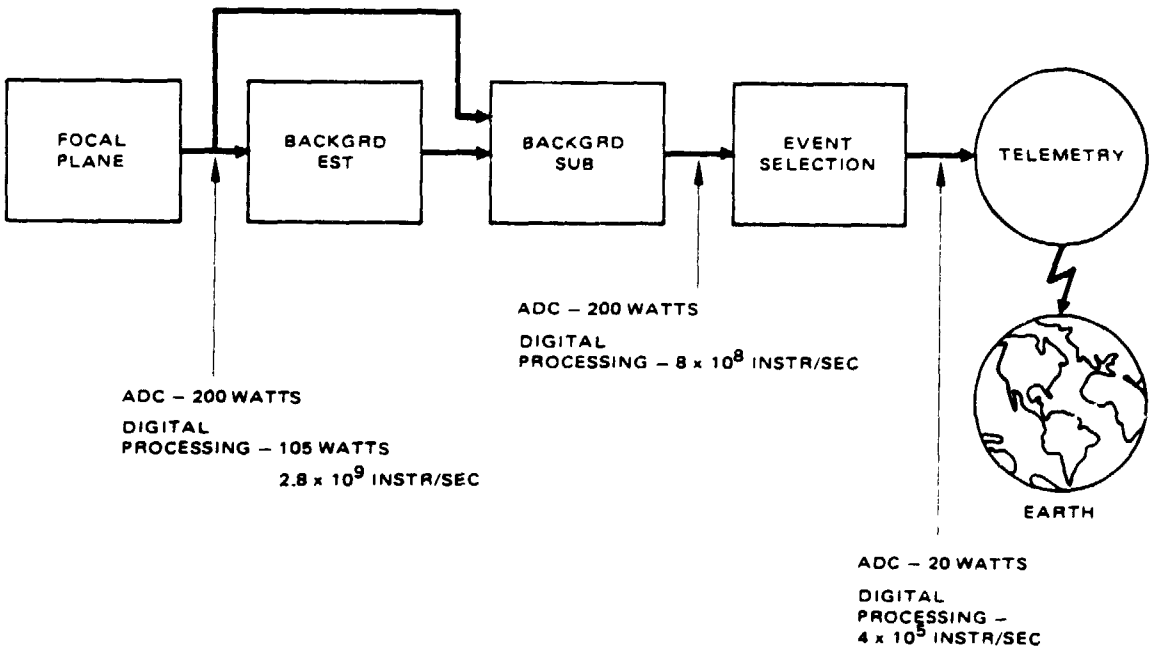


Figure 3-2. Data rates involved at each stage where encoding might be located.

conversion technology discussed in Section 3.4. Power reduction is valuable, not only for minimizing the on-board processor's burden on the spacecraft, but also in removing a tough constraint on the A/D converter design which could add significant cost to the detailed design and implementation phases of the lightning sensor/mapper.

The following three sections discuss trade-offs and implementation of each of the processing tasks listed in Figure 3-2. The conclusion is that these tasks can be performed effectively using off-the-shelf components in a processor requiring about 94 watts and 0.5 ft^3.

3.2 BACKGROUND ESTIMATION

Several approaches to background estimates were considered. The characteristics of a good background estimation algorithm for the Lightning Mapper application are:

(1) Leakage of lightning energy into the background estimates must be minimized. If a single data sample is used as a background estimate, care must be taken to insure that it does not accidentally contain a lightning event. Overall, the probability of a single data sample containing a lightning event is very small, but since these events are highly correlated in space and time, the usual estimators of background (i.e., recent samples from the same or nearby pixels) may be contaminated. Using a filtered background estimate based on many samples has the potential advantage that infrequent lightning events may be "averaged out". But large lightning events may be a thousand time brighter than the highest background and 10^5 times brighter than the smallest signal of interest. One solution is to take a very large sample average, which might then be too insensitive to spatial or temporal variations in the background. A better approach is to clip the raw data that is used for a background average to some maximum value just higher than the highest expected background; in this case the number of samples used in the average can be reduced by a factor of 1000 while meeting the same leakage requirement.

(2) Uncertainty in the background estimate caused by photon noise will be adjusted by system sizing discussed in Section 1.2. Since photons arrive at each sensor element according to a Poisson process, the number of photons in a single sample may be considered to be normally distributed with a standard deviation equal to the square root of the mean. The relative uncertainty in a single sample background estimate is determined by the sensor aperture since a larger sample mean will have a relatively smaller standard deviation. Figure 3-3 shows the characteristics of the focal plane signals resulting

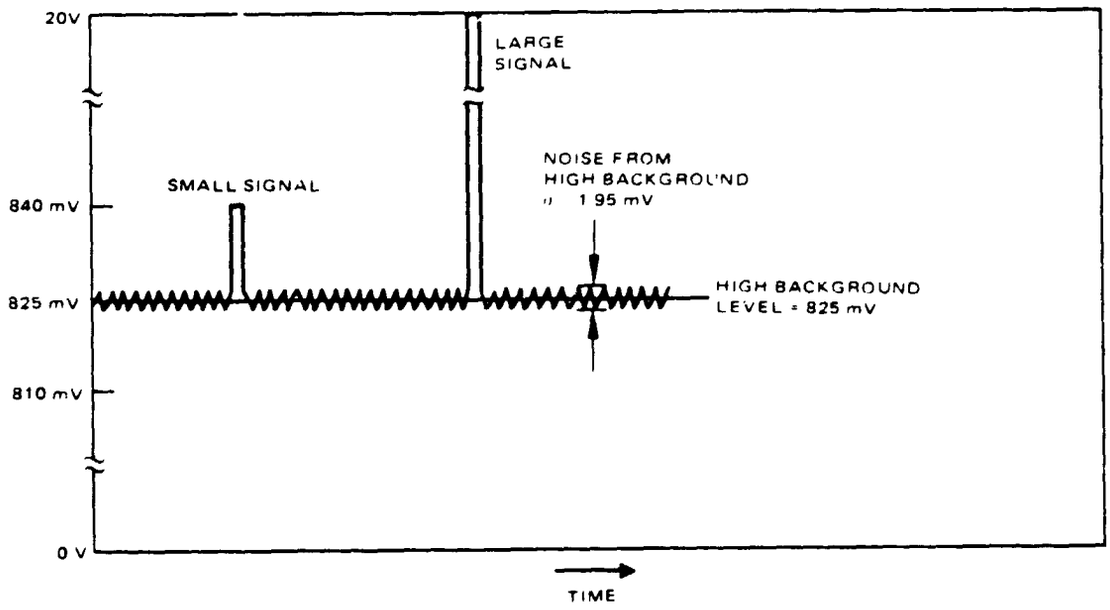


Figure 3-3. Worst-case model for high background and paired lightning events.

from the selected sensor optics and focal plane designs disccused in Section 1. In this figure we see that the uncertainty in a high background estimate is 13 percent of the smallest signal of interest. Since the data containing the signal will also contain the background, the total signal uncertainty is 26 percent in this case.

For the given sensor aperture 26 percent is signal uncertainty only when the background is maximum. At other times signals can be detected down to the read-out noise level. Uncertainty in the background estimate can be reduced by a factor $\sqrt{N}$ by averaging N samples, but uncertainty in the minimum signal with high background can be reduced only by increasing aperture, not by data processing.

Three general approaches to the background estimation problem were considered. The first was spatial averaging. Spatial averaging reduces the undertainty in the background estimate caused by photon noise and it also

introduces error in the estimate caused by different sensor element responsivities and variation in cloud reflectances which may not be random. Spatial averaging is easy to implement in analog circuitry simply by reading the multiplexed focal plane data through an analog low pass filter.

The spatial averaging approach suffers from two difficulties. First 400 or more samples are needed to reduce lightning contamination of the background estimate which requires the background to be fairly uniform over distances of 20 pixels (300 km).

A second and more serious difficulty stems from the need to calibrate the response of the data pixel with respect to the average response of the background pixels. Initial calibration to the required accuracy is very expensive for space qualified equipment but more important is the fact that the stability and non-linearity of detector element responses is too great to meet the less than 1 percent nonuniformity requirement. The dynamic problems can only be corrected with on-board references and a tremendous amount of on-board processing equipment.

The second background estimation technique considered is a modified frame-to-frame subtraction which consists of using each pixel intensity as reported in the previous frame as the present background estimate for that pixel. This algorithm is modified to avoid the obvious problem of occasionally using lightning events as background estimates when two events occur consecutively or one event straddles two sample intervals. This modification can be implemented simply in either analog or digital circuitry by having the event detection signal gate the new image data to the background estimate memory. An analog implementation is shown in Figure 3-4. A difficulty arises from the fact that background subtraction and thresholding must take place within a pixel readout time (1 to 2 msec) in order to switch the correct input to the background estimate memory. The memory requirement of one storage element per pixel to hold background estimates from frame to frame is significant. Analog memory for 40,000 background estimates is estimated to require about 20 watts and 10 in^3, or about 1 watt and 6 in^3 if digital memory is used.

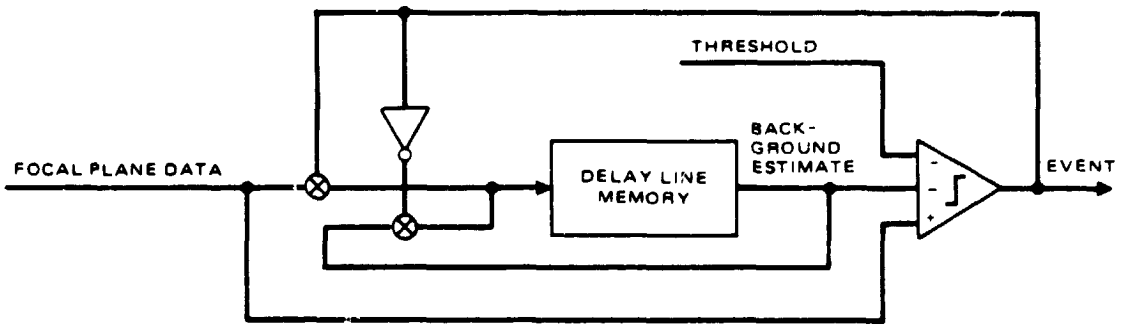


Figure 3-4. Modified frame-to-frame subtraction for analog signals.

Modified frame-to-frame subtraction suffers from the photon noise uncertainty of a single point background estimate. As mentioned above, the standard deviation of the background estimate is about 13% of the lowest signal with the currently proposed optics. A second problem is that consecutive undetected lightning events, each greater that the immediately previous event but with a differential that is less than the threshold, causes a temporary overestimation of the background. This is probably not a serious problem since increases in the background estimate will be temporarily halted by over-threshold events and eliminated completely by any frame in which an event does not occur. Modified frame-to-frame subtraction has the advantages that is very responsive to temporal changes in background (since the estimate is refreshed every few milliseconds), and the detected lightning events do not contaminate the estimate at all.

The third and final approach to background estimation is the time domain filtered estimate. Such a filter must have good high-frequency rejection to avoid lightning event contamination of the background estimate yet not roll off at such a low frequency that the background estimate does not respond to changing background. Multiple filters roll off more sharply than single pole

filters, but each additional pole in the filter transfer function corresponds to an additional element of storage per pixel. Study results reported in more detail below indicate that a single pole filter is adequate if it is preceeded by a clipper to limit input to the background estimator to the range of possible backgrounds.

Figure 3-5 shows a time-domain filter implementation. Multiplexed focal plane signals are fed through an isolation and clipping stage, multiplied by a fractional gain α and added to $(1 - \alpha)$ times the previous background estimate for the same pixel. Analog values for a row of focal plane pixels are stored in a CCD video delay line. These delay lines are commercially available in 768, 850, and 910 elements from Plessey Semiconductors as well as from other manufacturers.

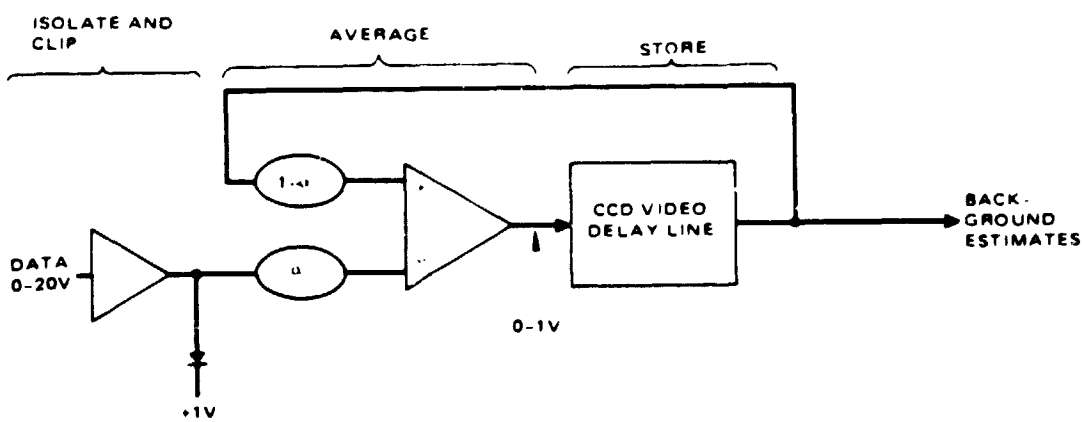


Figure 3-5. Analog signal background estimator.

The filter gain α must be chosen small enough to prevent clipped lightning events from contaminating low background estimates, but high enough to allow the estimate to reflect changes in background quickly. Figure 3-6 shows the effect of event leakage on background estimation for two gain levels. With the worst case of zero background, a lightning event occuring at Frame 1 will cause the background estimate to shoot up to α volts since the event is clipped

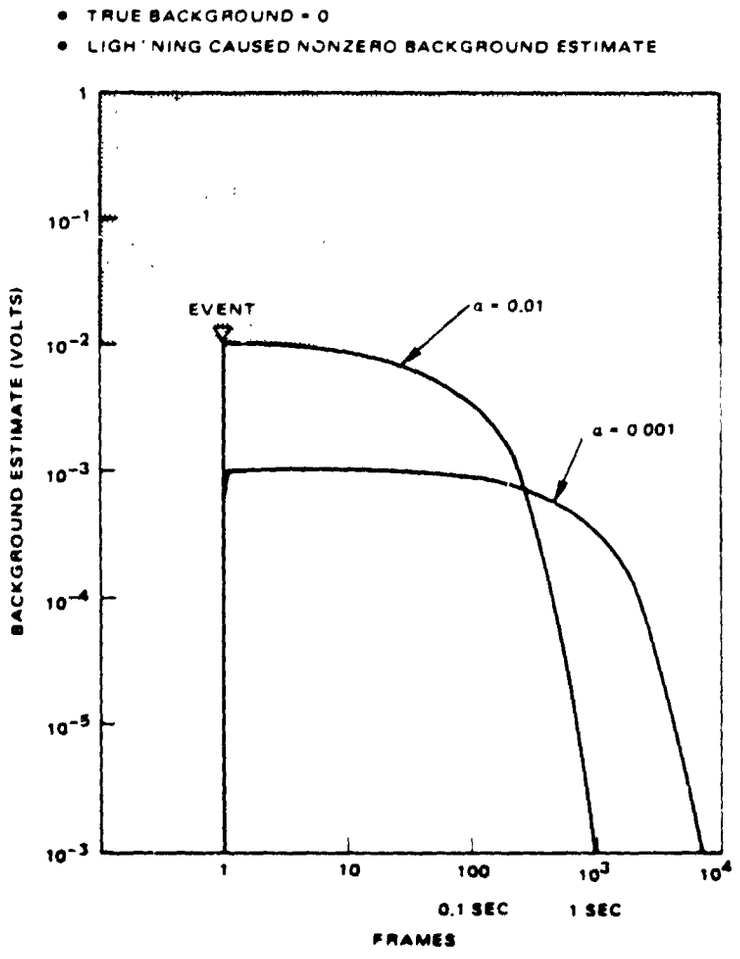


Figure 3-6. Event leakage into background estimate.

to one volt (see Figure 3-5). The background estimate then decays exponentially with time constant $1/\alpha$ frames. Additional events (now shown in Figure 3-6) could add to the erroneous background estimate, possibly causing subsequent pulses in the same stroke to be lost. Choosing $\alpha = 0.001$ keeps the background estimate from getting above the lowest signal of interest, shown as a grey region in Figure 3-6. The decay time of 1 second is short enough that the effects of separate flashes are independent.

Figure 3-7 shows effects of $\alpha = 0.01$ and 0.001 on the signal estimate. A cloud edge moving across the pixel raises the background intensity from 0 volts at Frame 0 to 1 volt at Frame 10^6 (about three hours later). A completely unresponsive background estimator would continue to estimate zero background, causing the signal to be estimated, erroneously as 1 volt. After the signal estimate is above threshold (grey region in Figure 3-7) a steady string of false alarms is generated. For all non-zero gain values, the background estimator essentially does not respond during the first $1/\alpha$ frames of the rise in background. It then begins to track the background with constant lag which gives a constant signal estimate equal to the background rate (e.g., 10^6 volts/frame) divided by α. From Figure 3-7, gains from $\alpha = 0.01$ to 0.001 can be seen to provide sufficient filter response.

3.3 COMPONENTS FOR BACKGROUND SUBTRACTION, THRESHOLDING, AND EVENT SELECTION

Background subtraction and thresholding can be implemented either with analog or digital logic. The analog design can be implemented with off-the-shelf components for a considerable savings in development cost, the penalty being a larger spacecraft burden (size, weight, and power) than with a custom analog integrated circuit approach. The digital design is sufficiently complex that a custom integrated circuit design approach must be taken. The basic building blocks, CMOS SOS gate arrays, are available off-the-shelf so design effort is much reduced; however, the A/D conversion for encoding all of the signals from the FPA would require very advanced designs with an estimated power consumption of about 200 watts. For these reasons the analog implementation was adopted so the encoding could be deferred to a point where signal volume has been reduced.

Again, for completeness, we state the digital processing requirements if one were to elect to use the high power A/D approach. Logic for subtracting two 17-bit numbers (i.e., background and threshold) from a third 17-bit number (i.e., the next sample) would be the equivalent of 500 two-input gates. The total sample rate could be handled by five CMOS-SOS gate array components which would operate with two watts and occupy one cubic inch.

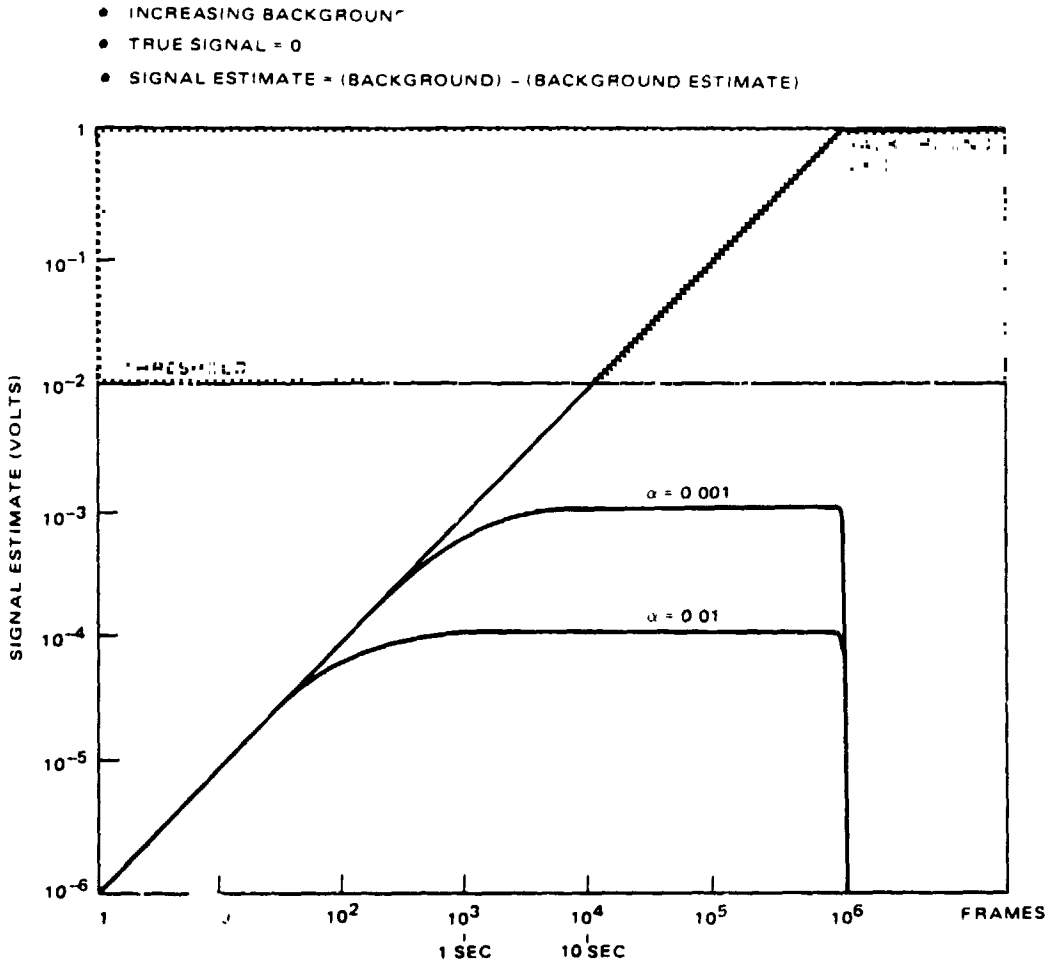


Figure 3-7. Background leakage into signal estimate.

The analog implementation recommended from the study is shown in Figure 3-8 and uses two operational amplifiers for each signal line. The background and thresholding functions for the 324 lines required for the DRO FPA can be handled with circuitry that uses 8 watts and occupies 36 cubic inches.

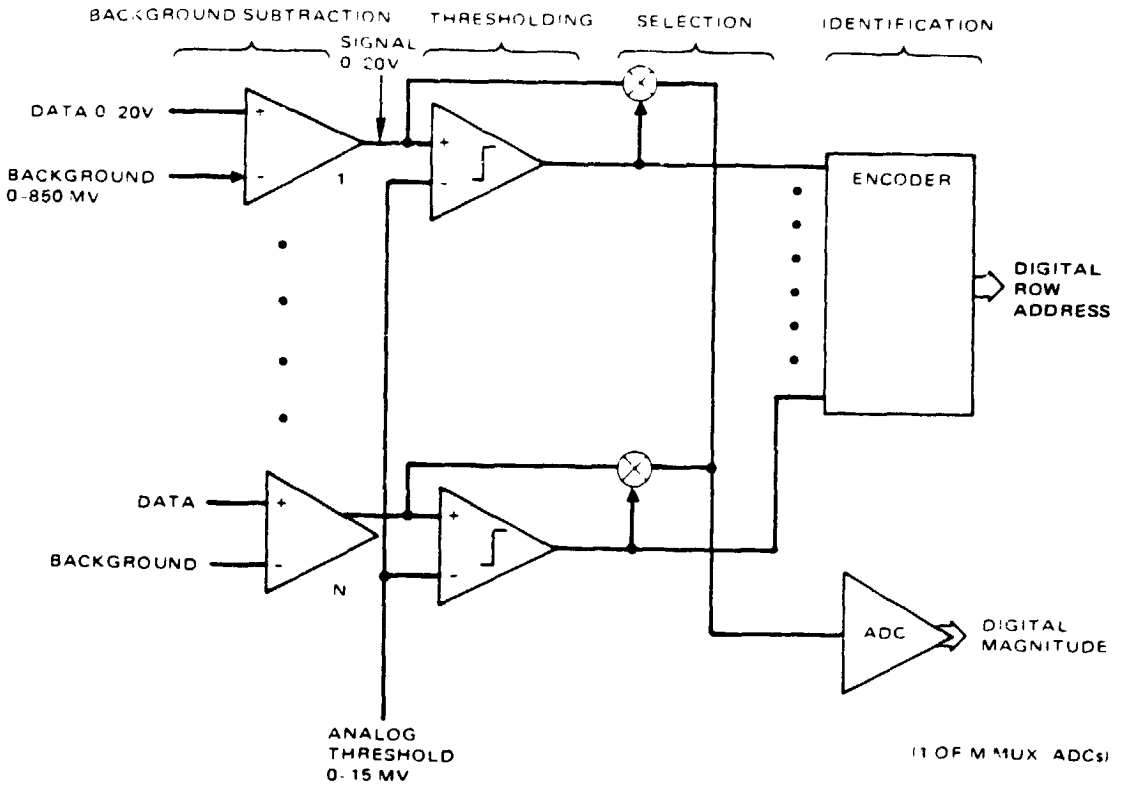


Figure 3-8. Analog implementation of event data selection.

Analog circuitry to select the small number of events from the large amount of signals is also shown in Figure 3-8. A "demand multiplexing" technique allows a threshold exceedance occurring on one of a group of N focal plane signal lines to gate the analog pixel intensity onto a single analog data bus that leads to an A/D converter. The N focal plane lines that share one A/D converter are selected from widely spaced areas of the image plane in order to minimize the probability of two lightning events occurring simultaneously in the same group. A total of M such selection circuits is needed to handle the M-N signal lines from the focal plane.

If two or more events or event and false alarm combinations occur simultaneously, the events will be lost. Figure 3-9 shows the fraction of lightning events lost as a function of false alarm rates and the number of selection

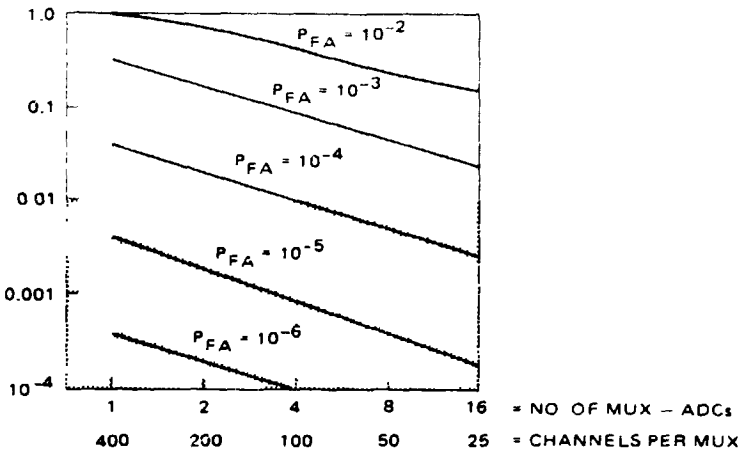


Figure 3-9. Fraction of events lost by competition from false signals.

circuits M. Lost events can be kept below one percent for the combinations that lie in the shaded area. A false alarm rate of 10^{-4} can achieve the one-percent rate event loss with a reasonable number of selection circuits. In the range suggested it is possible to use about 4 to 16 A/D converters that operate at a comfortable rate of a megasample per second.

Table 3-1 shows the fraction of lightning events above 1.17 microjoules per square meter per steradian that will be detected for a range of thresholds. Also shown are the fraction of false alarms, time between false alarms, and output data rate for each threshold setting. The percentage refers to the entire population shown for peak pulse energy/flash in the U-2 data for summer 1982. The same minimum threshold will admit 88 percent of all pulses shown for the same observations. These calculations are based on the system sized to ensure that pulses of 4.72 microjoules per square meter per steradian (minimum specified pulse) will result in S/N of 4 in the presence of the highest background level. Calculations are shown for detector noise only. When events occur in the maximum background situation, the percentage of the peak pulse

Table 3-1. Percent of events detected and false alarm rates versus threshold settings

Threshold, $\mu j/m^2$ sterad (S/N)	Probability of False Alarm	Fraction of Events* Detected	Mean Interarrival Time of False Alarms per Pixel	Telemetry Rate Required, bits/sec
1.165 (1.9)	2.7×10^{-2}	1.00	0.4 seconds	4×10^{10}
2.075 (3.4)	3.0×10^{-4}	0.98	3.3 seconds	5×10^{6}
3.37 (5.5)	3.3×10^{-11}	0.93	1 year	400
4.72* (8.1)	6.4×10^{-16}	0.90	10^{5} years	400

*For total population of peak pulses that exceed 1.165 $\mu j\ m^{-2}$ $sterad^{-1}$

population that is detected will be around 0.95 with the possibility of a kilobit data rate. These threshold levels must be carefully adjusted when throughput levels and population cutoff requirements are known more precisely. Having a variable threshold for day and night settings should also be considered.

3.4 ANALOG-TO-DIGITAL CONVERSION

As mentioned above, A/D conversion may be done either before or after event selection. If placed before event selection, the A/D converter must operate at the focal plane data rate encode with sufficient resolution for further on-board processing. That is, a fixed-point or integer format will greatly simplify design of special purpose digital hardware needed for the remaining on-board processing tasks.

If conversion is done after event selection, A/D converter design is simplified in two ways. Firs the required overall capacity is much smaller. The approach discussed in the previous section used 4-16 A/D converters, each operating at the focal plane channel data rate of 0.5-3 megasamples per second. The output data rate is less that 50 megasamples per second which represents a significant reduction of the total focal plane data rate of 400 megasamples per second. The second advantage for A/D conversion after event selection is that no more arithmetic processing need be done on-board. Thus the data can be transformed or reformatted in any way that will simplify the converter design, consistent with preserving the desired lightning for ground processing.

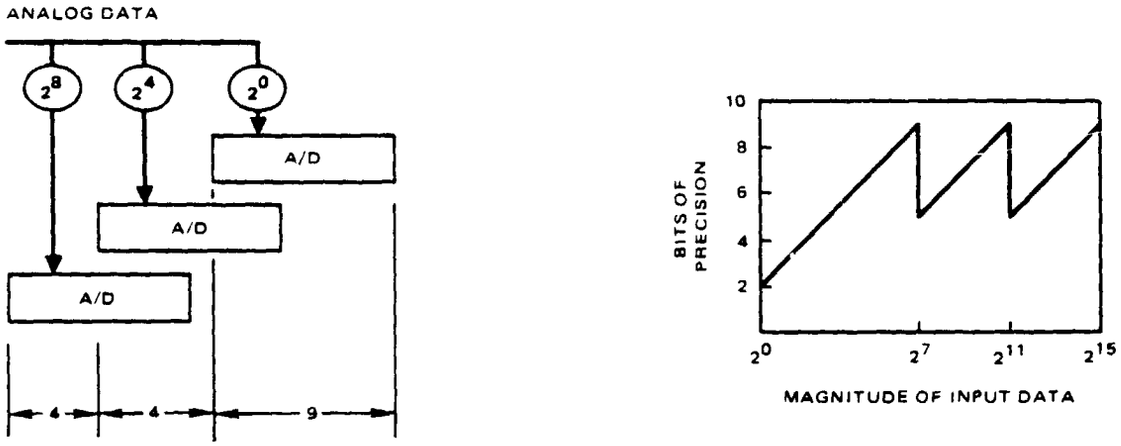
We first consider the most stressing design which is a raw data rate converter that produces a fixed-point digital stream for an input signal range of 10^4. Fixed point 17 bit output per sample provides two decimal-digit accuracy at the low end of the signal range. For larger signals the lower bits would not have meaning.

Table 3-2 summarizes representative A/D converters that are commercially available. Neither of the two types shown - flash converters nor successive approximation converters - meets the 17-bit resolution alone; however, several can be used in parallel in a piecewise linear technique that will handle larger dynamic ranges. Figure 3-10 shows how three 9-bit or two 10-bit converters may be combined to provide 17-bit fixed point conversion. A single analog input is amplified with different gain levels and applied to the multiple converters simultaneously. The largest A/D ouput which is not saturated is selected. The three-converter option accuracy ranges from 6 to 9 bits and requires 150 watts while the two-converter option yields 4 to 10 bit precision and requires 320 watts.

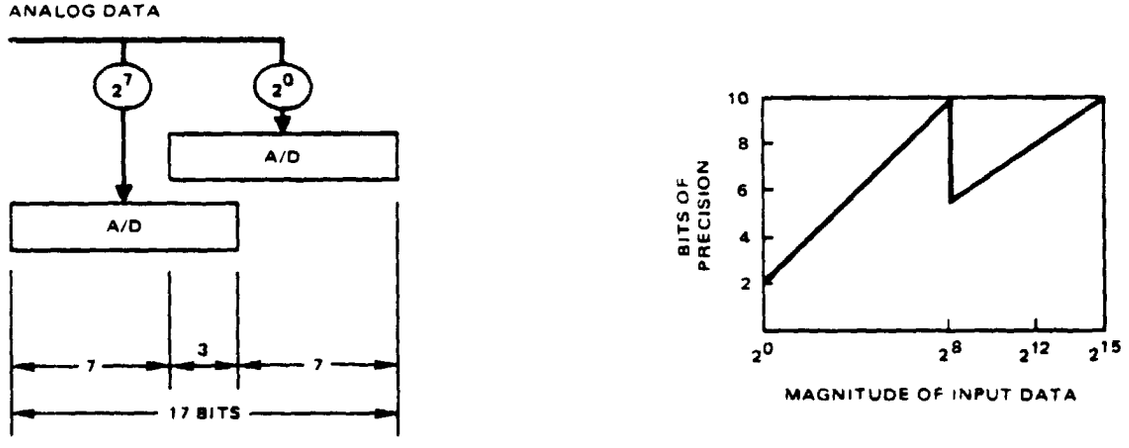
These levels of power were considered exhorbitant in view of satellite resources so that it was decided to select events before A/D conversion and operate at the reduced rate of 0.5 to 3 MHz per channel. Also, since the need for arithmetic processing has been eliminated, it is possible to use logarithmic encoding which will permit 12 bits instead of 17 bits per sample. This format allows a 7-bit mantissa for relative accuracy of two decimal digits, with a 5-bit exponent for a range of 2^{31}.

Table 3-2. Analog-to-digital converters

Model Number	F = Flash SA = Successive Approximation	Consumption, watts	Sample Rate, MHz	Resolution	Digital Data Rate per Watt
RCA CA3300D	F	0.315	15	6 bits	300 Mbits
TRW 1019J	F	2.5	20	9	72
AD HAS1002	SA	1.8	0.59	10	3.2
AD HAS0802	SA	1.8	0.67	8	3.0
AD HAS1202	SA	1.8	0.36	12	2.4
AD HAS578T	SA	1.2	0.2	12	2.0



a. Using three 9-bit converters



b. Using two 10-bit converters

Figure 3-10. Piecewise linear conversion.

Log encoding of the multiplexed analog signal may require a custom-designed nonlinear amplifier since a technology survey has not found any off-the-shelf log amplifier having sufficient bandwidth. Such a design is judged to involve low risk and moderate cost.

It is believed that suitable 12-bit successive approximation A/D converters can be purchased off-the-shelf in the 1985 era. The present models operate at 200 kbps and it is predicted that rates are advancing so rapidly that adequate devices will soon be available. Alternatively, analog sample and hold circuits can be used in parallel.

It is estimated that the arrangement shown in Figure 3-9 requires less than 50 watts for two converter modules using off-the-shelf A/D converters.

3.5 BUFFERING AND TELEMETRY

Lightning data must be assembled in a queue and buffered for telemetry. Queueing is needed to smooth the events that may occur in bursts of 6 million per second into a data rate which is consistent with the longer term average rates of a few thousands of events per minute.

Figure 3-11 shows a block diagram in which each event level is associated with a column address derived by counting the focal plane read-out clock cycles, and a row address obtained by encoding the binary value threshold exceedance lines. Each item is clocked into a first in first out (FIFO) memory when a non-zero row address appears on the encoder output. Data are clocked out when polled by the telemetry controller. FIFO's such as the Fairchild 3341 are commercially available and typically provide queueing for 64 4-bit words. When averaged, it is expected that events will occur no more often than every two seconds per multiplexer; therefore, 64 words will suffice.

3.6 PROCESSING OF DUAL-GAIN FOCAL PLANE DATA

To minimize the effects of analog and quantization noise upon the on-board data processing, a dual-gain amplifier circuit within each focal plane cell has been developed. Small data values, up to about 130 times the maximum expected background, are amplified with a fixed high gain. Larger data values

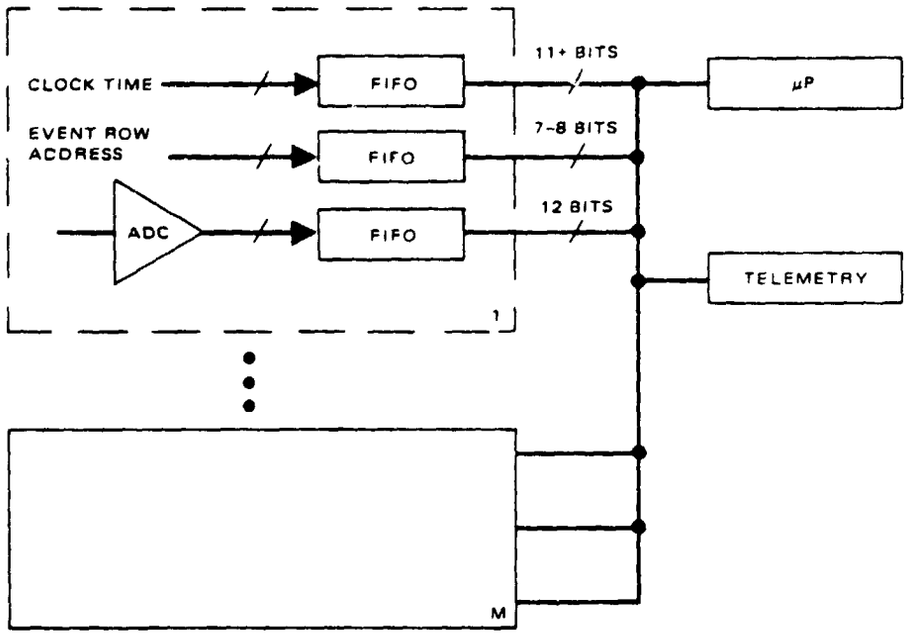


Figure 3-11. Analog-to-digital conversion and transmission.

are amplified with a second, fixed, low gain. Letting the high and low gains be a_1 and a_2, respectively, the amplifier transfer function is

$$y = \begin{cases} a_1 x & \text{for } x < b \\ a_2(x-b) + a_1 b & x \geq b \end{cases}$$

where x is the diode detector element signal and x = b is the point at which gains are switched. It will be shown here that background subtraction and estimation can be carried out in the same manner for the case in which the signal remains only in the first gain level and also for the case in which the signal spans both gain regions. If x_o is the pixel intensity for only a high background and x_1 is an added amount of signal caused by lightning, then $a_1 x_o$ represents the background estimate and $a_1(x_o + x_1)$ represents the combined pixel level for $x_o + x_1 < b$. Subtracting the background,

$$a_1(x_o + x_1) - a_1x_o = a_1x_1 = y,$$

which can be inverted by $1/a_1$ to obtain x_1 when $y \leq a_1b$. Consider a second lightning signal x_2 that is so large that the combination $x_2 + x_o > b$. The output for the large level signal is, $a_1b + a_2(x_o + x_2 - b)$, so that subtracting the previous background estimate of a_1x_o yields, $a_1b + a_2(x_o + x_2 - b) - a_1x_o$. If it can be determined that this signal has been large enough to occupy both levels of gain then the ground processor can subtract a_1b, multiply by $1/a_2$ and add b to yield,

$$x_2 \qquad + x_o\,(1 - a_1/a_2)$$

true signal error signal

In the proposed design, b is selected to be 2×10^7 carriers, which is much greater than the maximum error signal $(1-a_1/a_2)\,x_o = 8 \times 10^5$ carriers. This gives a relative signal error of 0.04 or less. Events greater than the breakpoint b will have correspondingly lower error signals, and events that are smaller than b will be interpreted correctly.

☆U.S. GOVERNMENT PRINTING OFFICE 1983—746-070/82