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# MODULAR APPROACH FOR SATELLITE COMMUNICATION GROUND TERMINALS

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## Abstract

The trend in satellite communications is toward completely digital, time division multiple acess (TDMA) systems with uplink and downlink data rates dictated by the type of service offered. Trunking terminals will operate in the 550 MBPS (megabit per second) region uplink and downlink, whereas customer premise service (CPS) terminals will operate in the 25 to 100 MBPS region uplink and in the 200 MBPS region downlink. Additional criteria for the ground terminals will be to maintain clock synchronization with the system and burst time integrity to within a matter of nanoseconds, to process required orderwire information, to provide adaptive data scrambling, and to compensate for variations in the user input-output data rates, and for changes in range in the satellite communication links resulting from satellite perturbations in orbit. To achieve the required adaptability of a ground terminal to the above mentioned variables, programmable building blocks can be developed that will meet all of these requirements. Application of this concept to the modulators and demodulators is not considered here. To maintain system synchronization, i.e., all bursted data arriving at the satellite within assigned TDMA windows, ground terminal transmit data rates and burst timing must be maintained within tight tolerances. With a programmable synchronizer as the heart of the ground terminal timing generation, variable data rates and burst timing tolerances are achievable. In essence, the unit inputs microprocessor generated timing words and outputs discrete timing pulses. Conversely, discrete event pulses are inputted and timing words are outputted to the controlling microprocessor. All timing loops are closed in the microprocessor. Additional housekeeping tasks, such as data scrambling and descrambling control words, orderwire generation and decoding, user interface control and ground terminal status, etc., are maintained under microprocessor control.

## Modular Approach for Satellite Communications Ground Terminals

### Summary

The trend in satellite communications is toward completely digital, Time Division Multiple Access (TDMA) systems with uplink and downlink data rates dictated by the type of service offered. Trunking terminals will operate in the 550 MBPS (megabits per second) region uplink and downlink, where as Customer Premise Service (CPS) terminals will operate in the 25 to 100 MBPS region uplink and in the 200 MBPS region downlink.

In spite of the variability of the data rates the ground terminal must maintain system clock synchronization and burst time integrity to within of nanoseconds, process required orderwire information, provide adaptive data scrambling - descrambling, and compensate for variables in the user input-output data rates and for changes in range in the satellite communication link resulting from satellite perturbations in orbit.

To achieve the required adaptability of the ground terminal to the above mentioned variables, basic building blocks, some being programmable, can be developed. It should be noted at this point that the limits of the ground terminal presented in this paper are from the user input-output expansion/compression type buffers to the high speed serial data stream(s) to and from the modems.

The modular approach is possible because of the similarity in the various memory units and the timing and synchronization that must be maintained relative to a high speed clock that is independent of slower burst rates.

The above mentioned data rates for the various types of service, trunking, and CPS, have resulted from NASA's Lewis Research Center, Communications Division studies on the Advance Communications Technology Satellite activities.

### Basic Ground Rules Covering Terminal Design

The ground terminal design presented in this paper is governed by the following ground rules:

- User input/output data is a continuous serial data stream.
- Parallel data transfers within the terminal are 64 bit words.
- A frame time equals 4096 64 bit words at a serial data clock rate of 275 MBPS (0.232 μs/word) for a trunking terminal.
- CPS terminals operate from a basic clock of 220 MBPS (downlink data rate).
- Forward Error Correction (FEC) is not addressed.
- Approximately 1 millisecond worth of expansion and compression buffering is required for each terrestrial interface channel.

The following list of approximate data rates were assumed as a reasonable design criteria.

- Terrestrial serial I/O rates of approximately 1.5 to 45 MBPS.
- CPS satellite uplink burst rate of 27.5 and 110 MBPS.
- CPS satellite downlink burst rate of 220 MBPS.
- Trunking satellite uplink and downlink burst rates of 550 MBPS. This constitutes two each 275 MBPS channels within the ground terminal on both the transmit and receive sides.

Table 1 illustrates the data rate and timing summary.

### General Design Approach for Modular Construction

The basic ground terminal either being operated as a trunking terminal or a CPS terminal in a TDMA system must perform the following functions:

1. Maintain synchronization with the system to within nanseconds.
2. Transmit bursted data to within a matter of nanoseconds.
3. Compensate for the nonmultiple terrestrial data rates and the satellite link data rates.
4. Have expansion and compression buffering to compensate for satellite orbital perturbations.
5. Process orderwire information.
6. Adaptive data scrambling - descrambling.
7. Monitor terminal status and data memory content levels.

To accomplish items one and two mentioned above and considering the various data rates previously summarized, a timing and control synchronizing subassembly that is programmable will meet the requirements. The unit is essentially a high speed counter with a basic clock rate of either 220 or 275 MHz that accepts precomputed timing words from the terminal's microprocessor, and outputs the necessary timing and control clocks and discretes for terminal control. The counter's content is also strobed at specific event times such as unique word detect, and inputted to the microprocessor for system - terminal synchronization determination and basic clock adjustment.

This programmable timing approach for terminal timing, control and synchronization allows the basic ground terminal to function as a trunking or CPS terminal.

To accomplish items three through seven several differents types of memory units, both in capacity and organization, are required. Examination of Table 1 illustrated the various capacities and speeds where as Fig. 1 illustrates the various memory organizations.

A memory unit can be configured as a two port unit with the basic addressing, control logic and memory organization that can operate either as a FIFO or as a ping pong memory. In addition, the memory unit organization and operation is governed by changes in the mother board or backplane wiring.

Three types of basic memory are required to meet the various terminal requirements.

1. Low speed buffer organized as 128 or 256 words x 64 bits (300 nsec access time).
2. Low speed or medium speed buffer organized as 1024 or 2048 x 64 bits (300 nsec access time) or 2048 or 4096 x 64 bits (70 nsec access time).
3. High speed timing and control memory organized as 128 or 256 x 32 bits (6 nsec access time).

To interface with the outside world, such as, the terrestrial serial data streams on one end and the modems on the other end, serial to parallel and parallel to serial converters have been developed. They operate over the required serial data rates by adjusting an internal timing delay to match the serial data rate. It is understood that these units represent an overkill for the 1.5 and 27.5 MBPS rate. The parallel I/O ports are windowed to allow "asynchronous" data transfers. The parallel to serial converters are capable of initiating a serial data stream to within ±1 bit time at the high speed clock rate.

The last major item required for the ground terminal is a microprocessor that meets the following minimum requirements:

1. Memory referenced instruction execution time of 1 microsecond.
2. Sixteen bit basic word length.
3. Parallel DMA I/O transfer rate of 2 MHz.
4. Parallel Direct I/O transfer rate of 1 MHz.
5. Two real time interrupts.
6. One reasonable speed serial I/O port.

With the above summarized basic subassemblies, a ground terminal can be constructed that will meet either TDMA trunking or CPS operational requirements. Major reconfiguration changes needed to meet different operational requirements might include changes to buffer memory size, memory organization by backplace wiring, and timing generation software.

The following text is a more indepth discussion of the terminal's subassemblies.

## Detailed Description

Along with a more detailed description of the individual subassemblies a summary of the subassembly to subassembly interfacing and an approach to generating the timing software will be presented.

### Timing Control and Synchronization Subassembly

As previously described, the timing, control and synchronization subassembly is basically a high speed counter with a basic clock rate of either 275 MHz or 220 MHz. Precomputed timing words are compared with the counter contents, and when a match is achieved a discrete output is set or reset depending on the associated function code accompaning the timing word. On the other hand a discrete timing event can be determined by strobing the counter content and inputting the timing word into the microprocessor for subsequent processing.

The counter circuit is a four bit ring counter which drives a 16 bit synchronous counter for a total of an 18 bit timing word. The ring counter is required to compensate for the propagation delay inherent in the 16 bit counter section when operating above 200 MHz. Eighteen bits at 275 MHz rate yields a 950 μs frame time (ground rules assumption).

In addition to the counter circuit, the subassembly contains a memory unit organized in two, ping pong, 32 bit by 64 word units expandable to two 128 word units for storing the precomputed timing words. As a word is "executed" the memory read address counter is incremented and the next cell's contents are ready for "execution." The two ping pong memories operate in the same fashion.

Other circuits included are memory for temporarily storing the strobed counter contents, steering and latching logic for the various output discretes, and read and write clock generations for terminal data transfers operating at the parallel data word rates.

The timing word is a 32 bit word which is organized as follows: (Bit 0 is the LSB).

Timing Required to ±1 Bit Time (Critical Timing).

Bit 0 to Bit 17 - Precision Timing Word.
Bit 18 to Bit 23 - (B23 = 1) 5 Bit Function Code.
Bit 24 to Bit 31 - Memory Cell Location.

Timing Required to ±4 Bit Times.

Bit 0 to Bit 15 - Relaxed Timing Requirement Word.
Bit 16 to Bit 23 - (B23 = 0) 7 Bit Function Code.
Bit 24 to Bit 31 - Memory Cell Location.

Below is a partial list of discrete generating function code for various subsystem control.

Terminal transmit related codes:

- 18 Bit - Start Parallel to Serial Converter.
- 16 Bit - Start Preamble - Orderwire Enable Envelope.
- 16 Bit - Stop Preamble - Orderwire Read Enable Envelope.
- 16 Bit - Start Burst Buffer Read Enable Envelope.
- 16 Bit - Clock User Read Enable Control Memory.
- *. 10 Bits - Word Read Clock.
- *. 10 Bits - Word Write Clock.

Terminal receive related codes:

- 18 Bits - Start Demod Unique Word Window.
- 18 Bits - Stop Demod Unique Word Window.
- 16 Bits - Start Orderwire Write Enable Envelope.
- 16 Bits - Stop Orderwire Write Enable Envelope.
- 16 Bits - Start Deburst Buffer Write Enable Envelope.
- *. 10 Bits - Word Read Clock.
- *. 10 Bits - Word Write Clock Envelope.

Terminal control miscellaneous codes:

- 18 Bits - Reset Counter.
- 16 Bits - Master Reset to Terminal Subsystem.
- 16 Bits - Generate Interrupt A - Input Timing Words.
- 16 Bits - Generate Interrupt B - Output Timing Words.
- 18 Bits - Switch Timing Word Memories.
- Don't Care - Zeros in the Function Field = NO - OP.

*k : Transmit and receive word clocks are 50 percent duty cycle and phased such that synchronous data transfer reads and writes do not occur simultaneously.

The timing word input memory (counter content strobed) is configured as a FIFO and its content are imputted into the microprocessor under program control.

All word transfers between the timing and control synchronizer and the microprocessor are via the Direct I/O port in order that the ground terminal initialization process is simplified. The DIO transfer is slower than via DMA but when considering the reassignment update rate, the I/O rate does not present a problem.

Memory Units Organization

Memory units of various capacities and organizations are used for expansion and compression buffers in user interfacing, burst and deburst buffers, timing and control buffers, preamble and orderwire buffers and scrambler/descrambler word buffers. Table 1 gives a rough estimate of memory size and required access time for memories handling the various data rates.

The memories are configured as a two port unit with latches on both the read and write data ports and addressing logic that allows for either FIFO or direct storage operation (RAM). In addition, ping pong operation and word widths are controlled by back plane wiring changes.

As stated in the terminals initial summary the memories are broken into three basic categories.

The low speed buffer organization is either a 128 or 256 words by 64 bit unit with a chip access time of 300 nsec. The basic chip organization is 128 x 8.

The low and medium speed buffer organization is either a 1024 or 2048 word x 64 bit unit with a chip access time of 300 nsec. The basic chip organization is 1024 x 8. Also the same card can be organized as medium speed unit with 2048 or 4096 word x 64 bit unit with a chip access time of 70 nsec. The benefit here is the 1024 x 8 and the 2048 x 8 chips are pin compatiable.

The high speed memory used in the timing and control have the required 6 nsec access time with the chip organization of 64 x 4 bits. The memory size is 128 or 256 x 32 bits.

The addressing and control logic is the same for all memories in as much as they are capable of operating in the various configuration. Included in the address and control logic are:

- A read or write requires the read or write clock falling edge and the required enable envelope signal.
- Read/write logic that arbitrates simultaneously occurring read and write commands.
- A read address counter that increments after a read operation. The read address counter contents can be read and a read address can be externally inputted under memory unit external control.
- A write address counter that corresponds in function to the read address counter.
- A memory content counter that is a write increment-read decrement, with its present value accessable under external control.
- A master reset that clears all counters.
- Certain internal control lines are brought out to the connector so the memory organization can be changed to meet the necessary requirements by changing the back plane wiring.

Figure 2 shows a block diagram of the basic memory unit with labeled control signals. As seen in the block diagram the addressing I/O port, is operated via the microprocessor direct I/O port and

during normal terminal operation the addressing data obtained is a low speed monitor function. On the transmit side, the user interface FIFO's read enable envelope control is generated by the user interface control memory. The same is true for the receive side user FIFO's write enable envelope control. The user interface control memory is loaded via the microprocessor DMA output buffer and its incrementing is controlled via the programmable synchronizer subassembly.

## Parallel to Serial and Serial to Parallel Converters

The parallel to serial and serial to parallel converters have been developed and operate over the required serial data rates. An internal time delay needs to be adjusted to match the desired serial data rate. The units are "asynchronous" in as much as the parallel input or output data is windowed for 1/2 the parallel transfer rate word time.

The parallel to serial converter that interfaces with the modulator is able to start outputting a serial data stream to within ±1 clock cycle of the high speed clock. It is independent of all other data rates and only requires that the converter has been loaded with a 64 bit word prior to being started. Subsequent parallel transfer are required during the input window, thus, the unit allows for tight uplink timing control.

The serial to parallel converter is self synchronizing with the demodulator unique word detect pulse and upon counting 64 bits, initiates a parallel word ready output flag. The parallel word must be picked up within the allotted window time.

For slower serial data rates of 1.5 and 27.5 MBPS, the high speed converters are not cost effective. The same basic design should be inplemented with slower and less expensive components to be cost effective.

## Controlling Microprocoessor Considerations

For microprocessor requirements stated in the initial summary the units are essentially an off the self item from several vendors. Figure 3 shows a block diagram illustrating the I/O arrangement.

What is of interest here is the layout of the memory associated with the DMA data transfers and an example of how to program the timing and control synchronizer.

Referring to Fig. 3, the subassemblies serviced via the DMA I/O interface on the output side are:

- Transmit side orderwire memory.
- The scrambler and descramble memories.
- The user interface ontrol memory.

On the input side is the receive orderwire memory.

The main memory organization for output words is such that even locations contain subassembly addressing data, where as, the odd locations contain data. This requirement is evident because the output buss to the subassemblies is 32 bits wide, 16 bits of address and 16 bits of data. To load a 64 bit word into the user subassembly, the address data is encoded with the subassembly address, the cell address and which 16 bits of the 64 bit word.

The unloading of the DMA output buffer and the inputting of data from the receive side orderwire buffer into the DMA input buffer are controlled by the timing and control synchronizer. The 64 bit input word is unloaded 16 bits at a time and stored in the DMA input buffer. Under interrupt control the orderwire data is transferred to or from main memory.

Programming the timing and control synchronizer, is best discussed using an example. Assume steady state operation. The following is an example of the generation of a new receive time assignment.

| Bit | Word | Function | Comment |
|---|---|---|---|
| 0 | 0 | Start | Demod window |
| 30 | 0 | Stop | Demod window |
| 0 | 1 | Start | Descrambler Envelope (Example assumes 1 word descrambler) |
| 12 | 1 | Start | Orderwire Enable Envelope (Expecting 4 OW Words) |
| 60 | 4 | Stop | Order Wire Envelope |
| 4 | 5 | Start | Deburst Buffer Write Enable (Expecting 4 Data Words) |
| 60 | 8 | Stop | Deburst Buffer Write Enable |

This type of coding would continue, governing a total frame period of operation.

Also included in the coding is any activities required for control of the transmit side, such as, transferring the terrestrial input data in tne proper burst order to the uplink burst memory, generating the required timing interrupts, etc. It is understood that the microprocessor would do the required program assembling and eventually the code generation would become automatic in response to orderwire information transmitted and received.

## Conclusions

Presented in the previous discussion is an approach to ground terminal design and construction. The approach utilizes a programmable timing generations concept, a flexible memory unit design and variable speed serial-parallel/parallel-serial converters that will meet the various ground terminal operational requirements. The requirements include CPS and trunking terminals, and could be expanded to include Demand Assignment Multiple Access (DAMA) and Network Control.

Other design approaches examined used single function, fixed timing subassemblies that are dedicated to executing a specific function. The utilization of multifunction units is more cost effective that fixed function subassembly design when considering production and maintainability.

The most significant feature of this design approach is the flexibility.

TABLE 1

| Serial rate, MBPS | Bit time, nsec | Word time, μs | Words per frame (minimum memory size) |
|---|---|---|---|
| 1.5 | 666. | 42.7 | 23 |
| 27.5 | 36. | 2.3 | 408 |
| 45. | 22. | 1.4 | 816 |
| 110. | 9.1 | .58 | 1638 |
| 220. | 4.5 | .29 | 3275 |
| 275. | 3.6 | .23 | 4096 |

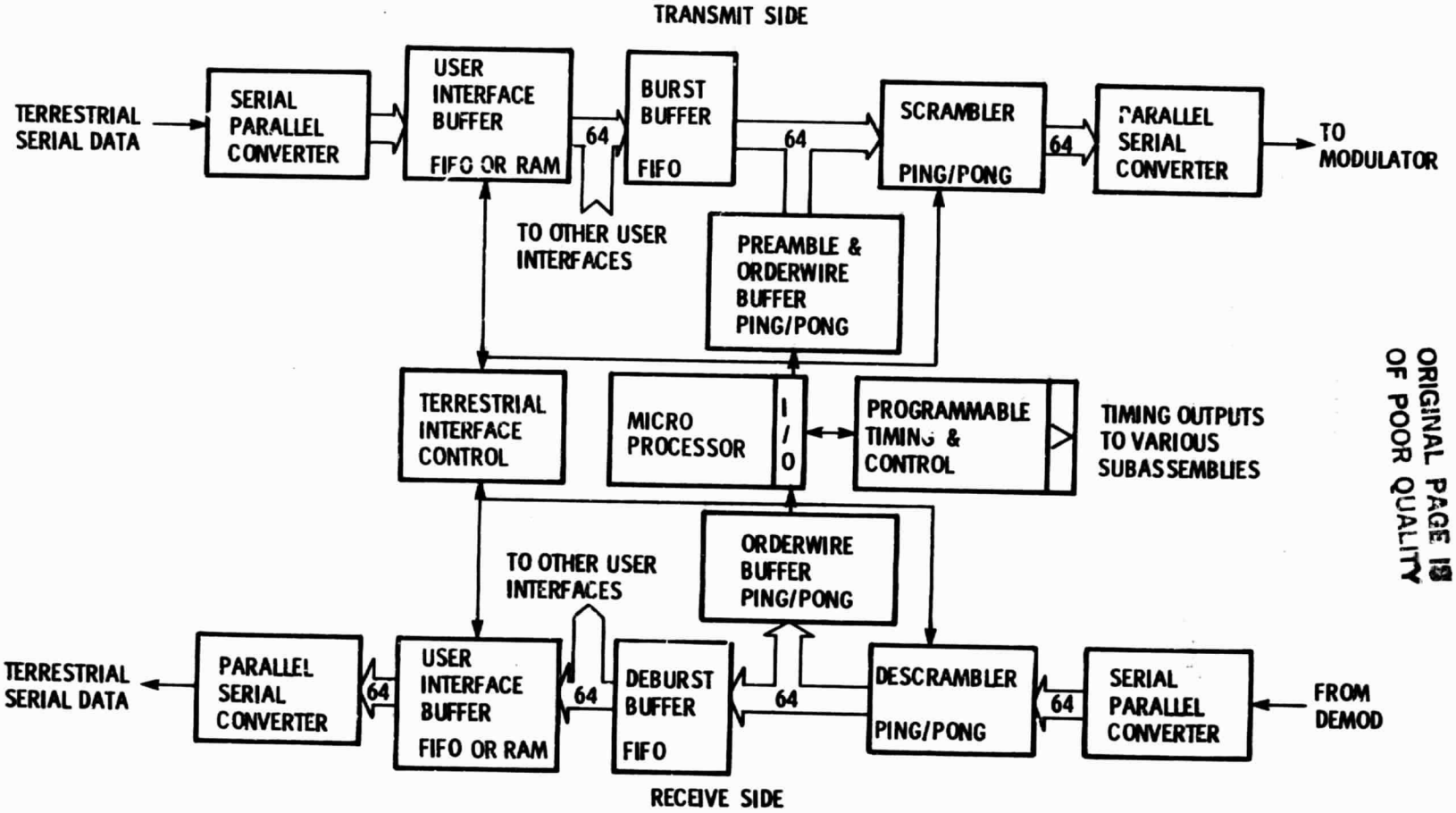


Figure 1. - Basic ground terminal block diagram.

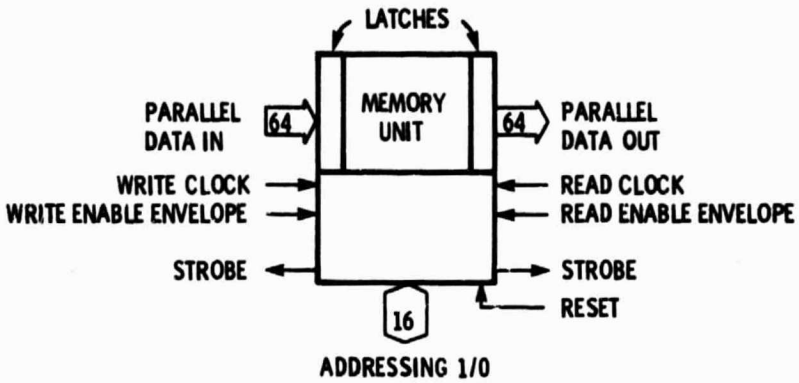


Figure 2. - Memory unit organization.

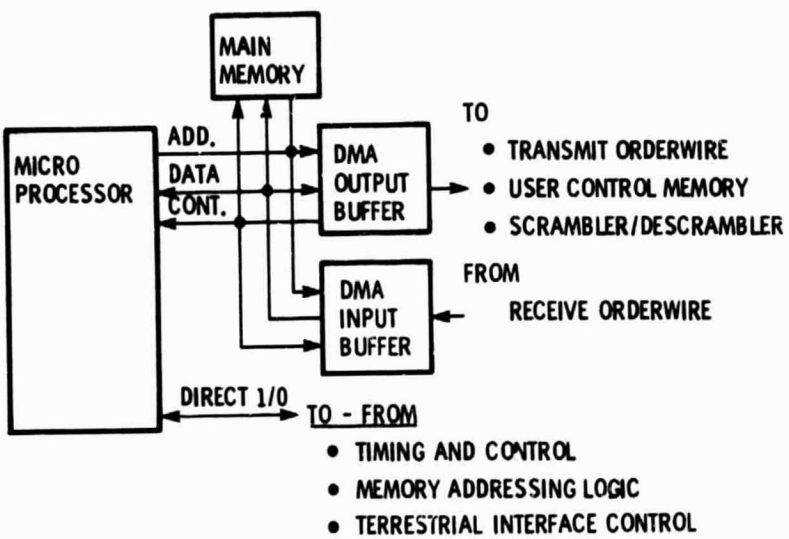


Figure 3. - Micro processor 1/0 organization.