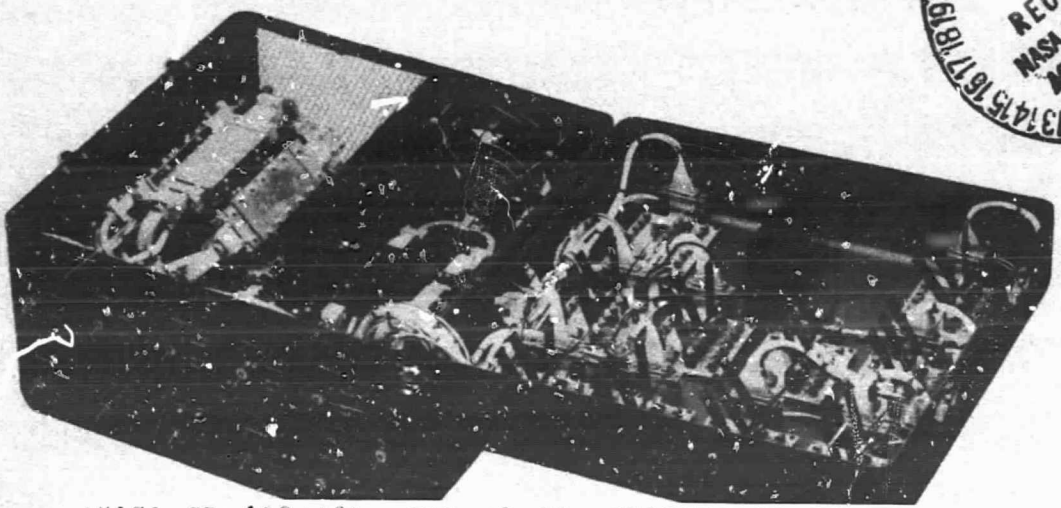
20 GHz Spacecraft FET Solid State Transmitter



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Final Report

No. CR 168240

July 1983
Contract No. NAS3-22503

Prepared for

National Aeronautics
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TRW Electronic
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TRW

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ABSTRACT

This final report details the engineering development of a solid state transmitter amplifier operating in the 20 GHz frequency band using GaAs field effect transistors (FETs). The major efforts include GaAs FET device development, single-ended amplifier stage, balanced amplifier stage, cascaded stage and radial combiner designs, and amplifier integration and test.

The result of this effort is the development of a multistage GaAs FET amplifier capable of 8.2 W CW output over the 17.9 to 19.1 GHz frequency band. The GaAs FET devices developed under this program represent state-of-the-art FET power device technology. Further device improvements are necessary to increase the bandwidth to 2.5 GHz, improve dc-to-RF efficiency, and increase power capability at the device level. Higher power devices will simplify the amplifier combining scheme, reducing the size and weight of the overall amplifier.

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1. INTRODUCTION

This report covers the work performed by TRW on the program entitled, "30/20 GHz Spacecraft GaAs FET Solid State Transmitter", under Contract No. NAS3-22503 sponsored by National Aeronautics and Space Administration, Lewis Research Center, Cleveland, OH 44135.

The objectives of this program are:

- Based on an assessment of the technology available by 1982, a 20 GHz GaAs transmitter shall be designed to provide 6 to 7.5 watts (CW) over the frequency band of 17.7 to 20.2 GHz
- 20 GHz GaAs FET shall be designed and developed, and device packaging and characterization shall be performed
- A proof-of-concept (POC) model of the space-qualifiable 20 GHz GaAs FET transmitter shall be developed and tested
- A reliability analysis on the POC model shall be performed
- A product assurance program shall be effected during fabrication of the POC model
- A technology assessment shall be made to establish the available device performance abilities as well as the growth prospects of GaAs FET devices.

The POC model design goals are shown in Table 1-1 below.

Table 1-1. Design Goals for POC Model 20 GHz Transmitter Amplifier

Frequency Band	17.7 to 20.2 GHz
Output Power	6 to 7.5 Watts
RF Gain at P_o	30 dB minimum
Gain Flatness	±0.5 dB total
Gain Variation	0.15 dB per MHz
Input/Output VSWR	<1.4
Noise Figure	<25 dB
Third Order IMD	<20 dBc at P_o
	<30 dBc at $P_o/2$
Group Delay Variation	<0.5 nsec per 0.5 GHz
AM/PM Conversion	<3° per dB above P_o
	2° per dB below P_o
Phase Linearity	<5 PK-PK deviation
Harmonics	<30 dBc at P_o
Spurious Response	<60 dBc at P_o
RF Efficiency	>13 percent
Projected Life	>10 years
Overdrive Limit	>24 mW
Temperature Range	0 to 75°C

2. SYSTEM DESCRIPTION

2.1 SYSTEM OVERVIEW

To meet POC model technical requirements and other criteria, (e.g., module commonality to minimize component parts, device power handling levels to maximize efficiency and minimize the number of devices to reduce cost) the following system considerations have been incorporated in the design of the POC model.

2.1.1 System Block Diagram

The 20 GHz transmitter system block diagram is shown in Figure 2-1. The amplifiers shown in the shaded box all have the same performance specification requirements and therefore can all be satisfied with one design. The major elements to be developed are:

- Driver Module (unshaded amplifier)
- Power Module (shaded amplifier)
- 8-Way Radial Splitter/Combiner

2.1.2 Driver Module and Power Module

It is desirable to design the driver modules and the power modules using the same mechanical configuration to reduce the POC model cost. The basic block diagrams for both driver and power modules are shown in Figure 2-2. Since the modules are interconnected with waveguides, input and output waveguide-to-microstrip transitions are required. To utilize the intrinsic input/output isolation of the FETs, two single-ended amplifier stages are cascaded as a unit. However, to achieve the gain flatness of the POC model, additional isolation is required between cascaded stages. To minimize the required number of transistors and Lange couplers, the single-ended configuration at the input of the modules is employed. Although the block diagrams for the driver and power modules are the same, the device types used differ depending on the operating power levels required of the FETs; thus, 1/4 W, 1/2 W, and 1 W devices are used as require.

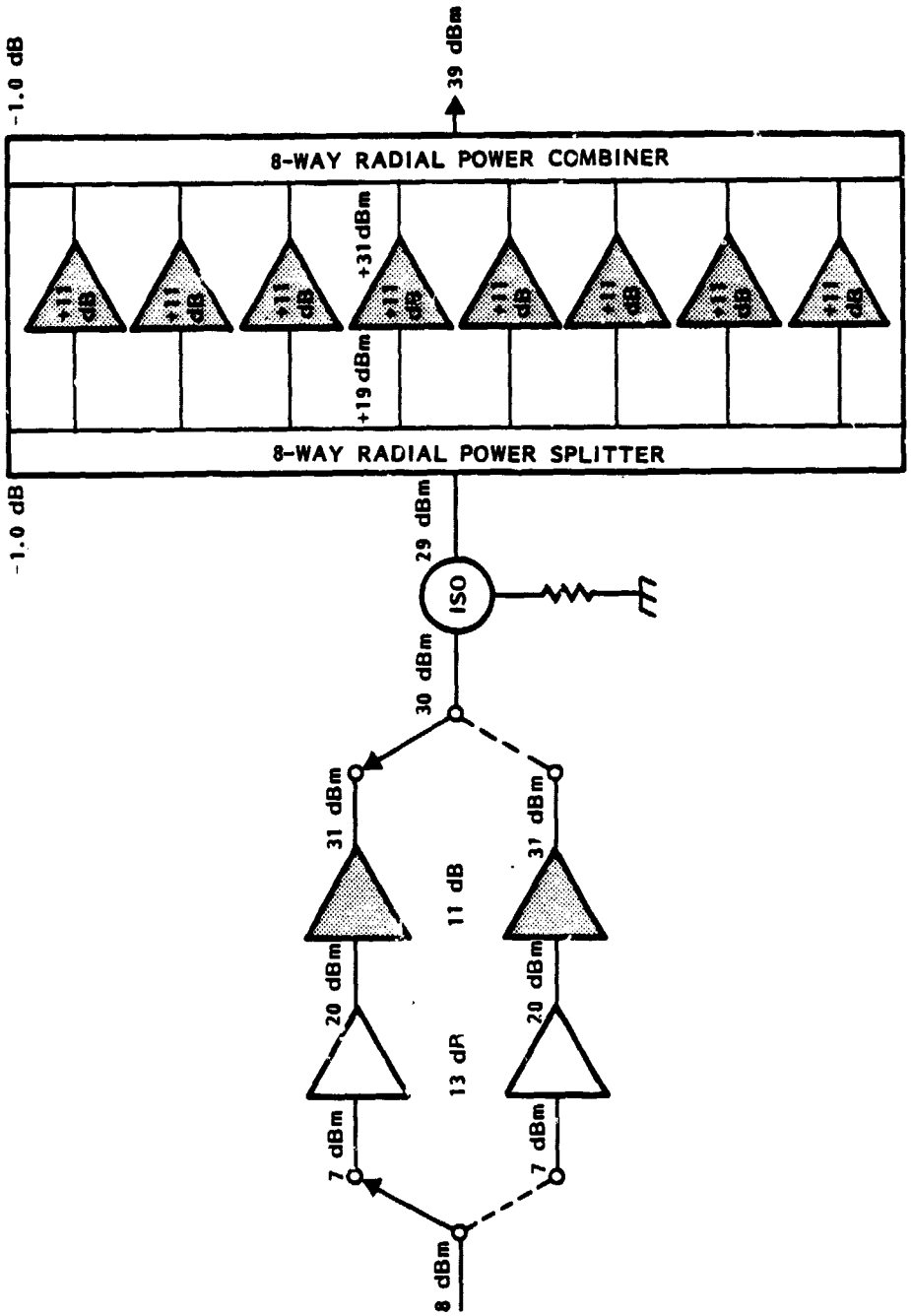


Figure 2-1. System Block Diagram of 20 GHz Transmitter

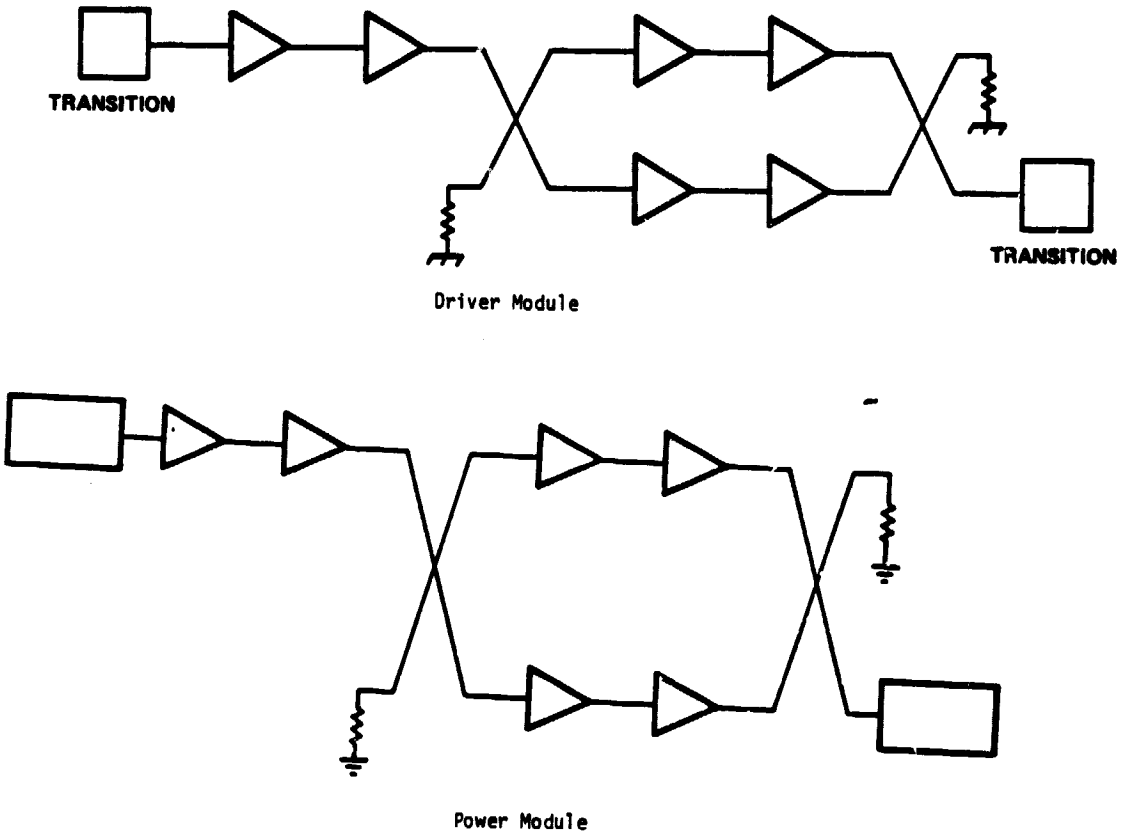


Figure 2-2. Block Diagram of Driver and Power Modules

2.2 GAIN BUDGET

The gain budget for the POC model is shown in Figure 2-1. The gain budgets for the driver module and the power module are shown in Figures 2-3 and 2-4, respectively.

2.3 CRITICAL CIRCUIT ELEMENTS

Based on the system described, the critical circuit elements to be developed are:

- Waveguide-to-microstrip transition
- Lange coupler
- Single-ended stage amplifiers for various power levels, as required
- Cascaded single-ended stages for various power levels, as required
- Balanced cascaded stages for various power levels, as required
- Driver module
- Power module
- Eight-way radial splitter/combiner
- Eight-way combined amplifier
- Regulators and other safety features
- POC model
- FET devices for various power levels, as required

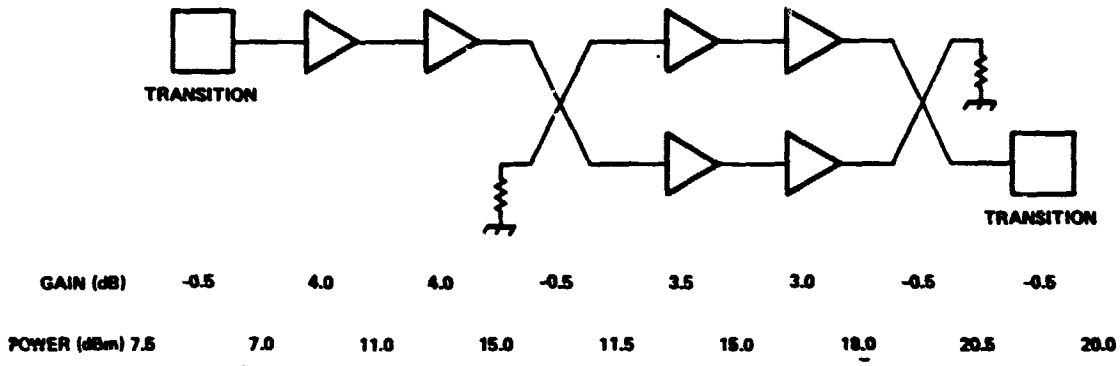


Figure 2-3. Power Gain Budget of Driver Amplifier

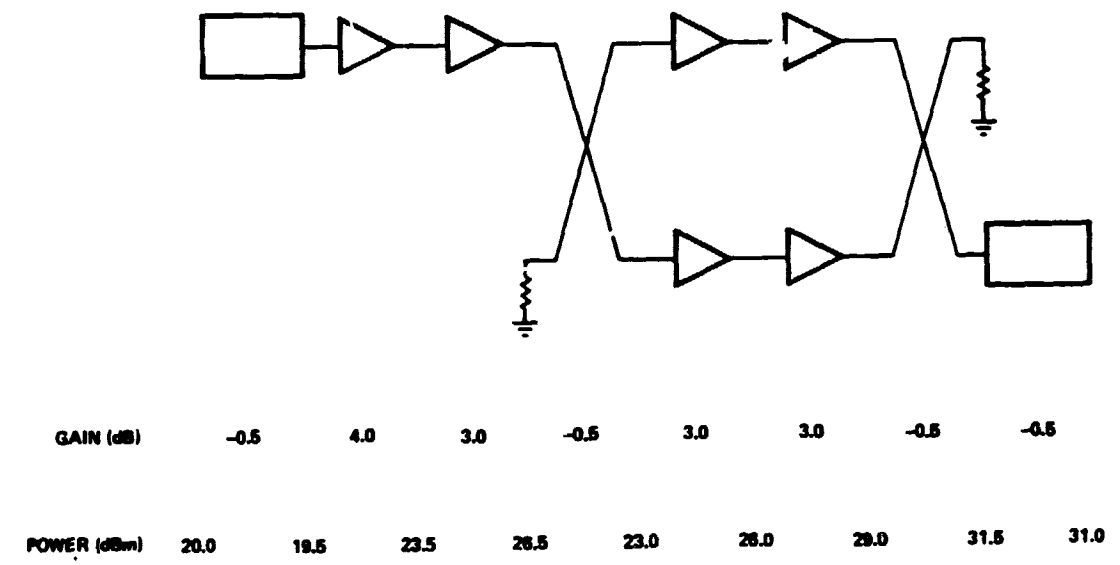


Figure 2-4. Power Gain Budget of Power Amplifier

3. NASA 20 GHZ POWER GaAs FET DEVELOPMENT

3.1 INTRODUCTION

This section of the final report describes the work carried out by Raytheon Special Microwave Devices Operation (SMDO) to develop power FETs for the NASA 30/20 GHz spacecraft GaAs FET solid state transmitter. The performance capability specification at 20 GHz for the developmental devices is reproduced from the Statement of Work in Table 3-1. Since K-band test equipment was not expected to become available at Raytheon within the time scale of the contract, it was agreed that device characterization would be performed in Ku band. Deliverable devices would originate from wafers which exceed the minimum performance specifications of Table 3-1 at 18 GHz. Toward the end of the program, however, a K-band test bench was constructed and some characterization was performed at 20 GHz. Details of rf characterization procedures are given in Section 3.4

Table 3-1. Performance Specifications of Developmental Devices at 20 GHz

DEVICE TYPE	1/4 W		1/2 W		1 W	
RF PARAMETERS	MIN	GOAL	MIN	GOAL	MIN	GOAL
Power Output (W)	0.25	0.25	0.5	0.5	0.8	1.0
Gain (dB)	4.0	6.0	4.0	6.0	4.0	5.0
Power Added Efficiency (%)	20	25	18	25	13	20

3.2 DESIGN CONSIDERATIONS

The approach to device design followed in this development has been to utilize as much as possible the general configurations and fabrication technologies already well-established at Raytheon while investigating the special requirements for high frequency performance. A fundamental requirement for high power device is a high power-per-unit-gate-width figure of merit together with a useful associated gain of at least 4 dB. Power-per-unit-gate-width is determined essentially by the maximum voltage and current (per-unit-gate-width) swings which can be achieved at the device output terminals. The former is limited by source-drain and gate-drain and gate-drain breakdown phenomena, while the latter is dependent on the active channel thickness and carrier concentration. Unfortunately, the material and channel geometry requirements are not compatible, and factors which increase open-channel current, such as high-carrier concentrations and large-channel thickness, may also decrease breakdown. In order to achieve high gain, the device must have a high transconductance as well as low gate-source capacitance. These also are strongly dependent on carrier concentration and not mutually compatible. In choosing the optimum material parameters, therefore, a number of conflicting requirements must be met, and the choice is often largely empirical. In this development, experience with low frequency devices has served as a starting point, and material parameters have been varied to establish the optimum values at Ku-K band. In particular, somewhat higher carrier concentration material was investigated; the goal was to increase the transconductance maintaining high breakdown voltage by paying careful attention to the channel geometry. Low parasitic source and drain resistances are necessary for high gain, and these were minimized by utilizing a recessed gate structure and surface n+ layers for low contact resistance. The parasitic resistances were further reduced in these devices by continuing the n+ layer to the edge of the gate recess. The carrier concentration profile of a typical wafer utilized in this program is shown in Figure 3-1, which illustrates the n+ surface, the n-type active layer, and the sharp transition to the high purity buffer region. The buffer layer is included to isolate the active region from the impure semi-insulating substrate material.

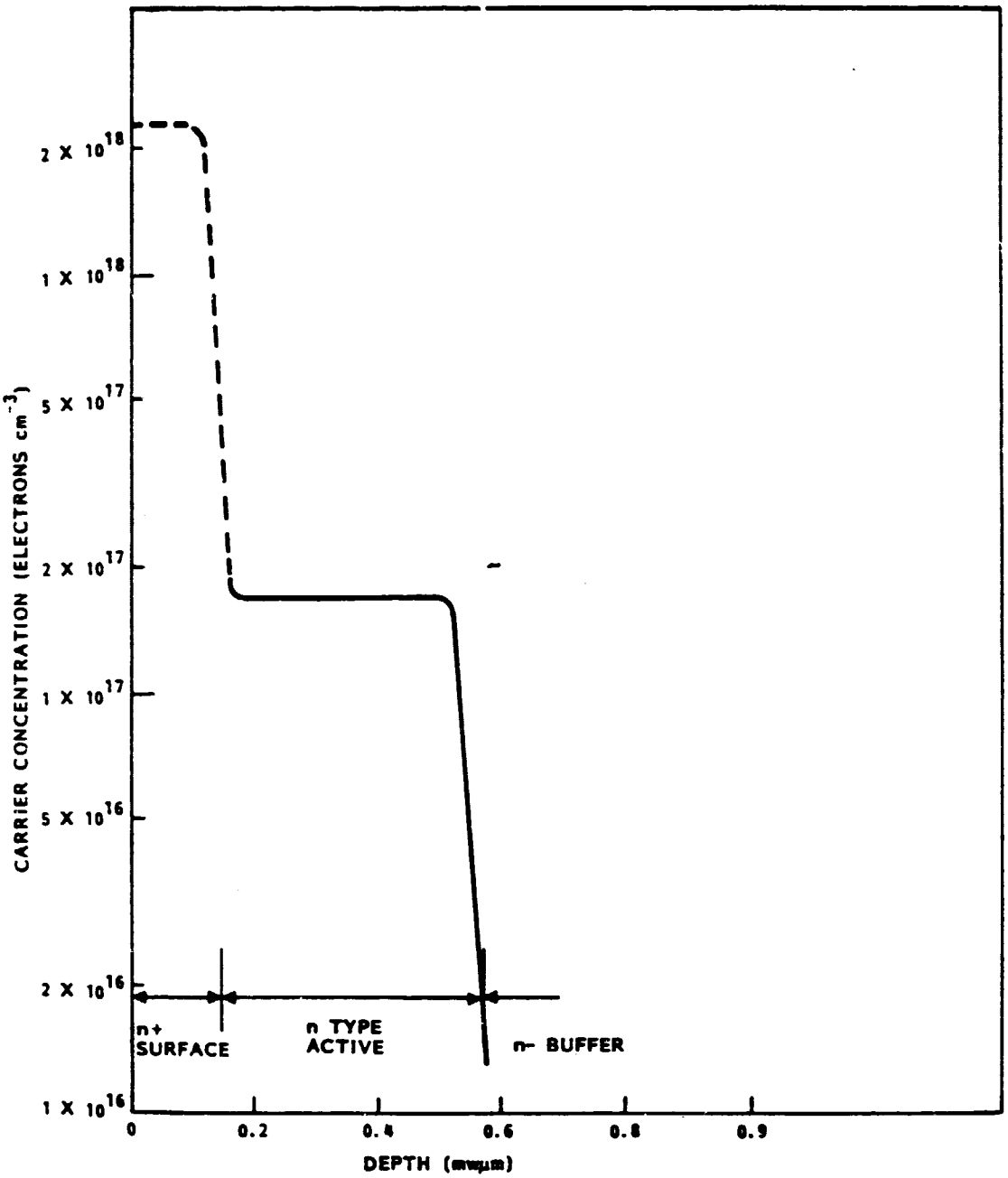


Figure 3-1. Carrier Concentration Profile of Ku-K Band Power FET Wafer

Gate length is a vital parameter for high frequency FET performance. It is generally assumed that this should be as short as possible to minimize gate capacitance and transmit time effects. The latter become extremely important at Ku-k band frequencies where it is generally considered that a 0.5 micron gate must be utilized rather than 1 micron, which has become standard at X-band. This principle was adhered to throughout this program, and devices were fabricated using mask sets with nominally 0.5 micron gate length. In producing gates by contact photolithography, the necessary compromise with fabrication yield was also recognized. The value achieved on most wafers was probably close to 0.7 microns. It is planned to produce gates by direct writing electron-beam lithography in the future, which has the capability of giving a high yield of true 0.5 micron (or less) geometries.

In order to achieve a large output current swing for high power devices, a number of basic gate width units must be connected in parallel to give a large total gate width. Design of power, as opposed to small signal devices, is largely concerned with the way this combining is carried out. Following the basic design philosophy, a conventional interdigitated geometry was adopted in this program together with the well-proven Raytheon via-hole fabrication process which has given excellent performance at X-band frequencies. Where large, total gate-width devices are concerned the interdigitated geometry has the advantage over the multifeed "pie" gate structure of giving a considerable more compact chip, which is believed to be an important factor affecting high frequency performance. The via-hole structure gives extremely low, common source inductance which is a critical parasitic parameter affecting gain and additionally ensuring that inductance is uniformly distributed along the chip. Distributed effects of this type are thought to be very important for high frequency operations, although there is little published theoretical or experimental documentation on the topic. An additional parameter believed to strongly influence high frequency operation is the width of any single-gate finger. Attenuation of the input signal as it propagates along the gate is an important loss mechanism. Although this loss is minimized by using a high conductivity gate metallization (Al) and making the film thickness as great as possible, it remains uncertain how large a unit-width can be tolerated at

any particular frequency. For any particular total gate-width, a tradeoff situation exists between deleterious distributed effects resulting from large numbers of gate units and the resistive losses resulting from large gate-width units. An additional important consideration is the impedance matching characteristics and bandwidth capability of the different configurations. The optimum total gate-width necessary to meet a particular performance specification is clearly dependent on the attainable power-per-unit-gate-width figure of merit which a priori is unknown for a new device structure. Furthermore, it is usual to split the total gate-width for a particular chip into a number of independent single cells to maximize the yield by allowing a number of different power specifications to be met by a single chip-type.

To address the above design unknowns, this development program was based on two-mask sets giving various combinations of unit-gate-width and total gate width as indicated in Table 3-2. Two chip types of 50 and 100 micron unit-gate-widths are included on each mask set. The chips are comprised of two independent cells, but the mask sets differ in the number of gate units carried by each cell. Thus, a total of six different total gate-widths are available for investigation, depending on whether one or two cells are utilized. In particular, a total gate-width of 1.2 mm for the 862 device and 0.8 mm for the 872 device is achieved with either 50 or 100 micron unit-gate-width, thus allowing a direct comparison of the alternative configurations from a single wafer. Estimated power output capabilities based on a conservative figure of merit of 0.5 W/mm are included in the table.

Fabrication of devices by via-hole technology has two additional important advantages over alternative methods. First, the necessarily thin (1.5) GaAs substrate and plated heat sink gives extremely low thermal impedance. The resultant low device operating temperature not only improves power performance, but also has important consequences for long term reliability. Secondly, the via-hole structure gives a completely visible chip surface which allows a detailed inspection for quality control purposes in contrast to competing low inductance technologies (such as air bridge source interconnects and flip-chip mounting) which obscure the active areas of the device.

Table 3-2. 862 and 872 Device Types

MASK SET	862				872			
N° OF CELLS PER CHIP	2				2			
N° OF GATE UNITS PER CELL	12				8			
UNIT GATE WIDTH (μ m)	50		100		50		100	
N° OF CELLS UTILIZED	1	2	1	2	1	2	1	2
TOTAL GATE WIDTH (mm)	0.6	1.2	1.2	2.4	0.4	0.8	0.8	1.6
ESTIMATED OUTPUT POWER AT 0.5 Wmm^{-1} (W)	0.3	0.6	0.6	1.2	0.2	0.4	0.4	0.8

3.3 FABRICATION TECHNOLOGY

The epitaxial GaAs utilized in this program was grown on semi-insulating Cr-doped substrates by chemical vapor deposition using the Ga, AsCl, H system with S as a donor impurity. A typical carrier concentration profile as determined by the capacitance-voltage method is shown in Figure 3-1. Active layer carrier concentrations covered the range 7 X 10^{16} to 2 X 10^{17} electrons/cm^3 with n+ levels in excess of 10^{18}. Active layer thickness before recessing the gate was typically 0.25 to 0.45 microns and n+ thickness was usually 0.2 microns. Processed material was grown at Raytheon Research division on substrates approximately 1-inch square. The new material growth facility at SMDO Northborough is capable of producing 3-inch diameter epitaxial wafers. Wafers were selected on the basis of carrier density profile, surface morphology, and flatness for FET fabrication. The latter criteria were extremely important for high-yield definition of submicron gates.

The steps in device fabrication are outlined in the flow chart of Figure 3-2 and described in greater detail below.

1) The active device areas are isolated by a combination of shallow mesa etching and oxygen ion-implantation. The avoidance of large mesa step aids in subsequent delineation of submicron gates.

2) Source and drain ohmic contacts and gate bond pad areas are defined in positive photoresist. The multilayer Ni/Au/Ge contact is deposited by electron-beam evaporation, defined by photoresist

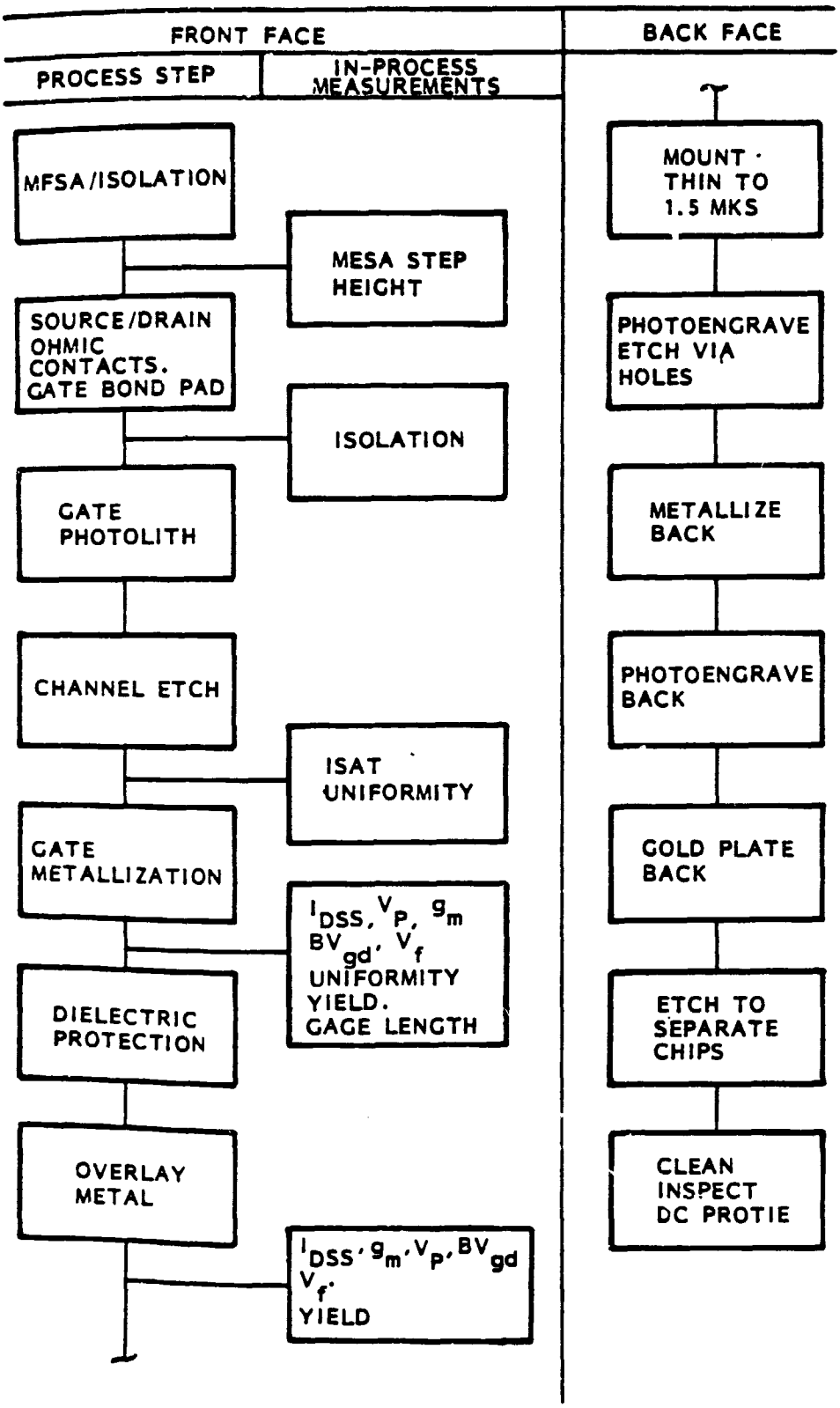


Figure 3-2. Process Flow Chart

lift-off and finally alloyed to produce low resistance ohmic contacts. At this stage the isolation between adjacent active areas is checked and an assessment of contact resistance made.

3) Delineation of the gate pattern in positive photoresist is carried out. By contact printing using 0.5 micron masks and a high precision Karl Zeiss submicron aligner. Eventually this step will be performed by direct-writing electron-beam lithography. This is the most critical part of the process and is the major factor determining the final yield of the wafer. Usually a compromise judgment between yield and gate length must be made at this stage.

4) The channel region, as defined by the gate photoresist, is etched to recess the gate and thereby set the source-drain saturation current I_{sat} which determines I_{dss} of the final device.

5) The aluminum gate metal is evaporated by electron-beam to a thickness of about 0.7 microns and defined by photoresist lift-off. Good adhesion of the aluminum film is essential to ensure a high gate yield at this part of the process. At this stage the dc characteristics of the transitors can be measured on a probe station and an estimate of uniformity and yield made. Measurement of gate length can also be made in a scanning electron microscope. Optical measurement of gate length can usually only establish whether it is less than 1 micron.

6) A dielectric layer of SiOx is applied over the wafer, leaving windows over the bond pad areas. Its purpose is to provide scratch protection for the delicate active areas of the device. the SiOx deposited over the gate acts as a lens and greatly magnifies the appearance of the gate length. Once deposited, therefore, the SiOx precludes any meaningful measurement of gate length.

7) The final step in front face processing is application of a second layer metallization of Ti/Pt/Au over the bond pad window areas to improve bondability. The overlay metal also forms a lateral connection between the Al gates and the Au based gate bond pads, the Pt layer acting as a barrier to the interaction of Au with Al, which can cause void formation in the gate stripes and is a potential reliability hazard. Following final metallization, a full assessment of the dc characteristics and appraisal of the probable yield is carried out. Any wafers which are unsatisfactory in these respects are rejected at this stage to avoid spending unnecessary effort on back face processing.

8) Back face processing commences with mounting the wafer face on an accurately parallel alumina disc and thinning to 1 to 1.5 mils by lapping and etching.

9) Photoresist is applied to the back face, and the via-hole mask is aligned to the source pad by infrared alignment.

10) Via-holes are etched completely through to the source pad areas and the photoresist is removed.

11) A Cr/Au film is evaporated over the back face such that the thin metal film extends into the via-holes.

12) A second photoengraving operation defines areas over the individual device chips to be gold plated.

13) the wafer is gold plated to produce the integral heat sinks.

14) Photoresist is removed and the chips are separated by etching through the GaAs from the back.

15) The chips are finally removed from the alumina disk, cleaned, inspected and sorted prior to dc probing.

A schematic cross section of a completed device is shown in Figure 3-3.

3.4 DC CHARACTERIZATION

A full dc characterization of the finished FET chips was carried out on a precision probe station using a standard transistor curve tracer. Sample characterization was also carried out at various stages in manufacture as indicated in the previous section. A final characterization of the fully assembled device on its microwave test fixture was completed before commencing RF testing. This final test was usually performed on a curve tracer for rapid assessment, but facilities also existed for a true dc characterization which may differ in detail from the 60 Hz swept characteristics of the curve tracer as a consequence of greater mean heating. The dc parameters measured are listed in Table 3-3 which includes details of the measurement conditions. Since high gain chips had a tendency to oscillate on the probe station at high drain bias, the measurements of I_{dss} and Gm were made close to the knee in the characteristics. The measurement conditions for current in Vp, Vf, BVgd, BVgs should correctly be scaled to total cell gate width to take account of the various device structures. However, the differences in gate width were not sufficiently great to significantly affect the measured parameters, and for simplicity a single set of conditions was used. Chips were selected for assembly on test fixtures or carries based on their dc parameters. Chips mounted on RF test fixtures may be properly terminated and the leads properly screened to prevent oscillation; thus, a greater degree of precision in measurement was

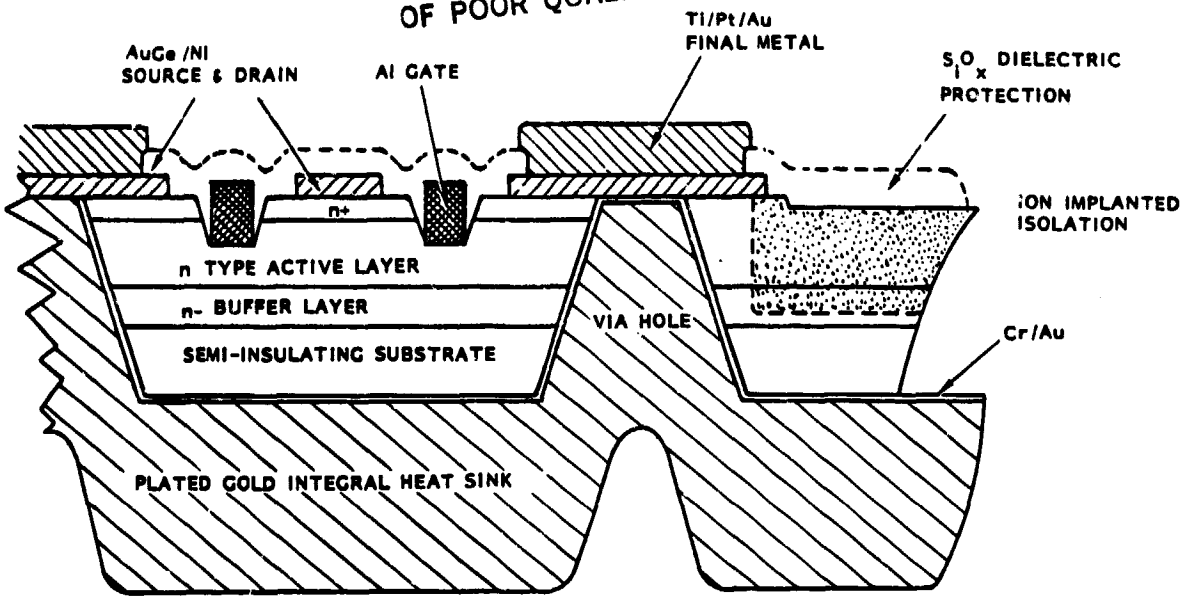


Figure 3-3. Schematic Cross Section Through Power FET

Table 3-3. DC Parameters

PARAMETER MEASURED	CONDITIONS OF MEASUREMENT
I_{dss} (mA)	V_{ds} = 2 TO 3V
Transconductande g_m (mS)	V_{ds} = 2 TO 3V, V_{gs} = 0-(-1)V.
Pinch-off voltage Vp (V)	V_{ds} = 3V, I_{ds} ≤ 1mA
Forward gate voltage V_f (V)	I_{gs} = 10mA
Gate to drain breakdown BVgd (V)	I_{gs} = 1mA
Gate to source breakdown BVgs (V)	I_{gs} = 1mA

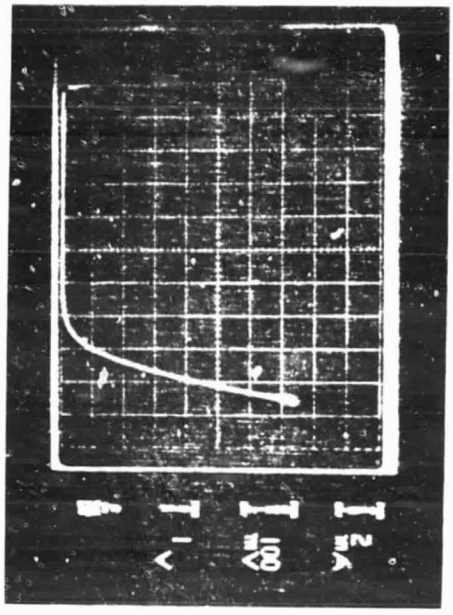
possible under these circumstances. Figure 3-4 shows the dc characteristics of a two-cell 50-micron unit-gate-width, 872 type device mounted in a test fixture to illustrate measurement of the various parameters.

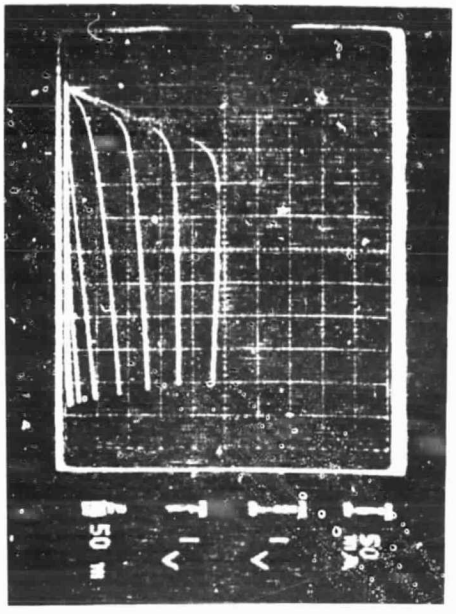
3.5 THERMAL CHARACTERIZATION

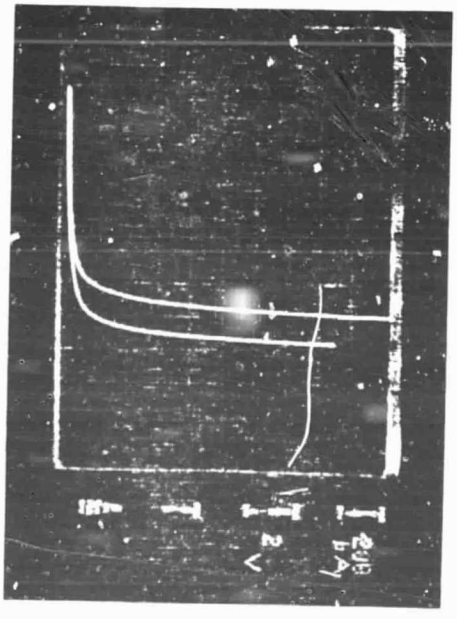
Two techniques are available for measuring the thermal impedance of FET devices. The first uses an infrared microscope (Barnes RM-2A) to measure the surface temperature directly while a known dc input power is applied to the device. The infrared technique has the disadvantage of limited spatial resolution since the viewed area is typically 10 to 20 microns diameter. The position of hot spots cannot therefore be defined to better than a drain finger width. The microscope also has to be calibrated for the emissivity of the surface, and since the area monitored encompasses gold, aluminum, and GaAs surfaces, a great deal of uncertainty in the measured temperature can result.

The favored method for thermal impedance measurement, particularly on the small-area devices developed on this program, utilizes the temperature-dependent optical properties of a nematic phase liquid crystal. In this technique the chip bonded on its test fixture is covered with a thin film of the liquid crystal placed on a high-power microscope stage and illuminated with plan polarized light. An analyzer is placed in the viewing arm of the microscope and rotated until a clear image of the chip surface is seen. The liquid crystal in its nematic phase rotates the plane of polarization of the transmitted light, thus the polarizer and analyzer are actually crossed under these conditions. The device is then dc biased. Any point on the chip surface which exceeds the critical nematic transition temperature of the crystal renders it optically inactive. This region of the surface then appears black. The thermal impedance with respect to this hot spot is easily calculated from a knowledge of the crystal nematic point and the dc power input to the device.

The liquid crystal technique is capable of very high resolution and can easily locate the position of the hot spot within a channel width. Thermal impedances measured by this technique are extremely reproducible. The disadvantage of this method is that the temperatures at which thermal impedance can be measured are restricted by the availability of crystals







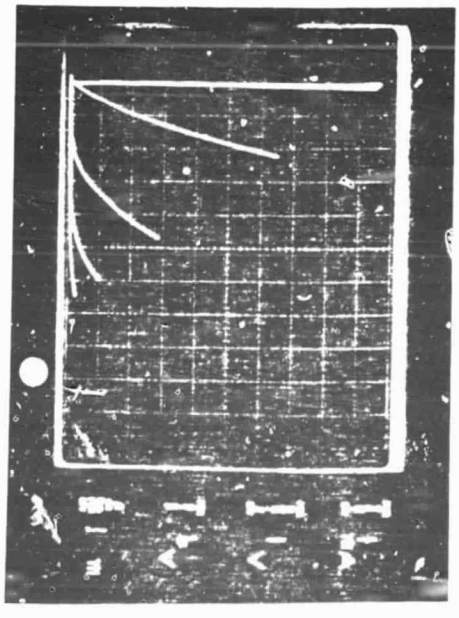


Figure 3-4. DC Characterization (Device 8A284B/872/50 Micron 2 Cell No. 1)

with different nematic points. Fortunately, most crystals show the transition at around 80°C which is close to the actual operating temperature of the device.

Devices delivered on the program were fabricated using both the initial mask sets and the updated design. The microwave performance of the various device types and the reasons for choosing one of the designs are discussed in Section 3.9. The results of thermal characteristics are presented in Section 3.10. A summarized description is given initially of the device types investigated on this program in order to clarify this report.

3.6 DESIGN OF 862, 872, AND 900 TYPE DEVICES

All devices investigated in this program used the Raytheon via-hole plated integral heat sink fabrication technology. In order to investigate the optimum device layouts, two mask sets, types 862 and 872, were utilized giving various combinations of total-gate-width and unit-gate-width as indicated in Table 3-2. Two chip types of 50-micron and 100-micron unit-gate-widths were included on each mask set. The chips were comprised of two independent cells, but the mask sets differed in the number of gate units carried by each cell; thus, a total of six different total gate widths were available for investigation depending on whether one or two cells were utilized. In particular, a total gate width of 1.2 mm for the 862 device and 0.8 mm for the 872 device was achieved with either the 50 or 100-micron unit-gate-width thus allowing a direct comparison of the alternative configurations from a single wafer. Estimated power output capabilities based on a conservative figure of merit of 0.5 W/mm are included in the table. Photographs of devices of both types at the completion of front face processing are shown in Figures 3-5 and 3-6.

After extensive processing and RF characterization as described in the following sections, the 100-micron unit gate 872 device type was chosen for a second mask iteration. Figure 3-7 shows a photograph of the slightly modified, type 900 structure. Most major dimensions, such as source pad area, drain finger width, and band pad areas, remained unchanged. The gate bus metallization, however, was moved away from the mesa edge to simplify alignment and avoid the possibility of high gate-drain feedback capacitance when alignment was imperfect. The source-drain space was reduced from 7 to

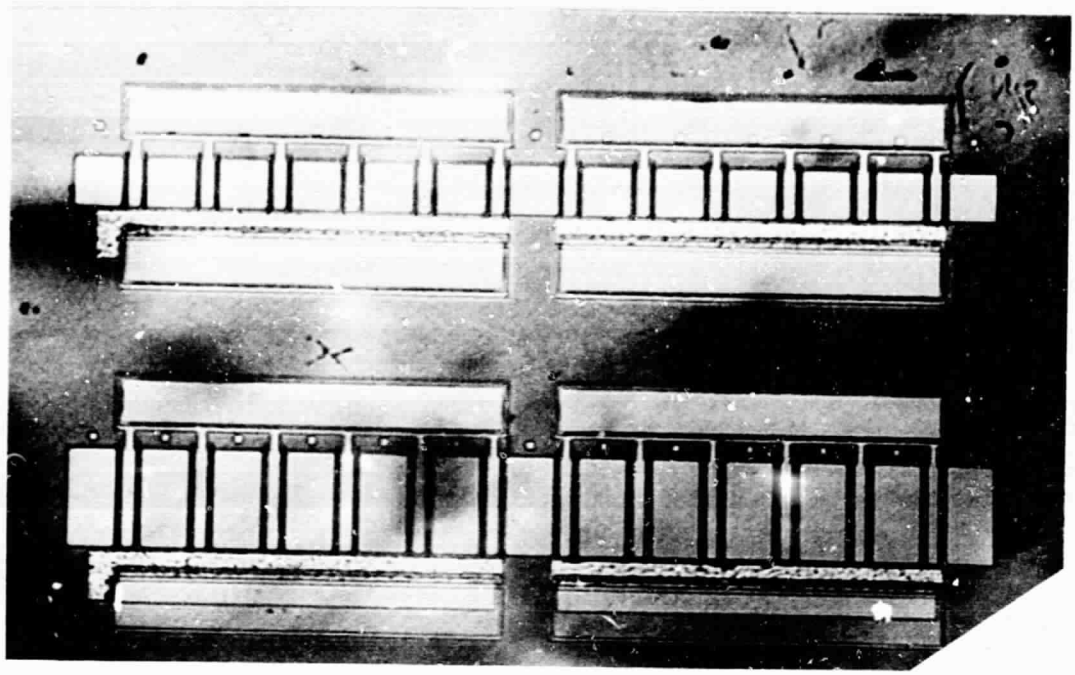


Figure 3-5. 862 Type Devices

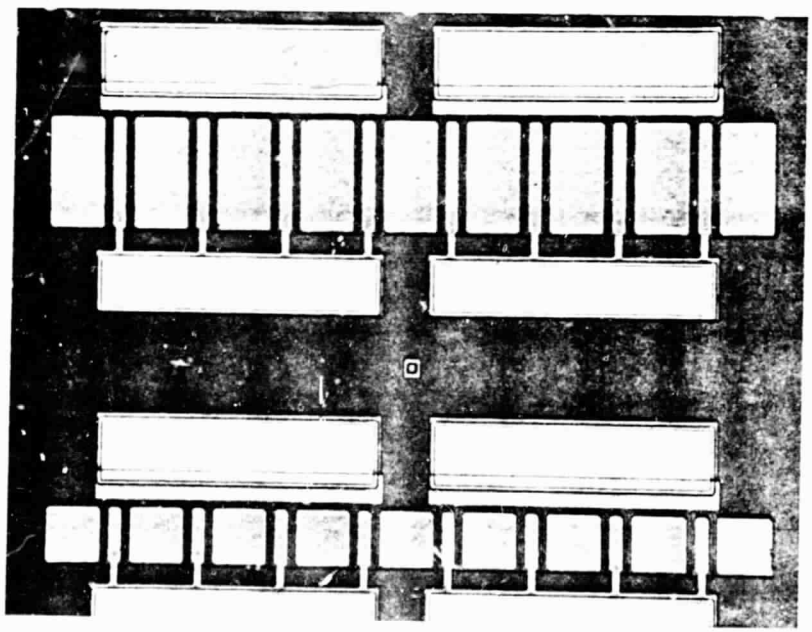


Figure 3-6. 872 Type Devices

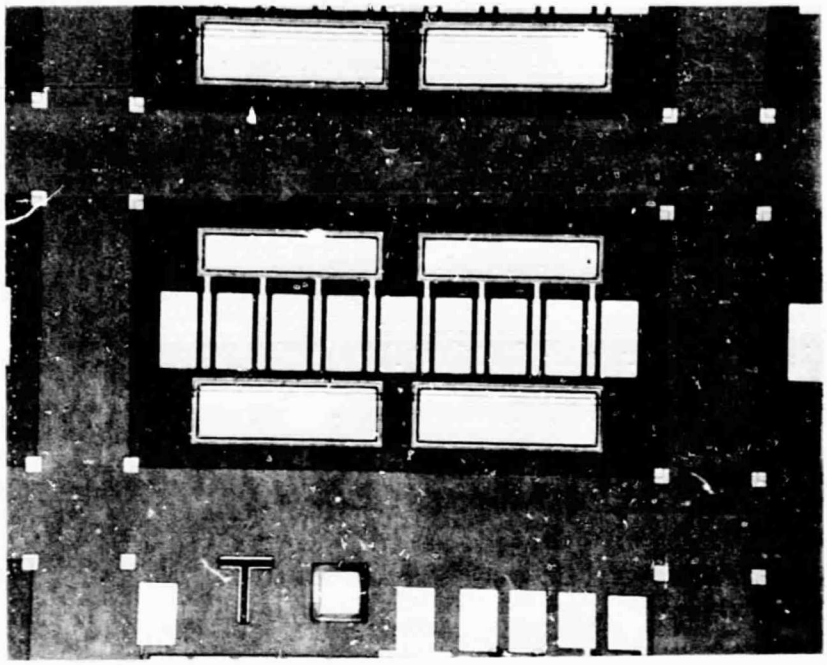


Figure 3-7. 900 Type Device

5 microns to reduce parasitic resistances, and the chip was made slightly larger to eliminate effects of excessive undercutting in final dice separation. The SiOx passivation was confined within the boundaries of the chip to prevent cosmetically undesirable overhangs after chip separation. Alignment marks were added to each chip for direct electron-beam writing of gates anticipating installation of the E-beam facility at SMDO.

A test pattern for in-process monitoring of device parameters and for performing several fundamental dc characterizations was incorporated as a drop-in. The test pattern shown in Figure 3-8 includes unit gate transistors for process monitoring, gates with pads at both ends for resistance measurements, an unpassivated gate for SEM examination of gate length, and a FAT FET for mobility profiling. Structures for measuring ohmic contact resistances and TiPtAu/Al overlay resistances are provided, as well as a unit gate FET, oriented at 90° to the conventional device, for investigating anisotropic channel etching. Alignment marks for all the mask layers are located on the test pattern.

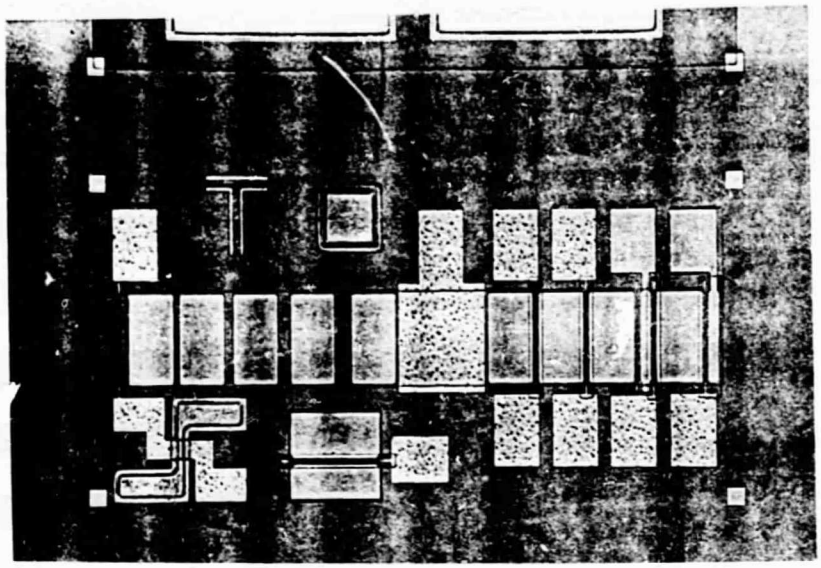


Figure 3-8. Test Pattern Included on 900 Type Mask Set

Contact photolithography was used for gate definition on all devices fabricated during this program. Nominally 0.5 micron masks were utilized with a Karl Suss submicron aligner. Gate dimensions actually achieved at high yield over 1-inch square wafers were typically 0.7 microns. Figure 3-9 shows an SEM photograph of a typical 0.7 micron gate on one of the 900 type devices. It was found that achievable gate length was limited mainly by wafer flatness, mask bowing, etc., which prevent intimate contact between mask and wafer over a large area. Thus, although 0.5 micron gates could be achieved over part of a wafer, yields of completely gated FETs were generally too low for acceptance as deliverable units. (Electron-beam direct writing of gate eliminates the flatness problem, and gates with length down to 0.4 microns have since been fabricated with extremely high yield.)

3.7 WAFER PROCESSING SUMMARY

Processing starts were made on 28 wafers during the course of this program, covering active carrier concentrations 6.0×10^{16} to 1.9×10^{17} electron/cm^3. Of these, 11 were 862 types, 10 were 872 types, and 7 were the final 900 type design. Wafer rejections, before reaching the final chip stage, totaled 6 and 5 for the 862 and 872 types, respectively,

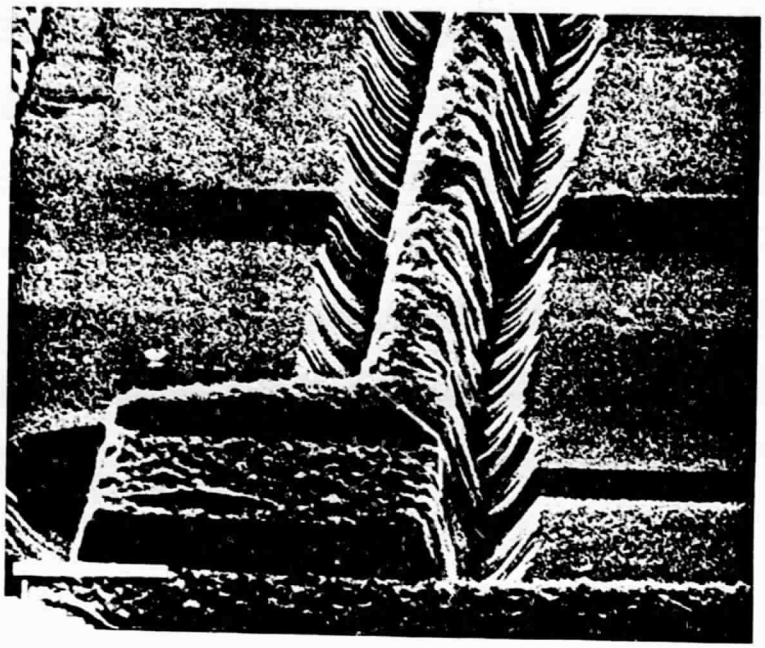
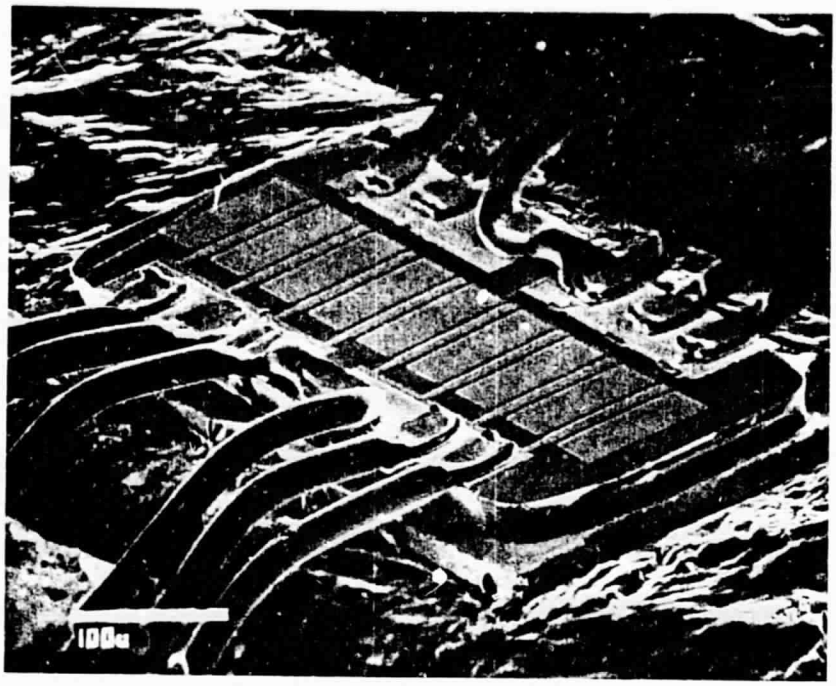
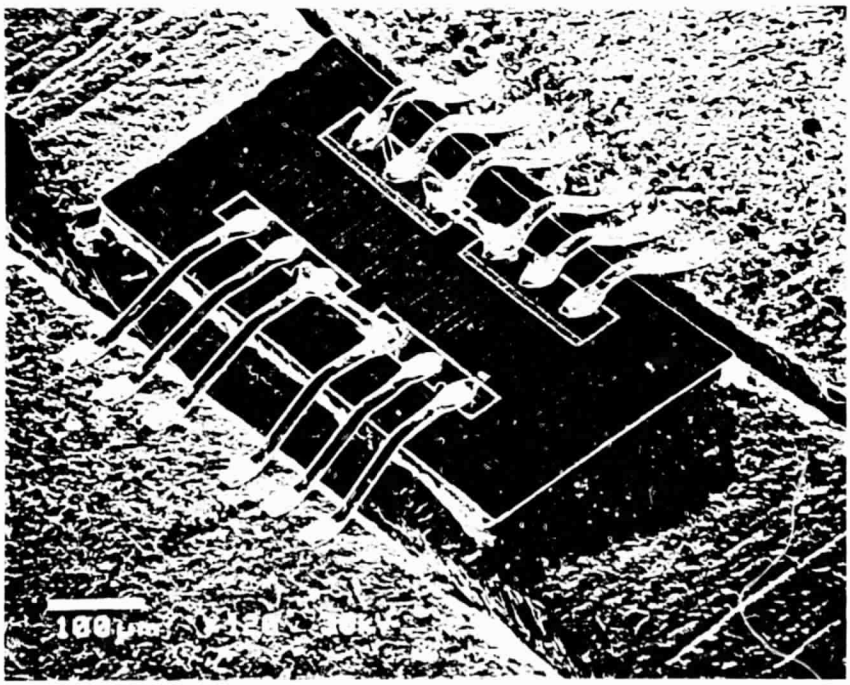


Figure 3-9. SEM of 0.7 Micron Gate: 900 Type Device Wafer 17A63A

whereas only one 900 type wafer was rejected. Most rejections followed completion of front face processing when thorough dc probe testing revealed low gate yield and/or high parasitic gate resistance. The latter effect was a recurring problem during the early stages of the program and was traced to a high contact resistance between the Al gate bus and TiPtAu final metal overlayer. The problem was studied independently using test patterns and finally solved by a minor process modification. Low yields of submicron gates were a consequence of inadequate wafer flatness and improved considerably when wafers were prechecked for flatness using a laser interferometer. Mask quality was also a significant factor. The 872 gate mask consistently printed shorter gates than the 862, and the 900 mask was superior to both. A few 862 and 872 wafers were lost during back face processing because of severe undercutting at the final etch dice stage. This problem was solved in the 900 type design by increasing the chip size slightly. Figure 3-10 compares SEM photographs of mounted and wire-bonded



a) 872 TYPE DEVICE (TWO-CELL)



b) 900 TYPE DEVICE (TWO-CELL)

Figure 3-10. SEM of Wire-Bonded Chips

872 and 900 type chips, showing how the former is undercut to the edge of the bonding pads, while the latter has additional GaAs around the active areas.

3.8 RF CHARACTERIZATION

Sample chips from each completed wafer were mounted using Au/Sn eutectic solder on the central ledge of gold plated copper test fixtures shown in Figure 3-11. Chips were wire bonded with 0.001-inch diameter gold wires, as shown in the SEM pictures of two-cell chips in Figure 3-10. Three bond wires per bond pad were used to minimize bond wire inductance, and the bond pads were interlinked on the chip. Interlinking of cells on the chip has been found essential for preventing spurious oscillations and obtaining optimum performance. The absence of source bond wires, as a consequence of via-hole technology, is a feature to be noted in Figure 3-10. The input and output 0.025-inch alumina ceramics in Figure 3-11 carry single section transformers for approximately matching the 100-micron unit-gate-width two-cell chip. Simple 50-ohm lines were generally used with single cell chips and also for S-parameter characterization.

The fixture mounted devices were characterized on the Ku-band power RF test bench shown schematically in Figure 3-12. The test bend is constructed around a Pacific Measurement Inc. (PMI) model 1038 system, which allows both swept frequency gain response and swept amplitude input power versus output power to be displayed on an oscilloscope screen. The swept amplitude facility has been found invaluable on this program for properly optimizing devices for best large signal performance. Typically, three devices of each type from each completed wafer were characterized. For example, in the case of 872 type devices, three single-cell devices of 50-micron and 100-micron unit gate-width plus three each of the two-cell units were characterized, giving twelve devices altogether.

The standard sequence of RF measurements follows. Devices were initially assessed for small signal gain and bandwidth capability by operating the bench in the swept frequency mode over 13 to 18 GHz at 0 to 10 dBm input. The device was biased approximately to the operating point (typically V_{DS} = 8 V, V_{GS} = 1.5 V) and the input and output tuned by moving small gold plated metal discs or indium foil around on the microstrip lines of the input and output ceramics. At this stage, the aim was to maximize

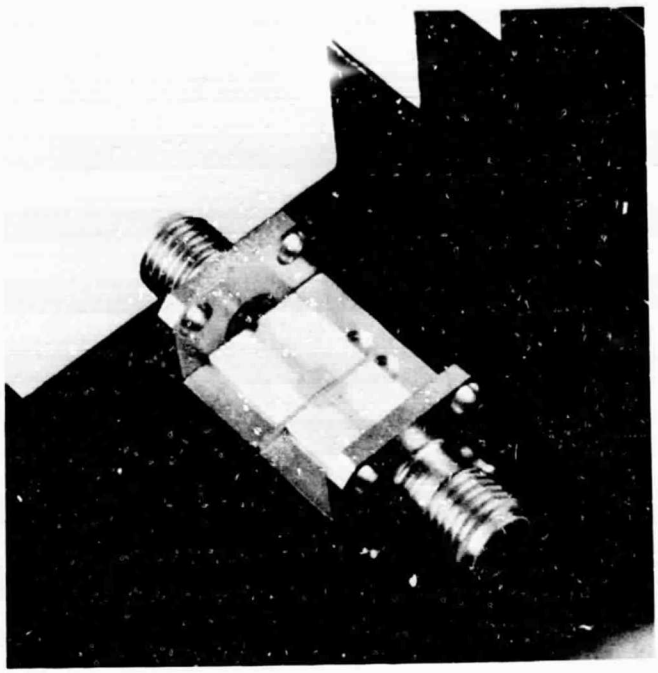


Figure 3-11. Ku-Band Test Fixture

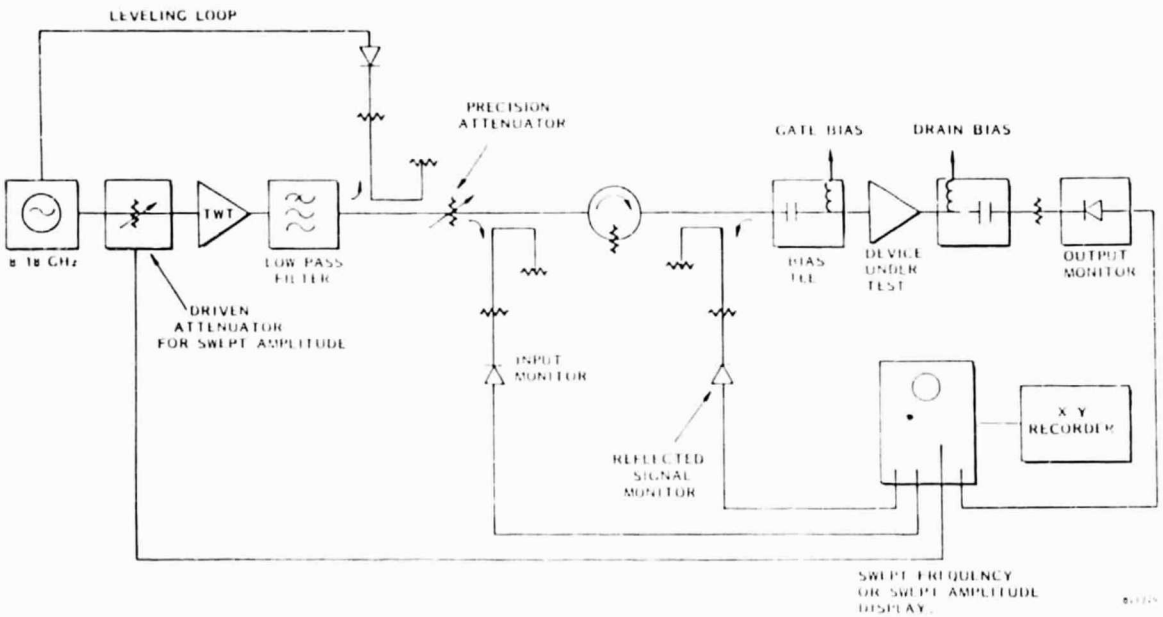


Figure 3-12. Ku-Band Power Test Bench Schematic

the gain at 18 GHz and obtain an indication of bandwidth capability. Tuning of the input was aided by viewing the reflected signal and adjusting for maximum return loss at 18 GHz. Figure 3-13 demonstrates typical swept frequency gain responses for two devices. Devices which achieved at least 5 dB small signal gain at 18 GHz were judged adequate for further characterization in the swept amplitude, high power mode. Before carrying out power measurements, the PMI system was accurately calibrated against a precision power meter. A 50 ohm through-line replica of the test fixture was then used to calibrate out the ceramic and connector losses in the test fixture such that power measurements could be referred to the device chip. The device chip was initially biased and tuned to duplicate the small signal conditions at 18 GHz while applying a swept amplitude power input covering a 20 dB dynamic range from small signal to saturation. Fine adjustment of the tuning and bias levels was then made to maximize the saturated power output while maintaining a high linear gain. Usually a compromise had to be made between these two quantities, and in this program a linear gain of around 5 dB was considered the minimum acceptable. Power output at 4 dB associated gain (which is the minimum gain required by the Statement of Work) then corresponds to 1 dB gain compression. It was usually necessary to make a significant adjustment to the output matching circuit to achieve high power performance while the optimum input match was essentially unchanged from its small signal condition. Figure 3-14 shows typical power transfer characteristics as recorded by PMI, illustrating the different performance achieved under optimized small signal and optimized high power conditions for the same device.

Small signal S-parameters were measured on selected devices using a Hewlett Packard 8409-A Semi-Automatic Network Analyzer over the 2 to 18 GHz band. The system was calibrated using microstrip short circuit and through-line replicas of the test fixture in order to achieve a reference plane at the device chip. Bond wires could be eliminated from the measurements, if desired, by subjecting the data to a de-embedding routine. Raw measured data was curve fitted to a third-order polynomial to remove amplitude and phase ripples caused by test fixture imperfections.

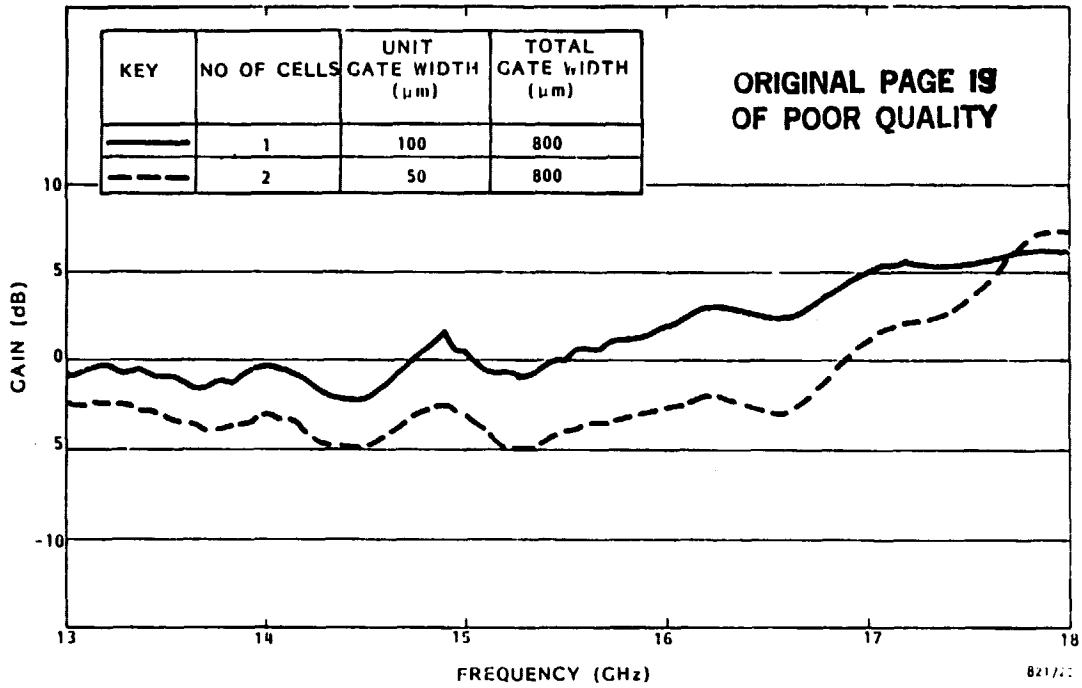


Figure 3-13. Small Signal Gain for 872 Devices

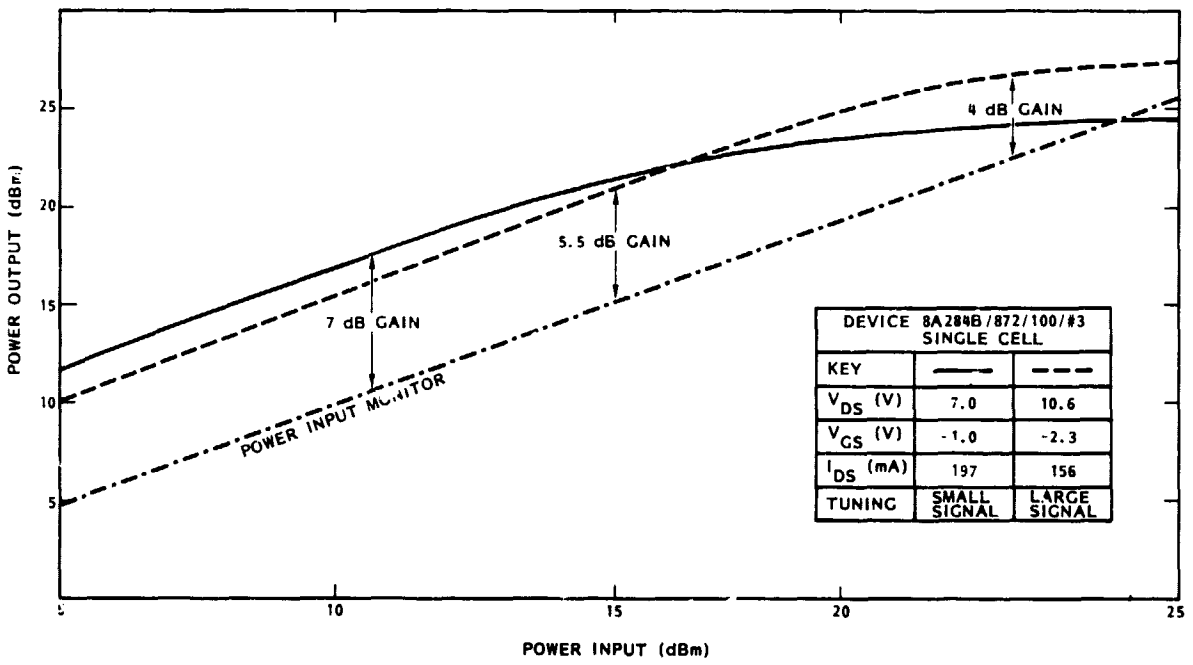


Figure 3-14. Device Optimized Under Small Signal and Large Signal Conditions

3.9 RF PERFORMANCE

3.9.1 862 AND 872 TYPE DEVICES

The best power performance achieved at 18 GHz for the various 872 and 862 device types is summarized in Table 3-4. All the results quoted for 872 type devices were obtained from Wafer No. 8A284B, which gave a particularly high yield of high performance chips. One other 872 wafer, 8A354, gave devices with performance approaching the results of Table 3-2. The single result quoted for an 862 type device was obtained from another extremely high performance wafer, 8A270, which gave a much lower chip yield. No 100-micron type chips were successfully characterized from this wafer. The full power transfer and efficiency plots for the three best 872 type devices are given in Figure 3-15. It is clear that the power scales extremely well with total gate width for the 872 devices giving a power per unit gate-width figure of merit at 4 dB associated gain of 0.63 W/mm^{-1}. The low linear gain of the two-cell device is almost certainly a consequence of the difficulty in impedance-matching the large gate-width. The matching transformers shown in Figure 3-11 were necessary to obtain the 1 W performance. Attempts to match the two-cell devices using simple 50-ohm lines on the test fixture clearly showed the need for matching elements very close to the chip. The lower linear gain of the 50-micron single-cell compared to the 100-micron is not believed to be significant and could probably have been raised to the same value by more careful tuning.

The similar optimum bias voltage conditions for all three devices from 8A284B is a consequence of the very uniform breakdown voltage and pinch-off parameters for this batch of chips.

The performance of the 862 single-cell 50-micron type device shown in Table 3-3 is remarkably good, and the figure of merit of 0.8 W/mm is close to the best values reported for X-band devices. This result, however, is not typical of the 862 device types, which generally performed poorly compared to the 872 devices. This was attributed to the poorer gate definition for this mask set, leading to longer gates in most cases. Also, the double-cell chips were rather long, and it is believed that distributed effects were significantly degrading performance. Table 3-3 shows that the required power performances were adequately met by the smaller total gate-width 872 devices; thus the 862 design with 12 gates per cell was discontinued.

Table 3-4. Performance Achieved with 862 and 872 Type Devices at 18 GHz

MASK SET	UNIT GATE WIDTH (μ m)	NO. OF CELLS	TOTAL GATE WIDTH (μ m)	OUTPUT POWER (mW)	ASSOCIATED GAIN (dB)	LINEAR GAIN (dB)	VDS (V)	POWER ADDED EFFICIENCY η ADD (%)	POWER PER UNIT GATE WIDTH (W/mm)
872	50	1	400	250	4	5	10.0	17	0.63
862	50	1	600	480	4	6	10.0	21	0.80
872	50	2	800	370	4	5.5	8.0	15.5	0.46
872	100	1	800	500	4	5.5	10.6	18	0.63
872	100	2	1600	1000	4	4.8	10.5	22	0.63

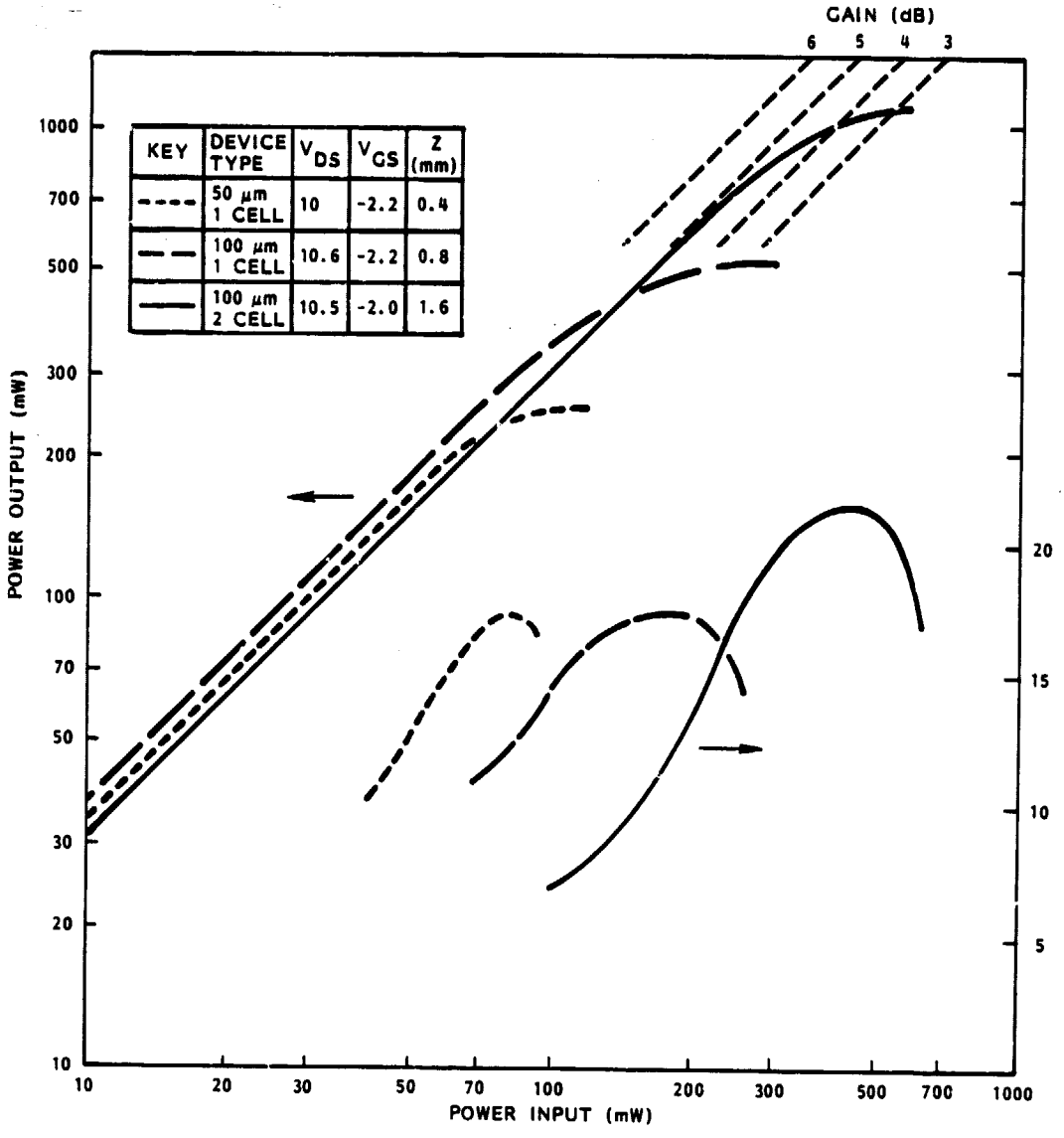


Figure 3-15. Performance of 832 Type Devices at 18 GHz

The results for the double-cell 50-micron 872 device, shown bracketed in Table 3-3, are included to compare with the single-cell 100-micron unit of identical total gate-width. The double-cell chip was found much more difficult to tune than the single-cell unit, and it was not possible to achieve such a broad bandwidth in the simple test fixture. This observation is well illustrated in Figure 3-13 where the optimum small signal swept gain is compared for the two devices. The two-cell device was clearly much narrower band although it appears to have a higher small signal gain capability. The lower power achieved with the two-cell device is believed, therefore, to reflect the difficulty of tuning in the 50-ohm system. The two-cell 100-micron devices showed a narrow band response very similar to Figure 3-13 and it was necessary, as explained above, to use close-to-chip matching elements to obtain high power performance. Use of these matching elements on the two-cell 50-micron unit would probably have enabled 0.5 W to be achieved.

S-parameter characterization revealed clearly the difference between single-cell and two-cell devices. In Figure 3-16 the magnitude of $|S_{21}|$ is plotted against frequency, using smoothed data, for the various chip configurations under the same bias conditions. At low frequencies the behavior is as predicted. The largest and smallest gate-width devices have the largest and smallest $|S_{21}|$ respectively. The two configurations with 800-micron gate-width give the same $|S_{21}|$. However, at high frequencies the two-cell devices track together and the one-cell devices track together, independently of total gate-width. The two-cell units have typically to 4 to 5 dB lower $|S_{21}|$ at 18 GHz. The results clearly indicate that the larger unit gate-width approach to achieving increased total gate-width is better than increasing the number of gate stripes, at least at around 800-micron total gate-width. It remains uncertain, however, how large a gate-width unit can be accepted before resistive losses dominate.

3.9.2 900 TYPE DEVICES

Table 3-5 lists the RF performance achieved at 18 GHz for the six successfully completed wafers using the 900 type mask set. Also listed are the dc parameters of the devices and active layer carrier concentrations. Every wafer gave devices exceeding the minimum specifications for the 1 W

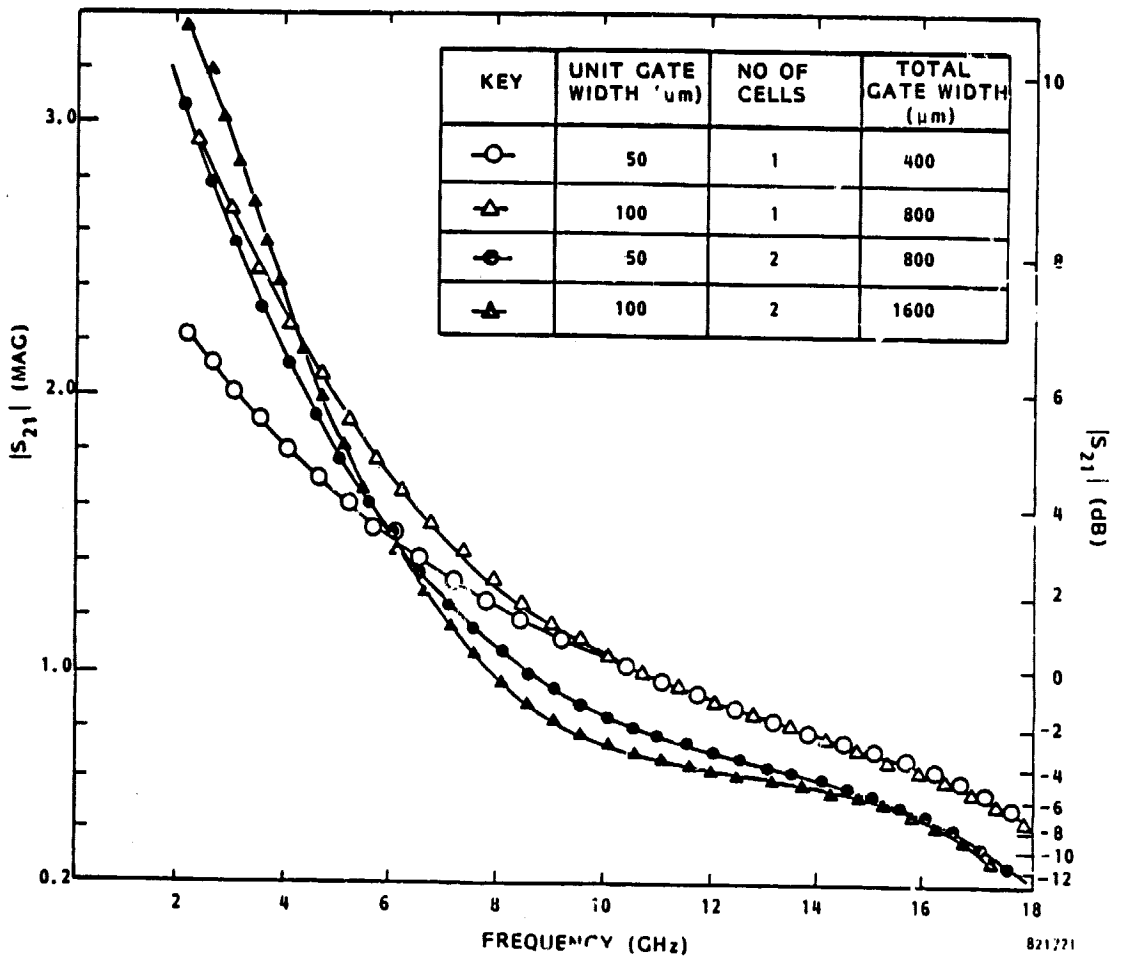


Figure 3-16. $|S_{21}|$ vs. Frequency for 972 Type Devices

Table 3-5. RF Performance of 900 Type Devices at 18 GHz

WAFER # ($N_D \times 10^{16}$)	NO. OF CELLS	DC PARAMETERS				P_{out} (dBm)	ASSOCIATED GAIN (dB)	LINEAR GAIN (dB)	POWER ADDED EFFICIENCY (%)
		I_{dss} (mA)	V_f(V) at 10mA	g_m (mS)	V_{BGD} (V)				
15B98A (8)	1	280	1.1	70	16	27	6.0	6.8	22
	2	560	1.0	120	15	30	5.5	6.0	22
15C4 (9.8)	1	200	0.95	70	15.2	27	5.0	6.0	26
	2	400	0.95	125	15.0	29.5	4.5	5.5	22
15B74 (16.5)	1	100	1.05	68	14.5	26	4.5	6.5	26
	2	380	1.3	200	10.0	29	4.0	5.5	18.5
8A494 (17)	1	220	0.95	100	11.0	28	5.5	6.5	27
	2	460	1.2	200	10.0	30	5.5	6.5	20
8A448 (7.8)	1	210	0.98	75	16.4	27	5.5	6.0	26
	2	480	0.88	130	14.4	30	5.0	5.5	21
17A63A (8.2)	1	250	0.9	60	13.0	27	5.0	6.0	21
	2	450	0.85	130	14.0	30	5.0	5.5	22

and 1/2 W units. The best wafers 15B98A and 8A494A produced two-cell devices giving 1 W power output with 5.5 dB associated gain. The improved performance compared with 872 type devices is attributed to the minor design changes, and in particular the improved gate mask which enabled much higher yields of short gate, low parasitic chips to be fabricated.

Toward the end of the contract a K-band (18 to 26.5 GHz) test bench was assembled similar to the schematic of Figure 3-10 and used to characterize devices at 20 GHz. Figure 3-17 shows the power transfer characteristics under small signal and large signal tuning at 20 GHz for a two-cell device from wafer 8A494A. A power output of 1 W at 1 dB compression with 5 dB associated gain and 22 percent power-added efficiency was achieved. Under optimized small signal tuning, the same device achieved 8 dB linear gain. Swept frequency measurements were also performed on this device and an attempt made to empirically match the device over the bandwidth of interest to TRW. Fine tuning with indium foil placed close to the chip gave the performance shown in Figure 3-18. The device gave a 1 dB bandwidth from 19.5 to 21.5 GHz with 28 dBm power output and 6 dB gain at band center corresponding to 1 dB gain compression.

3.10 THERMAL CHARACTERIZATION DATA

A technique for measuring thermal resistance and locating hot spots using nematic phase liquid crystals was outlined in Section 3.5. Figure 3-19 shows a sequence of microphotographs of a single-cell 100-micron unit gate 872 type device covered by a film of liquid crystal and biased (at V_{gs} = 0) to heat the channels. The phase transition point of the liquid crystal is 75°C and all points exceeding this temperature appear black. In picture 2, at an input power of 0.85 W, the hot spots at 75°C are visible toward the drain pad end of the centrally located channels. This is precisely the point that thermal models predict the hot spots to be located. The thermal resistance with respect to these hot spots is simply calculated from the channel temperature rise above ambient (ambient = 22°C) as $63°CW^{-1}$. The remaining photographs show the effect of increasing the dc

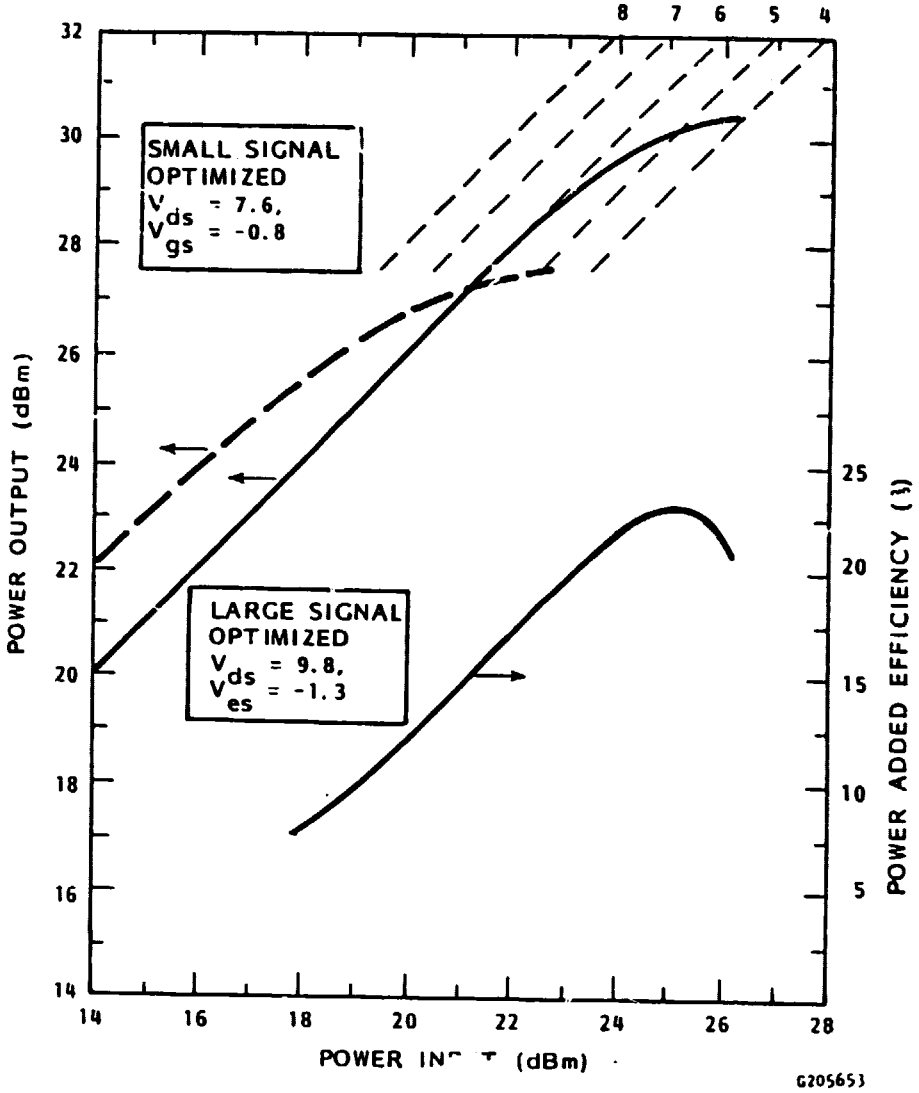


Figure 3-17. Performance of Two-cell 900 Type Device at 20 GHz

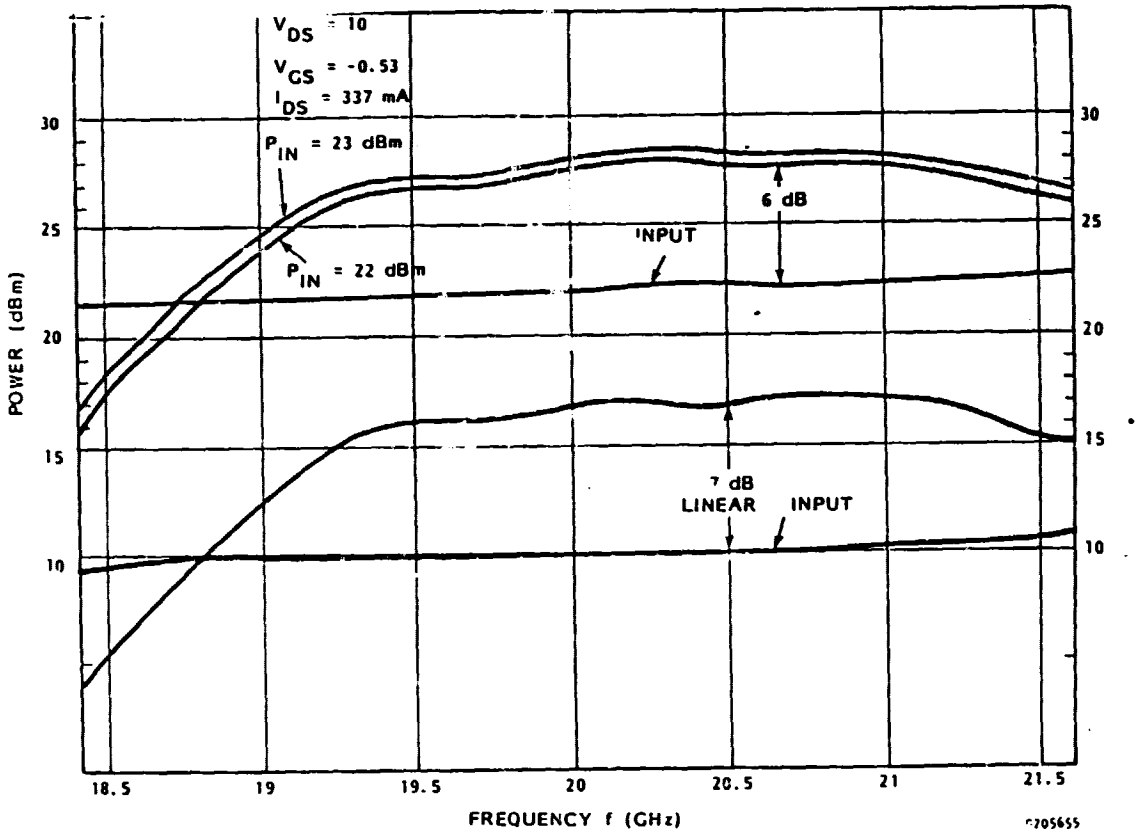


Figure 3-18. Bandwidth Performance of Two-cell 900 Type Device

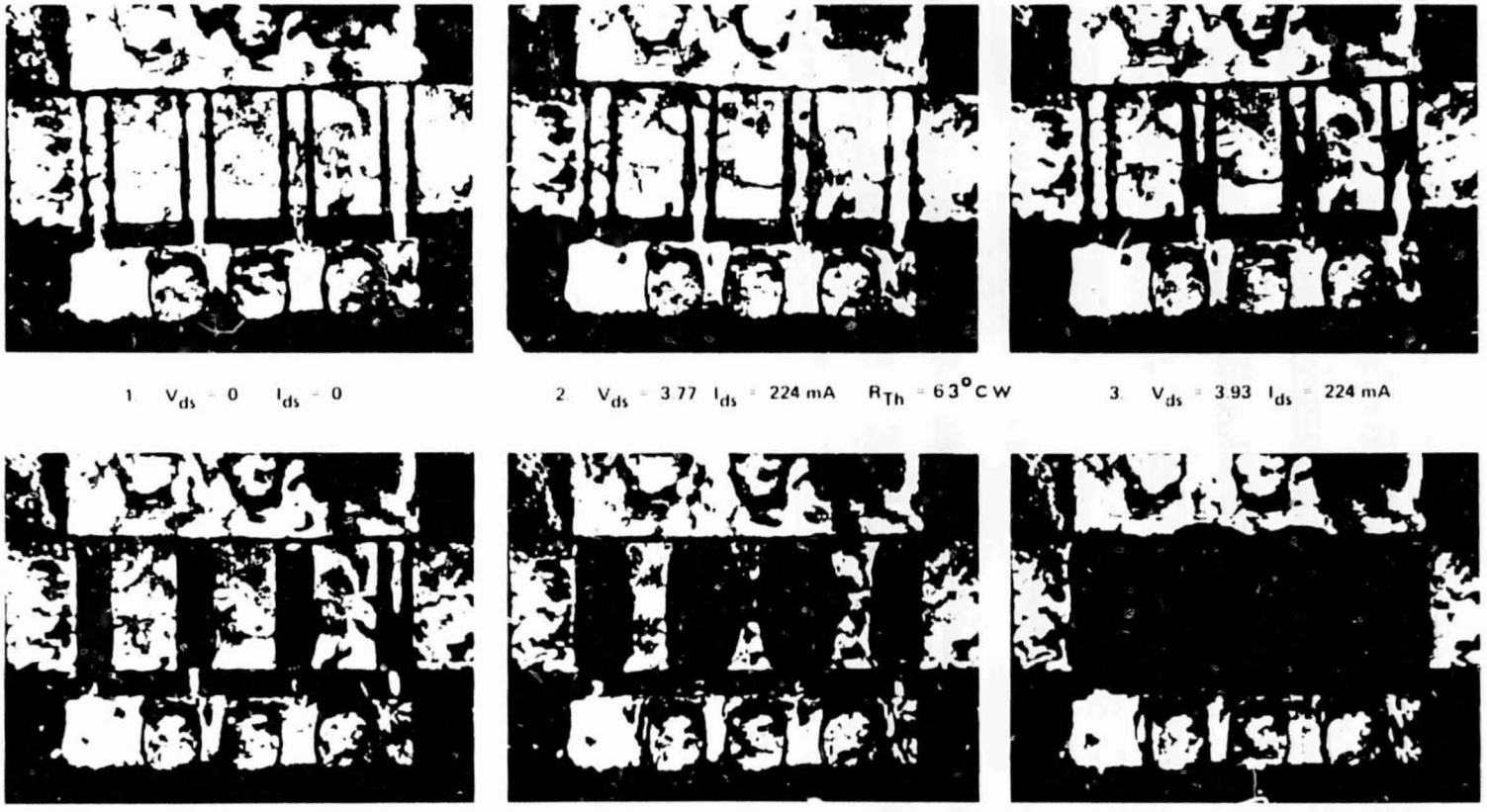


Figure 3-19. Liquid Crystal Thermal Resistance Measurements

power dissipation. In each case the edge of the black region is a 7[illegible] contour. Thus, the method gives a very clear representation of the temperature distribution in the chip. Table 3-6 lists the results of thermal resistance measurements with respect to the hot spot for seventeen 862 and 872 devices from four different wafers covering all the gate-width configurations. In all cases the devices were mounted with Au/Sn slder on the 0.020-inch wide x 0.025-inch high ridge of the test fixture shown in Figure 3-11. The final column gives the thermal resistance normalized to unit gate-width and confirms, within the device-to-device variation, that thermal resistance scales approximately inversely with gate-width as expected. The mean value of normalized thermal resistance is $53.4°CW^{-1}$ with a variance of $7.5°CW^{-1}$.

3.11 DEVICE ASSEMBLY AND DELIVERY

Devices delivered on this program were of 872 types originating from wafers 8A284B and 8A354, and of 900 types from wafers 8A494, 8A448 and 15B98A. All these wafers were considered "qualified" in that a large proportion of sample chips had surpassed the minimum specification requirements at 18 GHz on Raytheon's test fixture. Chips from these wafers were chosen on the basis of dc probe data and mounted on TRW's carriers in the Raytheon assembly area. The carriers were received in disassembled form; thus, it was necessary to solder the subcarriers carrying the quartz substrate to the copper bases simultaneously with mounting the chip on the copper ridge of the latter. This was accomplished using Au/Sn eutectic solder. Finally the chip was wire bonded to the 50-ohm lines of the quartz substrates using the configuration of Figure 3-10.

In anticipation of RF testing assembled devices before shipment, a waveguide test fixture was constructed to the design of TRW. A few devices were tested in this fixture using indium foil as a temporary runing element and were found to meet the specification requirements. However, in most cases the carriers were received without the necessary dc blocking and bias network bypass capacitors; thus, it was not possible to test devices before shipment. Nevertheless, this method of delivering devices functioned very successfully, although there were some instances of carriers broken in shipment. As an example of successful cooperation on this program, one group of devices was found to perform particularly poorly at TRW and were

Table 3-6. Thermal Resistance Data

DEVICE TYPE & NO.	TOTAL GATE WIDTH Z (mm)	AMBIENT TEMP. T_A (°C)	Bias at Hotspot = 75°C		THERMAL RESISTANCE R_{Th} $^oCW^{-1}$	NORMALIZED R_{Th} Z $^oCmmW^{-1}$
			V_{DS}	I_{dss} (mA)		
872/100/1 cell 8A284 #2	0.8	24	3.04	227	74	62
8A354 #1	0.8	25	2.82	224	79	63
#2	0.8	25	3.79	224	59	47
#3	0.8	25	3.33	232	65	52
#4	0.8	26	3.48	215	65	52
872/100/2 cell 8A354 #1	1.6	26	3.21	461	33	53
#2	1.6	26	2.78	469	38	60
8A283 #6	1.6	24	2.45	530	39	63
#7	1.6	24	2.69	531	36	57
872/50/1 cell 8A265 #4	0.4	25	3.16	151	105	42
872/50/2 cell 8A283 #2	0.8	24	3.51	285	51	41
#3	0.8	24	3.54	213	68	54
862/100/1 cell 8A348 #1	0.6	24	4.32	169	70	42
862/100/1 cell 8A348 #1	1.2	24	3.56	336	43	51
#2	1.2	24	3.32	347	53	64
8A334 #1	1.2	24	3.49	337	43	52
#2	1.2	24	3.31	359	43	52

$\overline{R_{Th}Z} = 53.4^\circ CW^{-1}$, $\sigma_{n-1} = 7.5^\circ CW^{-1}$

returned to Raytheon, after adding the chip capacitors, for reevaluation in the waveguide test fixture. The poor performance was confirmed at Raytheon and the reason traced to thin metallization on the quartz substrates. New carriers were shipped and the same chip batch gave the required performance.

3.12 CONCLUSIONS AND SUMMARY

Devices were developed giving 1/4 W, 1/2 W and 1 W output power with 4 dB associated gain and typically 20 percent efficiency at 18 GHz and were delivered to TRW, assembled on TRW's designated carriers. A second iteration of the 1/2 W and 1 W design resulted in improved performance and higher yield. 1 W output power with 5 dB associated gain and 23 percent efficiency was demonstrated at 20 GHz. A 1 dB bandwidth from 19.5 to 21.5 GHz with 28 dBm output power and 6 dB gain at band center was also demonstrated. Devices of this type were also delivered to TRW. A detailed thermal characterization gave a normalized thermal resistance of 53 $\pm$ 8°C/W/mm for all device chips when mounted on the Raytheon test fixture.

4. AMPLIFIER CIRCUIT DEVELOPMENT

4.1 WAVEGUIDE-TO-MICROSTRIP TRANSITION

4.1.1 Transition Design

Waveguide-to-microstrip transition, heretofore referred to as transition, can be designed with an exponential taper or a multistepped configuration. The exponential taper gives broader bandwidth and better match but is expensive to produce. For this application, a three-step transition is adequate.

The transducer (or transition) designed to transform from WR42 waveguide TE10 mode to microstrip is basically a series of quarter-wave sections of ridge waveguide. The ridged sections are designed to give the SWR over the frequer ,y band a Tchebycheff response. The design of the stepped transformer is detailed by Seymour B. Cohen[1]. The impedance ratio of any quarter-wave section is determined by

$$\ell_n \frac{Z_{m+1}}{Z_m} = \frac{a_m \ell_n \frac{Z_{n+1}}{Z_1}}{a_m}$$

For a transition from WR42 waverguide to 50-ohm microstrip with a 0.015-inch dielectric substrate operating over 17 to 23.5 GHz, the bandwidth ratio is

$$P = \frac{\lambda_g \text{ (17 GHz)}}{\lambda_g \text{(23.5 GHz)}} = 1.969$$

[1] Seymour B. Cohen, "Optimum Design of Stepped Transmission Line Transformer" IRE Transactions MTT, April 1955, pp. 16-21.

The waveguide impeance at the center frequency of the band is 425.58 ohms. The impedance transformation ratio is

$$\frac{Z_{in}}{Z_{out}} = \frac{425.58}{50} = 8.51$$

The values of a_m's are determined from the table in reference[1]. The input and the output impedances of each quarter-wave section can then be calculated, and the dimensions of the ridges are determined.

The three-step ridge transition was designed and fabricated. A photograph of the transition before and after assembly is shown in Figure 4-1. The insertion loss of two transitions connected back-to-back with 0.5-inch microstrip line is shown in Figure 4-2 and is less than 1 dB over most of the frequency band of interest. Therefore, the insertion loss per transition after accounting for the microstrip line loss is less than 0.4 dB. The return loss of the transition is better than 20 dB over the operating frequency as shown in Figure 4-3.

Since most of the commercially available test equipments under 18 GHz have coaxial input/output or different waveguide size connectors, the measurements shown in this section are limited to 18 GHz and above. It is assumed that the performance characteristics of the circuit elements perform within reason from 18 to 17.7 GHz.

4.2 LANGE COUPLERS

4.2.1 Coupler Design

The design of a Lange coupler (or interdigitated coupler) is based on the proximity coupling of two adjacent quarter-wavelength long microstrip lines. The coupled microstrip lines may be analyzed in terms of two fundamental modes of propagation denoted even and odd. As shown in Figure 4-4, in the even mode the current and voltages on the two strips are equal, while in the odd mode the current and voltages have opposite signs. Any other pseudo-TEM propagation on the two strips can be expressed as a combination of these two modes. It can be seen from the figure that more of the even mode field lines are in the substrate than the odd mode field

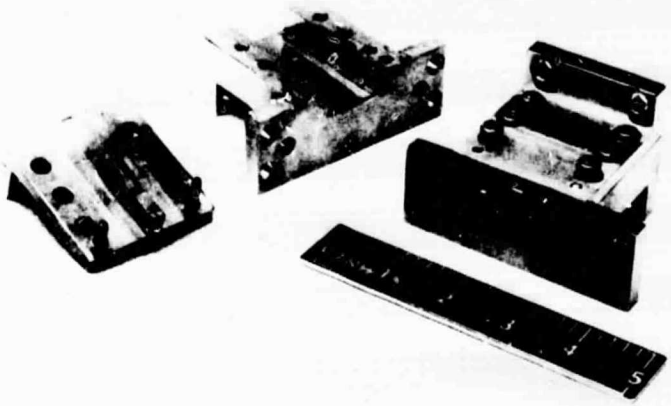


Figure 4-1. Waveguide-to-Microstrip Transitions

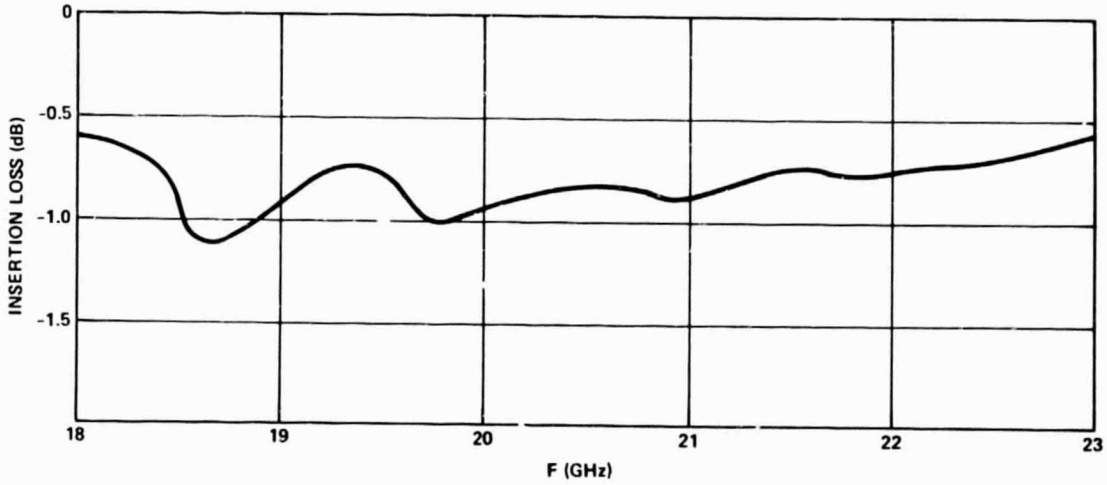


Figure 4-2. Insertion Loss of Two Transitions Connected Back to Back

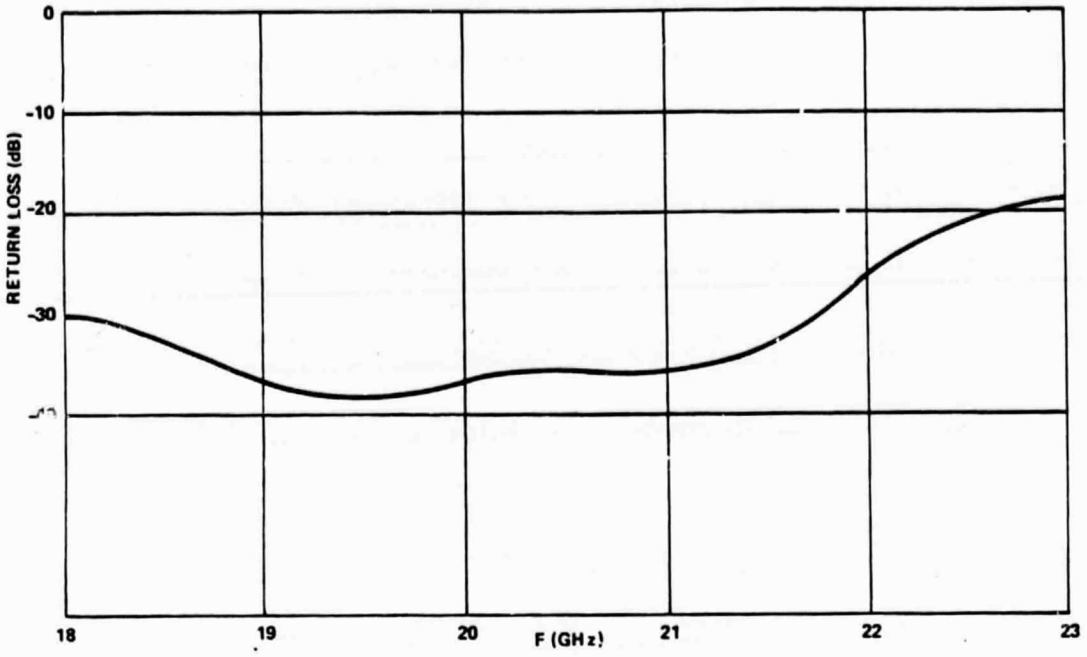


Figure 4-3. Return Loss of Waveguide to Microstrip Transition

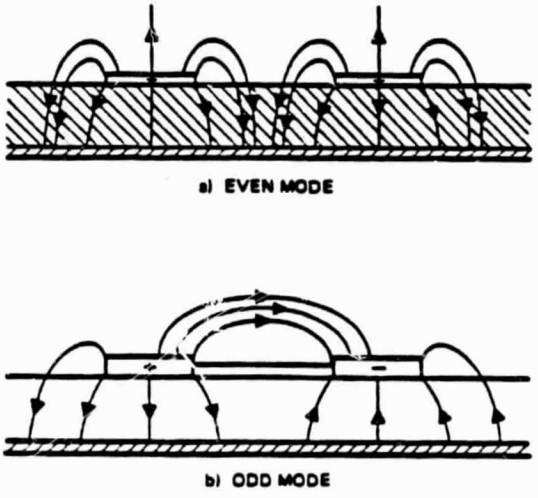


Figure 4-4. Electrical Flux Lines for
Two Fundamental Modes of Two
Coupled Microstrip Lines

lines. Because of the nonuniform dielectric structure of microstrip, the odd and even modes have different phase velocities causing dispersion. The even and odd mode impedances, Z_{oe} and Z_{oo}, respectively, required to achieve a desired power coupling ratio, C, are related by

$$C = 20 \log \frac{Z_{oe} - Z_{oo}}{Z_{oe} + Z_{oo}}$$

$$Z_o^2 = Z_{oe} \; Z_{oo}$$

where Z_o is the impedance to which the coupler ports are matched.

For a 3 dB coupler matched to 50 ohms, the even and odd mode impedance required is 120.7 and 20.7 ohms, respectively. The even impedance is determined primarily by the width dimension of the lines, whereas the odd mode impedance is a strong function of the proximity of the lines. In practice, it is difficult to realize the low value of Z_{oo} required for 3 dB or tighter coupling using a single pair of edge-coupled transmission lines in microstrip.

The basic idea behind the interdigital coupler is that for a given spacing between lines, tighter coupling is derived with multiple pairs of lines, alternately tied together at the ends, than for a single pair (Figure 4-5).

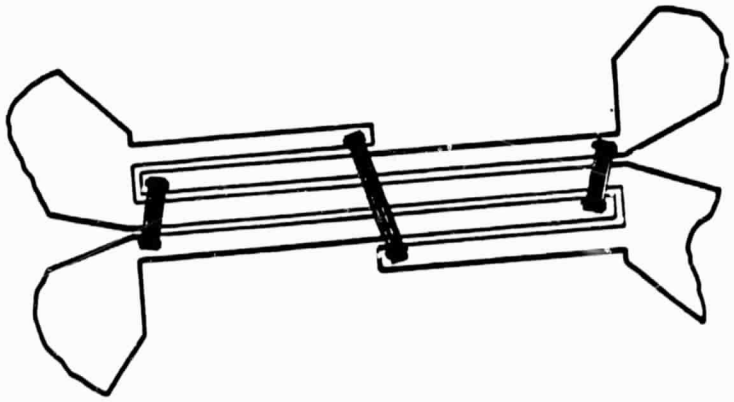


Figure 4-5. Layout and Bonding of Four-Finger Interdigitated Coupler

The interdigital coupler has been adopted widely for broadband transistor amplifier application below 18 GHz. A six-finger interdigital coupler on 0.015-inch quartz substrate, developed at TRW is shown in Figure 4-6. TRW has currently developed K-band and Ka-band interdigital couplers with encouraging progress. A first iteration six-finger interdigital coupler on a 0.015-inch quartz substrate, fabricated for the 18 to 26.5 GHz range, has an insertion loss of about 0.5 dB with 3.6 dB midband coupling. The isolation is better than 16 dB, with a VSWR of 1.6.

A major problem in the development of the interdigital coupler for high frequency is providing the crossovers without introducing a significant inductance which would result in poor phase relationship between alternate lines, causing large passband ripple. The crossovers are also a potential source of loss due to radiation. One method to reduce crossover inductance is to use a properly shaped ribbon connection for the crossovers and a quartz substrate to increase the length and width of lines. Another method is to deposit a thin layer of dielectric over the entire coupler. Crossovers are made by depositing metal over the dielectric layer; the inductance of a crossover made in this way is negligible. The interdigitated coupler designed and fabricated on quartz substrates for this amplifier is shown in Figure 4-7.

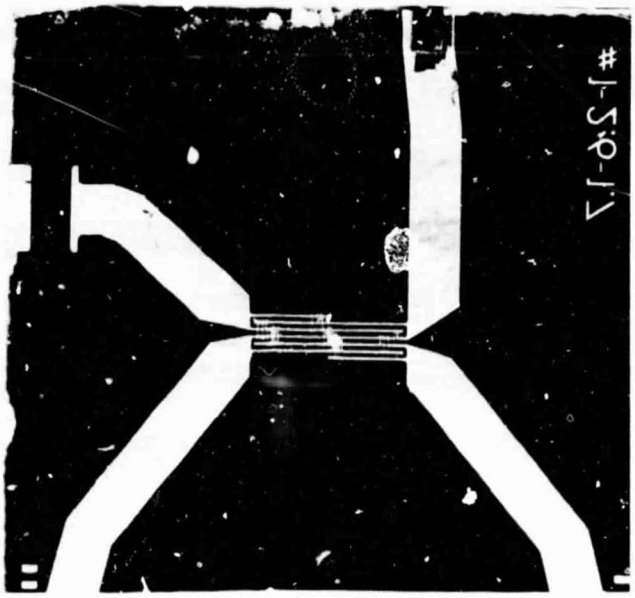


Figure 4-6. Layout and Bonding of Six-Finger Interdigital Coupler

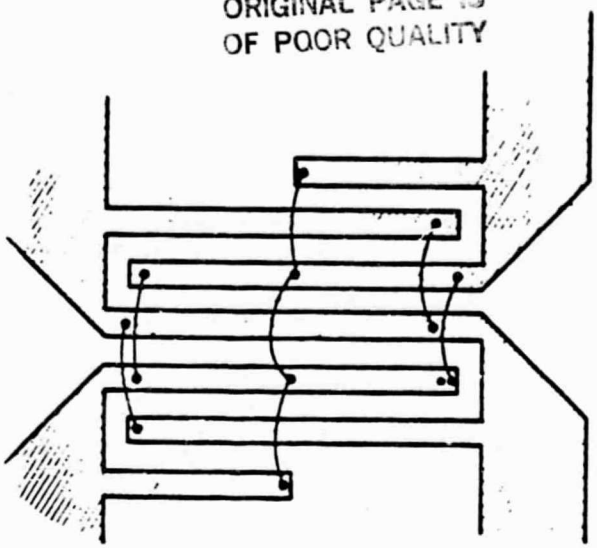


Figure 4-7. Layout and Bonding of Six-Finger Interdigital Coupler

4.2.2 Coupler Test Fixture

Since the coupler is a four-port device with one of the ports terminated using a 50-ohm chip resistor on the substrate, a three-port test fixture was designed and fabricated to test the coupler. The coupler test fixture is shown in Figure 4-8. Simple microstrip transmission was put into the coupler test fixture to calibrate out the insertion loss of the test fixture. The coupler is then installed into the fixture for testing.

4.2.3 Coupler Test Data

The measured insertion loss of the coupler is shown in Figure 4-9. For an ideal coupler with no loss, the direct and coupled output arms should have half the input power (or -3 dB). Thus, the insertion loss of the coupler is approximately 0.5 dB. The return loss and the isolation of the coupler, shown in Figure 4-10, is approximately 15 dB, which is quite adequate for the balanced amplifiers.

4.3 CARRIERS

The device carrier assembly was designed by TRW in conjunction with Raytheon. The details of the interface requirements between the device and the carrier assembly were worked out and agreed upon jointly. To minimize

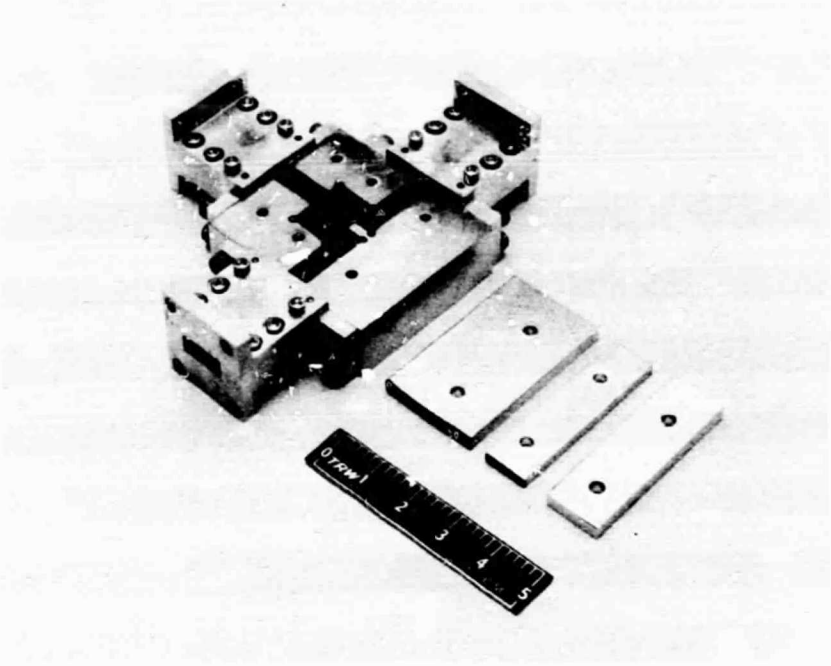


Figure 4-8. Coupler Test Fixture

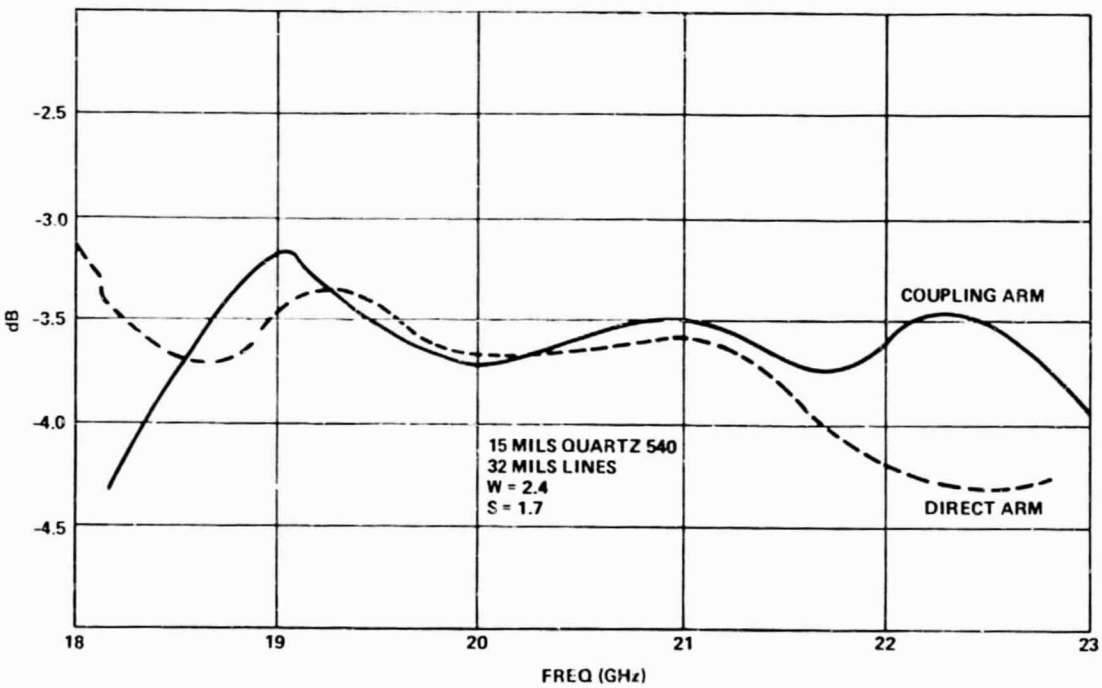


Figure 4-9. 3 dB Coupler Direct and Coupled Arm Response

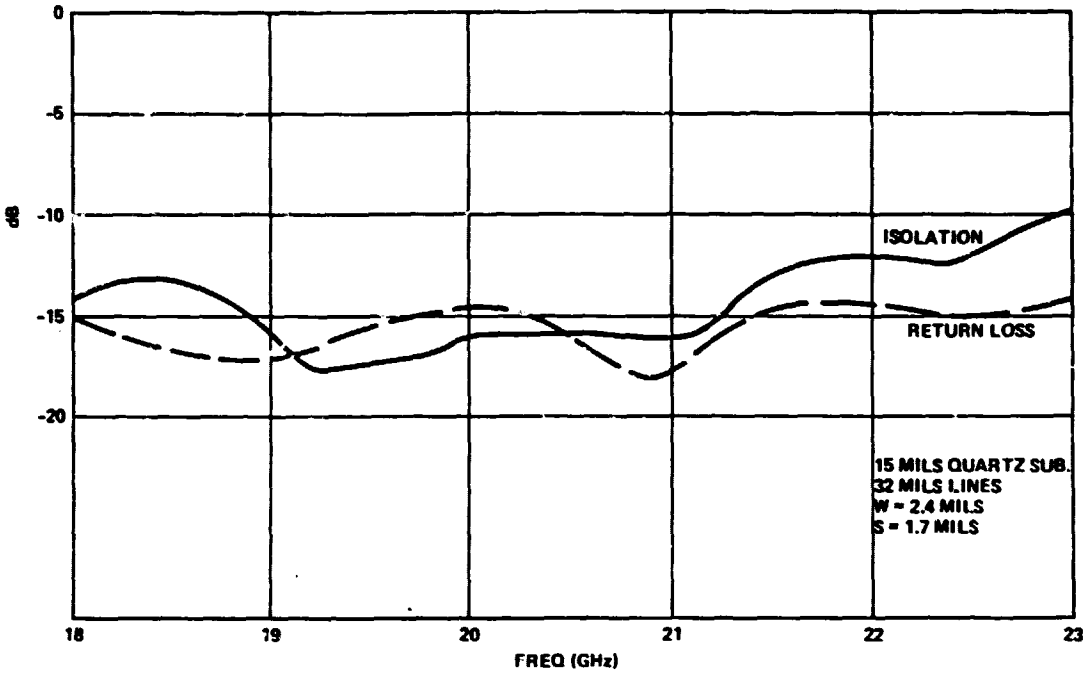


Figure 4-10. Coupler Isolation and Return Loss

parasitics, the dimensions of the carrier assembly and its assembly procedures are extremely critical. Since the carriers are used for power devices, thermal characteristics must be carefully evaluated.

4.3.1 FET Carrier Design

Each carrier assembly consists of the FET, a coupler-carrier, an input-matching substrate, output-matching substrate, and an Invar shim for each of the quartz substrates. Figure 4-11 is a drawing of the FET carrier, which is made of copper for maximum heat conduction. The FET is mounted to the ridge in the carrier with gold-germanium solder. The ridge is slightly wider than the device to preclude the possibility of interference with the substrates. The quartz substrates are soldered to Invar shims, which are then screwed to the carrier using the two tapped holes on each side of the ridge. Invar is used because it has a very low thermal expansion coefficient, making it a fairly close match to quartz which has a coefficient of practically zero. The substrates cannot be soldered directly to the carrier because the difference in thermal expansion between

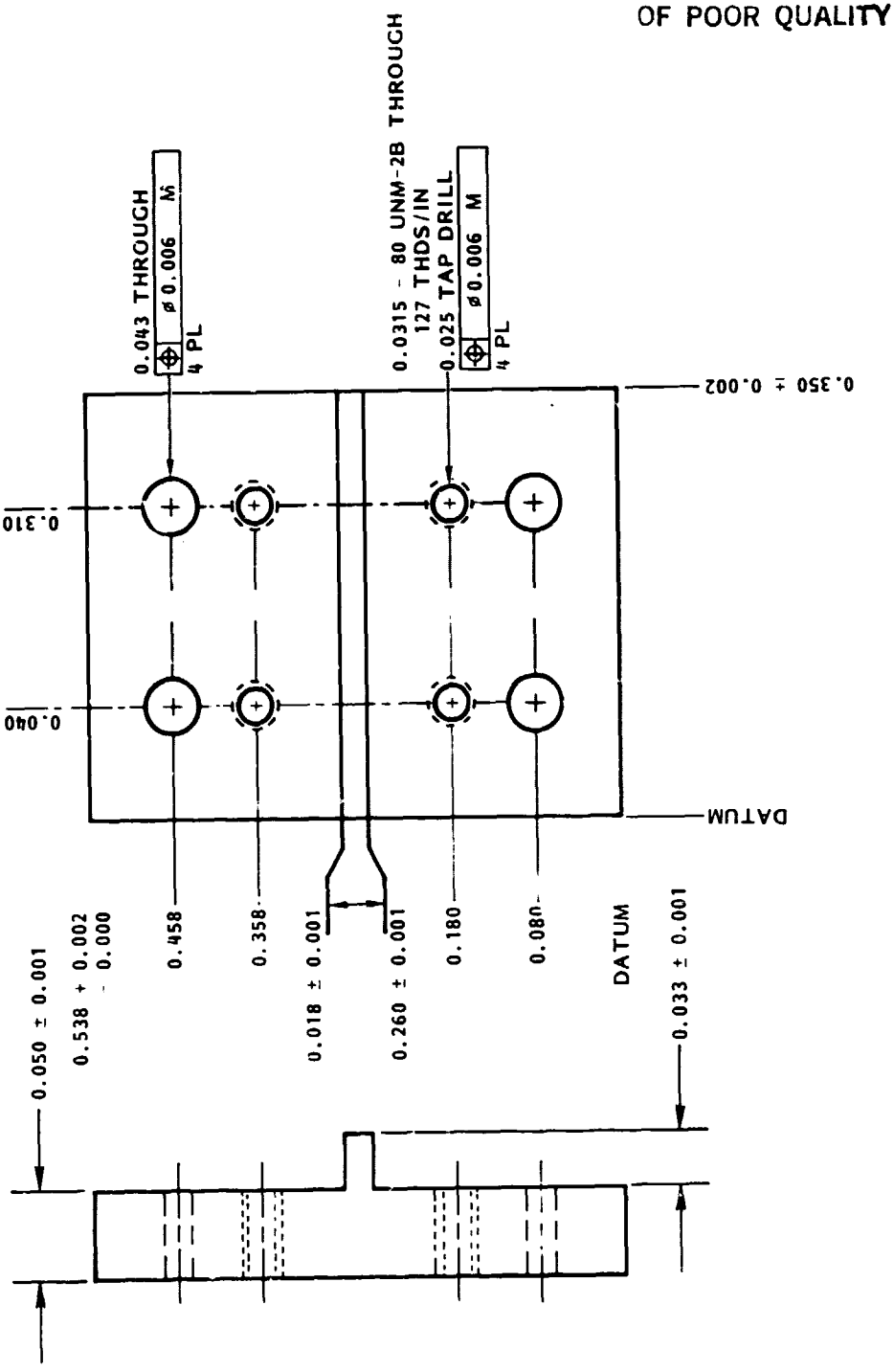


Figure 4-11. FET Carrier

copper and quartz would cause the substrates to crack or fall off as the assembly cools from the soldering process. Use of the shims also facilitates replacement of the substrates should it become necessary. The height of the ridge in the carrier is dimensioned so that when assembled, the top of the FET and the top surface of the substrates are coplanar. This results in the shortest possible bond wire lengths, thereby minimizing their inductance. It is critical that the corner at the bottom of the ridge have a minimum radius, otherwise the substrates cannot be pushed up against the ridge.

4.3.2 Thermal Considerations

A thermal analysis of the assembly was performed using a computer model of the carrier. The program determined that the thermal resistance from a 0.015-inch square area on the top of the ridge to the bottom of the carrier base is 5°C/W; about 85 percent of this resistance is in the ridge. The thermal resistance of the gold-germanium preform was calculated to be approximately 1°C/W. There is also resistance from the bottom of the carrier to the housing floor. Assuming a 0.0005-inch average air gap between the two surfaces, this resistance should be about 4°C/W. Given a device junction to base resistance of 20°C/W the total thermal resistance from junction to housing is 30°C/W.

4.3.3 Carrier Assembly

The device carrier assembly is shown in Figure 4-12. The input match quartz substrates and the output matching quartz substrate have already been soldered using Au-Ge eutectic in a belt furnace under forming gas atmosphere. This ensures a uniform solder flow and a void-free joint which could otherwise result in losses to the copper block with Invar shim sandwiched in-between for thermal expansion compatibility.

Figure 4-13 shows the microstrip circuitry on quartz substrate. The input and the output matching networks have the same configuration, except they are mirror image to each other. The center line with a gap at the left-hand side of the figure is the 50-ohm transmission line. A chip capacitor is placed across the gap to block the dc bias to the input (or output) connectors. The pie-shaped network is for low-pass filtering of

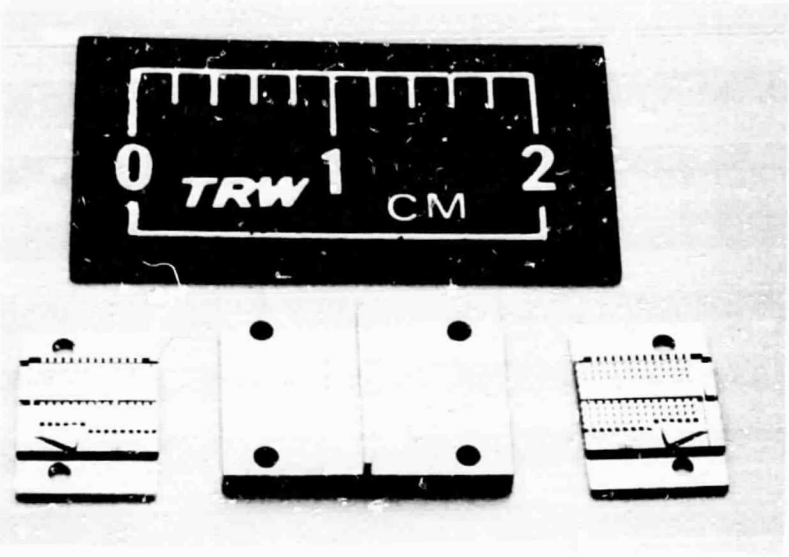


Figure 4-12. Device Carrier Assembly

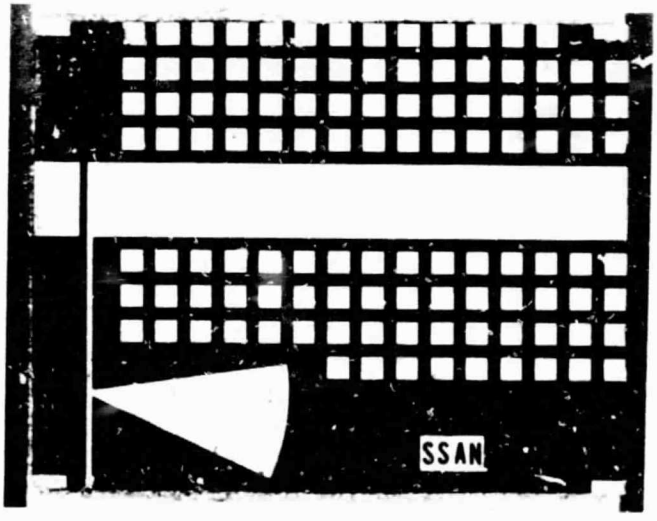


Figure 4-13. 20-GHz FET SSA
New Substrate for Input/
Output Matching Network

the bias network. The square pads are to be bonded-in with gold ribbons for matching circuits to match to the FET. Only parts of the square pads are used as appropriate depending on the input/output impedances of the FET. However, since for each type of FET (e.g., the 1/4 W FETs) the input/output impedances are nominally similar, the determination of which pads to use follow a general pattern. Thus, after one of the amplifiers has been tuned-up and optimized, it is relatively simple to repeat the procedure for subsequent amplifiers using the same device-type.

4.4 DEVICE TYPE

Since the amplifier chains operate at various power levels, smaller power devices should be used at the input where the operating power level is quite low. There are a number of advantages in choosing devices with appropriate power handling capabilities. First, the devices with high power handling capabilities generally cost more since the active areas of the FET is greatly increased, thus lowerig the yield in processing these devices. Secondly, the high power devices have lower input impedances making broadband matching difficult. Generally, when the operating power level is being pushed to the limit of the device power handling capability, the gain of the amplifier is lower because usually the amplifier is operated in a saturated mode. Thus, the stages operating at lowre power level should be made to operate with higher gain to minimize the number of stages required to meet the overall gain requirements. Lastly, the dc-to--RF efficiency will be greatly reduced by using high power devices for low power operation since the high power devices have to be biased at their optimum bias conditions.

The FET devices developed by Raytheon under this contract have been described in Section 3 of this report. There are three specific devices with power handling capabilities of 1/4 W, 1/2 W and 1 W respectively. These devices are judiciously placed in the POC model to give the optimum performances.

TRW has also taken theliberty to investigate other commercially available devices that can readily be used with the device carrier designed for the POC model.

The power handling capability of the devices is a function of total gate-width, GaAs active channel doping and thickness, and the dc bias conditions. The difference in the devices is in the active channel material which determines the drain saturation current at zero gate bias, Id_{ss}. For example, the low noise DXL2503, developed by Dexcel, has a thin channel with low I_{dss} (40 mA). It is typically biased at 20 to 25 mA drain current and has a saturated output power of less than 10 mW. The power device, DXL3503, has a thicker channel width, with an I_{dss} of 110 mA. Typically biased to 60 mA, it can produce over 50 mW. Both Dexcel and Avantek have developed devices with approximately 150 μm gate width.

TRW opted to use the commercially available Avantek 8041 devices for the first two single-ended stages of the driver module, mainly because these devices provide higher achievable gain per stage. The data sheets of the Avantek devices are shown at the end of Section 4.4 (Figure 4-14). Note that the Avantek devices provided close to 8 dB per stage as compared to the 4 dB budgeted.

Raytheon devices as described in Section 3 are also used. The 1/4 W, 1/2 W and 1 W devices are used as shown in Figure 4-15 and 4-16 for the driver amplifier module and the power amplifier module, respectively.

4.5 SINGLE-ENDED AMPLIFIER

4.5.1 Device S-Parameters

Normally an amplifier is designed by measuring the large signal S-parameters of the device. The input matching network is then designed based on the $|S_{11}|$ of the device, and the output matching network based on the $|S_{22}|$ of the device. The operating frequency for this amplifier (17.7 to 20.2 GHz) prevents the accurate determination of the S-parameters of the FET for the following reasons:

1) It takes two sets of test equipment to cover the band of 17.5 to 20.2 GHz. One set covers 12 to 18 GHz and another set covers 18 to 26.5 GHz.

2) The basic network analyzers cover only the 12 to 18 GHz band, although newer equipment does allow the network analyzer to operate at higher frequencies.

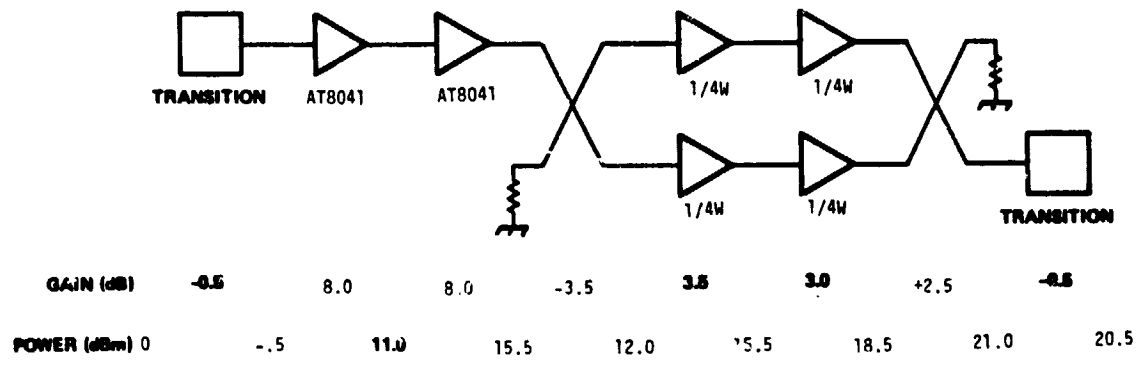


Figure 4-14. Power Gain Budget of Driver Amplifier

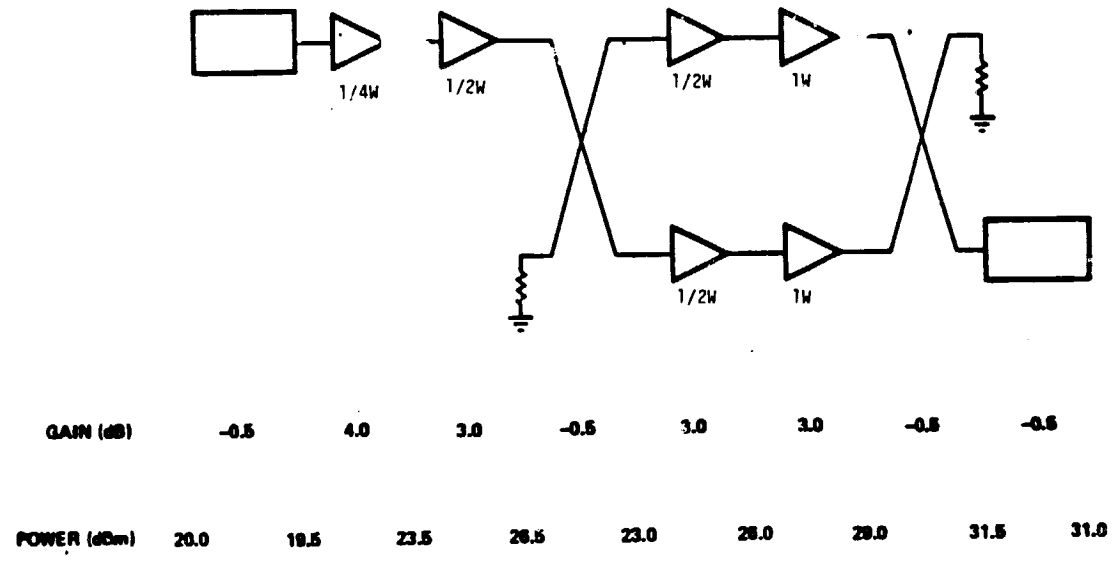


Figure 4-15. Power Gain Budget of Power Amplifier

AT-8041
10-26 GHz, Small Signal
Gallium Arsenide FET Chip

This part will be obsoleted by January, 1984. Consult the factory for current availability and recommended replacements.

FEATURES

- **2.8 dB NF, 7.0 dB Gain @ 18 GHz***
- **2.0 dB NF, 10 dB Gain @ 12 GHz***
- **1.7 dB NF, 13 dB Gain @ 8 GHz***
- **+8 dBm P_o (1 dB G.C.P.) @ 12 GHz**
- **Excellent Gain and Noise Flatness vs. I_{ds}**
- **Wide Dynamic Range**
- **All Gold-Based Metallization**

DESCRIPTION

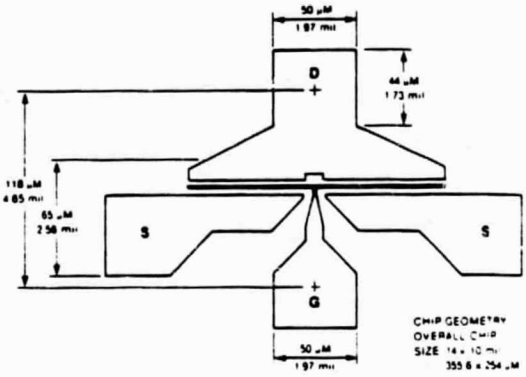
The AT-8041 is a gallium arsenide, n-channel metal semiconductor field effect transistor (GaAs FET) with a 0.5 μm-length Schottky barrier gate. It is designed for high gain, low noise amplification in both narrowband communications and radar amplifiers and in wideband electronic defense applications in the 10 to 26 GHz frequency range.

Among the performance features of this GaAs FET are the particularly flat curves for insertion power gain (S_{21}^2), maximum available (MAG) and noise figure vs. drain current, from relatively low bias levels through I_{DSS}. This simplifies the bias requirements of amplifier stages using the AT-8041.

All metallization, including the gate, in the AT-8041 uses a system of gold and refractory metals. This eliminates the corrosion, intermetallic growth and burn-out problems associated with other GaAs FET metal systems helping to assure long term reliability under severe operation conditions.

For microwave hybrid construction at frequencies up to 26 GHz, the AT-8041 is an unpackaged 10 x 14 mil chip. Its gold metal system provides excellent bond strength and assures compatibility with the wirebonding techniques used in thin or thick film hybrid circuit construction.

OUTLINE DRAWING:



AVANTEK M104 CHIP

TYPICAL COMMON SOURCE OPERATING CHARACTERISTICS (T_A = 25°C)

Symbol	Parameters/Test Conditions	Freq.	Value
NF_O	Spot Noise Figure: V_{DS} = 3V, I_{DS} = 8.0 mA	6.0 GHz 12.0 GHz 18.0 GHz	1.7 dB 2.0 dB 2.8 dB
G_A	Gain at Optimum Noise Figure: V_{DS} = 3V, I_{DS} = 8.0 mA	6.0 GHz 12.0 GHz 18.0 GHz	13 dB 10 dB 7 dB
MAG	Maximum Available Gain: V_{DS} = 3V, I_{DS} = 30.0 mA	12.0 GHz	14 dB
$P_{1\,dB}$	Output Power at 1 dB Gain Compression: V_{DS} = 5V, I_{DS} = 30.0 mA	12.0 GHz	+8 dBm

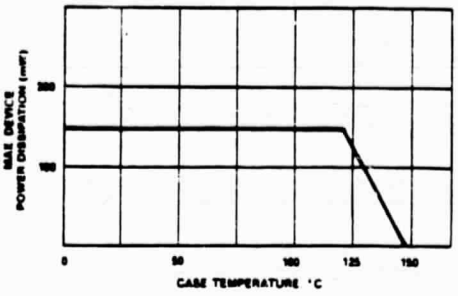
Avantek Inc • 3175 Bowers Ave • Santa Clara, Ca. 95051 • General Office (408) 727-0700 • Customer Service & Component Sales (408) 496-6710 • TWX 910-339-9274 • TELEX 34-6337

Figure 4-16. AVANTEK Data for 10 to 26 GHz Small Signal GaAs FET Chip

ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$)

Parameter	Symbol	Limit
Drain-Source Voltage	V_{DS}	+ 5V
Gate-Source Voltage	V_{GS}	– 4V
Drain Current	I_{DS}	50 mA
Continuous Dissipation	P_T ($T_{case} = 25°C$)	150 mW
Channel Temperature	T_{ch}	150°C
Storage Temperature	T_{stg}	– 65 to 150°C
Thermal Resistance	θ_{jc}	200°C/watt

MAXIMUM POWER DISSIPATION vs. CASE TEMPERATURE

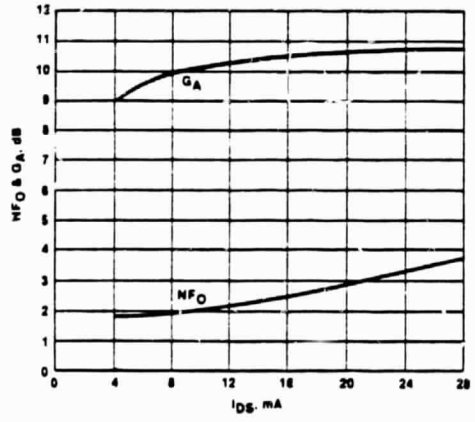


TYPICAL DC CHARACTERISTICS ($T_A = 25°C$)

Parameter	Symbol	Value	Test Conditions
Transconductance	G_M	20 mmho	$V_{DS} = 3V$, $V_{GS} = 0V$
Saturated Drain Current	I_{DSS}	30 mA	$V_{DS} = 3V$
Pinchoff Voltage	V_p	– 2V	$V_{DS} = 3V$, $I_{DS} = 1$ mA

TYPICAL PERFORMANCE CURVES ($T_A = 25°C$)

SPOT NOISE FIGURE (NF_O) AND ASSOCIATED GAIN (G_A) vs. I_{DS}
$V_{DS} = +3V$, FREQ = 12.0 GHz



SPOT NOISE FIGURE (NF_O) AND ASSOCIATED GAIN (G_A) vs. FREQUENCY
$V_{DS} = +3$ VOLTS $I_{DS} = 20\%$ I_{DS} (≅10 mA)

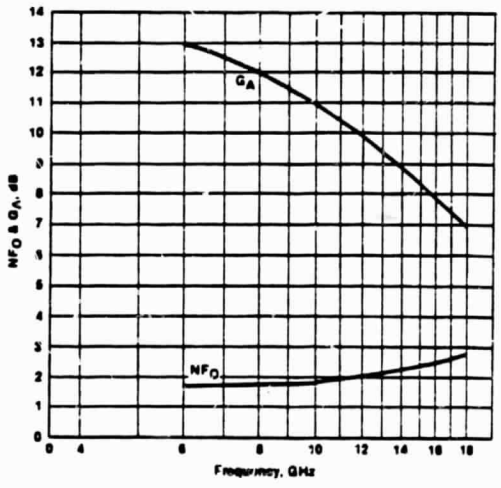
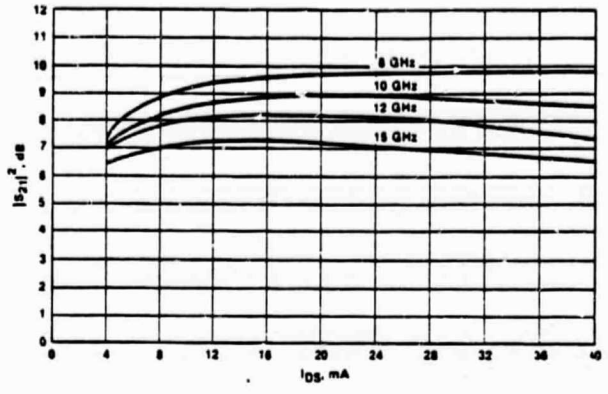


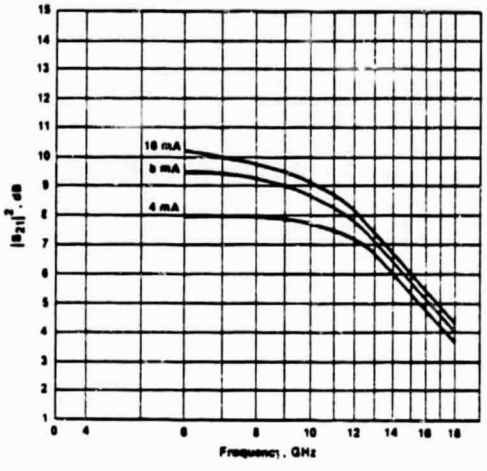
Figure 4-16. AVANTEK Data for 10 to 26 GHz Small Signal GaAs FET Chip (Contined)

TYPICAL PERFORMANCE CURVES (T_A = 25°C) (Cont.)

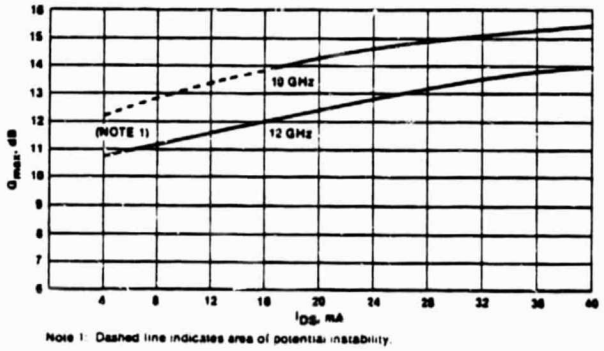
INSERTION POWER GAIN ($|S_{21}|^2$) VS. I_{DS} AND FREQUENCY
@ V_{DS} = 3V



INSERTION POWER GAIN ($|S_{21}|^2$) VS. FREQUENCY
AND I_{DS} AT V_{DS} = 3V



MAXIMUM AVAILABLE GAIN (G_{max}) VS. I_{DS}
V_{DS} = 3V



Note 1: Dashed line indicates area of potential instability.

Figure 4-16. AVANTEK Data for 10 to 26 GHz Small Signal GaAs FET Chip (Contined)

TYPICAL SCATTERING PARAMETERS*

Bias = 3.0V, 8 mA

...-8041
S—MAGN AND ANGLES

FREQ	11		21		12		22	
6000	.83	– 38°	3.90	132°	.048	63°	.87	– 12°
7000	.79	– 49.5	4.00	124	.048	60	.86	– 14.5
8000	.68	– 65	4.15	115	.051	56	.84	– 17.
9000	.63	– 79	4.40	107	.055	52	.83	– 20
10000	.64	– 88	4.50	99	.064	48	.81	– 22
11000	.63	– 96	4.50	89	.073	41	.79	– 24.5
12000	.62	– 104	4.50	78	.082	35	.76	– 27
13000	.57	– 114	4.65	68	.091	27	.73	– 29
14000	.54	– 124	4.50	60	.095	20	.70	– 30.5
15000	.47	– 147	4.30	50	.102	14	.66	– 31.5
16000	.41	– 172	4.10	39	.109	8	.63	– 36
17000	.40	169	3.70	31	.117	2	.60	– 37
18000	.42	146	3.30	23	.120	– 4	.58	– 39
19000	.45	131	2.90	15	.125	– 10	.55	– 40
20000	.50	120	2.60	5	.129	– 14	.53	– 41

AT-8041

Bias = 3.0V, 30 mA

S—MAGN AND ANGLES

FREQ	11		21		12		22	
6000	.73	– 58°	4.31	122°	.039	80°	.85	– 11°
7000	.69	– 71	4.35	114	.039	77	.84	– 14
8000	.60	– 89	4.40	106	.040	73	.82	– 16
9000	.57	– 105	4.53	98	.043	70	.80	– 20
10000	.60	– 116	4.60	91	.044	66	.79	– 21
11000	.60	– 126	4.75	81	.047	62	.77	– 23
12000	.62	– 131	4.80	71	.050	58	.75	– 26
13000	.58	– 138	4.78	61	.061	55	.74	– 28
14000	.56	– 145	4.82	54	.063	51	.67	– 30
15000	.50	– 155	4.41	44	.072	48	.64	– 31
16000	.47	171	4.20	34	.077	44	.60	– 33
17000	.48	157	3.75	26	.081	42	.58	– 35
18000	.49	136	3.35	17	.088	40	.56	– 36
19000	.53	123	2.91	11	.096	37	.52	– 37
20000	.55	114	2.60	2	.110	33°	.50	– 39

CHIP CODE M104

*S-parameters include bond wire inductance and are measured in the Avantek TF-001 test fixture. Test fixtures are available (see page 176).

Figure 4-16. AVANTEK Data for 10 to 26 GHz Small Signal GaAs FET Chip (Continued)

3) The 12 to 18 GHz test equipment generally operates with coaxial connector interfaces, whereas the amplifier has waveguide input/-output interfaces. the S-parameter measurements will incur additional errors by introducing additional coax-to-waveguide transitions.

4) With the existing waveguide-to-microstrip transition and the carrier configuration, extremely long transmission elements are introduced at both the input and output ports of the FET. This also makes the measurements less reliable.

5) Large signal characterization of the device requires tuning the device to optimum large signal conditions and the measurements of the impedance presented by the tuner. At 20 GHz, the impedance of the device is so low that off-substrate tuners with even their slight associated losses are unable to achieve the high impedance transformation ratio necessary to tune for optimum power output.

Attempts have been made to measure the device S-parameters without the waveguide-to-microstrip transition. Instead, special tests fixtures were developed to connect the carrier assembly to the 12 to 18 GHz test equipment with coax-to-microstrip connectors. The S-parameters were measured with this setup from 12 to 18 GHz. The S-parameters were then extrapolated to 20.2 GHz. The matching networks were designed based on the extrapolated S-parameters. However, the designs proved to be vastly inadequate due to the inaccuracy of the S-parameter values.

To tune the amplifier for optimum gain bandwidth, special provisions are incorporated to the input and output matching network by making them flexible to tune. they are also designed for different types of devices; i.e., the same design can be used for the 1/4 W, 1/2 W, and 1 W devices. The input/output matching networks are shown in Figure 4-13. These matching substrates also include bias and decoupling networks.

4.5.2 Device Operating Conditions

The POC model uses a total of 60 FET devices. Although each FET has its nominal operating conditions, the bias conditions of each device are optimized to achieve the final POC performance characteristics. Figure 4-17 is a block diagram summarizing the various types of devices used.

For convenience, every device is numerically numbered. Table 4-1 summarizes the operating condtions of each device respectively.

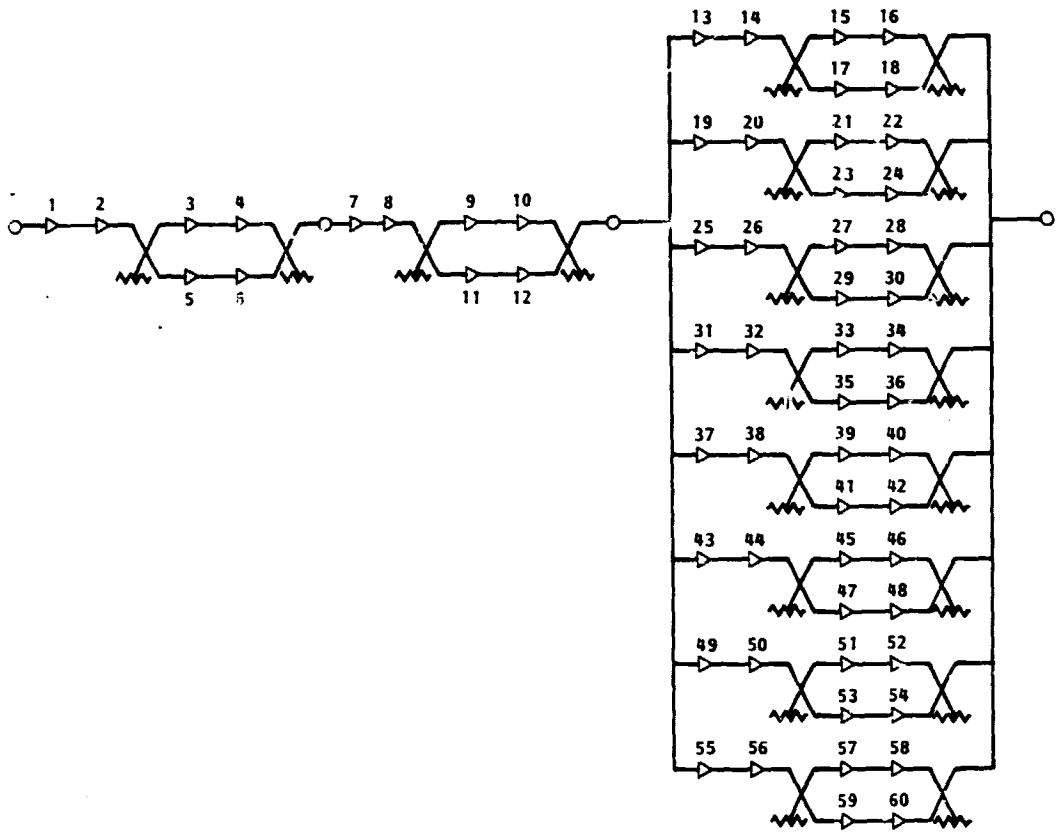


Figure 4-17. POC Block Diagram with Device Designation

Table 4-1. Device Operating Conditions

MODULE #	DEV. NO.	DEVICE DESIGNATION	DEVICE TYPE	OPERATING CONDITIONS		
				V_D	V_G	I_D
1	1	AV1	Avantek L.N.A.	5	-0.5V	10 mA
1	2	AV2	Avantek L.N.A.	5	-0.7V	9 mA
1	3	A44	Raytheon 1/4W	9.8	-2.5V	60 mA
1	4	A34	" 1/4W	9.8	-2.0V	67 mA
1	5	A3	" 1/4W	9.8	-2.4V	64 mA
1	6	A4	" 1/4W	9.8	-2.5V	64 mA
2	7	B6	" 1/2W	9.8	-1.6V	127 mA
2	8	B41	" 1/2W	9.8	-2.1V	140 mA
2	9	B31	" 1/2W	9.8	-2.2V	134 mA
2	10	C33	" 1W	9.8	-2.7V	251 mA
2	11	B32	" 1/2W	9.8	-2.4V	274 mA
2	12	C7	" 1W	9.8	-2.5V	231 mA
3	13	B33	" 1/2W	9.8	-3.0V	127 mA
3	14	BR3	" 1/2W	9.8	-1.7V	143 mA
3	15	B44	" 1/2W	9.8	-2.3V	140 mA
3	16	B5	" 1/2W	9.8	-2.1V	141 mA
3	17	C50	" 1W	9.8	-1.6V	210 mA
3	18	C8	" 1W	9.8	-1.8V	260 mA
4	19	AR1	" 1/4W	9.8	-2.6V	67 mA
4	20	B39	" 1/2W	9.8	-2.5V	140 mA
4	21	B59	" 1/2W	9.8	-1.1V	125 mA
4	22	B8	" 1/2W	9.8	-1.2V	152 mA
4	23	C39	" 1W	9.8	-1.8V	251 mA
4	24	C12	" 1W	9.8	-2.4V	258 mA
5	25	A45	" 1/4W	9.8	-2.5V	70 mA
5	26	B34	" 1/2W	9.8	-2.0V	145 mA
5	27	B55	" 1/2W	9.8	-1.1V	297 mA
5	28	B4	" 1/2W	9.8	-2.6V	140 mA
5	29	C54	" 1W	9.8	-2.2V	254 mA
5	30	C24	" 1W	9.8	-2.2V	255 mA

Table 4-1. Device Operating Conditions (Continued)

MODULE #	DEV. NO.	DEVICE DESIGNATION	DEVICE TYPE	OPERATING CONDITIONS V_D	V_G	I_D
6	31	B52	Raytheon 1/2W	9.8	-2.8V	140 mA
6	32	B43	" 1/2W	9.8	-2.0V	140 mA
6	33	B46	" 1/2W	9.8	-2.0V	140 mA
6	34	B10	" 1/2W	9.8	-1.3V	136 mA
6	35	C52	" 1W	9.8	-2.3V	250 mA
6	36	C9	" 1W	9.8	-2.1V	270 mA
7	37	C45	" 1/2W	9.8	-2.2V	140 mA
7	38	B36	" 1/2W	9.8	-2.0V	138 mA
7	39	B62	" 1/2W	9.8	-1.3V	141 mA
7	40	BR4	" 1/2W	9.8	2.0V	134 mA
7	41	C35	" 1W	9.8	-2.1V	266 mA
7	42	C0	" 1W	9.8	-2.0V	285 mA
8	43	B37	" 1/2W	9.8	-2.7V	124 mA
8	44	B67	" 1/2W	9.8	-1.8V	127 mA
8	45	B65	" 1/2W	9.8	-1.9V	160 mA
8	46	B17	" 1/2W	9.8	-2.5V	153 mA
8	47	C42	" 1W	9.8	-1.8V	280 mA
8	48	C9	" 1W	9.8	-1.9V	278 mA
9	49	B48	" 1/2W	9.8	-2.4V	144 mA
9	50	B64	" 1/2W	9.8	2.3V	148 mA
9	51	BR1	" 1/2W	9.8	-1.75V	134 mA
9	52	C46	" 1W	9.8	-1.5V	250 mA
9	53	BR2	" 1/2W	9.8	-1.7V	135 mA
9	54	C18	" 1W	9.8	-2.0V	280 mA
10	55	B39	" 1/2W	9.8	-2.5V	140 mA
10	56	B53	" 1/2W	9.8	-1.4V	147 mA
10	57	B63	" 1/2W	9.8	-2.5V	154 mA
10	58	C53	" 1W	9.8	-2.4V	252 mA
10	59	B16	" 1/2W	9.8	-2.0V	138 mA
10	60	C23	" 1W	9.8	-2.3V	253 mA

4.5.3 Amplifier Designs

As mentioned in Section 4.4, different device types are used for the POC model. The basic unit for the POC model is the cascaded two-stage single-ended amplifiers. Three of these basic units are assembled into a module; i.e., two of these basic units are combined into a four-FET balanced amplifier preceded by another basic unit of the cascaded single-end amplifiers. In this section, the results of the various combinations of the cascaded single-ended amplifiers are described.

4.5.3.1 Single-Stage Single-Ended Amplifiers

There are four different types of devices used in the POC model: namely, the Avantek AT8041, the Raytheon 1/4 W, the Raytheon 1/2 W, and the Raytheon 1 W FETs. Amplifiers using these devices all have the same carrier. The FET is mounted to the ridge of the carrier with gold-germanium solder. The ridge is slightly wider than the device to preclude interference with the substrates. The quartz substrates are soldered to Invar shims, whicha re then screwed to the carrier using the two tapped holes on each side of the ridge. The height of the ridge is dimensioned so that, when assembled, the top of the FET and the top surfaces of the substrates are coplanar. This results in the shortest possible bond wire lengths from the FET to the substrates, minimizing their inductances.

4.5.3.2 Single Stage Single-Ended Amplifier Test Fixture

The assembled carrier with input and output matching networks is then installed in the single-stage single-ended amplifier test fixture shown in Figure 4-18. An additional transmission line each between the carrier and the input and output waveguide-to-microstrip transitions were necessary because the dimensions of the housing for the amplifier stages support higher order waveguide modes, thus requiring waveguide mode suppressors to alleviate these higher-order modes. (The design of the waveguide mode suppressors is described in Section 4.13.) The transitions, the waveguide mode suppressors, and the carrier assembly are bolted together; thus, individual carrier assembly can be optimized in the test fixture and be easily removed from the fixture once it is tuned up. The optimized amplifier stage is then integrated into the final POC model.

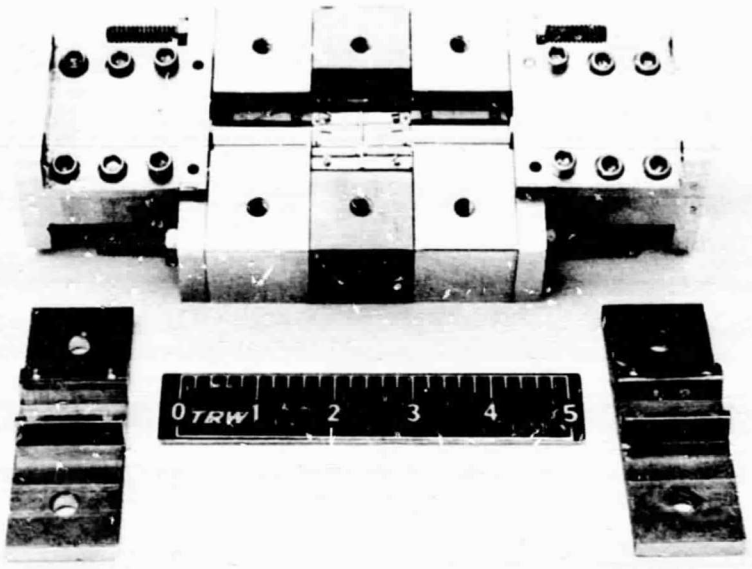


Figure 4-18. Single-Stage Test Fixture

4.5.3.3 Single-Stage Single-Ended Amplifier Test Data

The single-ended amplifier stage using the Avantek AT8041 FET is tuned up for optimum performance characteristics. The tuning elements, namely the square pads, are bonded into the matching network with gold ribbons through (thermo-electric bonding). The frequency response ar the return loss of the amplifier is shown in Figure 4-19. The P_{in}/P_{out} response of the amplifier is shown in Figure 4-20.

The single-ended amplifier stage using the Raytheon 1/4 W FET is tuned up the same way and its frequency response is shown in Figure 4-21. The P_{in}/P_{out} response is shown in Figure 4-22.

The frequency response of the Raytheon 1/2 W FET single-ended amplifier is shown in Figure 4-23 and the P_{in}/P_{out} in Figure 4-24.

The frequency response of the Raytheon 1 W FET single-ended amplifier is shown in Figure 4-25 and the P_{in}/P_{out} in Figure 4-26.

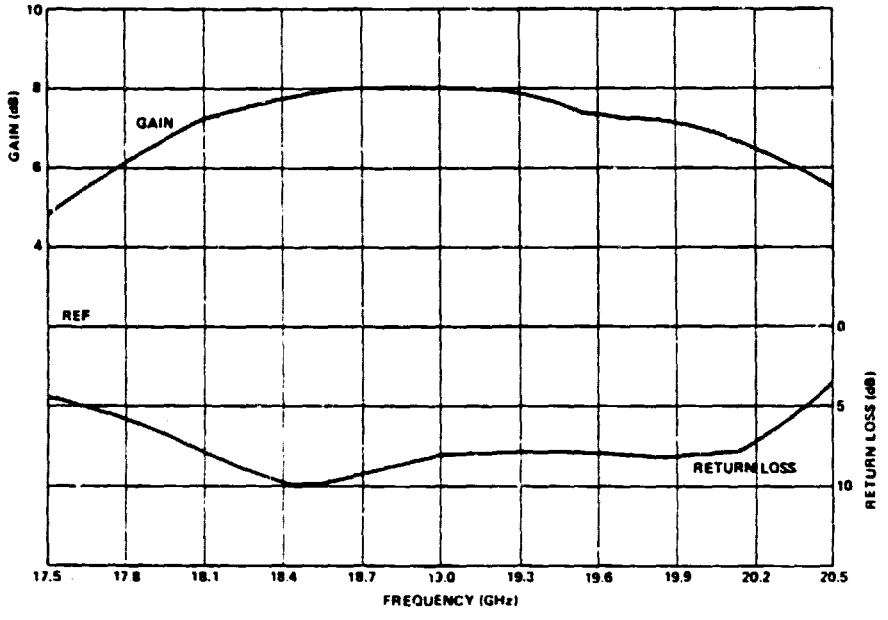


Figure 4-19. Frequency Response and Return Loss of Avantek AT8041 Stage

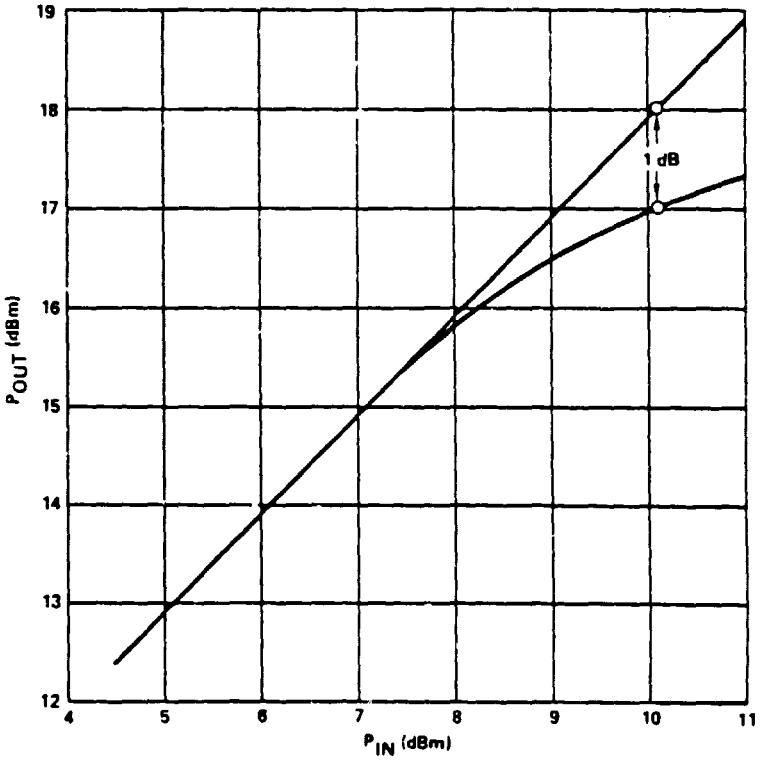


Figure 4-20. P_{in}/P_{out} Avantek AT8041 Device

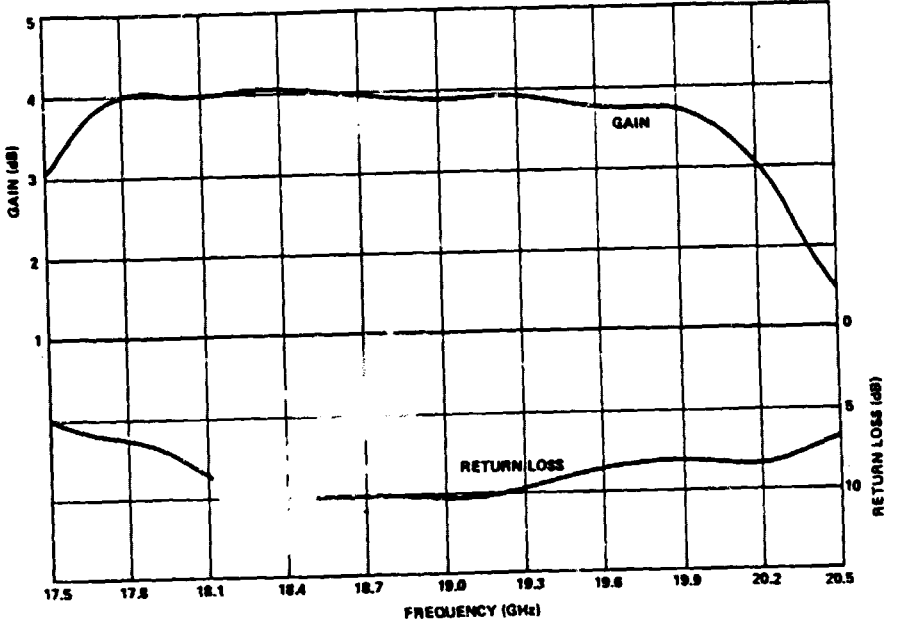


Figure 4-21. Frequency Response and Return Loss of 1/4 Watt Stage

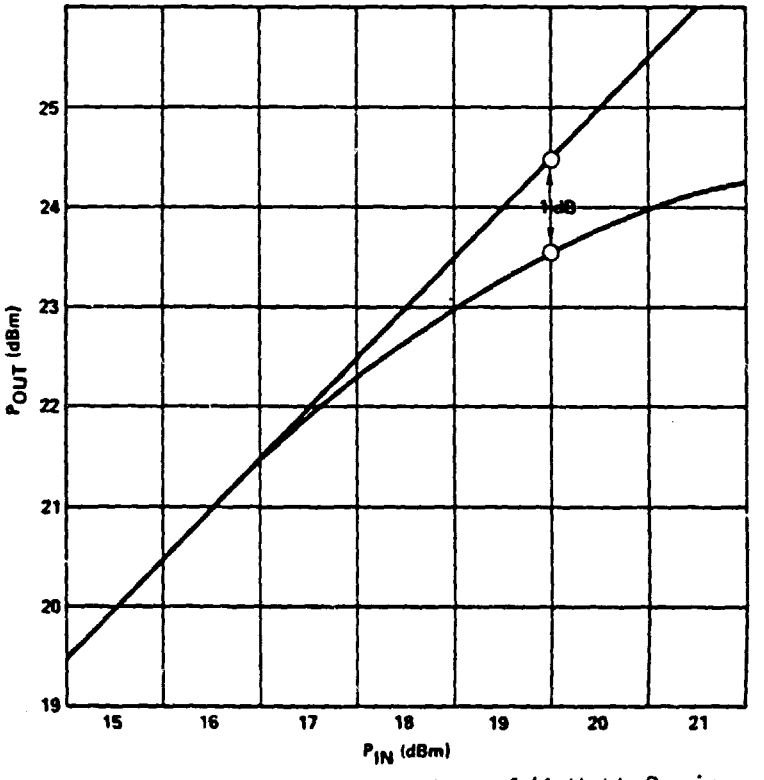


Figure 4-22. P_{in}/P_{out} Raytheon 1/4 Watt Device

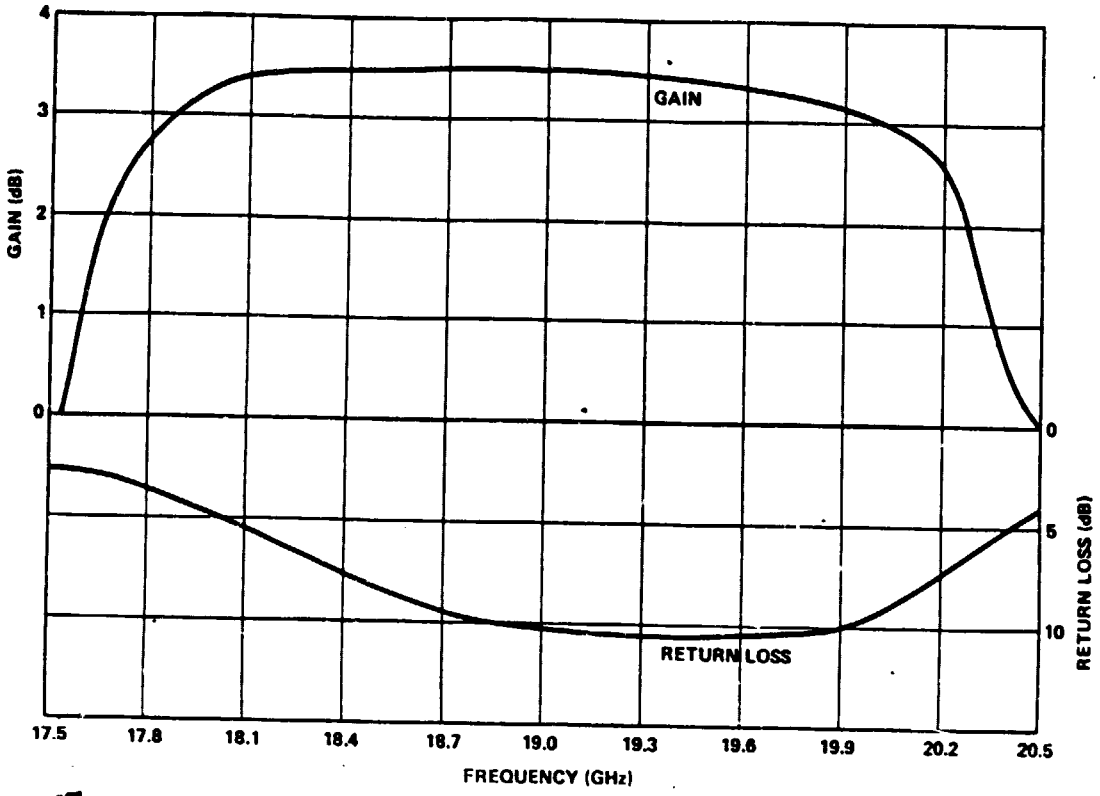


Figure 4-23. Frequency Response and Return Loss of 1/2 Watt Stage

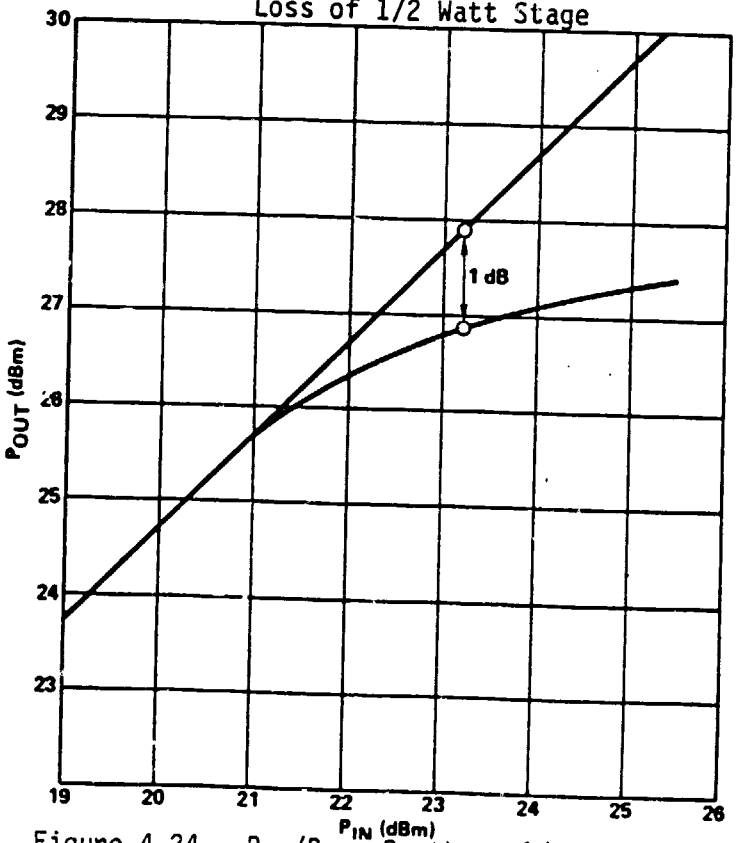


Figure 4-24. P_{in}/P_{out} Raytheon 1/2 Watt Device

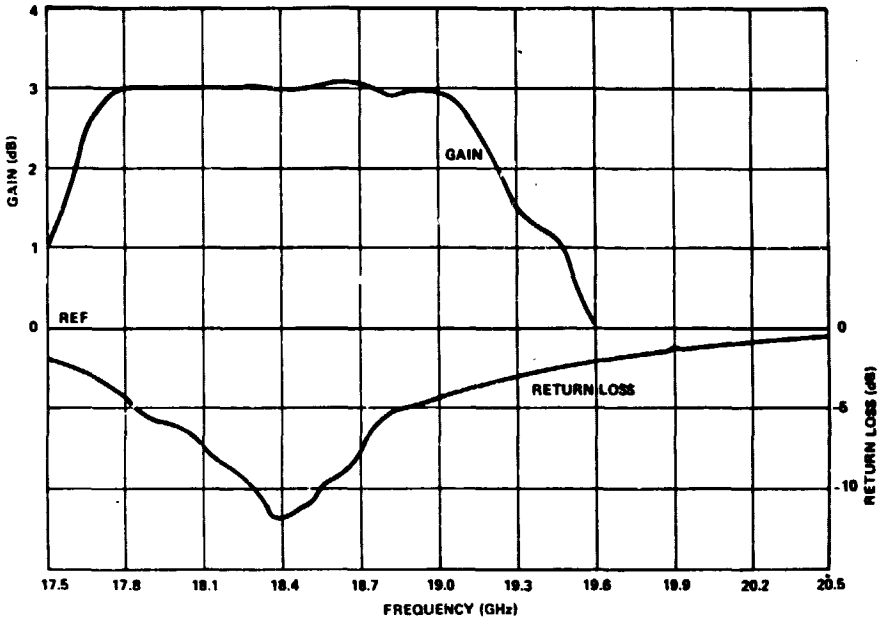


Figure 4-25. Frequency Response and Return Loss of 1 Watt Stage

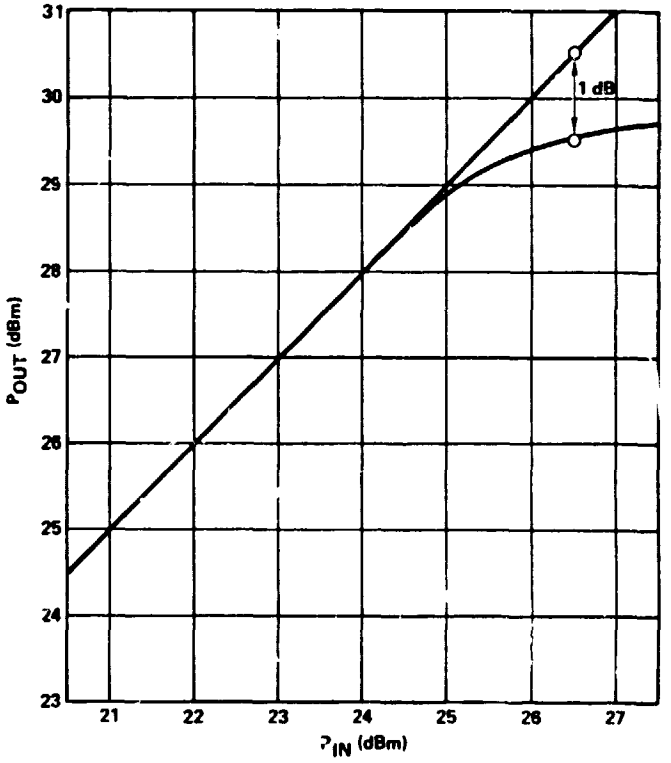


Figure 4-26. P_{in}/P_{out} Raytheon 1 Watt Device

4.5.3.4 Cascaded Single-Ended Amplifiers

There are four different combinations of cascaded single-ended amplifiers used for the POC model. The driver module consists of a cascaded amplifier of two single-ended stages with both stages using the Avantek AT8041 FETs, followed by the balanced configuration using two cascaded amplifiers of two single-ended stages, with both stages using the Raytheon 1/4 W FETs. The power module consists of a cascaded amplifier of two single-ended stages with one stage using the Raytheon 1/4 W FET and the other stage using the Raytheon 1/2 W FET, followed by the balanced configuration using two cascaded amplifiers of two single-ended stages, with one stage using the Raytheon 1/2 W FET and the other stage using the Raytheon 1 W FET. Thus, the four combinations of cascaded amplifiers are:

- Avantek-Avantek
- Raytheon 1/4 W-Raytheon 1/4 W
- Raytheon 1/4 W-Raytheon 1/2 W
- Raytheon 1/2 W-Waytheon 1 W.

4.5.3.5 Cascaded Single-Ended Amplifier Test Fixture

The test fixture for the cascaded single-ended amplifiers is the same as that used for the single-stage amplifier. The only difference is substitution of the single stage single-ended amplifier assembly with the cascaded single-ended amplifier assembly.

4.5.3.6 Cascaded Single-Ended Amplifier Test Data

Although the single-stage single-end amplifiers were optimized, the cascaded single-ended amplifiers had to be retuned slightly for optimum performance characteristics to take into account interaction between the two stages.

The frequency response and the P_{in}/P_{out} response of the Avantek-Avantek pair are shown in Figures 4-27 and 4-28, respectively.

The frequency response and the P_{in}/P_{out} response of Raytheon's 1/4 W-1/4 W pair are shown in Figures 4-29 and 4-30, respectively.

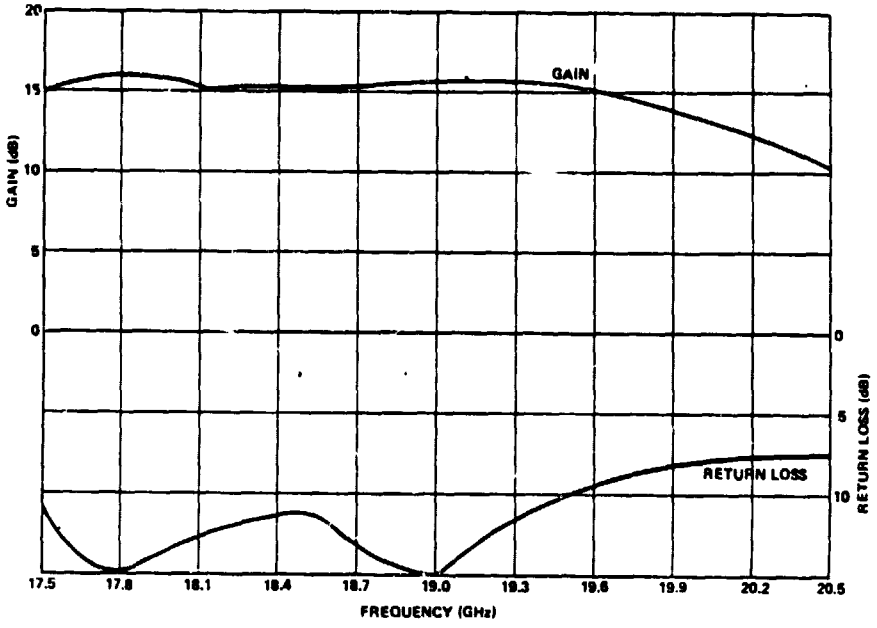


Figure 4-27. Frequency Response and Return Loss of Avantek Cascaded Pair

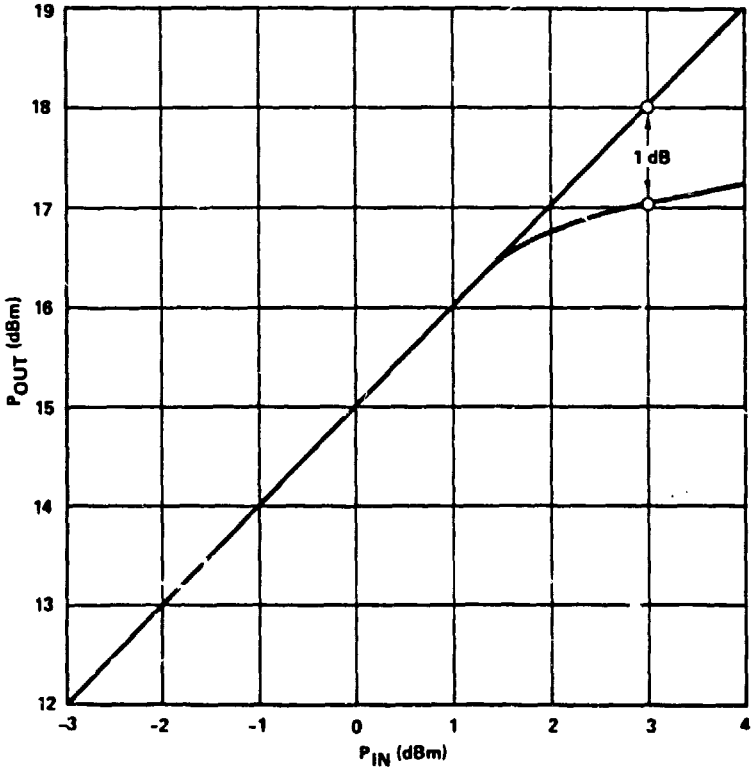


Figure 4-28. P_{in}/P_{out} Avantek Cascaded Pair

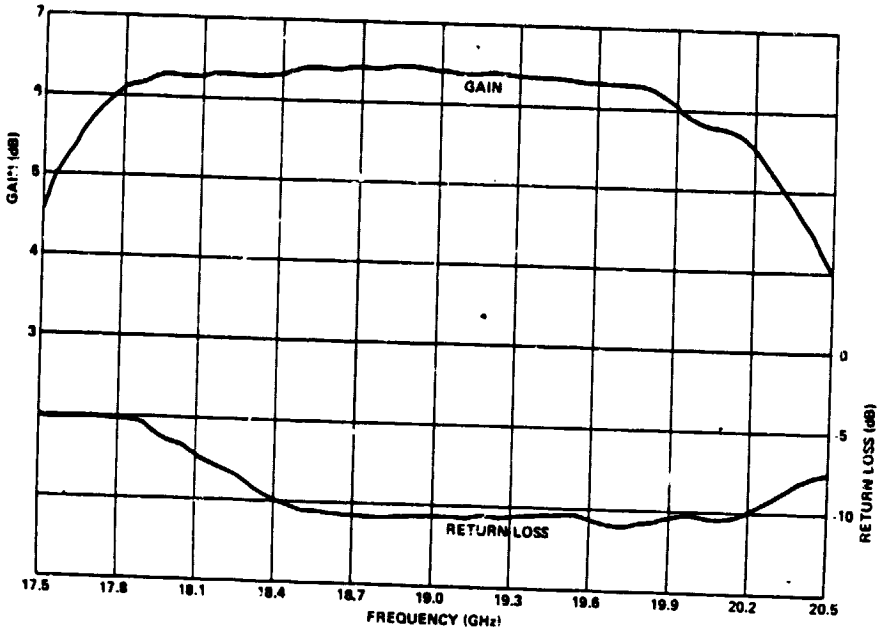


Figure 4-29. Frequency Response and Return Loss of 1/4 Watt - 1/4 Watt Cascaded Pair

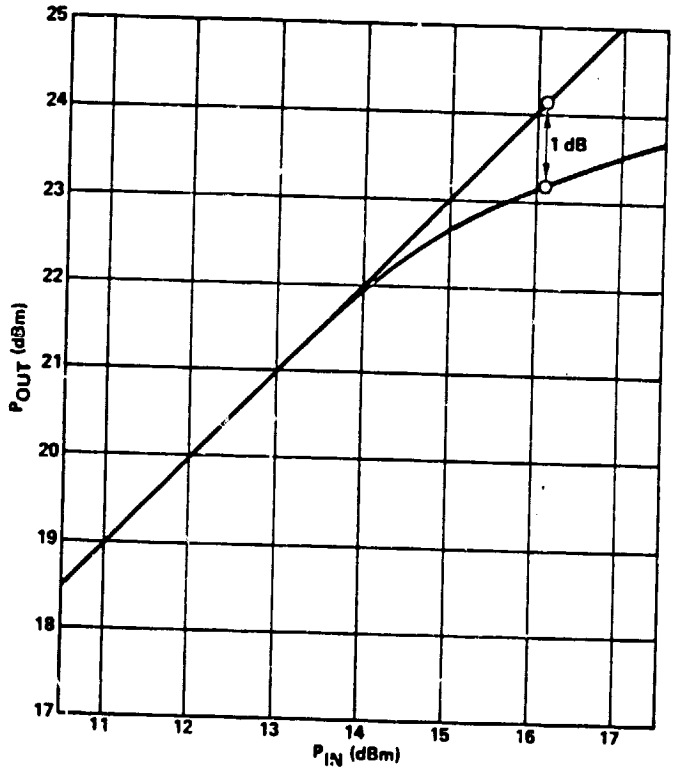


Figure 4-30. P_{in}/P_{out} 1/4 and 1/4 Watt Cascade

The frequency response and the P_{in}/P_{out} response of Raytheon's 1/4 W-1/2 W pair are shown in Figures 4-31 and 4-32, respectively.

The frequency response and the P_{in}/P_{out} response of Raytheon's 1/2 W-1 W pair are shown in Figures 4-33 and 4-34, respectively.

4.6 DRIVER AMPLIFIER MODULE

4.6.1 Driver Module Specifications

The block diagram for the driver amplifier module was shown in Figure 2-3 with associated gain budget. The electrical specifications of the driver module is shown in Table 4-2 below.

Table 4-2. Driver Module Specifications

Output Power	20 dBm
Gain	20 dB
Bandwidth	17.7 to 20.2 GHz (2.5 GHz)
Input VSWR	<1.4:1
Noise Figure	<25 dB

4.6.2 Driver Module Design

As described in Section 1, the driver module and the power module are designed to have the same mechanical configurations to minimize cost. Each module consists of two single-ended stages followed by a balanced two-stage amplifier. A dc-to-dc converter is required to convert the system bus voltage to the required bus voltages for the modules. Each FET device has its own regulator to control the bias voltages to the gate and the drain ports of the FET. The bias voltages are fed to the FETs with dc feed-throughs to minimize the RF from leaking through to the power supplies.

Construction and assembly of the modules must be compatible with space flight qualification. The RF modules are hermetically sealable to protect the GaAs FET chips. To prevent contamination of the GaAs FET chips after the modules are hermetically sealed, the substrates and electronic parts assembly with the module use no epoxy or flux in attachment. The substrate

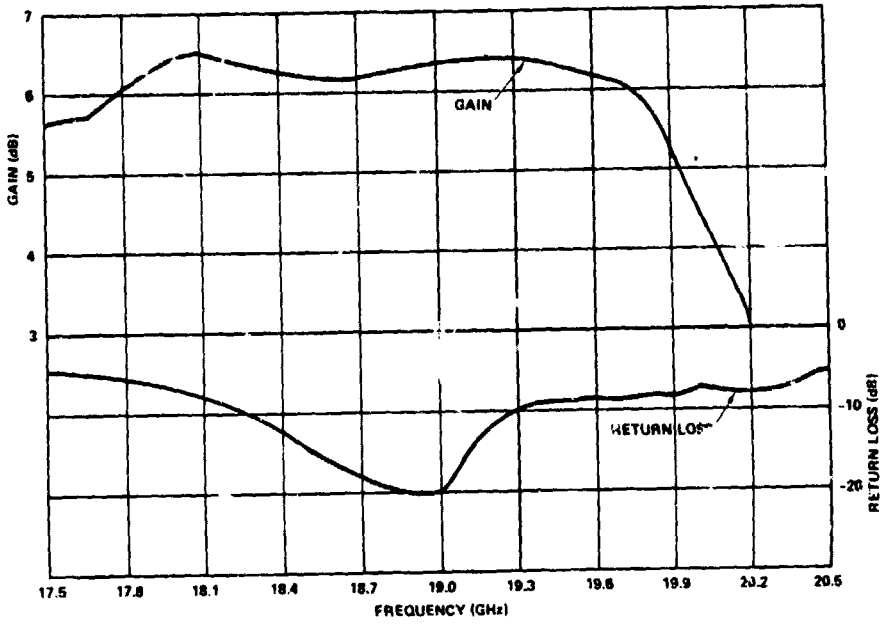


Figure 4-31. Frequency Response and Return Loss of 1/4 Watt and 1/2 Watt Cascade

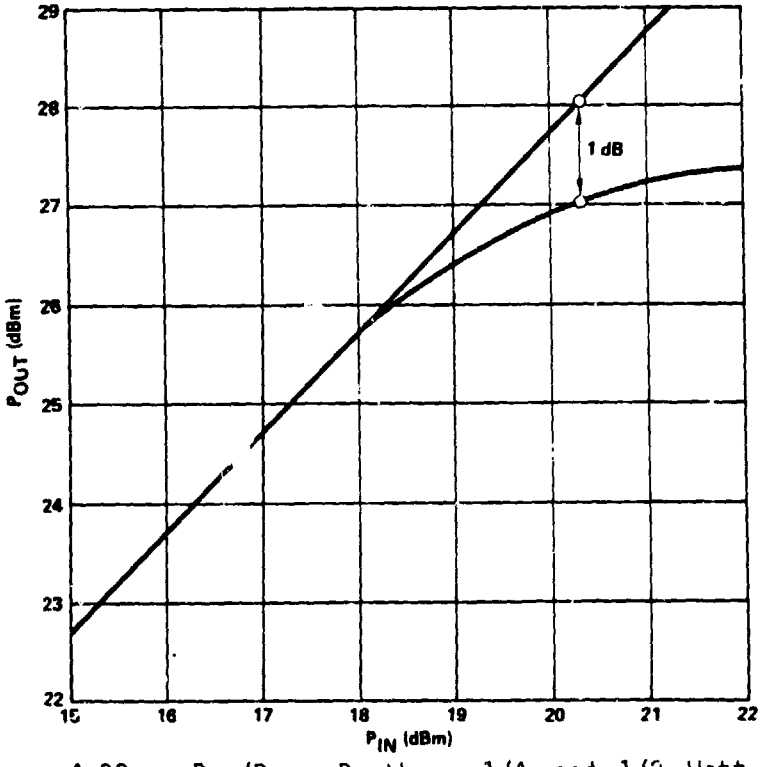


Figure 4-32. P_{in}/P_{out} Raytheon 1/4 and 1/2 Watt Cascade

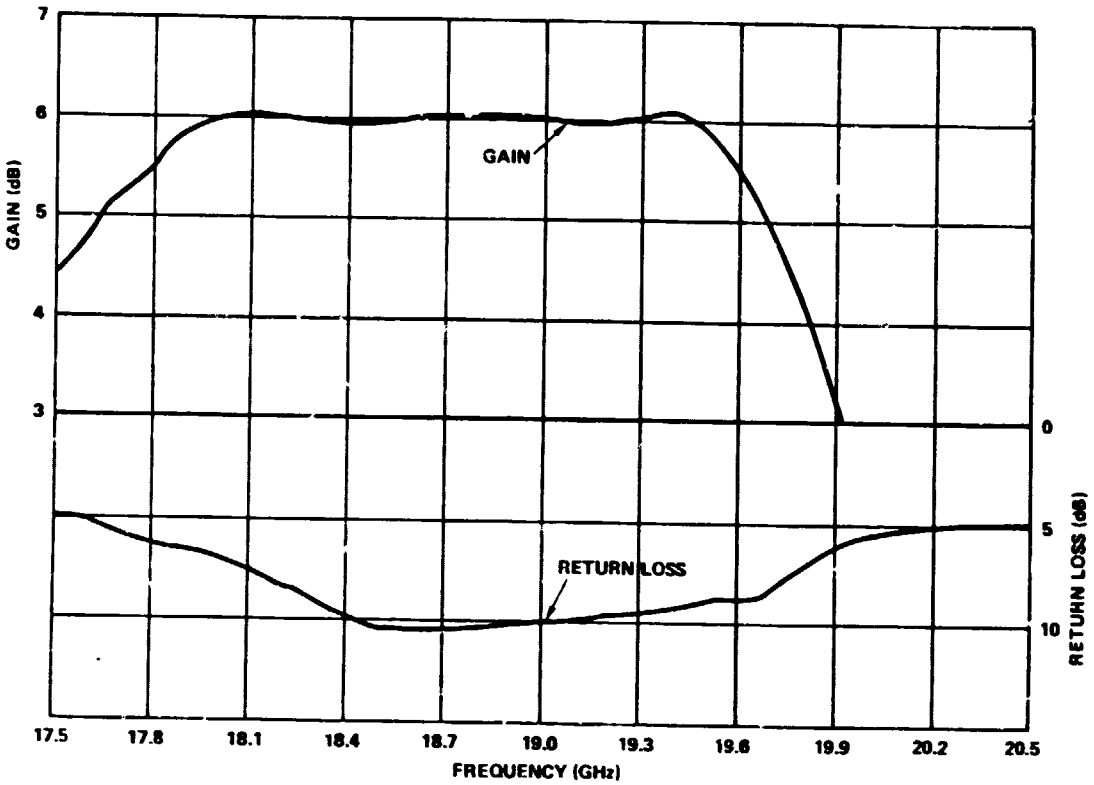


Figure 4-33. Frequency Response and Return Loss of 1/2 Watt - 1 Watt Cascaded Pair

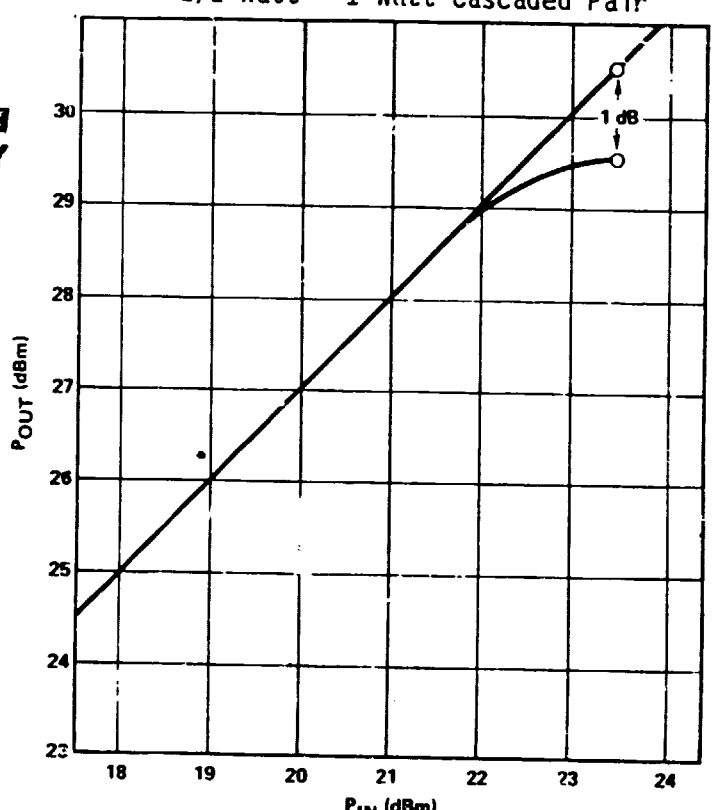


Figure 4-34. P_{in}/P_{out} Raytheon 1/2 and 1 Watt Cascade

carrier material has thermal expansion compatibility to meet the temperature environment. To remove heat generated within the GaAs FET power devices for reliable operation, material with good thermal conductivity is used for the carrier where the GaAs FET is installed.

The mechanical constructions of the modules are described in Section 5 of this report.

4.6.3 Driver Module Integration

The driver module is assembled into the final module with the various electrical pretested components. The components consists of:

- The input waveguide-to-microstrip transition
- The waveguide mode suppressor
- The cascaded single-ended (Avantek-Avantek) amplifier stages
- The input Lange coupler for the balanced stages
- Two cascaded single-ended (Raytheon 1/4 W-1/4 W) amplifier stages in balanced configuration
- The output Lange coupler for the balanced stages
- The waveguide mode suppressor
- The output waveguide-to-microstrip transition
- The dc feedthroughs to bias the FETs
- Other miscellaneous components such as chip capacitors, stand-offs, etc., needed to integrate the module.

Since all of the components have been optimized individually and designed to have sufficient isolation to minimize any effects on performance characteristics due to interaction between the stages, only minor adjustments are required to ensure that all electrical performance characteristics are optimized at the module level.

The assembled driver module is shown in Figure 4-35.

4.6.4 Driver Module Test Data

The frequency response and the P_{in}/P_{out} response of the driver module is shown in Figures 4-36 and 4-37, respectively. Table 4-3 summarizes the performance of the driver module compared to the specifications. Note that the driver modules have met all performance requirements except the

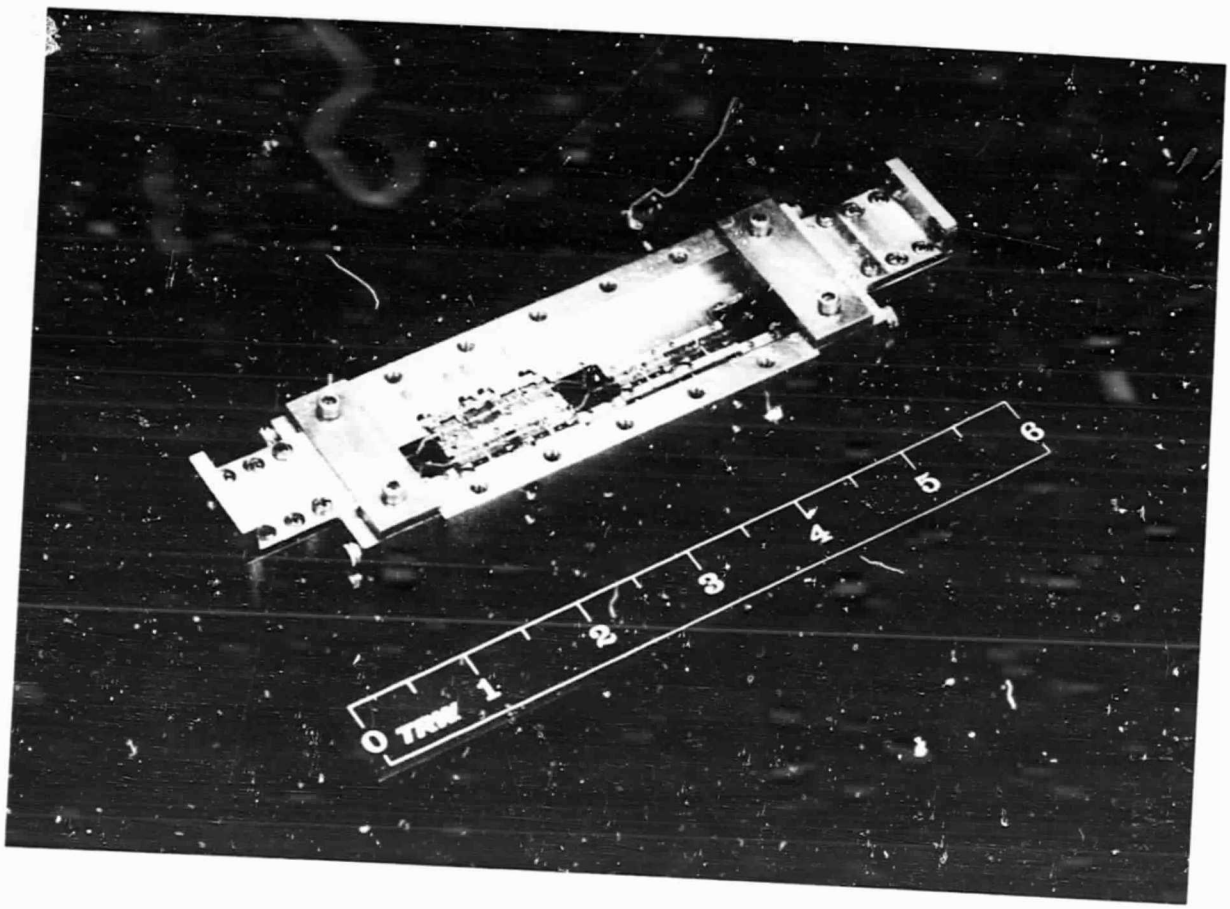


Figure 4-35. Driver Module

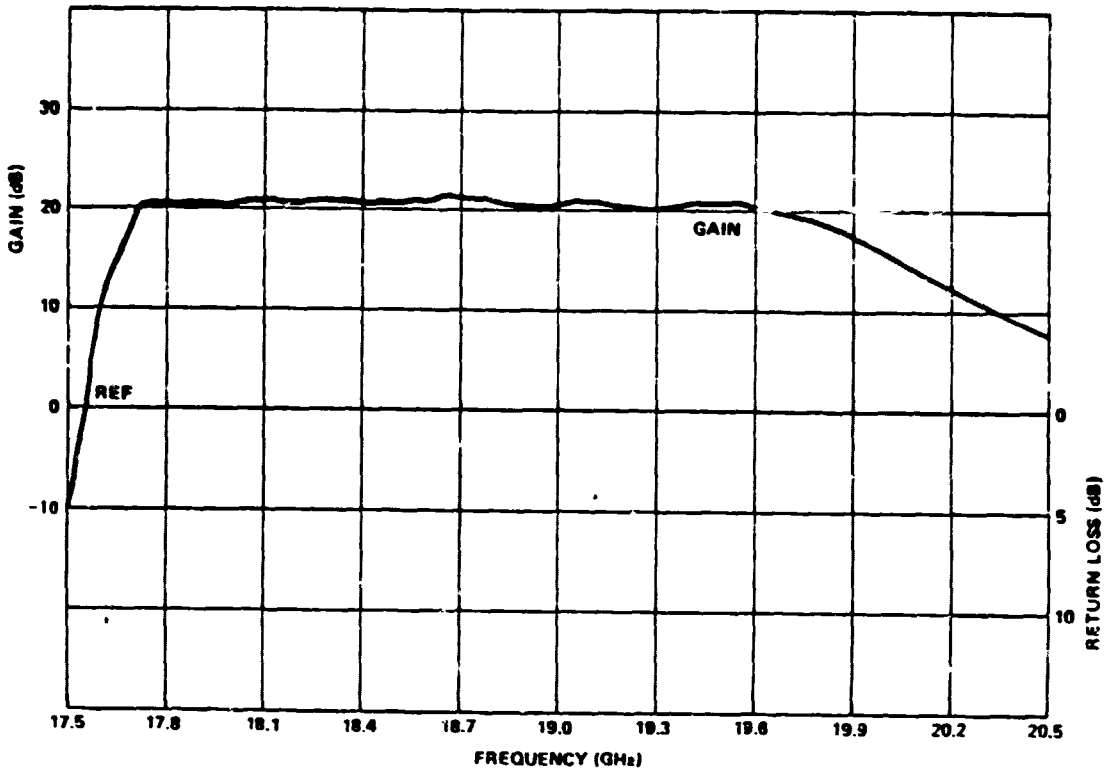


Figure 4-36. Frequency Response of Completely Integrated Driver Module

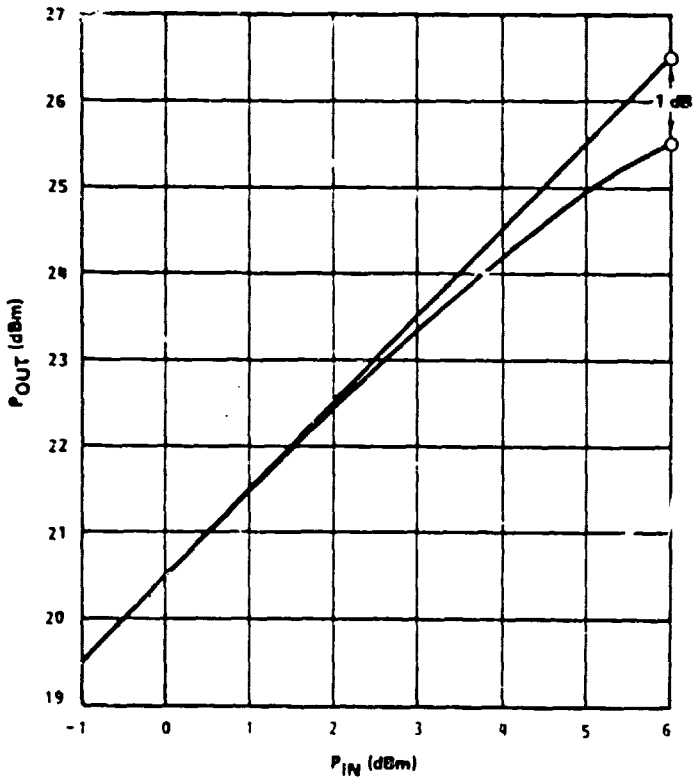


Figure 4-37. P_{in}/P_{out} of Driver Module

Tab. 4-3. Driver Module Specification vs. Performance

	Specifications	Performance
Output Power	20 dBm	20 dBm
Gain	20 dB	21 dB
Bandwidth	17.7 to 20.2 GHz (2.5 GHz)	17.7 to 19.7 GHz (2.0 GHz)

bandwidth. (The bandwidth limitation is caused primarily by the device capability. To increase the bandwidth capability, an improved device with higher input and output impedances and with reduced parasitic effects will be required; this will be described in Section 8.)

4.7 POWER AMPLIFIER MODULE

4.7.1 Power Module Specifications

The block diagram for the power amplifier module was shown in Figure 2-4 with associated gain budget. The electrical specifications of the power module is shown in Table 4-4.

Table 4-4. Power Module Specifications

Output Power	31 dBm
Gain (at 1 dB Compression)	11 dB
Bandwidth	17.7 to 20.2 GHz
Input VSWR	<1.4:1

4.7.2 Power Module Design

As described in Section 1, the driver module and the power module are designed to have the same mechanical configurations to minimize cost. East module consists of two single-ended stages followed by a balanced two-stage amplifier. A dc-to-dc converter is required to convert the system bus voltage to the required bus voltages for the modules. Each FET device has its own regulator to control the bias voltages to the gate and drain ports of the FET. The bias voltages are fed to the FETs with dc feedthroughs to minimize the RF from leaking through to the power supplies.

Construction and assembly of the modules must be compatible with space flight qualification. The RF modules are hermetically sealable to protect the GaAs FET chips. To prevent contamination of the GaAs FET chips after the modules are hermetically sealed, the substrates and electronic parts assembly with the module use no epoxy or flux in attachment. The substrate carrier material has thermal expansion compatibility to meet the temperature environment. To remove heat generated within the GaAs FET power devices for reliable operation, material with good thermal conductivity is used for the carrier where the GaAs FET is installed.

The mechanical constructions of the modules are described in Section 5 of this report.

4.7.3 Power Module Integration

The power module is assembled into the final module with the various electrical pretested compoents. The components consist of:

- The input waveguide-to-microstrip transition
- The waveguide mode suppressor
- The cascaded single-ended (Raytheon 1/4 W-1/2 W) amplifier stages
- The input Lange coupler for the balanced stages
- The cascaded single-ended (Raytheon 1/2 W-1 W) amplifier stages in balanced configuration
- The output Lange coupler for the balanced stages
- The waveguide mode suppressor
- The output waveguide-to-microstrip transition
- The dc feedthroughs to bias the FETs
- Other miscellaneous components such as chip capacitors, stand-offs, etc., needed to integrate the module.

Again, all of the components ahve been optimized individually and designed to provide sufficient isolation to minimize any interaction between stages. Only minor adjustments are required to ensure that all performance characteristics are optimized at the module level.

The assembled power module is shown in Figure 4-38.

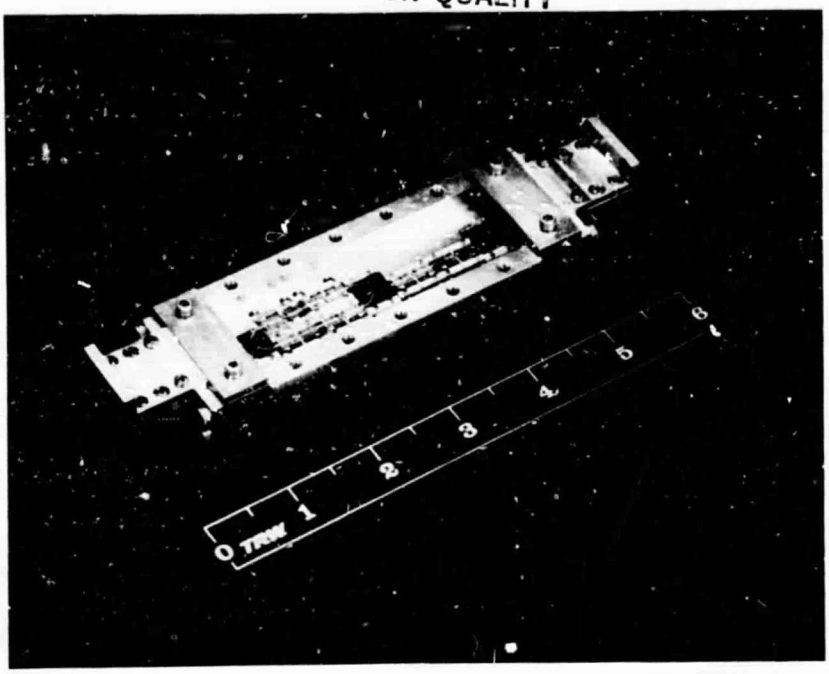


Figure 4-38. Power Module

4.7.4 Power Module Test Data

The frequency response and the P_{in}/P_{out} response of the power module are shown in Figures 4-39 and 4-40, respectively. Table 4-5 summarizes the performance of the power module compared to the specifications. Note that the measured bandwidth was only 1.6 GHz. The input and the output impedances of the higher power devices are even smaller than the low power devices, making them even more difficult to tune over a broad bandwidth. Again, the design of the FET devices must be improved to reduce the parasitics and to increase the input and output impedances.

Table 4-5. Power Module Performance Versus Specifications

	Specification	Performance
Output Power	31 dBm	31 dBm
Gain (at dB Compression)	11 dB	11.5 dB
Bandwidth	17.7 to 20.2 GHz (2.5 GHz)	17.8 to 19.4 GHz (1.6 GHz)
Input VSWR	<1.4:1	<1.2:1

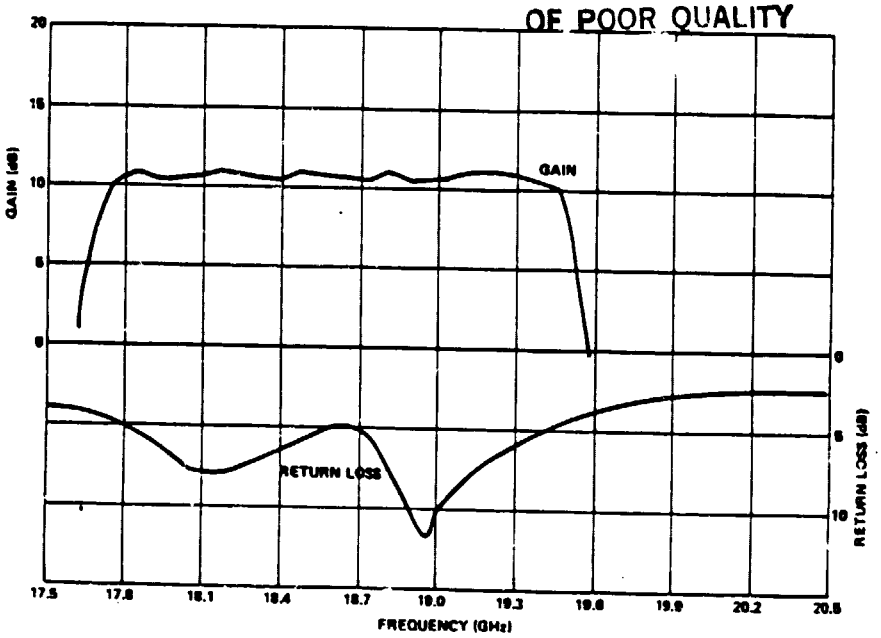


Figure 4-39. Frequency Response and Return Loss of Completely Integrated Power Module

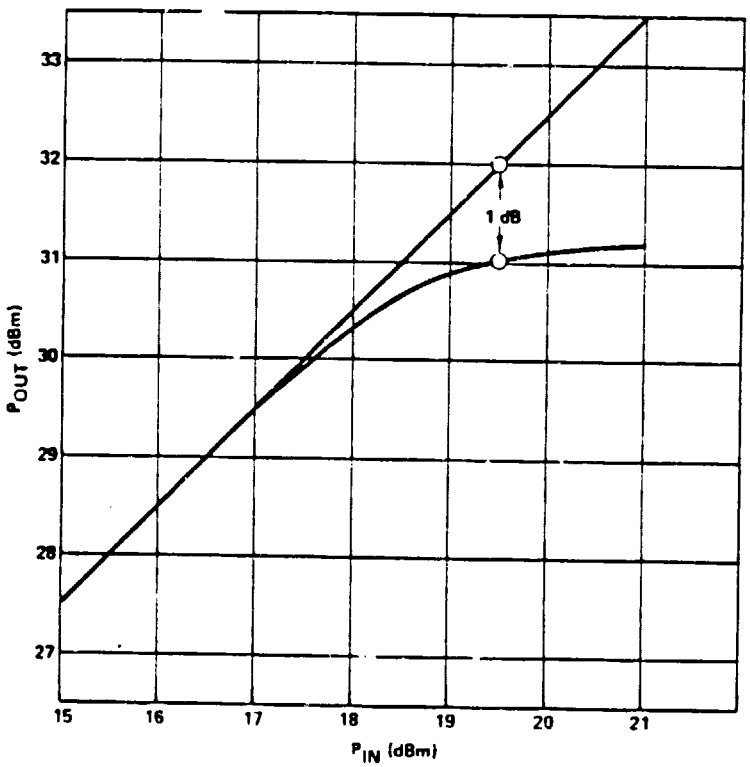


Figure 4-40. P_{in}/P_{out} Power Module

4.8 CASCADED DRIVER AND POWER MODULES

As shown in the block diagram for the POC model, the driver module and the power module are cascaded together to drive the eight-way combined assembly. The driver module and the power module were described in detail in the previous sections. The requirements and the performance of the cascaded driver/power module is shown in this section.

4.8.1 Module Design and Integration

There are no new components needed to cascade the driver module and the power module. The two modules are connected through the waveguide flanges. Provisions were provided, however, to insert an isolator with waveguide ports in the event there should be any adverse interaction between the two modules. It was found that there was no need to add the isolator since the cascaded modules performed quite satisfactorily.

4.8.2 Cascaded Module Specifications

The specifications for the cascaded module are shown in Table 4-6.

Table 4-6. Cascaded Driver/Power Module Specifications

Output Power	31 dBm
Gain (at 1 dB compression)	30 dB
Bandwidth	17.7 to 20.2 GHz (2.5 GHz)
RF Efficiency	>20%
Input VSWR	<1.4:1

4.8.3 Cascaded Driver/Power Module Test Data

The frequency response and the P_{in}/P_{out} response of the cascaded module are shown in Figures 4-41 and 4-42. Table 4-7 shows the performance characteristics of the cascaded driver/power module compared to the specifications. It is noted that the over bandwidth is limited to the bandwidth of the power module, as expected. The other parameter that failed to meet the performance goal is the dc-to-RF efficiency. This can be attributed to many factors. First, the device efficiency must be improved; it is currently approximately 20%. In the recommendations for device improvement, a

Table 4-7. Cascaded Driver and Power Module Specifications Versus Performance

	Specifications	Performance
Output Power	31 dbm	31 dbm
Gain	30 dB	30 dB
Bandwidth	17.7 to 20.2 GHz (2.5 GHz)	17.8 to 19.4 GHz (1.6 GHz)
RF Efficiency	>20%	8.7%
Input VSWR	<1.4:1	<1.2:1

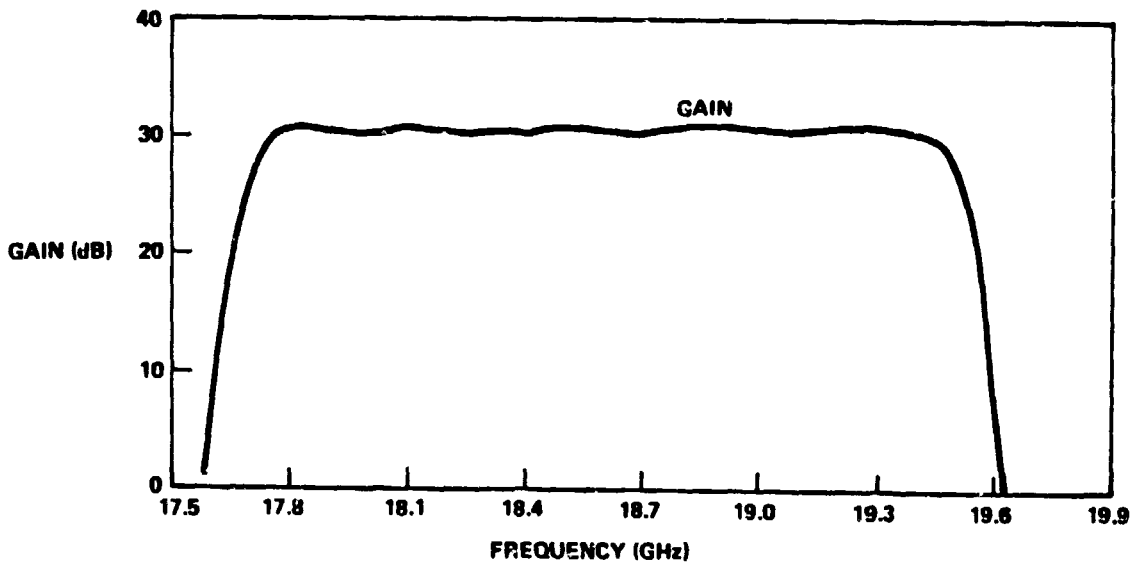


Figure 4-41. Frequency Response of Driver and Power Module Cascaded

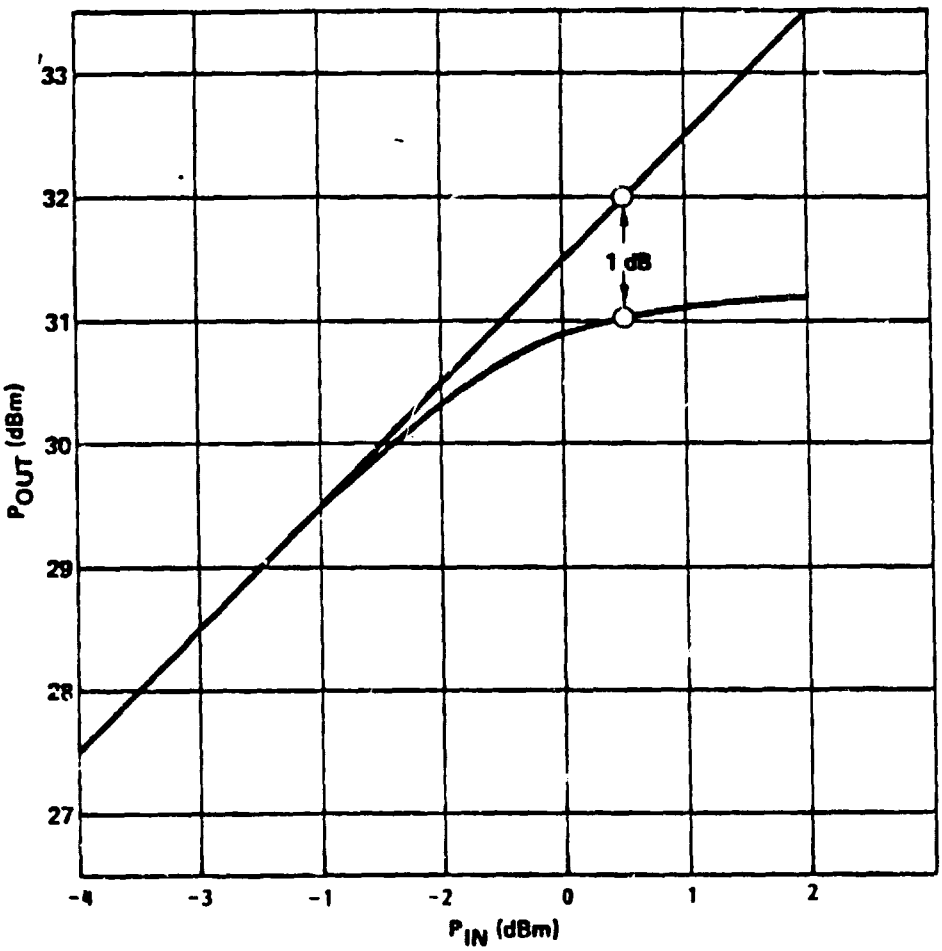


Figure 4-42. P_{in}/P_{out} Driver and Power Module Cascaded

25% device efficiency goal was thought to be achievable and was recommended. Secondly, because of the many stages needed to be cascaded to achieve an overall gain of 30 dB, a total of 3.5 dB of losses through passive circuits such as the Lange couplers, the eight splitter/combiner, etc. was encountered. Although the insertion losses of these components can be

minimized, it is believed that they are already quite well optimized, and therefore the improvement in these areas will be minimal. However, if the devices can provide more gain per stage, the number of stages might be reduced, thus reducing the number of passive components. The 20% efficiency is probably achievable but does require improvements in many of the device parameters.

The cascaded driver/power is shown in Figure 4-43.

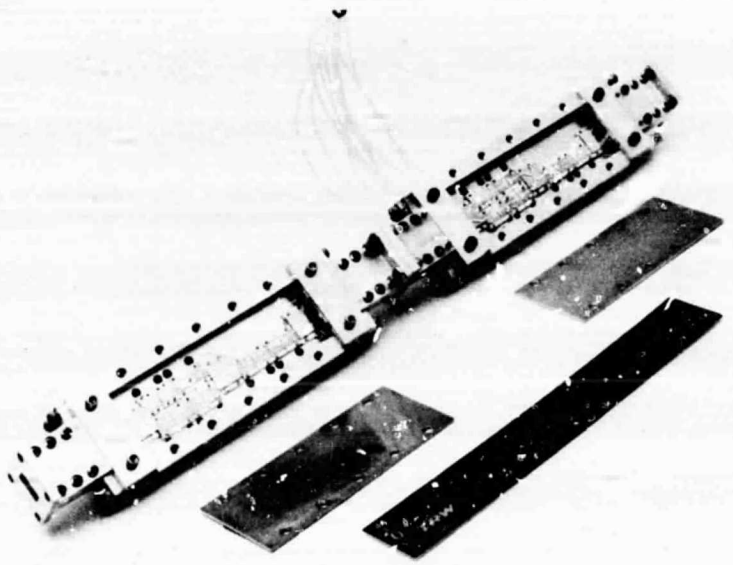


Figure 4-43. Integrated Power Driver Module

4.9 RADIAL POWER SPLITTER/COMBINER

4.9.1 General Discussion

To meet the efficiency and bandwidth objectives of this program, a power-combining scheme employing radial transmission lines was developed. Figure 4-44 illustrates a conceptual drawing of the FET amplifier/combiner system which employs radial transmission lines as the input splitter and output combiner. Unlike power-combining systems for two terminal devices having reflection gain, wherein a single manifold serves the dual functions of input power splitter and output power combiner, three terminal devices require the use of separate power splitters and combiners. As shown in the figure, the approach consists of two back-to-back radial transmission lines with the individual elemental amplifiers connected between the radial lines at the perimeter of the structure. Due to its radial symmetry, this configuration results in a minimum of interconnecting line lengths and hence minimize losses. The radial line splitter/combiner, with integral resistive isolation, has N radially symmetric microstrip ports and a central coaxial port. Due to the inherent impedance-transforming properties of radial lines, it is possible to transform the N 50-ohm peripheral ports to a single central ohm port. As a result, the combiner problem is reduced to two separable problems; i.e., design of the manifolds (power divider and power combiner) and design of the ensemble of nominally identical individual matched amplifiers which are connected between the radial line splitter and combiner. It is thus feasible to pretune each individual elemental amplifier in a separate 50-ohm test system. Similarly, the radial line splitter/combiner can conveniently be pretested as an N + 1 port structure with a 50-ohm interface at each port. To meet the requirements of the POC model, the splitter and combiner are designed to:

1) have high combining efficiency so that the output power is nearly equal to the sum of the individual FET amplifier power outputs

2) not alter the reliability, stability, or signal characteristics of the individual amplifiers

3) be sufficiently broadband so as not to limit the performance of the overall amplifier

4) provide adequate isolation between the elemental amplifiers in order to prevent interaction and/or oscillations and to obtain a graceful degradation behavior.

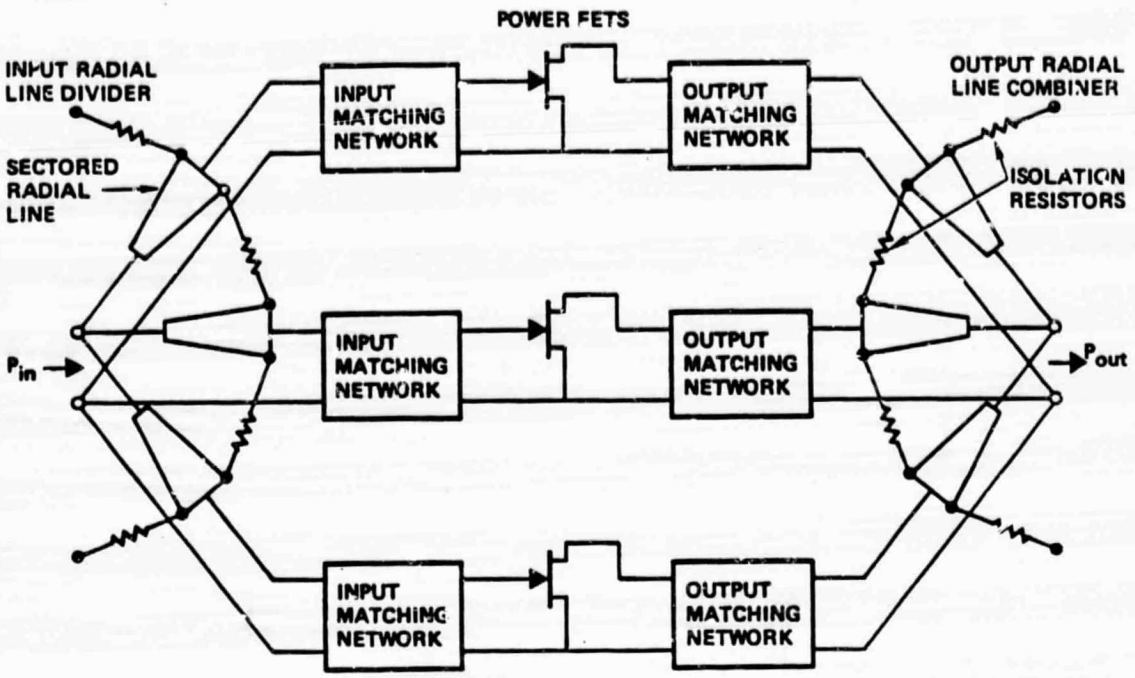


Figure 4-44. Radial Combiner/Splitter Scheme

When the amplitude and phase responses of the different signal paths of the combined amplifier are not identical, due to nonuniformity of the component amplifiers or amplitude and phase imbalances in the hybrids over the desired frequency band, the combining efficiency suffers. The use of electrically symmetric design is the most effective way of eliminating frequency-dependent imbalances in the hybrids. In addition, reducing the loss will, of course, increase the combining efficiency.

4.9.2 Assumptions and Criteria for Optimization

A schematic diagram of the single-stage radial n-way hybrid is shown in Figure 4-45, and the corresponding geometries of the isolation resistors are shown in Figures 4-46. The common port is designated the number 0 and is assumed to terminate in Z_s. The divided ports are designated the numbers 1 through n, and are each terminated in Z_L. The characteristic impedance of each of the quarter-wave lines in Z_0, and the resistance of an isolation resistor is R.

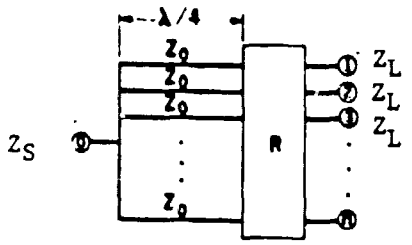


Figure 4-45. Schematic Representation of the Single-State N-Way Hybrids

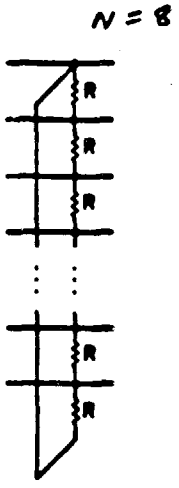


Figure 4-46. Arrangements of the Isolation Resistors for the Radial N-way Hybrids

The coupling among the n transmission lines diverging from port 0 may be strong because of their proximity. However, it is assumed that the phase velocities of all modes propagating along these lines are approximately equal, but the characteristic impedances of these modes may be different. At the center frequency where these lines are a quarter-wave long, only the characteristic impedance Z_0 of each line for the equal-amplitude, equal-phase mode (i.e., the common mode) is required in the analysis. For the remaining modes, these lines appear as quarter-wave transmission lines that are short circuited at port 0, and hence present an open circuit at their other ends irrespective of their modal characteristic impedances.

Coupling is neglected among all transmission lines beyond the first stage of the hybrids. The justification for this assumption is that such lines would be reasonably separated from one another.

Junction effects are neglected.

Let $S_{ij}(i,j=1,2,\ldots,n)$ be the scattering parameters among ports 1 through n normalized to Z_L. Thus,

$$\text{Match or Return Loss}(i) = -20 \log |S_{ii}| \text{ dB}$$

$$\text{Isolation}(i,j) = -20 \log |S_{ij}| \text{ dB} \quad i = j$$

The criterion for optimization of the isolation resistors is to

$$\text{Minimize the maximum of } |S_{ij}|, \qquad i,j = 1,2,\ldots,n \tag{1}$$

Thus, the match and isolation are given the same importance.

Maximizing the isolation alone without any regard to the match may lead to a catastrophic failure of the combined amplifier if any of its component amplifiers fails in a particular manner. For example, one can obtain a large degree of isolation in a Wilkinson hybrid with a large n by simply removing the isolation resistors altogether. However, the combined amplifier would be short circuited if an open circuit develops in the input or output terminals of any of the component amplifiers. On the other hand, maximizing the match alone without any regard to the isolation may lead to

undesirable interactions among the component amplifiers. Furthermore, a failure of one or more amplifiers with either of the two aforementioned criteria for optimization may cause the source and/or load impedances presented to the remaining amplifiers to vary significantly from their optimum values, reducing their output power. Thus, the criterion defined in (1), where both the match and isolation are maximized, presents an overall optimum condition that would guarantee a graceful degradation of the combined amplifier under arbitrary modes of failure of one or more of the component amplifiers.

Table 4-8 gives the optimum match and isolation for radial hybrids with n = 2 through 12 radial ports. The values of the optimum isolation resistor R and its power rating are also given.

4.9.3 Power Dissipation in Isolation Resistor

The power rating of the isolation resistors will be calculated for a power combiner when only one amplifier, out of the n being combined, fails. Since no power is dissipated in the isolation resistors when all amplifiers are operating under an ideal situation, the theory of superposition indicates that a single amplifier produces a current in each isolation resistor that is equal and opposite to that produced by the other amplifiers. Thus, as far as dissipation in the isolation resistors is concerned, the failure of only one amplifier is equivalent to the case when only that amplifier is working. The impedance presented by the failed amplifier to the combiner will affect the power dissipation, unless the combiner is perfectly matched. Thus, the worst case impedance will be considered in the calibrations.

The power rating P_r of the isolation resistors will be given relative to the power of each component amplifier. Thus,

$$P_r = \frac{\text{(Maximum power dissipated in isolation resistor due to the worst case failure of one component amplifier)}}{\text{Power of a component amplifier}}$$

Table 4-8. Optimum Performance of Single-Stage Radial N-way Hybrids

n	(Z_L/R) opt	Optimum Match and Isolation (dB)	P_r
2	0.25	∞	0.25
3	0.33333	∞	0.33
4	0.5	21.6	0.413
5	0.44721	19.5	0.358
6	0.42792	17.6	0.398
7	0.35955	17.2	0.484
8	0.35960	16.1	0.505
10	0.35961	14.9	0.536
12	0.35961	14.1	0.558

When the amplifier connected to port k fails, the maximum dissipation will occur at each of the two resistors connected to the kth transmission line. Due to the symmetry of the radial hybrid, this dissipation is independent of k.

$$P_r = (1 + S_{11} - S_{12})^2 g$$

For $n \geq 8$, the optimum results of the single-stage radial hybrid can be approximated, with excellent accuracy, as

$$(Z_L/R)_{opt} = (7 - \sqrt{17})/8 = 0.35961$$

$$S_{opt} = S_{11} = S_{12} = \left(\frac{\sqrt{17} - 3}{4}\right) - 1/n = 0.28078 - 1/n$$

$$g = Z_L/R$$

$$P_r = 0.35961/(0.71922 + 1/n)^2.$$

4.9.4 Power Combining Losses

The combining loss which occurs even with perfect, lossless materials is considered circuit loss and is independent of material losses. Circuit losses exist if the input signals applied to the combiner are not all of the proper amplitude and phase, if the load and source impedances are not matched to the combiner, and if the combiner does not have perfect coupling and phasing between ports.

Figure 4-47 illustrates the general block diagram of a splitter/combiner system. It consists of an input power splitter, N elemental amplifiers, and an output power combiner. The amplitude and phase of the signals arriving at the combiner input ports are dependent not only on the input splitter, but on the intervening amplifiers as well. Assuming perfect isolation between the combiner input ports, it can be shown that the transmission coefficients and port voltages are independent of each other. With this assumption the generalized N-way combining equation can be expressed as

$$\overline{V}_0 = \overline{T}_1\overline{V}_1 + \overline{T}_2\overline{V}_2 + \ldots + \overline{T}_N\overline{V}_N \qquad (2)$$

where, in general, all parameters are complex quantities, T_j is the voltage transmission coefficient from port j to the output with a magnitude given by

$$|T_j| = (\text{power coupling, output to port j})1/2.$$

Due to the assumed isolation, the Ts are fixed quantities determined by the combiner geometry, and the combining equation is valid for any voltages impressed on the input ports. This fact has great significance because it then follows that equation (2) may be used to analyze the effects of:

- unequal input signals, either in magnitude, angle or both
- unequal coupling of the input ports to the output, either by design or production tolerances
- input signal failures and the graceful degradation properties of the power combining system.

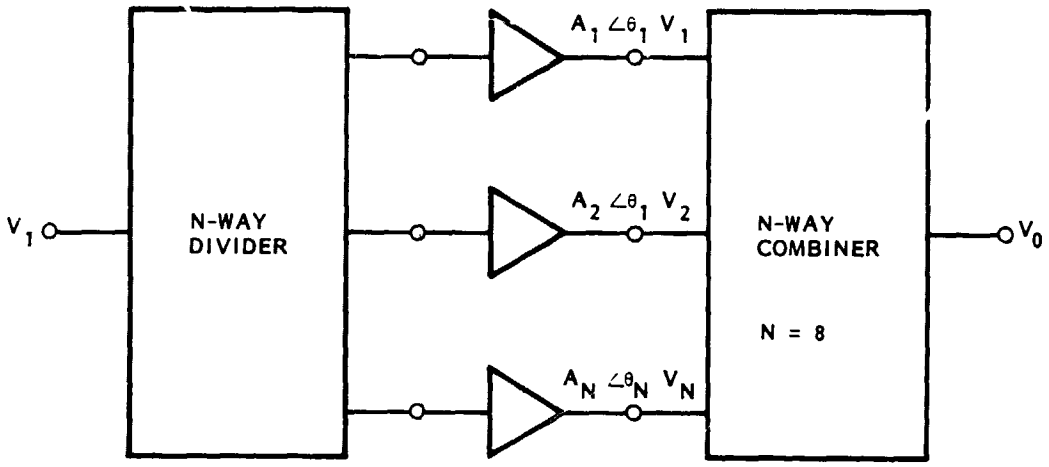


Figure 4-47. N-Way Power Combiner System

For an ideal combiner, the Ts are all equal in magnitude and phase with a value of 1/N. Then equation (2) reduces to

$$\overline{V}_0 = \frac{1}{N} \left(\overline{V}_1 + \overline{V}_2 + \ldots + \overline{V}_N\right). \tag{3}$$

This equation may be transformed to a more useful form

$$P_0 = \frac{1}{N} \left| \sqrt{P_1} \angle\theta 1 + \sqrt{P_2} \angle\theta_2 + \ldots + \sqrt{P_N} \angle\theta_N \right|^2 . \tag{4}$$

A vector sum of terms is used to account for the different relative phases of the combiner input signals. A combining efficiency, n_c, can be defined as the ratio of the combiner output power to the total combiner input power. Employing this definition, the combining efficiency is given by

$$n_c = \frac{1}{NP_T} \left| \sqrt{P_1} \angle\theta_1 + \sqrt{P_2} \angle\theta_2 + \ldots + \sqrt{P_N} \angle\theta_N \right|^2 \tag{5}$$

where P_T is simply the algebraic sum of the input powers. The parameter n_c gives a measure of how much of the available power from the amplifiers reaches the combiner output port.

Equations (4) and (5) are the basic equations used to analyze the effect of amplifier amplitude and phase imbalances on the overall power combining system. By setting $\theta_j = 0$, the equations can be used to analyze amplitude imbalances or graceful degradation. Alternately, with $P_1 = P_2 = \ldots = P_N$, the equations can be used to study the effects of the phase imbalances.

For the special case of unequal amplitudes but equal phase ($\theta_1 = \theta_2 = \ldots \theta_N = 0$), the equations for the combiner output power and efficiency reduce to

$$P_o = \frac{1}{N} (\sqrt{P_1} + \sqrt{P_2} + \ldots + \sqrt{P_N})^2 \tag{6}$$

$$n_c = \frac{1}{NP_T} (\sqrt{P_1} + \sqrt{P_2} + \ldots + \sqrt{P_N})^2 \tag{7}$$

In general, the combining efficiency is a slowly changing function of the input power.

As opposed to amplitude imbalances, amplifier phase imbalances are more detrimental to the performance of the amplifier/combiner system. The effect of these phasing errors can be analyzed with the aid of the general combining equation (4) with $P_1 = P_2 = \ldots = P_N$ and $\theta_j \neq 0$. For a N-way power combiner driven by N equal amplitude signals, M of which are out-of-phase, equation (4) becomes

$$P_o = \frac{P_{in}}{N} \{[(N-M) + M \cos \theta]^2 + M^2 \sin^2 \theta\}$$

where P_{in} equals the power of each individual amplifier and θ equals the phase error of the out-of-phase amplifiers. For this case, the combining efficiency, n_c, which is defined as the ratio of the total output power of the combiner to the total input power, can be expressed as

$$n_c = \frac{1}{N^2} \{[(N-M) + M \cos \theta]^2 + M^2 \sin^2 \theta\}.$$

After some algebraic manipulation the above reduces to

$$n_c = 1 - 2\frac{M}{N}\left(1 - \frac{M}{N}\right)(1 - \cos\theta)$$

This equation is plotted in Figure 4-48 for N = 8 and M = 1 and 4. For the case where M/N = 1/2 (half the amplifiers out of phase), the combining efficiency is reduced to 90 percent for a phase error 37°. In order to obtain a combining efficiency of 98 percent (0.1 dB loss), the phase error must be less than 16°.

The results of the discussion indicate the following conclusions:

1) Amplitude matching of the individual amplifiers is not critical

2) Amplifier phase errors are generally more important in determining the combining efficiency.

4.9.5 Graceful Degradation

The inherent redundancy in an N-amplifier/combiner system makes it possible (given sufficient isolation) to obtain a graceful degradation characteristic. This means that as the individual amplifiers fail, the remaining amplifiers are not affected and the maximum possible power is delivered to the output port. For certain applications, the enhanced reliability resulting from this graceful degradation characteristic makes the N-amplifier approach attractive.

The graceful degradation property of an N amplifier system can be examined with the aid of the in-phase combining equation (6) by setting selected input terms to zero. In an N-amplifier system with M failed amplifiers, the power output, relative to the maximum output power, is given by

$$\frac{P_o}{P_{max}} = \frac{(N-M)^2}{N^2} .$$

The output power is not directly proportional to the number of working amplifiers, but is proportional to the square of the number of working amplifiers. This graceful degradation characteristic is plotted in Figure 4-49 for an eight-amplifier system.

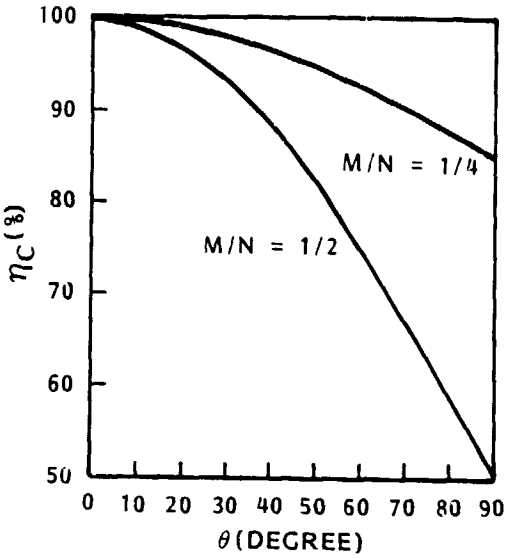


Figure 4-48. Effects of Phase Imbalance on Combining Efficiency

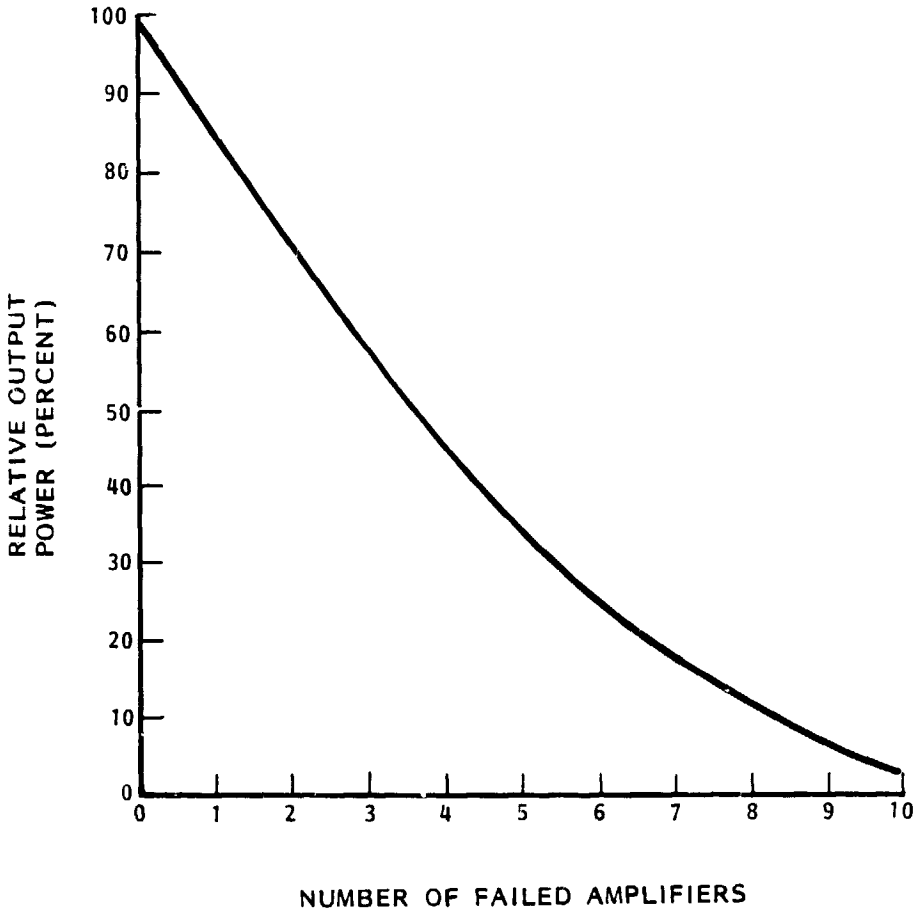


Figure 4-49. Graceful Degradation

An important consideration relative to graceful degradation is the power dissipated in the internal isolation resistors. The isolation resistors must have sufficient power capacity to handle the imbalance power caused by amplifier failures. It can be shown that maximum power is dissipated in the isolation resistors when one-half of the amplifiers have failed. For this case, the total power dissipated in the isolation resistors is $P_{max}/4$, where P_{max} is defined as the maximum output power (all amplifiers working).

4.9.6 Power Dissipation Data in Various Substrates

In the event one or more of the amplifiers should fail, the heat generated by power dissipated in the isolator resistors must be carried away to prevent the resistor and the subsystem from being damaged. Table 4-9 following is the thermal resistance calculation on thin film resistors with dimensions W x L deposited on various substrates. The substrate materials chosen for comparison are: duroid, quartz, aluminum and beryllia.

Detailed thermal analysis for a reliable space-qualifiable design dictated that beryllia should be used as the substrate material for the combiner circuit. To make the design of the splitter circuit the same as the combiner circuit, beryllia is also used for the splitter, even though the power dissipated in the splitter circuit is much less as compared to the combiner circuit.

4.9.7 Radial Transmission Line

Radial transmission lines can be considered as nonuniform transmission lines formed by two annular disks as shown in Figure 4-50. The electromagnetic fields are contained in the cylindrical region between the two disks. As a divider/combiner, only the lowest order E-type mode is desired to propagate on the radial line. This mode has no field variation circumferentially or axially, and therefore there are no field components in the radial direction. The field configuration is circularly symmetric about the z-axis, with the electric field lines parallel to the z-axis and the magnetic field lines forming circles concentric with the z-axis. This mode is easily excited by feeding the radial line in the center with a coaxial transmission line.

Table 4-9. Thermal Resistance in Various Substrates

SUBSTRATE HEIGHT= .015 IN

WIDTH W	LENGTH L	THERMAL RESIST. C/WATT DUROID	QUARTZ	ALUMIN	BERYLLIA
.005	.005	3634.2	665.4	35.0	4.7
.005	.010	3132.9	573.6	30.2	4.1
.005	.015	2753.2	504.1	26.5	3.6
.005	.020	2455.5	449.6	23.6	3.2
.005	.025	2216.0	405.7	21.3	2.9
.005	.030	2019.0	369.7	19.4	2.6
.005	.035	1854.2	339.5	17.9	2.4
.005	.040	1714.2	313.9	16.5	2.2
.005	.045	1593.9	291.8	15.3	2.1
.005	.050	1489.4	272.7	14.3	1.9
.005	.055	1397.8	255.9	13.5	1.8
.005	.060	1316.7	241.1	12.7	1.7
.005	.065	1244.6	227.9	12.0	1.6
.005	.070	1179.9	216.0	11.4	1.5
.005	.075	1121.7	205.4	10.8	1.5
.010	.010	2672.2	489.3	25.7	3.5
.010	.015	2329.6	426.5	22.4	3.0
.010	.020	2064.9	378.1	19.9	2.7
.010	.025	1854.2	339.5	17.9	2.4
.010	.030	1682.5	308.1	16.2	2.2
.010	.035	1539.9	282.0	14.8	2.0
.010	.040	1419.6	259.9	13.7	1.8
.010	.045	1316.7	241.1	12.7	1.7
.010	.050	1227.8	224.8	11.8	1.6
.010	.055	1150.1	210.6	11.1	1.5
.010	.060	1081.6	198.0	10.4	1.4
.010	.065	1020.8	186.9	9.8	1.3
.010	.070	966.5	177.0	9.3	1.3
.010	.075	917.7	168.0	8.8	1.2
.015	.015	2019.0	369.7	19.4	2.6
.015	.020	1781.5	326.2	17.2	2.3
.015	.025	1593.9	291.8	15.3	2.1
.015	.030	1442.1	264.1	13.9	1.9
.015	.035	1316.7	241.1	12.7	1.7
.015	.040	1211.4	221.8	11.7	1.6
.015	.045	1121.7	205.4	10.8	1.5
.015	.050	1044.3	191.2	10.1	1.4
.015	.055	976.9	178.9	9.4	1.3
.015	.060	917.7	168.0	8.8	1.2
.015	.065	865.3	158.4	8.3	1.1
.015	.070	818.5	149.9	7.9	1.1
.015	.075	776.5	142.2	7.5	1.0
.020	.020	1566.4	286.8	15.1	2.0

Table 4-9. Thermal Resistance in Various Substrates (Continued)

.020	.030	1261.9	231.0	12.2	1.6
.020	.035	1150.1	210.6	11.1	1.5
.020	.040	1056.4	193.4	10.2	1.4
.020	.045	976.9	178.9	9.4	1.3
.020	.050	908.5	166.4	8.7	1.2
.020	.055	849.1	155.5	8.2	1.1
.020	.060	797.0	145.9	7.7	1.0
.020	.065	750.9	137.5	7.2	1.0
.020	.070	709.8	130.0	6.8	.9
.020	.075	673.0	123.2	6.5	.9
.025	.025	1244.6	227.9	12.0	1.6
.025	.030	1121.7	205.4	10.8	1.5
.025	.035	1020.8	186.9	9.8	1.3
.025	.040	936.6	171.5	9.0	1.2
.025	.045	865.3	158.4	8.3	1.1
.025	.050	804.0	147.2	7.7	1.0
.025	.055	750.9	137.5	7.2	1.0
.025	.060	704.3	129.0	6.8	.9
.025	.065	663.2	121.4	6.4	.9
.025	.070	626.6	114.7	6.0	.8
.025	.075	593.8	108.7	5.7	.8
.030	.030	1009.5	184.8	9.7	1.3
.030	.035	917.7	168.0	8.8	1.2
.030	.040	841.2	154.0	8.1	1.1
.030	.045	776.5	142.2	7.5	1.0
.030	.050	721.1	132.0	6.9	.9
.030	.055	673.0	123.2	6.5	.9
.030	.060	630.9	115.5	6.1	.8
.030	.065	593.8	108.7	5.7	.8
.030	.070	560.8	102.7	5.4	.7
.030	.075	531.3	97.3	5.1	.7
.035	.035	833.5	152.6	8.0	1.1
.035	.040	763.5	139.8	7.4	1.0
.035	.045	704.3	129.0	6.8	.9
.035	.050	653.6	119.7	6.3	.8
.035	.055	609.8	111.6	5.9	.8
.035	.060	571.1	104.6	5.5	.7
.035	.065	537.6	98.4	5.2	.7
.035	.070	507.6	92.9	4.9	.7
.035	.075	480.7	88.0	4.6	.6
.040	.040	698.9	128.0	6.7	.9
.040	.045	644.4	118.0	6.2	.8
.040	.050	597.7	109.4	5.8	.8
.040	.055	557.4	102.1	5.4	.7
.040	.060	522.1	95.6	5.0	.7
.040	.065	491.1	89.9	4.7	.6

Table 4-9. Thermal Resistance in Various Substrates (Continued)

.040	.070	463.5	84.9	4.5	.6
.040	.075	438.9	80.4	4.2	.6
.045	.045	593.8	108.7	5.7	.8
.045	.050	550.6	100.8	5.3	.7
.045	.055	513.3	94.0	4.9	.7
.045	.060	480.7	88.0	4.6	.6
.045	.065	452.0	82.8	4.4	.6
.045	.070	426.5	78.1	4.1	.6
.045	.075	403.8	73.9	3.9	.5
.050	.050	510.4	93.5	4.9	.7
.050	.055	475.7	87.1	4.6	.6
.050	.060	445.4	81.5	4.3	.6
.050	.065	418.7	76.7	4.0	.5
.050	.070	395.0	72.3	3.8	.5
.050	.075	373.9	68.5	3.6	.5
.055	.055	443.2	81.1	4.3	.6
.055	.060	414.9	76.0	4.0	.5
.055	.065	389.9	71.4	3.8	.5
.055	.070	367.8	67.3	3.5	.5
.055	.075	348.1	63.7	3.4	.5
.060	.060	388.3	71.1	3.7	.5
.060	.065	364.9	66.8	3.5	.5
.060	.070	344.1	63.0	3.3	.4
.060	.075	325.6	59.6	3.1	.4
.065	.065	342.8	62.8	3.3	.4
.065	.070	323.3	59.2	3.1	.4
.065	.075	305.9	56.0	2.9	.4
.070	.070	304.9	55.8	2.9	.4
.070	.075	288.4	52.8	2.8	.4
.075	.075	272.8	50.0	2.6	.4

SUBSTRATE HEIGHT= .025 IN

WIDTH	LENGTH	THERMAL RESIST. C/WATT			
		DURCID	QUARTZ	ALUMIN	BERYLLIA
.005	.005	2482.4	454.5	23.9	3.2
.005	.010	2260.1	413.8	21.8	2.9
.005	.015	2074.3	379.8	20.0	2.7
.005	.020	1916.8	351.0	18.5	2.5
.005	.025	1781.5	326.2	17.2	2.3
.005	.030	1664.0	304.7	16.0	2.2
.005	.035	1561.1	285.8	15.0	2.0
.005	.040	1470.1	269.2	14.2	1.9

Table 4-9. Thermal Resistance in Various Substrates (Continued)

.005	.050	1316.7	241.1	12.7	1.7
.005	.055	1251.4	229.1	12.1	1.6
.005	.060	1192.3	218.3	11.5	1.6
.005	.065	1138.5	208.5	11.0	1.5
.005	.070	1089.4	199.5	10.5	1.4
.005	.075	1044.3	191.2	10.1	1.4
.010	.010	2046.3	374.7	19.7	2.7
.010	.015	1869.4	342.3	18.0	2.4
.010	.020	1720.7	315.1	16.6	2.2
.010	.025	1593.9	291.8	15.3	2.1
.010	.030	1484.5	271.8	14.3	1.9
.010	.035	1389.2	254.4	13.4	1.8
.010	.040	1305.4	239.0	12.6	1.7
.010	.045	1231.1	225.4	11.9	1.6
.010	.050	1164.8	213.3	11.2	1.5
.010	.055	1105.3	202.4	10.6	1.4
.010	.060	1051.6	192.5	10.1	1.4
.010	.065	1002.8	183.6	9.7	1.3
.010	.070	958.4	175.5	9.2	1.2
.010	.075	917.7	168.0	8.8	1.2
.015	.015	1701.4	311.5	16.4	2.2
.015	.020	1561.1	285.8	15.0	2.0
.015	.025	1442.1	264.1	13.9	1.9
.015	.030	1340.0	245.4	12.9	1.7
.015	.035	1251.4	229.1	12.1	1.6
.015	.040	1173.8	214.9	11.3	1.5
.015	.045	1105.3	202.4	10.6	1.4
.015	.050	1044.3	191.2	10.1	1.4
.015	.055	989.7	181.2	9.5	1.3
.015	.060	940.5	172.2	9.1	1.2
.015	.065	896.0	164.1	8.6	1.2
.015	.070	855.5	156.6	8.2	1.1
.015	.075	818.5	149.9	7.9	1.1
.020	.020	1428.5	261.6	13.8	1.9
.020	.025	1316.7	241.1	12.7	1.7
.020	.030	1221.2	223.6	11.8	1.6
.020	.035	1138.5	208.5	11.0	1.5
.020	.040	1066.4	195.2	10.3	1.4
.020	.045	1002.8	183.6	9.7	1.3
.020	.050	946.4	173.3	9.1	1.2
.020	.055	896.0	164.1	8.6	1.2
.020	.060	850.7	155.8	8.2	1.1
.020	.065	809.8	148.3	7.8	1.1
.020	.070	772.6	141.5	7.4	1.0
.020	.075	738.7	135.2	7.1	1.0
.025	.025	1211.4	221.8	11.7	1.6

Table 4-9. Thermal Resistance in Various Substrates (Continued)

[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
.025	.035	1044.3	191.2	10.1	1.4
.025	.040	976.9	178.9	9.4	1.3
.025	.045	917.7	168.0	8.8	1.2
.025	.050	865.3	158.4	8.3	1.1
.025	.055	818.5	149.9	7.9	1.1
.025	.060	776.5	142.2	7.5	1.0
.025	.065	738.7	135.2	7.1	1.0
.025	.070	704.3	129.0	6.8	.9
.025	.075	673.0	123.2	6.5	.9
.030	.030	1037.1	189.9	10.0	1.3
.030	.035	964.5	176.6	9.3	1.3
.030	.040	901.3	165.0	8.7	1.2
.030	.045	845.9	154.9	8.1	1.1
.030	.050	797.0	145.9	7.7	1.0
.030	.055	753.4	137.9	7.3	1.0
.030	.060	714.3	130.8	6.9	.9
.030	.065	679.0	124.3	6.5	.9
.030	.070	647.1	118.5	6.2	.8
.030	.075	618.1	113.2	6.0	.8
.035	.035	896.0	164.1	8.6	1.2
.035	.040	836.6	153.2	8.1	1.1
.035	.045	784.6	143.7	7.6	1.0
.035	.050	738.7	135.2	7.1	1.0
.035	.055	697.8	127.8	6.7	.9
.035	.060	661.2	121.1	6.4	.9
.035	.065	628.3	115.0	6.1	.8
.035	.070	598.5	109.6	5.8	.8
.035	.075	571.4	104.6	5.5	.7
.040	.040	780.5	142.9	7.5	1.0
.040	.045	731.5	133.9	7.0	1.0
.040	.050	688.3	126.0	6.6	.9
.040	.055	649.9	119.0	6.3	.8
.040	.060	615.5	112.7	5.9	.8
.040	.065	584.6	107.0	5.6	.8
.040	.070	556.7	101.9	5.4	.7
.040	.075	531.3	97.3	5.1	.7
.045	.045	685.2	125.5	6.6	.9
.045	.050	644.4	118.0	6.2	.8
.045	.055	608.1	111.3	5.9	.8
.045	.060	575.8	105.4	5.5	.7
.045	.065	546.7	100.1	5.3	.7
.045	.070	520.4	95.3	5.0	.7
.045	.075	496.5	90.9	4.8	.6
.050	.050	605.7	110.9	5.8	.8
.050	.055	571.4	104.6	5.5	.7

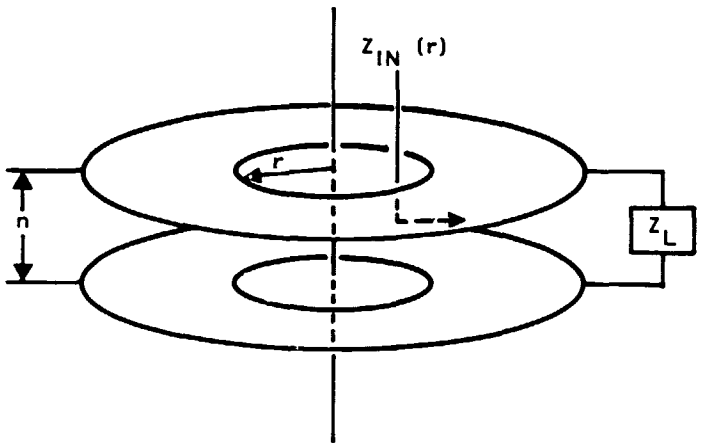


Figure 4-50(a). Radial Transmission Line

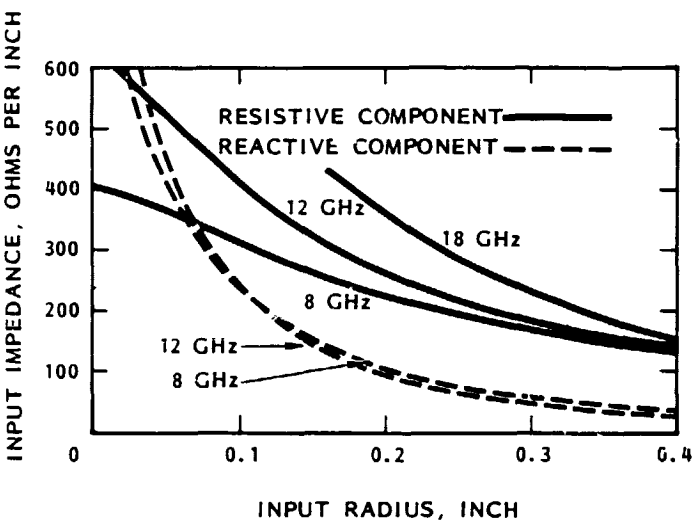


Figure 4-50(b). Effect on Input Impedance of Input Radius

The transmission line equations describing wave propagation on the radial line are:

$$\frac{dV}{dr} = - j\, k\, Z_o\, I$$

$$\frac{dI}{dr} = -j\, k\, Y_o\, V$$

$$Z_o = \frac{1}{Y_o} = \frac{\mu}{\varepsilon} \frac{h}{2\pi r}$$

These equations are similar to the wave equations for uniform transmission lines, with the exception that the characeristic impedance Z_o is a function of position. In fact, it is this 1/r dependence of Z_o which makes the radial line ideal as an impedance transformer in a combiner.

In addition to the load admittance, the substrate dielectric constant and the operating frequency must be specified to uniquely define the radial line geometry. In terms of the normalized parameters, the substrate thickness h (in inches) is given by:

$$h = \frac{\frac{Y}{L}\, y}{10.16\pi Y_L f_o}$$

where

Y/L = normalized load admittance

y = electrical length of outer radius

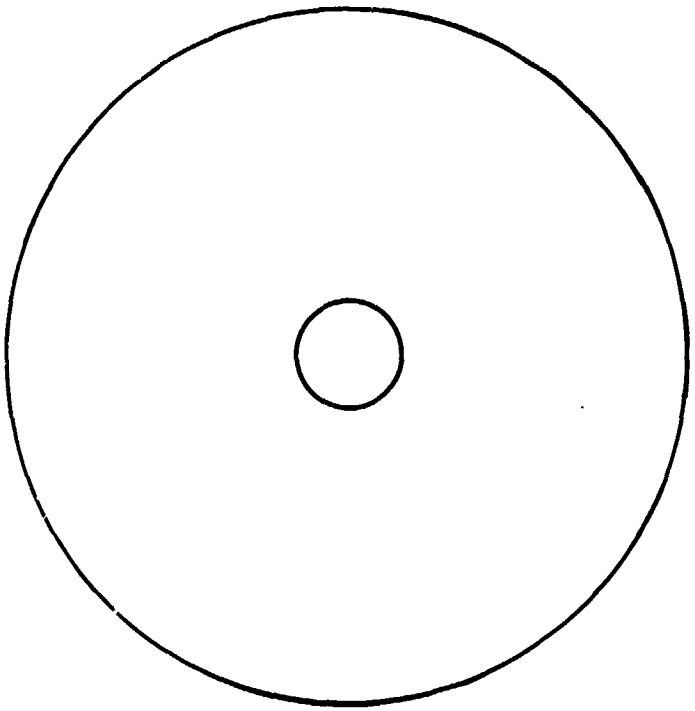
where f_o is the design center frequency in GHz. Of note, h is independent of the substrate dielectric constant. The substrate thickness h, the inner radius r_i, and the outer radius r_o are tabulated in Table 4-10 as a function of the normalized load admittance Y/L, for the following assumed conditions:

1) Total radial line load admittance, $Y_L = 0.16\ \nu$ (8/50 mhos)

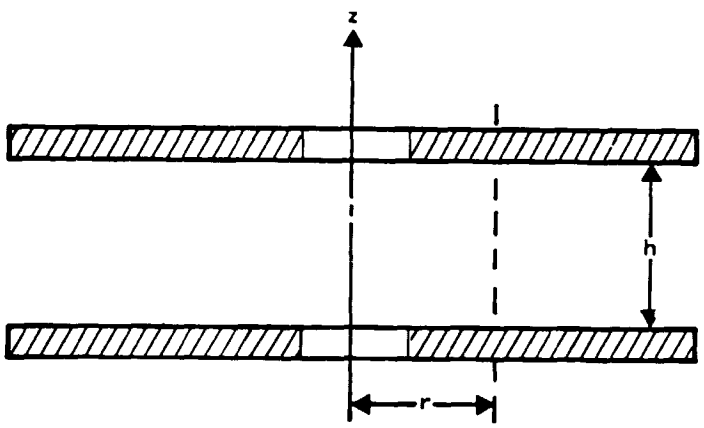
2) Design center frequency, f_o = 18 GHz

3) Substrate dielectric constant ε_Y = 3.78 (fused quartz)

The geometry of the radial transmission line is shown as follows in Figure 5-51.



TOP VIEW



SIDE VIEW

Figure 4-51. Geometry of the Radial Transmission Line

Table 4-10. Radial Line Parameters

Y/L	h (in.)	r_i(in.)	r_o(in.)
1.0	0.0347	0.0159	0.2571
1.1	0.0350	0.0166	0.2353
1.2	0.0360	0.0185	0.2224
1.3	0.0379	0.0215	0.2159
1.4	0.0404	0.0255	0.2135
1.5	0.0434	0.0304	0.2141
1.6	0.0469	0.0363	0.2170

In order to minimize the input Q and thereby maximize bandwidth, a value of Y/L close to unity should be chosen. On the other hand, with Y/L = 1, the required electrical length increases and a smaller inner radius, r_i, results. This can present fabrication difficulties for the coax-to-radial line transition and unwanted parasitics. As a compromise, Y/L was chosen to be 1.2. This will result in an input Q for the radial line divider/combiner of 1.93.

4.9.8 Coaxial to Radial Line Transition

Radial transmission line consists of two parllel conducting planes between which electromagnetic energy is propagated in a radial direction. An input impedance looking outward into the radial line at a given radius (r) reference plane can be derived. Figure 4-50b shows a plot of the input impedance as a function of the input radius for frequencies of 8 and 12 GHz. The impedance has been normalized to a groundplane spacing of unit, and the radial line is assumed to be terminated at a large radius by its characteristic impedance at that radius.

The reactive components of the input impedance increases rapidly with decreasing input radius. Consequently, entering the radial line at a large radius would appear advantageous However, an increase in the input radius reduces the real part of the input impedance, although to a lesser degree. Because the input impedance is proportional to the groundplane spacing h, the impedance can be scaled by adjustment of h. But increasingly larger input radii would require increasingly larger groundplane spacings for the

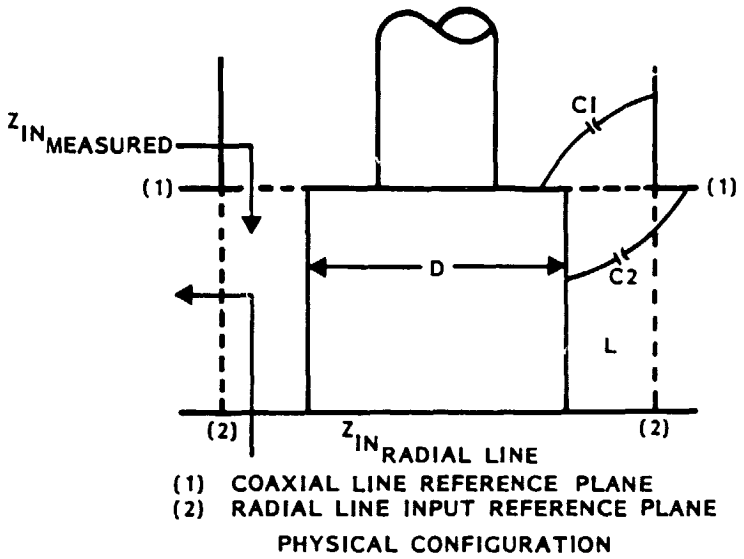
same impedance level to be maintained, and undesirable higher order propagating modes would then be introduced. Thus, a tradeoff exists between input radius and groundplane spacing. The equivalent circuit at the junction of the transition is shown in Figure 4-52.

4.9.9 Splitter/Combiner Design

Having shown the parameters that affect the performance of the radial splitter/combiner and the tradeoffs between the various parameters, a radial splitter/combiner was designed and optimized with computer aided design. Using a 0.025 inch thick beryllia substrate, the radial splitter/combiner layout is shown in Figure 4-53. The theoretical design results are shown in Figure 4-54. The components for the splitter/combiner are shown in Figure 4-55. The components are (clockwise from the scale):

- The top plate with the eight ridges for the waveguide-to-microstrip transitions
- The waveguide-to-coax transition where the coax probe is attached to the center of the beryllia substrate
- The bottom plate that mates with (1)
- The radial splitter/combiner microstrip circuit on beryllia and the transmission lines that connect the radial splitter/combiner to the waveguide-to-microstrip transitions
- The center hub that provides waveguide mode suppressor as well as tuning adjustment provisions if additional tuning is necessary.

Figure 4-56 shows how the components are placed before the final assembly of the radial splitter/combiner. The assembled radial splitter/combiner is shown in Figure 4-57.



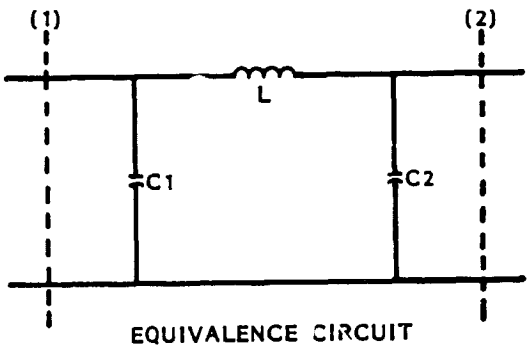


Figure 4-52. Modeling of Junction

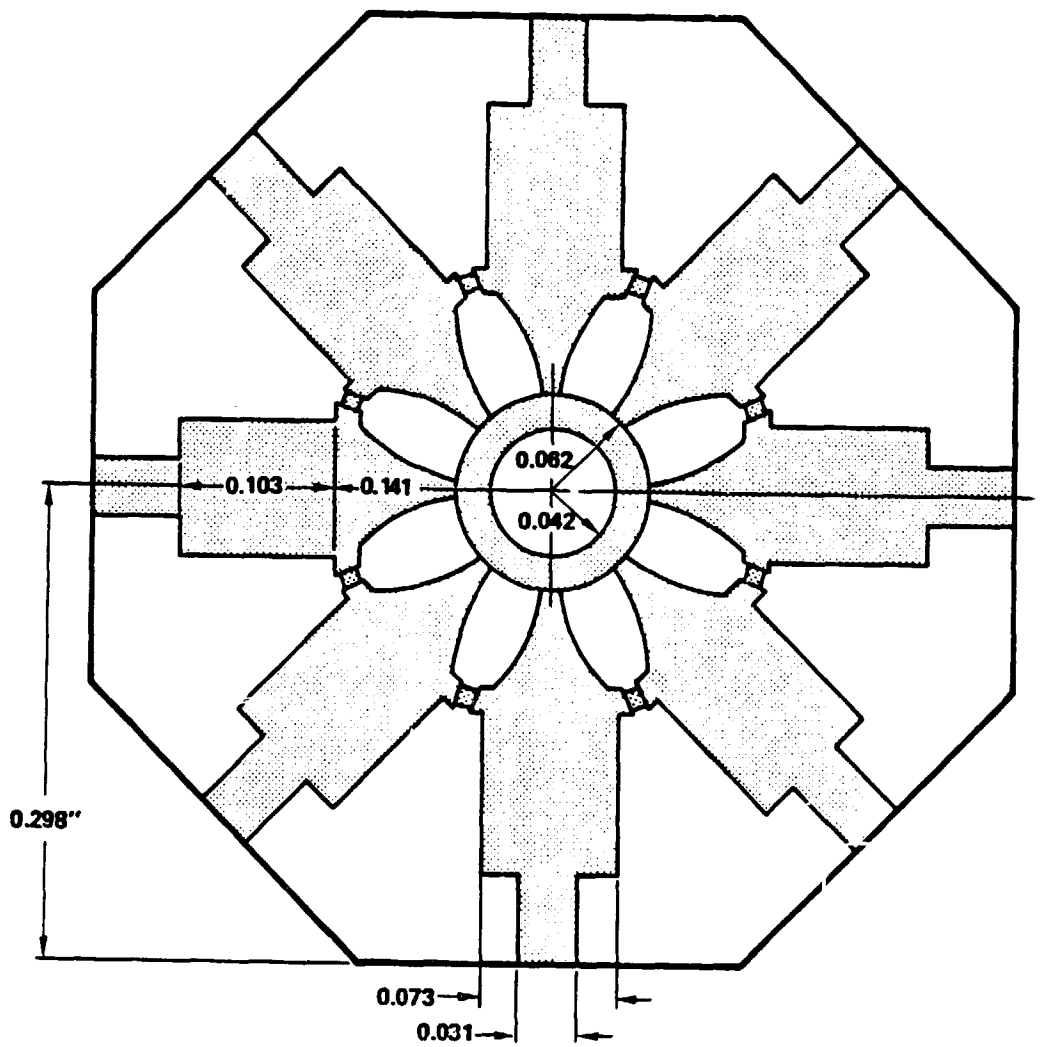


Figure 4-53. Splitter/Combiner Layout

FREQ.	RETURN LOSS				LOSS	ISOLATION			
	COMMON		1-8			1 TO 2	1 TO 3	1 TO 4	1 TO 5
GHz	dB	ANGLE	dB	ANGLE		1 TO 8	1 TO 7	1 TO 6	
17.50	16.2	132.2	15.2	144.5	9.14	15.7	23.7	18.4	17.6
18.00	16.6	121.2	17.7	139.4	9.13	15.3	24.3	18.5	17.6
18.50	17.7	104.8	21.8	136.5	9.11	15.0	24.9	18.6	17.7
19.00	19.2	79.4	31.1	152.6	9.09	14.7	25.5	18.7	17.8
19.50	19.8	41.4	27.2	-92.2	9.08	14.6	26.0	18.9	17.9
20.00	18.0	1.7	19.3	-87.1	9.11	14.6	26.4	19.2	17.2
20.50	14.9	-26.6	15.0	-92.1	9.18	14.7	26.7	19.5	18.5

Figure 4-54. 20-GHz Splitter/Combiner Design Results

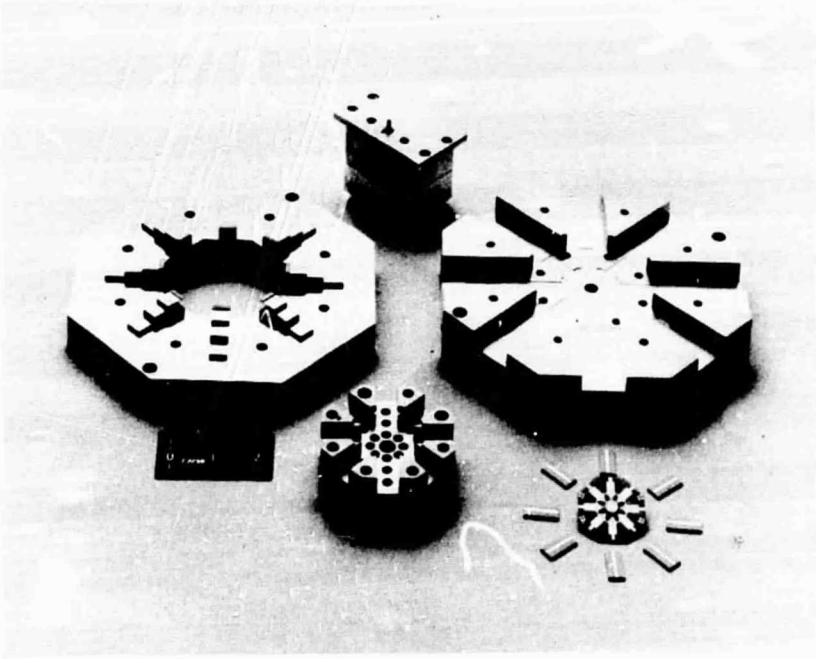


Figure 4-55. Splitter/Combiner Components

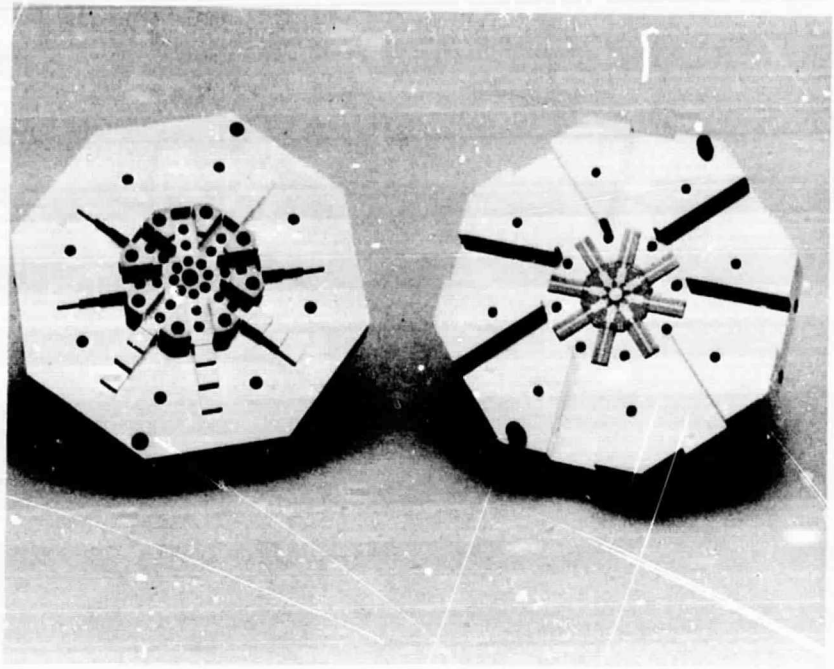


Figure 4-56. Splitter/Combiner Detail

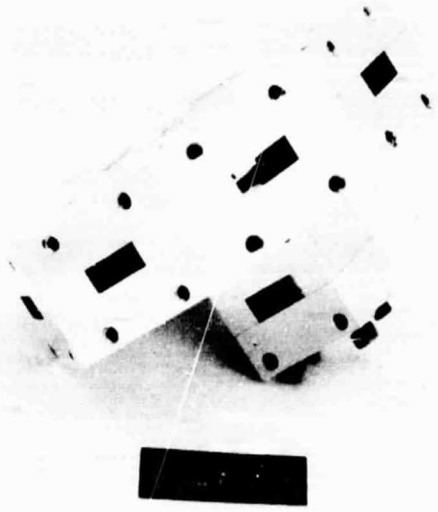


Figure 4-57. Assembled Splitter/Combiner

4.9.10 Splitter/Combiner Test Data

The splitter and the combiner were separately tested first. To test them separately required measuring the characteristics of each port with all other ports terminated with a 50-ohm load. After the transmission through each port for both the splitter and the combiner is optimized, the overall transmission of the radial splitter/combiner was measured by connecting the splitter and the combiner back-to-back through eight pairs of 90° waveguide bends. The performance characteristics of this set-up are shown in Figure 4-58. It is seen that the insertion loss was reasonably close to what was expected. This means that the phases through the eight paths are relatively uniform and the combining efficiency is very close to theoretical prediction.

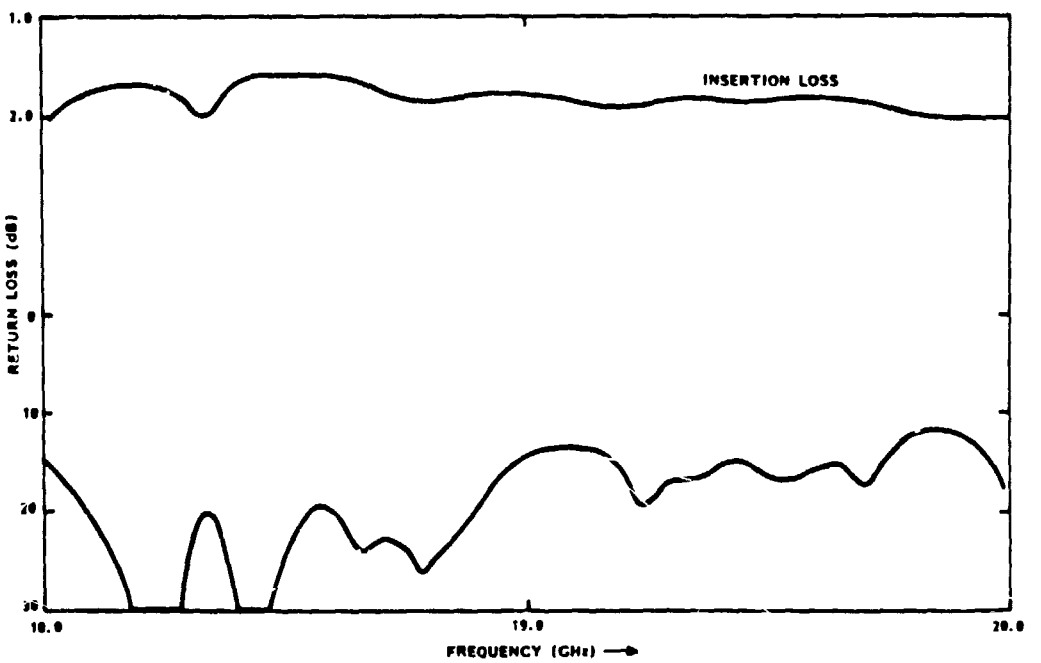


Figure 4-58. Loss Characteristics of Combiner/Divider Connected Back-to-Back

4.10 EIGHT-WAY COMBINED AMPLIFIER MODULE

4.10.1 Module Design

The eight-way combined amplifier module consists of the eight-way power splitter, the eight power amplifier modules and the eight-way power combiner, with input and output transitions to provide waveguide connectors. The performance characteristics of the individual components have been described in previous sections of this report. The assembling and the testing of these eight-way combined amplifier modules were the most critical tasks of the development of the POC assembly. Mechanically, the components all have to fit and, when assembled, form a sturdy and flight-worthy structure. Electrically, the amplitude and phase characteristics have to match within a specified range as described in Section 4.9.4. More critically, the procedure to assemble and test the complete module are complex. The procedure used is briefly described as follows:

1) After having tested the power divider and power combiner separately, one amplifier module was inserted between the divider/combiner with the other seven ports of the respective divider/combiner terminated with 50-ohm waveguide loads.

2) The output of the single-amplifier configuration was measured. Since the other ports were all terminated, the output of this configuration should be the sum total of the performance characteristics of the divider, single power amplifier module, and the combiner.

3) Having ascertained that the single-amplifier configuration was working properly, a second amplifier module was added. To alleviate unwarranted uncertainties, symmetry was mantained by inserting the second amplifier module physically opposite to the first module already inserted. Thus, if the position of the first amplifier module was marked as "1," the second amplifier module was inserted at a position marked as "5." The 50-ohm waveguide loads were still in place at all of the other ports.

4) The output of the two-amplifier configuration was measured, and the output should have been the sum total of the output power of the two amplifier modules minus the insertion losses due to other passive components and loss due to combining of the two modules. The combining loss was minimized by judiciously choosing the two amplifier modules with best amplitude and phase matching.

5) The third amplifier module was then inserted in position "3," and the output performances were optimized.

6) The four-amplifier configuration followed by inserting the fourth amplifier module in position "7." Again, amplifier modules for "3" and "7" have similar amplitude and phase characteristics to maintain symmetry.

7) The fifth amplifier module was inserted in posotion "2," and the output performances were optimized.

8) The six amplifier configuration had the sixth amplifier module in position "6."

9) The seventh amplifier module was inserted in position "4" and the output performances were evaluated.

10) Finally, all eight modules were put together to form the eight-way combined amplifier module.

4.10.2 Amplitude/Phase Configuration

As mentioned in Section 4.9.4, the combined efficiency of the radial combiner depended heavily on the phase matching of the modules to be combined and less critically on the amplitude matching. Furthermore, the amplitude characteristics of the modules were made to match closely enough by choosing appropriate individual amplifier stages that formed the modules. The variations in transmission phases, however, could easily be caused by a short length of transmission line (i.e., the electrical equivalent length due to any irregularities) at these frequencies. On the other hand, because of the fact that a short length of transmission line does represent a sizable phase shift at these frequencies, the phase differences can easily be compensated by inserting short lengths of transmission line in the form of waveguide shims. The advantages of using the waveguide shims are: 1) they do not destroy the broadband electrical performance, and 2) they are mechanically easy to implement.

To measure the absolute transmission phase of the amplifier modules is relatively complex at these frequencies. However, the differential transmission phases between the modules can be determined comparatively easily. By means of a differential phase measuring technique in the form of a bridge, the transmission phase of each module as compared with a reference transmission phase through a reference arm is determined. A waveguide shim with appropriate thickness is then inserted to minimize that phase differential. The phase compensation on all of the eight modules were

performed using this method. After phase compensation, the modules were ready to be combined. Figure 4-59 shows the results of the phase matching on these modules.

4.10.3 Module Integration and Test Data

Following the procedures described in Section 4.10.1 and 4.10.2, the power modules were inserted between the divider and the combiner to form the assembly with a block diagram shown in Figure 4-60. Nominally, the output power of each power module is 1.25 W. A total power of 10 W is available by combining eight of them. An output power of 8 W can reasonably be achieved with the insertion losses of the divider and the combiner, if the combining efficiency is sufficiently high. However, some of the power modules have output power as much as 1.5 W; this provided some margin of safety. The eight-way combined module is shown in Figure 4-61.

The combined output power of the module was measured at 8.2 W. This was surprisingly good result and indicated that all of the precautionary actions taken on this program had paid off handsomely.

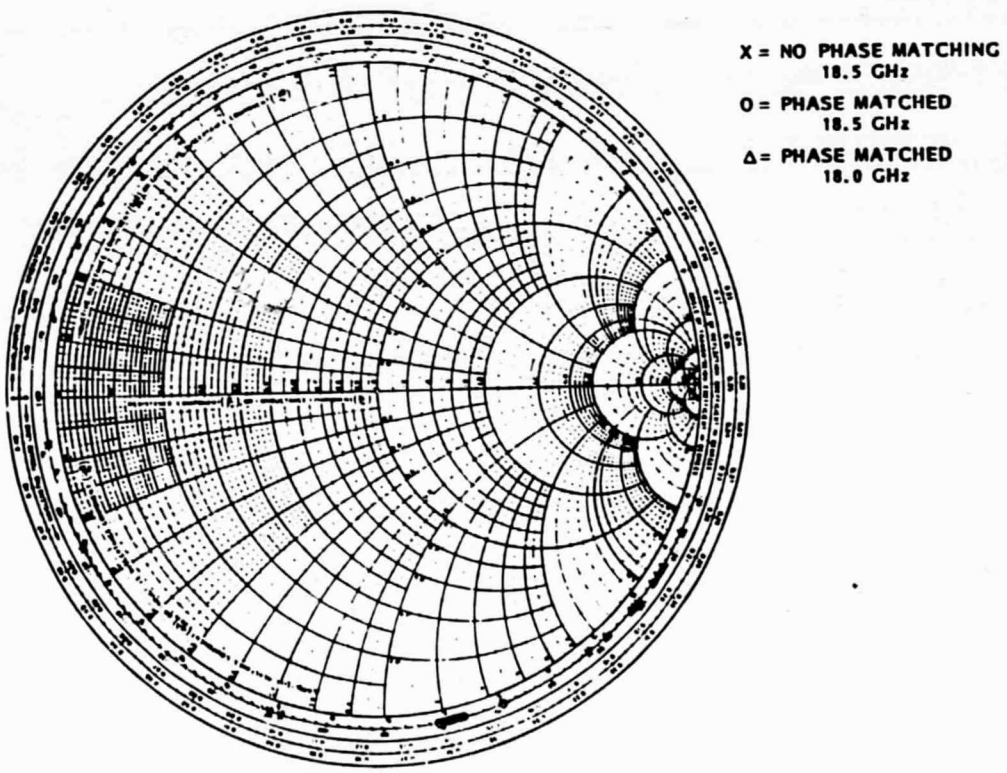


Figure 4-59. Phase Matching of 20 GHz FET Amplifier Modules

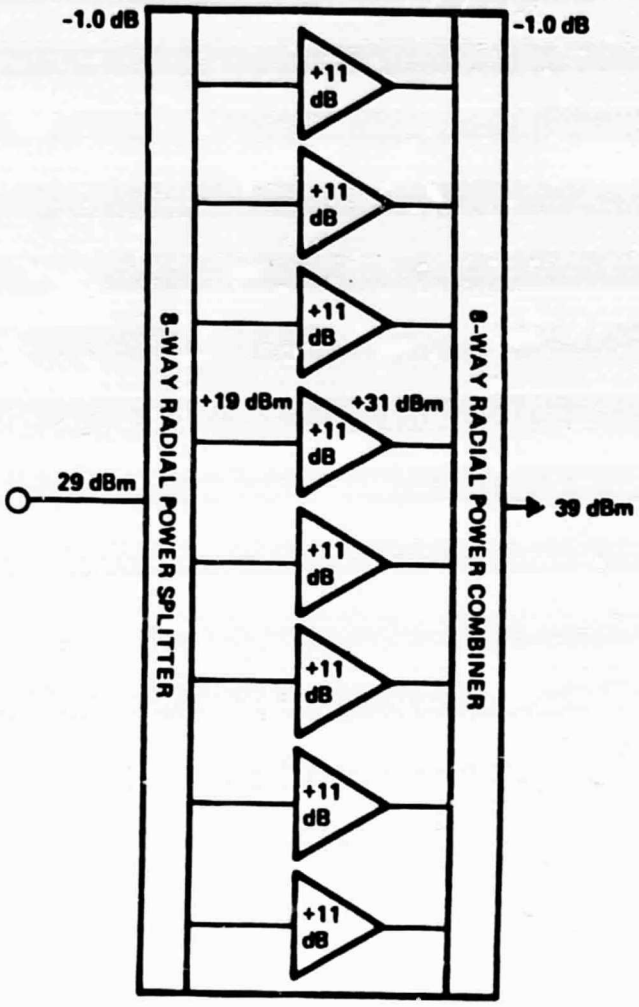


Figure 4-60. Eight-Way Combined Module Block Diagram

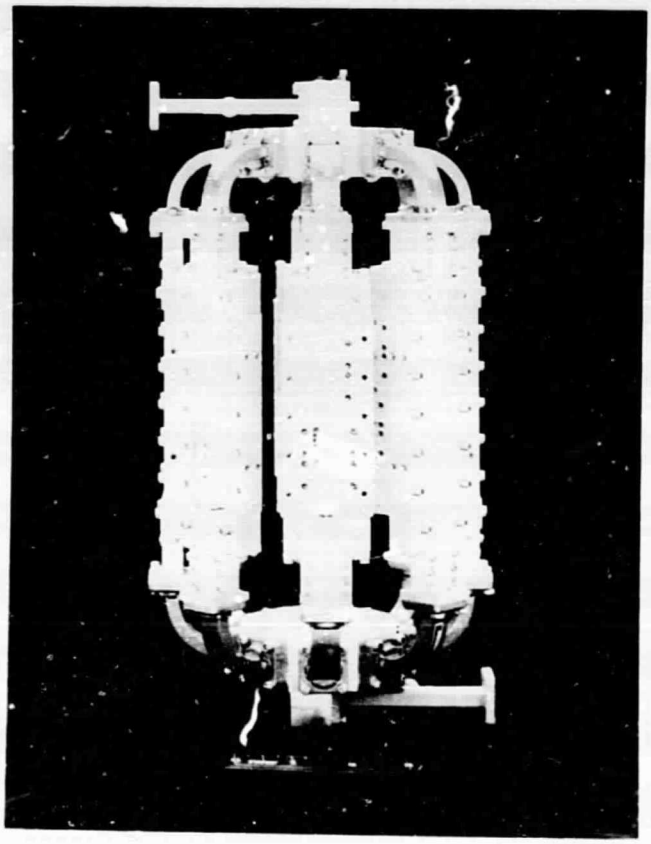


Figure 4-61. Assembled Power Amplifier

4.11 GRACEFUL DEGRADATION

It is appropriate to describe a very important advantagous feature of the solid state power amplifier over TWT. Over the years, such claims have been made, and theoretical calculations have shown the feature of graceful degradation of solid state power amplifiers using output combining to achieve the required output.

Basically, when a TWT fails, there is no transmitter output and, therefore, the transmitter is no longer operative. However, with solid state power amplifiers, should one or more of the power amplifiers used to be combined to form the output stage fails, there will be a reduced output power, but the transmitter is not totally nonoperative. Thus, the mission may have to operate at a reduced capacity but does not have to be aborted.

Theoretical output power is calcuated from the relationship of

$$P_{out} = P_{outmax} \left(\frac{M}{N}\right)^2 ,$$

where

M = number of working amplifiers

N = total number of amplifiers

Poutmax = output power with all amplifiers working

Assuming P_{outmax} is 9 W, Table 4-11 shows the theoretical and measured P_{out} data by turning off one amplifier at a time.

The theoretical calculation is based on equal output power of 1.25 W for each module. Since some of the actual power modules have output power of 1.5 W, the measured P_{out} might appear to be higher than the calculated data. Nevertheless, the measured data agrees with theory.

Table 4-11. Graceful Degradation Data

Number of Amplifiers "ON"	Measured P_{out} (Watts)	Theoretical P_{out} (Watts)
8	8.20	9.00
7	6.44	6.89
6	5.12	5.10
5	3.51	3.52
4	2.20	2.25
3	1.26	1.27
2	0.540	0.56
1	0.183	0.140

4.12 REGULATOR

4.12.1 Regulator Design

The following requirements must be taken into account when designing the regulator circuits:

1) Provide a regulated $+V_D$ which will supply a quiescent current of $\geq I_{DSS/2}$ to the device
2) Provide a regulated $-V_G$ which once adjusted for $I_{DSS/2} = I_D$ will maintain the device operating point as shown in Figure 4-62.
3) Provide intrinsic current limit for V_D; i.e., keep I_D from reaching I_{DSS} with the loss of gate bias
4) Provide protection if the gate is accidentally shorted to drain during RF tuning of the amplifier
5) Provide transient protection through bias
6) Prevent V_D from increasing as a result of any increase due to self-biasing through some resistive network when the gate is biased "OFF."

The regulator circuit that met all of these criteria is shown in Figure 4-63. The design is for all types of FETs used for the POC assembly. Due to the current requirements for the different types of FET, R_1, R_2, and R_3 have to be appropriately chosen as shown in the table included in Figure 4-63.

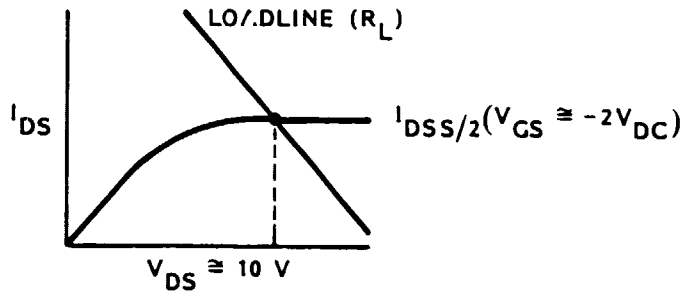
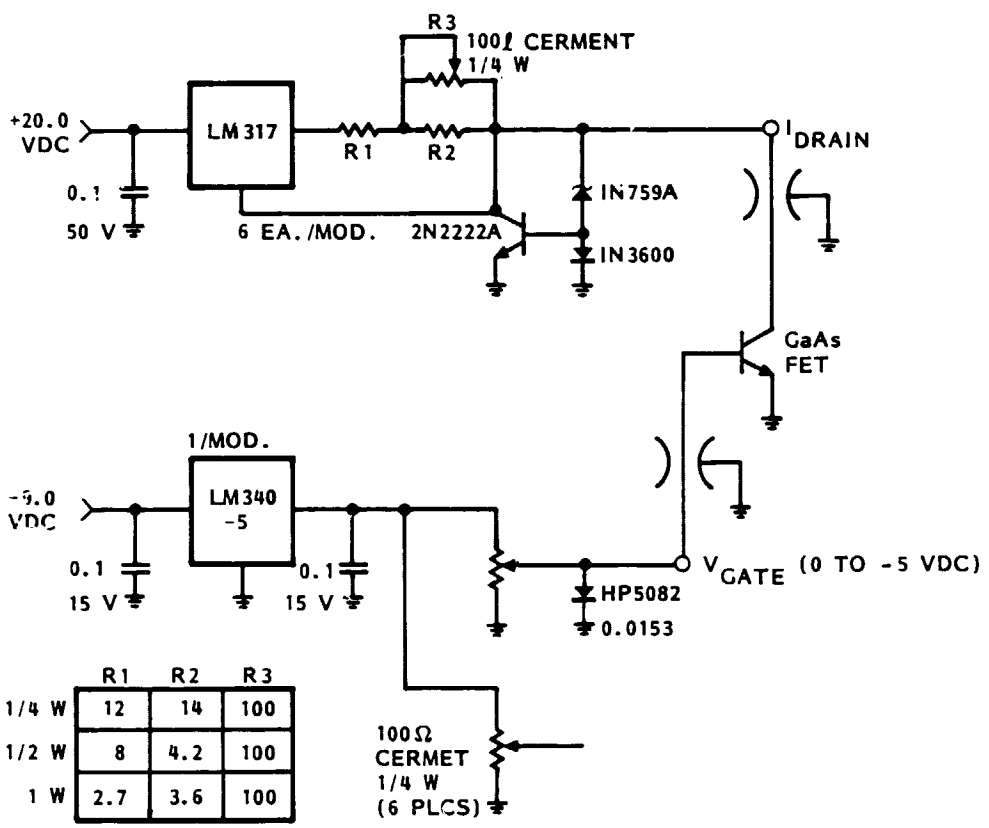


Figure 4-62. FET Operating Conditions



	R1	R2	R3
1/4 W	12	14	100
1/2 W	8	4.2	100
1 W	2.7	3.6	100

NOTE: ALL RES. 1/4 W 5% VAL. IN OHMS
ALL CAP. μF

Figure 4-63. NASA 20/30 Bias Regulator

4.12.2 Regulator Boards

There are six FETs in ea of the driver modules and the amplifier modules. A regulator as shown in Figure 4-62 is required for each of the FETs. It was, therefore, decided to make a regulator board with six regulators to serve each module. The final POC assembly has ten regulator boards for the ten modules which constitute the overall 20 GHz GaAs FET transmitter.

4.13 WAVEGUIDE MODE SUPPRESSOR

In order to accommodate six amplifier stages in each of the driver modules and the power modules, the modules have dimensions that will support undesirable higher order modes. These higher order modes will generally have additional spurious responses and will also cause the amplifier to oscillate. It is, therefore, necessary to incorporate these waveguide mode suppressors.

Figure 4-64 shows the equation and the dimensions of the waveguide mode suppressor for the cutoff frequency required.

Figure 4-65 shows the photograph of the mode suppressor used for these amplifier modules.

With the dimensions for this perticular design, the cutoff frequency is 30 GHz, which eliminated any waveguide modes below 20 GHz.

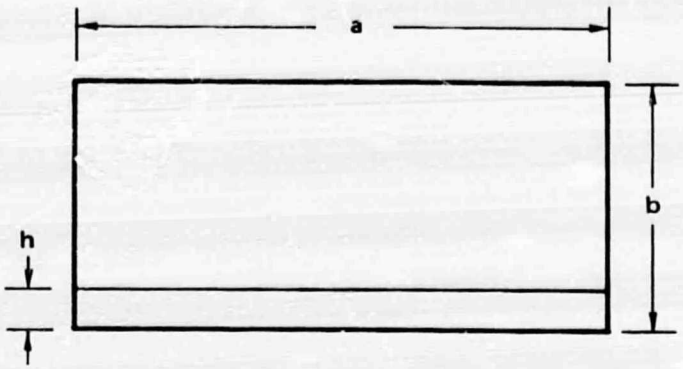
4.14 POC AMPLIFIER ASSEMBLY

4.14.1 POC Assembly Design

The overall POC amplifier is ready to be assembled. Referring to the block diagram of the 20 GHz transmitter shown in Figure 2-1, since it is only a P.O.C, the redundancy feature in the driver module was eliminated. Figure 4-66 shows the block diagram of the final POC assembly configuration. Figure 4-67 is a photograph of the POC assembly. Figure 4-68 shows in detail the solid state transmitter packaging.

The procedure of assembling the POC amplifier is briefly reviewed:

1) The driver amplifier module and nine (9) power amplifier modules were separately assembled and tested



$$FO = \frac{C}{2a}\sqrt{1 - \frac{h(\epsilon_N - 1)}{b\epsilon_N}}$$

Fo = CUT OFF FREQUENCY OF LOWEST WAVE GUIDE MODE

h = HEIGHT OF MICROSTRIP SUBSTRATE

a = CHANNEL WIDTH

b = CHANNEL HEIGHT

ϵ = RELATIVE DIELECTRIC CONSTANT

Fc $\approx$ 30 GHz

Figure 4-64. Waveguide Below Cut-Off Calculations

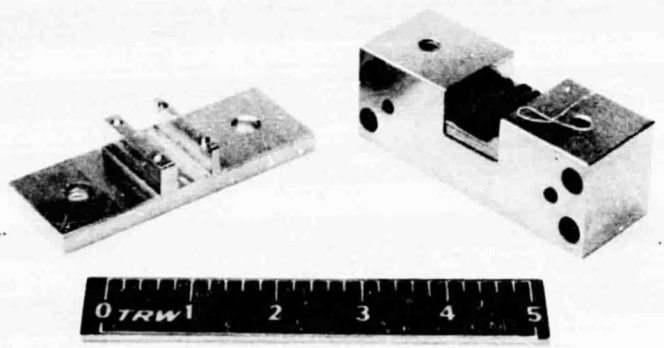


Figure 4-65. Waveguide Mode Suppressor

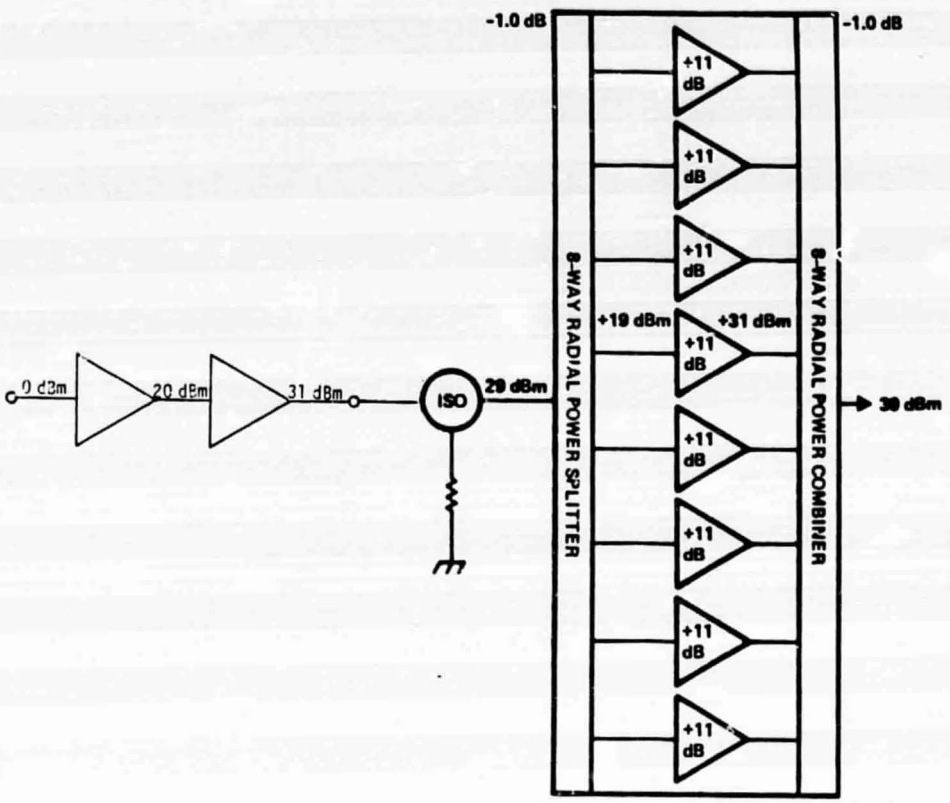


Figure 4-66. 20 GHz Transmitter System Block Diagram

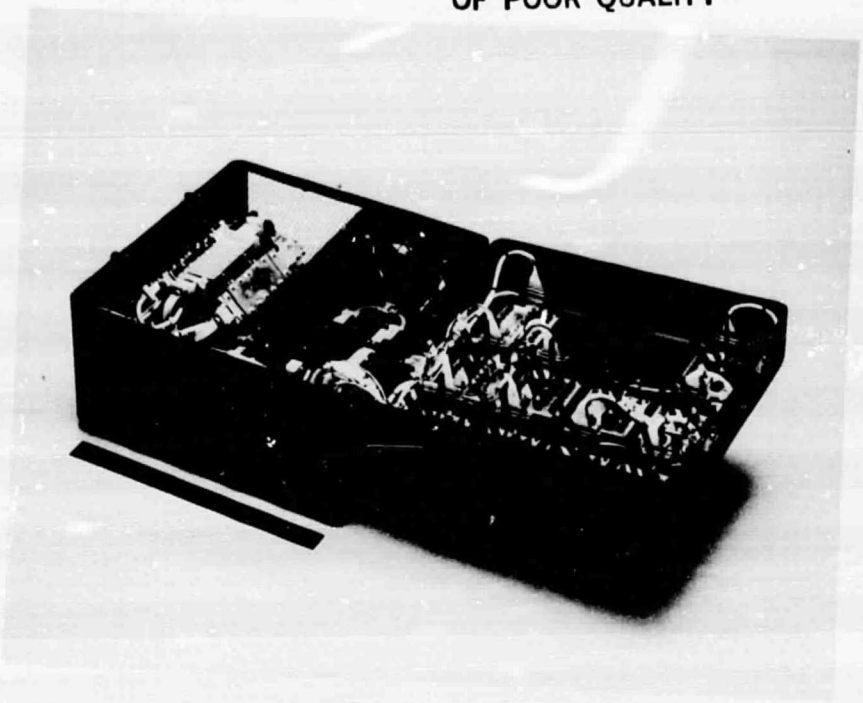


Figure 4-67. POC Assembly

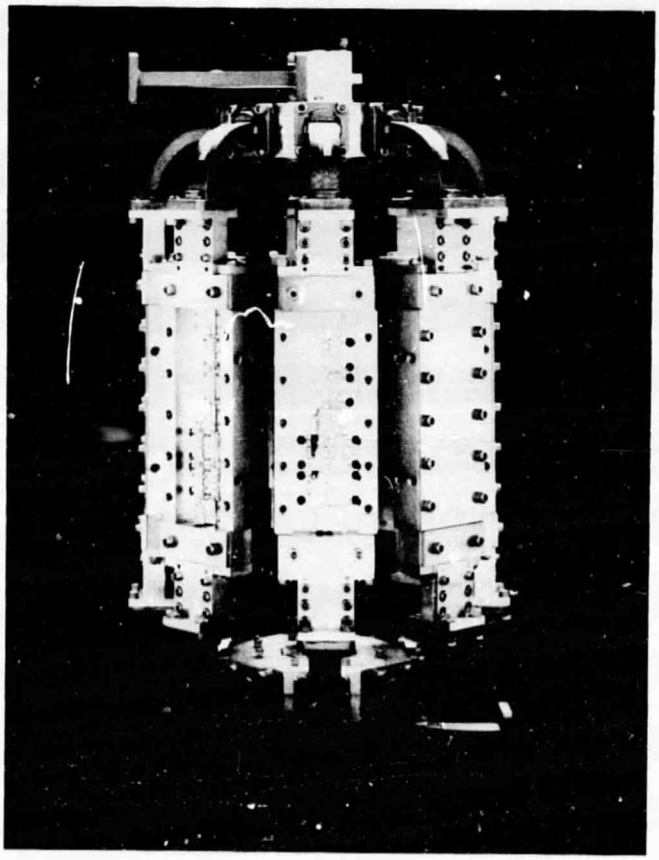


Figure 4-48. Solid State Transmitter Packaging

2) The driver module and one of the power modules were used to drive the eight-way combined amplifier power

3) The radial divider/combiner circuits were developed and evaluated

4) The eight-way combined amplifier module was developed and tested

5) The POC amplifier was assembled using these pretested components.

4.14.2 POC Assembly Test Data

Comprehensive tests were performed on the POC assembly. The list of tests and the corresponding figures that follow showing the test data are indicated in Table 4-12.

Table 4-12. Listing of Tests

Frequency Responses	Figure 4-69
P_{in}/P_{out}	Figure 4-70
Return Loss	Figure 4-71 and 4-72
IMD_3	Figure 4-73
Phase Linearity	Figure 4-74
Group Delay	Figure 4-75
AM/PM Conversion	Figure 4-76
Noise Figure	Figure 4-77
DC to RF Efficiency	Figure 4-78 and 4-79
Power added Efficiency Summary	Figure 4-80

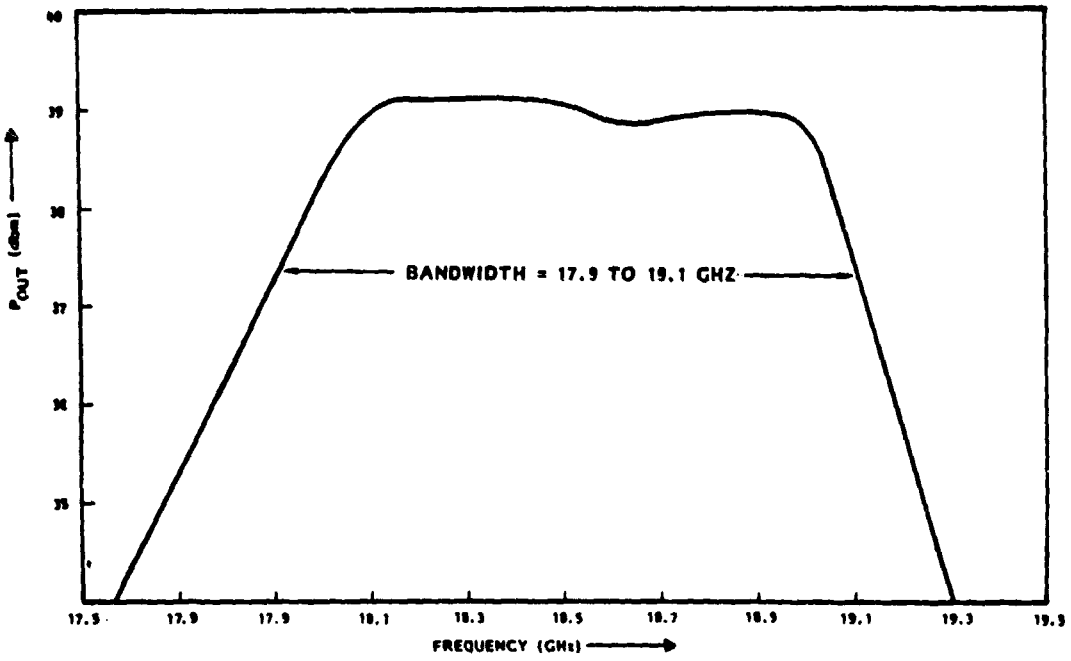


Figure 4-69. NASA 20 GHz FET Transmitter Frequency Response

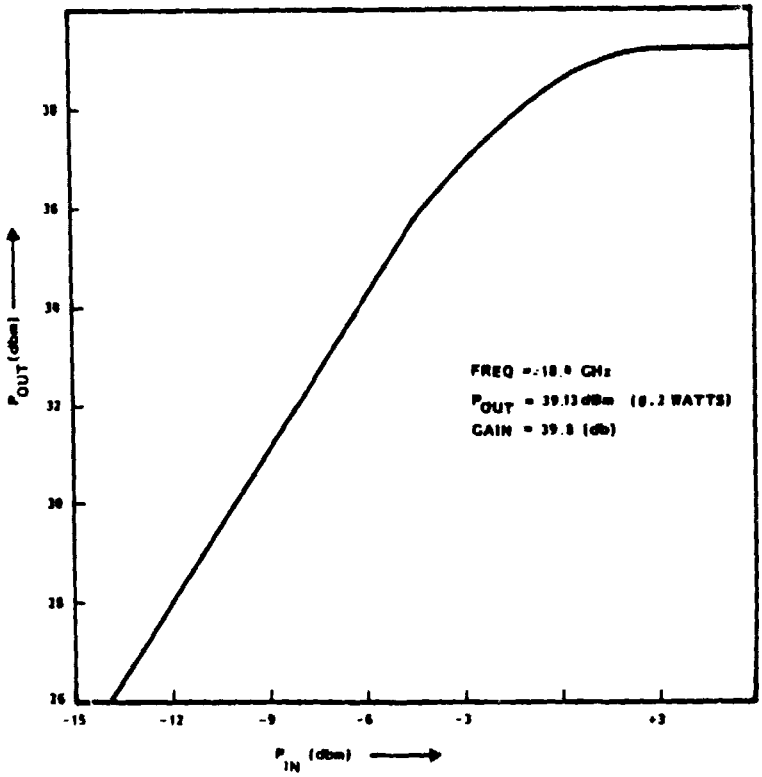


Figure 4-70. NASA 20 GHz FET Transmitter P_{IN}/P_{OUT} Characteristics

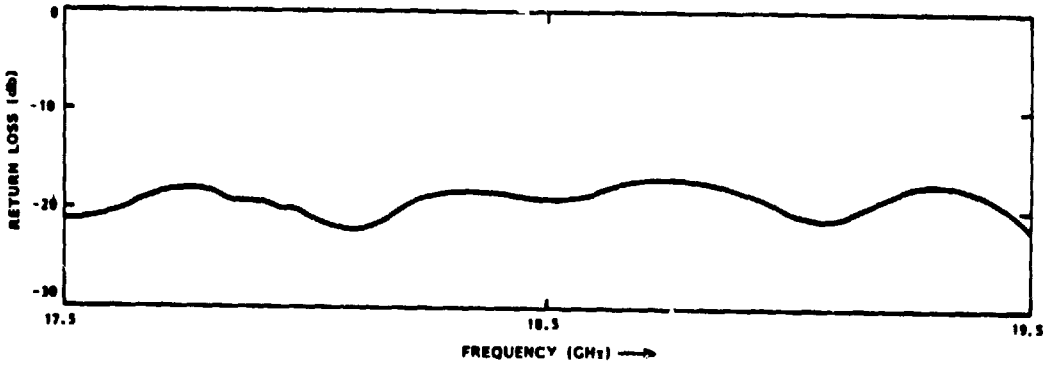


Figure 4-71. NASA 20 GHz FET Transmitter Input Return Loss

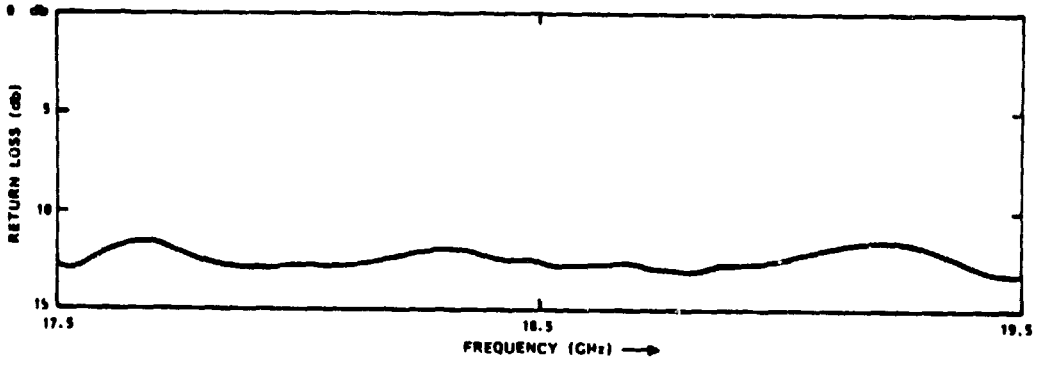
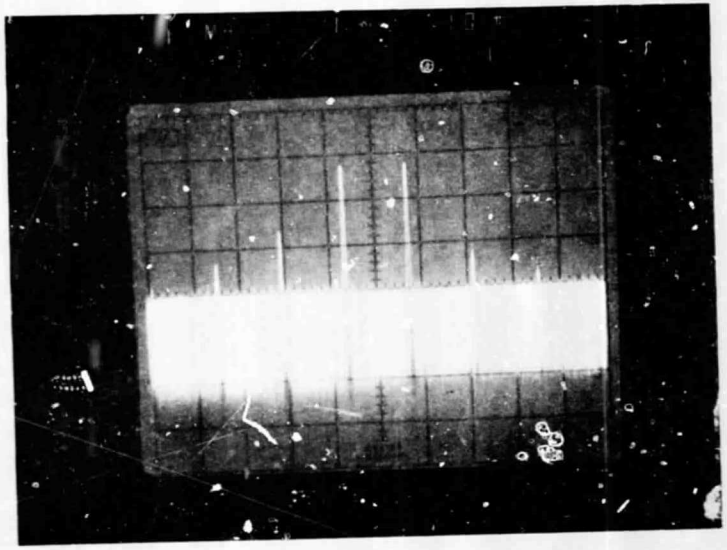


Figure 4-72. NASA 20 GHz FET Transmitter Output Return Loss

FREQUENCY = 18.5 GHz

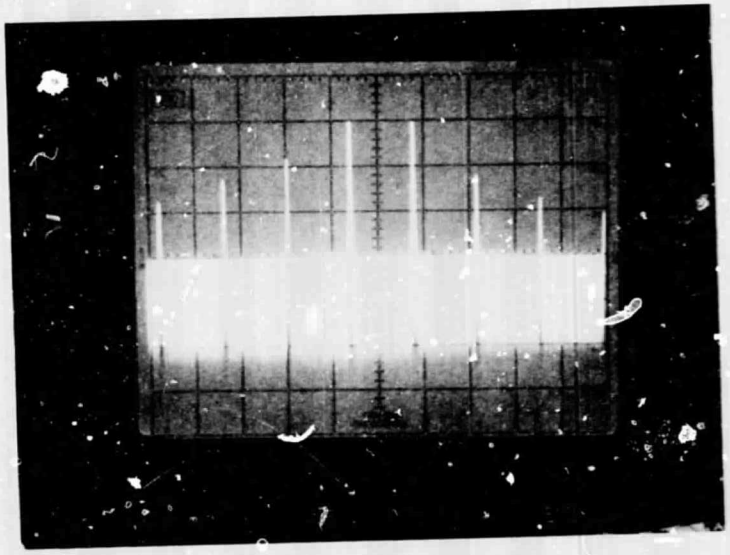
P_{in} = -2 dBm



10 dB/DIV

50 MHz/DIV

P_{in} = +3 dBm



10 dB/DIV

50 MHz/DIV

Figure 4-73. Intermodulation Characteristics of 20 GHz FET Transmitter

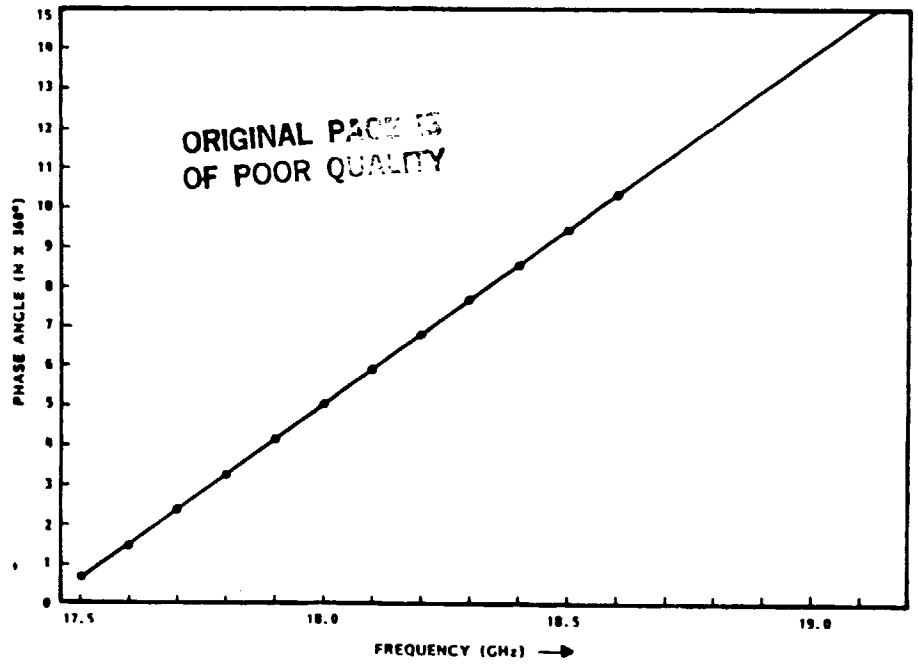


Figure 4-74. NASA 20 GHz FET Transmitter Phase Linearity

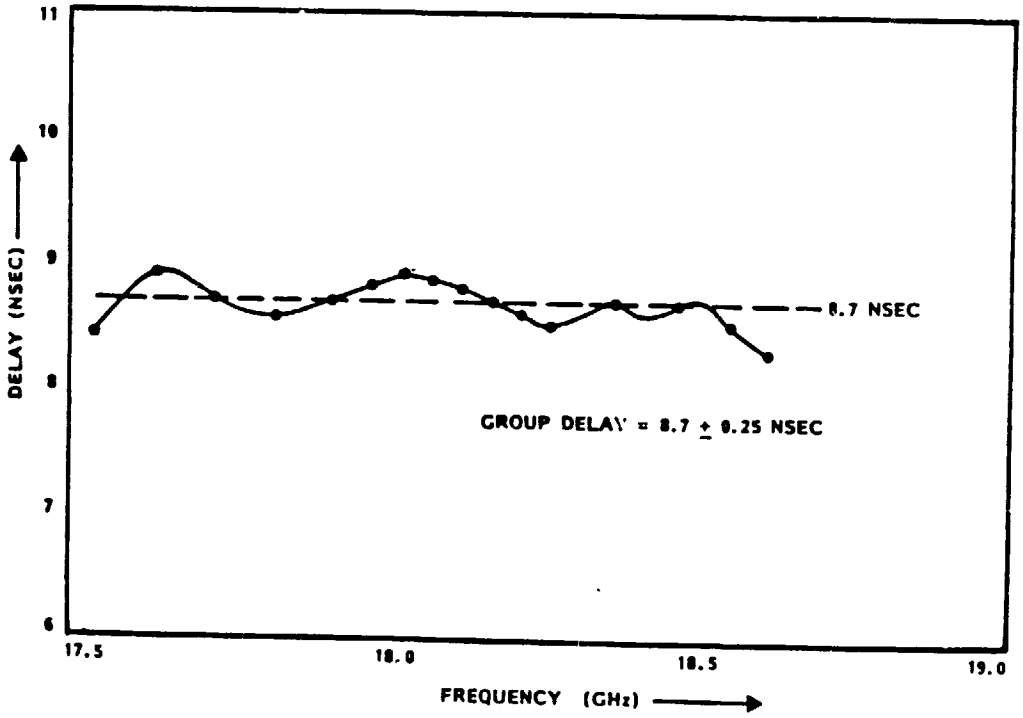


Figure 4-75. 20 GHz NASA FET Transmitter Group Delay Response

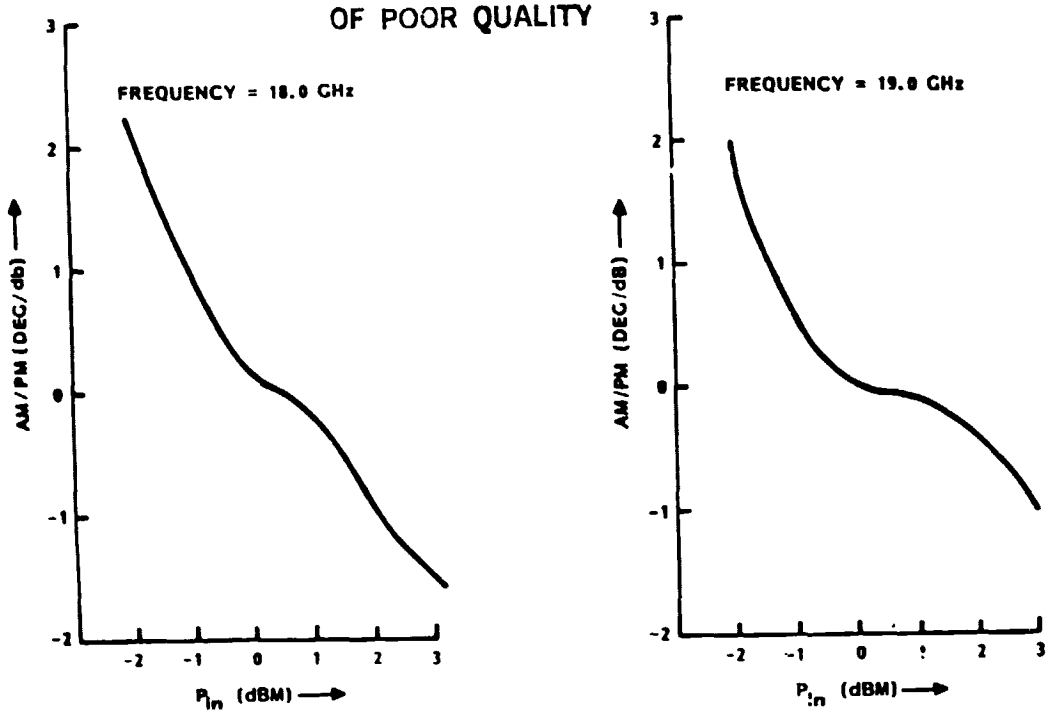


Figure 4-76. NASA 20 GHz FET Transmitter AM/PM Conversion

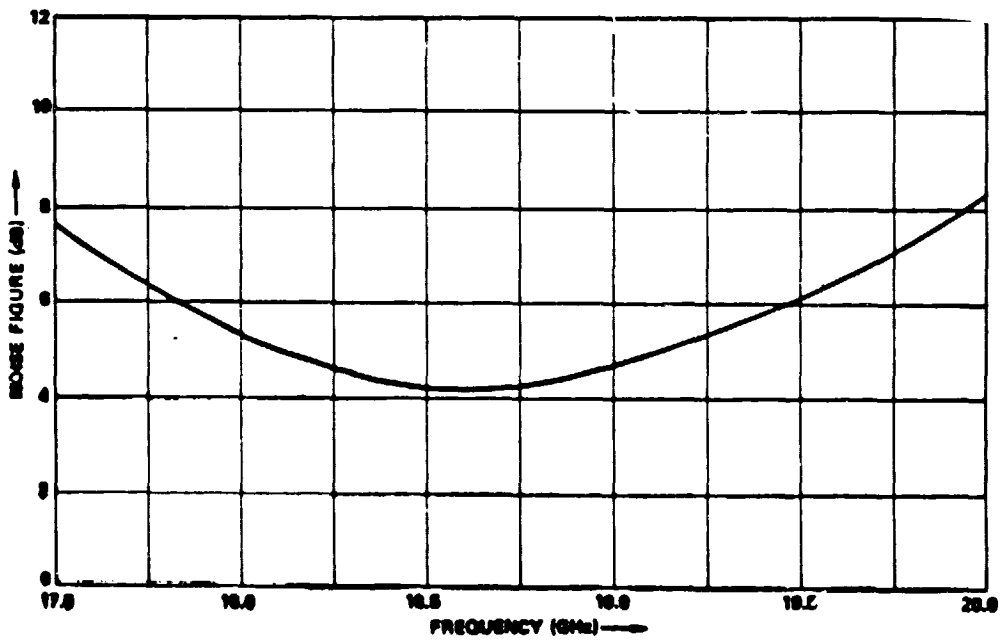


Figure 4-77. Driver Module Noise Figure Performance

	EFFICIENCY (%)	TEST CONDITIONS
1) DEVICE η AT 10 GHZ (NARROWBAND)	20	(V_D = 10 V, I_D = 350 P_o = 1.0 W GAIN = 5 DB)
2) SINGLE-STAGE EFFICIENCY (BROADBAND)	17	(V_D = 10 V, I_D = 250 P_o = 0.8 W GAIN = 3.5 DB)
3) POWER MODULE EFFICIENCY	13.3	ASSUMING SIMILAR EFFICIENCY FROM 1/2 W
4) UNIT AMPLIFIER EFFICIENCY	10.7	EIGHT MODULES COMBINED WITH RADIAL COMBINER/ DIVIDER

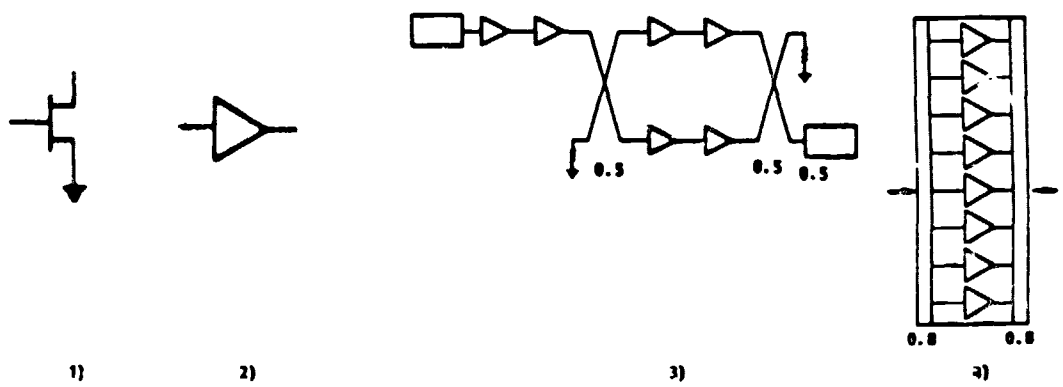


Figure 4-79. Degradation of Efficiency from Device to Unit Amplifier Level

	I_{DC}(AMPS)	V_D(V)	P_{DC}(W)
MODULE NO. 1	0.317	9.8	3.1
MODULE NO. 2	1.05	9.8	10.29
MODULE NO. 3	1.04	9.8	10.19
MODULE NO. 4	1.01	9.8	9.89
MODULE NO. 5	1.02	9.8	9.89
MODULE NO. 6	1.06	9.8	9.99
MODULE NO. 7	1.12	9.8	10.38
MODULE NO. 8	1.15	9.8	10.97
MODULE NO. 9	1.07	9.8	11.27
MODULE NO. 10		9.8	
TOTAL	9.79 A	9.8 V	95.96 W

$$\eta_{PA} = 8.54\%$$

Figure 4-80. Power Added Frequency

5. MECHANCIAL CONSIDERATIONS

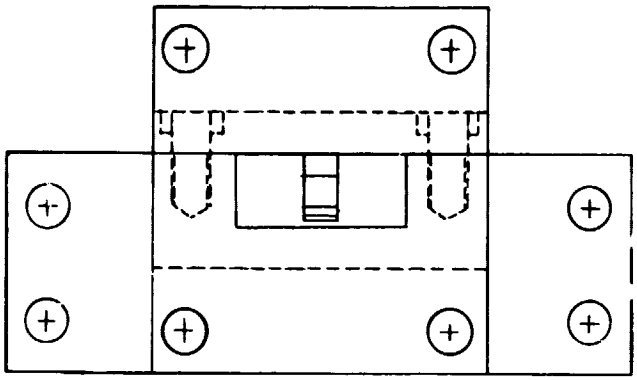
5.1 WAVEGUIDE TO MICROSTRIP TRANSITION

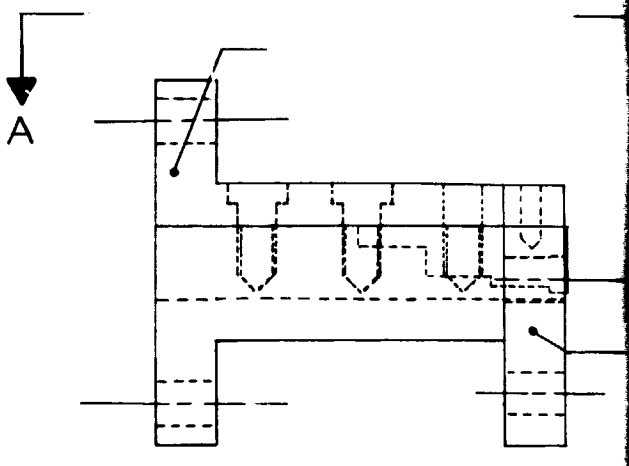
The input and output of each submodule is waveguide, but the amplifiers are done in microstrip; consequently, a waveguide-to-microstrip transition is necessary. The transition is designed in two pieces to simplify fabrication. Figure 5-1 is a drawing of the assembled transition. The lower half (Figure 5-2) consists of a channel machined to waveguide dimensions and a flange at each end. The flange at the waveguide port is a standard UG-595/U rectangular flange. The upper half contains the transition ridge and forms the top of the waveguide. When assembled, the last step of the ridge is 0.015 inch from the waveguide surface. This assures that when interfaced with a 0.015 inch quartz substrate, the step touches the microstrip line, and the ground planes of the substrate and waveguide line up.

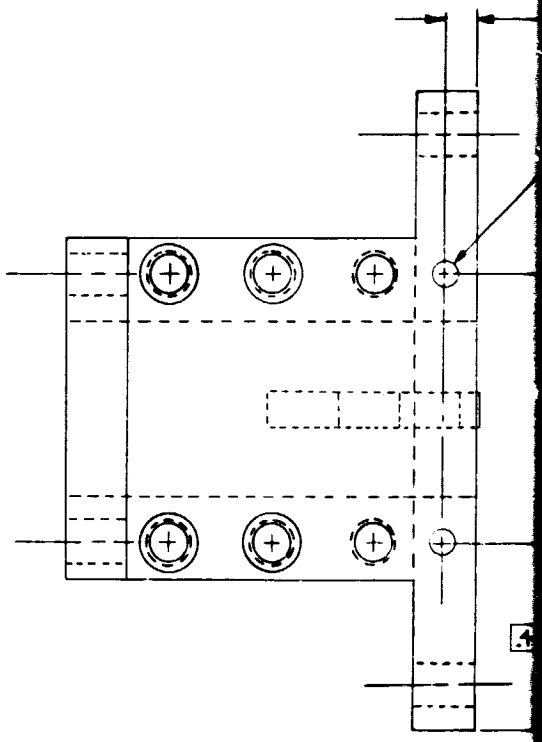
The waveguide-to-microstrip transition is assembled to a thruline housing (Figure 5-3). This housing is simply a block with a short length of substrate mounted in a narrow channel for mode suppression. The flange at the microstrip port of the transition contains two small holes. Screws through these holes secure the transition to the thruline housing, and a gold ribbon is connected between the ridge and the microstrip line on the thruline substrate. The other four holes are clearnace holes (which also appear in the thruline) that are for screws to connect the transition/thruline assembly to the amplifier submodule.

5.2 LANGE COUPLERS

The Lange coupler is etched on a 0.015 inch quartz substrate that is soldered to a gold-plated Invar shim. The shim prevents cracking of the substrate due to thermal stress. The substrate/shim assembly is epoxied to the coupler carried (Figure 5-4). The recess in the carrier facilitates proper alignment of the substrate. The carrier has clearance holes for mounting the assembly into the submodule.

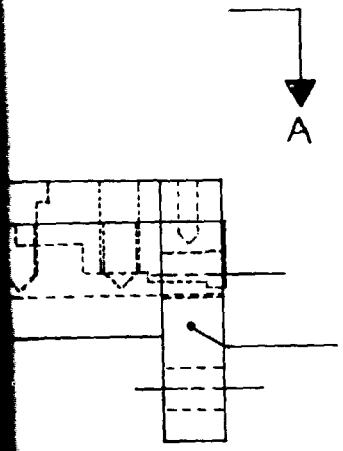


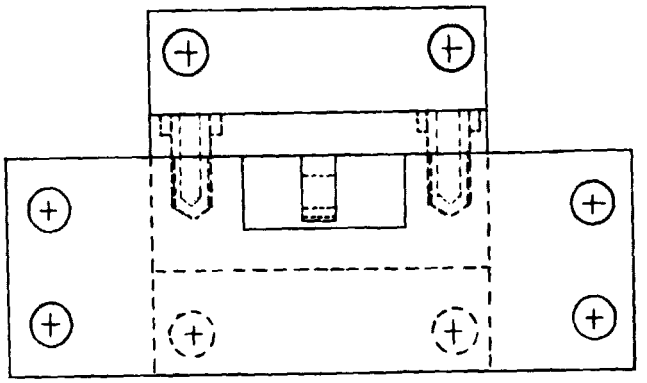


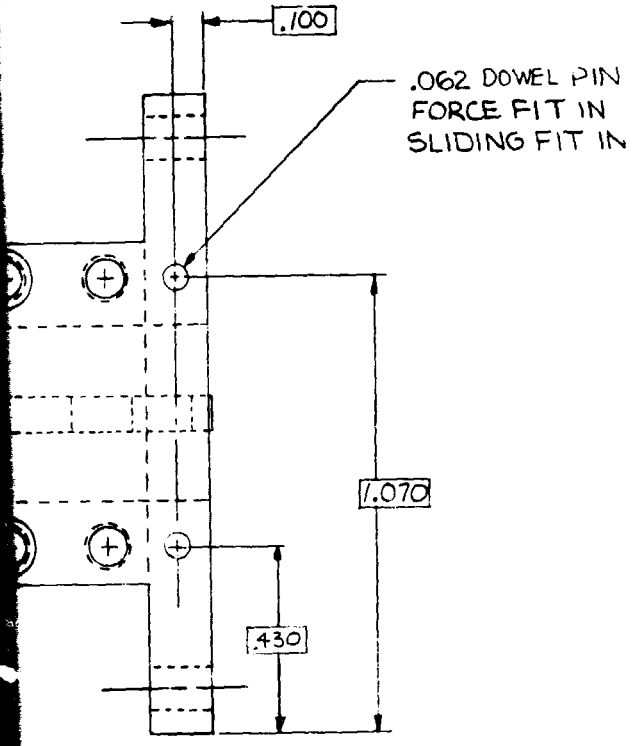


VIEW A-A

FOLDOUT FRAME



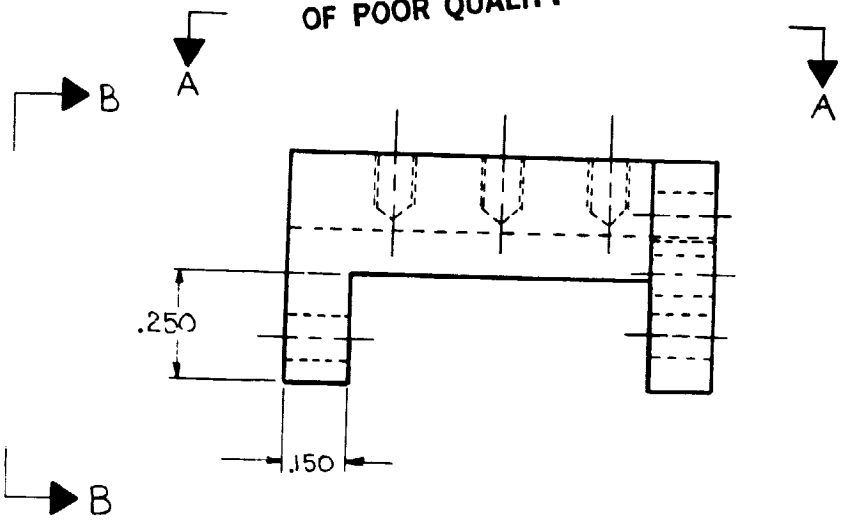


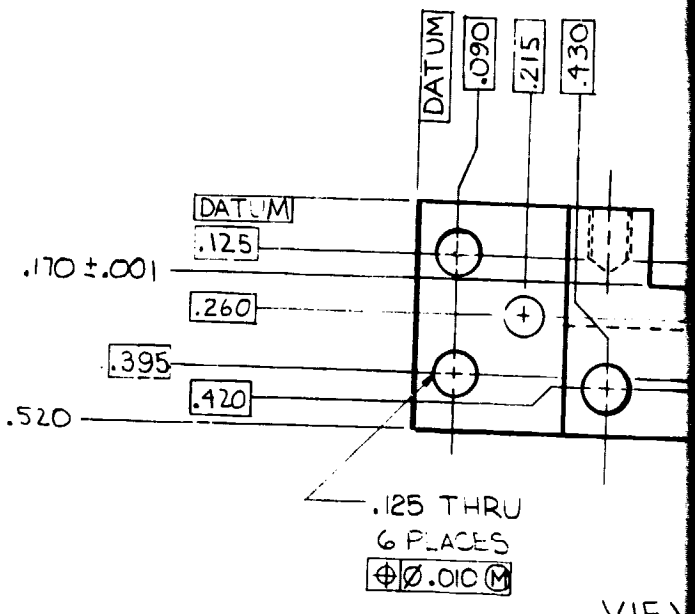


A-A

1. MATL- BRASS
2. GOLD PLATE PARTS UNASSEMBLED .000050 TO .000100 INCHES THICK PER MIL-G-45204, TYPE I, GRADE C.
3. MASK ALL TAPPED HOLES AND DOWEL PIN HOLES.
4. INSTALL PINS AFTER PLATING.

Figure 5-1. K-Band FET Circuit Transistion Assembly





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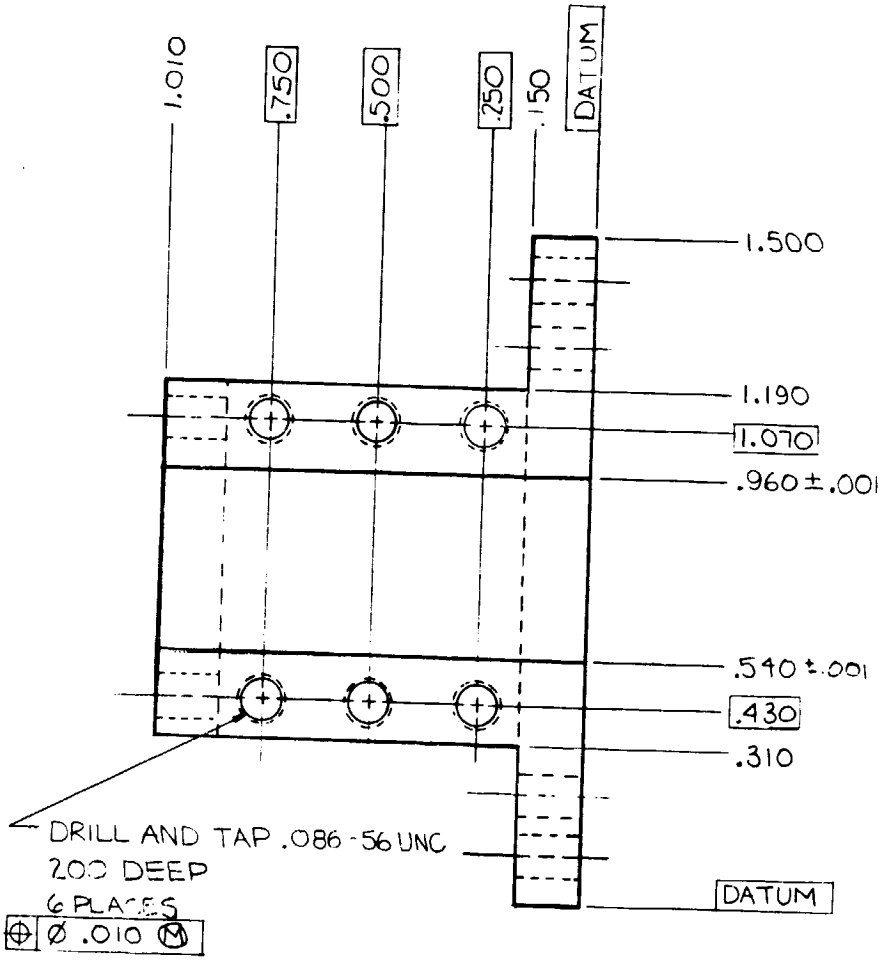

VIEW A-A

NOTE: TH
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MATERIAL:

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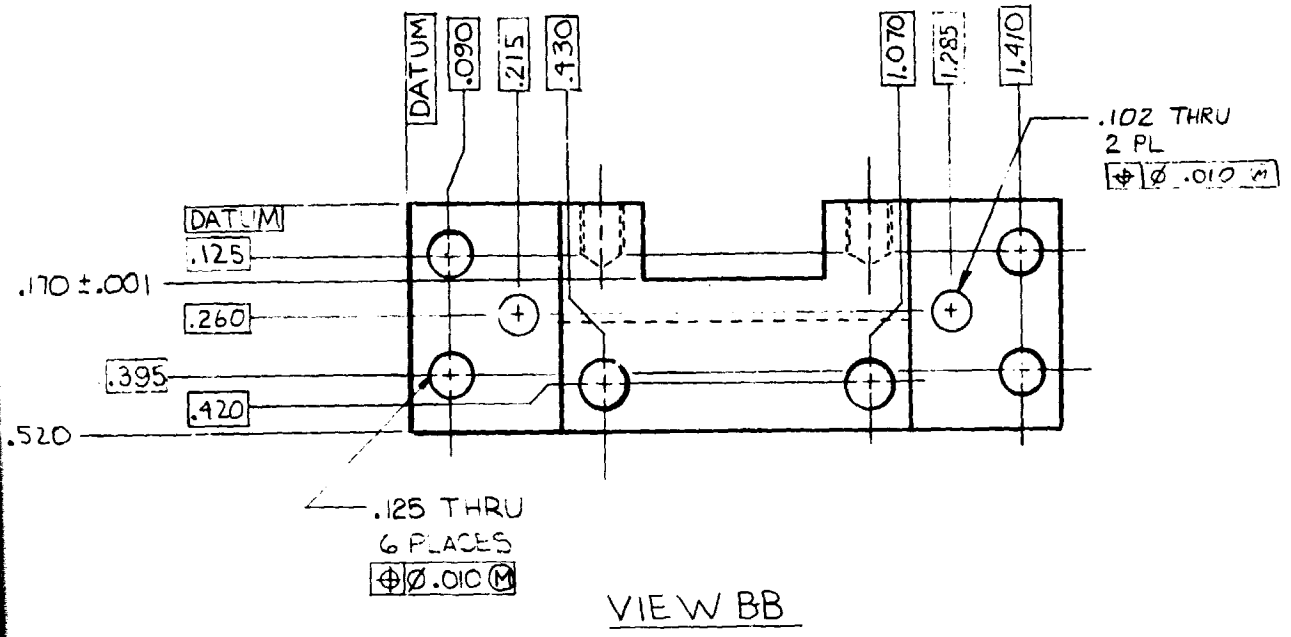

VIEW BB

NOTE: THE 1.000±.005 LENGTH DIMENSION SHOULD BE MACHINED WITH PARTS SSAN 121 AND SSAN 122 ASSEMBLED PER SSAN 123
ALL DIMENSION ±.005 UNLESS OTHERWISE NOTED

MATERIAL: BRASS

Figure 5-2. K-Band FET Circuit Waveguide to Microstrip Transistion

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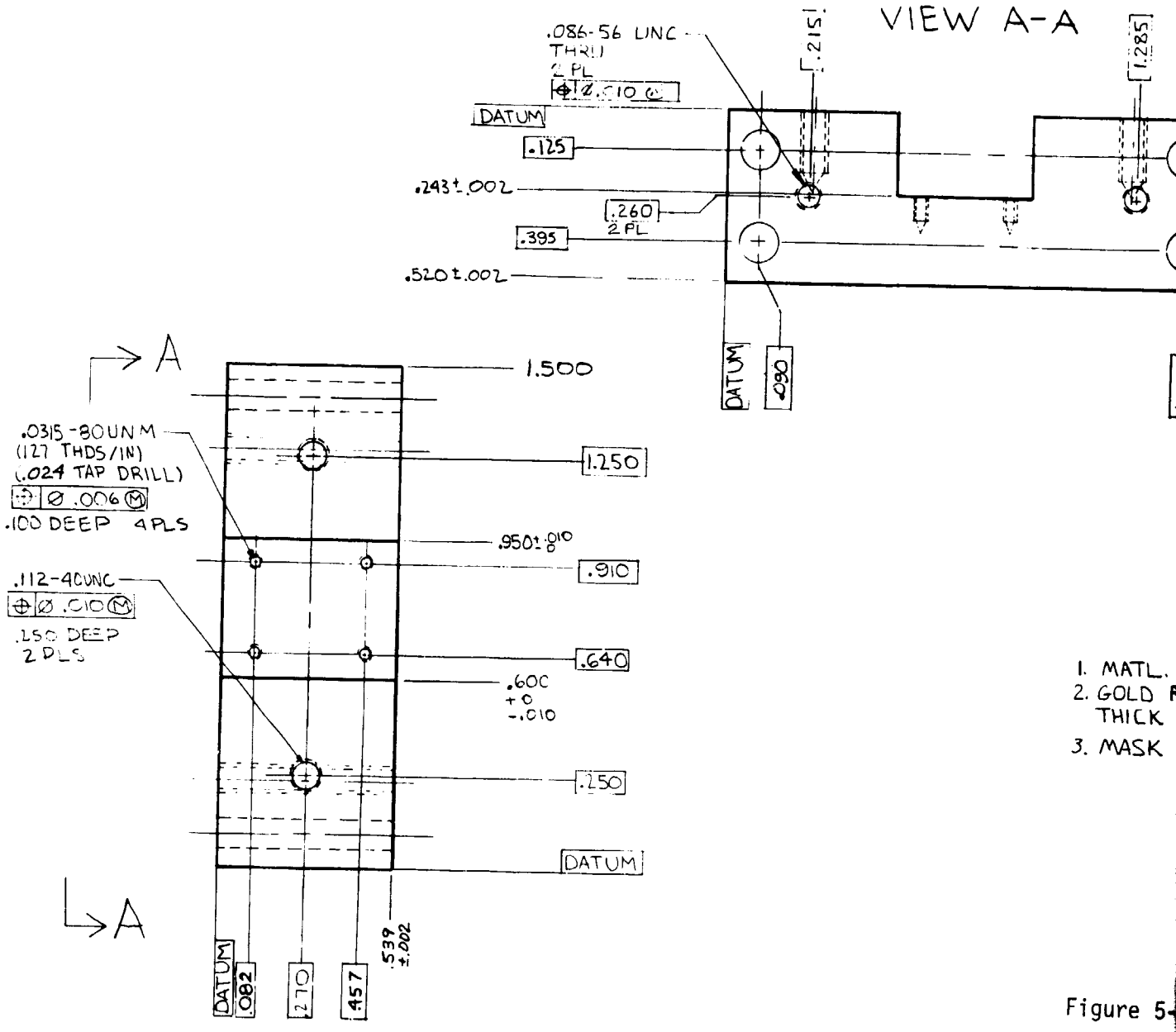
NOTE: ALL DIMENSIONS ARE ±.005 UNLESS OTHERWISE SPECIFIED



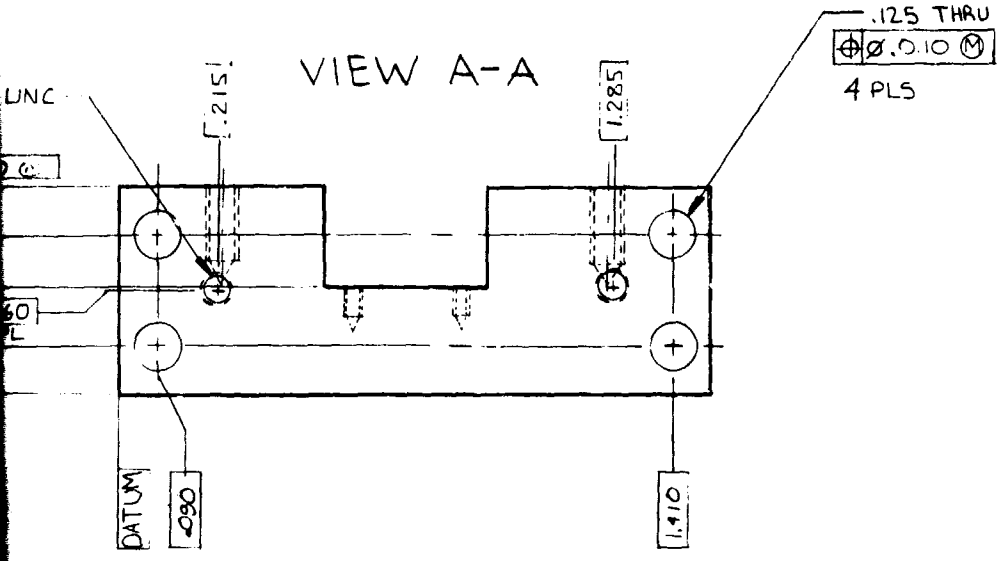
1. MATL.
2. GOLD F
THICK
3. MASK

Figure 5-

PRECE

FOLDOUT FRAME

WISE SPECIFIED



1. MATL. - BRASS
2. GOLD PLATE .000050 TO .000100 INCHES THICK PER MIL-G-45204, TYPE I, GRADE C.
3. MASK #2 AND #4 HOLES.

Figure 5-3. Thruline, Housing

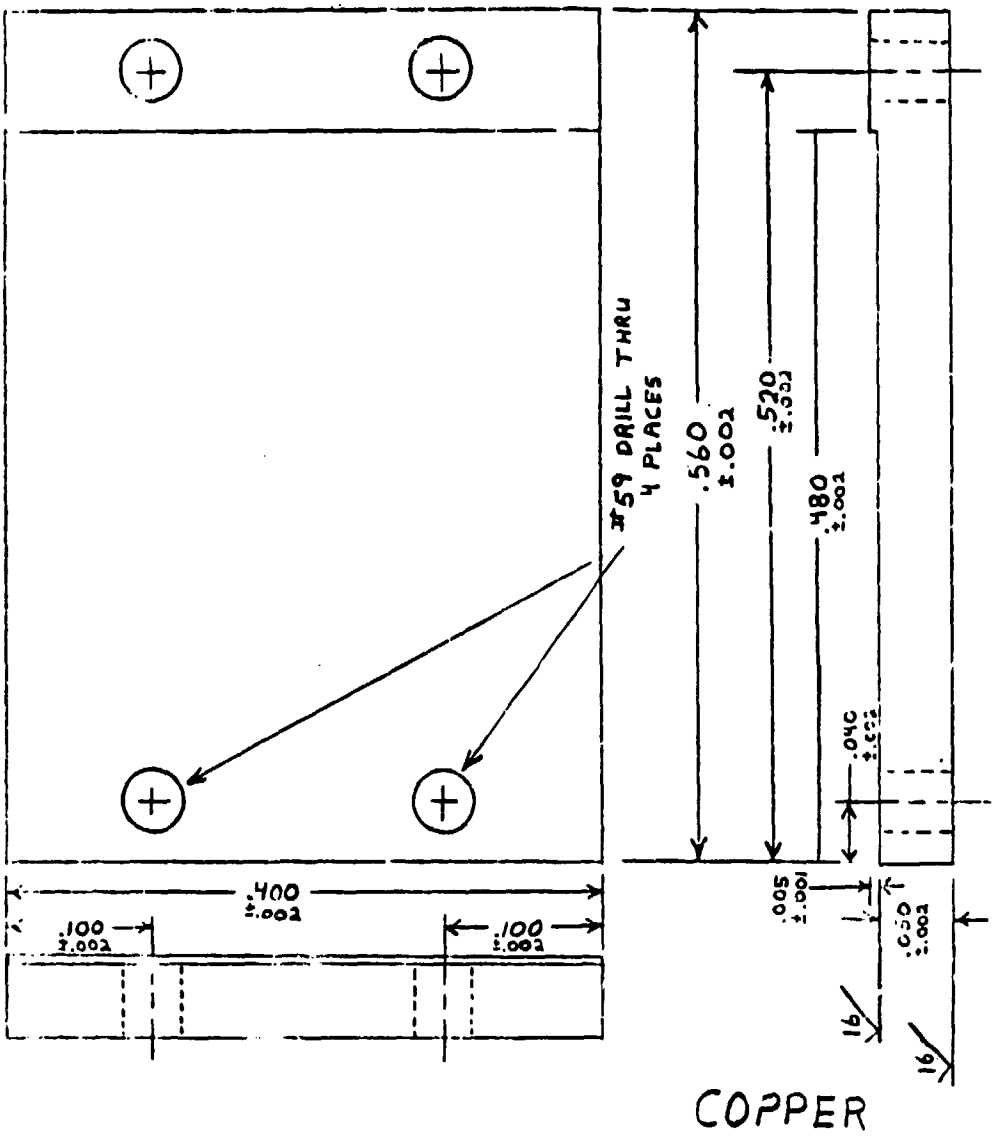


Figure 5-4. K-Band FET Coupler Carrier

5.3 FET CARRIER DESIGN

Figure 5-5 shows the components that make up the carrier/matching circuit assembly. Each assembly consists of the FET, a copper carrier, an input matching substrate, output matching, and an Invar shim for each of the quartz substrates. Figure 5-6 is a drawing of the FET carrier, which is made of copper for maximum heat conduction. The FET is mounted to the ridge in the carrier with gold germanium solder. the ridge is slightly wider than the deivce to preclude the possibility of interference with the substrates. The quartz substrates are soldered to Invar shims, which then are screwed to the carrier using the two tapped holes on each side of the ridge. Invar is used because it has a very low thermal expansion coefficient, making it a fairly close match to quartz which has a coefficient of practically zero. The substrates cannot be soldered directly to the carrier because the difference in expansion between copper and quartz would cause the substrates to crack or fall off as the assembly cools from the soldering process. Use of the shims also facilitates replacement of the substrates should it become necessary. The height of the ridge in the carrier is dimensioned so that when assembled the top of the FET and the top surface of the substrates are coplanar. This results in the shortest possible bond wire lengths, thereby minimizing their inductance. It is critical that the corner at the bottom of the ridge have a minimum radius, otherwise the substrates cannot be pushed up against the ridge.

5.4 SUBMODULE DESIGN

The driver and power submodules have an identical mechanical design. They are packaged in a machined aluminum housing shown in Figure 5-7. The carriers are mounted to the floor of the housing using minature 0.80 UNM screws, which are approximately half the size of a No. 0-80 UNF screw. The twelve 0.128-inch diameter holes are soldered in feedthrough capacitors that bring in the gate and drain bias for each FET. The taped holes at the ends of the housing accept screws for assembling the transition/thruline assemblies to the submodule. There are also holes for the attachment of a cover and heat sinks. Eccosorb attached to the inside of the cover prevents undesirable moding in the submodule.

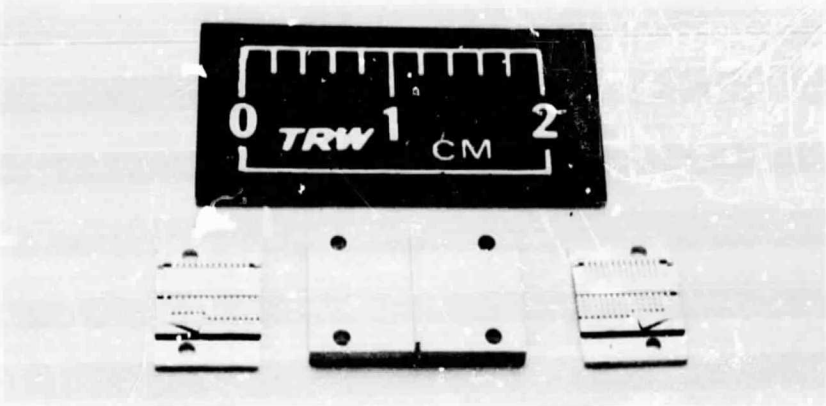


Figure 5-5. Carrier Matching Circuit Assembly Components

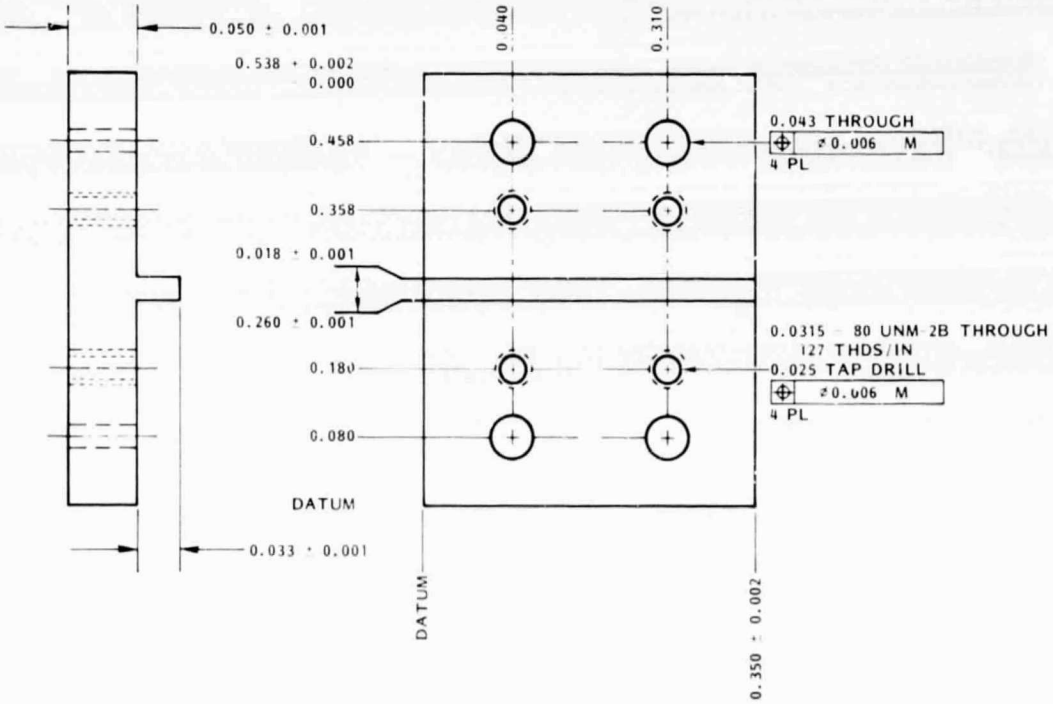


Figure 4-11. FET Carrier

Figure 5-6. FET Carrier

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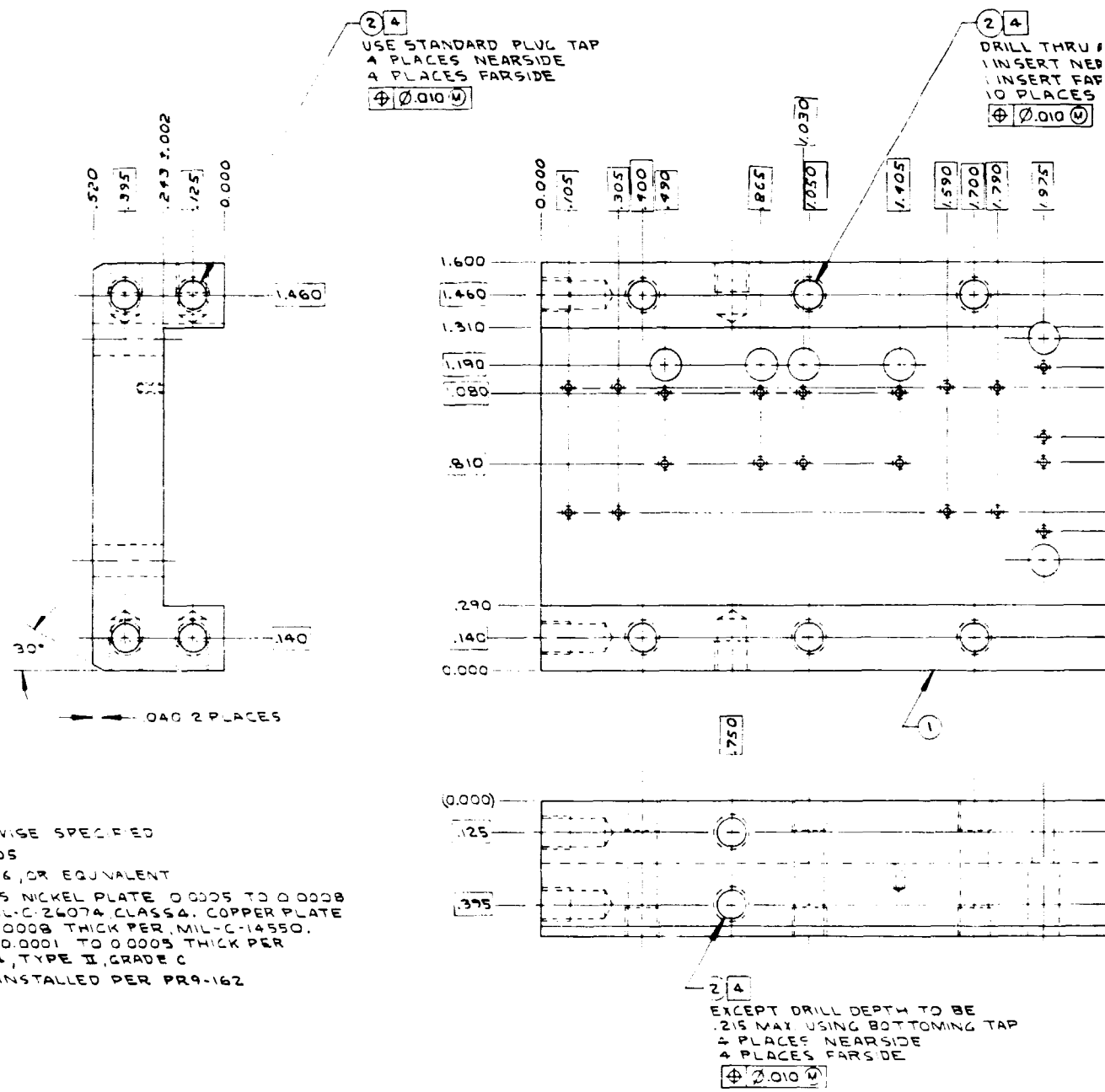

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS ± .005
2. MATL: AL ALY, 6061-T6, OR EQUIVALENT
3. FINISH: ELEC ROLESS NICKEL PLATE 0.0005 TO 0.0008 THICK PER MIL-C-26074 CLASS 4. COPPER PLATE 0.0005 TO 0.0008 THICK PER MIL-C-14550. GOLD PLATE 0.0001 TO 0.0005 THICK PER MIL-G-45204, TYPE II, GRADE C

[4] ALL INSERTS TO BE INSTALLED PER PR9-162

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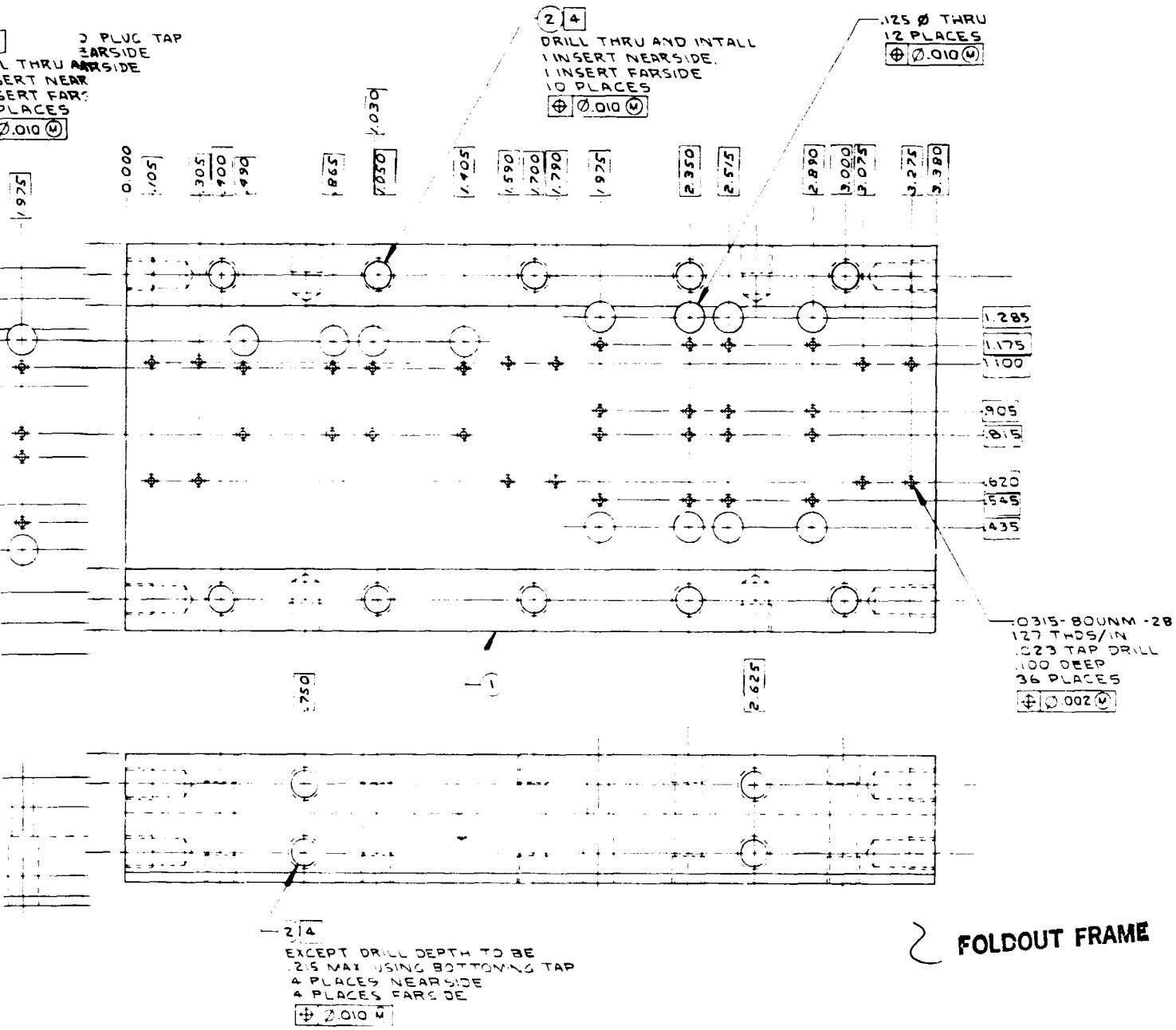

Figure 5-7. Power Amplifier Module

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5.5 RADIAL SPLITTER/COMBINER

The eight-way radial splitter and combiner have an identical mechanical design. Their construction is similar to that of the waveguide-to-microstrip transition. The lower half (Figure 5-8) is an octagonal block of aluminum with waveguide channels radiating from a central cavity. The top half (Figure 5-9) has the ridge transitions and an octagonal hole over the substrate cavity. There are nine BeO substrates exposied in the bottom half. The splitter/combiner substrate mounts in the center and has eight thruline substrates extending out to the transitions in a spoke-like pattern. A cover drops into the hole in the top half. The bottom of the cover has mode suppressor channels to clear the thruline substrates.

The substrate contact (Figure 5-10) is epoxied into the hole in the center of the combiner/splitter substrate. This contact launches the coaxial line that goes from the radial substrate to the coax/waveguide transition. The center conductor of this line is a pin that is captured by the spring fingers on the contact. The outer conductor is simply a hole drilled in both the bottom half of the splitter/combiner and in the transition. A drawing of the transition is shown in Figure 5-11 and a section view of it assembled to the combiner is shown in Figure 5-12. The center pin of the coaxial line protrudes into the waveguide channel machined in the transition. The amount of pin protrusion is adjusted by sliding the pin in or out of the substrate contact. A sliding waveguide backshort anchored by a setscrew is used to tune the transition.

5.6 CASCADED DRIVER/POWER MODULE

This unit is two submodules cascaded at the input of the amplifier assembly. The output of the first module could be interfaced directly to the input of the second module; however, the resulting assembly would be too long to package efficiently. Consequently, two E-plane waveguide bends are used between the modules to form a U-shaped assembly. E-plane bends at the assembly inout and output restore the linear in/out configuration.

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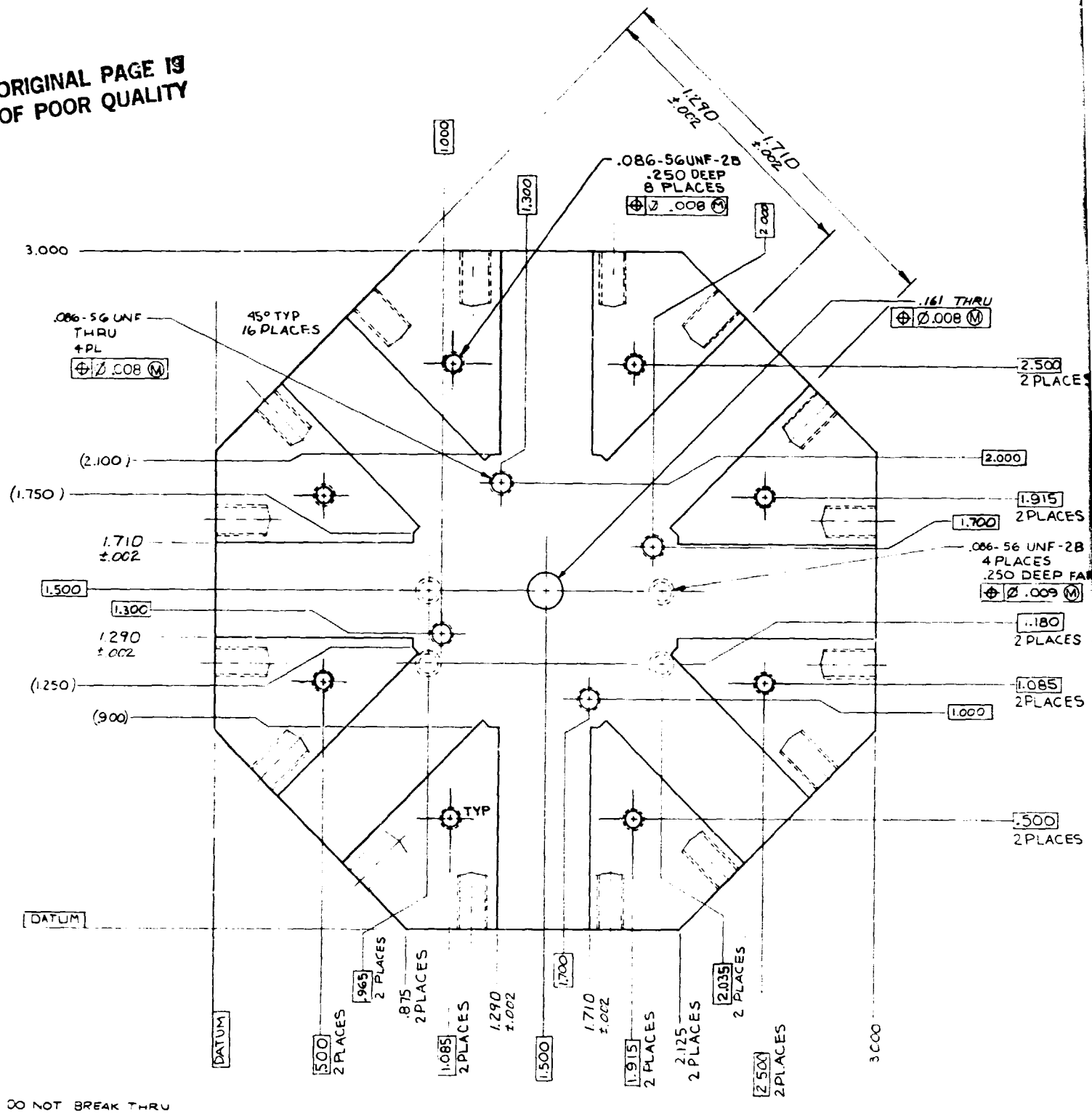

DO NOT BREAK THRU

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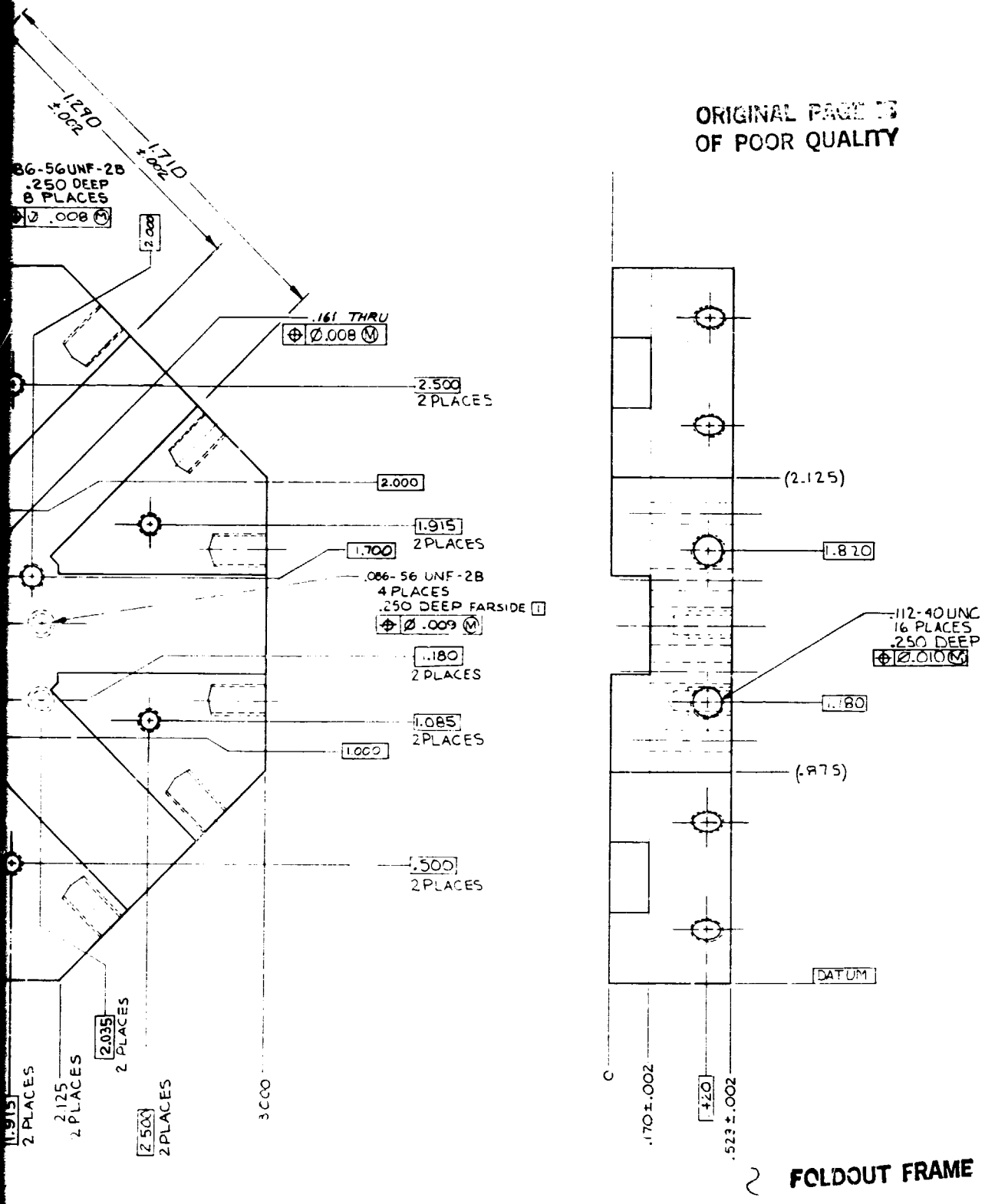

Figure 5-8. Combiner Bottom Assembly

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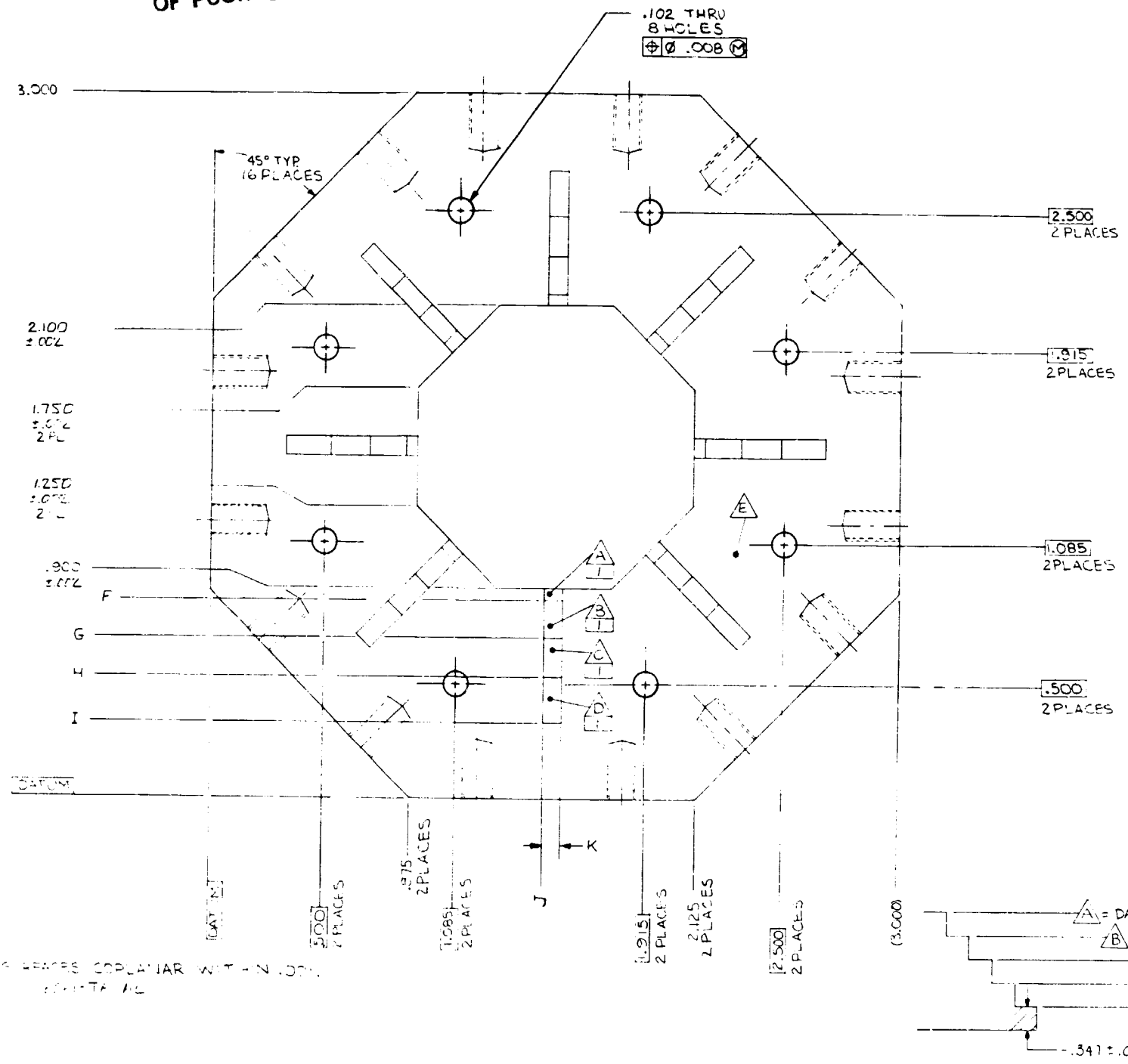


FOLDOUT FRAME

DIM. (±.002)	-1	-2
B	.007	.009
C	.041	.046
D	.102	.102
E	.153	.143
F	.850	.850
G	.690	.688
H	.521	.516
I	.325	.316
J	1.458	1.416
K	.084	.168

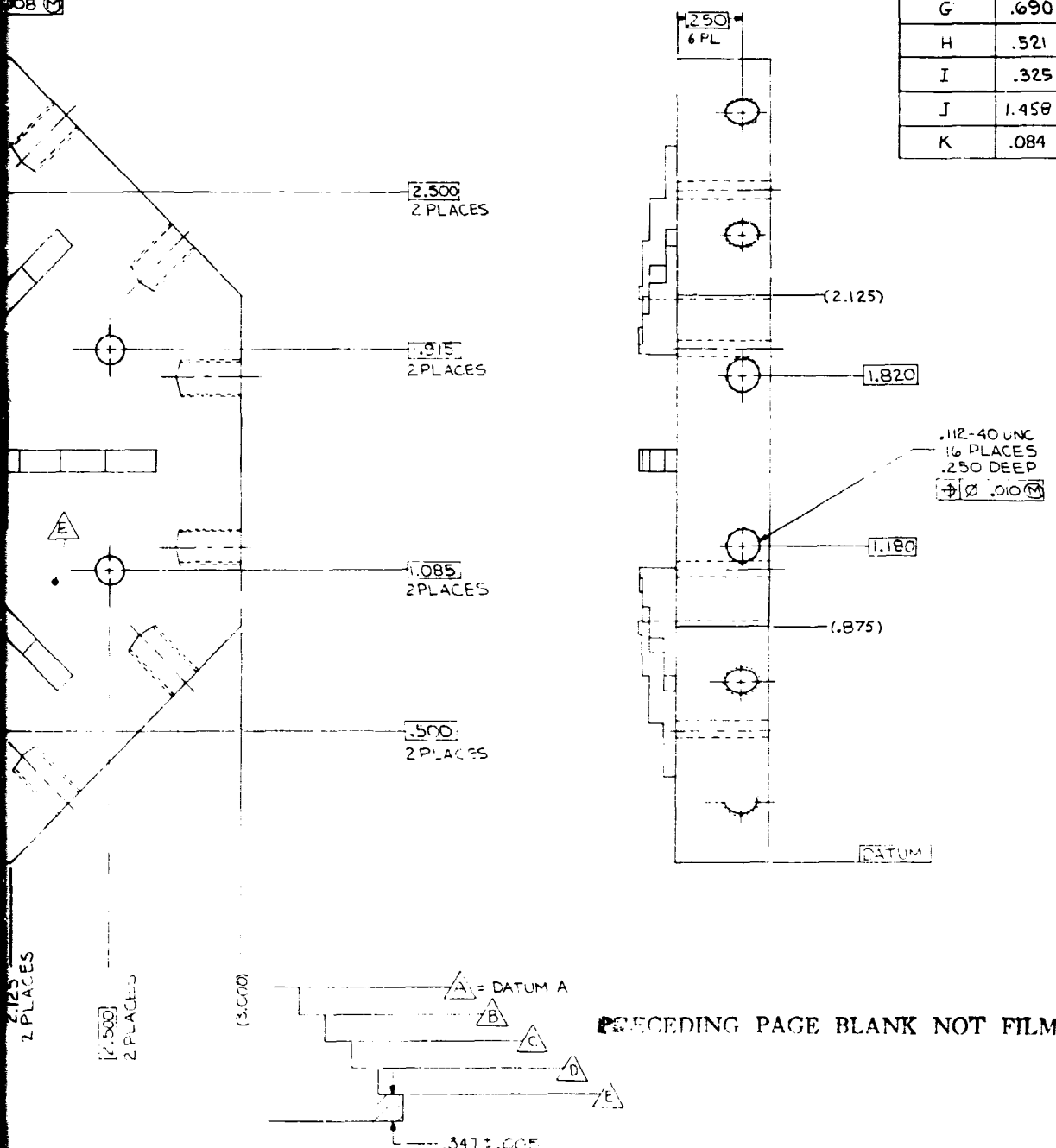
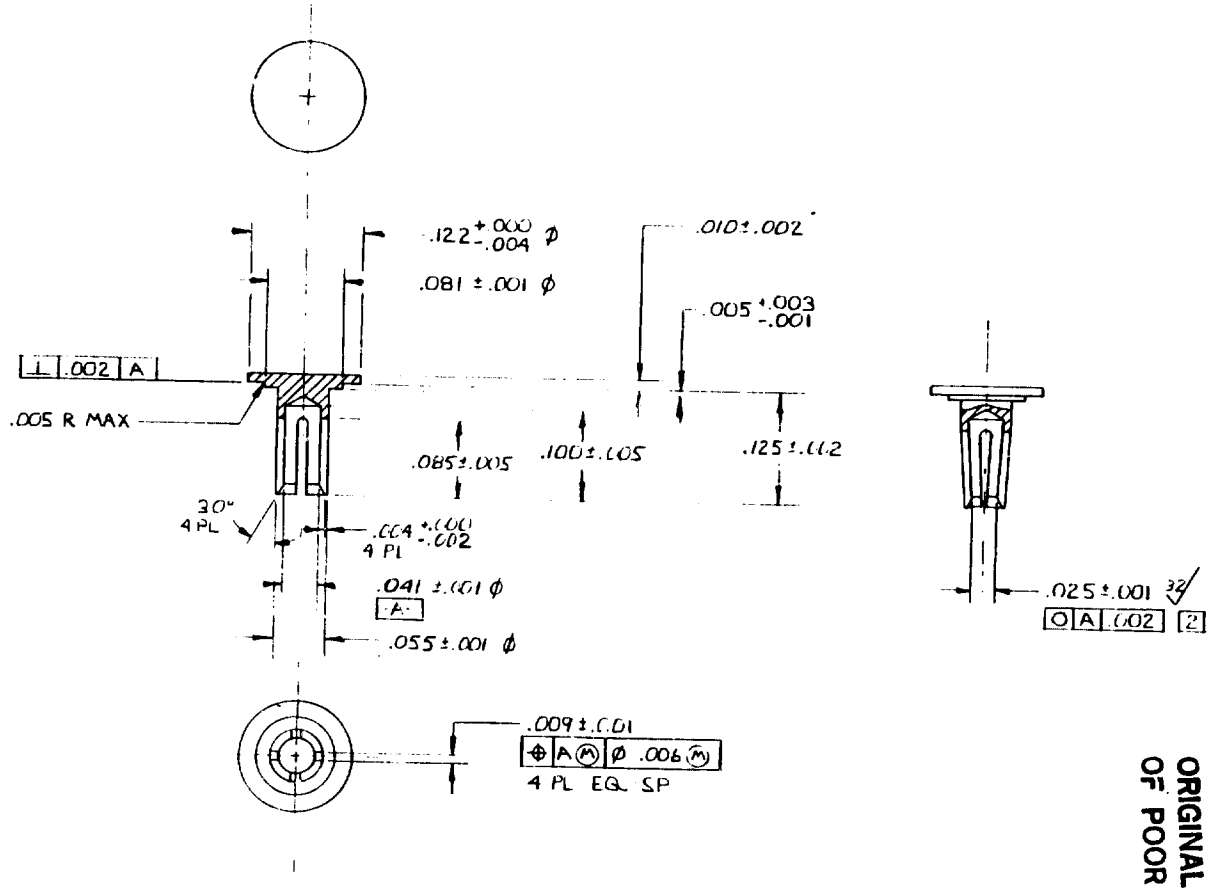
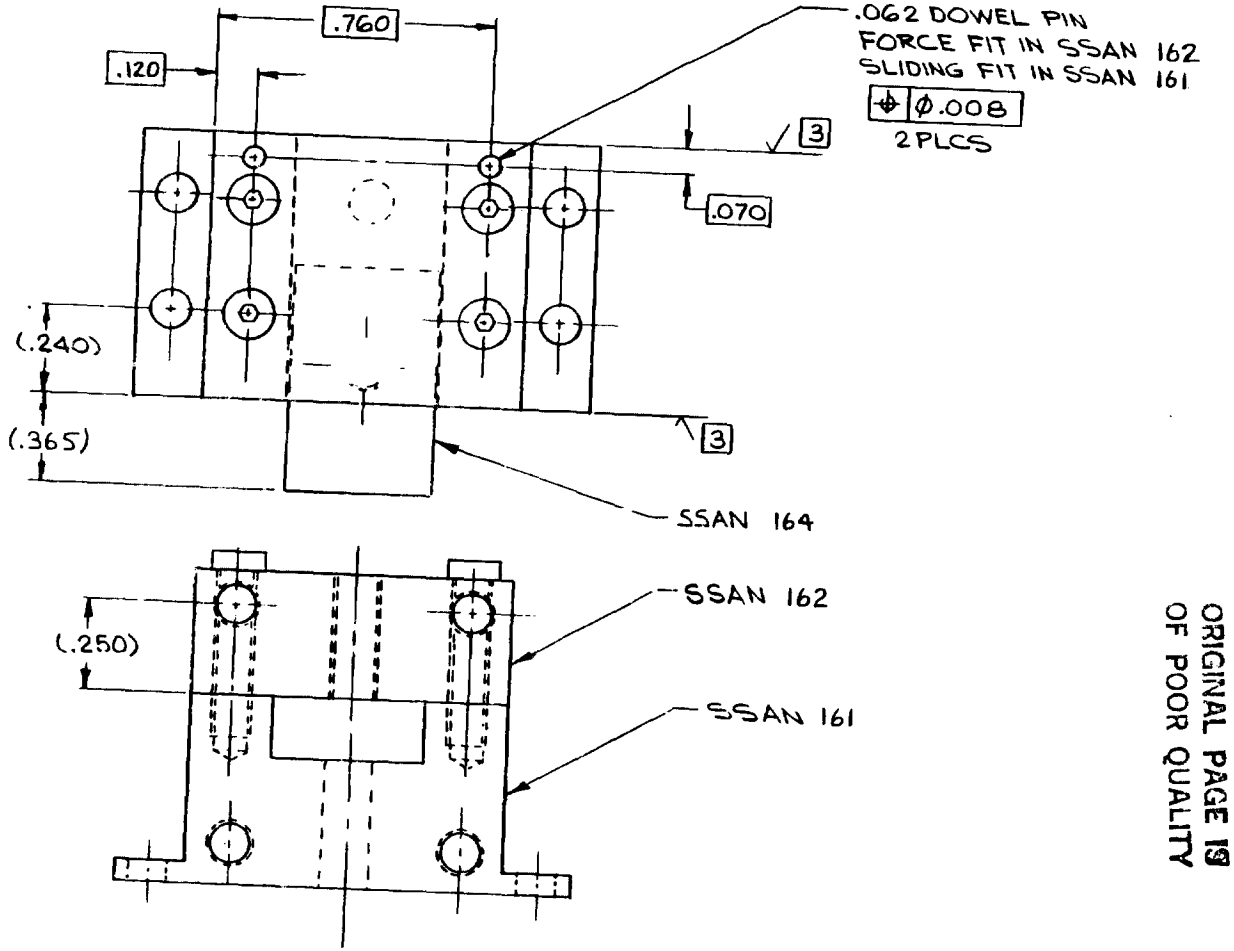


Figure 5-9. Combiner Top Assembly



1. MATL: NO 172 BE CU ALLOY CONDITION H (C252560-052).
2. HEAT TREAT TO CONDITION HT PER MIL-H-7199. HOLD IN RESTRAINED CONDITION.
3. NICKEL PLATE PER QQ-N-290, CLASS 2, .0005 TO .0008 THICK.
4. GOLD PLATE .000050 TO .000100 INCH THICK PER MIL-G-45204, TYPE II, GRADE C.
5. PLATING AREA = .061 IN²

Figure 5-10. Substrate Contact



NOTES:
1. ASSEMBLE PARTS AS SHOWN.
2. INSERT DOWEL PINS.
3. FACE OFF SURFACES CHECKED WITH PARTS STILL ASSEMBLED.

Figure 5-11. Input/Output Housing Assembly

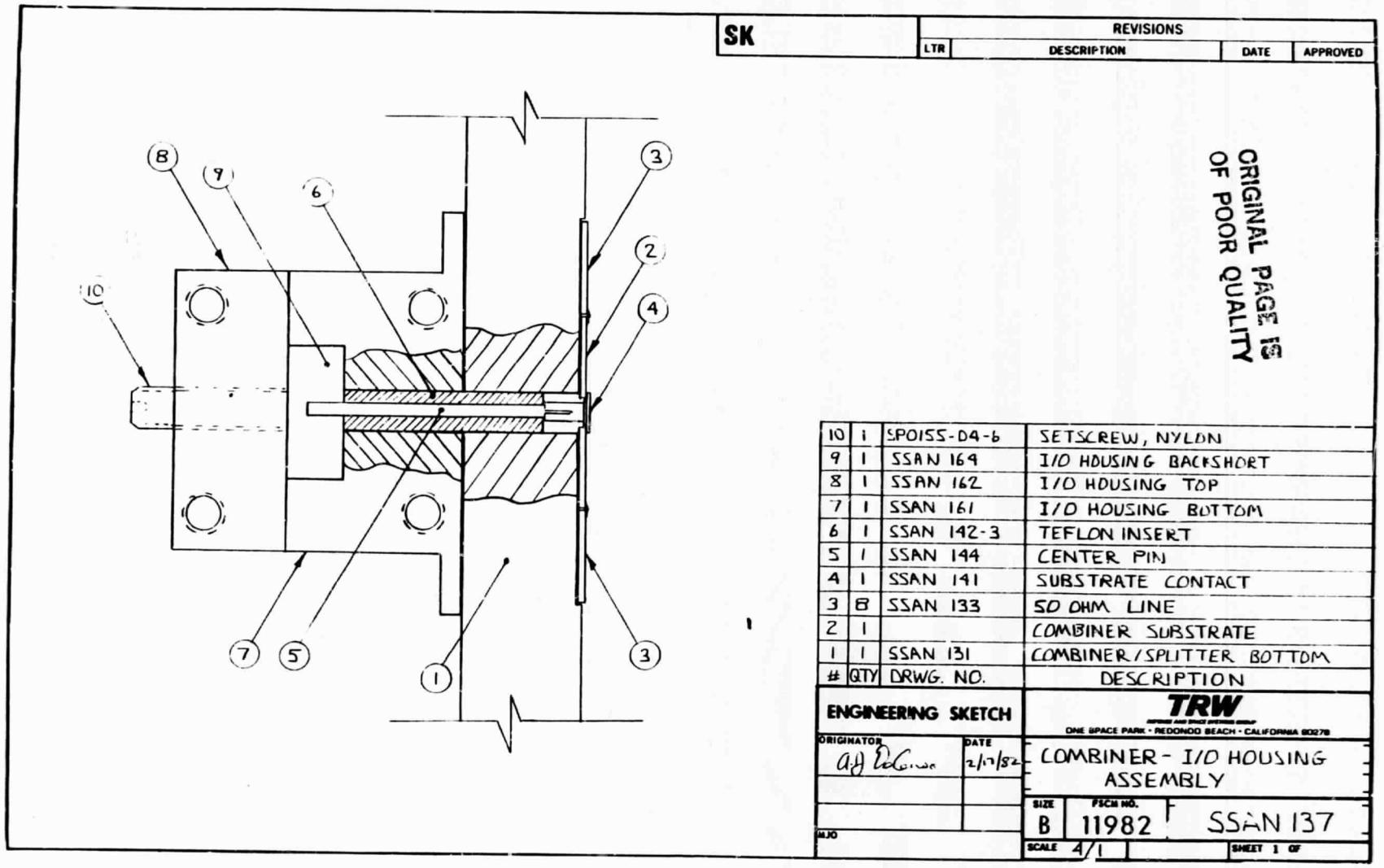


Figure 5-12. Combiner Input/Output Housing Assembly

5.7 EIGHT-WAY COMBINED AMPLIFIER

Figure 5-13 is a drawing of the eight-way combined amplifier subassembly. The output of the driver assembly interfaces with the waveguide input of the radial splitter. An amplifier submodule is connected to each of the eight outputs from the splitter. E-plane bends at the ends of the submodules form the amplifier into a cylindrical arrangements with the submodules parallel to each other. Fins attached to the submodules extend inward and are cooled by a fan at the combiner end of the assembly. Waveguide shims placed at the ports of the combiner and splitter are used for phase matching between submodules.

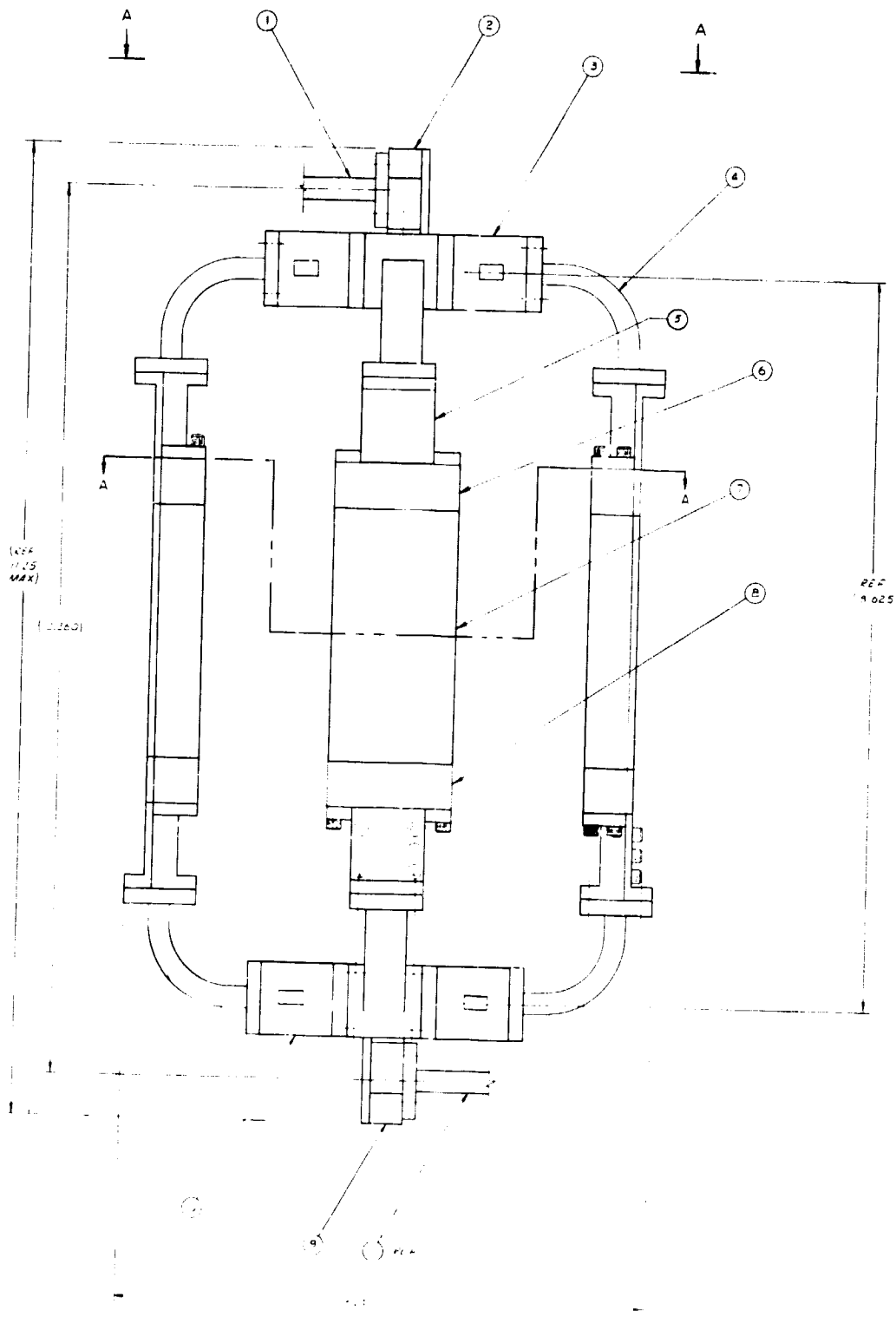
5.8 REGULATORS

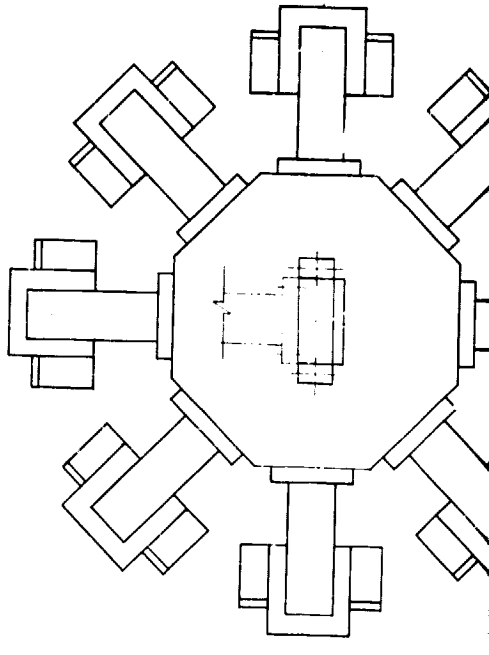
Each FET requires a regulator and all the regulator for one module are contained on one printed circuit boards. The design uses packaged regulators and discrete components integrated onto a two sided glass-epoxy board. The regulator devices are mounted in line so that their heat sinks can be screwed to a single anodized aluminum fin. Bias voltages are set for each FET by adjusting trimpots on the board. The ten regulator boards are mounted in the cover of the amplifier and have wire harnesses connecting them to the submodules.

5.9 POC AMPLIFIER ASSEMBLY

The entire amplifier assembly is packaged in a 12 X 12 X 10 inch aluminum. The driver module assembly and radial power amp assembly are mounted in the main enclosure which is 7 inches high. Sheet metal aluminum brackets hold the components in place. Cooling is provided by an intake fan that blows air past the driver assembly and around a ducting wall that separates the driver from the power amp. A fan located inside the radial subassembly draws air past the fins on the submodules and blows it out the exhaust vent.

The upper part of the box is 3 inches deep and is hinged to the lower part. The ten regulators are located in this cover. Some of the air from the intake fan blows up and over the regulator cooling fins. Amplifier operation is controlled by switched on the side of the box, and status is conveyed through a bank of LED indicators.





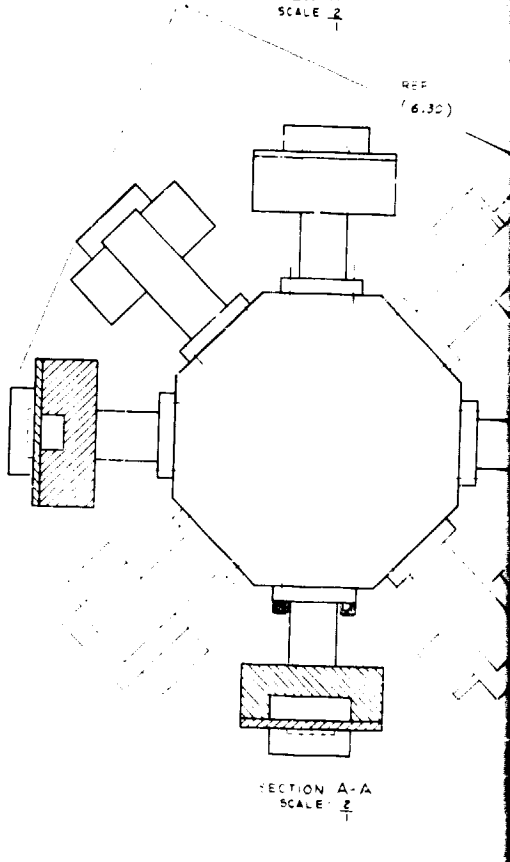


Figure 5

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PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	ITEM NO
TB-D	WAVEGUIDE WR42	1
SSAN 169	HOUSING INPUT	2
SSAN 1318132-	DIVIDER	3
42BH-18	WAVEGUIDE	4
SSAN 123	WAVEGUIDE TRANSISTION	5
SSAN 111	THRU-LINE CARRIER	6
SSAN 103	MODULE DRIVER AMP	7
SSAN 111	THRU-LINE CARRIER	8
SSAN 169	HOUSING OUTPUT	9
SSAN 1318132-	COMBINER	10

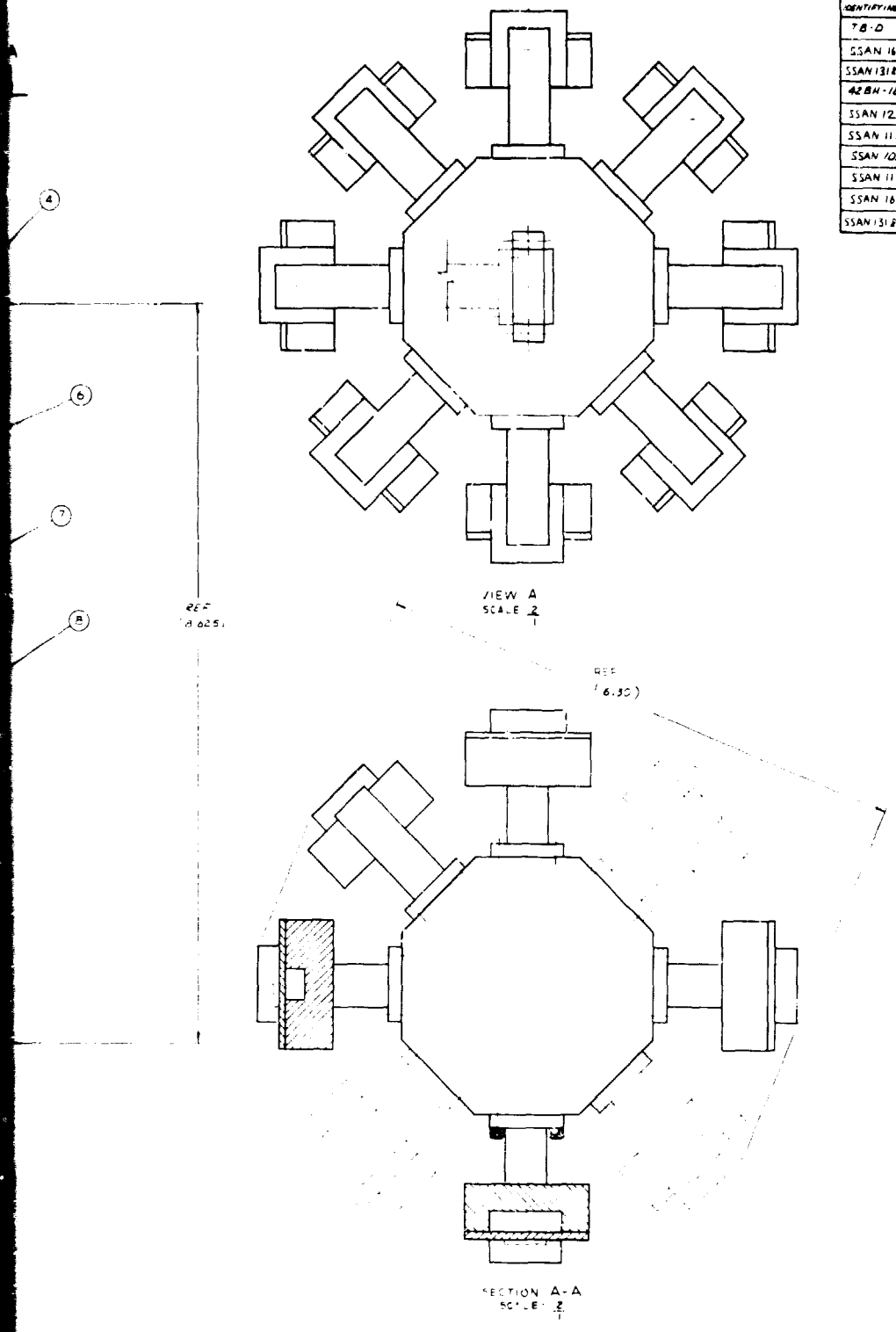

Figure 5-13. Layout Eight-Way Radial Power Amplifier Subassembly

5.10 THERMAL CONSIDERATIONS

A thermal analysis of the FET carrier assembly was performed using a computer model of the copper carriers. This program determined that the thermal resistance from a 0.015 inch square area on the top of the ridge to the bottom of the carrier base is 5°C/W. About 85 percent of this resistance is in the ridge. The thermal resistance of the gold-germanium preform was calculated to be approximately 1°C/W. There is also resistance from the bottom of the carrier to the housing floor. Assuming a 0.005-inch average air gap between the two surfaces this resistance should be about 4°C/W. Given a device junction to base resistance of 20°C/W, the total thermal resistance from junction to housing is 30°C/W. The temperature rise in the aluminum housing is very small, no more than 1°C/W, but the interface from the submodule housing to the cooling fin is approximately 40°C, assuming a dissipation of 9 W per module. If the hottest FET develops 2.0 W of heat, its junction temperature should be 2.0 W x 35°C/W + 40°C = 110°C. This is considered to be an acceptable temperature for reliable operation of the amplifier.

6. CONCLUSIONS AND RECOMMENDATIONS

6.1 CONCLUSIONS

With the excellent cooperative efforts from the Special Microwave Device Operations (SMDO) of the Raytheon Corporation, TRW has successfully developed the proof-of-concept (POC) model of the 20-GHz GaAs FET transmitter for the NASA 30/20 GHz Satellite System. The performance achieved by the FET devices developed by Raytheon for power amplifiers at 20 GHz represent the state-of-the-art capabilities in GaAs FET amplifiers. With Raytheon's devices, TRW was able to develop the amplifier using the latest microwave integrated circuit techniques, the radial power combiner expertise and the overall amplifier design capabilities including computer aided design, extensive EHF test facilities, space qualification experience, etc. The successful accomplishments by Raytheon and TRW were made possible with the helpful guidance, construction suggestions, and most importantly, the often needed encouragement and understanding provided by the NASA Project Manager and other personnel from the NASA Lewis Research Center in Cleveland, Ohio.

Table 6-1 is a summary of the achieved performance characteristics of the amplifier as compared to the specifications. It is noted that the amplifier outperformed the specifications in all categories except for bandwidth and dc-to-RF efficiency. The 17.9 to 19.1 GHz bandwidth achieved is rather impressive, nevertheless. Basically, the gain-bandwidth product achievable is limited by the device. To strive for the power required, first devices with large cell dimensions are necessary. Secondaly, paralleling of a number of cells is also required. This necessarily reduces the input and the output impedances of the devices. The impedance levels are further impaired due to parasitics which increase with larger devices. Thus, to improve the gain-bandwidth product of high-power devices, the present devices used have to be improved. TRW and Raytheon have certain define ideas as to how these devices can be improved, and the approaches to accomplish these improvements are delineated later (see Section 6.2).

Table 6-1. Summary of POC Performance

Parameter	Specifications	Performance
Frequency Band	17.7 to 20.2 GHz	17.9 to 19.1 GHz
Output Power	6 to 7.5 W	8.2 W
RF Gain	30 dB	38.6 dB
Gain Flatness	±0.5 dB	±0.5 dB
Input/Output VSWR	1.4:1	1.2:1
Noise Figure	<25 dB	8 dB max
Group Delay	0.5 nsec/0.5 GHz	0.5 nsec
AM/PM Conversion	<3°/dB	<2°/dB
RF Efficiency	13%	8.54%

The dc-to-RF efficiency of the amplifier can be improved by

- Improving the efficiency of the device
- Increasing the combining efficiencies of the amplifier.

The device efficiency can be improved by optimizing the doping characteristics and reducing the RF losses of the device's parameters. if the output power of the device can be improved by a factor of two, the eight-way combiner can be simplified to a four-way combiner, thus reducing the combiner losses. The combiner loss can further be reduced by improving the combining circuitry. Again, recommendations to increase the dc-to-RF efficiencies are summarized in Section 6.2.

6.2 RECOMMENDATIONS

TRW and Raytheon jointly recommend that the effort to improve the state-of-the-art EHF GaAs FET power amplifier techniques should be continued. Table 6-2 summarizes what should be the objectives for the next phase development as compared to what have been accomplished to date. Table 6-3 delineates the fundamental approaches to improve the present 1 W devices. Unfortunately, the approaches summarized are conflicting in certain aspects. For example, higher power devices lead to larger parasitics, thus reducing the bandwidth capability. To clarify some of these issues, Table 6-4 provides the tradeoff areas needed to be examined to

arrive at an optimum design for the device. Nevertheless, TRW and Raytheon firmly believe that the objectives set forth in Table 6-2 can be achieved with reasonable effort.

Table 6-2. Expected Improvements in Efficiency

- Assuming device efficiency improved to 25 percent
- Assuming gain improvement of 1 dB

	Present (%)	Expected After Improvement (%)
Device	20.0	25.0
Stage	17.0	20.8
Module	13.3	18.2
Unit Amplifier	10.7	16.1

Table 6-3. Proposed Improvements in 1-Watt Device for Greater Bandwidth and Efficiency

- Single cell configuration compared with present two-cell configuration
- Reduction of overall chip size to reduce parasitics
- Combined via holes and air bridge techniques to achieve low parasitic interconnect
- Increase device source periphery to 2 MM
- Increase gate thickness by plating to reduce gate resistance
- Reduce gate length (E-beam technology)

6.3 ACKNOWLEDGMENT

The successful completion of this program are due largely to the extremely well-coordinated cooperative efforts between Raytheon and TRW, resulting from the firm commitment made by the high-level management of the responsible activities under Dr. T.T. Fong of TRW and Dr. B. Hewitt of Raytheon. J. Goel of TRW and P. White of Raytheon, the Program Managers, were principally responsible for the technical direction of this program. the following engineers and technicians from TRW contributed heavily toward the program.

6.4 ENGINEERS

- A.J. DeCenso – Mechanical work and design and fabrication
- Gordon Oransky – Coupler and combiner
- Patrick O'Sullivan – Amplifier stages

6.5 TECHNICANS

- Farrokh Abidi – Technical and electrical assembly work
- Jamin Carman – Technical and electrical assembly work

TRW and Raytheon are heavily indebted to the valuable support, the often-needed direction and understanding and the constructive suggestions provided by Mr. Jack Shank, the NASA Project Manager from Lewis Research Center in Cleveland, Ohio and Mr. Gerald Chomos of Lewis Research Center, who became the Project Manager at a later phase of the program.

Table 6-4. Desired Improvements, Possible Methods and some Trade-offs

HIGHER POWER	INCREASE PERIPHERY	REDUCES GAIN AND BANDWIDTH UNLESS PARASITICS AND DISTRIBUTED EFFECT REDUCED
		REDUCES BANDWIDTH
	INCREASE BREAKDOWN	AT EXPENSE OF LOWER CURRENT OR LOWER G_M BECAUSE LIMITED BY PHYSICS UNLESS FUNDAMENTAL NEW STRUCTURE FORTHCOMING
	REDUCE THERMAL RESISTANCE	— THINNER CHIPS INCREASE PARASITICS
HIGHER GAIN	REDUCES PARASITICS AND DISTRIBUTED EFFECTS	
	INCREASE M_D TO INCREASE G_M	— DECREASES BREAKDOWN AND INCREASES GATE CAPACITANCE
	DECREASE GATE LENGTH	— POSSIBLY DECREASES POWER INCREASE GATE RESISTANCE
HIGHER EFFICIENCY	INCREASE GAIN	
	INCREASE BREAKDOWN VOLTAGE	
	REDUCE KNEE VOLTAGE	— REDUCE PARASITIC SOURCE RESISTANCE
GREATER BANDWIDTH CAPABILITY	INCREASE GAIN OVERALL	
	INCREASE S_{21}	— REDUCE PARASITICS AND DISTRIBUTED EFFECTS
	DECREASE S_{11} S_{22} S_{12}	
	DECREASE DISPENSION	

APPENDIX A

AN 18 GHz 8-WAY RADIAL COMBINER

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ABSTRACT

This paper describes a 16 to 20 GHz 8-way radial microstrip combiner with transitions to WR42 waveguide. It demonstrates greater than 20% bandwidth and insertion loss of only 0.8 dB. Excellent phase and amplitude balance has been achieved.

Introduction

A combiner is a useful tool for enhancing the power output of an amplifying system beyond the current capabilities of a single amplifier.

The radial combiner is an efficient type of combiner for achieving this. It can combine any number of amplifiers in one stage in contrast to an arrangement of planar binary symmetric hybrids such as Wilkinson combiners or Lange couplers. It also has less loss than either of the above combiners or the fork hybrid (reference 1) by virtue of its shorter interconnecting lines. Due to its symmetry it also has good amplitude and phase balance.

Fabricated combiners have been described previously. Reference 2 describes a 12-way radial combiner centered at X-band. Reference 3 describes an X-band 6-way combiner using halfwave long radial microstrip lines and also one using uniform lines with halfwave lines connecting to the isolating resistors.

This paper describes for the first time an 18 GHz 8-way radial microstrip combiner with transitions to WR42 waveguide. It demonstrates greater than 20% bandwidth and insertion loss of only 0.8 dB. Excellent phase and amplitude balance has been achieved.

Design Background

The schematic of the combiner is shown in Figure 1. It comprises eight exponentially tapered transmission lines that connect together at the center to form the common port and are bridged at the radial end by resistors. Identical matching networks on the radial ports match to 50Ω and the common port is also matched to 50Ω.

Figure 2 shows computed curves of the combiner radial port input impedance $Z_R = (R_R + jX_R)$ and common port input impedance $Z_C = (R_C + jX_C)$ when the radial ports are matched. The parameters are plotted as a function of the taper fractional wavelength (ℓ/λ_T), taper characteristic impedance (Z_2) at the radial end and isolating resistor (R_I). The taper characteristic impedance at the common end is set at 100Ω. The taper wavelength λ_T is related to the uniform line wavelength λ by:

$$\lambda_T = \frac{\lambda}{\sqrt{1-\rho^2}}$$

where ρ, the taper rate is given by:

$$\rho = \frac{\log_e (Z_1/Z_2)}{4\pi\ell/\lambda}$$

Note that:

1.) The common port input resistance R_C is largest at a ℓ/λ_T value of approximately 1/4.

2.) R_C is largest for a lower value of isolating resistor R_I and higher value of Z_2.

3.) Radial port resistance (R_R) varies more slowly with frequency for a lower value of R_I.

4.) Radial port reactance is lower for a lower value of R_I.

The optimum choice of line length is therefore quarter-wave, with a high value of Z_2 and low value of R_I.

Choice of Dielectric

Beryllia was chosen as the dielectric over Alumina for two reasons.

1.) By virtue of its lower dielectric constant, the input impedances at the common and radial ports are higher and thereby simplifying matching.

2.) The thermal conductivity of Beryllia is approximately ten times that of Alumina, and consequently, heat dissipated in the resistors is conducted better to the ground plane.

Theoretical Design

A computer program was written for the combiner, in which the matching circuit, tapered line and resistor details were inputted. The program calculated return loss of all ports, transmission loss and isolation between radial ports. The program took into account in addition, the coupling between the tapered lines and parasitics of the resistors. The tapered line length was chosen at a quarter wave and resistance value at 70Ω. Since the tapered lines must bridge to the resistors, their widths at the low impedance end was set. The even mode characteristic impedances at the narrow and wide ends of the taper were at 96Ω and 27Ω, respectively. Because of the coupling between the tapered lines, their odd mode impedances were lower than these values.

The common and radial port matching circuits were varied on the computer until a reasonable match was obtained on all ports between 16.0 and 20.0 GHz. No effort was made to adjust the parameters for improvement of radial to radial port isolation. The predicted response of the combiner is shown in Figure 3. Predicted return loss is greater than 11 dB. Radial to radial port isolation varies between 15 dB and 26 dB. The transmission calculations did not take into account the dissipative loss of the microstrip conductors.

Construction

Figure 4 shows the microstrip outline. The substrate is 0.025 inch thick Beryllia. The radial port matching consists of 29.5Ω lines of length 0.397λ at the center frequency. Microstrip lines in 0.42 inch wide troughs connect from the radial ports of the combiner to the microstrip-to-waveguide transitions, which are stepped ridge waveguide types. This design was chosen in order that the waveguide resonance of the combiner cavity was above the working frequency.

The common port coaxial line transition to waveguide is a capacitive probe, the design of which is described in Reference 4.

Measured Performance

The measured results of the final combiner are shown in Figure 5. The common and radial port return losses are tuned to peak around 18.5 GHz maximum VSWR over a 20% bandwidth is better than 1.5. The transmission loss is 0.8 dB at band center which 0.5 dB can be attributed to the actual copper substrate dissipation, and the remaining 0.3 dB is due to different transitions. The amplitude unbalance of the eight transmission paths is between 0.25 and 0.8 dB over the range 16 to 20 GHz. The phase unbalance is ± 11° at 18 GHz.

Conclusions

This paper has described a radial combiner designed for 18 GHz. It has low transmission loss, low amplitude and phase unbalance and reasonably good radial to radial port isolation.

Acknowledgments

This work was done under joint sponsorship of NASA and U.S.A.F. Space division under Contract No. NAS3-22503. The authors would like to thank Mr. Jack Shank, the contract monitor on this program.

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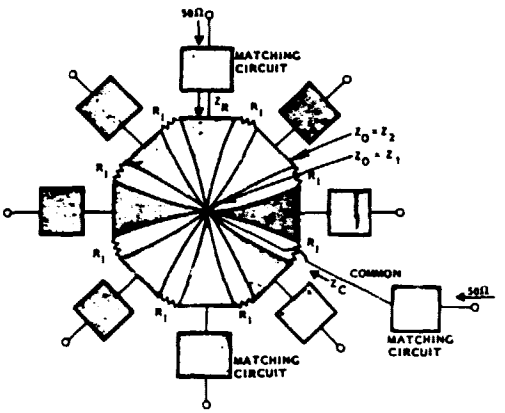

Figure 1. Radial Combiner Schematic

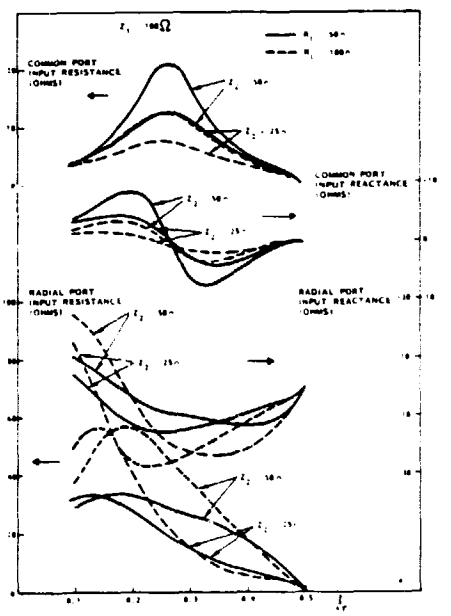

Figure 2. Combiner Computed Impedance Data

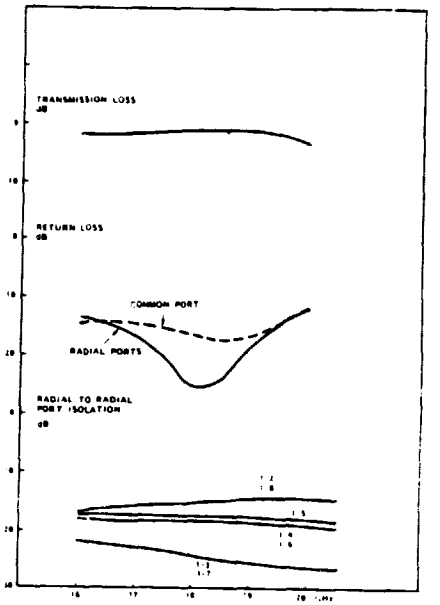

Figure 3. Combiner Predicted Performance

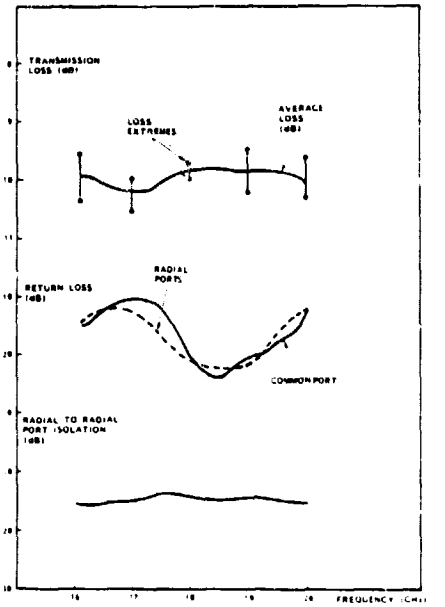

Figure 5. Combiner Measured Performance

Substrate: Beryllia 0.025 thick

Dimensions in Inches

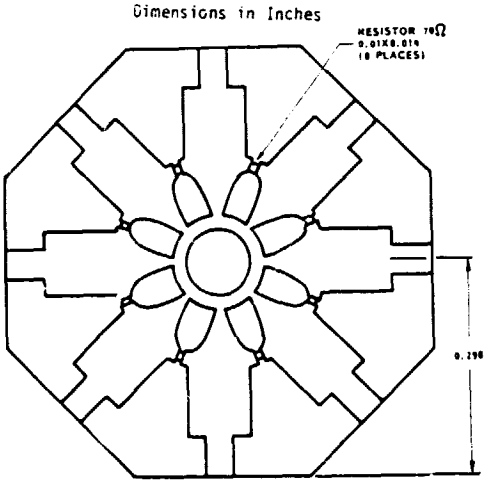

Figure 4. Combiner Microstrip Outline

APPENDIX B

A 1 WATT GaAs POWER AMPLIFIER FOR THE NASA 30/20 GHz COMMUNICATION SYSTEM

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ABSTRACT

A multistage GaAs FET power amplifier, employing cascaded balanced stages using state-of-the-art 1/4, 1/2, and 1 watt devices, has been developed. A linear gain of 30 dB with 1.25 watts output has been achieved over a 17.7 to 19.4 GHz frequency band. The development and performance of the amplifier and its components are discussed.

Introduction

Studies of the growth in communications traffic indicate that the frequency spectrum allocated to fixed service satellites at C- and Ku-band will reach saturation by the early 1990's. K-band, with uplink frequencies at 27.5 to 30.0 GHz and downlink frequencies at 17.7 to 20.2 GHz is the next higher frequency band allocated for this purpose. Current plans for the development of satellite systems to implement this band include the possibility of a NASA demonstration experiment in the mid-1980's. System studies have identified the use of multibeam antenna systems as a major factor in achieving minimum cost and efficient use of frequency and orbital resources. Such multibeam systems, however, require reliable, efficient, lightweight, solid state transmitters. This amplifier has been developed for the downlink of a 30/20 GHz communication system.

This paper reports on the development of a GaAs FET amplifier capable of output power greater than 1 watt over a bandwidth of 17.7 to 19.4 GHz with a linear gain of 30 dB. Assembly techniques and test results for the amplifier and its circuit components will be discussed.

Passive Components

The most common transmission mode above 18 GHz is waveguide; however, it is easier to design GaAs FET amplifiers using microstrip transmission line. Generally, waveguide-to-SMA and SMA-to-microstrip transitions are used to bridge from waveguide to microstrip. The problem is that commercial SMA-to-microstrip launchers have unacceptable losses above 10 GHz. A lower loss direct waveguide-to-microstrip transition, which can be accomplished using a quarter-wave ridge transformer has been employed. Two such transitions connected back to back by 0.5 inches of 50 ohm microstrip line measure 0.5 dB or less loss from 17 to 21 GHz.

To achieve high power levels over a broad frequency range, some form of power combining is required. There are several approaches for realizing a practical hybrid coupler compatible with microstrip transmission line. These approaches are based on the proximity coupling of two adjacent quarter-wavelength microstrip lines.[5,6,7] A six-finger interdigital coupler on 0.015 inch quartz was developed at TRW to fill this need. The coupler design was chosen for its low VSWR and high isolation features. A low VSWR thin film tantalum nitride load resistor was included on the same coupler substrate. The coupler test data indicate an equal power split with less than 0.5 dB loss over the 17 to 21 GHz range. Figure 1 shows a diagram of the coupler design.

Power Amplifier

Two important design considerations for an amplifier used in a spaceborne system application are performance and mean-lifetime-failure. The GaAs FETs developed for this design (Raytheon 872) were designed for minimum thermal resistance, minimum parasitic source inductance, and maximum high-power, broadband gain. The 1-watt FET design is shown in Figure 2. The sources are connected to the ground via holes etched in the thinned substrate, which is approximately 0.002 to 0.003 inches thick. This reduces thermal resistance and the parasitic source inductance. These two FET properties play an important role in the amplifier design and performance; low thermal resistance can be directly related to a longer device MTBF and results in a longer amplifier lifetime. Similarly, the parasitic source inductance will seriously affect the FET RF performance, particularly the bandwidth. Typical operating device junction temperatures are 110°F, corresponding to a 5×10^6 hour MTBF. The high power and broadband characteristics of the FETs are acquired through a combination of material and physical device parameters.

Assembly of a single amplifier stage begins with Au/Ge eutectic soldering of the FET onto a gold-plated, copper chip carrier. The chips are then wire-bonded to the RF lines of gate and drain substrate assemblies. The substrate is 0.015 inch quartz, which has been Au/Ge eutectic soldered to a gold plated INVAR shim. An INVAR shim is used since its thermal expansion coefficient closely matches that of quartz, and therefore minimize the stresses built up during soldering. Quartz was chosen because of its low dielectric constant, low tangential loss, and good surface finish.

Amplifier design followed after device S-parameters were measured in test fixtures which closely simulated the actual mounting arrangement in the amplifier. Data were obtained on each device type, 1/4, 1/2, and 1 watt FETs up to 18 GHz, using an Automated Network Analyzer. The S-parameter data were then extrapolated to 21 GHz and matching circuits were designed and optimized over the 17 to 21 GHz frequency band using computer aided design programs. Circuit designs generated for the gate and drain substrate assemblies included a biasing filter, blocking capacitors, and some tuning pads.

Devices were then assembled into fixtures to measure and optimize their individual gain, bandwidth, and output power. A waveguide measurement system and a scaler network analyzer were used for testing. The devices were connected to this system using the waveguide-to-microstrip transitions discussed earlier. To facilitate assembly and tuning, the waveguide transitions were connected to a length of microstrip line in a housing which prevented waveguide mode propagation below 30 GHz. The devices being tested were then

connected to these lines. This type of test fixture keeps RF radiation to a minimum and helps in tuning the assembled MIC amplifier. After taking the data on these tuned individual devices, the results were analyzed. Devices were then selected for combining and were then tested as directly cascaded device pairs. With this accomplished, device pairs were then chosen for integration into the power amplifier.

A schematic diagram of the power amplifier is shown in Figure 3. The power amplifier can be divided as shown into two identically configured submodules. The submodules differ only in the device types used. Submodule No. 1 uses only 1/4-watt devices, whereas, submodule No. 2 has 1/2 and 1-watt devices. Since the first stages of a submodule are gain stages, devices were chosen for these stages for best gain characteristics. Subsequent stages were selected to operate in a balanced configuration using the interdigitated couplers described earlier. Each submodule was assembled and tested prior to final assembly of the amplifier. The submodules were then assembled into the complete power amplifier as shown in Figures 3 and 4. Data obtained from tests on the overall amplifier are shown in Figures 5 and 6. Figure 5 demonstrates the 30 ± 0.5 dB gain over the 1.7 GHz bandwidth. The P_{in} vs. P_{out} characteristic shown in Figure 5 demonstrates the 1.25-watt output power at the 1 dB gain compression point. The measured noise figure is 8.4 dB.

Conclusion

The development and performance of a 1.25 watt GaAs FET power amplifier with a linear gain of 30 ± 0.5 dB of gain over a bandwidth of 1.7 GHz centered at 18.5 GHz has been demonstrated. Assembly techniques for the amplifier and its components have been described.

Acknowledgement

This amplifier has been developed under the sponsorship of NASA Lewis Research Center, Cleveland, Ohio, contract number NAS3-22503. The authors wish to thank J. Shank of NASA for his support. We also wish to thank F. Abidi and J. Carman for their work in assembling and testing of the amplifier.

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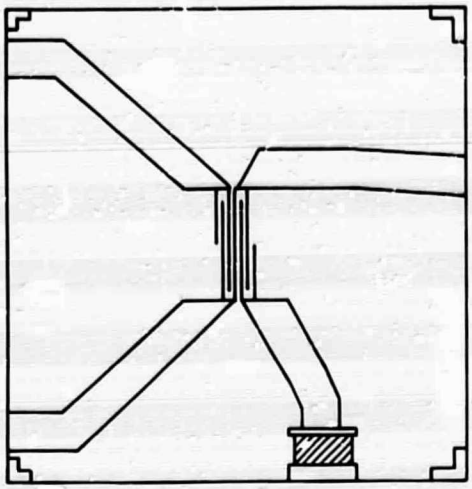

Figure 1. Six-Finger Interdigital Coupler Circuit Diagram

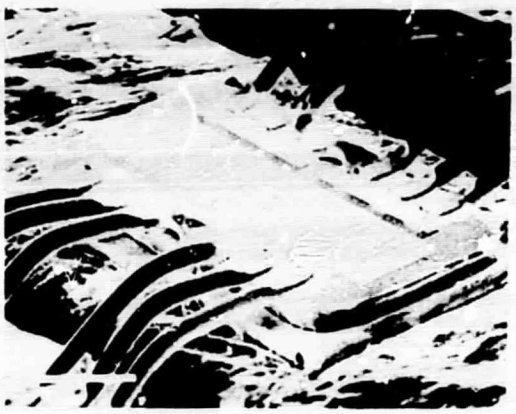

Figure 2. Raytheon 1-Watt GaAs FET

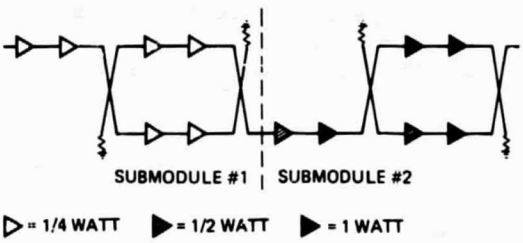

Figure 3. Schematic Diagram of the Power Amplifier

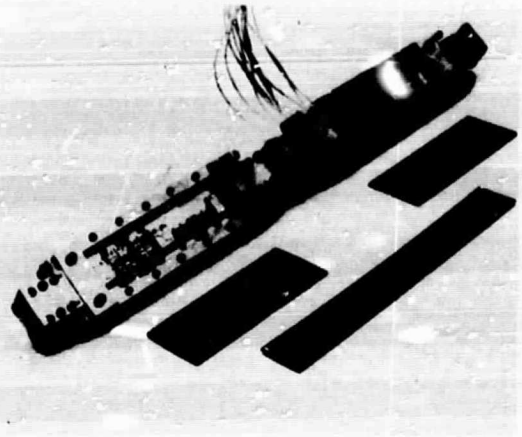

Figure 4. Picture of the Power Amplifier With Waveguide to Microstrip Transistions

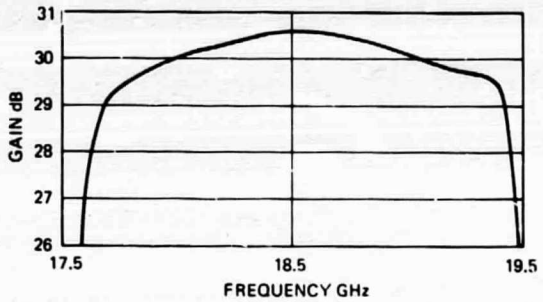

Figure 5. Frequency Response of the Power Amplifier at a 0 dBm Input Power Level

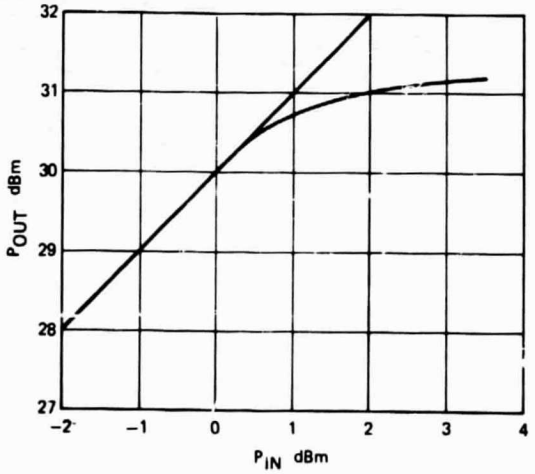

Figure 6. Pout vs. Pin for the Power Amplifier

APPENDIX C

AN 8.0 WATT K-BAND FET AMPLIFIER FOR SATELLITE DOWNLINK

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ABSTRACT

An 8.2 Watt FET amplifier with 38.6 ± 0.5 dB gain over 17.7 to 19.1 GHz frequency band has been developed. This amplifier combines the outputs of eight multistage amplifier modules utilizing a radial combiner. This state-of-the-art power level has been achieved with a noise figure of less than 8.0 dB and AM/PM of less than 2°/dB. The third order intermodulation products at 1 dB gain compression were 20 dBc and variation in group delay over the frequency band was less than ± .25 nSec.

Introduction

The growth of satellite communication traffic indicates that presently allocated C and Ku band spectrum will saturate in the near future. With the recent advances in GaAs power device technology[1] to higher frequencies and with the use of radial combining techniques,[2] it is now possible to have solid state transmitters in K-band. The radial combiner, being less lossy compared to the other binary or serial combiners, provides the most economical combining method to achieve the required high output power.

This paper describes the results achieved by combining 16 power devices. A combination of Lange interdigitated couplers and an 8 way radial combiner has been successfully demonstrated to obtain 8.2 Watts over 17.7 to 19.1 GHz frequency band. An advantage of this combining scheme is the graceful degradation of gain and output power in case one or more device failure. The overall amplifier exhibits excellent phase linearity, low intermodulation products, AM/PM conversion and noise figure performance.

Device Selection and Stage Design

Device selection is the most important criterion for successful completion or any amplifier program. Two special devices were developed by Raytheon for this project. The design consisted of the conventional interdigitated structure, in which many gates are connected in parallel to achieve the required output power. The unit gate width was optimized for high frequency operation and 100um was selected; the gate length (0.6 to 0.7um) was chosen to be the shortest consistent with high yield optical lithography. The device design consists of 8 gates combined to form one cell, which yielded 0.5 Watt output power with 5 dB gain. The output device shown in Figure 1 consists of two cells to give 1.0 Watt with 4.5 dB gain. The total gate width of a 2 cell device was 1.6 mm. The via hole technique was employed to minimize the thermal resistance and the source inductance, the two most important parameters for high frequency and high power operation. The integrated plated heat sink, together with extremely thin GaAs chip and via hole processing, ensures minimum thermal resistance.[7] Aluminum was chosen for gate metalization because submicron gates can be readily fabricated with high yield using aluminum.

In designing the single state amplifier, first the device S-parameters were measured up to 18.0 GHz. An accurate model was then derived to extrapolate the device parameters up to 21.0 GHz by computing the model response. Low power driver stages were designed based on the predicted S parameters. The substitution method was employed to get the optimum impedance contours for the high power devices. The large signal characteristics thus obtained were utilized to design the high power output stages.

Module Development

For manufacturing ease, a modular approach was selected to build the transmitter amplifier shown in the block diagram of Figure 2. Two different type modules were used; a driver module with 21 dB gain and 25.5 dBm output power and a power module with 10 dB gain and output power in excess of 31.0 dBm. The block diagram of the power module is shown in Figure 3. The driver module is electrically identical to the power module except it uses lower power devices due to gain and efficiency considerations. All the modules used in this transmitter consist of two cascaded stages driving a higher power balanced stage. These modules were built by utilizing the design techniques explained in the preceeding section. All the components of driver and power modules were built using 15 mil fused silica substrate. The six finger interdigitated coupler used tantalum nitride resistive film to realize the thin film termination resistor. All the modules were assembled and tuned with waveguide to microstrip transition on the input and output. The results obtained from the first two modules cascaded together have already been reported.[4] 1.25 Watts output power with 30 ± 0.5 dB gain was achieved over 17.7 to 19.1 GHz frequency band.

Radial Splitter/Combiner

In order to achieve higher power levels, an 8-way radial splitter/combiner was developed. The splitter and combiner are identical components and are a useful tool for enhancing the output power of an amplifier system beyond the capabilities of an individual device or module.[5] It can combine any number of amplifiers in one stage in contrast to planar binary hybrids such as Wilkinson or Lange couplers.[6] Due to its short interconnecting lines the radial combiner has lower loss and excellent phase and amplitude balance. A computer program was developed to design the microstrip divider to optimize the return loss on all ports, transmission loss and isolation between radial ports by varying the matching circuit, tapered line and the resistor shape. Because of the heat dissipation considerations, the combiner and dividers were fabricated on 25 mil thick BeO. The design provides greater than 20% bandwidth, less than 0.8 dB combining loss and excellent phase and amplitude balance. These detailed results on the combiner developed for this program are reported in a different session.

Amplifier Performance

The transmitter amplifier with block diagram, shown in Figure 2, was assembled using the amplifier modules and splitter combiner described in the preceeding sections. Figure 11 shows the photograph of the completely assembled unit. Frequency response of the completed transmitter is shown in Figure 4. It covers from 17.7 to 19.1 GHz frequency band with 39.0 dB gain and ± 0.5 dB gain flatness. The transfer characteristic of the transmitter amplifier at 18.4 GHz is shown in Figure 5. It exhibits 8.2 Watts (39.13 dBm) output power at 1 dB gain compression point. It also demonstrates excellent power limiting capability under saturated condition.

The group delay of the amplifier measured from 17.5 to 18.5 GHz is shown in Figure 6. It exhibits a constant group delay of 8.7 nSec with a variation of only 0.25 nSec in 1.0 GHz bandwidth. This is an important parameter in a communication amplifier which indirectly indicates the excellent phase linearity. AM/PM conversion, another important characteristic of the amplifier, was measured over 6.0 dB variation in the input power. The worst variation (2°/dB) was observed at the low drive level. The intermodulation performance was measured at different points in the band with two equal amplitude carriers 50 MHz apart. The photograph of Figure 7 shows the third order intermodulation distortion at 1 dB gain compression point measured at mid band. It was typically 20 dB below either of the two carriers in the complete 1.4 GHz band. The overall transmitter, including all the D.C. power supply and regulators, is shown in the photograph of Figure 8.

Conclusion

State-of-the-art performance has been demonstrated with solid state FET power amplifier in K-band. This amplifier delivers 8.2 Watts of output power with 39.0 dB gain over 1.4 GHz frequency band. The design of this multistage amplifier comprises the power, gain and bandwidth which can be further improved with improvement in the device technology. With all the devices operating around 110°C junction temperature, the life of the amplifier was better than 10 years based on the device MTFF of 10^7 hours extrapolated from high temperature stress tests. The results achieved here show that GaAs solid state amplifiers are good potential candidates for replacing the TWTA's in the future communication systems.

Acknowledgment

This work was performed under joint sponsorship of NASA Lewis (Contract No. NAS3-22503) and U.S.A.F. Space division. The authors wish to thank Jack Shank and Rod Knight of NASA Lewis for their support. The authors would also like to thank A.J. DeCenso for his support in mechanical design. Jamin Carman and F. Abidi's help in tedious assembly work is also greatly appreciated.

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Figure 1. Raytheon 1 W Device

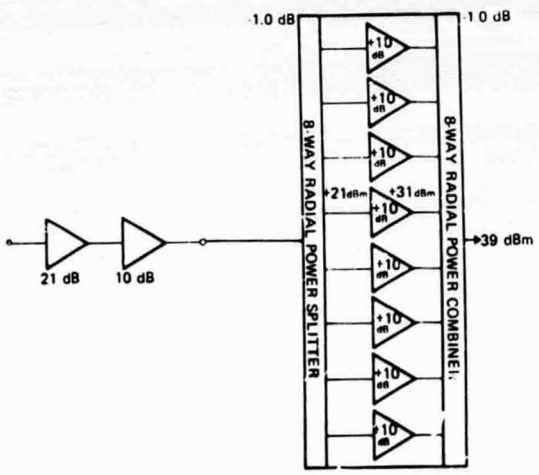
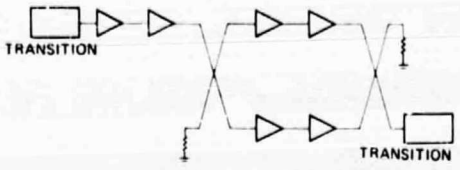


Figure 2. Block Diagram



GAIN (dB)	0.5	4.0	3.0	0.5	3.0	0.5	0.5	
POWER (dBm)	20.0	19.5	23.5	26.5	23.0	26.0	29.0	31.0	31.0

Figure 3. Power Gain Budget of Power Amplifier

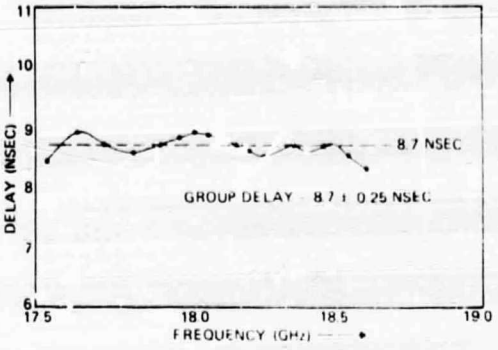


Figure 6. Transmitter Group Delay Response

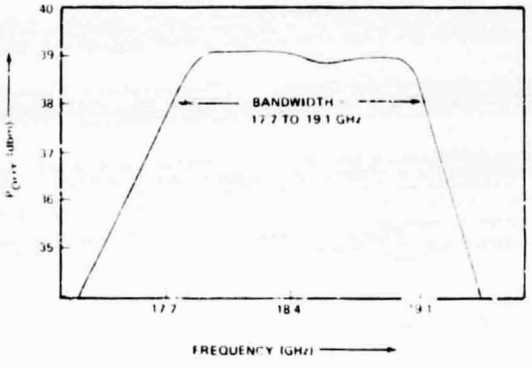


Figure 4. Transmitter Frequency vs Power

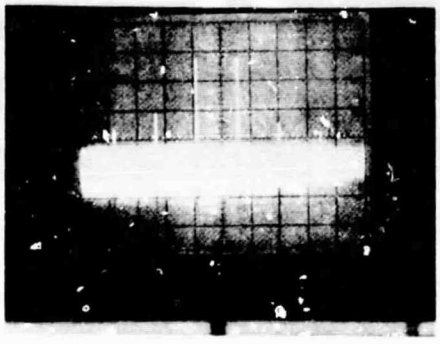


Figure 7. Transmitter Intermodulation Characteristics (Frequency = 18.5 GHz)

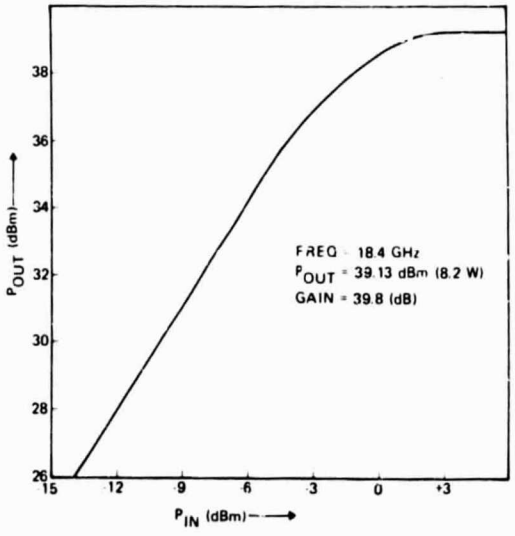


Figure 5. P_{IN}/P_{OUT} Characteristics of Transmitter

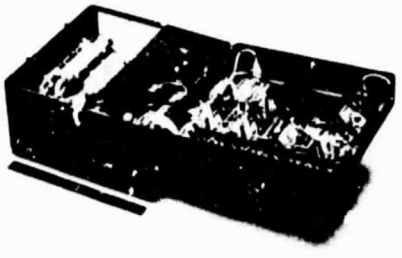


Figure 8. Complete Transmitter Amplifier