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25 kW RESONANT dc/dc POWER CONVERTER

R.R. Robson

Hughes Research Laboratories
3011 Malibu Canyon Road
Malibu, CA 90265

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16. Abstract

The feasibility of processing 25-kW of power with a single, transistorized, series resonant converter stage has been demonstrated by the successful design, development, fabrication, and testing of such a device. It employs four Westinghouse D7ST transistors in a full-bridge configuration and operates from a 250-to-350 Vdc input bus. The unit has an overall worst-case efficiency of 93.5% at its full rated output of 1000 V and 25 A dc. A solid-state dc input circuit breaker and output-transient-current limiters are included in and integrated into the design. Full circuit details of the converter are presented along with the test data.

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SECTION 1
INTRODUCTION

To meet the goals of multi-hundred-kilowatt space power systems planned for the middle to late 1980s and beyond, advanced power-processing technology is required to convert the power available from solar arrays or other space-borne power sources to the various voltage and/or current levels required by the spacecraft bus and/or loads. This technology can be built on the strong technical base of multi-kilowatt series resonant converters which have been developed in recent years. This technical base includes advanced switching components, magnetic components, filter components, mathematical circuit models, control philosophies, and switch drive strategies. Much of the recent effort has been centered around the application of high power transistors in resonant converters. Transistor switches display marked advantages over the more commonly applied thyristors. Among these advantages are: higher frequency operation, lower switch losses, positive commutation, lower peak tank currents, and inherent current limiting in the switch. It is anticipated that the eventual application of this technology base to multi-kilowatt space power systems will result in both reduced specific mass due to the higher conversion frequencies, and in reduced thermal control due to more efficient operation.

To date, the highest known power level of a resonant power converter designed for space operation is 2.5 kW. However, studies have shown that a module size of 25 kW is appropriate for a multi-hundred-kilowatt space-power system. A 10-kW transistorized dc/dc resonant power converter, designed for laboratory testing, was developed under Contract No. NAS 3-22471. This contractual program was established to take the next step in the development of series resonant converters for spaceborne and airborne applications.

The goals of this program were to develop a transistorized single-stage 25-kW dc/dc resonant power converter, with a minimum efficiency requirement of 92% and a maximum goal of 96%.

SECTION 2

SUMMARY

A 25-kW resonant dc/dc power converter was designed, developed, fabricated and tested using government-furnished Westinghouse D7ST transistors as the high-power switches. The base-drive requirements and circuitry for the D7ST transistor were obtained from a preceding contract (NAS 3-22471: "Resonant Circuit Transistor Characterization"). Under this preceding contract, the D7ST transistor was characterized for use as a switch in series resonant converters and a base-drive circuit was developed. This base-drive circuit was further refined and improved under the present contract.

The converter developed under the present contract operates from a 250-to-350-Vdc input bus and provides an output power of 25 kW (1000 V or ± 500 V at 25 Adc). It has a resonant frequency of 20.6 kHz, an output ripple of 3% (peak-to-peak), regulation of better than 0.1%, a response time of less than 2 ms, and its output can be either constant voltage or constant current with automatic crossover. The full-power, 250-V input electrical efficiency measured was 94.8% for the power stage alone, 94.4% with housekeeping power included, and 93.9% with the losses of the solid-state input circuit breaker and output transient-current limiters included. Full circuit details of the converter are presented, along with the test data.

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SECTION 3

CONVERTER DESIGN AND DEVELOPMENT

The hardware designed, developed, fabricated, and tested under this contractual effort is shown in Figure 1. It was designed to meet the following contract specifications and/or goals:

- Resonant frequency - 15 kHz minimum, 20 kHz goal
- Input power - 250 to 350 Vdc
- Output power - ±100 to ±500 V at 25 Adc or 200 to 1000 V at 25 Adc (0 to 25 kW)
- Voltage regulated - 1% (10% load to 100% load)
  - 5% (open circuit to 10% load)
- Current limited (5 to 30 A)
- Output ripple - 1% peak (10% load to 100% load)
  - 5% peak (open circuit to 10% load)
- Efficiency - 92% minimum, 96% goal
- D7ST transistor switches
- Single series-resonant power stage

The delivered hardware has the following specifications and additional features:

- Resonant frequency - 20.6 kHz
- Input power - 250 to 350 Vdc
- Output power - ±100 to ±500 V at 25 Adc or 200 to 1000 V at 25 Adc (0 to 25 kW)
- Voltage regulated - 0.1% (5% load to 100% load)
  - output peaks a maximum of 81 V under open circuit conditions
- Current regulated - 1% (0 to 30 A)

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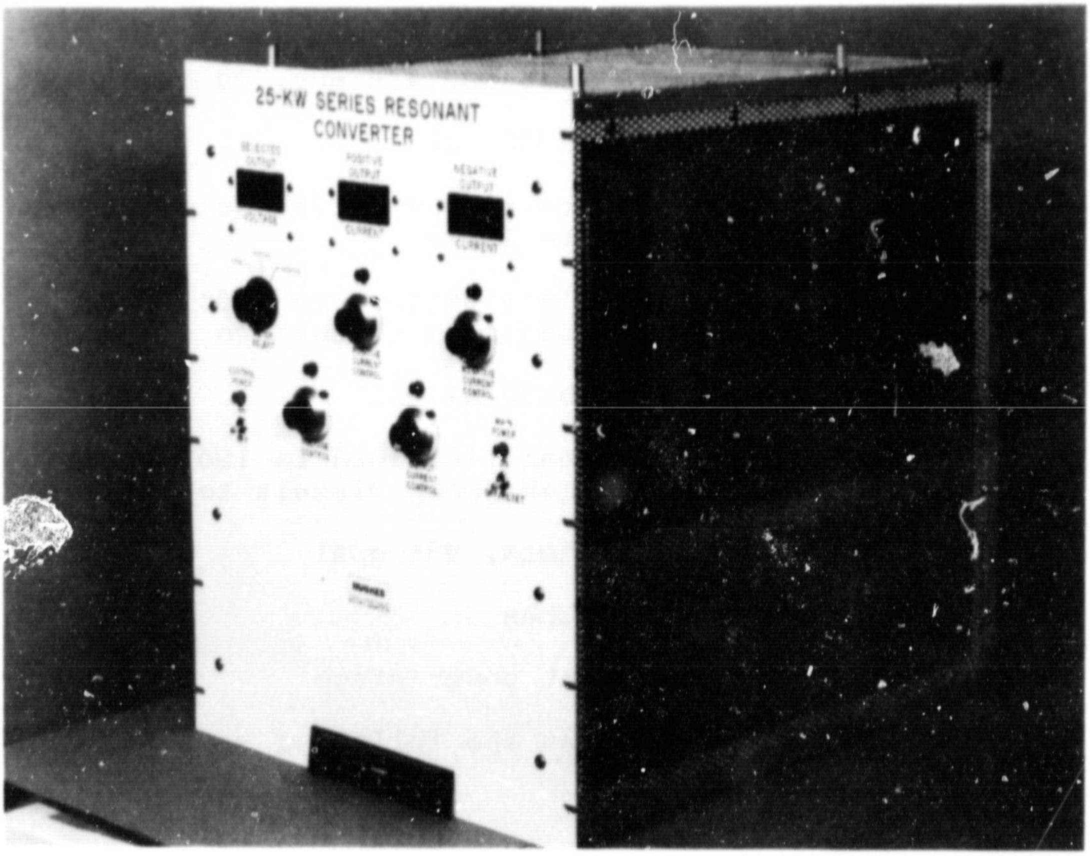

Figure 1. The 25-kW series-resonant converter.

- Output ripple - 10% peak to peak (200 V, 5 A)
  - 2.5% peak to peak (200 V, 25 A)
  - 1.4% peak to peak (1000 V, 5 A)
  - 0.9% peak to peak (1000 V, 25 A)
  - 13% peak to peak (200 V, 0 A)
  - 1.4% peak to peak (1000 V, 0 A)
- Efficiency - 94.4% (250 V input)
  - 94.0% (300 V input)
  - 94.0% (350 V input)
- D7ST transistor switches
- Single series-resonant power stage
- 30-kW solid-state input circuit breaker
- Transient output-current limiters
- Converter will process 30-kW at 300 V input (1000 V, 30 A output)
- Output voltage can be programmed to zero
- Remotely programmable (resistance or voltage)
- Remote on/off (power stage)
- Cooling - forced air
- Size - 48.3-cm W x 62.2-cm H x 61-cm D (19-in. W x 24.5-in. H x 24-in. D)
- Weight - 135.6 kg (299 lbs)
- Component weight - 54.3 kg (119.7 lbs) (includes harness, PC cards, and mounting hardware)
- Specific component weight - 2.17 kg/kW

A block diagram of the converter is shown in Figure 2. The theory and equations relating to operation of a series resonant converter are presented in Appendix I. The major features of the 25-kW converter design are discussed in the following sections.

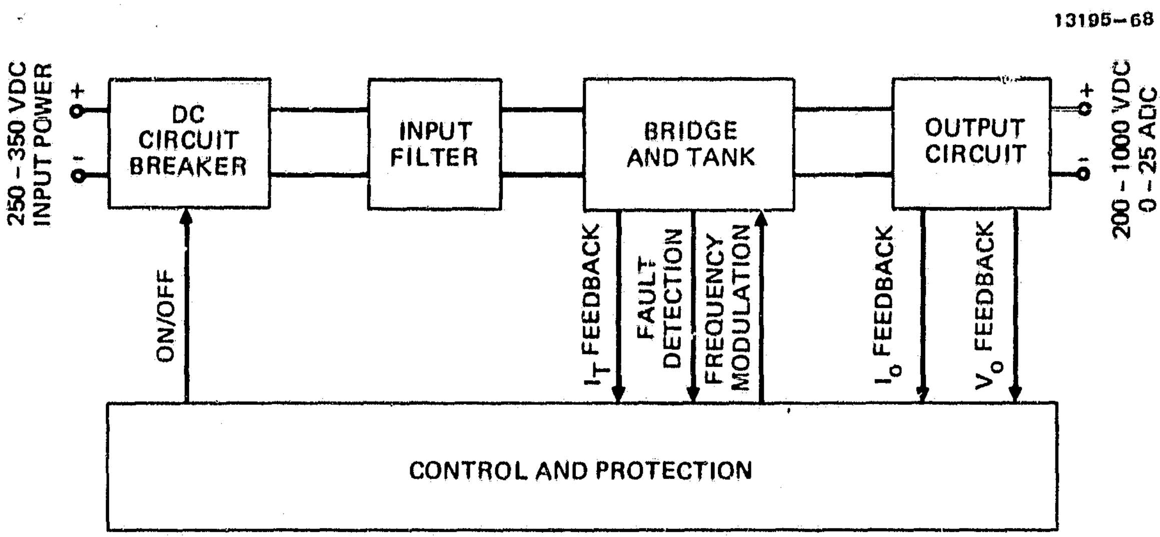

Figure 2. Block diagram of the 25-kW series-resonant converter.

A. BRIDGE CIRCUITRY

A schematic of the bridge and tank circuitry is shown in Figure 3. Transistors Q1 through Q4 are the four switches of the full-bridge, and T3-1 through T3-4 provide the regenerative-feedback base-drive for these transistors. SR1 and SR2 are saturable reactors that limit the value of di/dt in Q1 through Q4, allowing these transistors to saturate quickly, thereby reducing switching losses. SR1 and SR2 saturate in approximately 500 nsec, after which they are effectively out of the circuit. Diodes CR1 through CR4 provide the paths for returning excess energy in the tank circuit to the source (commutating diodes). C3, C4, C98-X, CR33-X, CR54-X, and CR55-X suppress voltage spikes across the collectors-to-emitters of Q1 through Q4, caused by stray wiring inductance and the saturated inductance of SR1 and SR2. These voltage-spike-suppression components are physically mounted as close to Q1 through Q4 as possible. T5 prevents premature conduction of the commutating diodes and the associated "tailing" on the collector currents. Major aspects of the bridge design and components are expanded upon below.

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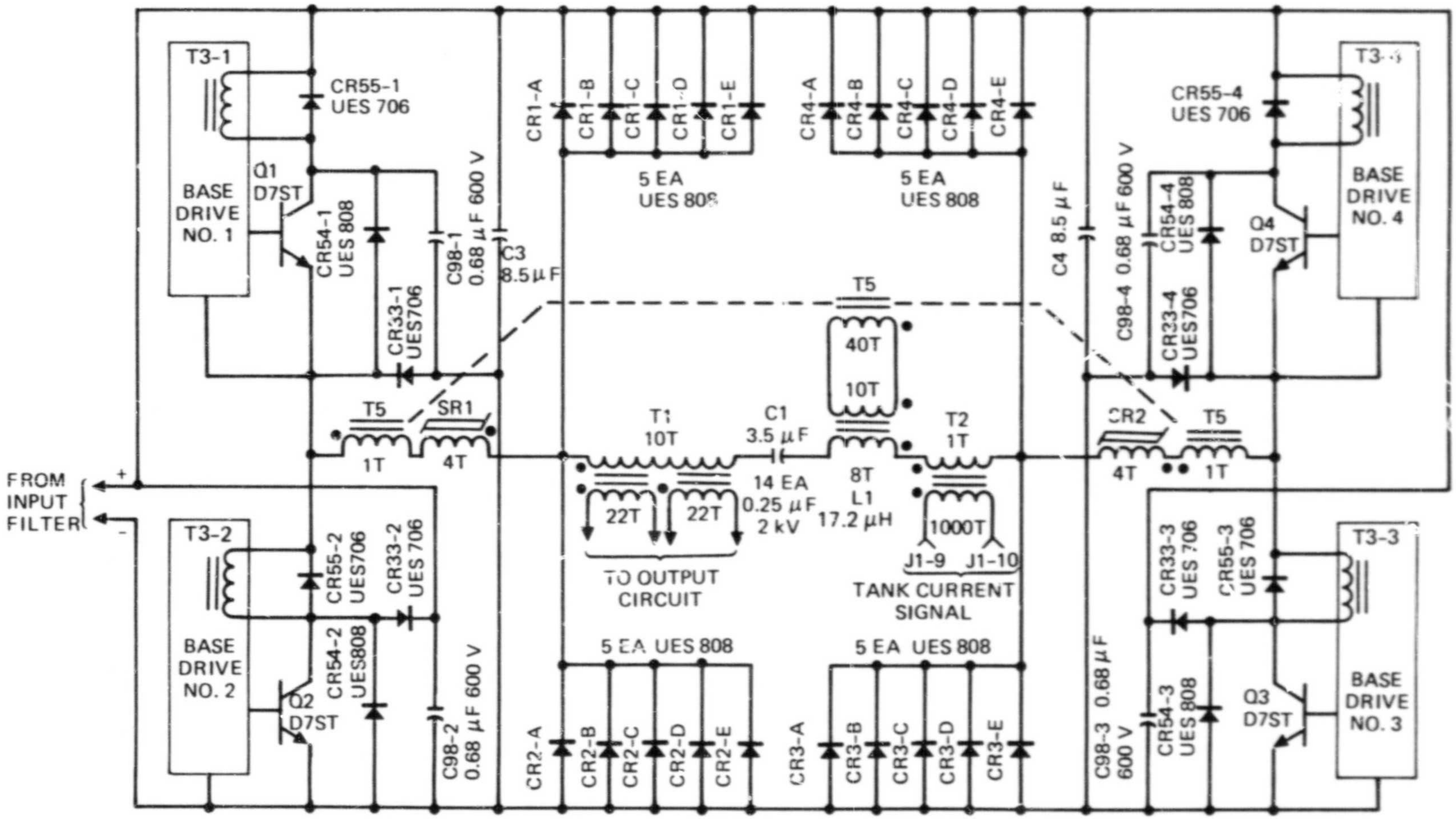

Figure 3. 25-kW series-resonant-converter bridge and tank circuitry.

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1. Transistor Switches

The switches used for the bridge circuit are Westinghouse D7ST transistors; they were provided as Government Furnished Equipment (GFE) to the program. These transistors have a $V_{CEO}(sus)$ rating of 500 V, a peak collector current of 500 A, and a power rating of 1250 W.

The GFE transistors were tested for their turn-on characteristics, saturation voltage, and storage time. Figure 4 shows the waveforms for a typical transistor. In this figure, and in all similar figures of this report, the zero levels for the waveforms are indicated by the lines at the immediate left of the photographs. In Figure 4(a) there is a delay of approximately 100 ns from the time that the base voltage goes positive until the collector voltage starts to fall; the collector voltage then falls to 20 V in approximately 65 ns and stays in a quasi-saturation state for 350 ns before going to zero. The transistors were turned on into approximately 40 A of diode current and were driven by the same base current and base-drive circuit as that planned for the 25-kW converter. The quasi-saturation state is very lossy and can drop the overall efficiency by 1 to 2% or more. The quasi-saturation state is caused by the rise in collector current before the base current has risen to a level sufficient to saturate the transistor (linear operation). The saturable reactors, SR1 and SR2 of Figure 3, prevent this quasi-saturation condition by delaying the rise in collector current until the base current has had a chance to get the transistor into saturation.

Figure 4(b) shows a saturation voltage of approximately 0.5 V at the time of peak collector current (80 A) and a storage time of 6 μs. The measured collector voltage goes negative while the collector current is still positive because of the internal inductance of the transistor package. Table 1 summarizes the characteristics of the GFE transistors, including numbers 12 and 36 which were supplied under contract NAS 3-22471 and which were re-tested here. At a full power level of 25 kW, the

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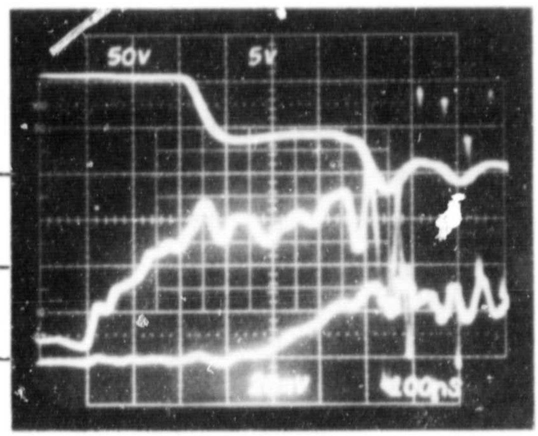
a) WAVEFORM SHOWING TURN-ON DELAY AND QUASI SATURATION FOR A SOURCE VOLTAGE OF 100 V AND COMMUTATING DIODE CURRENT OF 40 A.



b) WAVEFORMS SHOWING THE SATURATION VOLTAGE AND BASE CURRENT FOR A SOURCE VOLTAGE OF 150 V AND ZERO COMMUTATING DIODE CURRENT.

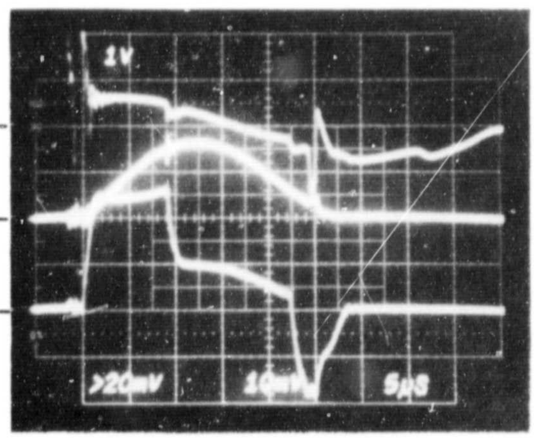


Figure 4. Typical current and voltage waveforms during testing of the D7ST transistor (transistor number 11).

Table 1. Characteristics of the GFE D7ST Transistors

Transistor Number	Turn-On Delay, ns	Quasi-Saturation, ns	Saturation Voltage, (at 80 A) V	Storage Time, μs
24	90	450	0.5	5.5
19	100	580	0.6	5.5
39	100	400	0.6	6.5
11	100	400	0.5	6.0
45	100	400	0.5	6.5
42	150	420	0.5	7.0
18	110	360	0.5	7.0
44	110	380	0.5	7.0
36	120	450	0.5	7.5
12	100	400	0.5	7.5

quasi-saturation time at turn-on gets longer because of higher commutating diode currents, the storage time gets shorter because of higher collector currents which use up more of the excess base drive, and the saturation voltage is higher because of higher collector currents.

2. Commutating Diodes

A significant problem exists in obtaining fast-recovery diodes which are capable of operating at the current and voltage levels required of the commutating diodes in a 25-kW converter. Most high-current (>100 A), fast-recovery (t_{rr} < 100 ns) diodes are produced with voltage ratings up to 150 V. Diodes rated above 150 V require a compromise between recovery times (which increase t_{rr} to 200 ns or more) and forward conduction voltages (which increase V_F to 1 V or more). Therefore, series or parallel techniques for handling 25-kW power levels must be used. The commutating diodes across the four bridge transistors should be as fast as possible to minimize excessively high simultaneous conduction currents during the switching interval. The GFE diodes provided to the program (manufactured by Power Transistor Company) are rated at an average current of 50 A, and have a recovery time of t_{rr} = 200 ns. The recovery time on these diodes was considered to be too slow for use as commutating diodes, in addition to which their limited quantity (only eight) was not adequate since they would also have to be operated in parallel to handle the current. Figure 5 shows the reverse recovery characteristics of one of the GFE diodes and a Unitrode UES-806 for the same test conditions. The reverse current and time are both considerably larger for the GFE diode.

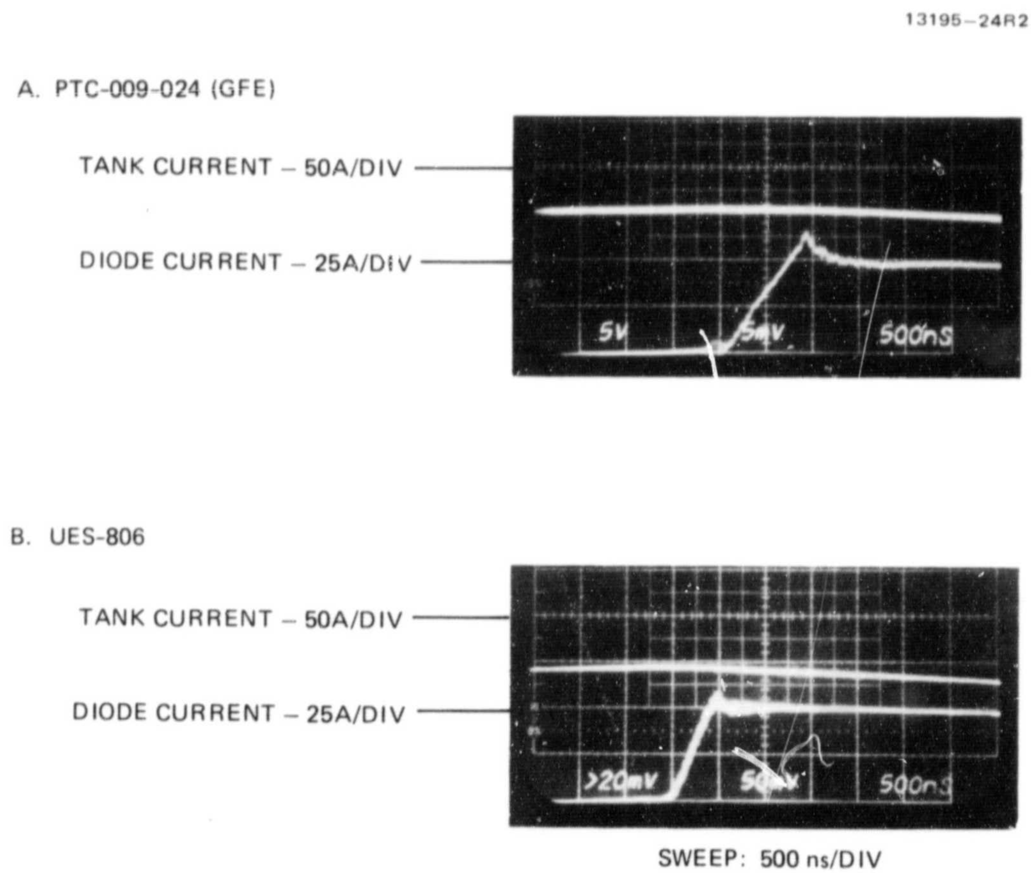


Figure 5. Reverse recovery characteristics of a GFE diode and a Unitrode UES-806 diode.

The Semicon SUES-808 diode with ratings of 600 V, 35 A, and 50 ns was chosen as the best compromise for the commutating diodes. Five diodes are used in parallel to provide a current rating of 175 A (assuming they share equally). Several techniques were considered to force the paralleled diodes to share. Resistors in series with each diode were not seriously considered because of the associated power loss. The "closed-chain-of-reactors" technique illustrated in Figure 6 is very effective but has implementation problems. It is very difficult to mount the balancing transformers physically close to the diodes and keep the stray lead inductances both equal and small. It was decided to rely on matching of the diodes to guarantee adequate current sharing. If the forward voltage drop is matched to within 20 mV, then the diodes will share to better than 5%

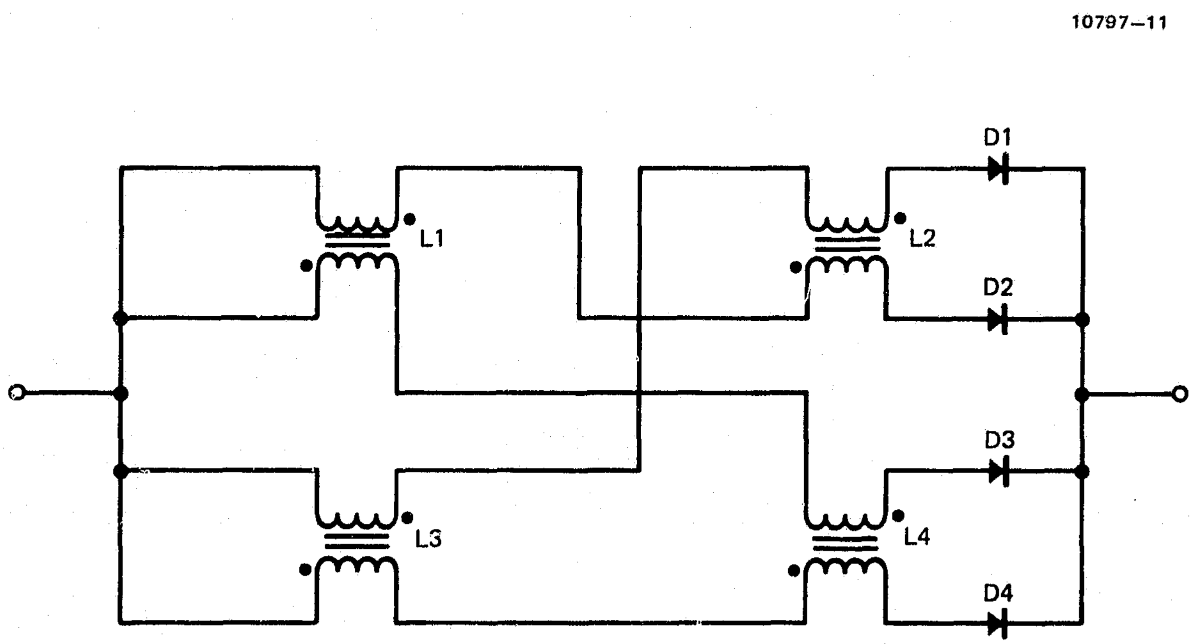


Figure 6. "Closed-chain-of-reactors" technique for forcing paralleled diodes to share the current.

The forward voltage drops on a batch of thirty-five SUES-808 diodes were measured by discharging a 640-μF capacitor through a 1-Ω resistor and the diode under test. Voltage versus current of the diode was displayed on an X-Y storage oscilloscope and the forward voltage drop at various current values along the curve tabulated. These data are presented in Table 2. The four groups of five diodes that were selected for the commutating diodes are: numbers 3, 5, 6, 16 and 18; numbers 2, 7, 8, 9, and 26; numbers 10, 19, 21, 24, and 28; and numbers 13, 15, 23, 25, and 29.

3. Suppression of Voltage Spikes

Stray wiring inductance, leakage inductance of transformers, and the saturated inductance of a saturable reactor can all cause large voltage spikes (>200 V) to occur in the circuit of Figure 3. At a bus voltage of 350 V, a 200-V spike will exceed the collector-to-emitter rating of the D7ST transistors and possibly cause the device to fail.

The diodes and capacitors used for voltage spike suppression in Figure 3 provide three time frames of protection. For times greater than 100 μs, the voltage across Q1 is prevented from exceeding the bus voltage by CR55-1, CR55-2, and CR54-2. The voltage across Q2 is prevented from exceeding the bus voltage by CR55-1, CR54-1, and CR55-2. Q3 and Q4 are similarly protected. In the intermediate time frame of 5 μs to 100 μs, C3 and C4 provide a low impedance ac clamp for the above diodes to work against. For the time frame of less than 5 μs, the voltage across a D7ST is clamped to the voltage of its associated C98-X by way of CR33-X. C98-X charges to nominally the bus voltage and is maintained at that voltage. As the time frame decreases, the associated protection components are mounted physically closer to the D7STs in order to minimize stray inductance. This combination of techniques keeps the voltage spikes across the D7STs to less than 50 V above the bus

Table 2. Tabulation of the Forward Voltage Drops of 35 SUES-808 Diodes at Various Currents

SUES-808 Number	Forward Voltage Drop, V					
	I_F = 10 A	I_F = 20 A	I_F = 30 A	I_F = 40 A	I_F = 50 A	I_F = 60 A
1	0.98	1.08	1.16	1.22	1.27	1.32
2	0.99	1.08	1.13	1.18	1.22	1.26
3	1.03	1.13	1.19	1.24	1.29	1.33
4	1.02	1.10	1.16	1.21	1.26	1.29
5	1.03	1.12	1.18	1.23	1.27	1.32
6	1.04	1.13	1.18	1.23	1.28	1.32
7	0.98	1.06	1.12	1.17	1.22	1.26
8	0.98	1.07	1.13	1.18	1.22	1.26
9	0.98	1.08	1.13	1.18	1.22	1.27
10	0.97	1.05	1.11	1.15	1.19	1.23
11	0.95	1.05	1.11	1.17	1.22	1.26
12	0.94	1.05	1.12	1.17	1.22	1.27
13	1.01	1.09	1.15	1.20	1.24	1.28
14	1.00	1.08	1.14	1.18	1.22	1.26
15	1.00	1.08	1.16	1.19	1.23	1.28
16	1.03	1.12	1.18	1.24	1.28	1.33
17	0.96	1.04	1.10	1.15	1.18	1.23
18	1.03	1.13	1.18	1.24	1.28	1.32
19	0.97	1.05	1.11	1.16	1.20	1.23
20	0.96	1.07	1.14	1.19	1.24	1.29
21	0.98	1.06	1.12	1.16	1.20	1.24
22	0.96	1.07	1.14	1.20	1.25	1.30
23	1.00	1.08	1.14	1.19	1.23	1.27
24	0.97	1.05	1.11	1.15	1.19	1.23
25	1.00	1.09	1.14	1.19	1.23	1.27
26	0.99	1.08	1.14	1.18	1.22	1.26
27	0.99	1.08	1.13	1.18	1.22	1.26
28	0.97	1.06	1.12	1.16	1.20	1.24
29	1.00	1.08	1.14	1.19	1.23	1.27
30	0.95	1.05	1.11	1.17	1.21	1.26
31	1.04	1.13	1.18	1.22	1.26	1.31
32	1.02	1.10	1.16	1.20	1.24	1.28
33	1.06	1.15	1.20	1.25	1.30	1.33
34	1.03	1.12	1.18	1.23	1.27	1.32
35	1.04	1.13	1.18	1.23	1.27	1.31

voltage and less than 1 μs in width, with peak currents greater than 300 A in the bridge and tank circuitry.

4. "Tailing" of the Collector Currents

Initial testing of the converter revealed that the current in the transistor switches (Q1, Q2, Q3, and Q4 of Figure 3) was "tailing" out rather than following the half-sinusoidal shape of the tank current. This effect is shown in Figure 7 which depicts the ideal and "tailed" out waveforms. This "tailing" is due to stray inductance and the saturated inductance of the saturable reactors. For purposes of discussion, Q2, CR2, CR54-2, T3-2, and SR1 of Figure 3 will be referenced specifically, but the following discussion applies to any of the four transistor switches. Also assume for the moment that T5 does not exist. If Q2 is conducting, then when the half-sinusoidal current pulse passes 90°, the stray and SR1 inductances start to force the cathode of CR2 negative with respect to the bus return. As soon as the cathode of CR2 is ≈0.7 V negative, CR2 starts to conduct, and current circulates through CR2, SR1, T3-2, Q2, and back to CR2. The amount of inductance required to cause this problem can be calculated from

$$V = L\,\frac{di}{dt} \quad . \tag{1}$$

The current in Q2 is

$$I = 200 \sin \omega t$$

and

$$\omega = 1.26 \times 10^5 \quad .$$

Substituting into (1):

$$V = 200\,\omega L \cos \omega t \quad .$$

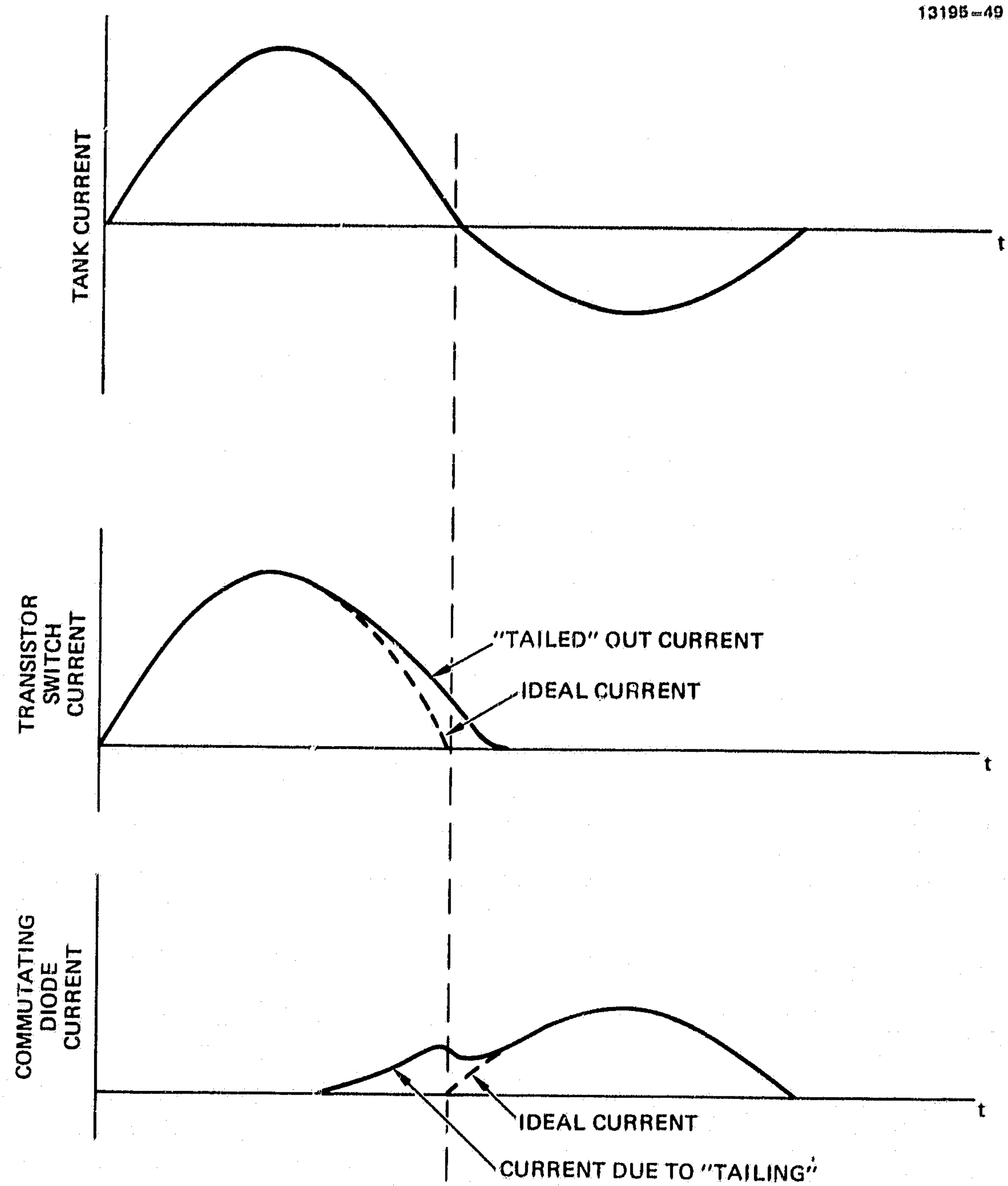


Figure 7. "Tailing" of the transistor switch current due to stray inductance.

The maximum voltage developed will be

$$V_m = 200\ \omega L \quad ,$$

and

$$L = \frac{V_m}{200\ \omega} \quad .$$

If we assume that the total voltage drop across Q2, T3-2, and CR2 is 2 V, then

$$L = 7.9 \times 10^{-8} = 0.079\ \mu H.$$

Therefore, a total inductance of 0.08 μH due to stray inductance and SR1 will begin to cause "tailing" in this circuit. It is not possible to keep even the stray inductance below 0.08 μH, and therefore a circuit change was required to eliminate the "tailing". The "tailing" cannot be tolerated because it causes turn-off losses in Q2.

Many schemes (>20) were analyzed and/or evaluated in the circuit in an effort to solve this problem. This included the method used by Stuart[1] (at the University of Toledo) and others of putting inductance in series with each switch instead of using the saturable reactor of Figure 3. These techniques cannot be scaled to this power level and still keep the collector-to-emitter voltage on the transistor switches under control. Even if some of these techniques could have been scaled, they would only have eliminated the problem with the saturated inductance of the saturable reactors, and not the stray inductance problem.

The only scheme found that works is the addition of transformer T5 of Figure 3. A portion of the voltage across the series-resonant inductor (L1) is fed back out-of-phase with the voltage developed across the stray and SR1 inductances and effectively cancels it out. The cathode of CR2 is not driven negative now; therefore, CR2 does not conduct, and the "tailing" is eliminated. A similar problem was encountered with CR54-2 conducting, causing "tailing". The problem with CR54-2 was minimized but not totally eliminated by mounting it as physically close to Q2 as possible. The problem with CR54-2 could be further minimized by a lower inductance package for the D7ST.

The power removed from L1 by T5 is purely reactive and therefore does not introduce an efficiency penalty into the circuit (except for the small winding and core losses of T5). Figure 8 shows the collector-to-emitter voltage of Q3 going negative before the tank current (and collector current) has gone to zero (due to the inductance of the D7ST package), and the cathode of CR3 remaining positive (because of T5) until the tank current has gone to zero.

B. TANK CIRCUITRY

The series resonant tank (see Figure 9) is composed of C1, L1, T1, and T2 of Figure 3. The final parameter values for this tank circuit are:

- $C = 3.356\ \mu F$ (measured at 1 kHz)
- $\omega = 1.29 \times 10^5$ (20.6 kHz) (measured at 25 kW)
- $L = 17.8\ \mu H$ (calculated)
  $= 19.0\ \mu H$ (measured at 1 kHz)
- $Z_O = \sqrt{\frac{C}{L}} = 0.434\ \Omega$
- Source Voltage = V_S = 250 to 350 V
- Output Voltage = 1000 V

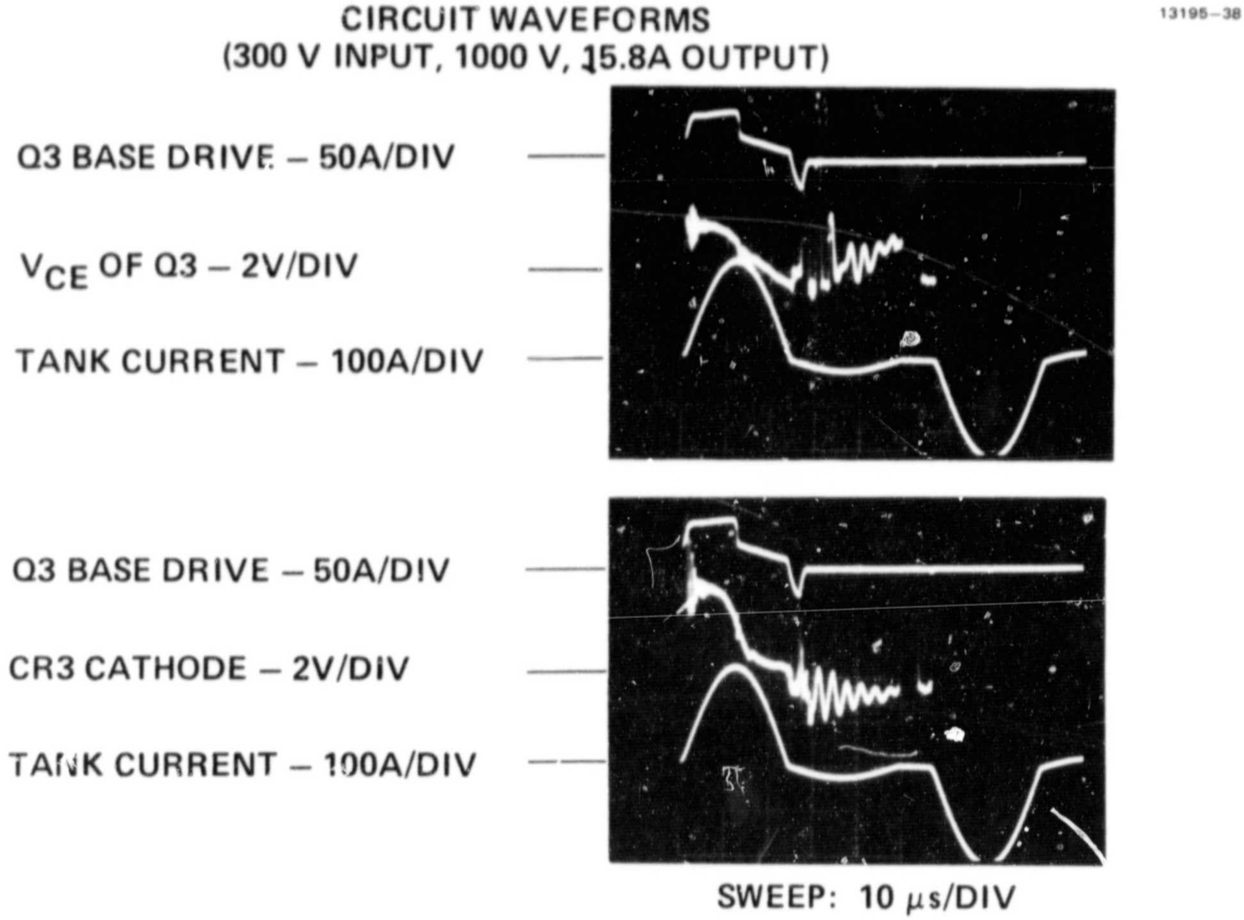


Figure 8. Oscillographs showing the C-E voltage of Q3 going negative before the tank current goes to zero and the cathode of CR3 remaining positive until the tank current goes to zero.

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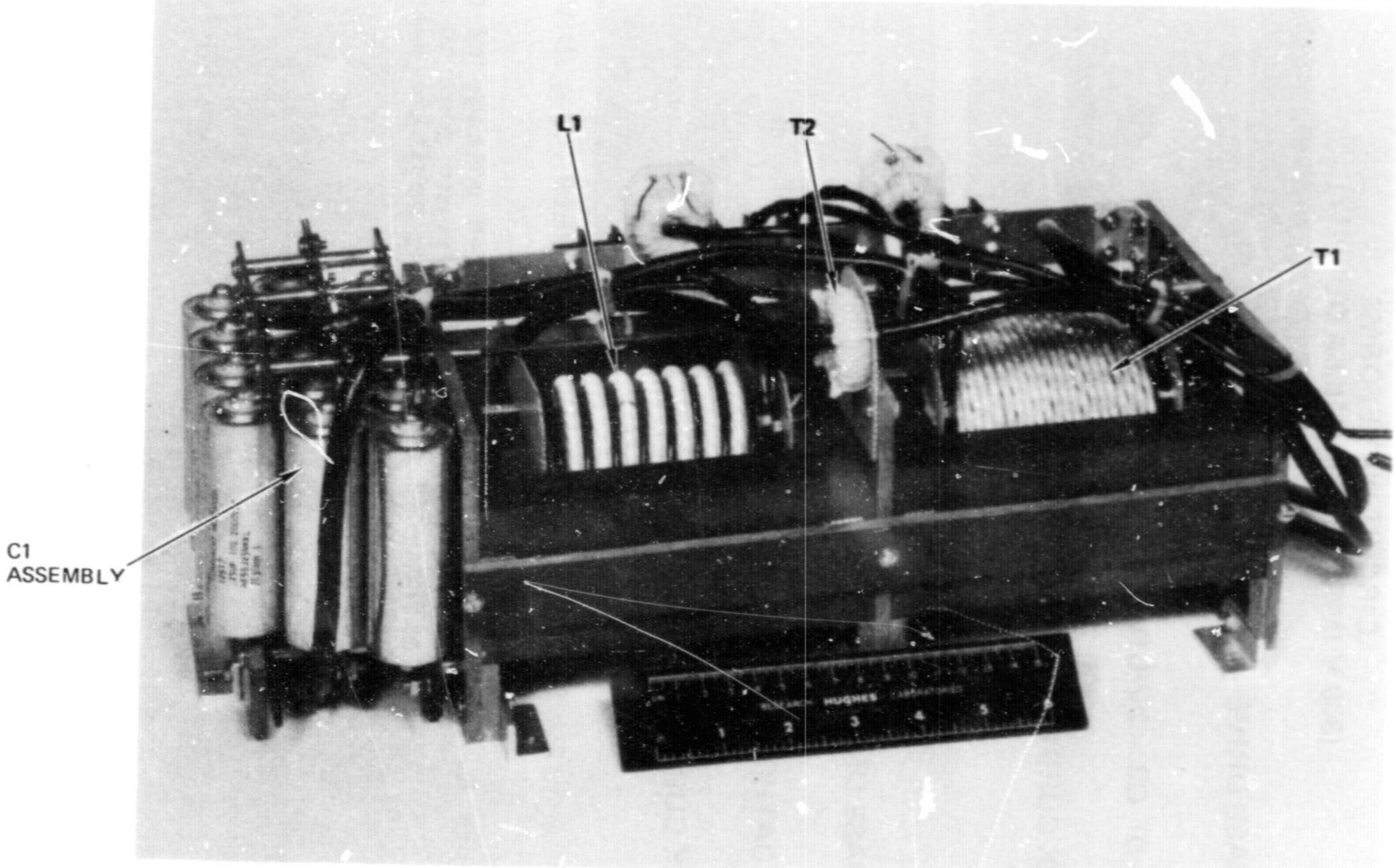

Figure 9. The series resonant tank assembly.

- Transformer Turns Ratio = 10:44 = 1:4.4
- Output Current = 25 A (30 A)
- Average Tank Current = 110 A (132 A)
- Minimum Diode Conduction Angle ≈ 0.35 rads

T2 is a 1000:1 current transformer that provides a tank-current feedback-signal to the control circuit. The other components and characteristics of the tank circuit are discussed below.

1. Series Resonant Capacitor

The series resonant capacitor (C1) is made up of fourteen 0.25-μF ± 10% polypropylene capacitors in parallel. Each capacitor is rated for 2000 Vdc and 25 A rms at 20 kHz. This particular capacitor was selected because of its ready availability from Component Research; it also provides a means of easily changing the total capacitance value in relatively small steps, which is desirable in a development program. Polypropylene is the only dielectric that is feasible at the required current and frequency because of its low dissipation factor.

2. Magnetic Cores

The magnetic core configuration chosen for L1 and T1 is shown in Figure 10. The E-core configuration was chosen (over a C-core configuration) to minimize the air-gap fringe-flux interaction with surrounding components and structure. Each core is composed of six separate parts: two side bars, two end bars, and a two-section center post. The two-section center post allows the air gap to be placed in the center of this post, and the air gap can be adjusted by substituting various length center posts and/or moving the end bars in or out. The core is clamped together by the mounting frame, as shown in Figure 9.

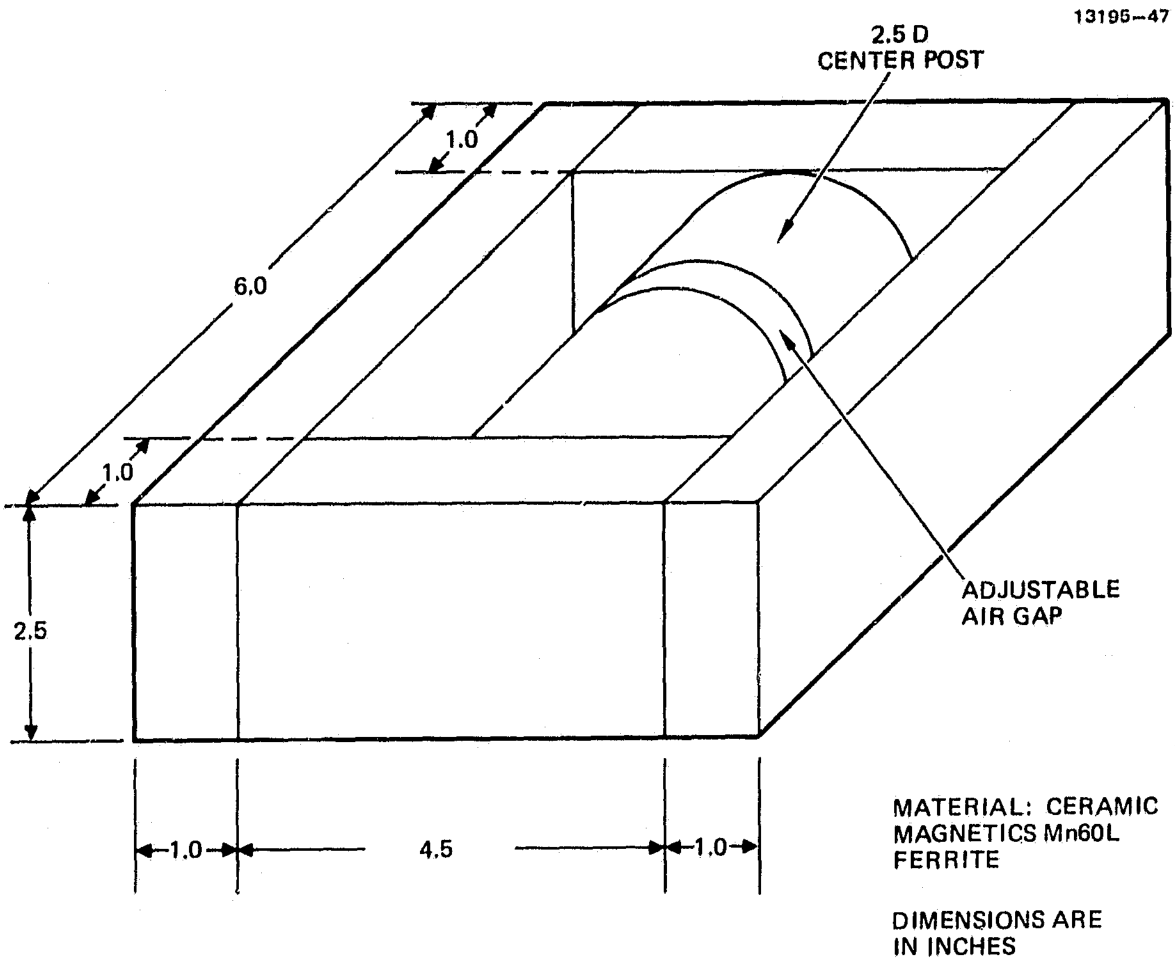

Figure 10. Core configuration for the resonant inductor and output transformer.

Mn60L ferrite from Ceramic Magnetics Inc. was chosen as the core material because of its very-low-loss characteristics (8 mW/cm^3 at 20 kHz and 1000 gauss; 45 mW/cm^3 at 20 kHz and 2000 gauss). The cores were sized to operate at 1000 to 1500 gauss where the losses will be less than 20 mW/cm^3. For the core shown in Figure 10, the total loss is less than 24 W, and therefore cooling of the core is not a problem. At full-power operation the temperature of the cores was below 40°C.

3. Series Resonant Inductor

The series resonant inductor (L1) is wound from eight turns of 1323/36 (5 AWG) Litz wire on the center post of the ferrite E-core described above. The core has a 2.44-cm (0.96-in.) air gap in the center post. The secondary winding that feeds T5 is wound from ten turns of 150/36 Litz wire and is wound between the turns of the main winding.

This inductor measured 19.0 μH at 1 kHz, but calculations based on a measured resonant capacitor value of 3.356 μF and a resonant frequency of 20.6 kHz indicate that the inductance of the resonant tank is really 17.8 μH. This inductance includes the leakage inductance of the output transformer which was measured to be 1.9 μH. Therefore, the inductance of the series resonant inductor is really about 16 μH.

4. Output Transformer

The output transformer has a 10-turn primary of 1323/36 (5 AWG) Litz wire and two 22-turn secondaries of 210/33 (10 AWG) Litz wire wound on the center post of the ferrite E-core described above. The core has a 0.019-cm (0.0075-in.) air gap in the center post, and the primary winding is sandwiched between the two secondary windings to improve coupling. The transformer has a primary leakage inductance of 1.9 μH and a primary inductance of 1.06 mH.

Operating at 25 kW, the windings of the transformer approach 140°C, which is the temperature limit on the wire. The transformer is not potted, but does have a small amount of forced-air cooling. No effort was made under this program to provide better cooling for the windings.

5. Output Transformer Saturation Under Light Load Conditions

When the converter is operating into a light load (~250 Ω), sub-resonant-frequency currents (that have also been observed by TRW[2] and Stuart[3] of the University of Toledo) flow in the series resonant tank. These sub-resonant-frequency currents result when the voltage on the resonant capacitor is still greater than the input bus voltage after the normal commutating diode-conduction period, and the modulation frequency is such that the tank current is discontinuous. Under these conditions, the commutating diodes start to conduct again in an effort to further lower the voltage on the resonant capacitor. The voltage applied to the output transformer is not sufficient to cause the output rectifiers to conduct, and therefore the primary inductance of the output transformer appears as part of the series resonant tank. The tank then starts to ring at a frequency determined by the resonant capacitor, the resonant inductor, and the output-transformer primary inductance (note that this is not a sub-harmonic of the normal resonant frequency, but a function of the output transformer primary inductance). These sub-resonant-frequency currents cause additional volt-seconds to be applied to the output transformer core with the result that the output transformer then approaches saturation during the normal resonant-frequency pulse. As the output transformer approaches saturation, it draws a very large magnetizing current (>50 A). When the magnetizing current is equal to the resonant tank current, there is no current available for the output; therefore, the output rectifiers stop conducting and the primary inductnce of the transformer is added in series with the resonant tank. This added inductance increases the resonant period of the tank circuit, causing the transistor switches to turn OFF before the tank current has gone through zero, since their turnoff is determined by the normal resonant-tank period and not by the time at which the tank current actually passes through zero.

Figure 11 shows sub-resonant-frequency currents starting to flow approximately 85 μs after the start of the normal resonant current pulse. Figure 12 shows the effect of the output transformer approaching saturation. The T1 secondary current goes to zero before the tank current does (at ≈23 μs), which causes the T1 primary voltage to reverse and the T1 primary inductance to be inserted into the resonant circuit. The tank then starts to resonate at a lower frequency, followed by turn-off of the transistor switches at ≈ 28 μs.

This phenomenon does not cause any major problems in the operation of the converter or cause any components to be overstressed (with the possible exception of the transistor switches if they are not properly protected - see Section 3.F.8 below on protection circuits). It does cause jitter in the feedback loops and an increase in audio noise.

C. BASE DRIVE CIRCUIT

The base-drive strategy and basic circuit for driving the transistor switches was developed under Contract NAS3-22471 (Resonant Circuit Transistor Characterization).[4] The strategy developed is as follows. Regenerative (or proportional) feedback of the collector current is used since it minimizes the required power from the rest of the base-drive circuitry. At the same time, the transistor is maintained at a constant β (except during the leading-edge pulse), which saves on base-drive power. The base current is allowed to go to zero as the collector current goes to zero, which minimizes the storage time. The base-drive parameters from the transistor characterization that resulted in minimum total device dissipation are employed, and the base-emitter junction is kept reverse biased during the transistor off-time, which eliminates dV/dt turn-on caused by C_{OB} of the transistor switch.

Data taken on the D7ST transistor during Contract NAS3-22471 at 20 kHz and 250 A showed that the minimum device

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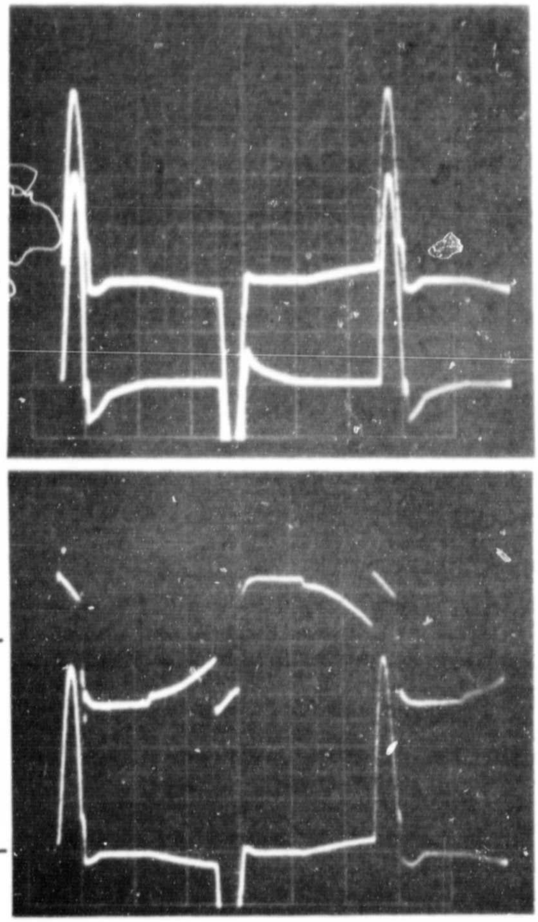
TANK CURRENT – 50A/DIV

T1 SECONDARY – 10A/DIV

T1 PRIMARY – 200 V/DIV

TANK CURRENT – 50A/DIV



SWEEP: 50 μs/DIV

Figure 11. Oscillographs showing sub-resonant-frequency currents flowing in the tank under light load (200 Ω) conditions.

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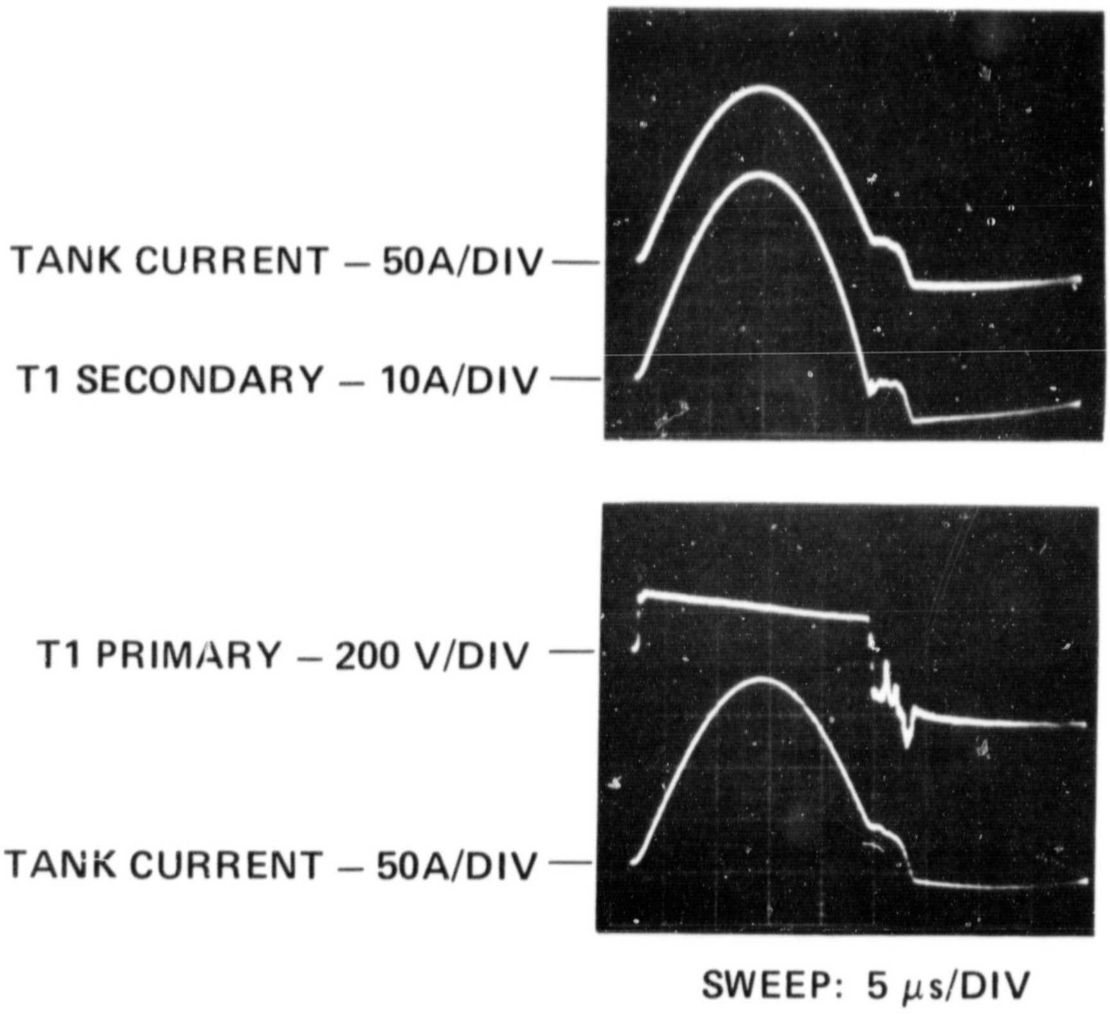
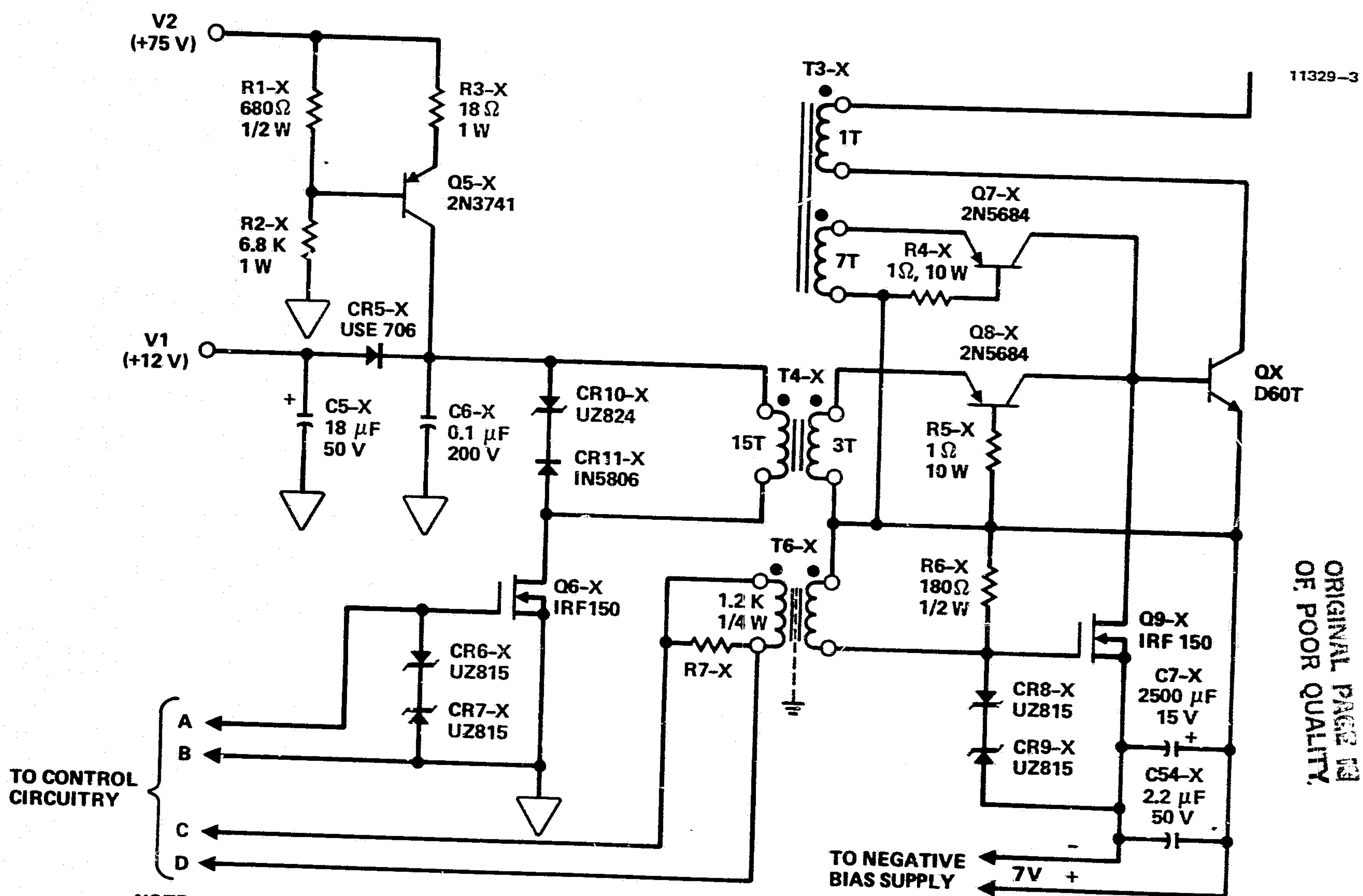


Figure 12. Oscillographs showing the effect of the output transformer approaching saturation under light load (200 Ω) conditions.

dissipation occured at a regenerative feedback ratio of 10:1, with a leading-edge pulse of 30-A amplitude and 12.5-μs width (30 A was the highest amplitude available from the test equipment). Testing in a half-bridge series resonant test circuit, however, revealed that the regenerative-feedback ratio must be lowered to at least 8:1 and the leading edge pulse increased to 40 A in order to keep the D7ST in saturation. It is also important that the leading-edge pulse have a rise time of 1 μs or less in order to minimize the turn-on time and get the transistor into saturation quickly. The turn-off pulse (negative I_B pulse) needs to be large in amplitude in order to minimize the storage time, which then allows for maximum utilization of the series-resonant tank.

Conventional transformer-coupled base-drive circuits will not provide a 30 A pulse with a rise time of 1 μs or less because of the leakage inductance of the transformer, base-emitter inductance of the transistor switch, and stray inductance of the wiring. The circuit of Figure 13 was developed under Contract NAS3-22471 to provide a 30-A pulse with a rise time of 1 μs or less and a 7:1 regenerative feedback ratio. Referring to Figure 13, Q5-X forms a constant-current source that charges capacitor C6-X to the voltage potential of V2. When Q6-X is turned on to apply a leading-edge pulse to QX, the high voltage charge (V2 = 75 V) on C6-X is applied to the primary of T4-X. This high voltage overcomes the effect of the leakage inductance of T4-X, the stray wiring inductance, and the base-emitter inductance of QX, allowing the base current to rise to 30 A in approximately 1 μs. After the charge on C6-X has decayed to potential V1 (12 V), the remainder of the leading-edge pulse is supplied from V1 through CR5-X. The width of the leading edge pulse is controlled by the on-time of Q6-X.

The regenerative feedback is supplied by transformer T3-X. A separate transformer is used for the regenerative feedback so that the leakage inductance of T4-X (supplying the leading-edge



NOTE: THE -X ON PART IDENTIFIERS REFERS TO THE BRIDGE TRANSISTOR THAT THE BASE DRIVE IS ASSOCATED WITH (Q1, Q2, Q3 OR Q4)

Figure 13. Base-drive circuitry for the 10-kW converter (one to four) developed under Contract NAS 3-22471.

pulse) can be minimized. Transistors Q7-X and Q8-X are used to isolate the tranformers so that the base of QX can be held at a negative bias during the time that it is turned-off. Q9-X supplies the turn-off pulse to the base of QX, and holds it at the negative bias level of -7 V. T6-X is used to provide an isolated turn-off pulse to Q9-X during the on-time of QX.

This basic circuit was used for the 25-kW converter with some modifications, which are shown in Figure 14. It was found to be necessary to increase C6 from 0.1 μF to 0.39 μF in order to get a leading-edge pulse with a rise time of less than 2 μs. This resulted in a power requirement of 110 W (440 W for all four base-drive circuits) just to obtain the rise time on the leading edge pulse. By replacing R1, R2, R3, and Q5 of Figure 13 with CR30 and L2 of Figure 14, C6 is resonantly charged with a power requirement of only 20 W and a lower voltage source. The resonant charging of C6 is automatically triggered by the switching action of Q6. Figure 15 shows the current and voltage waveforms associated with this resonant charging.

Q18 and CR9 were added to the circuit to improve the drive signal to Q9 and improve the reset characteristics of T6. R8 and R9 were added to eliminate the ringing caused by the input capacitance of the IRF-150s (Q6 and Q9).

A base-emitter voltage-sense circuit composed of VR29, R61, R62, C9, and U9 was added to provide an indication of whether the D7ST is ON or OFF. If the base-emitter voltage is greater than -5V the D7ST is considered to be ON, if this voltage is less than -5V it is considered to be OFF. A value of -5V was chosen as the transition point since during turn-off, the base-emitter voltage that can be measured (terminals on the transistor package) is a few volts negative while the transistor itself is still forward biased. This is due to the resistance and inductance that exists inside the transistor package.

Standard optical couplers, such as a 6N136, were found to be inadequate for use in this base-emitter voltage-sense circuit (U9-U10 combination). The input-to-output capacitance

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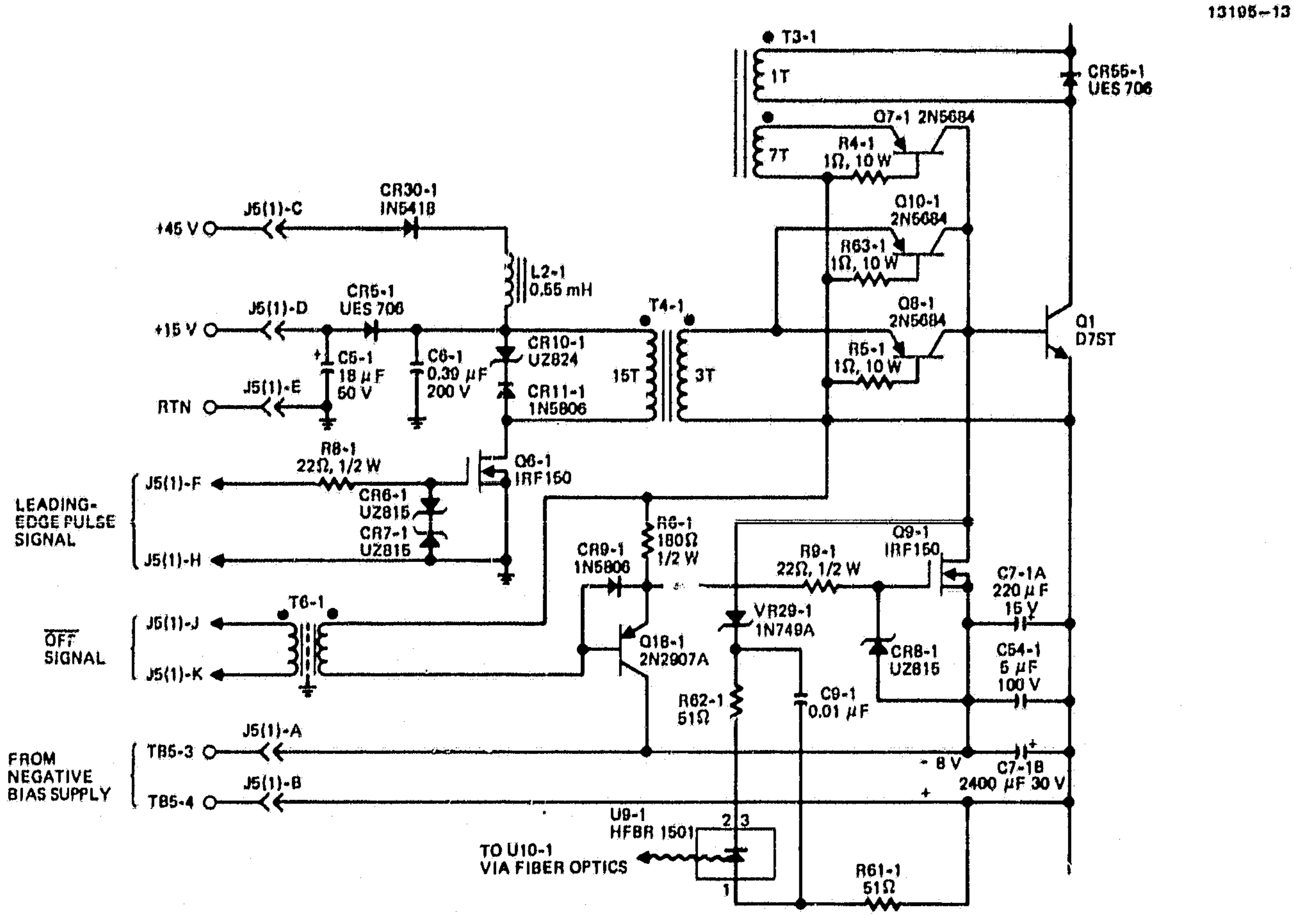

Figure 14. Base-drive circuitry for the 25-kW converter (one of four).

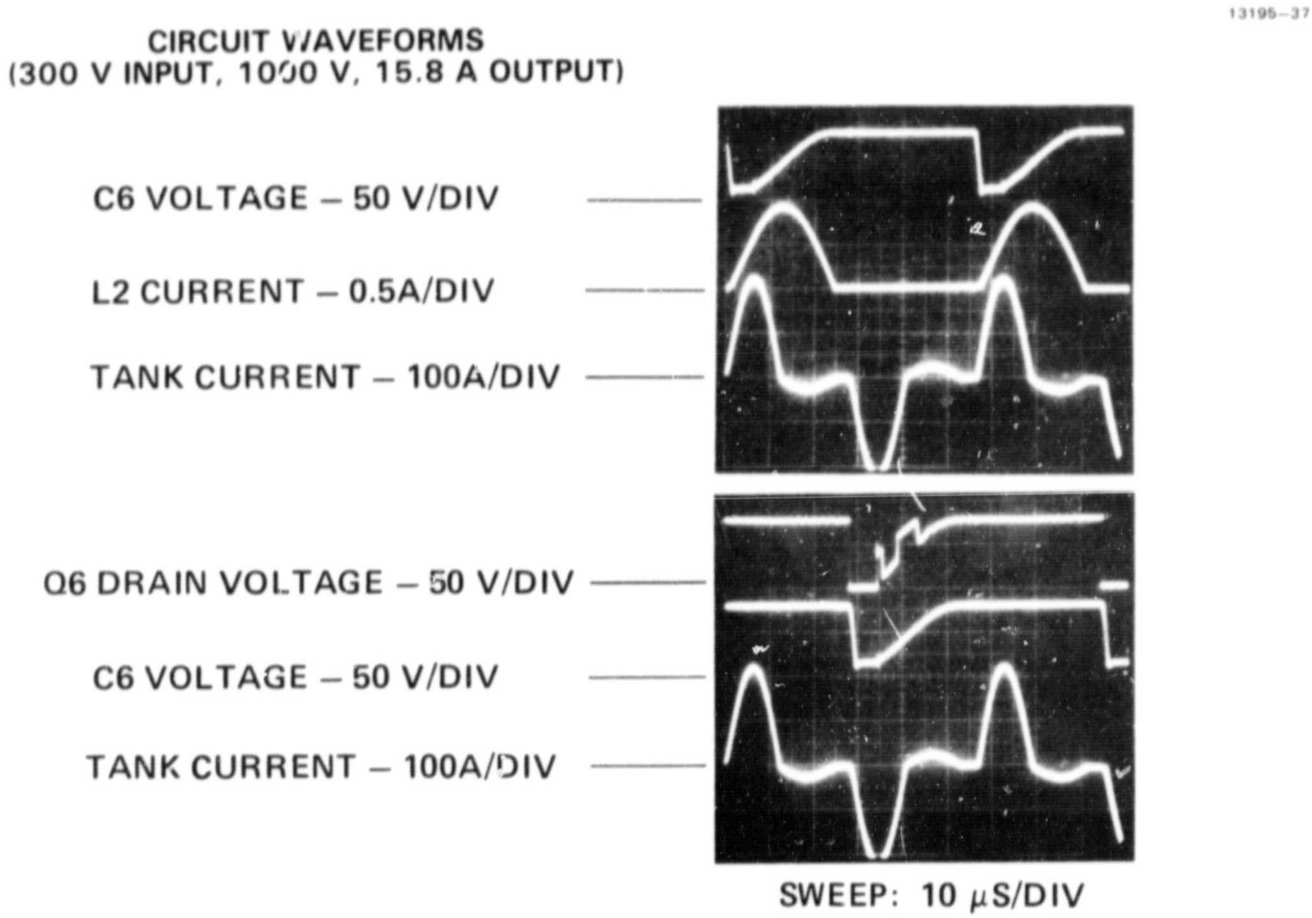

Figure 15. Oscillographs showing the resonant charging of C6.

of these devices (~1 pF for a 6N136) is sufficient to cause false signals under the 1000-V/μs conditions that exist in the circuit. Replacing the optical coupler with a fiber-optic link was the only way found to eliminate the noise problem and still maintain the sub-microsecond response required of the circuit.

Figure 16 shows the transistor switch (D7ST) base-drive waveforms provided by the circuit of Figure 14. The leading-edge pulse is 50 A in amplitude and 12.5-μs wide. The turn-off pulse is -30 A, which keeps the storage time down to ~4 μs. Initial testing of the converter was done with a 30-A leading-edge pulse which resulted in a power stage efficiency of 92% at 25 kW and 350 V input. Increasing the leading-edge pulse to 50 A, increased this efficiency to 94.3% at the cost of only 80 W of housekeeping power. This represents an overall efficiency gain of 2% and demonstrates the necessity of getting the transistor switches into hard saturation quickly.

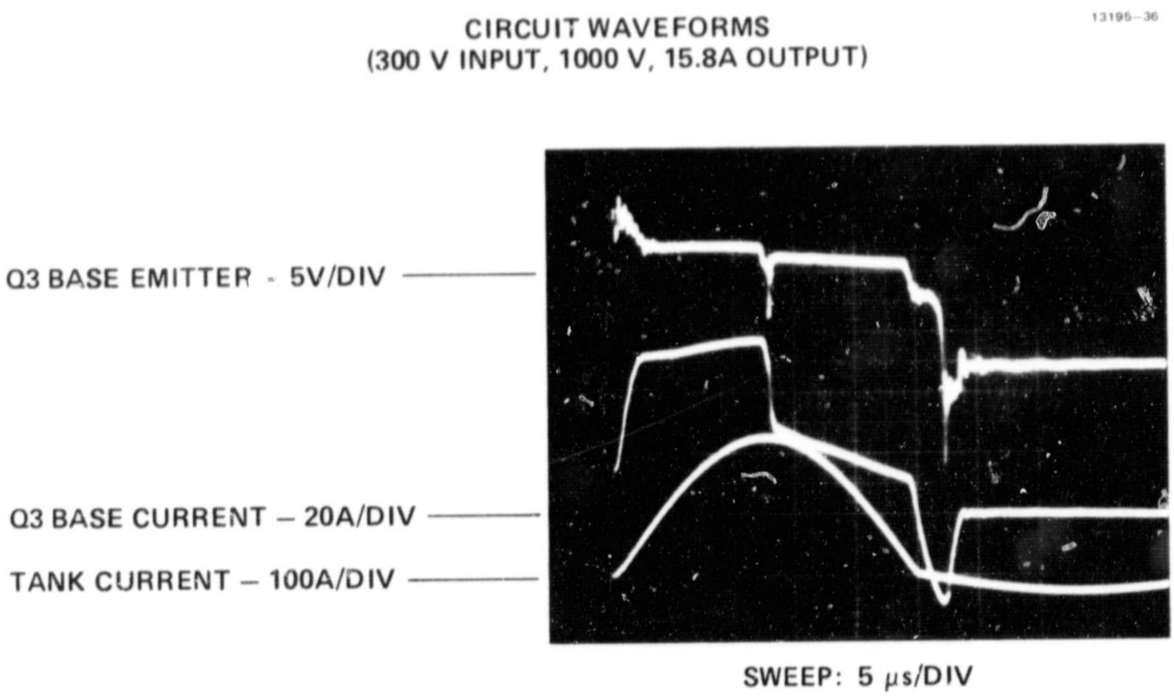

Figure 16. Transistor switch (D7ST) base-drive waveforms.

D. OUTPUT CIRCUIT

The schematic of the output circuitry is shown in Figure 17. The ac current supplied by T1 is rectified by two full-bridge circuits, CR12 through CR15, and CR16 through CR19. The split secondary on T1 and the two rectifier circuits allows the output to be configured as a single 0-to-1000-V output or as a dual 0 to ± 500 V output. The two halves of the output are filtered by C100 through C103 and C104 through C107. The filtered power is then connected to the output terminals through transient-output-current limiters (Q35/Q36 and Q37/Q38 with their associated components) which will be discussed in Section 3.E below. The currents in the positive and negative output legs are measured by current transformers T10 and T11, respectively, for use by the control circuitry and by shunts R99 and R100, respectively, for the front panel meters. The output voltage is sensed either locally or remotely by the voltage divider, R184 through R196, to provide a feedback signal to the control circuitry. By selection of one of three connector plugs (P6) that is mated to J6, the voltage, which is sensed and controlled can be either the total output voltage, the positive half, or the negative half. The three voltages are also displayed on one front panel meter by way of a rotary switch. The front-panel-meter circuitry is shown in Figure 18.

The GFE diodes were used for the output rectifiers (CR12 through CR19) where their 1000-V, 50-A, and 200-ns rating adequately matched the circuit requirements. A faster recovery time is desirable but not critical to circuit operation or efficiency.

The original output-circuit design called for 40 μF of polypropylene capacitor in each half of the output. This was increased to 80 μF in order to reduce the output ripple which is still larger than desired under light load or reduced output voltage conditions (see test data). The output capacitors were not further increased because increasing them increases the

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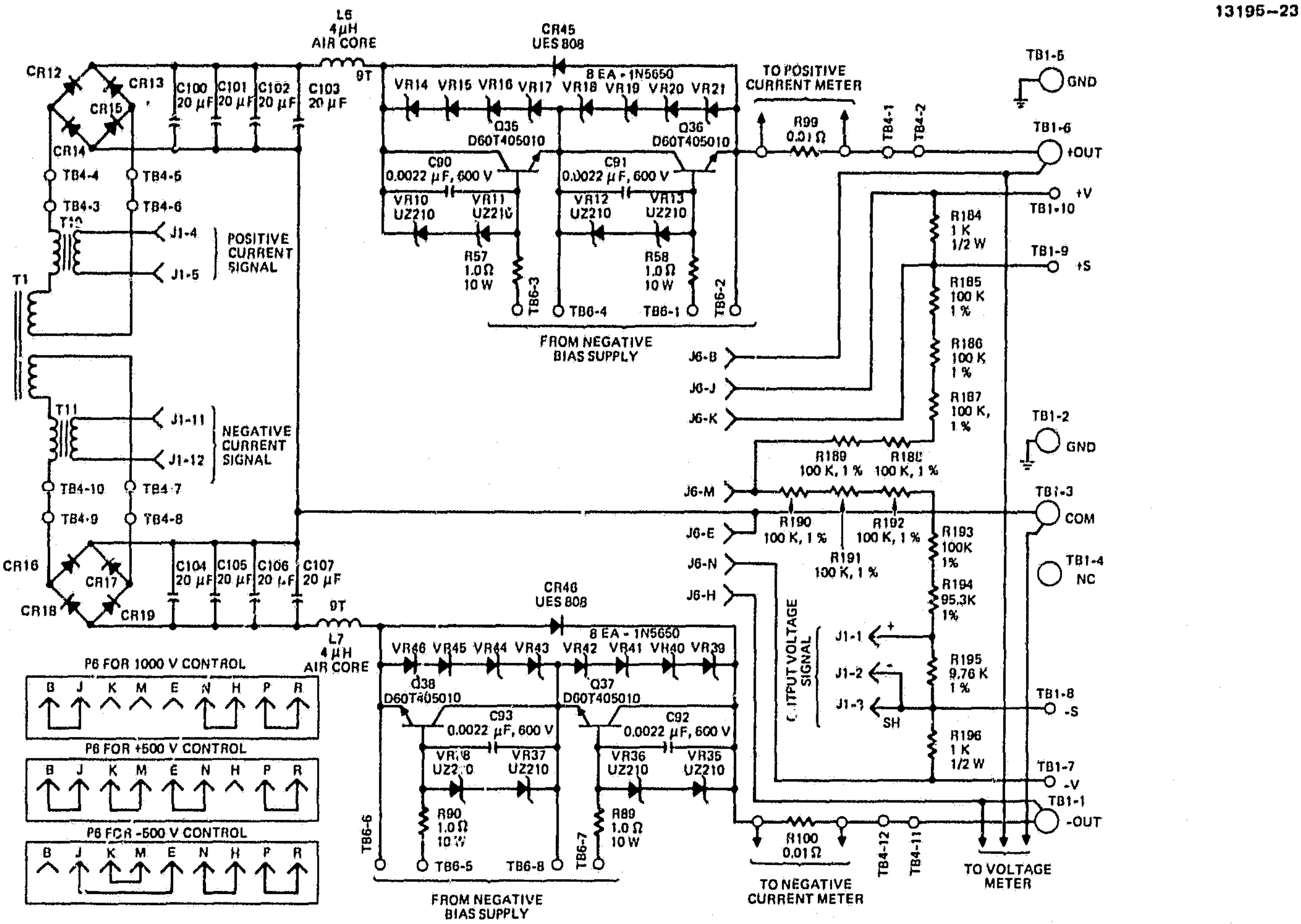

Figure 17. Output circuitry of the 25-kW converter.

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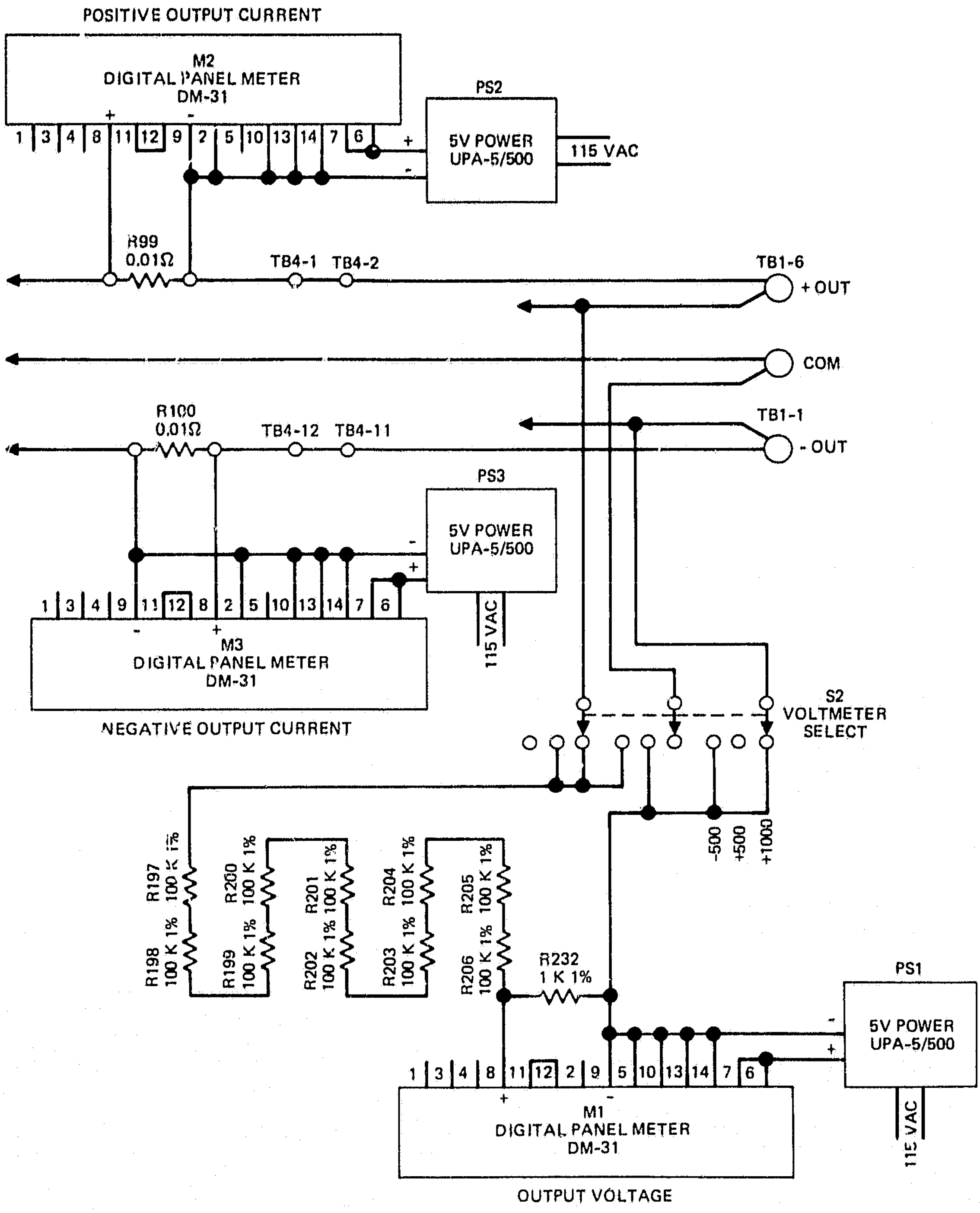

Figure 18. Front panel meter circuitry.

response time of the voltage feedback loop, which is not desirable. Therefore, a compromise must be made between output ripple and response time.

E. OUTPUT-TRANSIENT-CURRENT LIMITERS

The output-transient-current-limiters are shown as part of the output circuitry in Figure 17. Only the positive output will be discussed since the negative output operates in an identical manner.

Several possibilities were considered to provide the output-transient-current-limiting function. A 0.5-Ω resistor in each output lead would limit the peak current to 1000 A, but would also dissipate a total power of 625 W at an output of 25 A. This corresponds to 2.5% of the maximum output power, and is therefore unacceptable. Another approach is to use an inductor in series with the output. A 40-μH inductor will limit the output current to approximately 700 A for an output-filter capacitor of 80 μF. This would cause a damped oscillation at a frequency of 2.8 kHz during a transient. These inductors would also make the output of the inverter inductive at all times (which may be undesirable).

A third approach considered was to use inductors whose cores are held in saturation by permanent magnets. The device (shown pictorially in Figure 19, along with its B-H curve) works on the theory that the permanent magnet will keep the core saturated until the ampere-turns in the winding exceed a certain value. While the core is saturated, the device will have a very low inductance, but once the core comes out of saturation the inductance will increase dramatically, thereby limiting the transient current. However, the peramanent magnet looks like an air-gap, and the actual B-H curve looks more like the dotted curve in Figure 19 than the solid curve. The greatest inductance change measured with this device was 3 to 1, which is not sufficient to make the device practical. Holding the core

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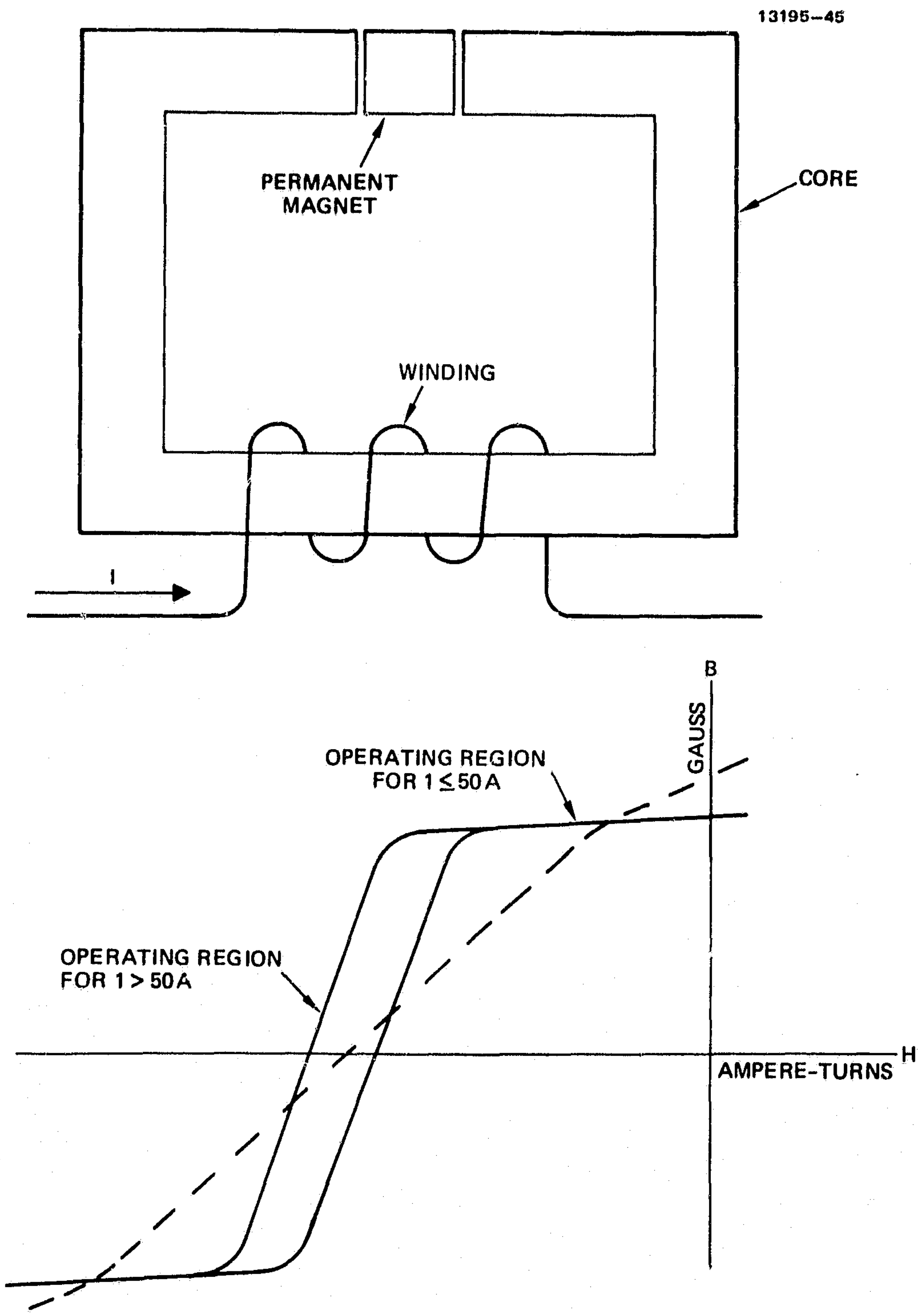

Figure 19. Permanent-magnet biased inductor.

in saturation with a second winding is also not practical because of the voltage and/or current (depending on the turns ratio) involved with the second winding.

The device that was decided upon is a transistor. Q35 of Figure 17 receives a constant base-drive current from an output of the negative-bias supply through R57; therefore, Q35 acts as a constant-current source (beta times its base current). The base drive is set for a constant collector current of ~60 A, which keeps Q35 in hard saturation over the normal output-current range of 0 to 30 A. When a transient-current condition exists (>60 A), Q35 comes out of saturation and limits the current to 60 A. In practice, a relatively large current spike (~250 A) exists on the leading edge of a transient, as shown in Figure 20. This current spike is due to the excess carriers stored in Q35. Once the excess carriers are depleted, Q35 tries to come out of saturation very quickly (< 100 ns). If allowed to do so, a destructive voltage transient would result on the collector of Q35 due to high di/dt and circuit inductance. To prevent this destructive voltage spike from occuring, C90, VR10, and VR11 were added to the circuit to limit di/dt to a safe value. VR14 through VR17 are transient voltage suppressors that limit the voltage across Q35 to ~250 V and force it to share the voltage with the other transistors (Q36, Q37, and Q38). Inductor L6 was added to the circuit to roll off the leading-edge on very fast transients. Figure 20 shows the large current spike on the leading edge which lasts for ~25 μs, then a current plateau at 75 A for ~150 μs which corresponds to current flowing through the transient voltage suppressors as well as the transistors, another plateau at 60 A lasting ≈600 μs and representing the beta-limited current of the transistors, and finally the current falling to 25 A as the stored charge in the output capacitors is depleted. For purposes of comparison, the output-transient-current limiter was shorted out (except for L6) and the peak output current was 640 A for a 200 V charge on the output capacitor. At 500 V on the output capacitor, the peak current would be 1600 A without the transient-current limiter.

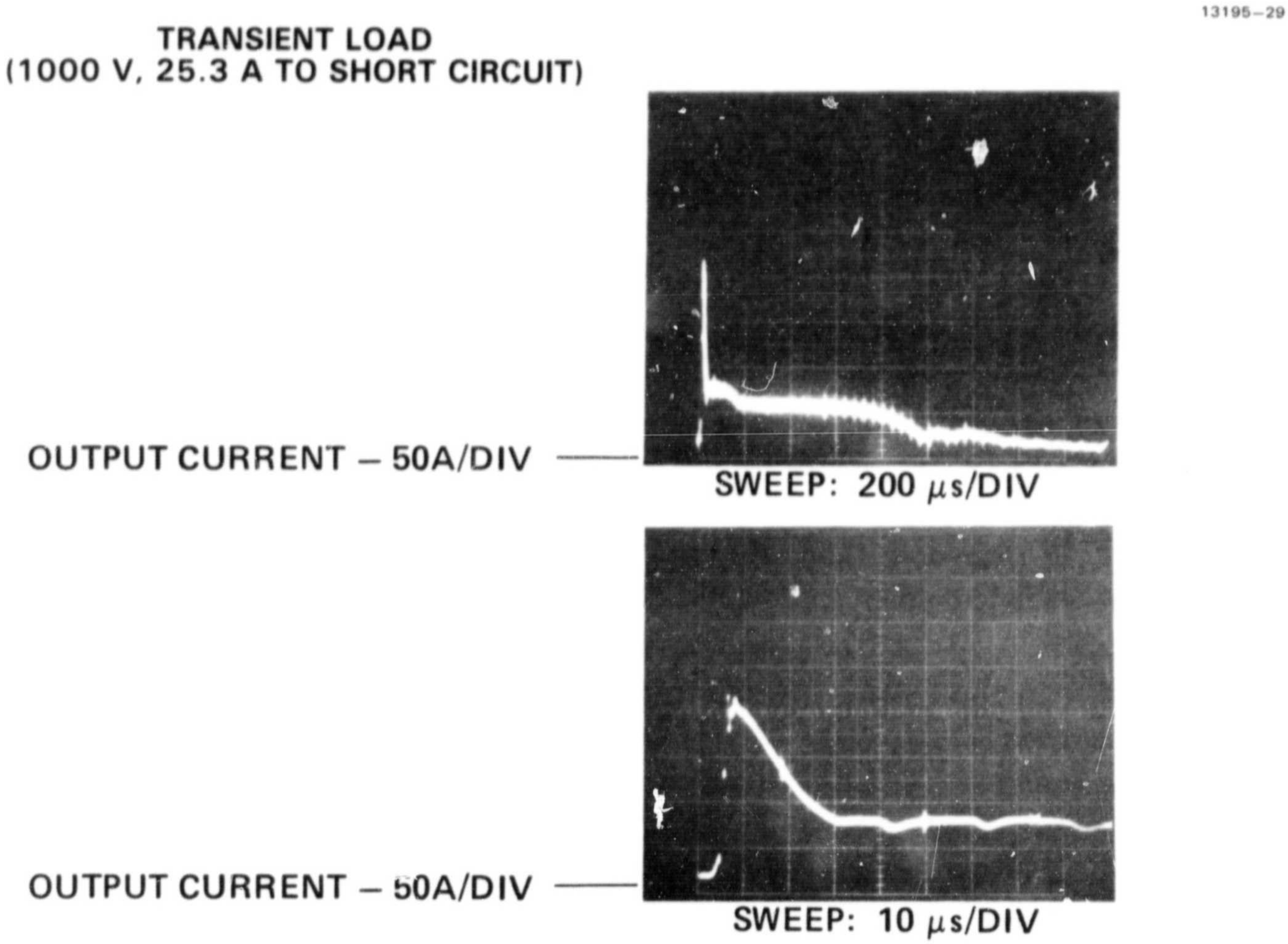

Figure 20. Transient output current during a transient from full load to short circuit.

The initial design of the output-transient-current limiters called for only one transistor in each leg of the output. The transistor chosen was a high voltage (650 V) version of the Westinghouse D60T (D60T654005). This transistor would discharge a 40-μF capacitor charged to 500 V, but would fail when the capacitor was charged to 525 V, indicating very little margin (if any) in the design. Failure was the result of forward-biased second-breakdown. In earlier testing of a design where the transistor was reverse biased during the high current transient, reverse-biased second breakdown occured with the capacitor charged to only 75 V. This shows the necessity of keeping the transistor forward biased.

The possibility of using a slower but more rugged transistor in place of the D60T was investigated. Tests using a D7ST (≈ 3 times slower) indicated that the peak current increased in direct proportion to the storage time. Even though the D7ST will absorb three times the energy that a D60T will, it is also required in this application because of the factor-of-three increase in peak current. Therefore, the net gain in safety margin was zero. The most straightforward approach (and the one chosen) to the solution of this problem was to use two D60Ts (D60T405010) in series. This approach increases the safety margin in two ways. First, the total energy to be absorbed is now shared by two devices which increases the margin by a factor of two. Second, because the maximum voltage that the transistor sees is now 250 V instead of 500 V, at least twice as much energy can be absorbed without failure (energy absorbtion capability drops significantly as the voltage increases). This gives another factor of two in safety margin and a total factor of at least four.

F. CONTROL AND PROTECTION CIRCUITS

The control circuitry for the converter involves four feedback loops: one for controlling the output voltage, one for controlling the average current in the tank circuit, one for controlling the current in the positive-output leg, and one for controlling the current in the negative-output leg. All four loops have separate reference signals and automatically cross-over from one loop to another with each loop preventing its controlled parameter from exceeding the value set by its reference signal. Protection circuits are included to prevent the output voltage from exceeding 50 V over the reference level, to prevent the peak tank current from exceeding 350 A, to prevent the transistor switches from turning off if the tank current is greater than 70 A, and to trip the input circuit breaker if the bus voltage falls below 50 V, if Q1 and Q2 or Q3 and Q4 are on simultaneously, or if the Q1 or Q4 collector currents flow for greater than 50 μs. These circuits are discussed in the following sections.

1. Output-Voltage Feedback Loop

The output-voltage feedback loop is shown in Figure 21. The output voltage feedback-signal is isolated from the floating output by isolation amplifier AR1. This feedback signal is then compared against the output-voltage-reference signal (from R28) and the difference integrated by the feedback around AR2. R120 and C64 form a lead-lag network with R21 for loop compensation. The integrator is confined to the normal operating range by the clamp circuit comprised of R24, R27, CR20, and VR6. Q40 is used to reset the integrator to zero. Comparator U16 senses when the output voltage is more than 50 V higher than the referenced level and immediately triggers the integrator reset circuit. This keeps the output voltage under control during transient and open circuit conditions.

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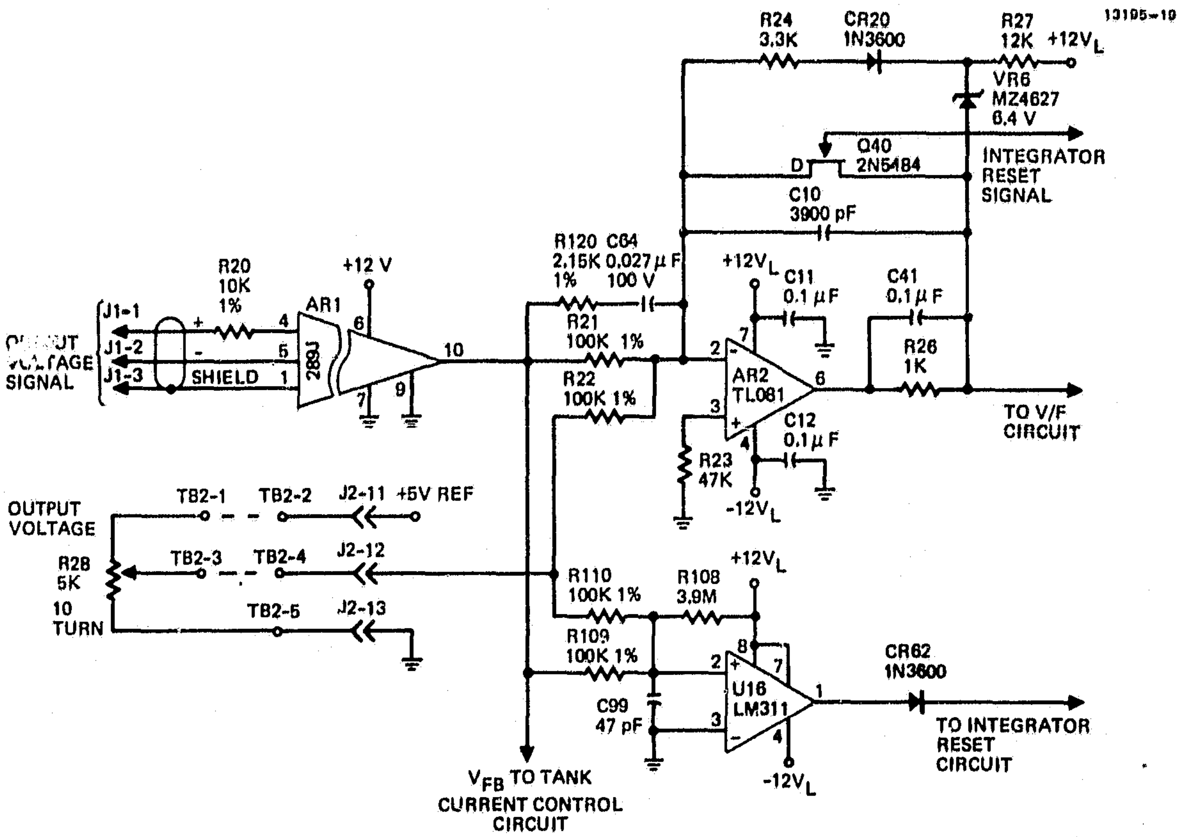

Figure 21. Output voltage feedback loop.

2. Tank-Current Feedback Loop

The tank-current feedback loop is shown in Figure 22. The sum of the average current in the positive-output leg and the negative-output leg is related to the average current in the series-resonant-tank circuit by the turns ratio of T1. Therefore, the average tank current can be sensed and used to control the sum of the output currents, while at the same time protecting the bridge and tank-circuit components. The tank current is sensed by current transformer T2, rectified by CR24 through CR27, and converted to a voltage by R34. This voltage is then compared against the tank-current reference signal (from R30) and the difference integrated by AR3. This integrator is confined to its normal operating range by a clamp circuit comprised of R35, R36, CR22, and VR8 and reset by Q41. AR5A and AR5B sense when the output voltage has fallen below a certain level (determined by the output current reference-signal - 185 V for a reference level of 25 A) and then linearly phase the output current back to 11 A as the output voltage falls to zero. The static-output operating envelope produced in this manner is shown in Figure 23 where the solid curve represents the rated output current, and the dashed curve represents extended operation at the maximum current limit. Comparator U15 senses when the peak tank current exceeds 300 A and immediately triggers the integrator-reset circuit, which in turn phases the inverter OFF. The integrators can immediately start to integrate up and phase the inverter back ON to the referenced set point. This comparator limits the peak tank current and protects the components of the bridge and tank circuitry during transient conditions. Currents are limied to a peak value of 350 A and the voltage on resonant capacitor C1 is limited to 1600 V.

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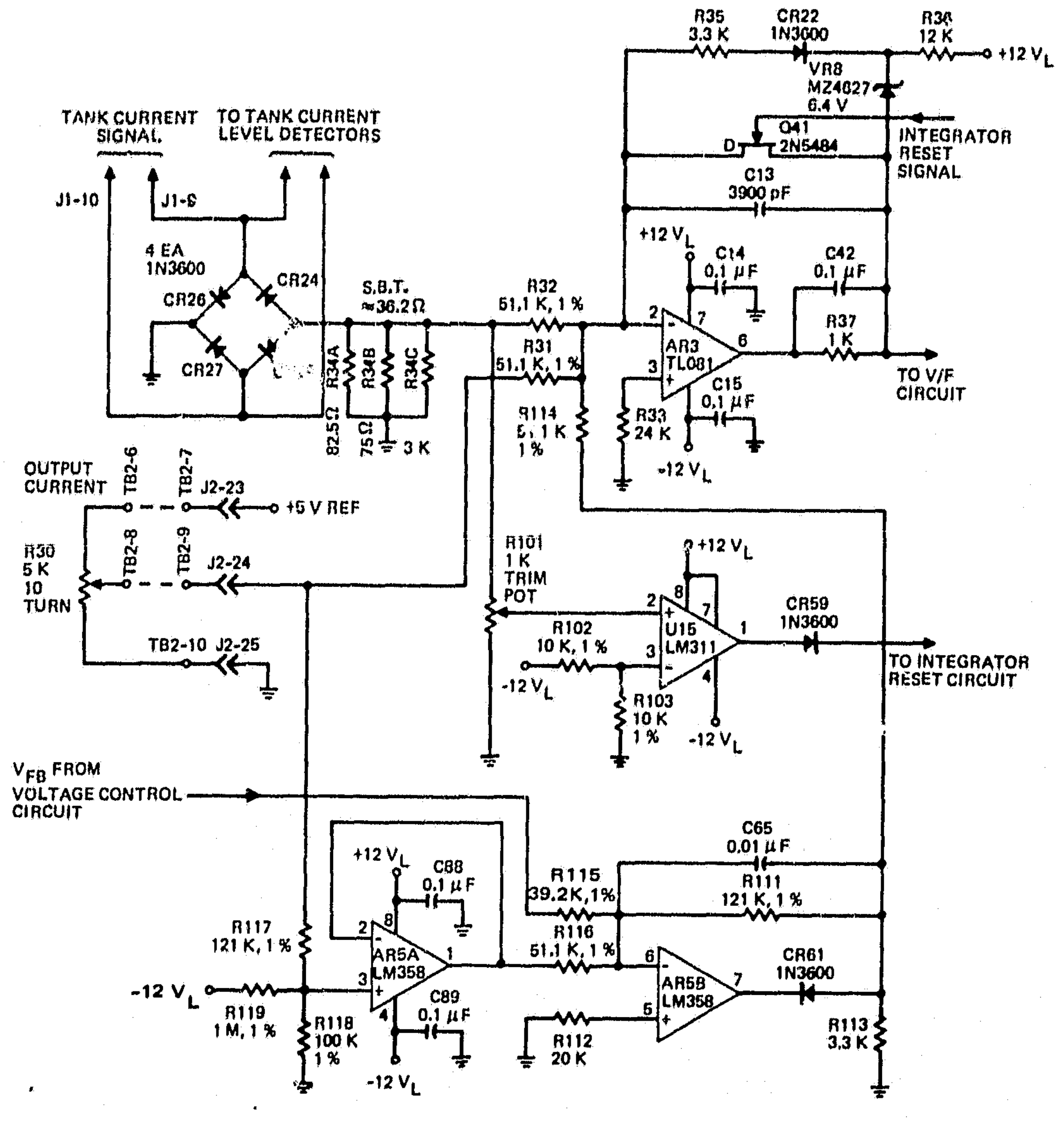

Figure 22. Tank current feedback loop.

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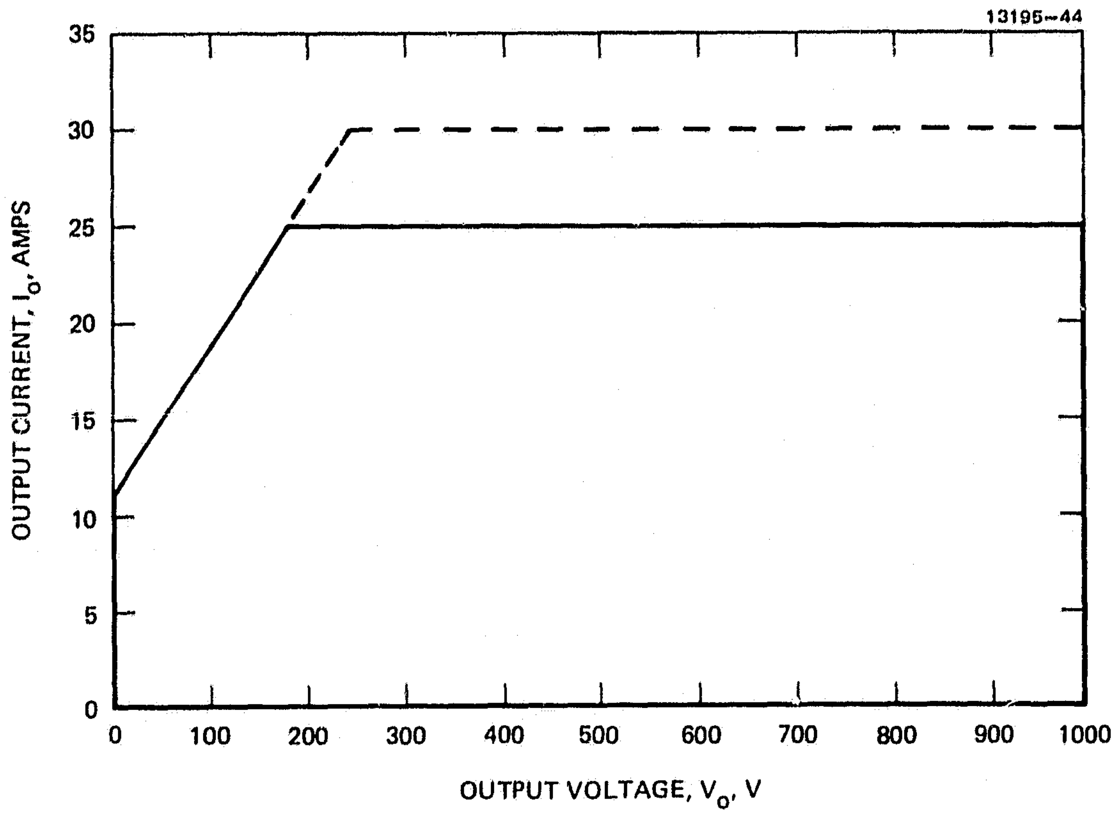

Figure 23. 25-kW converter static output operating envelope.

3. Positive and Negative Output-Current Control Loops

The positive and negative output-current control loops are shown in Figure 24. The two loops are identical and therefore only the positive loop will be described. The positive output current is sensed by current transformer T10 (Figure 17), rectified by CR80 through CR83, and converted to a voltage by R132. This voltage is then compared against the reference signal from R131 and the difference integrated by AR6. This integrator is confined to its normal operating range by a clamp circuit comprised of R136, R138, CR84, and VR2, and reset by Q42.

4. Voltage-to-Frequency Converter and Integrator Reset Circuitry

The voltage-to-frequency (V/F) and integrator reset circuitry is shown in Figure 25. The outputs from the voltage and current feedback circuits, along with the integrator reset signal, are diode-OR'd to the input of the V/F converter. The diode-OR'd functions provide control by limiting how far R38 is allowed to phase ON the inverter, while VR9 provides a maximum limit to which the inverter can be phased ON. The actual V/F converter, U2, uses AR4 to improve its linearity, operating range, and response time. The output of the V/F converter is then routed to the base-drive circuitry to time the turn-on of the transistor switches in the bridge.

The excessive output voltage, excessive tank current, and external ON/OFF signals are diode-OR'd to produce the integrator reset signal. This signal resets the integrators in all four feedback loops and drives the V/F output to zero frequency.

5. Controlling Feedback Loop Indication

The circuitry for indicating which feedback loop has control of the converter is shown in Figure 26. The quad comparator (U14)

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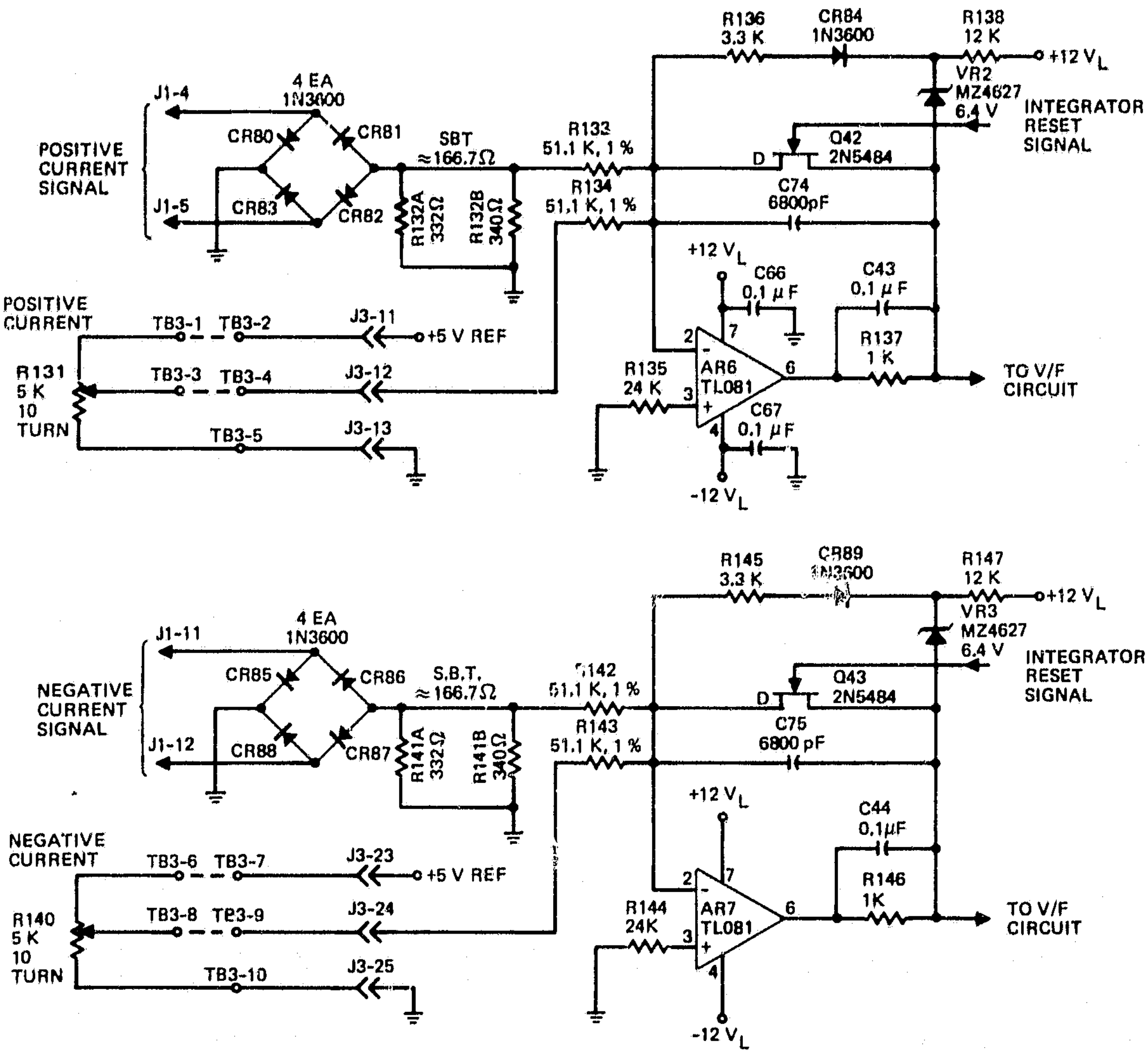

Figure 24. Positive and negative output-current control loops.

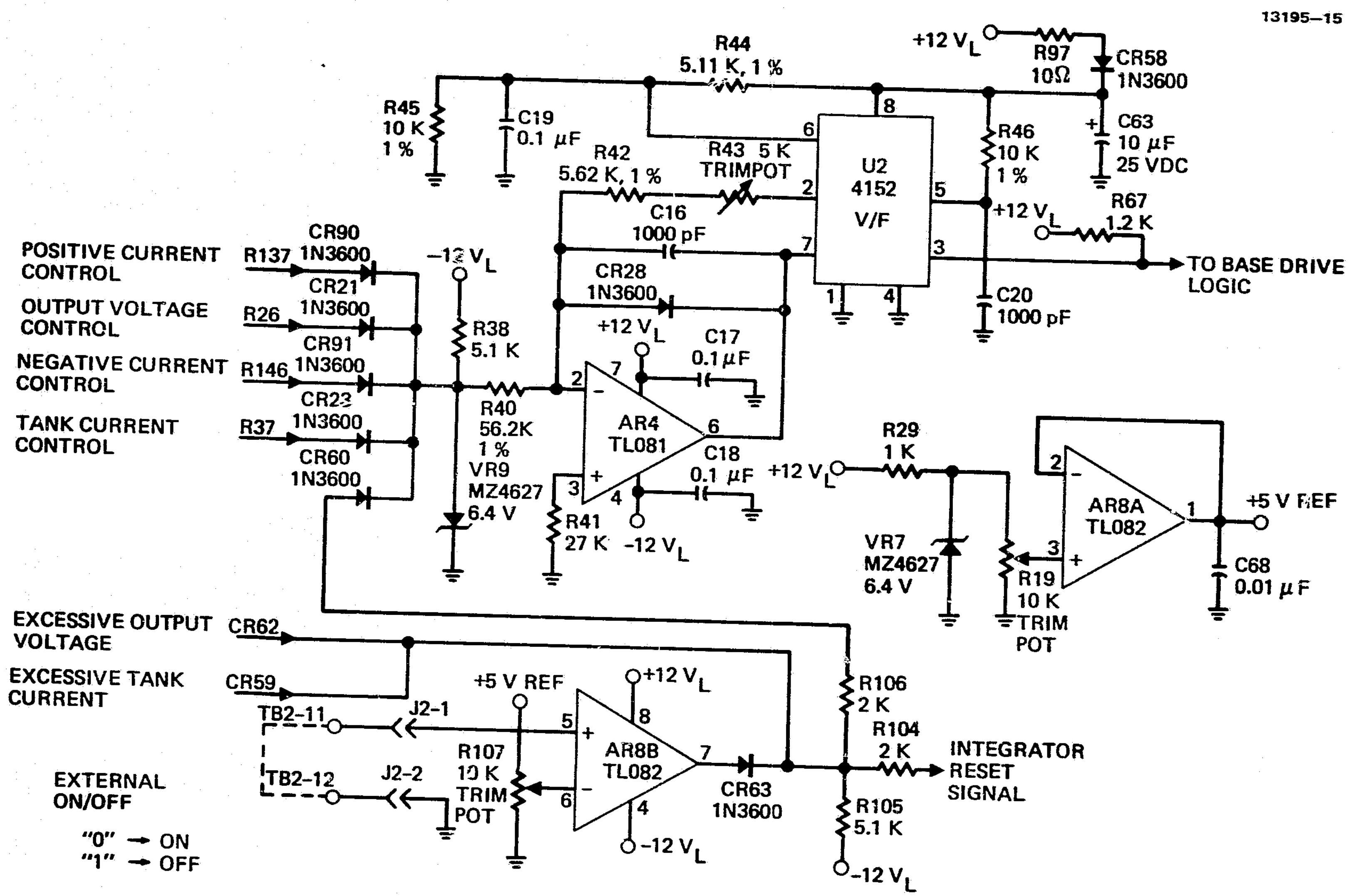

Figure 25. Voltage-to-frequency and integrator reset circuitry.

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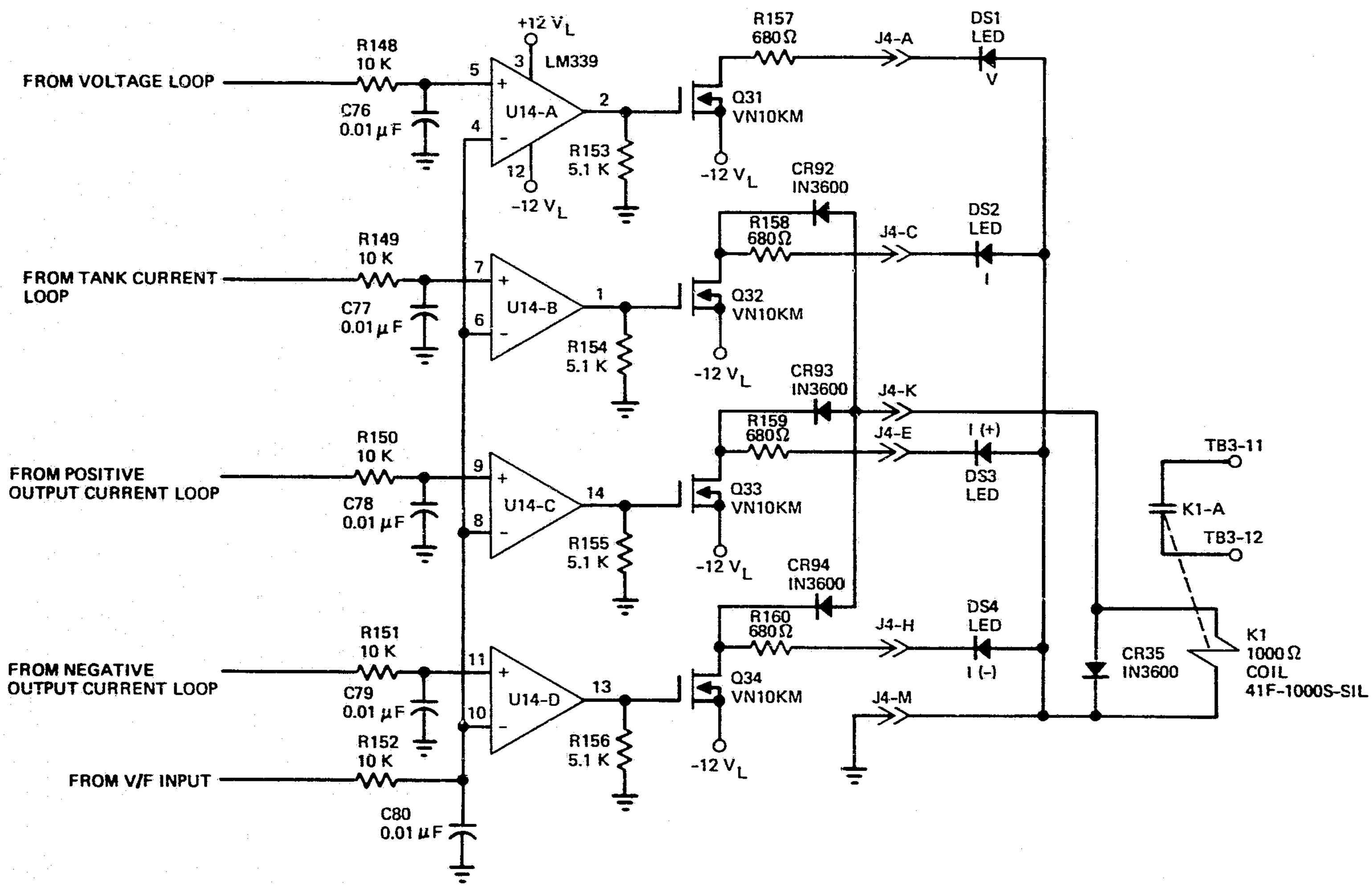

Figure 26. Controlling feedback loop indication circuitry.

looks at the outputs of the four control loops and compares them against the input to the V/F converter. The control loop which has control of the converter will provide a positive voltage to its comparator relative to the input of the V/F converter. The output of that comparator will then go positive, turning on the appropriate indicator lamp on the front panel. Any of the current-control-loop comparators will also activate relay K1 to provide an external signal that indicates the converter is in a current-limited mode.

6. Base-Drive Logic

The base-drive steering and protection logic is shown in Figure 27. The output pulses from the V/F converter provide the basic repetition rate at which the transistor switches in the bridge circuit are turned ON and OFF. The pulses from the V/F converter are negative logic AND'd, with the reverse base-bias signals by U11. This guarantees that all four transistor switches are OFF before trying to turn any of them ON. In reality this prevents turning Q1 and Q3 ON while Q2 and Q4 are ON, and vice-versa. The output of U11 negative-edge triggers U24, which is a monostable multivibrator with a 22-µs-wide output pulse. This 22-µs-wide pulse sets the ON time of the transistor switches before the turn-off pulse is applied. Due to storage time the transistor switches do not actually turn-off until they have been ON for 25 µs which is the period of a half-sinusoidal resonant-current pulse. R211, R212, C139, and CR101 guarantee proper operation of U24 for very narrow trigger pulses.

The output of U24 is used to toggle U3, a flip-flop, which alternately allows the output of U24 to be applied to the base-drive for Q1/Q3 or Q2/Q4 by way of the steering gates, U4A and U4C. The outputs of U4A and U4C are negative logic OR'd, with the output of U27 by U4B and U4D. U27 is a monostable multivibrator which is triggered if Q1 and Q2 or Q3 and Q4 are ON simultaneously. When U27 is triggered, all four bridge

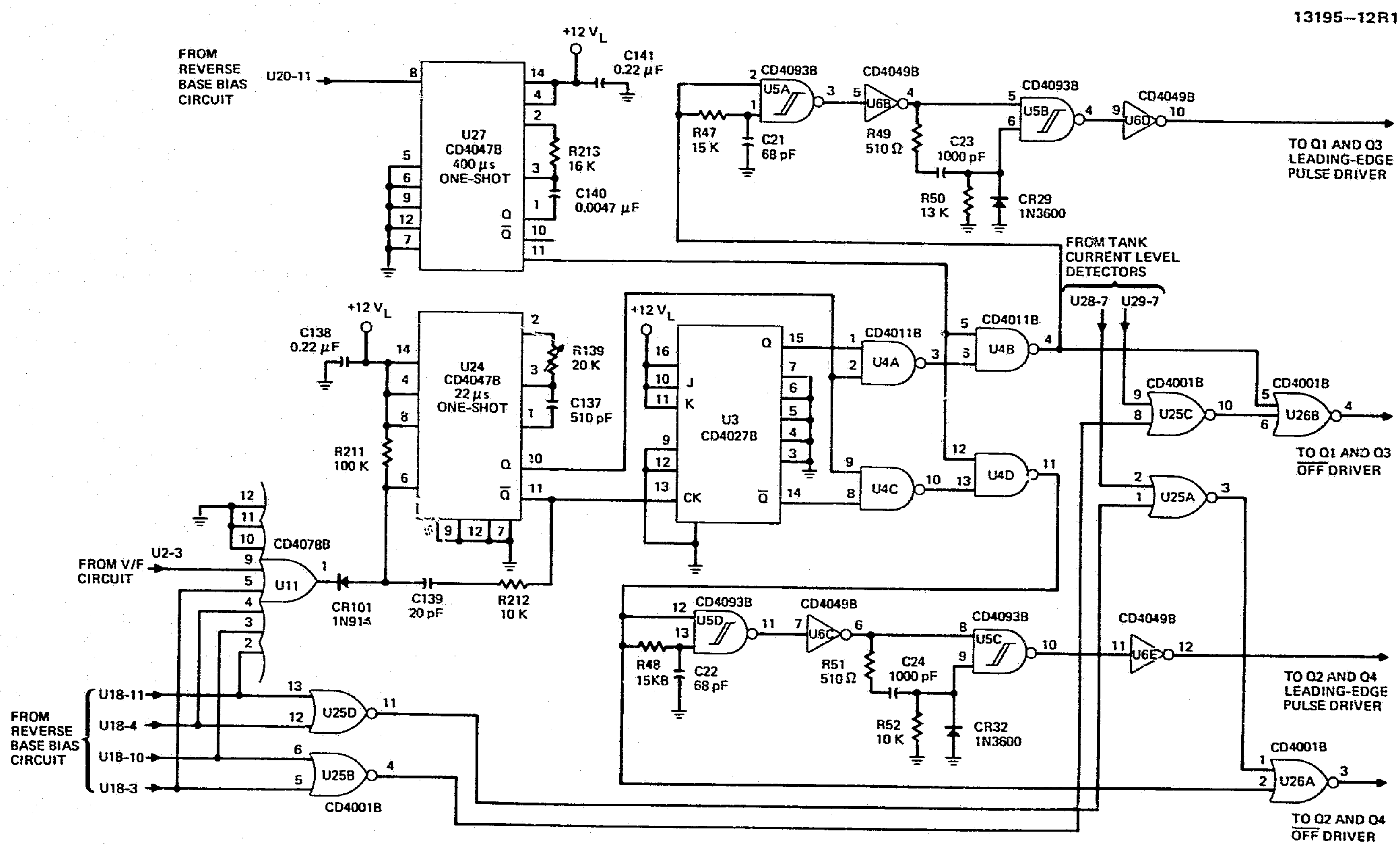

Figure 27. Base-drive steering and protection logic.

transistors are turned ON for 400 μs. The reason for doing this will be discussed later in this section.

The U4B and U4D outputs follow analogous paths; therefore, only the U4B output will be discussed. The output pulse from U4B follows two paths. First, it is applied to U26B which effectively turns Q9-1 and Q9-3 of the base-drive circuits OFF, permitting Q1 and Q3 of the bridge circuit to be turned ON. The trailing edge of the pulse from U4B turns Q9-1 and Q9-3 back ON, starting the turn-off of Q1 and Q3 unless prevented from doing so by U25C. U25C prevents turning Q1 and Q3 OFF until the tank current is below a level at which it is safe to do so (input from U29-7). This will be further discussed in Section 3.F.8 below. The input to U25C from U25B blanks the pulse from U29-7 that is associated with commutating diode conduction.

The output pulse from U4B is also delayed for approximately 1 μs by R47, C21 and U5A. This delay allows time for Q9-1 and Q9-3 to turn OFF and also provides a means of balancing both halves of the tank current, if necessary, by varying this time delay slightly. The delayed pulse is inverted by U6B and shortened by R49, R50, C23, CR29, and U5B to the width required for the leading-edge base-drive pulse (≈12 μs). This shortened pulse is then used to drive the gates of Q6-1 and Q6-3 of the base-drive circuitry by way of the base-drive-signal drivers.

7. <u>Reverse Base-Bias Logic</u>

The reverse base-bias logic is shown in Figure 28. The optical signals from U9-X of the base-drive circuits are received by the respective U10-X which provide 5-V signals. The 5-V signals are converted to 12-V signals by VR31 through VR34, R121 through R128, Q47 through Q50, and R161, R163, R165, and R167. The signals are delayed for ≈1 μs by R162, R164, R166, R168, C81 through C84, and U18A through U18D.

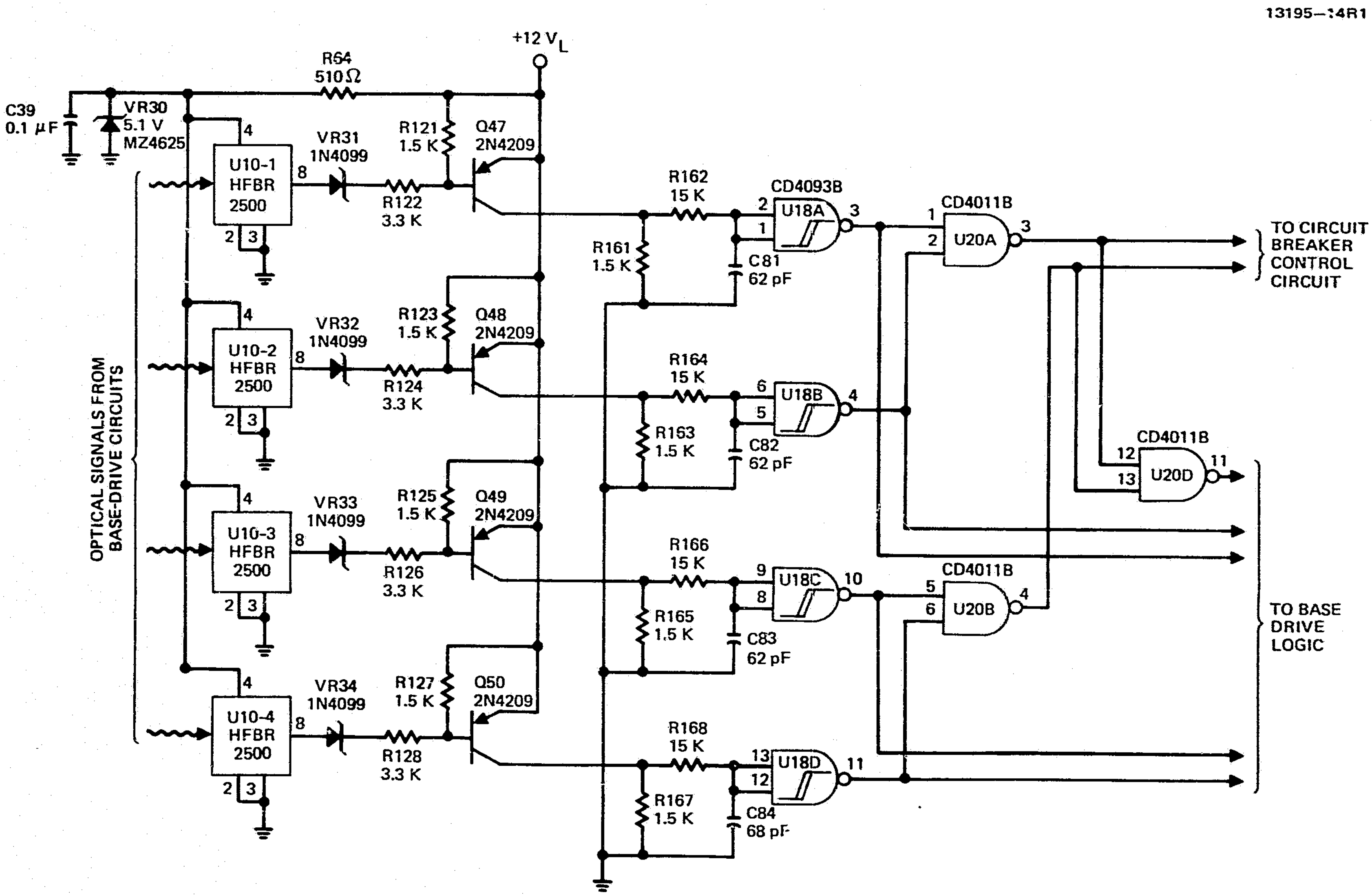

Figure 28. Reverse base-bias logic.

The signal at the output of U18 is a "0" if the respective transistor switch (Q1 through Q4 of the bridge) is reverse biased and a "1" if it is forward biased. The output of U20A is a "0" if Q1 and Q2 are forward biased at the same time and the output of U20B is a "0" if Q3 and Q4 are forward biased at the same time. These signals are used to trip the input circuit breaker under the above conditions and are also negative logic OR'd by U20D which triggers U27 of Figure 27. The outputs of U18A through U18D are also used by the base drive logic of Figure 27.

8. Tank-Current Level Detector

The tank-current level detection circuitry is shown in Figure 29. It basically consists of two comparators (one for positive tank current and one for negative tank current) which compare the tank current signal against a fixed reference. The outputs from these comparators prevent the base-drive logic from turning-off the D7ST transistors in the tank circuit until their collector currents are below a safe level. The safe level is determined by the reverse-biased safe-operating-area (SOA) of the D7ST transistors. However, reverse-biased SOA curves are not available for the D7ST and therefore this circuit was set by empirical data at 70A. No failures of the D7STs occurred at this value, but one failure did occur at 90A.

9. Signal Drivers

The base-drive-logic signal drivers shown in Figure 30 interface the base-drive logic of Figure 27 with the base-drive circuitry of Figure 14. The signal drivers provide current amplification of the signals and core reset for transformers T6-X of Figure 14.

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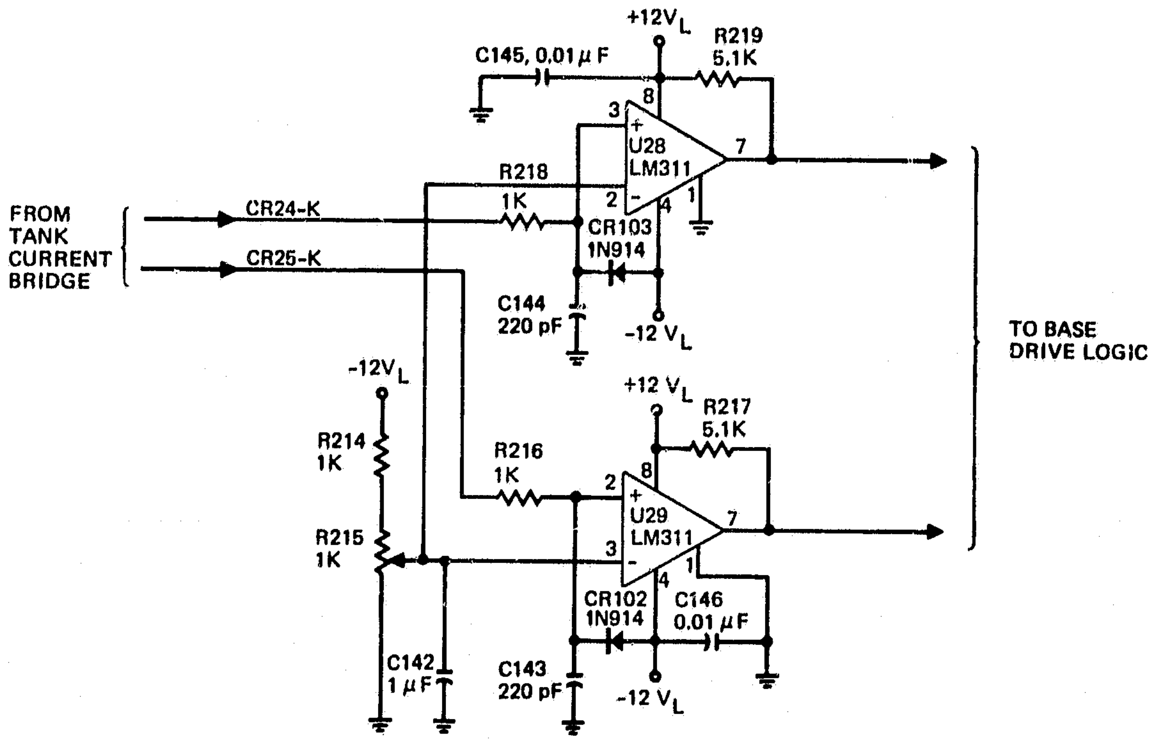

Figure 29. Tank-current level detection circuitry.

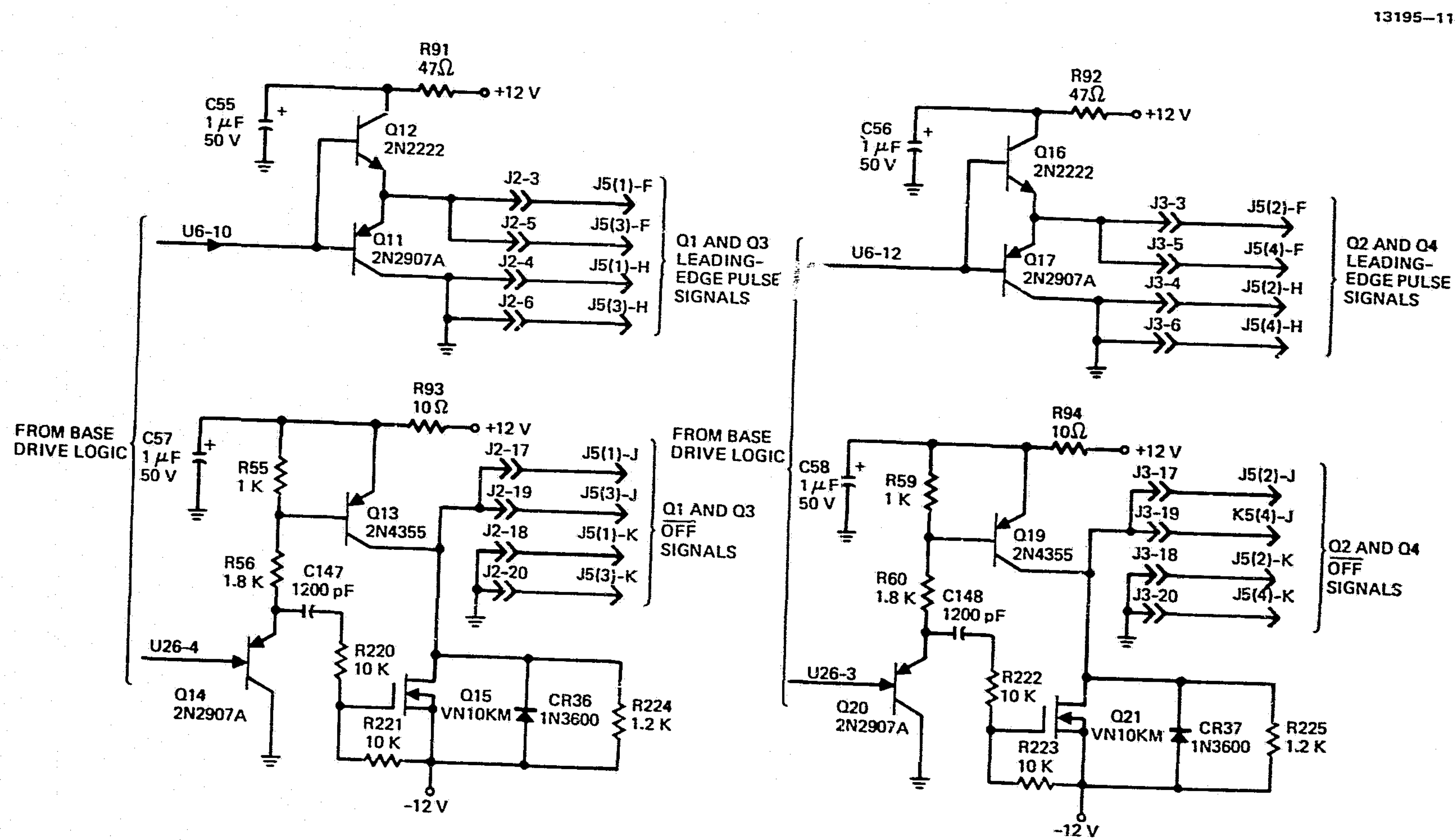

Figure 30. Base-drive-logic-signal drivers.

10. Protection Philosophy for the D7ST Switches

The protection philosophy for the D7ST switches that was embodied in the original design of this converter (and also the 10-kW converter developed under contract No. NAS 3-22471) was to turn all four of them OFF in the event of a malfunction. The ability to turn the transistor OFF was considered to be a distinct advantage over SCR switches, and is real enough, provided the transistor does not fail due to second breakdown.

A total of seven D7ST transistors failed during the development of this converter. The first three failed catastrophically (smoke and fire) with their bases, emitters, and collectors all shorted together. These three failed early in the development before the input circuit breaker was operating properly. The short between all three leads, however, made it impossible to determine the original failure mechanism. The other four D7STs failed quietly, and all exhibited collector-to-emitter shorts. The collector-to-emitter short suggests a second-breakdown failure, particularly since the base-drive circuit subjects the D7STs to reverse-bias during turn-off.

Transistors in general can absorb much more energy (>10 times) if they are forward biased than if they are reverse biased. Therefore, a better approach to protecting them during a malfunction is to turn them ON. Turning all four bridge transistors ON places a short on the input bus, and therefore the input circuit breaker must be opened quickly in order to isolate the input bus from the short. The input circuit breaker opens in less then 20 μs and the input filter provides the isolation during this time.

The base-drive logic and protection circuitry was modified to incorporate this new protection philosophy. U27 of Figure 27 turns all four bridge transistors ON if the reverse-base-bias circuitry senses that Q1 and Q2 and/or Q3 and Q4 are on simultaneously. U24 of Figure 27 guarantees that the base-drive logic doesn't try to turn the D7STs OFF before the end of the normal resonant half-cycle, and the tank-current level detectors of Figure 29 guarantee that the D7STs are within their reverse-biased safe-operating-area before they are turned OFF. No D7ST failures occurred after all of this circuitry was incorporated.

G. INPUT FILTER AND UNDERVOLTAGE CIRCUITRY

The input filter and undervoltage trip circuitry is shown in Figure 31. The filter is a two-stage LC filter comprised of L3, L4, C2, C31, and C32. L5 provides rolloff at high frequency and is the inductance of wirewound resistor R25. R25 provides damping of the natural resonance of the filter. Calculations predicted a peaking of 14% at 500 Hz and an attenuation of 99.3% at 20 kHz for this filter. A low power mock-up of this filter had a peaking of 14% at 500 Hz and an attenuation of 98.9% at 20 kHz. The actual filter of the converter, however, did not peak as the repetition rate of the tank circuit was varied from near-zero frequency to greater than 10 kHz. R25 was temporarily removed and the filter still did not peak. This lack of peaking may be the result of energy being drawn from the filter and then part of this energy being returned to the filter. This situation is a form of nonlinearity and may effectively provide damping of the filter.

The undervoltage circuit, comprised of R2, R3, VR27, VR28, Q5, U1, and C8, detects whether the bus voltage is above or below 50 V. The input circuit breaker is opened any time the voltage is below 50 V. The converter itself is not harmed by an undervoltage condition, but an undervoltage condition does indicate some form of malfunction. In particular, if the output of the filter does not increase above 50 V in 200 μs after the circuit breaker is closed, it can be assumed that a short on the output of the filter exists, and the circuit breaker is opened to prevent the input bus from reacting to the short.

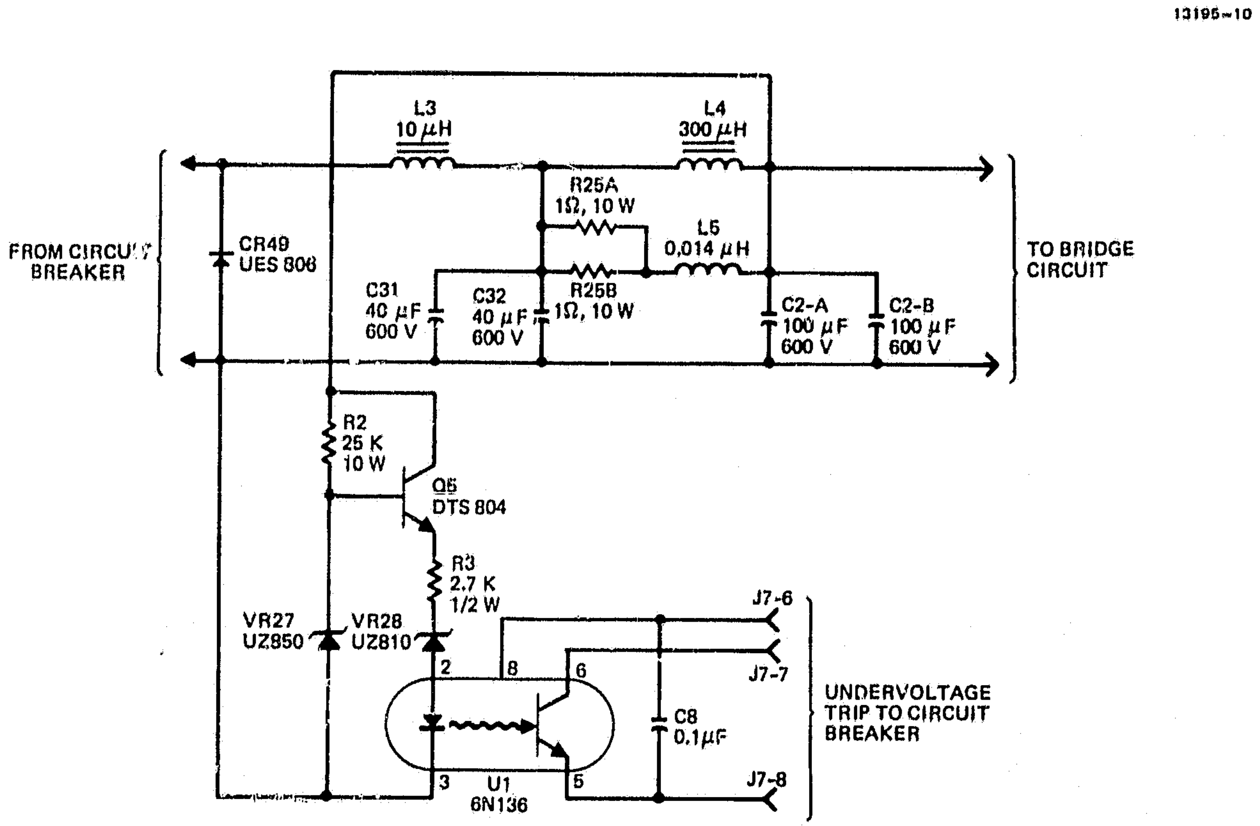

Figure 31. Input filter and undervoltage circuitry.

H. SOLID STATE INPUT CIRCUIT BREAKER

The main DC bus for the inverter is protected by a solid-state circuit breaker which is shown in Figure 32. The switch used in this circuit breaker is a D7ST transistor (Q23 of Figure 32) that is driven by a small, free-running inverter operating at 50 kHz. The inverter consists of U8, Q25 through Q30, T7, and associated components. The base-drive current to Q23 is maintained at a constant level by sensing the primary current of T7 with R83. The voltage across R83 is buffered by AR9 and compared against the reference voltage of R72. The output of AR9 varies the output pulse width of U8 which in turn keeps the current through R83 at a constant level. The circuit breaker is opened and closed by turning the inverter circuit OFF and ON by way of the shut-down input to U8. During opening of the circuit breaker, SCR Q22 is also triggered, which draws 70 A of reverse base current from Q23. This reduces the turn-OFF time of Q23 to 12 μs. Without the SCR, it takes 100 μs for Q23 to turn OFF.

R87, CR50, and C71 form a snubber to prevent dv/dt triggering of the SCR during closing of the circuit breaker. T13 provides a signal to trip the circuit breaker and prevent R88 from burning up if the SCR should false trigger while the circuit breaker is closed. CR41 prevents reverse biasing Q23 by more than 0.7 V where its reverse-biased safe-operating-area is close to its forward-biased safe-operating-area. CR44 and VR23 through VR26 provide transient protection for Q23, while C38 and C70 suppress voltage transients due to the inductance of the input bus and di/dt when the circuit breaker opens. This circuit breaker will switch 30-kW at an input voltage of 250 to 350 Vdc.

The control circuitry for the circuit breaker is shown in Figure 33. The circuit breaker can be tripped (or commanded to open) by five types of signals: the ON/OFF switch, undervoltage on the bus, bridge "latch-up" (Q1 and Q2 and/or Q3 and Q4 on

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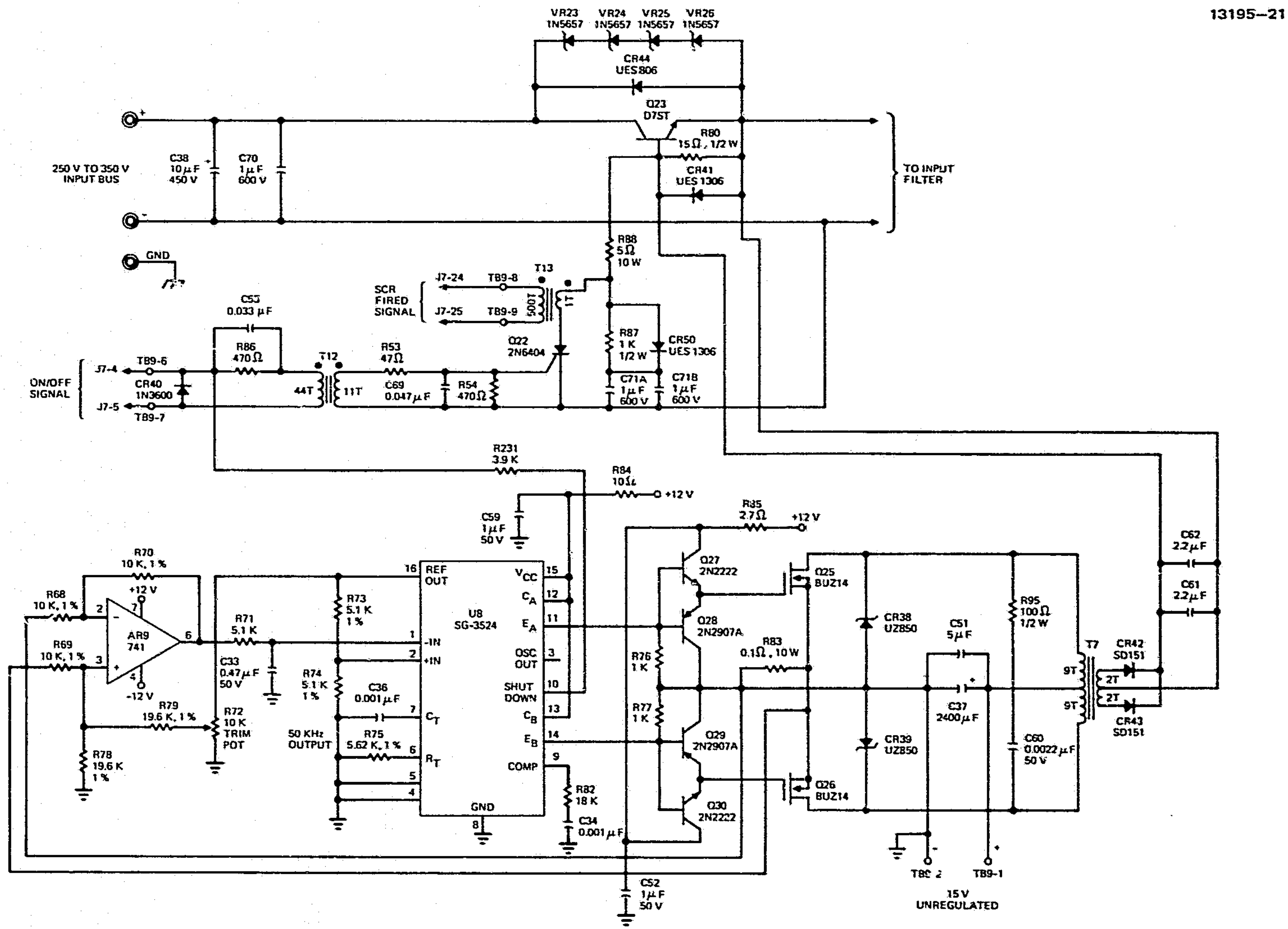

Figure 32. Solid-state input circuit breaker.

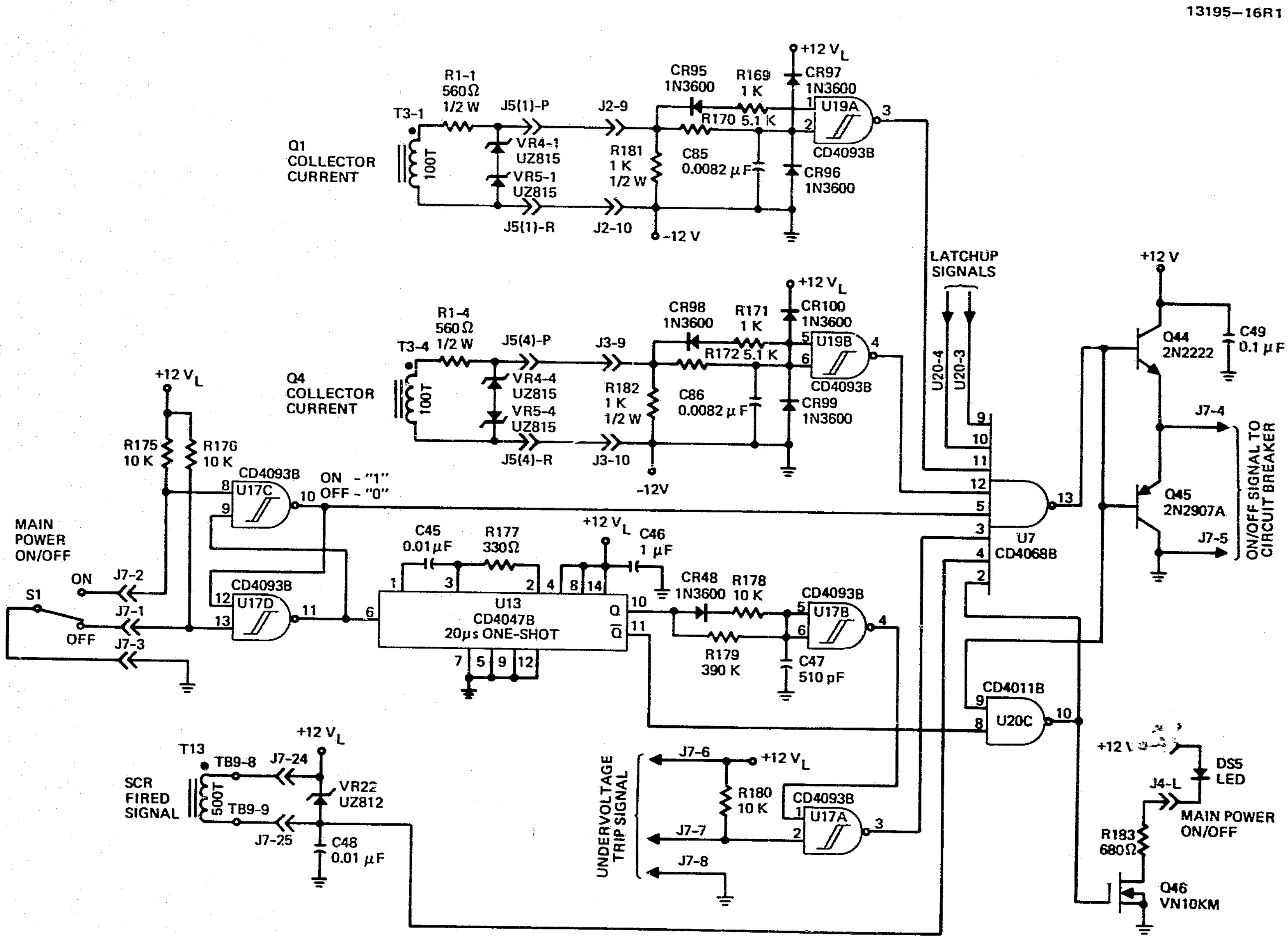

Figure 33. Circuit breaker control circuitry.

simultaneously), SCR (Q22) fired, and Q1 or Q4 collector current for longer than 50 μs.

The circuit breaker is controlled by the flip-flop composed of U7 and U20C. The output of U7 is buffered by Q44 and Q45 which then actually controls the circuit breaker. The flip-flop is set by the input to Pin 8 of U20C and tripped by the inputs to U7.

The ON/OFF switch (S1) is debounced by U17C and U17D. The output of U17C is used directly to trip the flip-flop when S1 is turned OFF. When S1 is turned ON, the output of U17D triggers a 20-μs one-shot (U13) to provide a pulse to set the flip-flop. The output of U13 also triggers a one-shot composed of CR48, R178, R179, C47, and U17B. The output of U17B disables the undervoltage trip signal for ~200 μs by way of U17A. The undervoltage trip signal would hold the flip-flop in a tripped condition if not disabled until the voltage at the output of the input filter rises to greater than 50 V. Trip signals for "latch-up" are provided directly by the reverse-base-bias circuitry of Figure 28.

The collector current of Q1 and Q4 should be a pulse of 25-μs duration. If collector current flows for more than 25 μs, then a malfunction of some form has occurred. Collector current in Q1 and Q4 is sensed by auxiliary windings of T3-1 and T3-4, respectively. If one or both of these signals is present for 50 μs or longer, the output of U19A or U19B will transition to a "0" and trip the flip-flop. These five types of trip signals protect the converter from malfunctions of the control circuitry and also protect the input bus in case of catastrophic failure of the converter.

I. NEGATIVE BIAS SUPPLY

Each of the base-drive circuits requires an isolated negative 8 V for use as the negative bias during the time that the transistors switches (Q1 through Q4 of Figure 3) are OFF. The output-transient-current limiter transistors (Q35 through

Q38 of Figure 17) also require isolated base-drive power. These negative-bias and base-drive voltages are supplied by the free-running-inverter outputs of Figure 34. The SG-3524 pulse-width-modulator (U30) operates at a fixed output-pulse width since the +12-V power is regulated. Q51 through Q54 buffer the output of U30 and drive the inverter switches (Q55 and Q56).

J. HOUSEKEEPING POWER

A schematic of the housekeeping power is shown in Figure 35, where 115-Vac, 60-Hz power is fused by F1, interlocked by J6-P and J6-R, and controlled by a front panel switch (S3). This 115-Vac power operates the blowers (B1 through B5) and the front-panel meter power supplies (PS1, PS2, and PS3). The 115-Vac power is also converted to unregulated dc by way of T14, T15, T16, CR51, CR56, CR57, CR72, CR73, CR76, CR77, C97, C123, C129, C130 and C133. The unregulated dc is regulated by standard linear series-pass regulator techniques (Q24, Q57, Q59, and U22). The regulators provide the +12-V, -12-V, and +45-V dc power required by the converter. C25 through C30, C50, R65, and R66 provide additional filtering and isolation for the control and logic circuits.

K. MECHANICAL

The 25-kW converter was designed to be used in a laboratory type environment with forced air as the cooling medium. It is self contained in a rack-mountable chassis that is 48.25-cm W x 62.25-cm H x 61-cm D (19-in. x 24.5-in. x 24-in.). It weights 135.6 kg (299 lbs), and has lifting-eyes on the top.

Figures 36 through 41 are various views of the converter with component locations called out on the photographs. The mechanical layout is designed to keep the lead lengths (and hence, the stray inductance) of the bridge circuitry to a minimum and is also modularized for ease of maintenance. One of the

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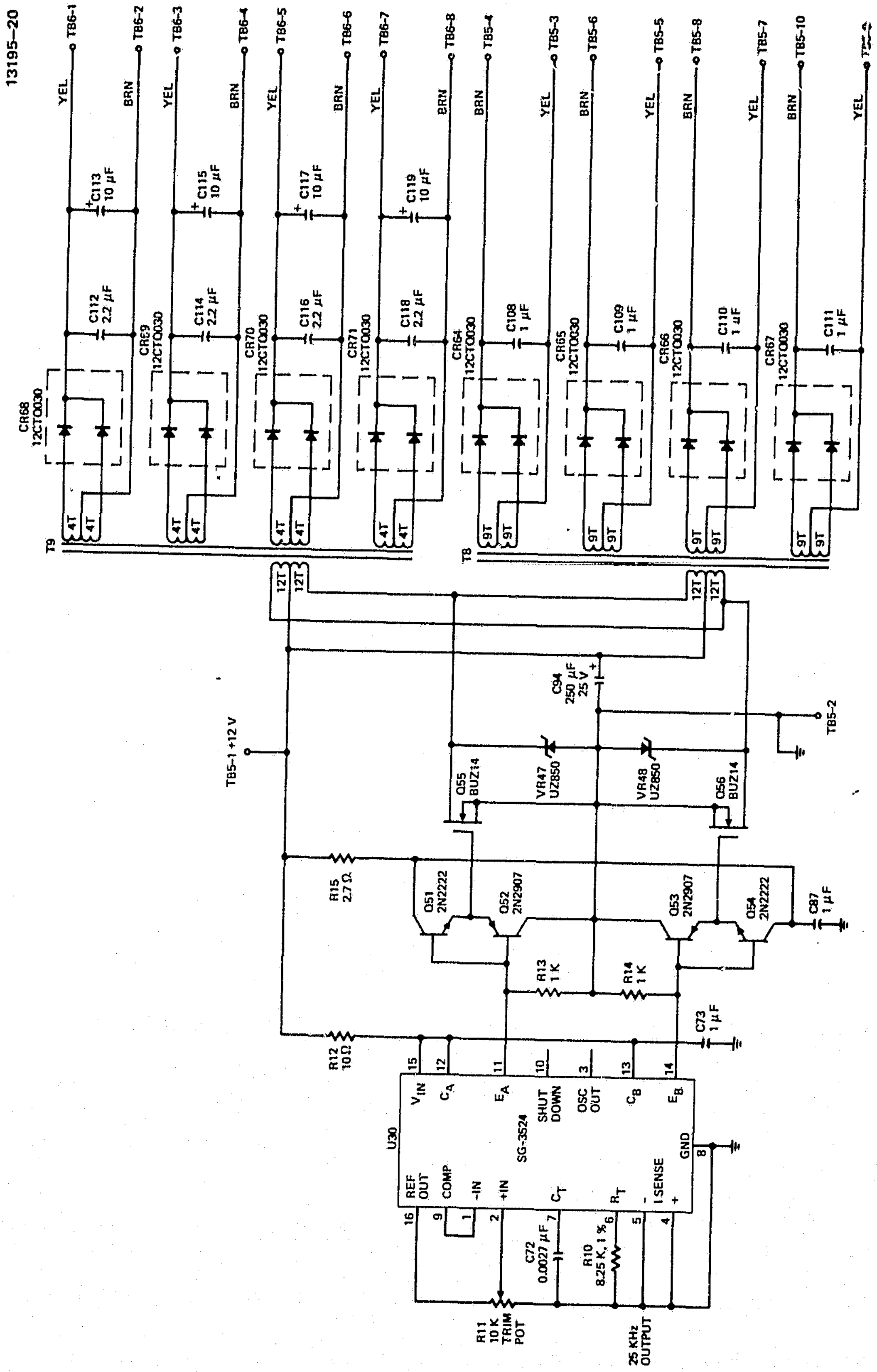

Figure 34. Negative bias supply schematic.

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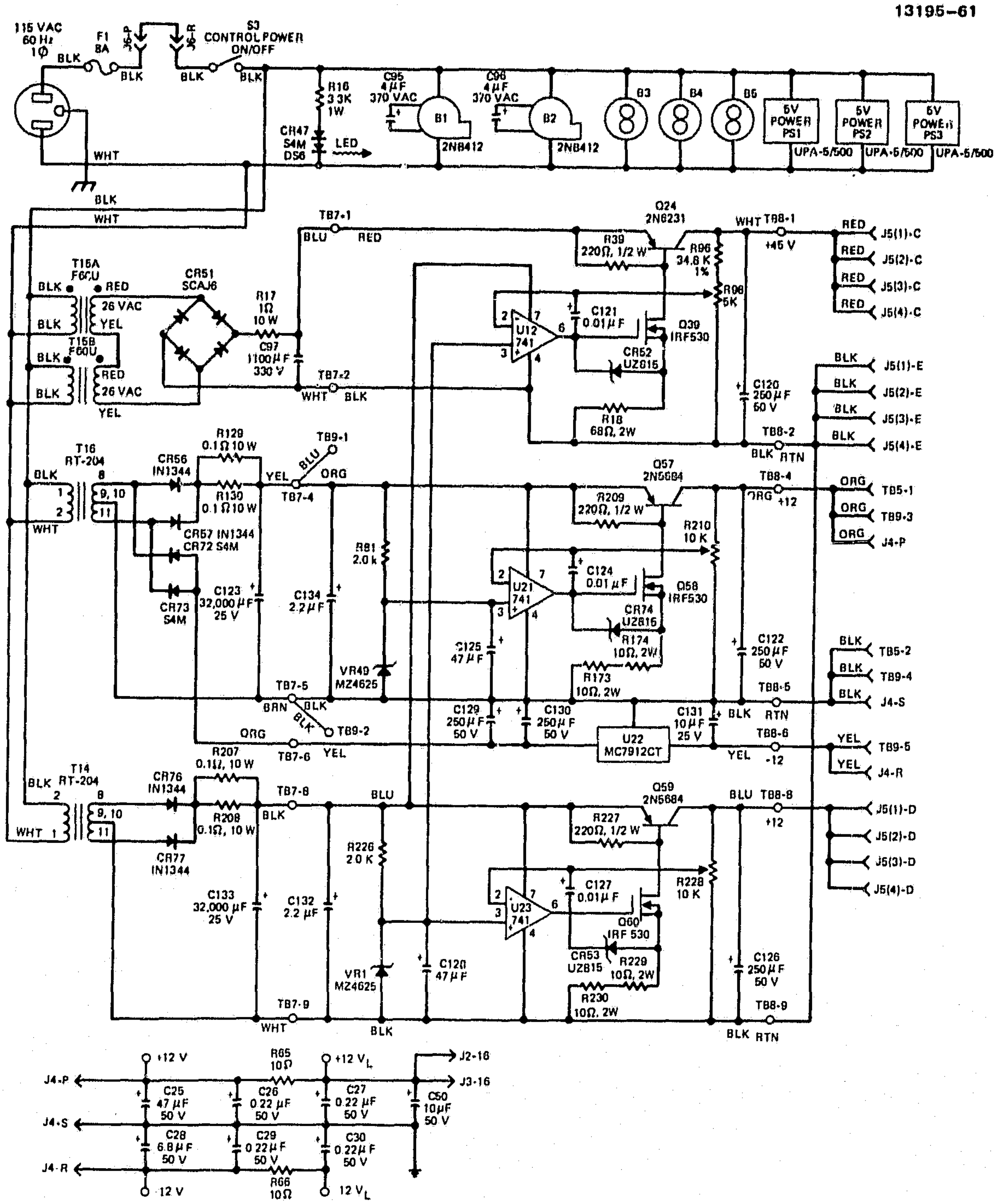

Figure 35. Housekeeping power schematic.

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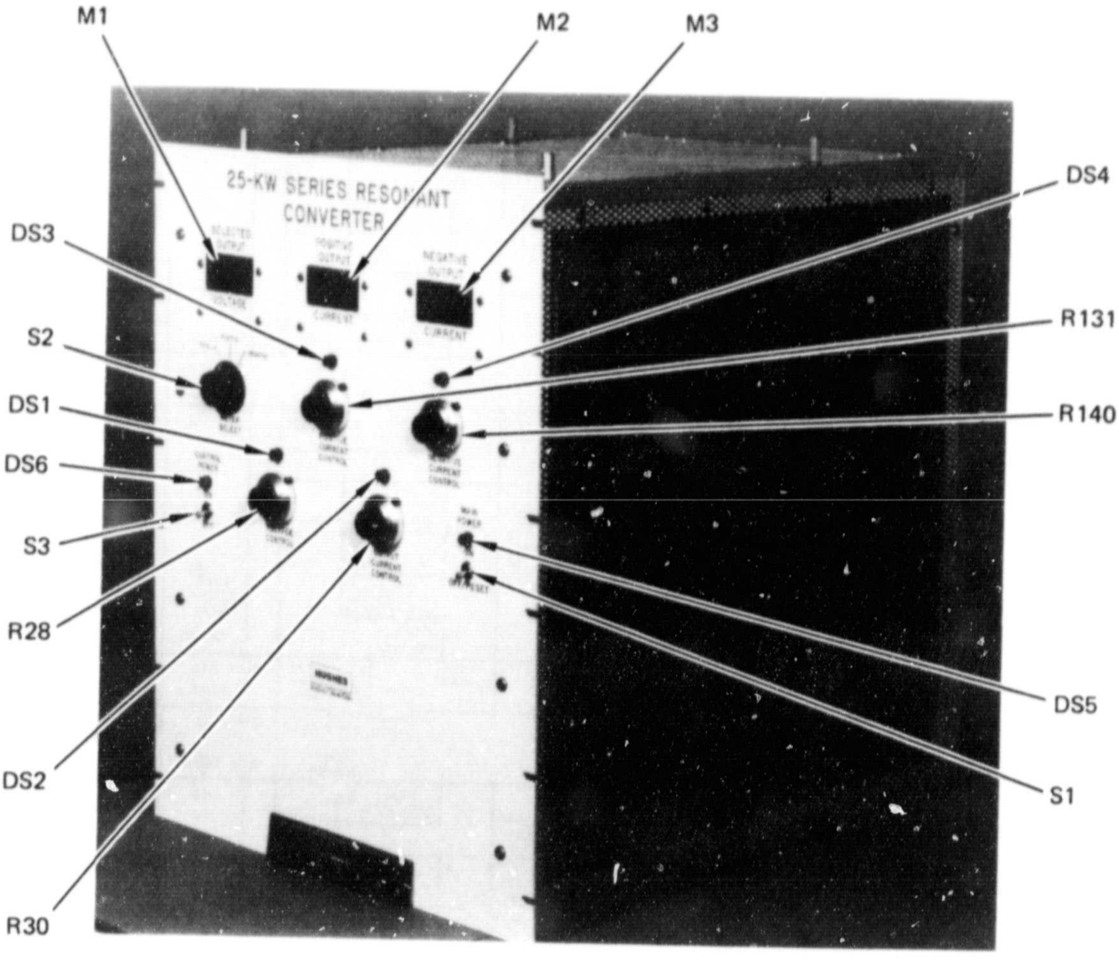

FRONT VIEW

Figure 36. Front view of the converter.

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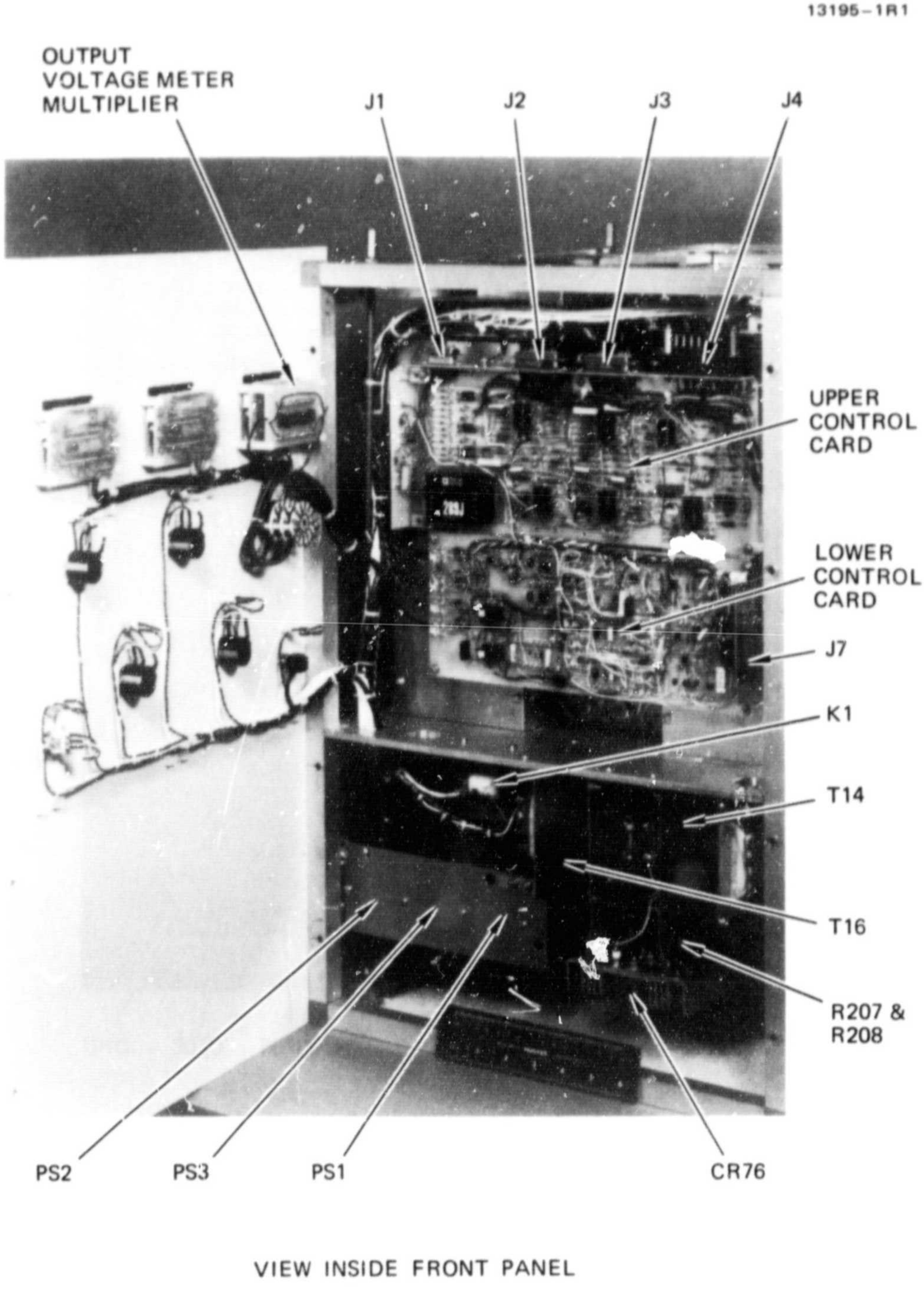

Figure 37. View inside the front panel of the converter.

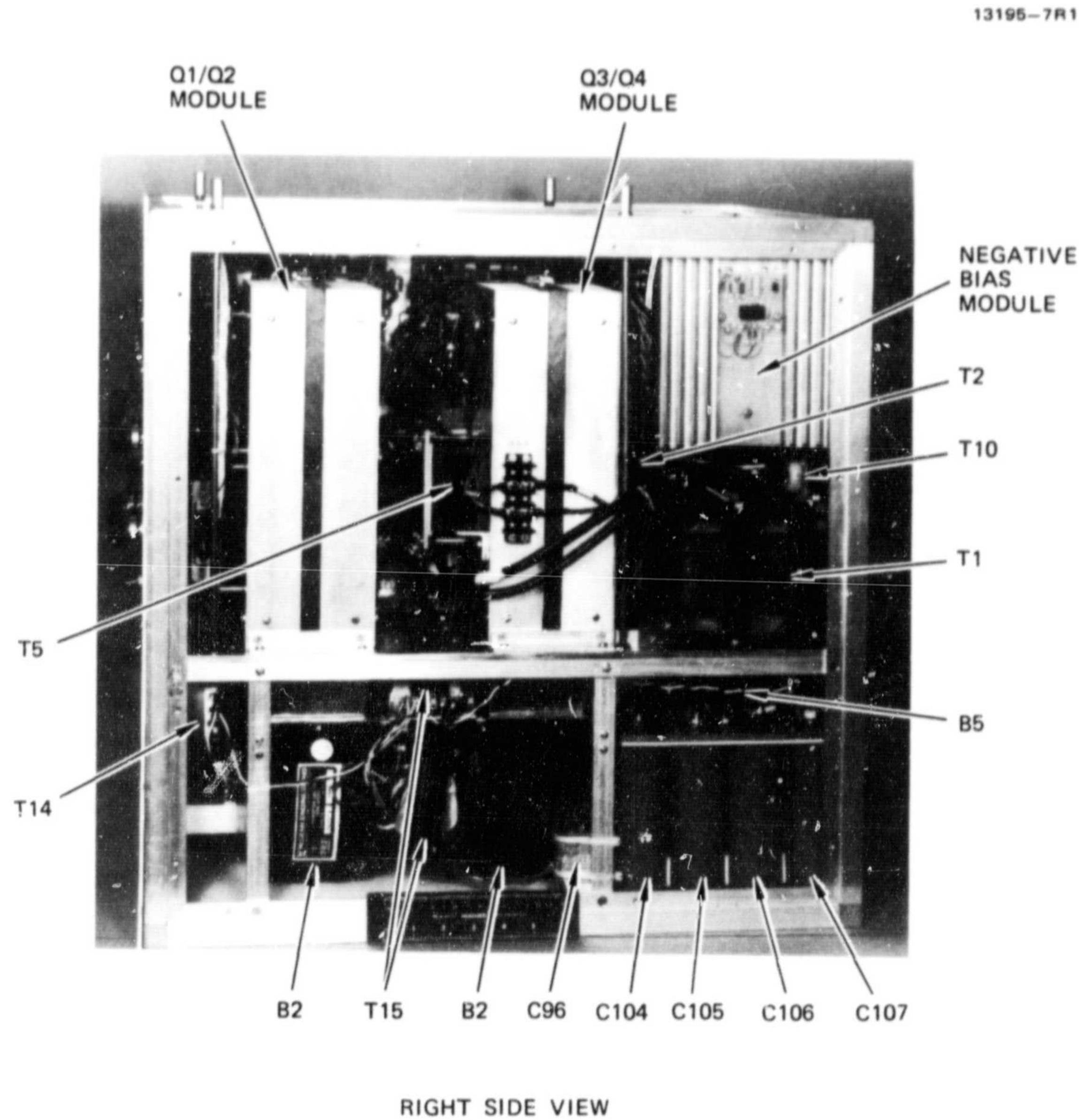

Figure 38. Right side view of the converter.

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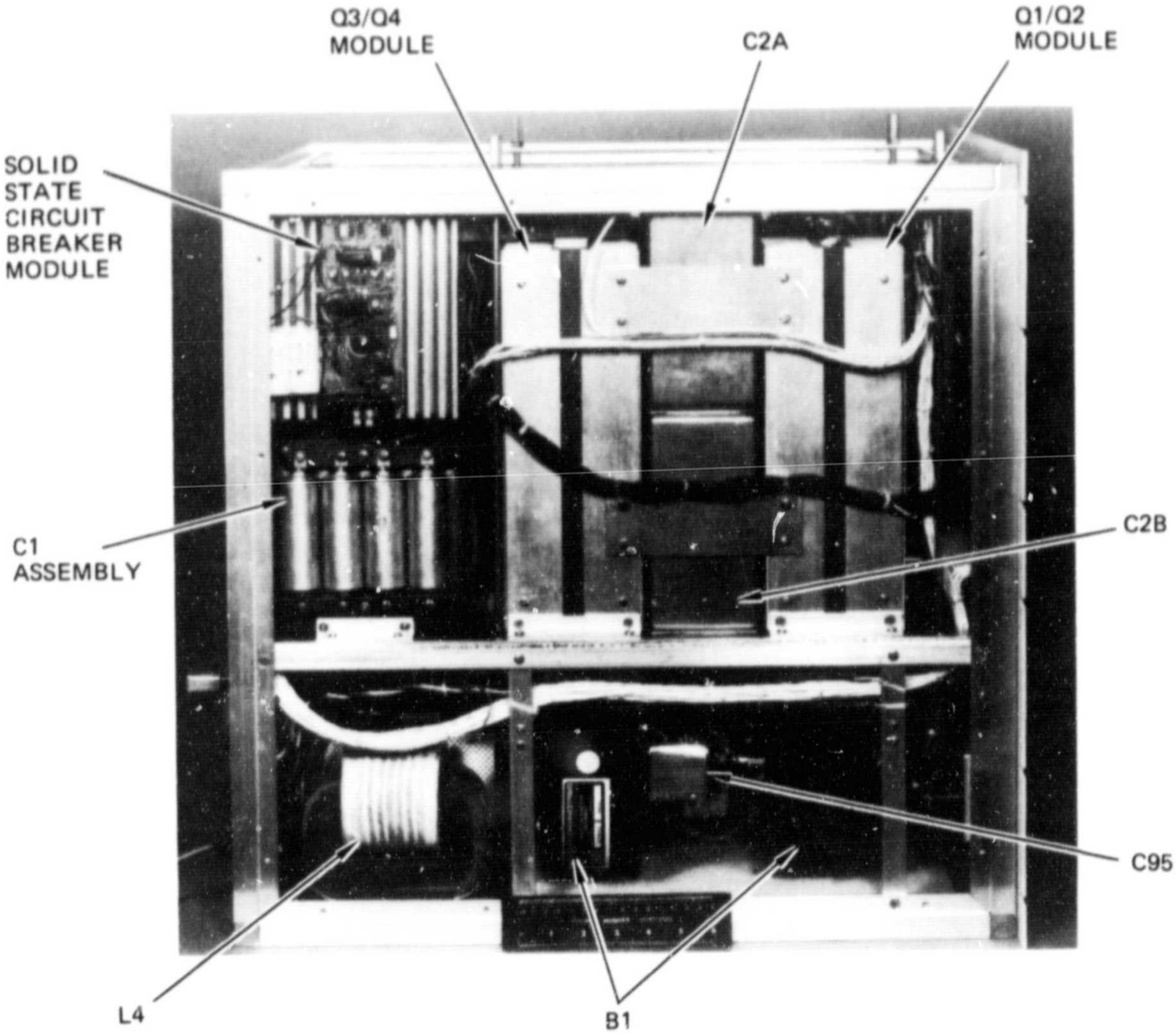

LEFTSIDE VIEW

Figure 39. Left side view of the converter.

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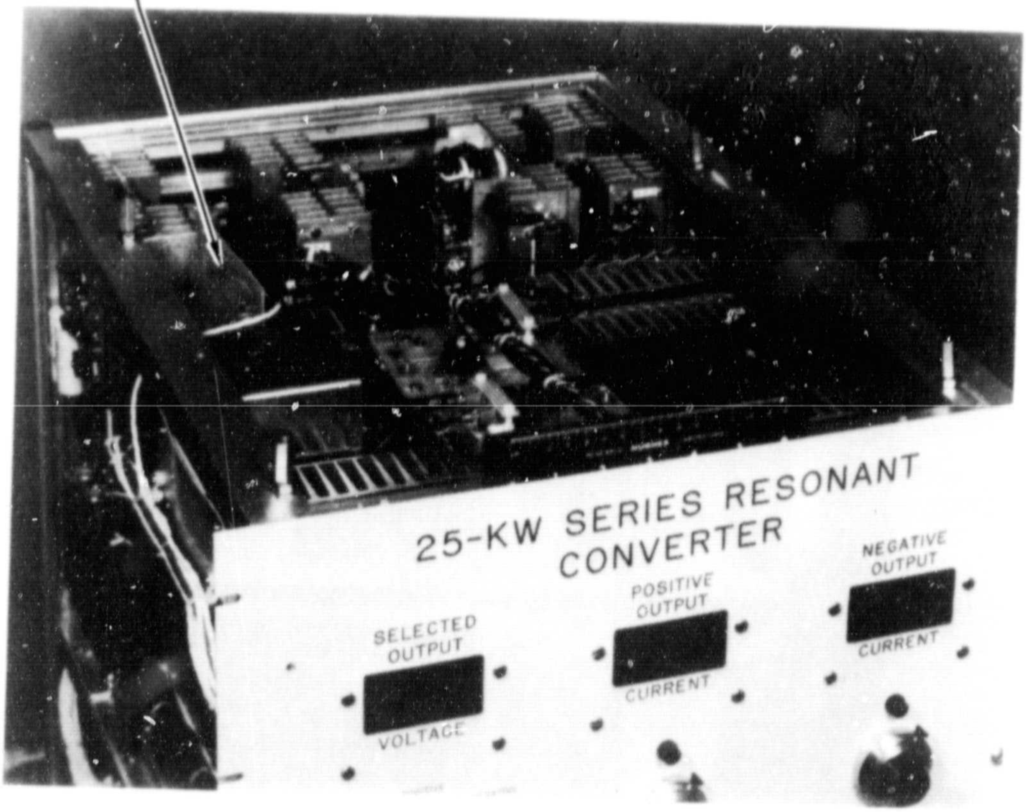
INPUT
UNDERVOLTAGE
TRIP CIRCUIT



TOP VIEW

Figure 40. Top view of the converter.

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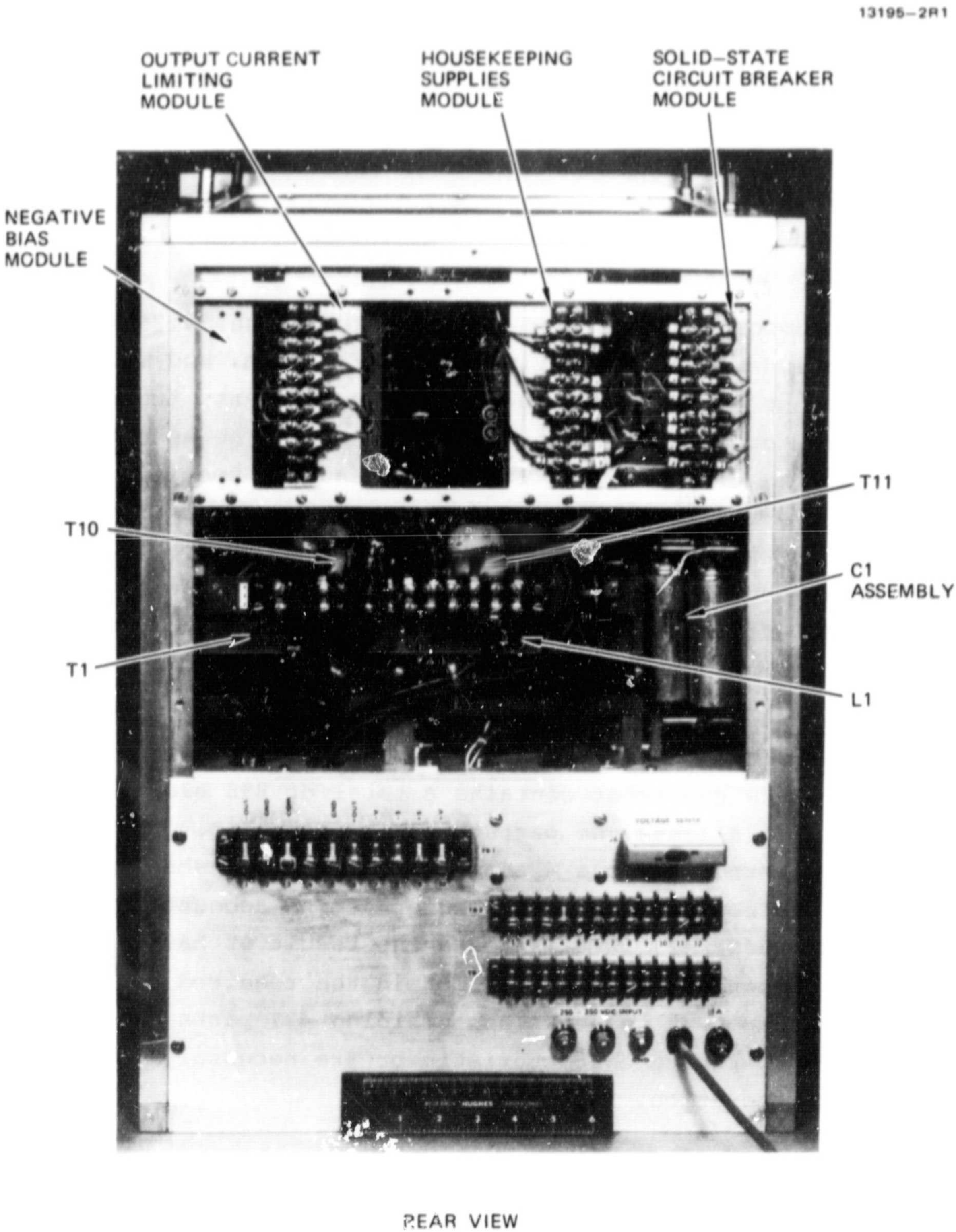

Figure 41. Rear view of the converter.

main heatsink modules (Q1/Q2) is shown in Figure 42. It consists of a 1.6-cm (0.625-in.)-thick copper plate with four aluminum heatsink extrusions bolted to it. Half of the bridge components (Q1/Q2 half) are mounted to this heatsink, along with the base-drive circuits for Q1 and Q2. The assembled module weights 28.1 kg (62 lbs).

L. WEIGHT BREAKDOWN

The components of the 25-kW converter weigh 54.28 kg. This weight includes harnesss, printed circuit cards, and mounting hardware, but does not include heatsinks, blowers, front panel components, or unregulated-power components. The specific weight of the components is 2.17 kg/kW and the specific weight of the converter as delivered is 5.42 kg/kW. For a flight type packaging design, with a packaging factor of 1.7 to 2.0, the converter should have a specific weight in the range of 3.7 to 4.3 kg/kW. Table 3 lists the weights for various components or groups of components.

M. PARTS COUNT

The 25-kW converter contains a total of 858 electrical parts. Table 4 lists the parts count by function. The first 13 functions listed in Table 4 are considered to be absolutely necessary to construct a 25-kW converter and account for 421 parts. Of these 421 parts, 46 are the result of having to parallel components in order to obtain the required current rating or component value. The remaining 437 parts enhance the converters operating characteristic or are necessary for laboratory operation.

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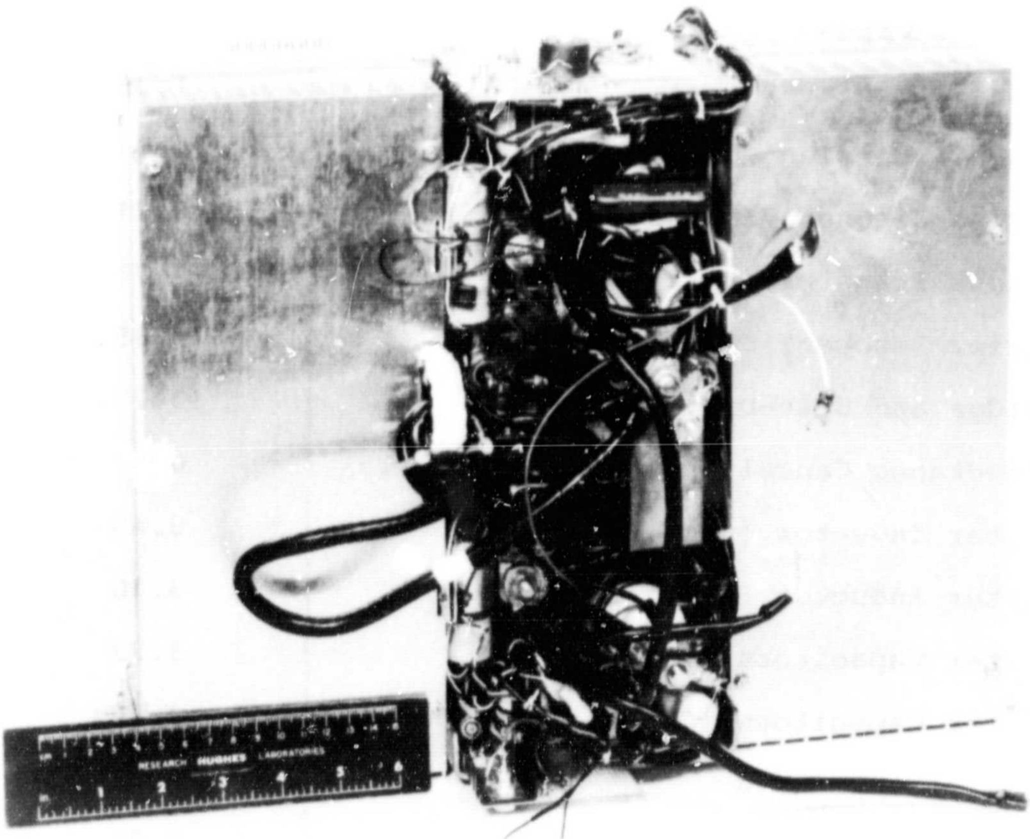

Figure 42. Q1/Q2 heatsink module.

Table 3. Weights of Various Components or Groups of Components

Component or Group	Weight, kg
Negative Bias Supply	0.52
Control Cards	0.71
Input Circuit Breaker	1.36
Output-Transient-Current Limiters	1.01
Series Resonant Inductor (L1)	6.21
Output Transformer (T1)	7.71
Series Resonant Capacitor (C1)	2.35
Bridge and Base-Drive	13.27
Inductance Cancelling Transformer (T5)	0.62
Filter Inductor (L3)	0.43
Filter Inductor (L4)	5.10
Filter Capacitors (C31 and C32)	3.23
Filter Capacitors (C2A and C2B)	3.45
Undervoltage Card	0.09
Output Rectifiers	0.21
Output Capacitors (C100 through C107)	6.69
Harness	0.99
Housekeeping Power Regulators	0.33
TOTAL	54.28

Table 4. Parts Count by Function for the 25-kW Converter

Function		Parts Count
Input Filter		9
Base Drive		120
Bridge and Tank		57
Output Circuit		16
Negative Bias Supply		28
Voltage Control Loop		41
Tank Current Control Loop		31
Current Cutback		14
+5V Reference		5
V/F Converter		21
Base-Drive Interface Circuits		32
Light Load Protection		15
Base-Drive Timing and Logic		32
	SUBTOTAL	421
Reverse Base Bias Sensing		59
Input Circuit Breaker		87
Output Transient-Current Limiters		53
Undervoltage Trip		7
Output Current Loops		44
Voltmeter		14
Current Meters		6
External ON/OFF		2
D7ST On Time Detection		21
Remote Current Mode and Control Loop Indicators		32
Housekeeping Supplies		75
Cooling		7
Connectors and Terminal Boards		30
	TOTAL	858

SECTION 4

TESTING

The 25-kW converter that was designed, developed, and fabricated under this contract was also tested under a variety of conditions to determine its operational characteristics. Testing was conducted for stability, steady-state waveforms, output ripple, input current ripple, regulation, transient waveforms, and efficiency. The test results for each of these parameters are discussed in the following sections.

A. STABILITY

The voltage and the current control loops all have integrators in their forward loops to provide very high dc gain, necessary for good regulation. In addition to the integrator, the voltage-control loop has a lead-lag network on the input of its integrator for loop compensation. The Bode plots for this loop for a variety of output conditions are shown in Figures 43 and 44. These figures show the bandwidth increasing and the stability decreasing as either the output voltage increases or the load resistance decreases. The worst-case gain margin is 10 dB, and the worst-case phase margin is 45°.

The current control loops do not have any compensation in addition to their integrators. The Bode plots for the tank current loop for a variety of conditions are shown in Figures 45 and 46. The bandwidth and the stability of this loop are similar to the voltage loop for the conditions tested, with a worst-case gain margin of 6 dB and a worst-case phase margin of 65°.

The positive output current loop and the negative output current loop are identical to the tank current loop except that they are 4-dB lower in gain.

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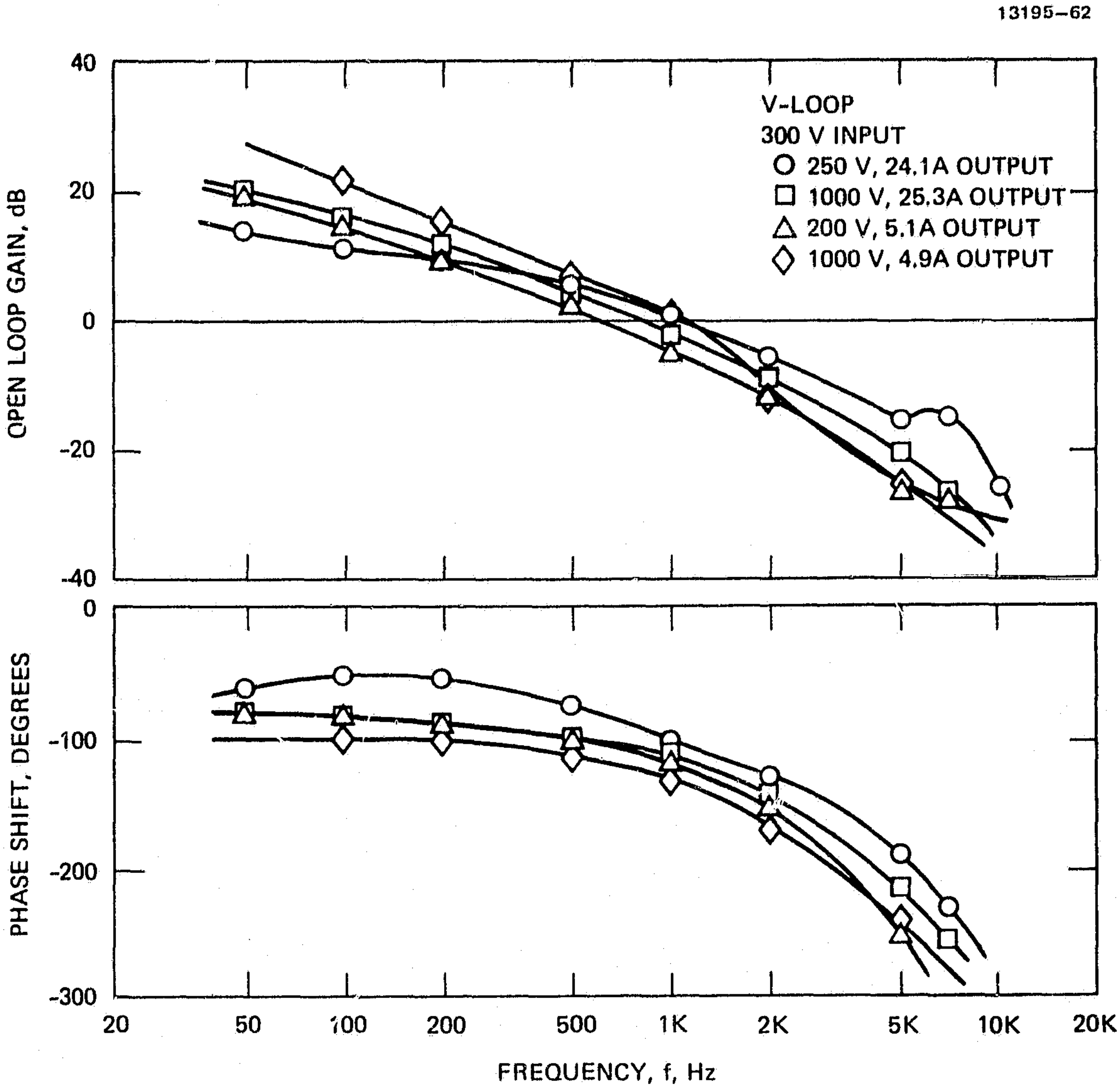

Figure 43. Bode plots of the voltage-control loop for various output conditions and a 300-V input.

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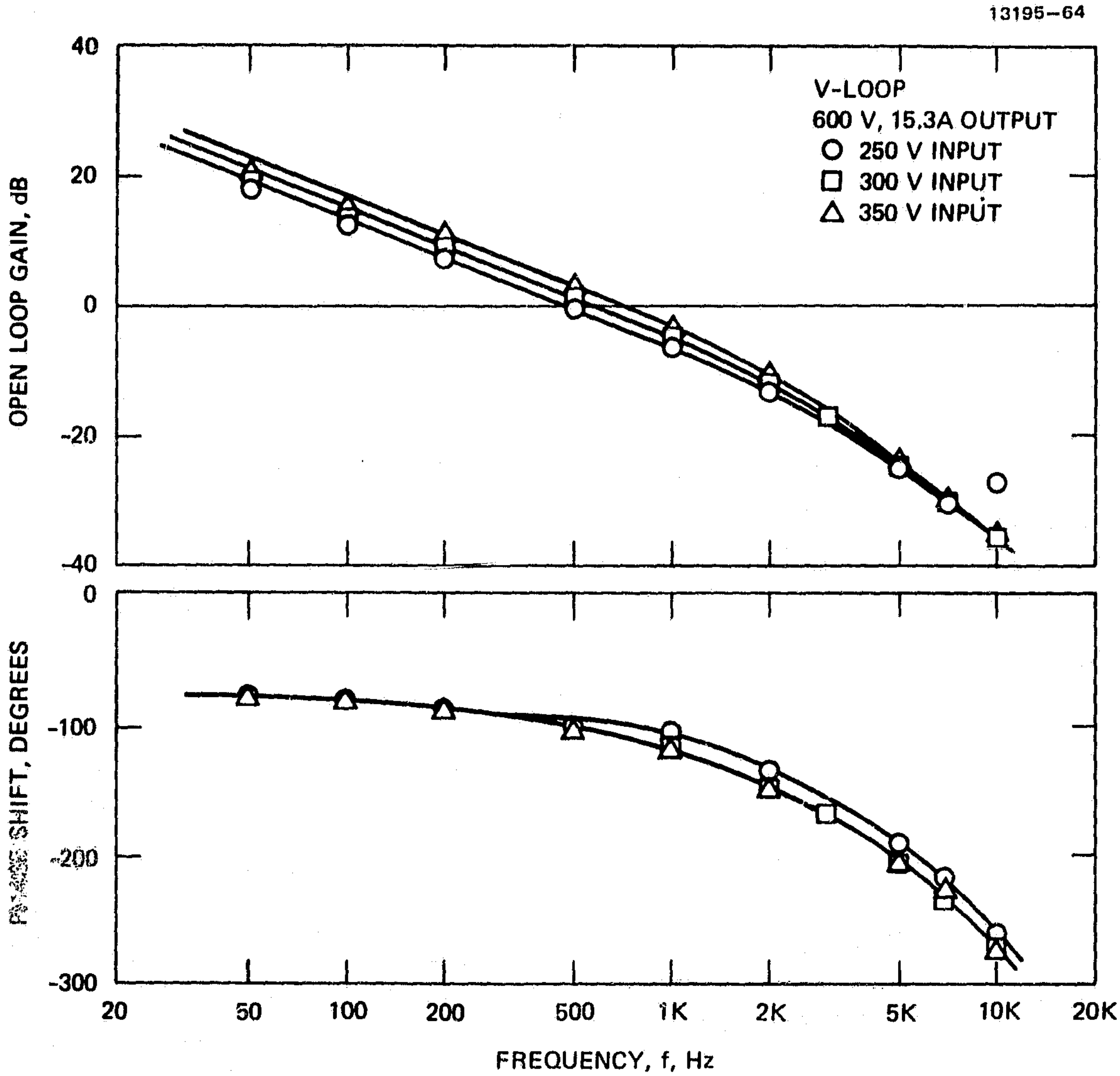

Figure 44. Bode plots of the voltage-control loop for various input voltages and a 600-V/15.3-A output.

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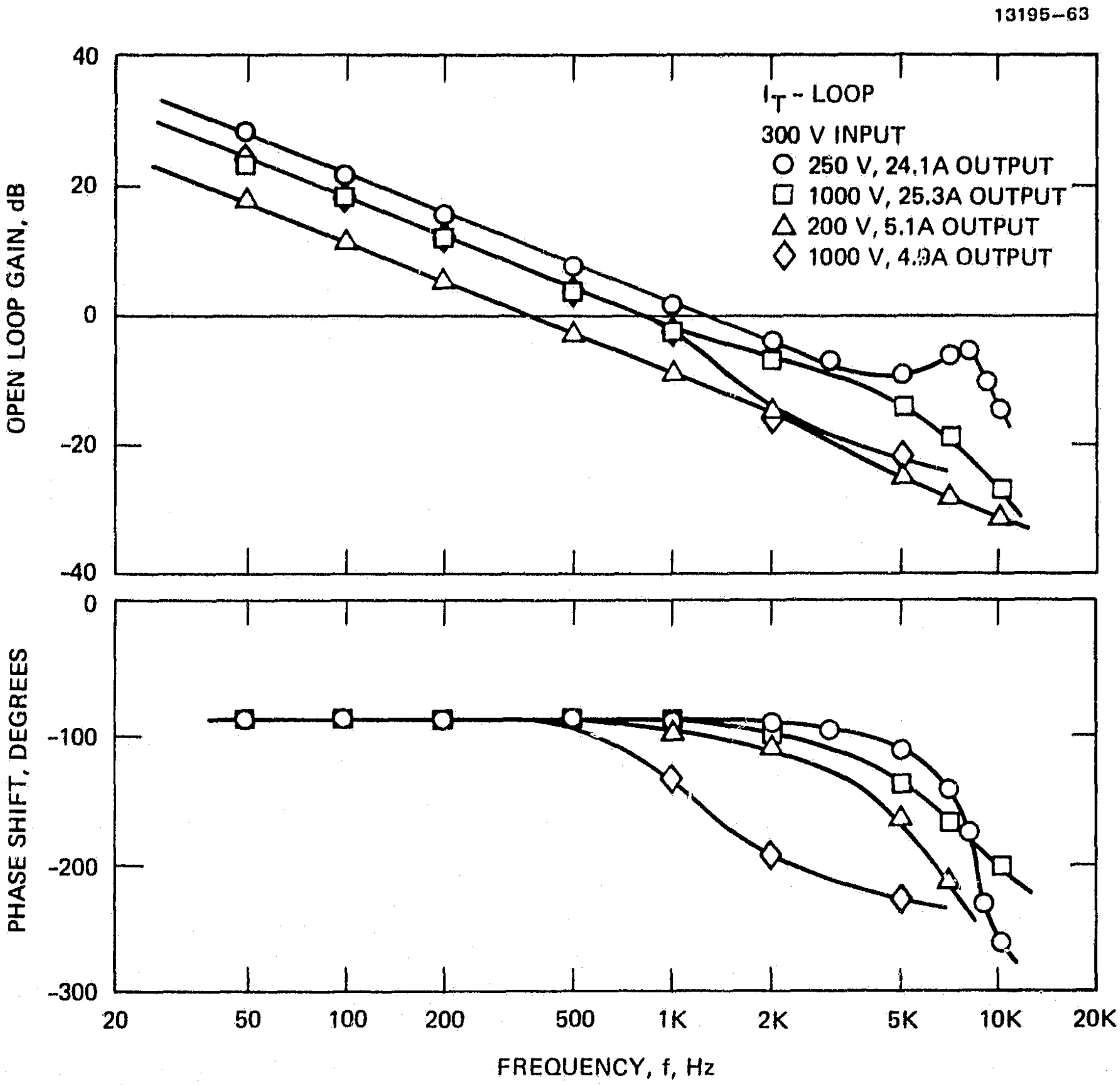

Figure 45. Bode plots of the tank-current control loop for various output conditions and a 300-V input.

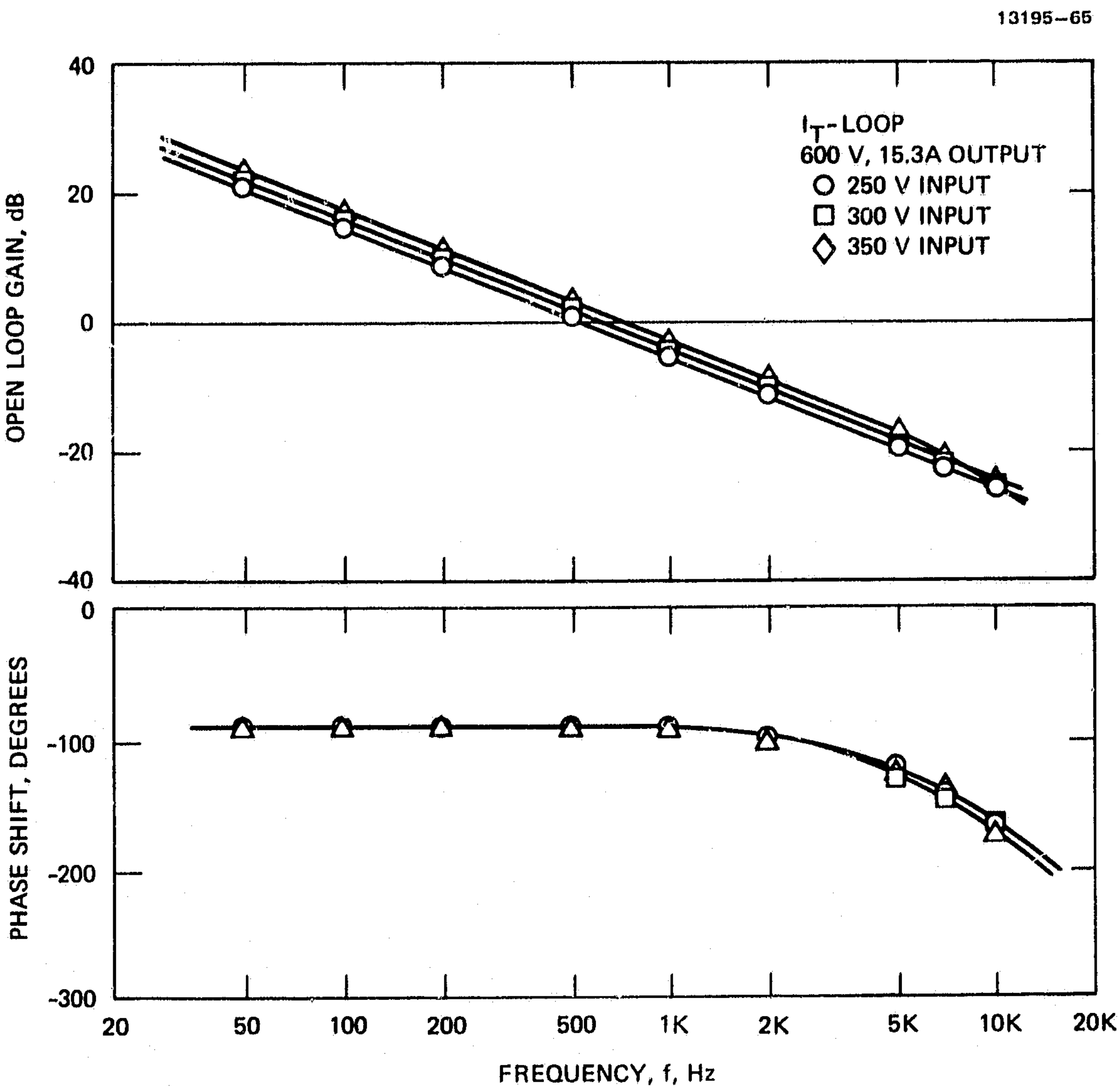

Figure 46. Bode plots of the tank-current control loop for various input voltages and a 600-V/15.3-A output.

B. STEADY-STATE WAVEFORMS

Photographs of oscilloscope traces of the major current and voltage waveforms in the inverter were taken for various output conditions. Figure 47 shows the Q3 base-drive current, resonant capacitor voltage, and tank current for a 300-V input, a 40-Ω load, and output voltages of 200, 600, and 1000 V. At an output of 1000 V and 25.3 A the peak tank current is 240 A and the peak voltage on the resonant capacitor is 700 V. Figure 48 shows the same three waveforms for output conditions of 1000 V/4.9 A, 250 V/24.4 A and OV/5A. The 1000 V/4.9 A case is a lightly loaded condition and the waveforms show the effects of sub-resonant-frequency currents and output transformer saturation. The OV/5A case shows the transistor switch and commutating diode portions of the tank current being equal, indicating that all of the energy is returned to the source with none being transferred to the load. The output transformer primary voltage and resonant-inductor voltage waveforms are shown in Figure 49.

C. OUTPUT RIPPLE

The output ripple for three different output conditions and a 300-V input is shown in Figure 50, along with the tank current as a reference. Figure 51 is a map of output ripple (in % peak-to-peak) for various output operating points and for inputs of 250, 300, and 350 V. Figure 52 is a similar map except that it is in volts peak-to-peak. From Figure 51 it can be seen that the output ripple increases in percentage as the output goes to lower voltages and lighter loads. From Figure 52 it can be seen that the output ripple increases in absolute value as the output goes to lighter loads, and is highest for the open circuit, low voltage case. The peak-to-peak ripple could be reduced by adding more output capacitance, but this would also decrease the bandwidth of the frequency response.

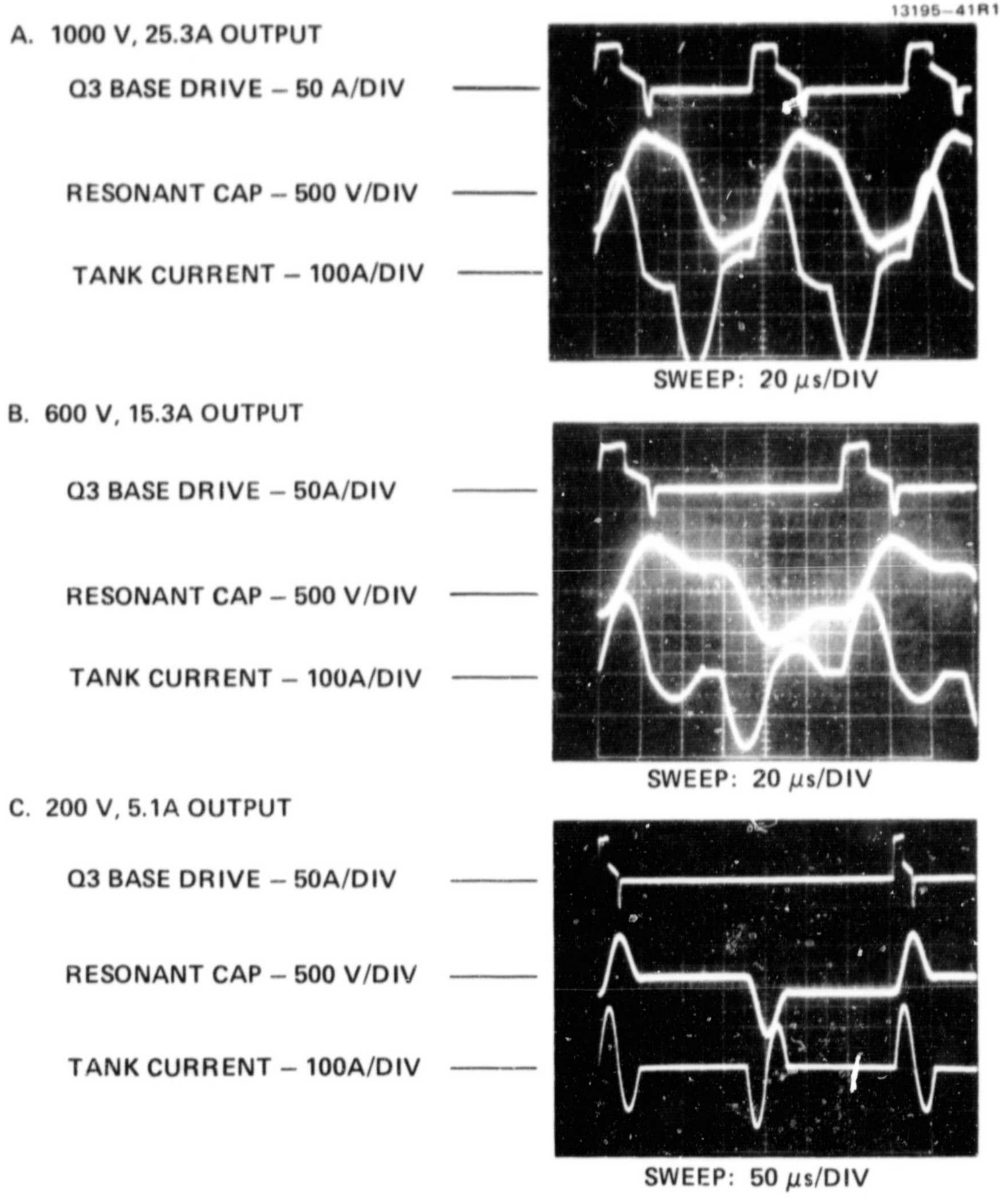

Figure 47. Steady-state base-drive, resonant-capacitor voltage, and tank current waveforms for a 40-Ω load and 300 V input.

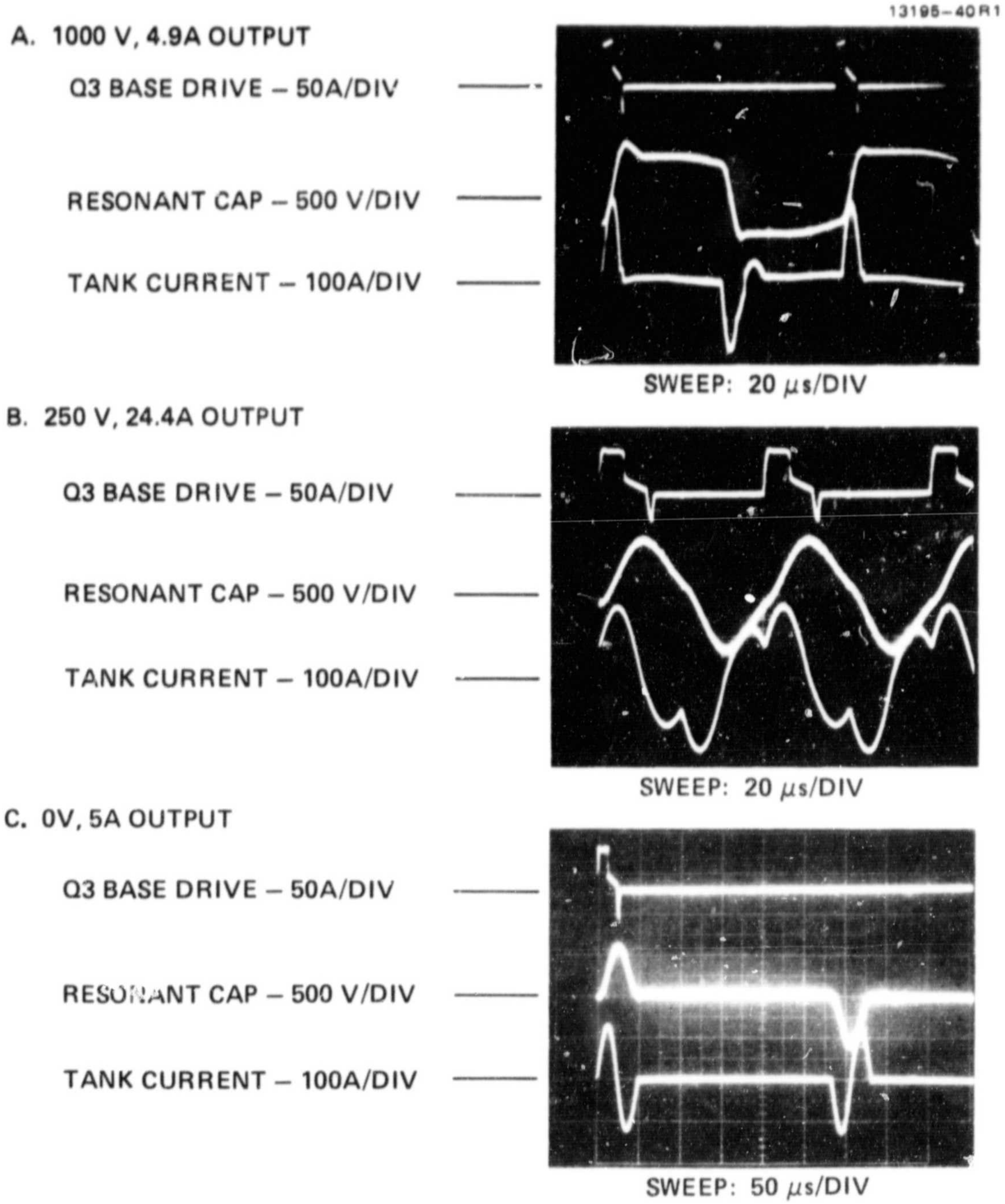

Figure 48. Steady-state base-drive, resonant-capacitor voltage, and tank current waveforms for various load conditions and a 300 V input.

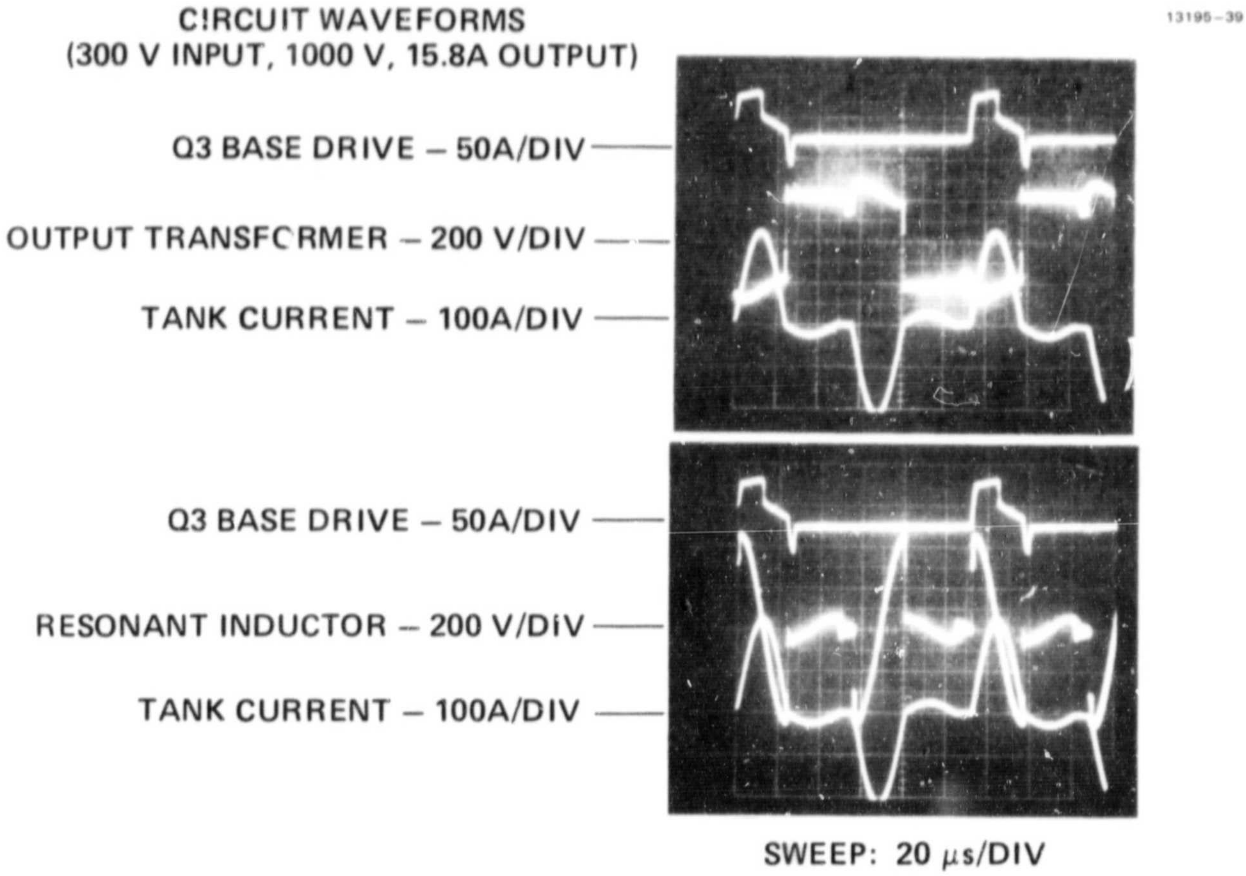

Figure 49. Steady-state base-drive, output transformer, tank current, and resonant-inductor waveforms.

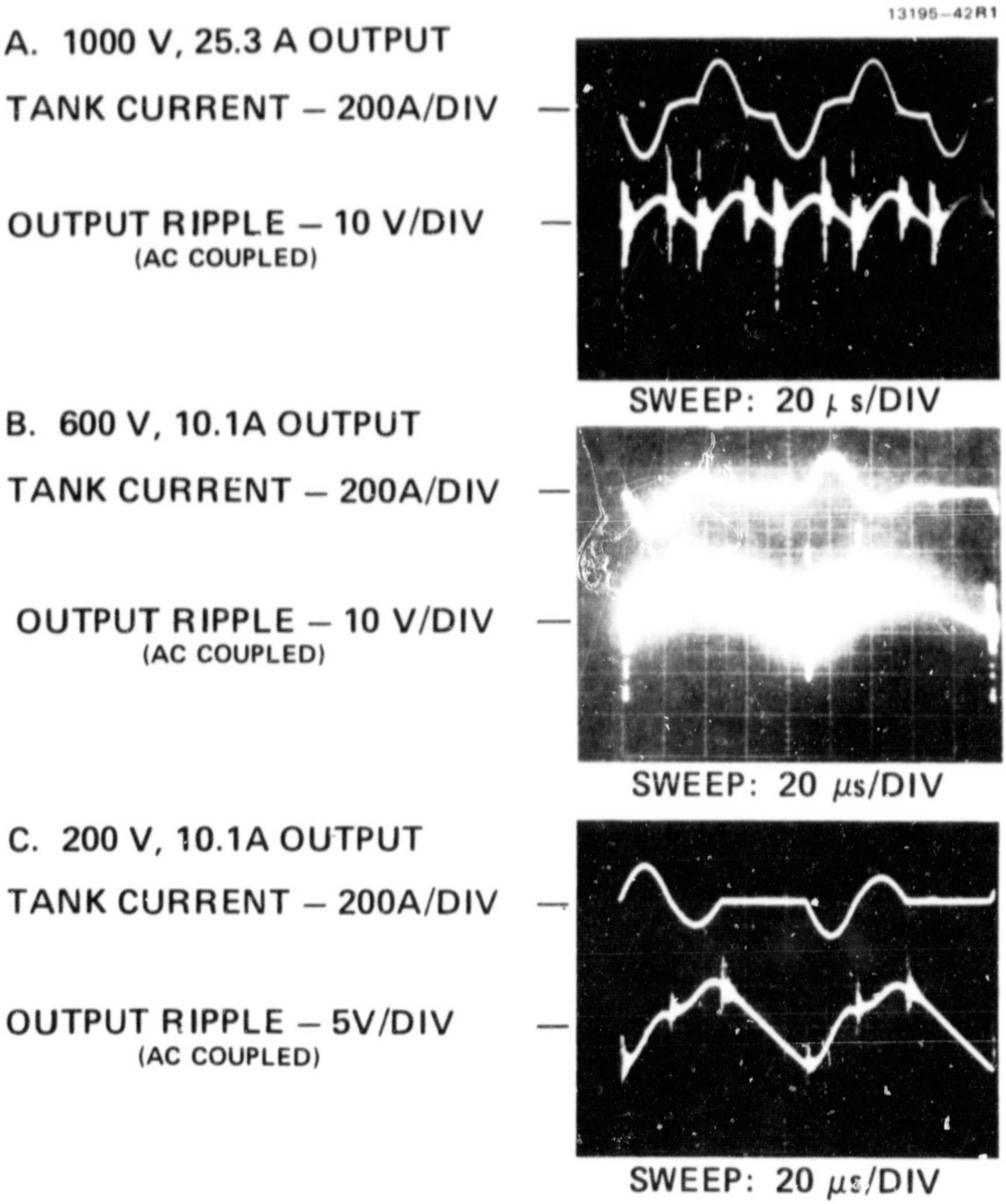

Figure 50. Output-voltage ripple for an input of 300 V and three separate output conditions.

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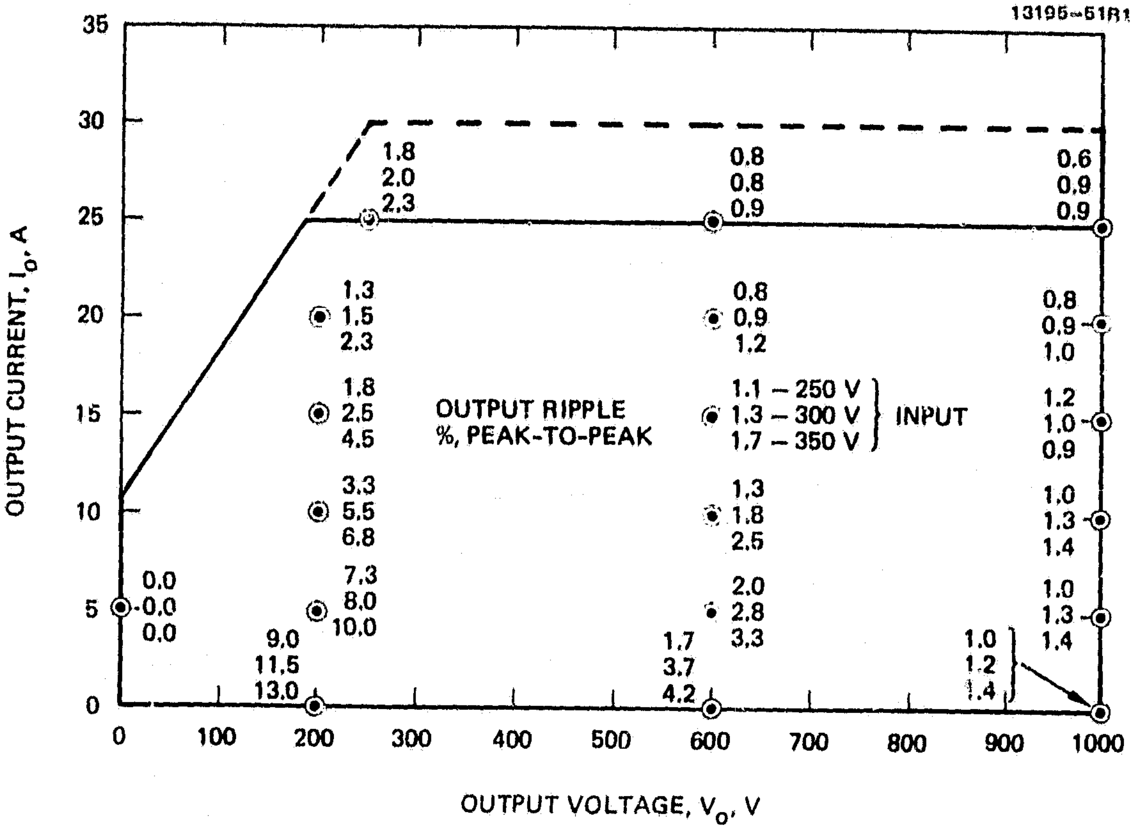

Figure 51. Map of output-voltage ripple for various operating points (% peak-to-peak).

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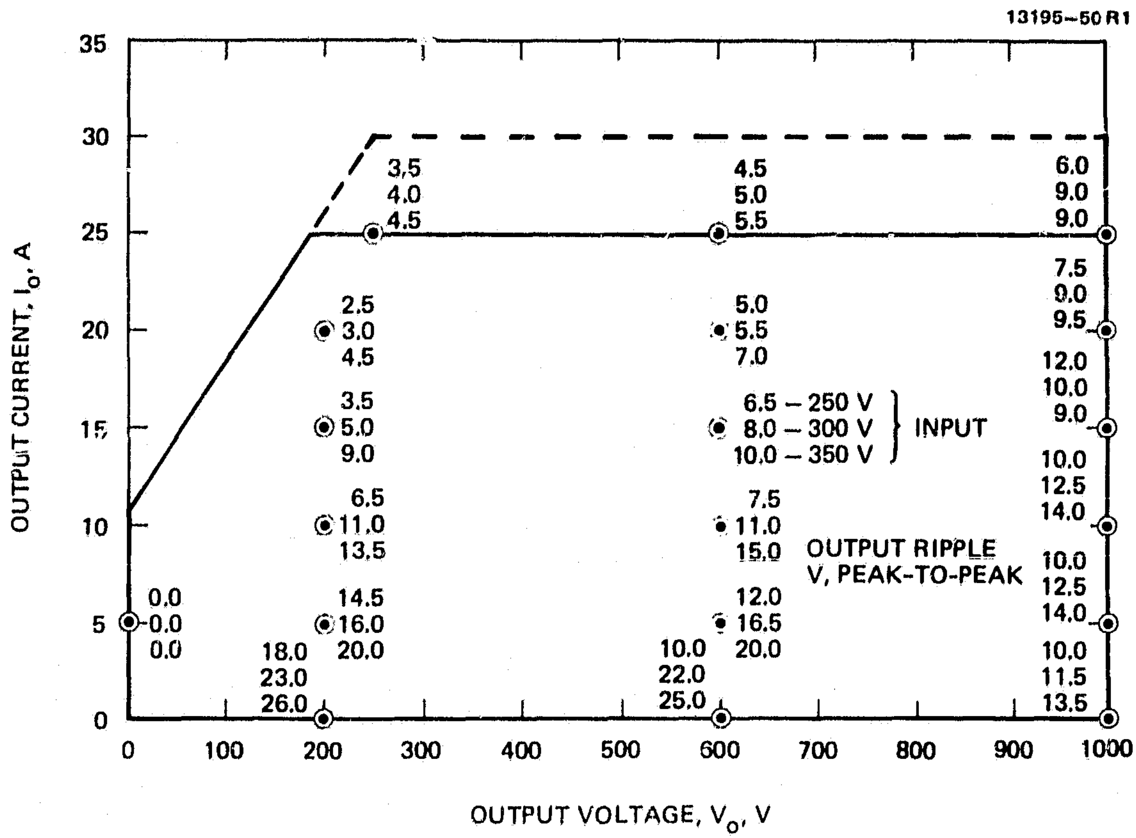

Figure 52. Map of output-voltage ripple for various operating points (volts peak-to-peak).

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D. INPUT CURRENT RIPPLE

The input-current spectrum is shown in Figures 53 and 54 for full load and lightly loaded conditions, respectively. Superimposed on the spectra is the MIL-STD-461B conducted emissions limit. As can be seen from Figures 53 and 54, the input filter of the converter is not adequate to meet MIL-STD-461B. The Contract imposed no EMI/EMC requirements, and therefore these data are for information only. It is interesting to note that all of the emissions are harmonics of the modulation frequency and that the resonant frequency and its harmonics or subharmonics do not appear. The even harmonics of the modulation frequency are larger in amplitude than the odd harmonics because of the full wave rectification provided by the bridge circuit. Signals below the 3-mA level are not reliable data (with respect to amplitude) because of pickup in the measurement equipment. The current peak at 46.8 kHz is not related to operation of the resonant tank, but is instead the operating frequency of the small inverter which drives the input circuit breaker.

E. LINE AND LOAD REGULATION

The output voltage of the converter varied less than 1 V as the input was varied over the range of 250 to 350 V, provided that the output was loaded. For the open-circuit-output condition, the output varied as shown in Table 5.

The output voltage of the converter varied less than 1 V as the output current was varied over the range of 5 to 25 A. In going from 5 A to 0 A, the output voltage increased as shown in Table 6.

If the converter is operated as a dual-output supply and the loads are equal, then the two outputs will track each other within 1 V. However, if the loads are not equal, then the output with the lighter load will be at a higher voltage. Figure 55 shows how the negative output voltage tracks the positive output voltage for a 20-Ω load on the positive output and various loads on the negative output.

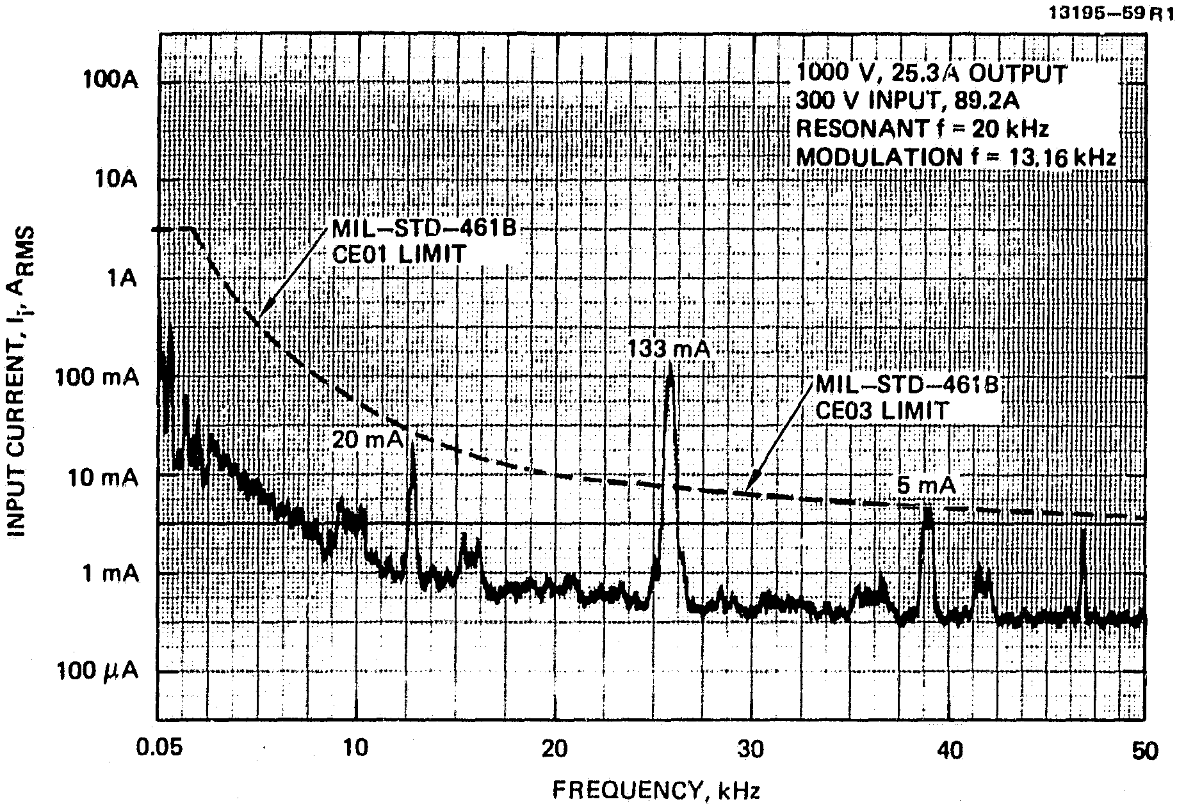

Figure 53. Input-current spectrum for a full-load condition.

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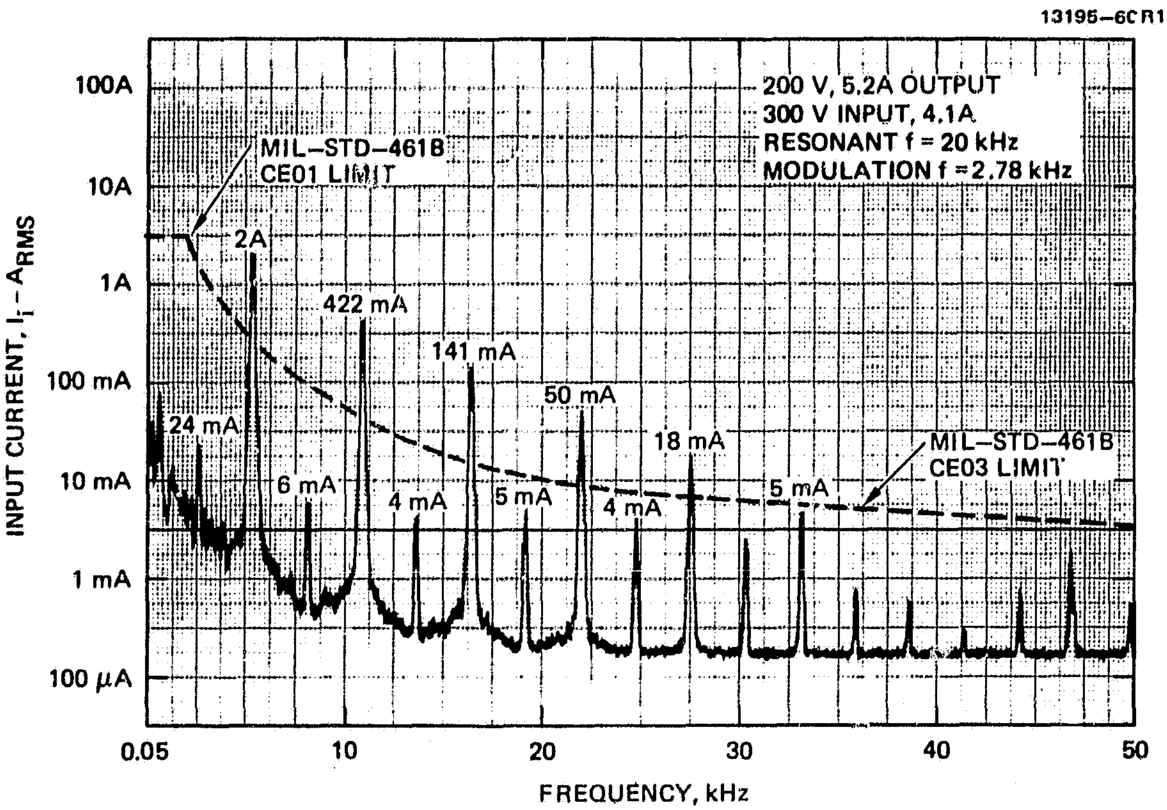

Figure 54. Input-current spectrum for a lightly loaded condition.

Table 5. Line Regulation for the Open-Circuit-Output Condition

Input Voltage, V	Output Voltage, V		
	Nominal Output Voltage, V		
	200	600	1000
250	200	600	1001
300	204	612	1003
350	209	617	1005

Table 6. Load Regulation for 5-A to 0-A Loads

Input Voltage, V	Output Voltage, V					
	Io, A		Io, A		Io, A	
	5	0	5	0	5	0
250	200	271	600	661	1000	1060
300	200	276	600	663	1000	1062
350	200	281	600	678	1000	1065

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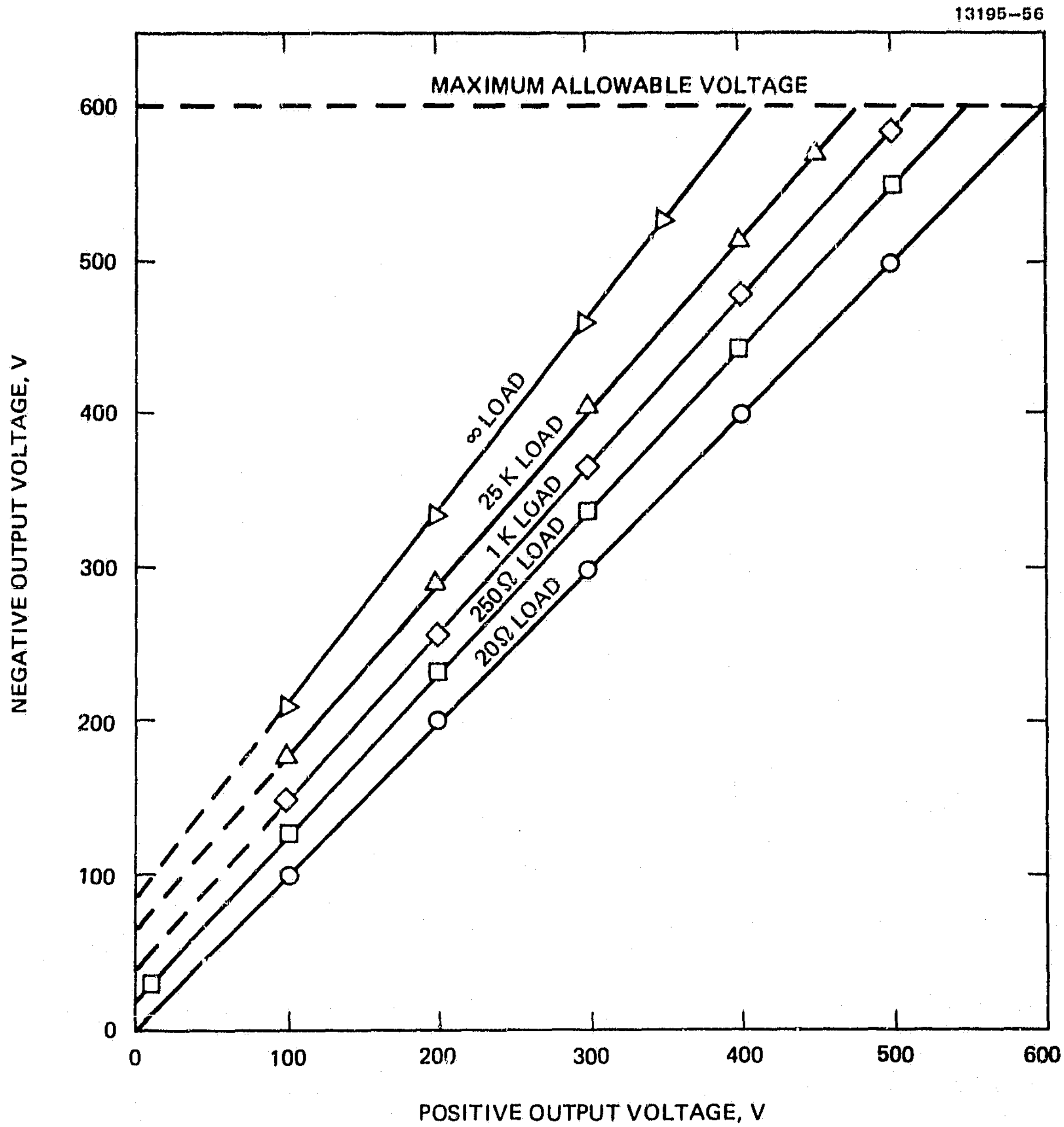

Figure 55. Negative output voltage versus positive output voltage for a 20-Ω load on the positive output and various loads on the negative output.

F. TRANSIENT LINE AND LOAD TESTS

The converter was tested for its response during turn-on of the main bus supply and for load transients of the operating point to short circuit, short circuit to the operating point, operating point to open circuit, open circuit to the operating point, open circuit to short circuit, and short circuit to open circuit.

The circuit shown in Figure 56 was used as a closing switch and as an opening switch for the transient load testing. It provides a risetime and falltime of ~ 10 μs for the transients being generated.

The input bus voltage and current are shown in Figure 57 during turn-on to a full load output. Figure 57(a) shows turn-on of the power stage with the input circuit breaker already closed. The input current is well behaved and does not overshoot. The little blip at 3 ms is associated with the automatic crossover between one control loop and another which occurred at that time. Figure 57(b) shows closing of the input circuit breaker with the power stage already ON. There is a 330-A current spike which decays to zero in 700 μs, and then the current starts to rise again in a controlled manner. Figure 58 shows the input-bus current during closing of the input circuit breaker with the power stage turned OFF. Figure 58 is almost identical to Figure 57(b), indicating that the large current spike is the result of charging up the input filter and is not associated with the converter itself.

The tank current, output current, and input current response to a load transient of 1000 V at 25.3 A to short circuit is shown in Figure 59. The tank current is limited to a peak of 300 A and the effect of the peak tank current limiting circuitry can be seen. The converter is phased completely OFF at 50 μs by way of the peak tank current limiting circuitry having reset all the integrators in the control loops. At 170 μs the integrators are phasing the converter back ON in a

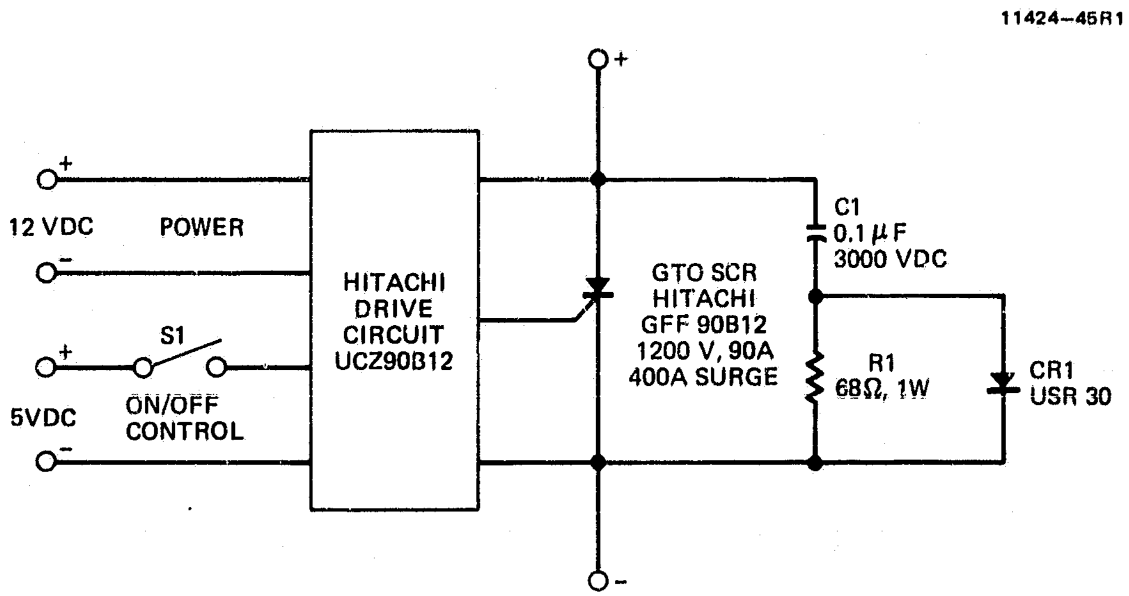

Figure 56. Circuit used as a closing and opening switch for transient load testing.

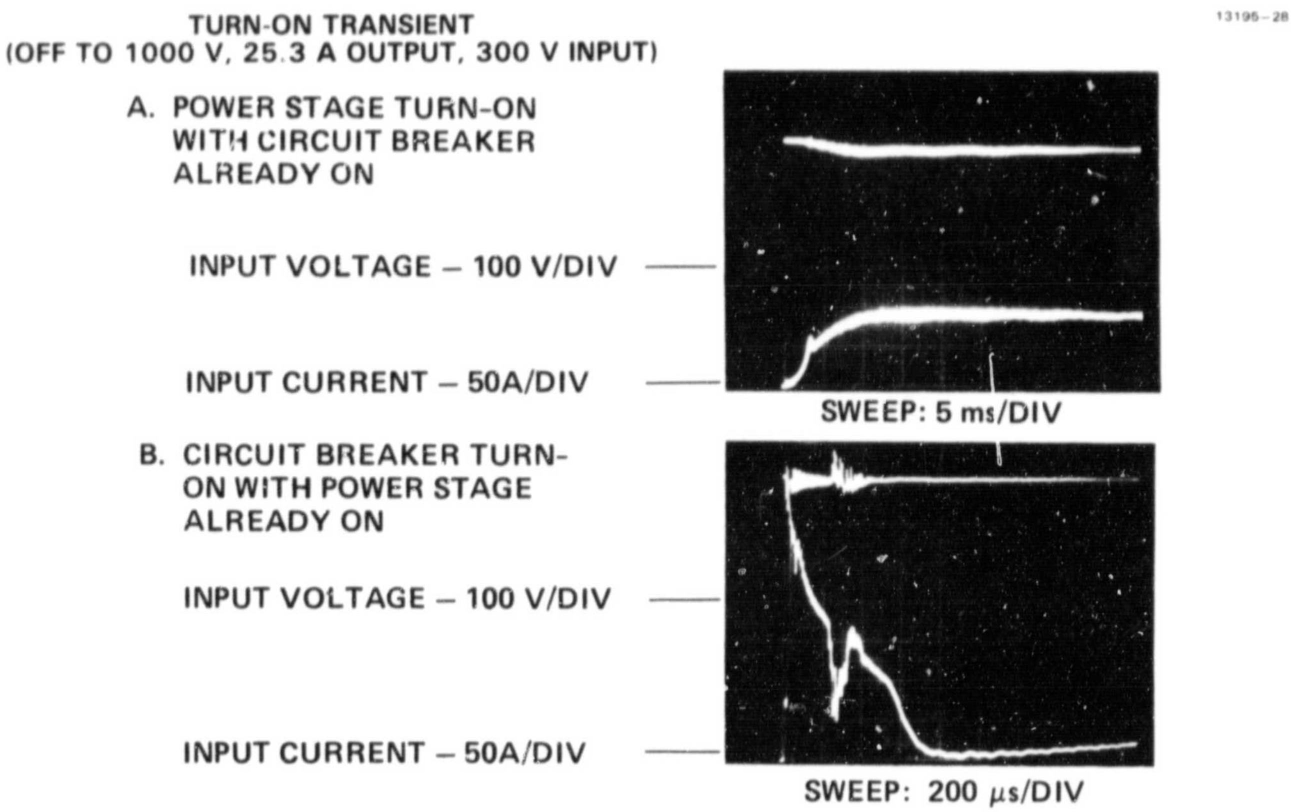

Figure 57. Input bus voltage and current during turn-on to the full load output.

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TURN-ON TRANSIENT
(CIRCUIT BREAKER TURN-ON
WITH POWER STAGE OFF)

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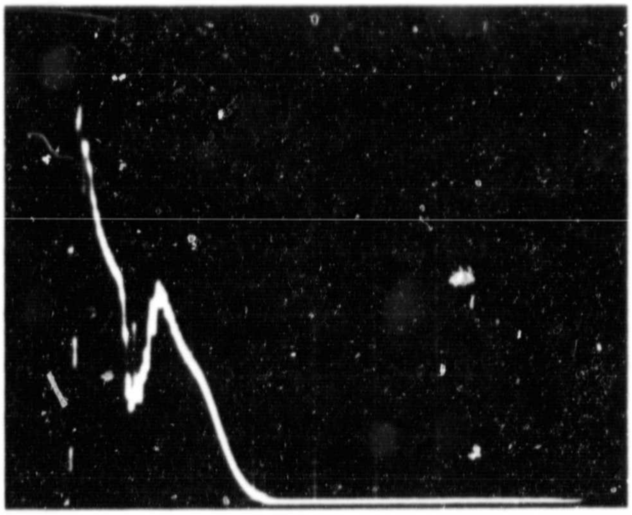

INPUT CURRENT – 50A/DIV

SWEEP: 200 μs/DIV

Figure 58. Input bus current during closing of the input circuit breaker with the power stage off.

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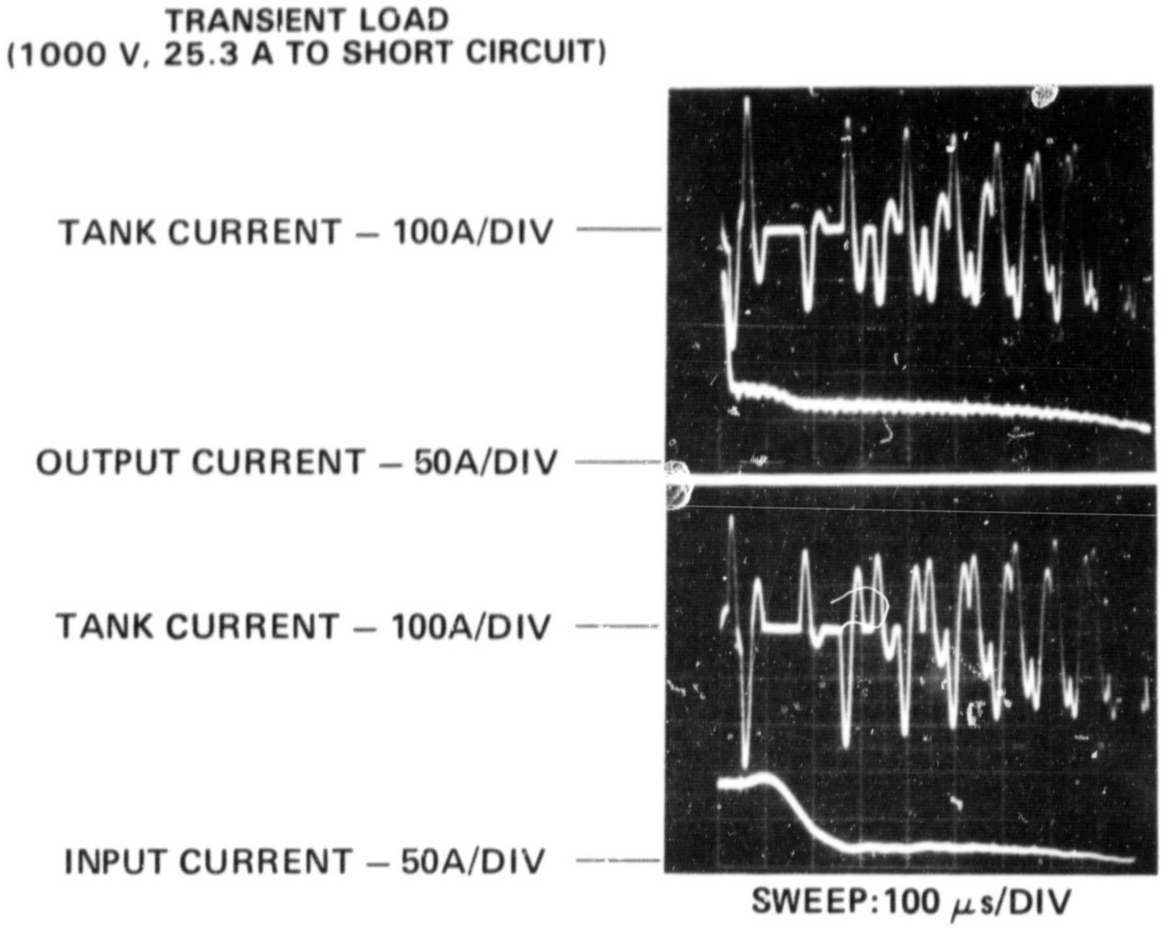

Figure 59. Tank current, output current, and input current response to a load transient of 1000 V at 25.3 A to short circuit.

controlled manner. The output current is limited by the output-transient-current limiters as described in Section 3.E above. The input current shows a slight increase in amplitude at 100 μs and then drops toward zero.

Figure 60 shows the response of the tank current, output voltage, and input current to a load transient of short circuit to 1000 V at 25.3 A. All three waveforms are well behaved with no overshoot and the output voltage is approaching 1000 V in 10 ms.

The tank current, output voltage, and input current response to a load transient of short circuit to open circuit at 1000 V is shown in Figure 61. The tank current and input current peak at 2 ms as the output capacitors are charged and then both drop toward zero. The output voltage rises to 1000 V in 12 ms with no overshoot.

Figures 62(a) and 62(b) show the response of the tank current and output voltage to load transients of 200 V at 5.2 A and 1000 V at 25.3 A, respectively, to open circuit. In both cases the tank curent is quickly phased OFF by the output voltage limiting circuit. The output voltage overshoots its setpoint by 40 V in Figure 62(a) and by 70 V in Figure 62(b). In both cases the output voltage slowly drops back toward the setpoint since there is no load to discharge the output capacitors.

The response of the tank current, input current, and output voltage to a load transient of open circuit at 1000 V to a full load of 1000 V at 25.3 A is shown in Figure 63. The input current overshoots ~ 20 A for 1 ms as the converter recovers from the transient. The output voltage drops ~ 150 V as the full load is applied and recovers within 2 ms.

Figure 64 shows the tank current and output voltage response to a 20% step change in load. In Figure 64(a) the load is increased from 20.6 A to 25.3 A and the output voltage drops ~ 30 V. In Figure 64(b) the load is decreased from 25.3 A to 20.6 A and the output voltage overshoots by ~ 30 V. The effect on the tank current is minimal in both cases.

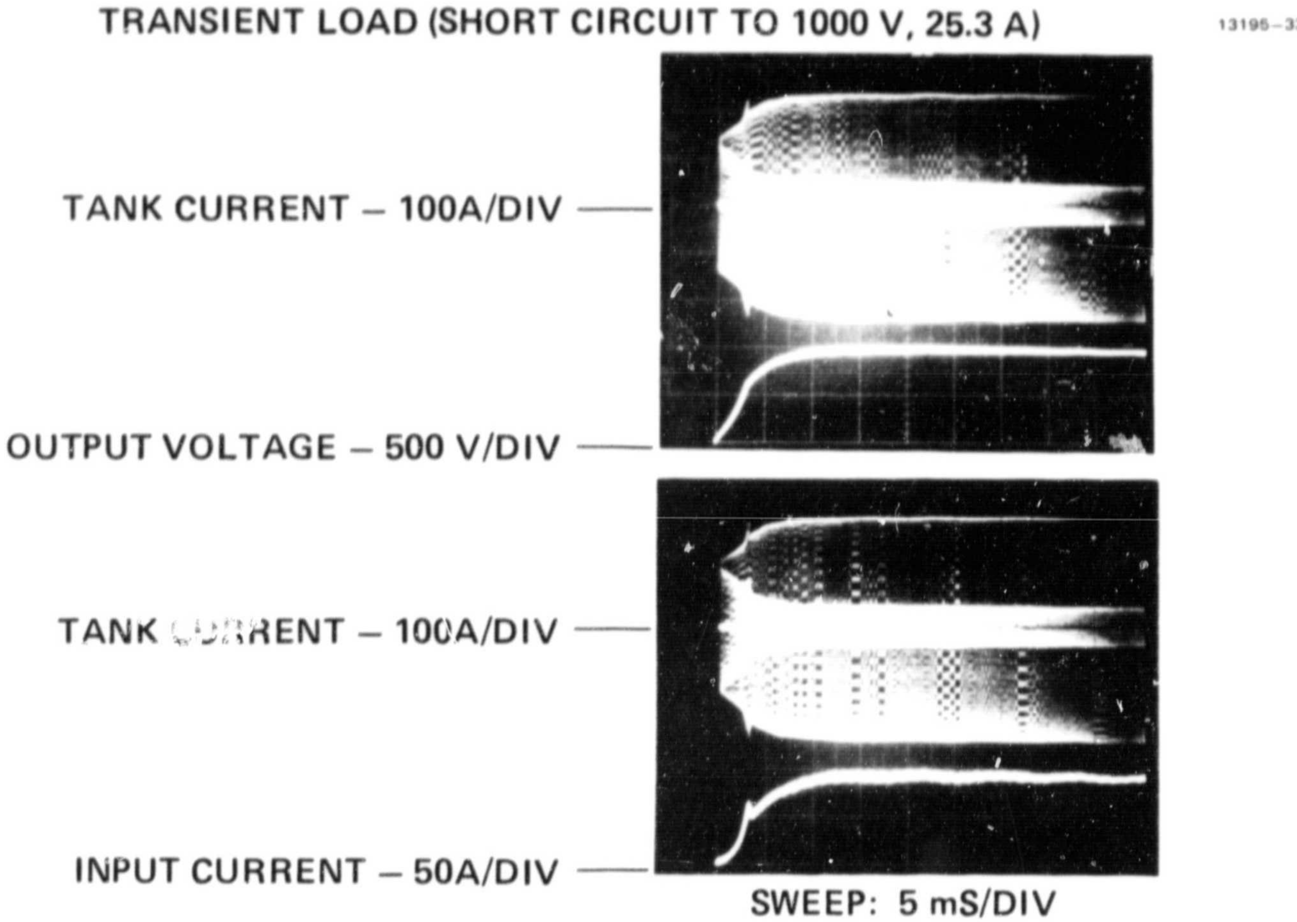

Figure 60. Tank current, output voltage, and input current response to a load transient of short circuit to 1000 V at 25.3 A.

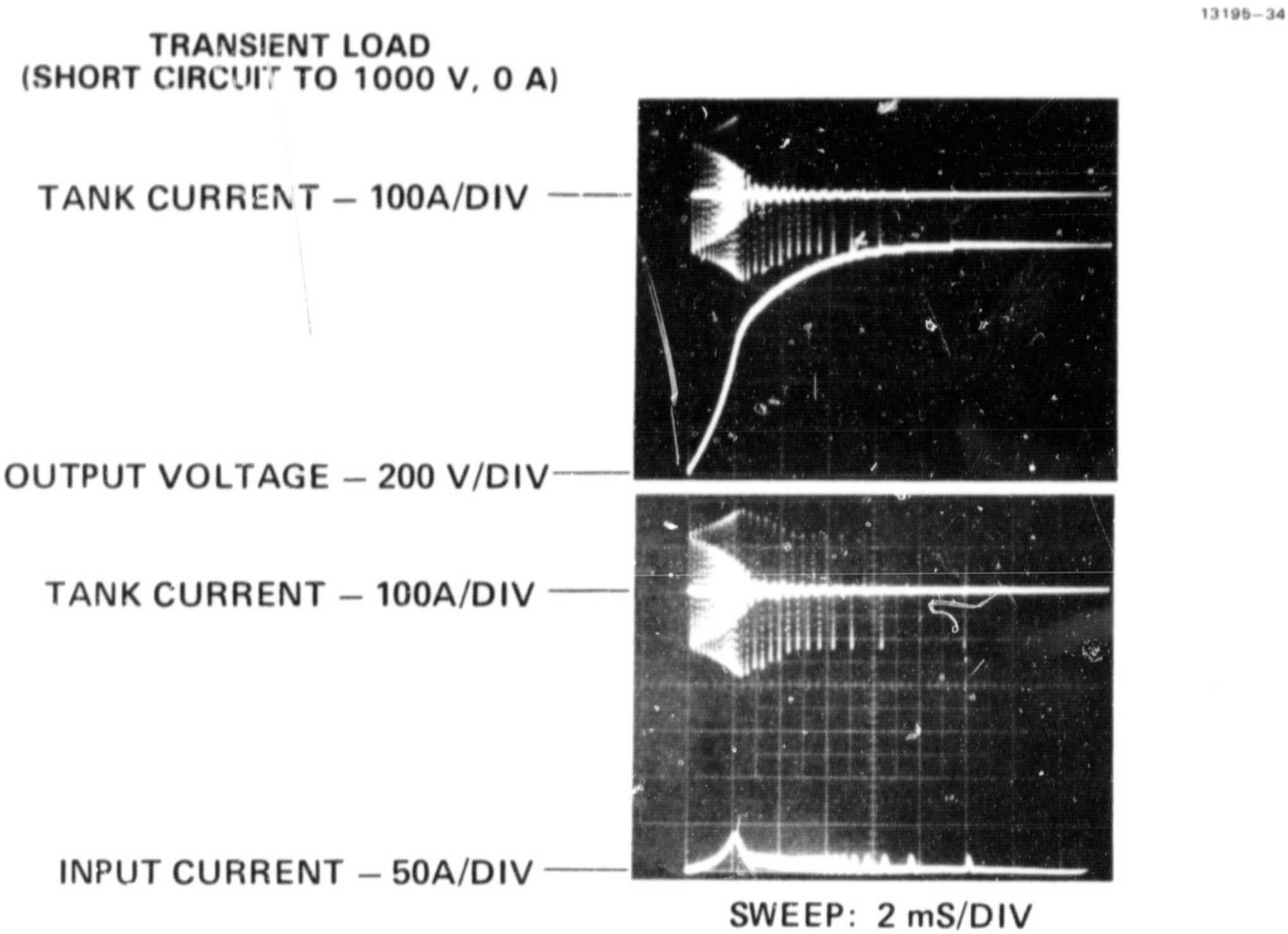

Figure 61. Tank current, output voltage, and input current response to a load transient of short circuit to open circuit at 1000 V.

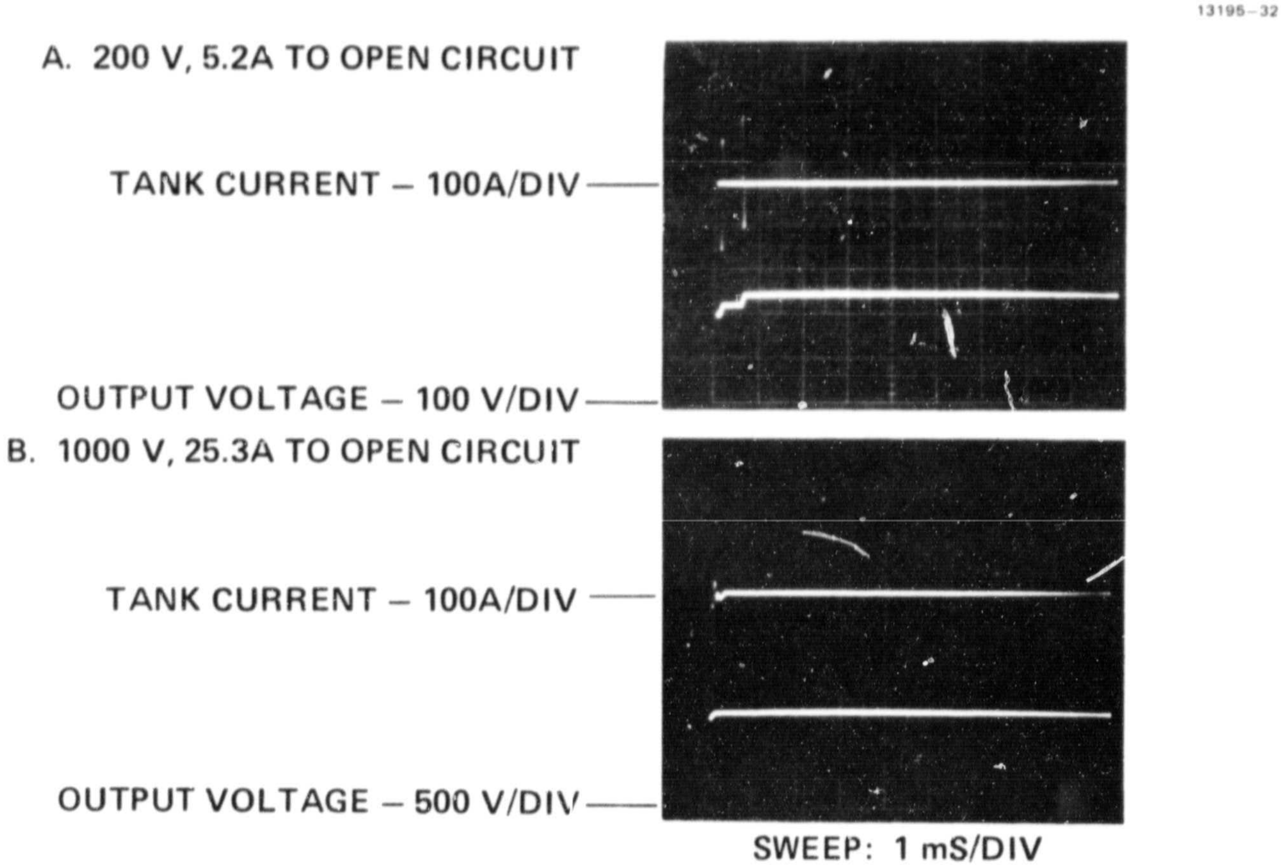

Figure 62. Tank current and output voltage response to load transients of the operating point to open circuit.

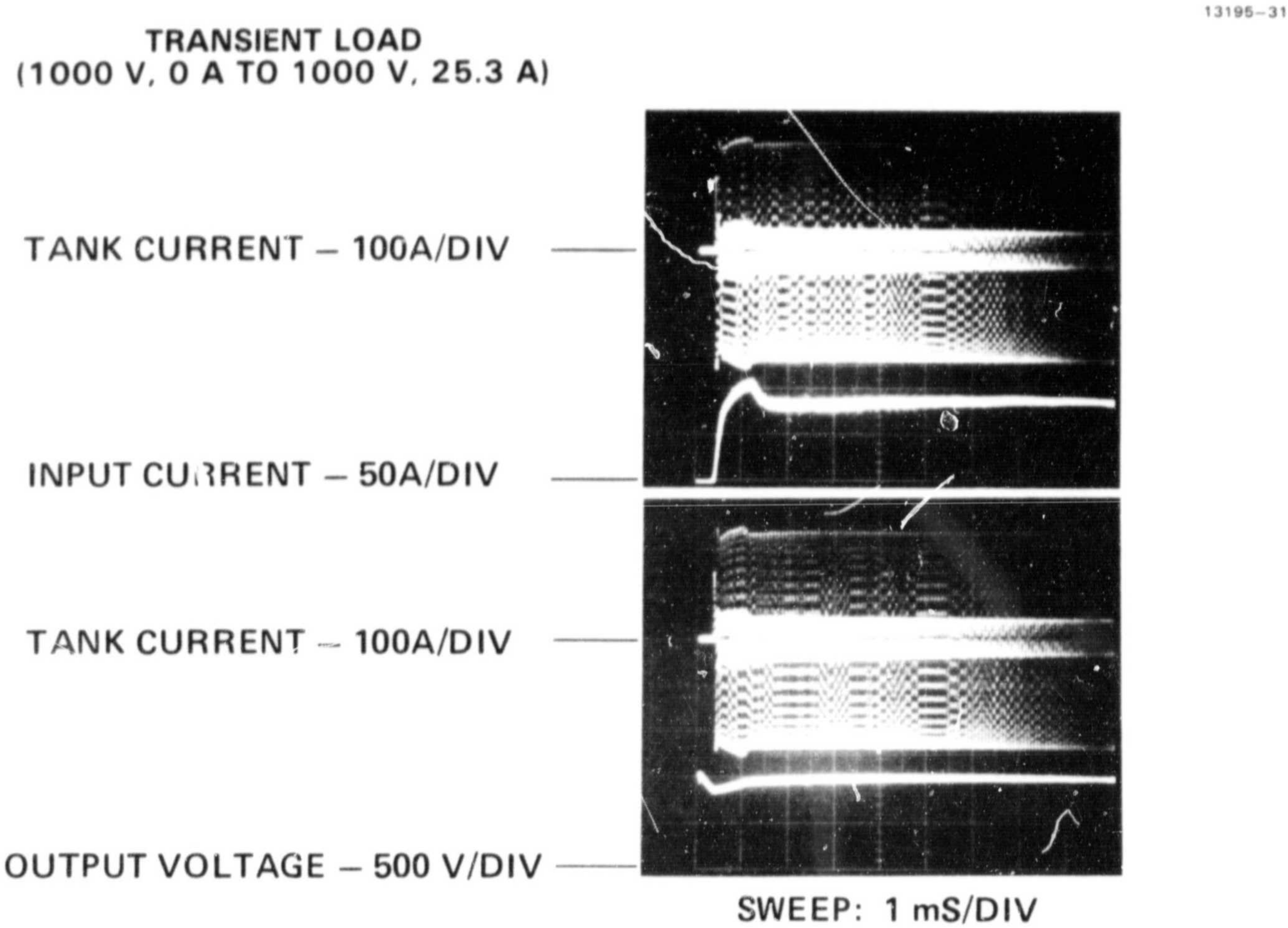

Figure 63. Tank-current, input-current, and output-voltage response to a load transient of open circuit at 1000 V to full load of 1000 V at 25.3 A.

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TRANSIENT LOAD

A. 1000 V, 20.6A TO 1000 V, 25.3A

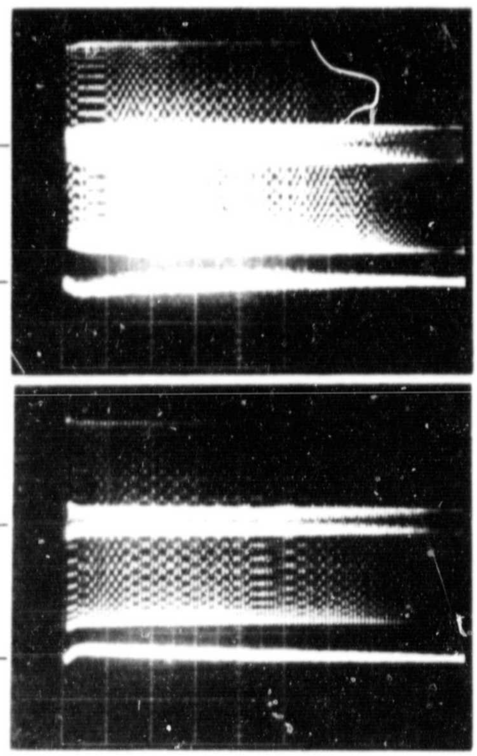
TANK CURRENT – 100A/DIV

OUTPUT VOLTAGE – 100 V/DIV
(AC COUPLED)

B. 1000 V, 25.3A TO 1000 V, 20.6A

TANK CURRENT – 100A/DIV

OUTPUT VOLTAGE – 100 V/DIV
(AC COUPLED)



SWEEP: 1 mS/DIV

Figure 64. Tank-current and output-voltage response to a 20% step change in load.

G. EFFICIENCY MEASUREMENTS

The efficiency of the converter was measured under static conditions while operating into a resistive load. This converter contains two elements that are not normally associated with the efficiency numbers quoted for converters: the input circuit breaker and the output-transient-current limiters. Therefore, three different efficiencies will be discussed. These efficiencies are defined as follows:

- POWER STAGE EFFICIENCY - the output power divided by the 250 to 350 V input-bus power and includes the losses associated with the input circuit breaker and the output-transient-current limiters, but not the housekeeping power.
- TOTAL EFFICIENCY - power stage efficiency with housekeeping power losses added. This is the overall efficiency of the hardware as delivered.
- CONVERTER EFFICIENCY - total efficiency with the input circuit breaker and output-transient-current limiter losses removed (both power stage losses and housekeeping power losses removed).

Power stage and total efficiency curves versus output power are shown in Figures 65 and 66 for a constant load of 40 Ω and a constant output of 1000 V, respectively. Both figures show that the efficiency is nearly constant for output power levels above 6 kW. The converter was operated at 30 kW (1000 V, 30 A output) for inputs of 300 and 350 V (cannot get 30 kW out at 250 V in). As can be seen from Figure 66, the efficiency drops off at 30 kW and the D7ST transistor switches may be in thermal runaway at the 350 V input point. The fall off in efficiency at high power is primarily due to an increase in the saturation voltage of the D7STs at these power levels.

Figures 67, 68, and 69 are maps of the power stage, total, and converter efficiencies, respectively, for the operating points tested. The 300-V input, 1000-V/25-A output operating

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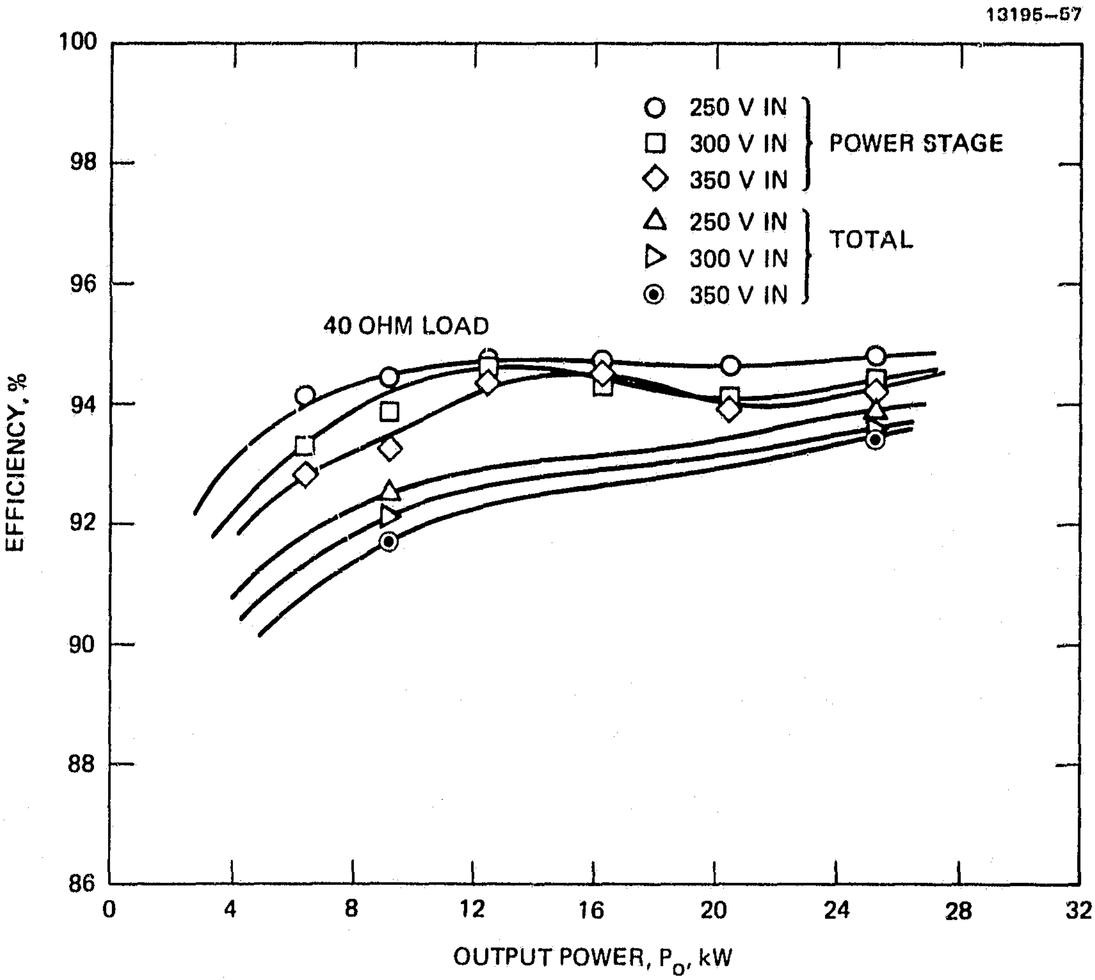

Figure 65. Power stage and total efficiency versus output power with a constant 40-Ω load.

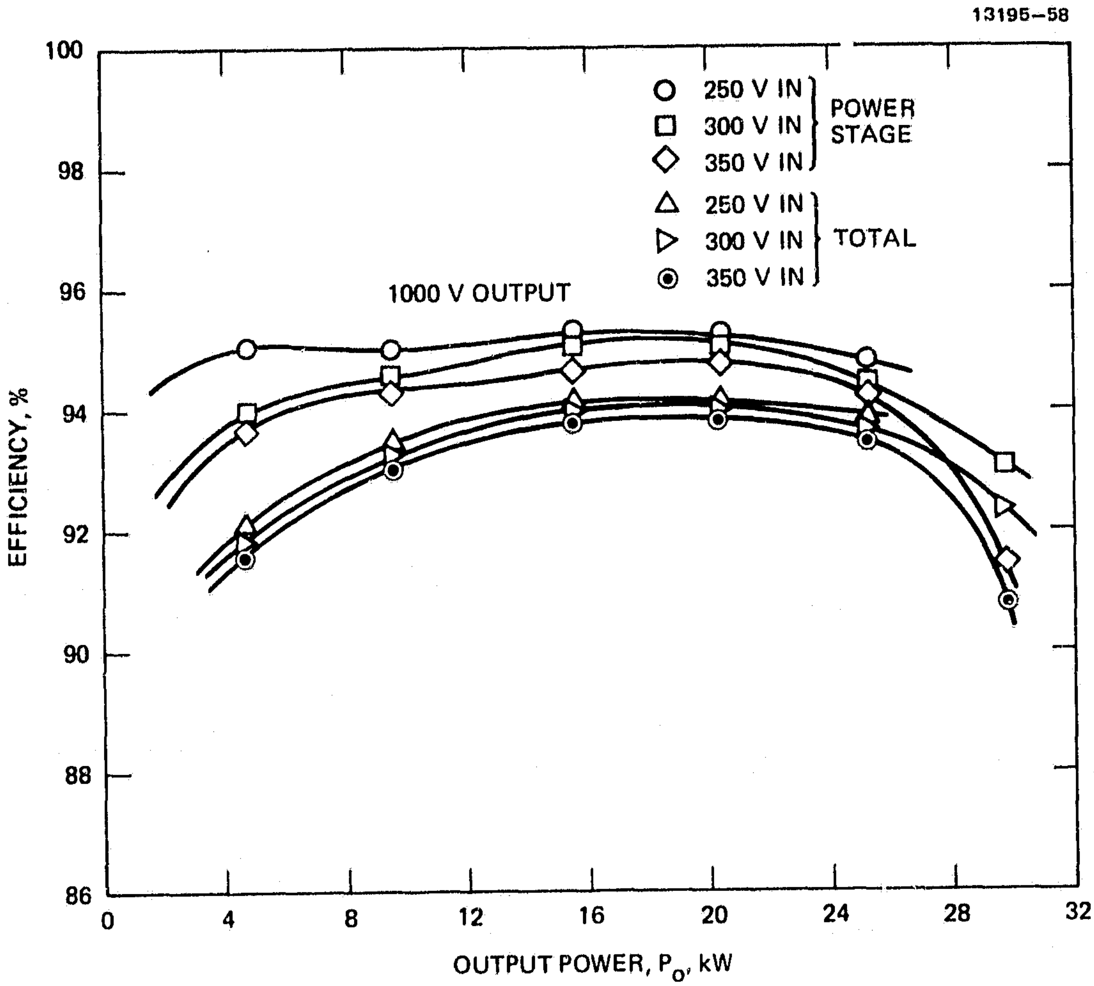

Figure 66. Power stage and total efficiency versus output power for a constant 1000-V output.

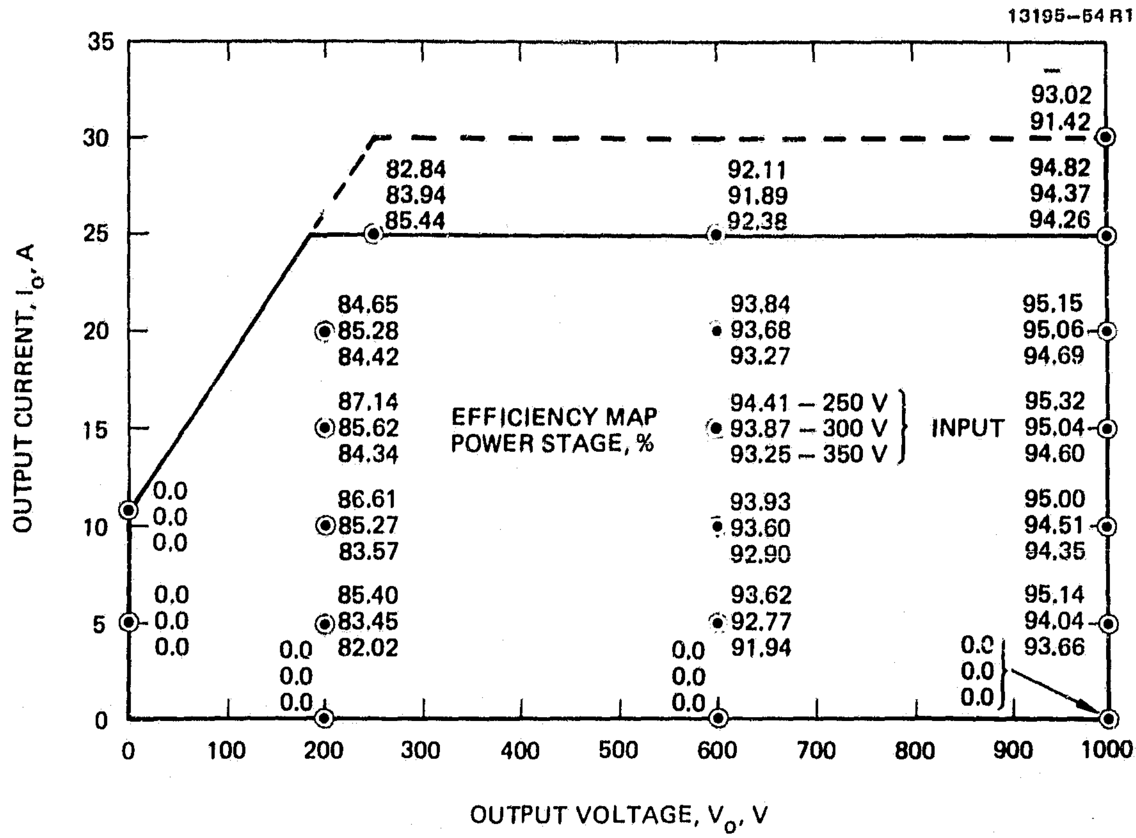

Figure 67. Map of the power stage efficiency for various operating points.

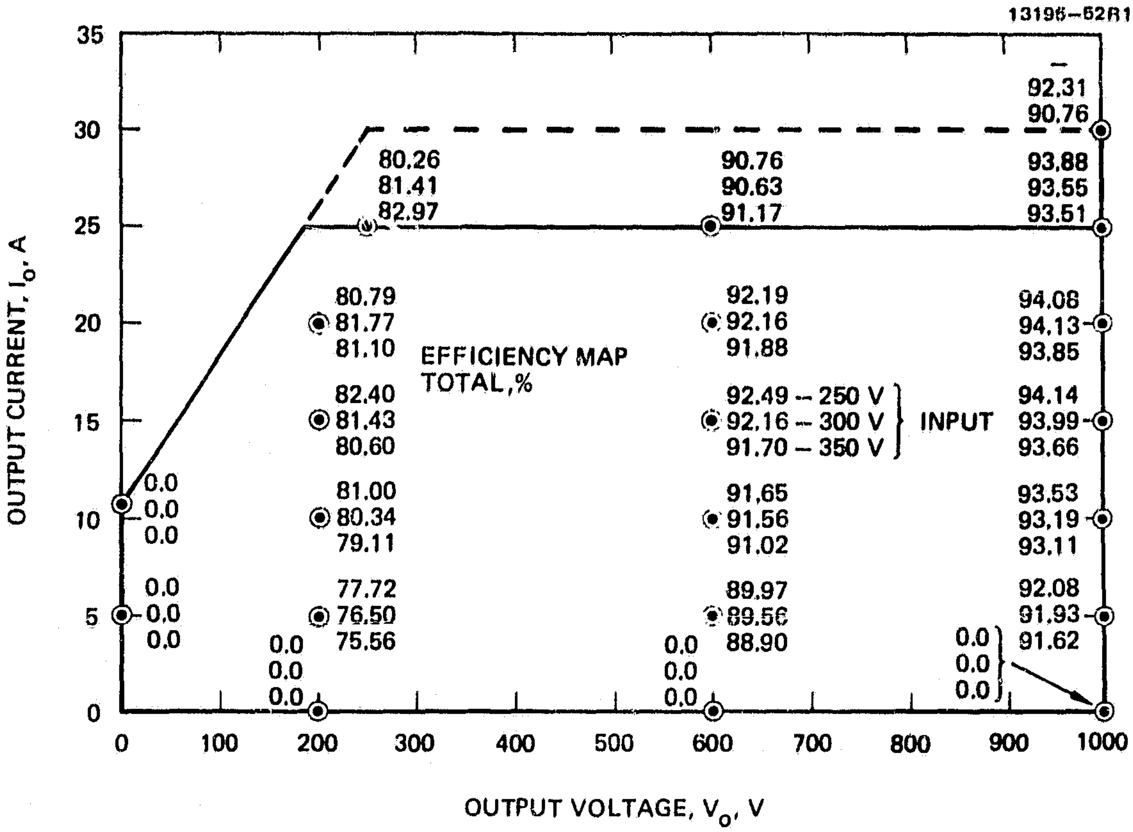

Figure 68. Map of the total efficiency for various operating points.

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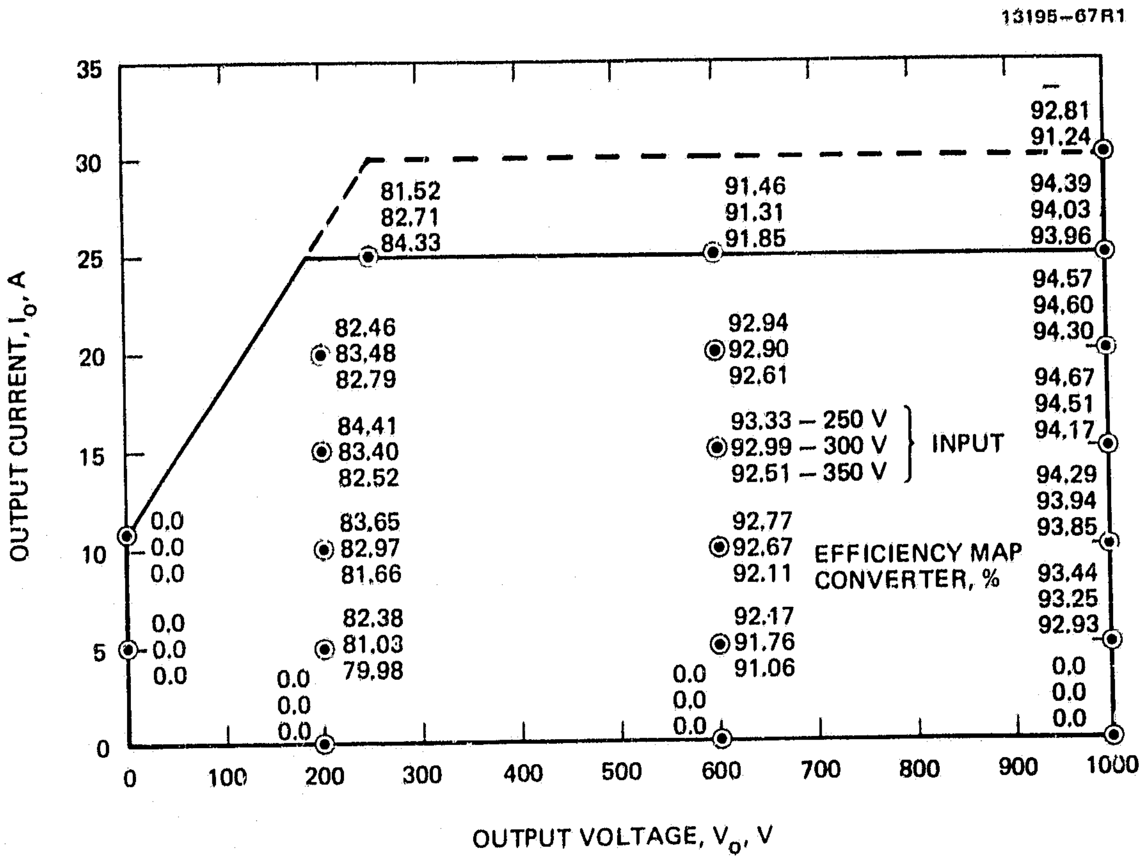

Figure 69. Map of the converter efficiency for various operating points.

point has a power stage efficiency of 94.37%, a total efficiency of 93.55%, and a converter efficiency of 94.03%. Therefore, at the 25-kW power level, housekeeping power accounts for 0.66% (converter efficiency) and the input circuit breaker and output-transient-current limiters for 0.54% (total efficiency) of the difference in efficiencies from the ideal of 100%.

The map of total dissipated power for the operating points tested is shown in Figure 70. The worst-case dissipation (ignoring the 30-kW points) is 1752 W at an input voltage of 350 V and an output of 1000 V/25.3 A.

Figures 71 and 72 are maps of total housekeeping power, and converter housekeeping power, respectively. The highest housekeeping power requirements (again ignoring the 30-kW points) occur at an input of 250 V and an output of 1000 V/25.3 A. By comparing Figures 71 and 72 it can be seen that the input circuit breaker and output-transient-current limiters contribute significantly to the housekeeping power requirements.

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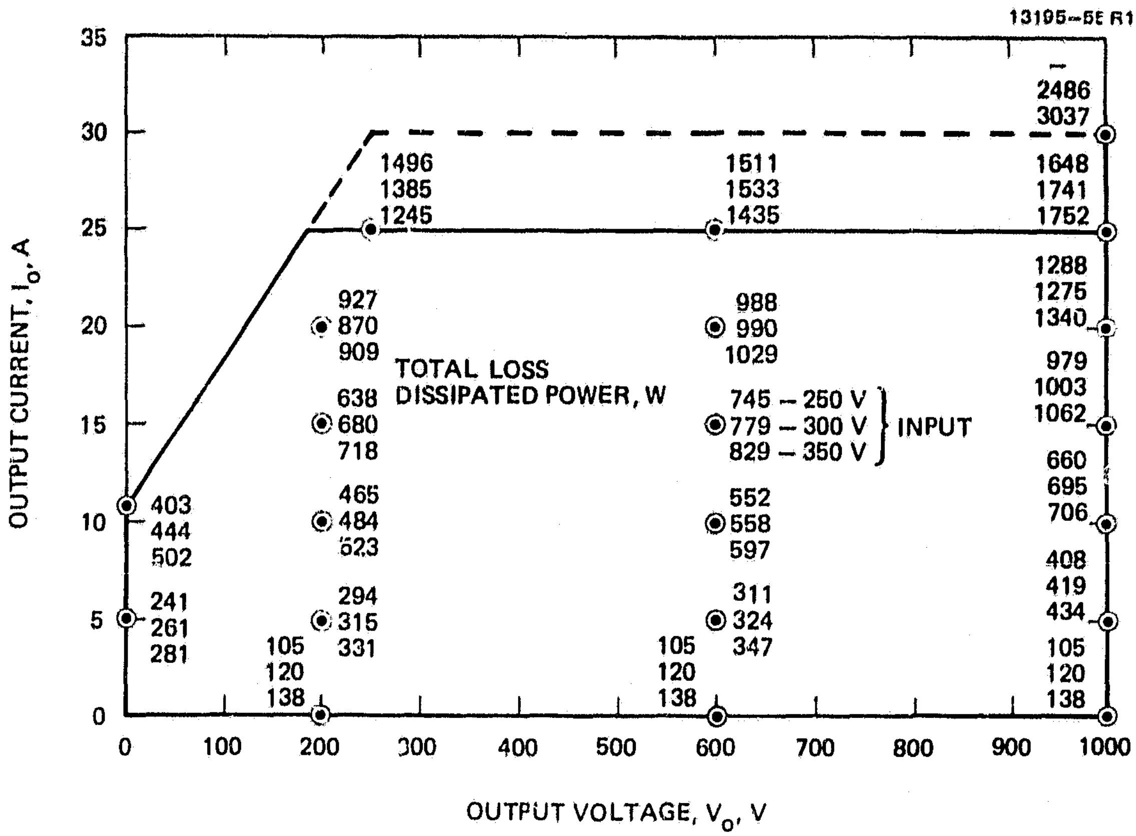

Figure 70. Map of the total dissipated powers for various operating points.

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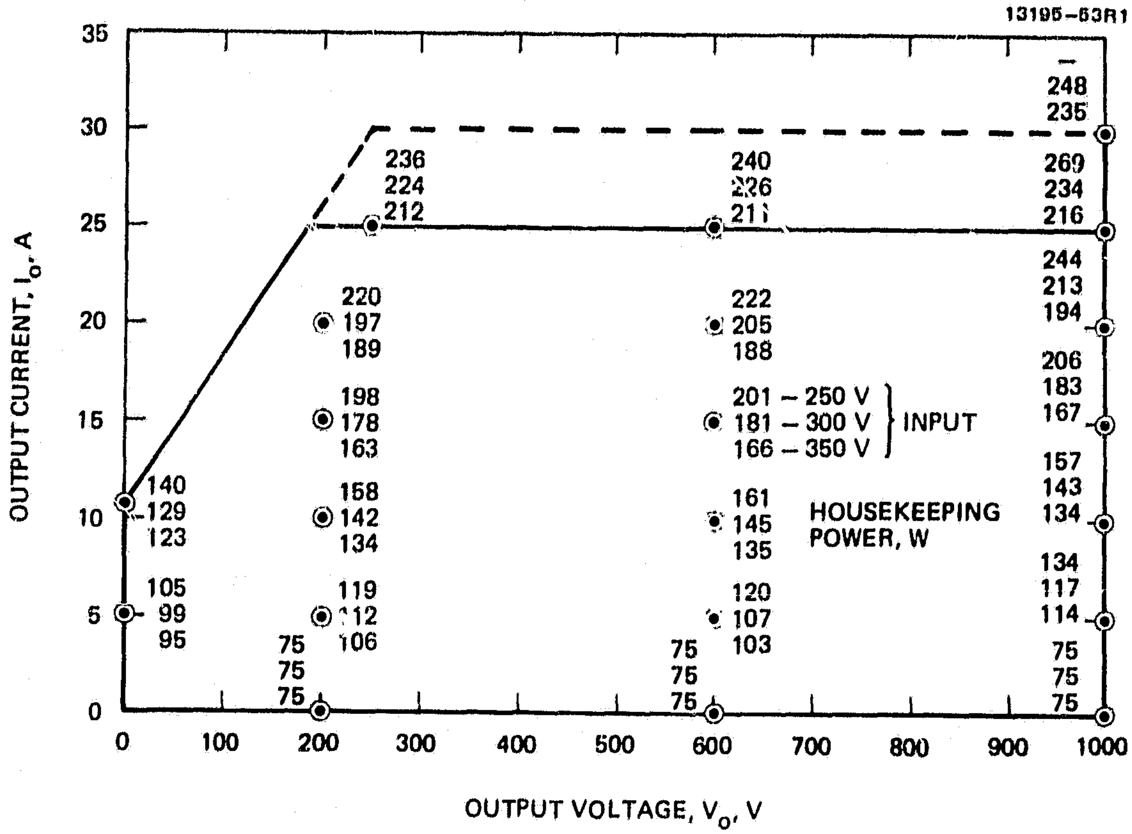

Figure 71. Map of total housekeeping power for various operating points.

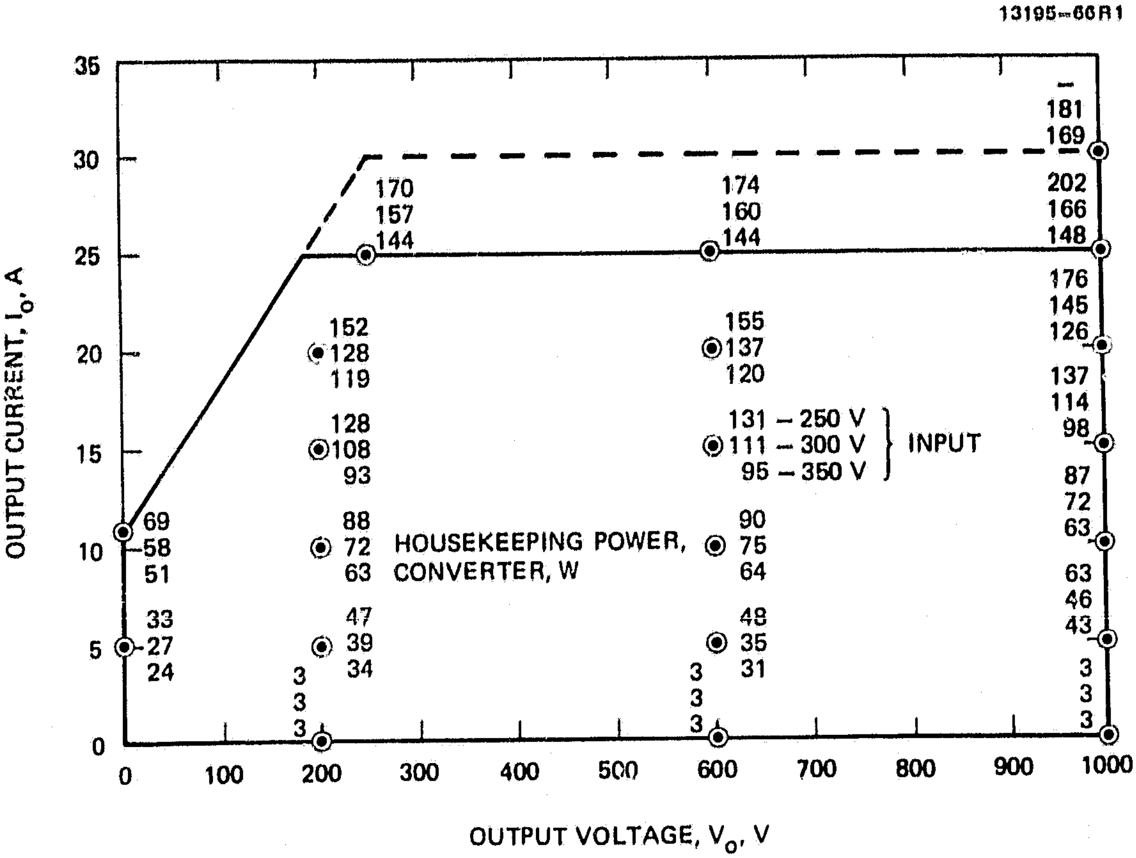

Figure 72. Map of converter housekeeping power for various operating points.

SECTION 5

CONCLUSIONS AND RECOMMENDATIONS

The feasibility of processing 25-kW of power with a single, transistorized, series resonant converter stage has been demonstrated by the successful design, development, fabrication, and testing of such a device. It employs four Westinghouse D7ST transistors in a full-bridge configuration and operates from a 250 to 350 V dc input bus. The unit has an overall worst-case efficiency of 93.5% at its full rated output of 1000 V and 25 A dc. A solid-state dc input circuit breaker and output-transient-current limiters are included in and integrated into the design.

There are no inherent problems that would prevent this 25-kW design from being upgraded to a space-qualified status. The major areas that would need to be addressed are:

- Reliability and qualification of the D7ST transistors.
- Qualifying the series resonant capacitor.
- Electrical design with reduced core size and thermal design of the series resonant inductor and output transformer.
- Input filter design to meet MIL-STD-461B.
- A method of precharging the input filter to prevent large in-rush currents when the input circuit breaker is closed.
- Thermal-vacuum packaging of the entire unit, including heat pipes and the bridge circuit electrical layout, which is critical.

Future effort should be in the areas of:

- Use of gate-turn-off (GTO) SCR switches which will have higher reliability due to their higher voltage ratings and will also permit higher power levels.

- Switch development (transistors or GTO-SCRs) toward shorter turn-off times and lower inductance packages.
- AC topologies for use with ac distribution systems.
- Standardized control circuitry based on the design used for this 25-kW converter.

REFERENCES

1. R.J. King and T.A. Stuart, "Modeling the Full-Bridge Series-Resonant Power Converter," IEEE Transactions on Aerospace and Electronic Systems, AES-18, 4, 449-459 (July 1982).

2. J.J. Biess and L.Y. Inouye, "Design Study for Improved Ion Thruster Power Processor Final Report - Volume II," Technical Report NASA CR-165288, prepared by TRW Defense and Space Systems Group, Redondo Beach, CA., December 1980.

3. T.A. Stuart and R.J. King, "A study of the High Frequency Limitations of Series Resonant Converters," results of NASA Grant NSG-3281 for the period 1 Sept 1981 to 31 August 1982, University of Toledo, Sept. 1982.

4. R.R. Robson and D.J. Hancock, "A 10-kW Series Resonant Converter Design, Transistor Characterization, and Base-drive Optimization," NASA Contractor Report CR-16554, 1981.

APPENDIX I

OPERATION OF A FULL BRIDGE SERIES RESONANT INVERTER (SRI)

A full-bridge series resonant inverter (SRI) is shown in Figure I-1. If it is assumed that the impedance of the output capacitor (C_O) reflected at the primary of the output transformer (T) is much less than the impedance of the series resonant capacitor (C), then the output voltage reflects into the series resonant tank as a dc voltage (V_{OR}). The polarity of V_{OR} will be positive for positive current flow in the tank circuit (L, C, and T), as shown in Figure I-1, and negative for negative current flow in the tank circuit, as shown in Figure I-2.

The current (i) during the time that Q_1 and Q_4 are conducting (Figures I-1 and I-3) will be:

$$i(t_0<t<t_1) = \sqrt{\frac{C}{L}}\,[V_S - V_C(t_0) - V_{OR}]\sin \omega t + i(t_0)\cos \omega t \quad \text{(I-1)}$$

where V_S is the source voltage, $V_C(t_O)$ is the voltage on capacitor C at $t = t_O$, V_{OR} is the reflected output voltage, $i(t_O)$ is the current in the tank circuit at $t = t_O$, and ω is the resonant frequency.

At $t = t_1$, any excess energy in the tank will be returned to the source through diodes D_1 and D_4 (Figures I-2 and I-3). At this time, the current will be

$$i(t_1<t<t_2) = \sqrt{\frac{C}{L}}\,[V_S - V_C(t_1) + V_{OR}]\sin \omega t\,. \quad \text{(I-2)}$$

During this time interval, V_{OR} is negative, and the current in the tank circuit at $t = t_1$ is zero. For steady-state

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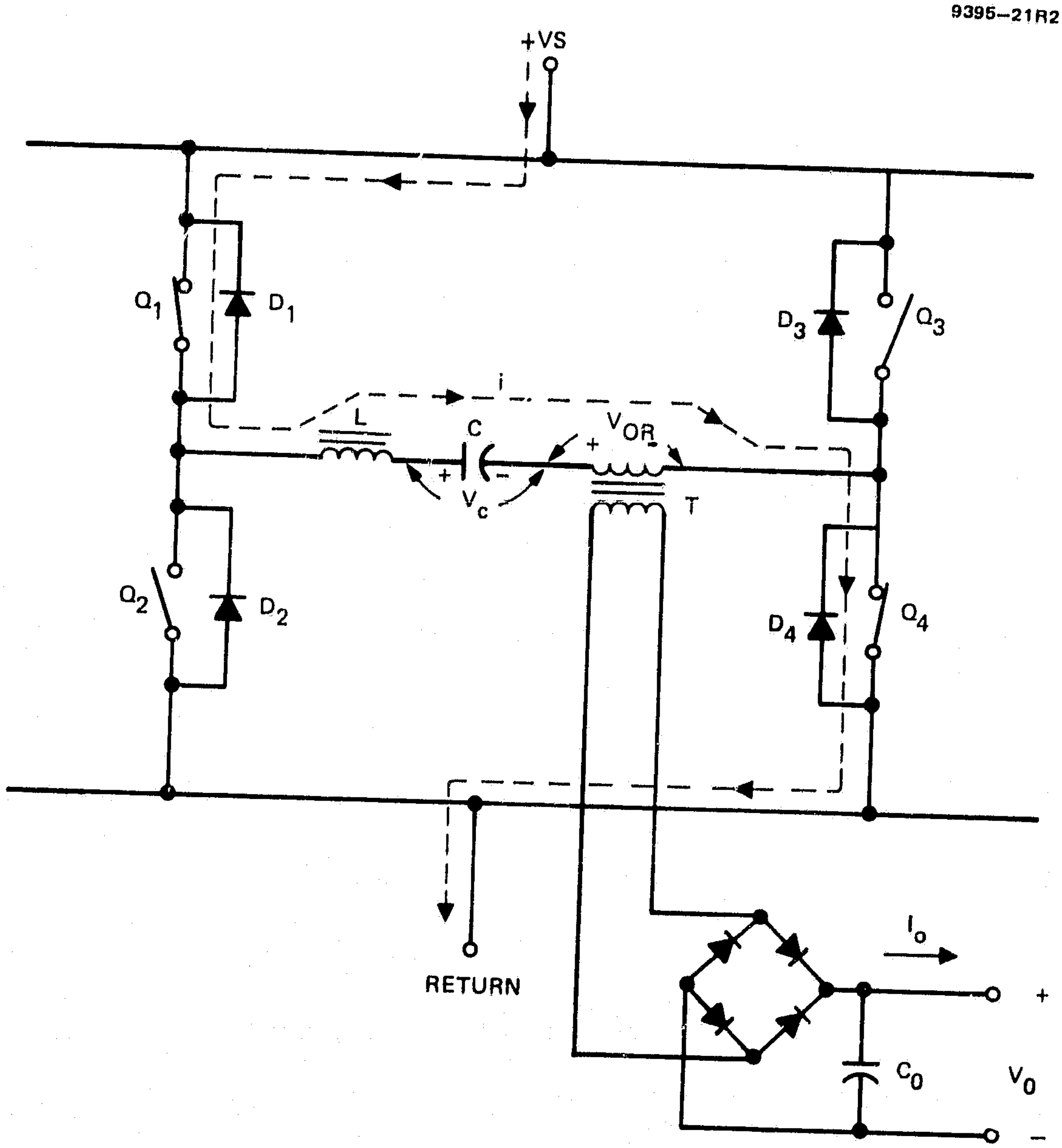

Figure I-1. Current flow (i) in the SRI during the time Q_1 and Q_4 are conducting.

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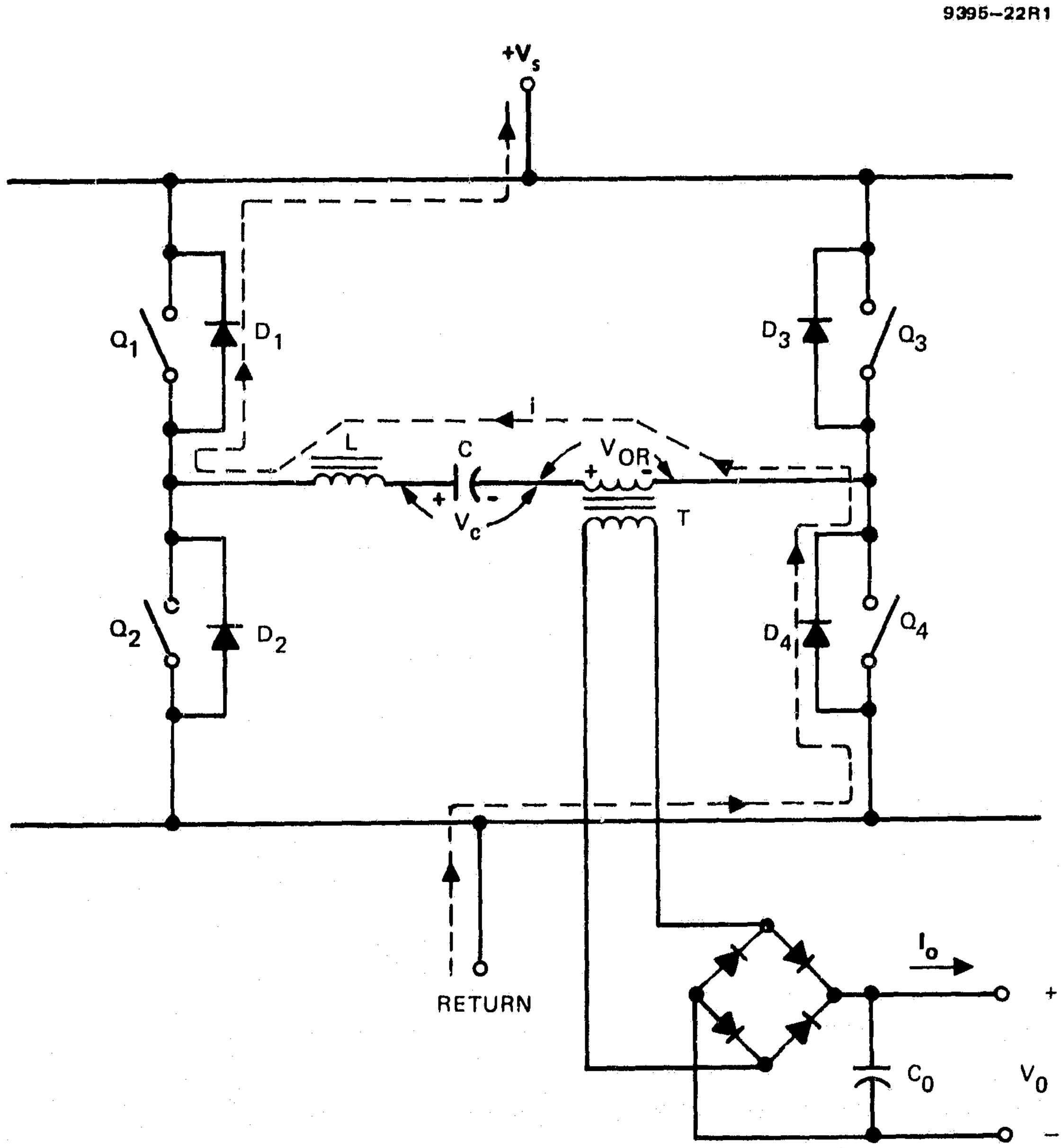
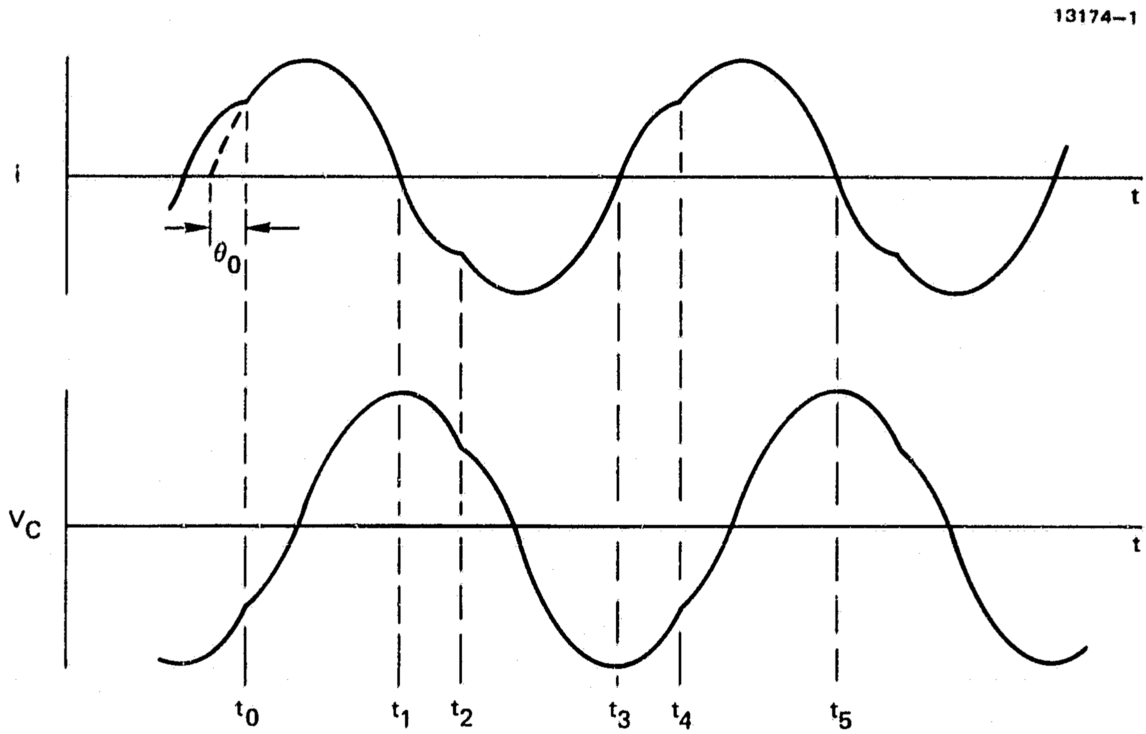


Figure I-2. Current flow (i) in the SRI during the time D_1 and D_4 are conducting.



$t_0 \leq t \leq t_1$ – Q1 AND Q4 CONDUCTING

$t_1 \leq t \leq t_2$ – D1 AND D4 CONDUCTING

$t_2 \leq t \leq t_3$ – Q2 AND Q3 CONDUCTING

$t_3 \leq t \leq t_4$ – D2 AND D3 CONDUCTING

$t_4 \leq t \leq t_5$ – Q1 AND Q4 CONDUCTING

Figure I-3. Tank current and resonant capacitor voltage waveforms for the circuit of Figure I-1.

operating conditions, the current during time interval $t_2 < t < t_3$ (Figure I-3 and I-4) is

$$i(t_2 < t < t_3) = -i(t_0 < t < t_1) \quad . \tag{I-3}$$

The current during the time interval $t_3 < t < t_4$ (Figures I-3 and I-5) is

$$i(t_3 < t < t_4) = -i(t_1 < t < t_2) \tag{I-4}$$

and

$$i(t_4 < t < t_5) = i(t_0 < t < t_1) \quad . \tag{I-5}$$

The voltage across the capacitor C will be

$$V_C = \frac{1}{C} \int i \, dt \quad , \tag{I-6}$$

$$V_C(t_0 < t < t_1) = \frac{1}{C} \int i(t_0 < t < t_1) dt \quad , \tag{I-7}$$

$$\begin{aligned} V_C(t_0 < t < t_1) &= -[V_S - V_C(t_0) - V_{OR}] \cos \omega t \\ &+ \frac{i(t_0)}{\omega C} \sin \omega t + V_S - V_{OR} \quad , \end{aligned} \tag{I-8}$$

$$V_C(t_1 < t < t_2) = -[V_S - V_C(t_1) + V_{OR}] \cos \omega t + V_S + V_{OR} , \tag{I-9}$$

$$V_C(t_2 < t < t_3) = -V_C(t_0 < t < t_1) \quad , \tag{I-10}$$

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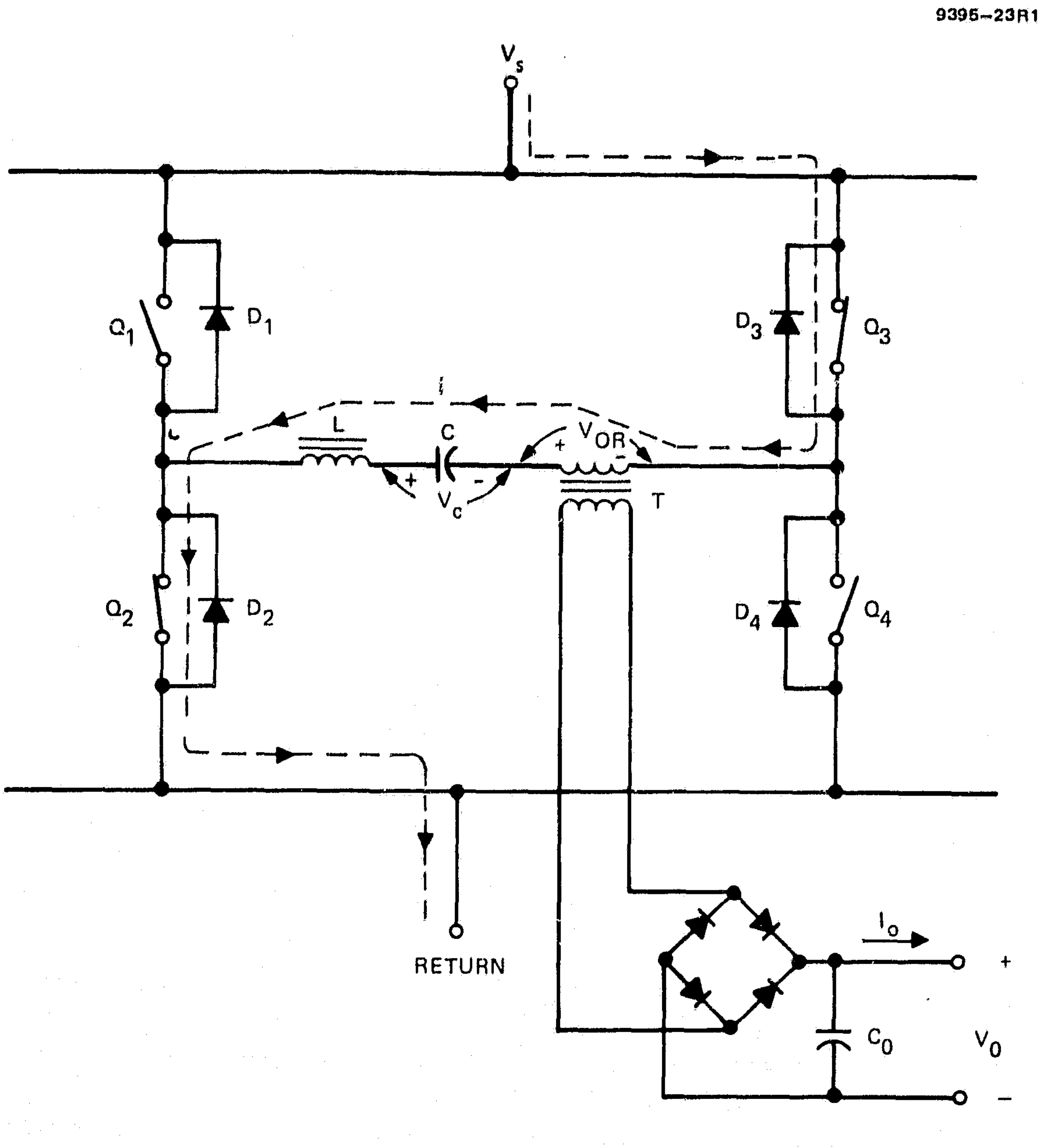

Figure I-4. Current flow (i) in the SRI during the time Q_2 and Q_3 are conducting.

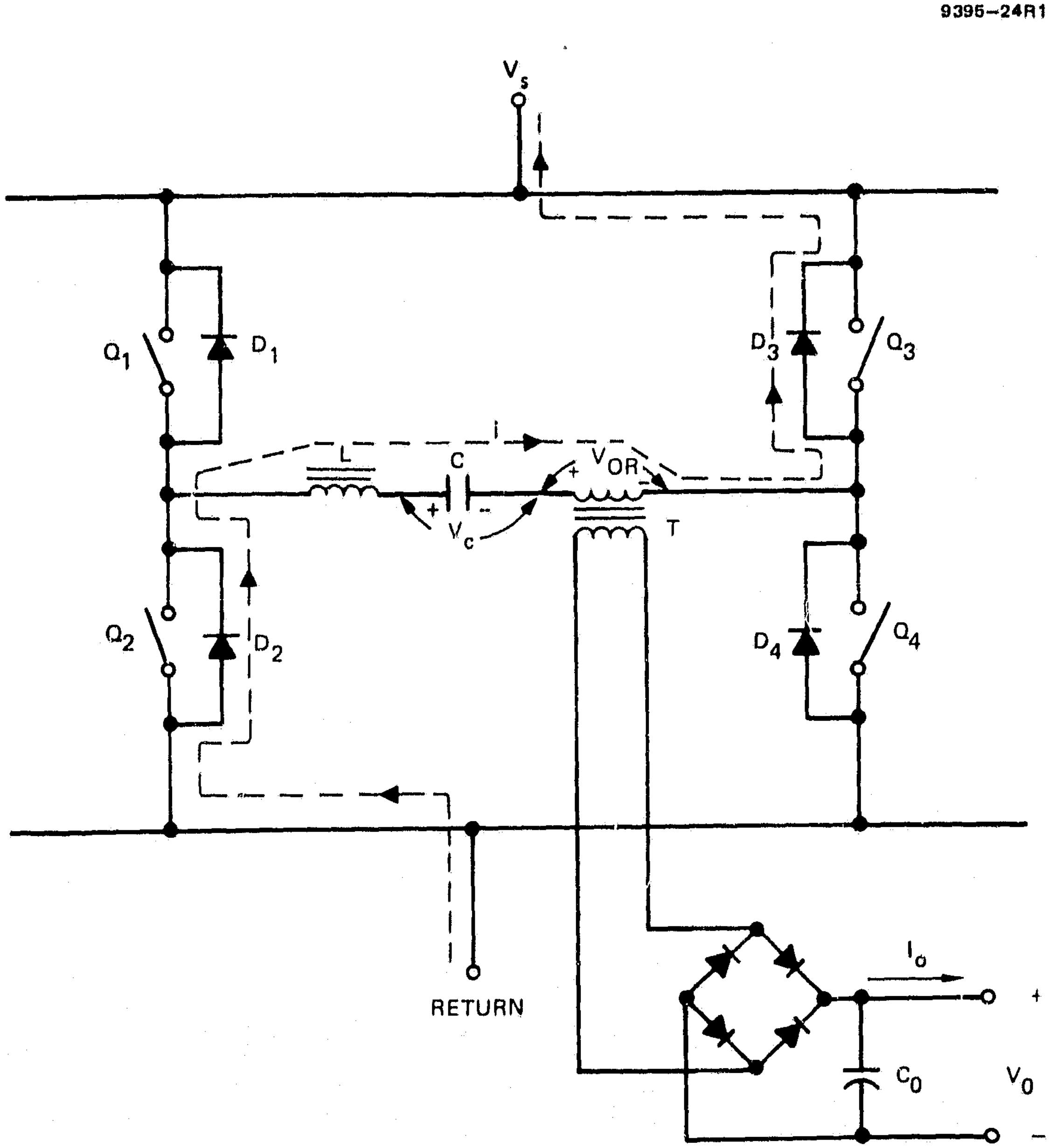

Figure I-5. Current flow (i) in the SRI during the time D_2 and D_3 are conducting.

and

$$V_C(t_3<t<t_4) = -V_C(t_1<t<t_2) \quad . \qquad \text{(I-11)}$$

From Equations (I-2) and (I-3):

$$i(t_o) = -\sqrt{\frac{C}{L}}\ [V_S - V_C(t_1) + V_{OR}] \sin \omega(t_2 - t_1). \qquad \text{(I-12)}$$

From Equations (I-9) and (I-11):

$$V_C(t_0) = [V_S - V_C(t_1) + V_{OR}] \cos \omega(t_2 - t_1) - (V_S + V_{OR}) \ . \qquad \text{(I-13)}$$

From Equation (I-1) (See Figure I-3):

$$\theta_o = \tan^{-1} \frac{I(t_0)}{\sqrt{\frac{C}{L}}\ [V_S - V_C(t_0) - V_{OR}]} \quad . \qquad \text{(I-14)}$$

And from Equation (I-8):

$$V_C(t_1) = -[V_S - V_C(t_0) - V_{OR}] \cos (\pi - \theta_o) + \frac{i(t_0)}{\omega C} \sin (\pi - \theta_o) + (V_S - V_{OR}) \quad . \qquad \text{(I-15)}$$

Equations (I-12) through (I-15) contain transcendental functions with the four unknowns, $i(t_O)$, $V_C(t_O)$, θ_O, and $V_C(t_1)$, equal to the number of equations. All other terms in the equations are fixed by the operating conditions for which a solution to these equations is desired.

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Hughes has developed a specialized computer program to solve these equations. Once the unknowns have been determined, Equation (I-1) can be solved for the peak current (i_p) in the tank circuit under a given set of steady state operating conditions:

$$i_p = i(\pi/2-\theta_o) = \sqrt{\frac{C}{L}}\,\lfloor V_S - V_C(t_0) - V_{OR}\rfloor \sin(\pi/2-\theta_o) \tag{I-16}$$

$$+ \, i(t_0)\cos(\pi/2-\theta_o) \quad .$$

The voltage across the inductor (V_L) can be calculated from:

$$V_L = L\frac{di}{dt} \quad . \tag{I-17}$$

We now have a set of equations (and a solution) that describes all the voltages and currents in the series-resonant tank circuit.

Table I-1 is a copy of the computer printout listing the values of i(t) for different values of ωt. Figure I-6, which is a plot of these values of i(t) versus ωt, shows the steady-state current waveform in the tank circuit for the following conditions:

V_S	=	250V
V_{OR}	=	237.5V
$t_2 - t_1$ (Figure I-3)	=	0.628 rad
C	=	2.43 μF
L	=	26.06 μH
f	=	20 kHz.

Table I-1. Computer Listing of Values of i(t) for Different Values of ωt

	ωt, rad.	i(t), A
J,P,I = 1	0.00	31.1
J,P,I = 2	0.30	87.2
J,P,I = 3	0.60	135.6
J,P,I = 4	0.90	172.0
J,P,I = 5	1.19	193.2
J,P,I = 6	1.49	197.4
J,P,I = 7	1.79	184.1
J,P,I = 8	2.09	154.5
J,P,I = 9	2.39	111.3
J,P,I = 10	2.69	58.2
J,P,I = 11	2.98	0.0
J,P,I = 12	3.05	-3.3
J,P,I = 13	3.11	-6.6
J,P,I = 14	3.17	-9.9
J,P,I = 15	3.24	-13.2
J,P,I = 16	3.30	-16.3
J,P,I = 17	3.36	-19.5
J,P,I = 18	3.42	-22.5
J,P,I = 19	3.49	-25.5
J,P,I = 20	3.55	-28.3
J,P,I = 21	3.61	-31.1
J,P,I = 22	3.91	-87.2
J,P,I = 23	4.21	-135.6
J,P,I = 24	4.51	-172.0
J,P,I = 25	4.81	-193.2
J,P,I = 26	5.10	-197.4
J,P,I = 27	5.40	-184.1
J,P,I = 28	5.70	-154.5
J,P,I = 29	6.00	-111.3
J,P,I = 30	6.30	-58.2
J,P,I = 31	6.60	0.0
J,P,I = 32	6.66	3.3
J,P,I = 33	6.72	6.6
J,P,I = 34	6.78	9.9
J,P,I = 35	6.85	13.2
J,P,I = 36	6.91	16.3
J,P,I = 37	6.97	19.5
J,P,I = 38	7.04	22.5
J,P,I = 39	7.10	25.5
J,P,I = 40	7.16	28.3
J,P,I = 41	7.22	31.1
STOP		

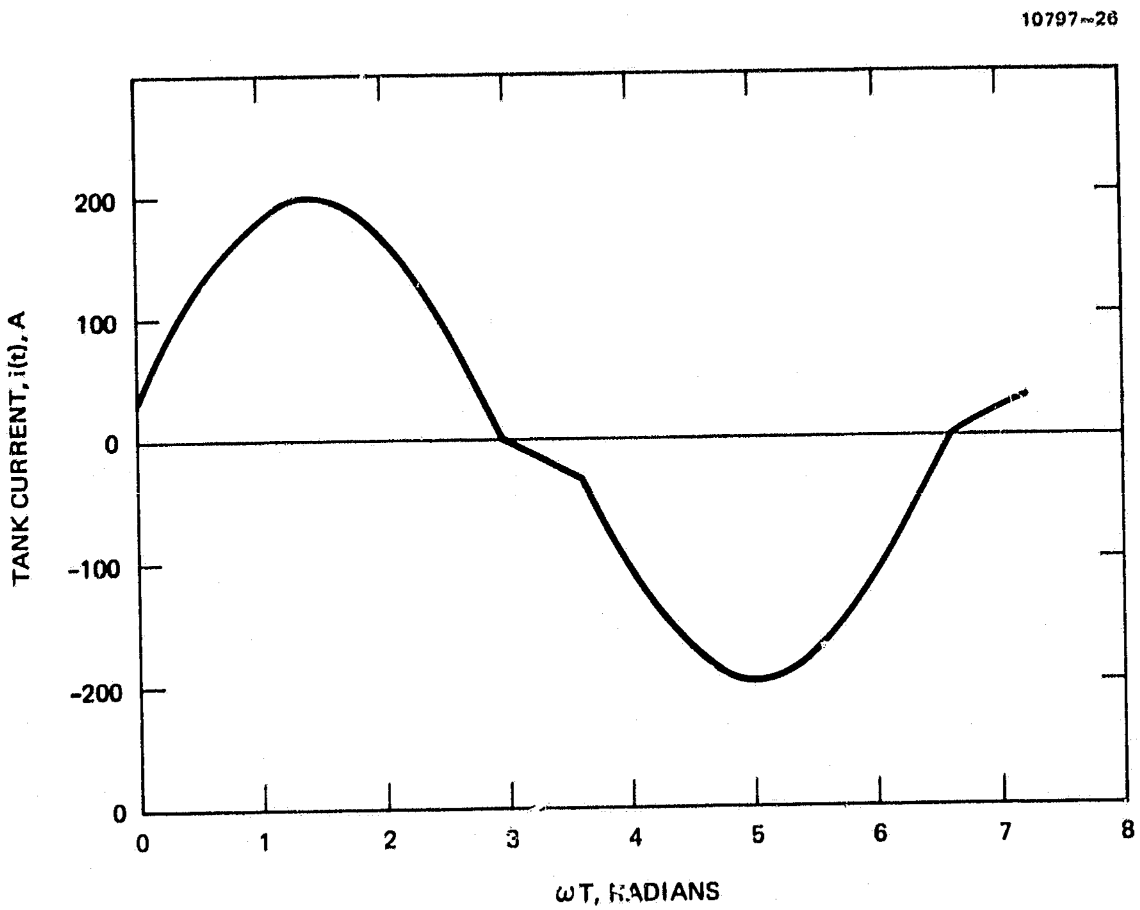

Figure I-6. Plot of i(t) versus ωt for an SRI. (Data plotted from Table I-1.)

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Thomas Stuart of the University of Toledo[I-1,I-2] has developed a closed form solution for this same set of equations which can also be used for the analysis and design of SRIs.

Equation (I-1) states that

$$i = \sqrt{\frac{C}{L}} \left[V_S - V_C(t_0) - V_{OR} \right] \sin \omega t + i(t_0) \cos \omega t \,, \qquad \text{(I-18)}$$

for $0 < t < \pi$. This shows that the current waveform in the switch is a half-sine wave pulse, with an initial step-rise in current on the leading edge of $i(t_0)$ (the current flowing in the commutating diode at the time the transistor is turned on). This sine-wave current is the major advantage of series-resonant inverters as compared to squarewave inverters, since it permits the switch to turn on at lower currents and off under zero-current conditions, thereby reducing the stresses and switching losses in these switches.

The output power of the inverter is $V_O \times I_O$ (see Figure I-1) where V_O reflects back to the primary of the transformer T by the turns ratio, N_P/N_S. Thus,

$$V_{OR} = \frac{N_P}{N_S} V_O \,, \qquad \text{(I-19)}$$

where V_{OR} is the reflected voltage. V_{OR} must be less than source voltage, V_S, if series-resonant action is to occur; a value of $V_{OR} = 0.95\ V_S$ is chosen to allow for some margin in the design and still utilize most of the source voltage. Then,

$$0.95\ V_S = \frac{N_P}{N_S} V_O \,, \qquad \text{(I-20)}$$

or

$$\frac{N_S}{N_P} = \frac{V_O}{0.95\ V_S} , \tag{I-21}$$

where V_O is the maximum output voltage desired, and V_S is the lowest operating source voltage.

With the turns ratio of the transformer defined, the average current in the primary of the transformer (which is also the average current in the tank circuit) is

$$I_{avg} = \frac{N_S}{N_P} I_O = \frac{V_O \times I_O}{0.95\ V_S} \tag{I-22}$$

$$I_{avg} = \frac{Po}{0.95\ V_S} \tag{I-23}$$

If the tank current is a pure sine wave (100 % duty cycle), then $I_{avg} = 0.637\ i_P$, where i_P, the peak value of the sine wave current, is

$$i_P = \frac{P_O}{0.637 \times 0.95\ V_S} . \tag{I-24}$$

Since the inverter cannot operate at 100% duty cycle because of the turn-on and turn-off times of the switches, the tank current cannot be a pure sine wave, and the peak current will have to be higher than this value. How much higher will depend on the turn-on and turn-off times of the switches, and also on the operating frequency; however, 20% is a reasonable assumption.

The choice of L and C determines the resonant frequency of the series-resonant tank, and also affects the peak current in the tank. The resonant frequency for a tank circuit is

$$f = \frac{1}{2\pi \sqrt{LC}} \quad . \tag{I-25}$$

Once the resonant frequency of operation has been chosen, this equation relates C to L as

$$C = \frac{1}{(2\pi f)^2 L} = \frac{1}{\omega^2 L} \quad . \tag{I-26}$$

The leakage inductance of the output transformer (T) in Figure I-1 must be added to the inductance of the inductor (L) to obtain an equivalent inductance (L_E) for the circuit, and

$$C = \frac{1}{\omega^2 L_E} \text{ and } L_E = \frac{1}{\omega^2 C} \quad . \tag{I-27}$$

From Equations (I-1) and (I-12) it follows that

$$i = \sqrt{\frac{C}{L}}\ A \sin \omega t + \sqrt{\frac{C}{L}}\ B \cos \omega t \quad , \tag{I-28}$$

where

$$A = [V_S - V_C(t_0) - V_{OR}] \quad , \tag{I-29}$$

$$B = -[V_S - V_C(t_1) + V_{OR}] \sin \omega(t_2 - t_1) \quad , \qquad \text{(I-30)}$$

and

$$i = \sqrt{\frac{C}{L}} \, (A \sin \omega t + B \cos \omega t) \quad . \qquad \text{(I-31)}$$

It can be seen that i (the current in the tank circuit) is directly proportional to $\sqrt{C/L}$, where L is again L_E. Since $\sqrt{C/L} = \omega C$, it can be seen that i is also directly proportional to C. Therefore, C is chosen to provide a peak tank current large enough to produce the desired output power. Excess current in the tank contributes to losses and is therefore undesirable.

SRIs are controlled by modulating the repetition rate (frequency modulation) at which the switches in the bridge circuit are commanded to turn-on. Each command results in a half-sinusoid current pulse of the resonant tank at its natural frequency. The repetition rate varies from near zero for open-circuit-output conditions to approximately 85% of the resonant frequency (determined by the turn-on and turn-off time of the switch being employed) under full-load conditions. The parameter that is actually controlled in this manner is the average current in the tank circuit. Figure I-7 shows how the normalized average tank current varies as a function of the ratio of the modulation frequency to the resonant frequency (f_m/f_r). Curves are shown for two values of q where

$$q = \frac{V_{OR}}{V_S} \quad . \qquad \text{(I-32)}$$

The curves in Figures I-7, I-8, and I-9 were normalized to unity for q = 0.95 and f_m/f_r = 0.5.

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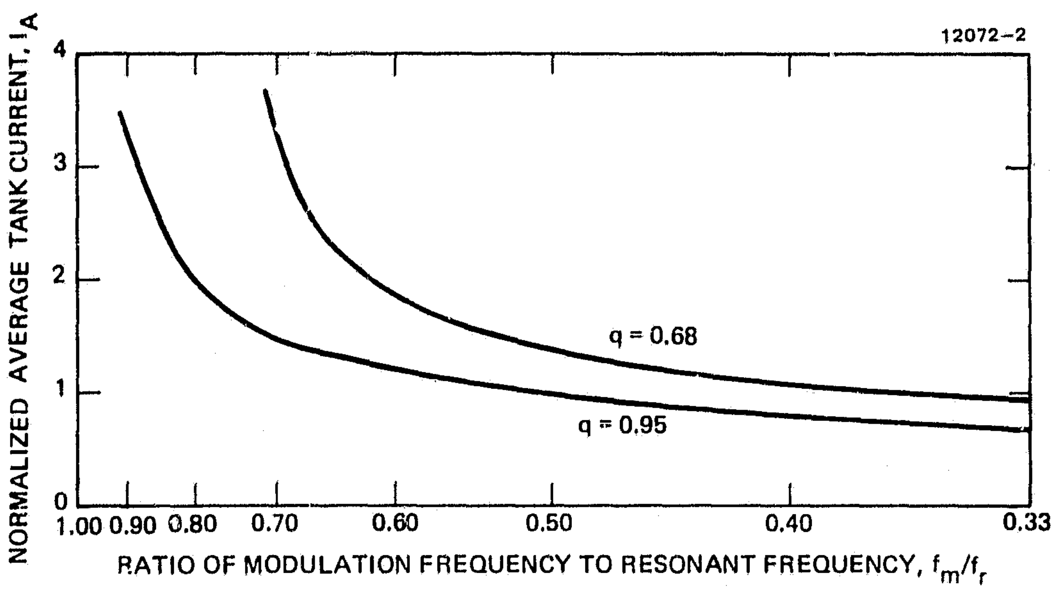

Figure I-7. Normalized average tank current versus the ratio of modulation frequency to resonant frequency.

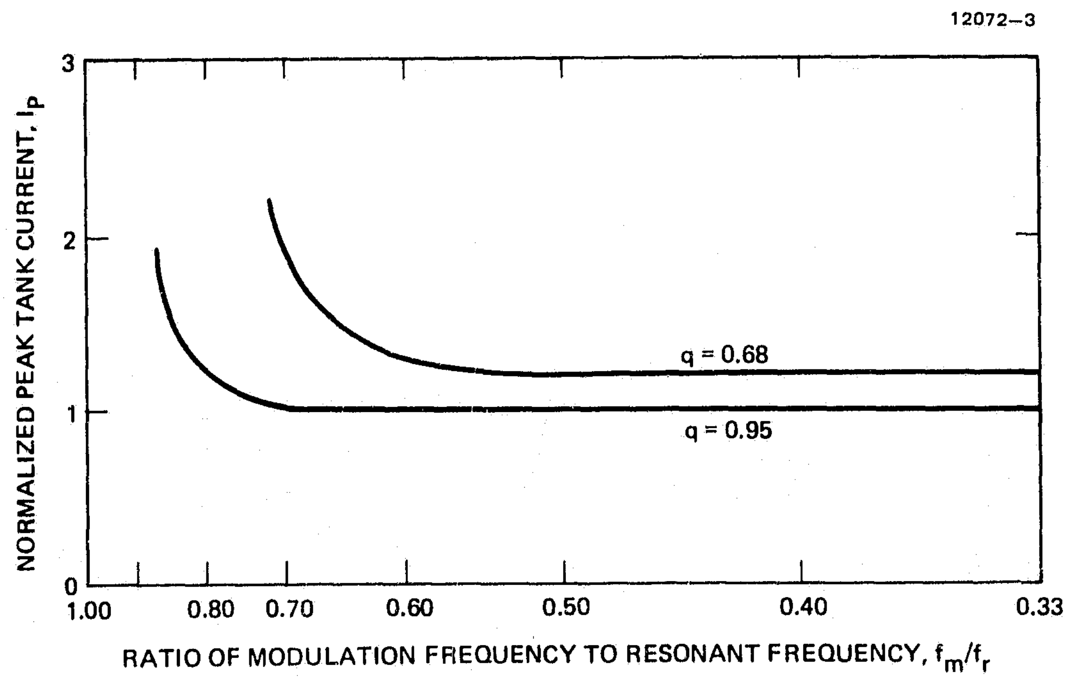

Figure I-8. Normalized peak tank current versus the ratio of modulation frequency to resonant frequency.

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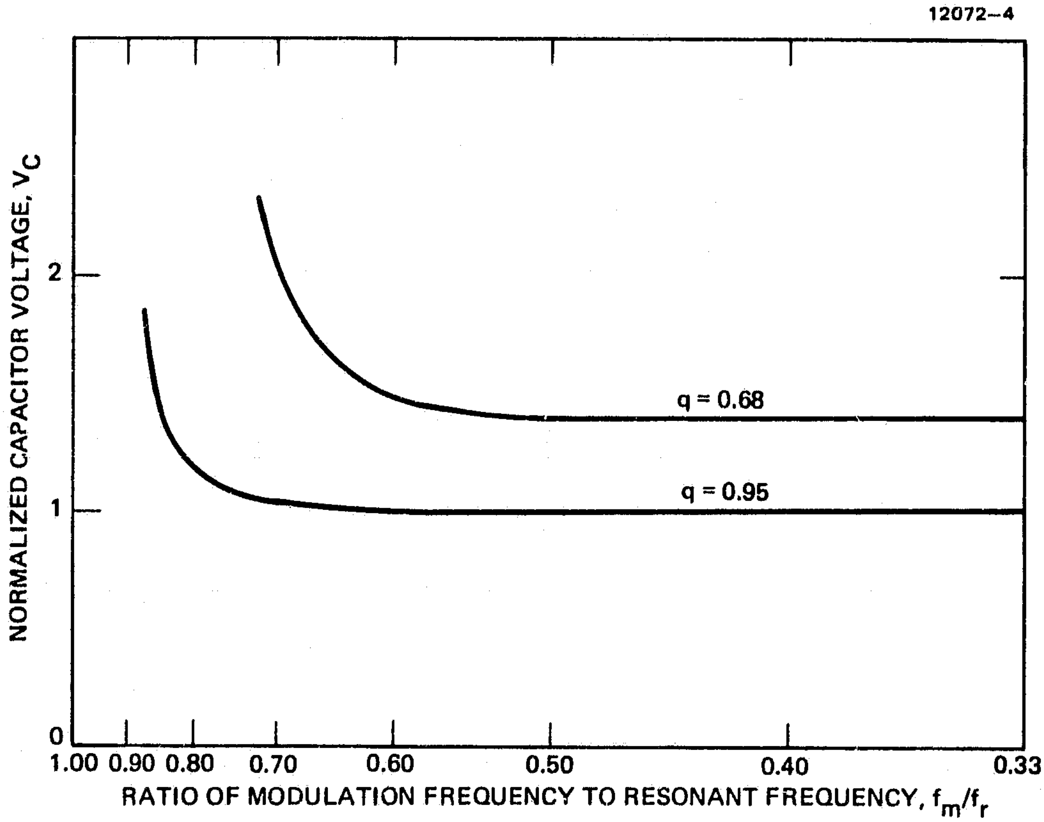

Figure I-9. Normalized resonant capacitor voltage versus the ratio of modulation frequency to resonant frequency.

Figures I-8 and I-9 show how the normalized peak tank current and resonant capacitor voltage, respectively, vary with f_m/f_r. As can be seen from these figures, the peak tank current and resonant capacitor voltage both increase sharply as f_m/f_r approaches unity. It can also be seen that for lower values of q the sharp increase occurs at lower values of f_m/f_r; therefore, if the inverter is operating at a high power level and q suddenly drops due to a change in the load or an output short circuit, the control circuit must immediately lower the f_m/f_r ratio in order to prevent the peak tank current and resonant capacitor voltage from rising to destructive levels. The control circuit must also keep the time periods balanced from turning on one set of switches in the bridge to turning on the next set of switches (approximately square-wave) in order to keep the power balanced between each set of switches. If the times are not balanced, one set of switches can carry most of the power and be overstressed. The control circuit must also guarantee that the set of switches on one side of the bridge (say Q1 and Q4) are turned off before the set of switches on the other side of the bridge (Q2 and Q3) are turned on. If both sets are allowed to be on at the same time, a fault (shorted condition) will develop across the power source.

The control technique that Hughes has found to be optimal for control of SRIs is the use of a voltage-controlled-oscillator (VCO) or voltage-to-frequency converter (V/F). Under steady-state conditions, this control technique turns the switches in opposite sides of the bridge ON and OFF, using a square-wave signal. The use of a square-wave signal guarantees that each side of the bridge is ON for the same amount of time, keeping the current in the tank, the current in all of the transistor switches, the voltage across the series-resonant capacitor, and the flux in the transformer balanced from one half-cycle to the next. This technique results in a simpler and much more stable system than the control technique used in the functional model power processors (FM/PPUs)[I-3] where the time to turn ON the other side of the bridge is determined on a half-cycle basis.

REFERENCES

I-1. R.J. King and T.A. Stuart, "A Normalized Model for the Half Bridge Series Resonant Converter," IEEE Transactions on Aerospace and Electronic Systems, AES-17, 2, 190-198 (March 1981).

I-2. R.J. King and T.A. Stuart, "Modeling the Full-Bridge Series-Resonant Power Converter," IEEE Transactions on Aerospace and Electronic Systems, AES-18, No. 4, 449-459 (July 1982).

I-3. R.R. Lowell, et al., 30-Centimeter Ion Thruster Subsystem Design Manual, NASA TM 79191, Section 6, June 1979.