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Grant No. NAG-3-316-1

CARRIER RECOVERY METHODS FOR A DUAL-MODE MODEM: A DESIGN APPROACH

Submitted to:

NASA/Lewis Research Center
21000 Brookpark Road
Cleveland, OH 44135

Attention: Dr. Dennis J. Connolly
Solid State Devices and Passive Components Section

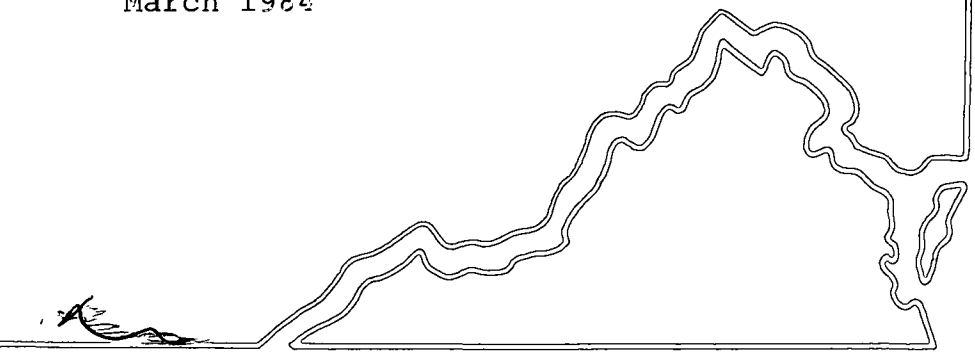
Submitted by:

Charles W. Richards, IV
Graduate Research Assistant

Stephen G. Wilson
Professor

Report No. UVA/528219/EE84/102

March 1984



UNIVERSITY OF VIRGINIA

COMMUNICATIONS SYSTEMS LABORATORY
DEPARTMENT OF ELECTRICAL ENGINEERING
SCHOOL OF ENGINEERING AND APPLIED SCIENCES
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CHARLOTTESVILLE, VIRGINIA

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PREFACE

This report constitutes the Master of Science thesis of Charles W. Richards at the University of Virginia. The work was performed under NASA Contract NAG-3-316, and supervised by Professor Stephen G. Wilson.

CARRIER RECOVERY METHODS FOR A DUAL-MODE MODEM

A DESIGN APPROACH

ABSTRACT

Multimode modulation schemes in a single modem appear to be desirable in digital telecommunication systems, due to the ability to exploit either energy or bandwidth efficiency. The application of a coherent, quadrature phase shift keying (QPSK) modulation scheme provides energy efficiency while a coherent, 16-quadrature amplitude shift keying (16-QASK) scheme provides better use of bandwidth with some degradation in energy efficiency. The selectable use of either QPSK or 16-QASK modulation within a single modem provides the option of exploiting either energy or bandwidth efficiency.

This research deals with a dual mode modem with selectable QPSK or 16-QASK modulation schemes. The theoretical reasoning as well as the practical trade-offs made during the development of a modem are presented, with attention given to the carrier recovery method used for coherent demodulation. Particular attention is given to carrier recovery methods that can provide little degradation due to phase error for both QPSK and 16-QASK, while being insensitive to the amplitude characteristic of

a 16-QASK modulation scheme.

A computer analysis of the degradation in symbol error rate (SER) for QPSK and 16-QASK due to phase error is presented. Results find that an energy increase of roughly 4 dB is needed to maintain a SER of $1X10^{-5}$ for QPSK with 20° of phase error and 16-QASK with 7° phase error.

A hardware implementation of a selectable dual mode, QPSK or 16-QASK modem is presented. The dual mode modem operates at a carrier frequency of 10 MHz and at a fixed symbol rate of $500X10^{3}$ symbols per second. The carrier recovery method used is a decision feedback type, does not require bit timing, and is capable of either two-level decisions (QPSK) or four-level decisions (16-QASK). The implemented modem is designed based on results from research on high speed (1 gibabit/sec.) modems and is easily scaled up to a higher carrier frequency and/or symbol rate.

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LIST OF SYMBOLS

a	product of data estimates and data
b	product of data estimates and data
B_L	loop bandwidth
dB	decibel
$\hat{d}$	estimates
$d_{\hat{I}}$	data with amplitude = $\pm A$
d_{dis}	minimum distance
$\overline{E_b}$	average bit energy
E_s	symbol energy
$\overline{E_s}$	average symbol energy
e(t)	error signal
F(s)	filter transfer function
g(θ)	S-curve
H(s)	loop transfer function
j(t)	pattern jitter
K	gain constant
$n_c(t)$	in-phase noise
N_o	noise spectral density
nq(t)	quadrature-phase noise
$\Phi_i(t)$	basis function
R_b	bit rate
R_s	symbol rate
S_o	signal of constellation
τ	time constant

LIST OF SYMBOLS CONTINUED

T_b	bit duration
T_s	symbol duration
σ^2	phase error variance
θ	phase error
θ_i	phase input
θ_o	phase output
ω_{acq}	acquistion range
ω_c	carrier frequency
$\omega hold$	hold-in range
ζ	damping coefficient

CHAPTER ONE

INTRODUCTION

In digital telecommunication systems there are three parameters which are the constraining factors: energy efficiency, bandwidth efficiency and equipment complexity. There often occurs a compromise between the energy and bandwidth parameters, wherein the system is optimized for one specific application. However, a present trend in modern telecommunication systems is towards flexibility or adaptability. There is a desire for multimode systems that can be optimized for many applications. This paper discusses such a system, showing the theoretical reasoning as well as the practical trade-offs taken during the development of such a system.

Two of the more practical modulation schemes, especially in terms of combined implementation are quadrature phase shift keying (QPSK) and 16-ary quadrature amplitude shift keying (16-QASK). A QPSK scheme provides efficient use of energy while the 16-QASK scheme provides better use of bandwidth with some degradation in energy efficiency. The combined use of these two modulation schemes in a selectable coherent configuration within a single modem is easily achieved [1]. A system of this nature provides the option of either energy or

bandwidth efficiency and is easily implemented through the combined use of generic, QPSK building blocks.

We shall investigate the general design of a coherent dual-mode (QPSK OR 16-QASK) modem with a significant portion of the paper dedicated to the investigation and design of a carrier recovery method. In any coherent modulation scheme one of the critical aspects is carrier synchronization. Not only is there a need to have accurate carrier tracking to within a few degrees of phase angle difference between receiver and incoming signal, in order to maintain a reasonable symbol error rate (SER), but also a desire for operation with two signal constellations. Due to these constraints, it is reasonable to center the research on the important issue of carrier recovery for a dual-mode system.

This thesis is organized into six chapters with background material covering energy efficiency, bandwidth efficiency and probability of error characteristics of both QPSK and 16-QASK given in Chapter Two. Next the causes of phase errors and the degradation to the SER occurred by a fixed phase error for both coherent QPSK and 16-QASK are investigated in Chapter Three. In the following chapter, the concepts of crosstalk and pattern jitter are investigated followed by a discussion of the effect pattern jitter has on carrier recovery accuracy. Several methods that can be implemented to perform accurate carrier recovery are

listed, and the reasons for the choice of a decision feedback method as a means for carrier synchronization for a dual-mode modem are given.

Chapter Four also describes in detail the decision feedback method of carrier recovery and an analysis is presented for both QPSK and 16-QASK modulation schemes. In Chapter Five a detailed design for an actual hardware implementation of a selectable dual-mode, QPSK or 16-QASK, modem is presented. The modem operates at a carrier frequency of 10 MHZ and at a fixed symbol rate of 500×10^3 symbols per second. The carrier recovery method used is a decision feedback type. It does not require bit timing, and is capable of either two-level decisions (QPSK) or four-level decisions (16-QASK). The entire modem is designed based on results from research on high speed (1 gigabit/sec.) modems and is easily scaled up to a higher carrier frequency and/or symbol rate.

From this design a prototype was constructed with test results contained in Chapter Six. These results show the successful operation of the decision feedback technique of carrier recovery. Also in this final chapter is a discussion of possible design improvements and methods to overcome carrier lock ambiguity.

CHAPTER TWO

BACKGROUND

This chapter provides the necessary background to cover the methods and techniques that are commonly used to describe digital signals, particularly QPSK and 16-QASK signalling schemes. Energy efficiency, and bandwidth efficiency, for both QPSK and 16-QASK are investigated and a comparison between the two modulation techniques will be made.

2.1 Signal Representation

Convenient functions that are commonly used to form orthonormal basis are sinusoids whose frequencies are at a common carrier frequency. The orthonormal bases are then combined to form a general signal that is represented by:

$$S_i(t) = k(a_i \cos\omega_c t + b_i \sin\omega_c t) \qquad i = 0,1...M-1 \qquad (2.1)$$

a_i and b_i are the basis coordinates of the i th signal and are actually the data that is contained in the $s_i(t)$ signal. The collection of coordinates (a_i, b_i) are the signal points of the signal constellation. The usual constellations for the two cases of interest are QPSK (M=4)

and 16-QASK (M=16), shown in Figure 2.1. Note that a_i and b_i do not have to be of the same magnitude, e.g. 16-QASK causes the signal constellation to have an amplitude characteristic as well as a phase characteristic.

The time-domain form of a QPSK signal at the receiver is expressed as:

$$r(t) = \sqrt{2}(d_1(t)\cos\omega_c t + d_2(t)\sin\omega_c t) + n(t) \qquad (2.2)$$

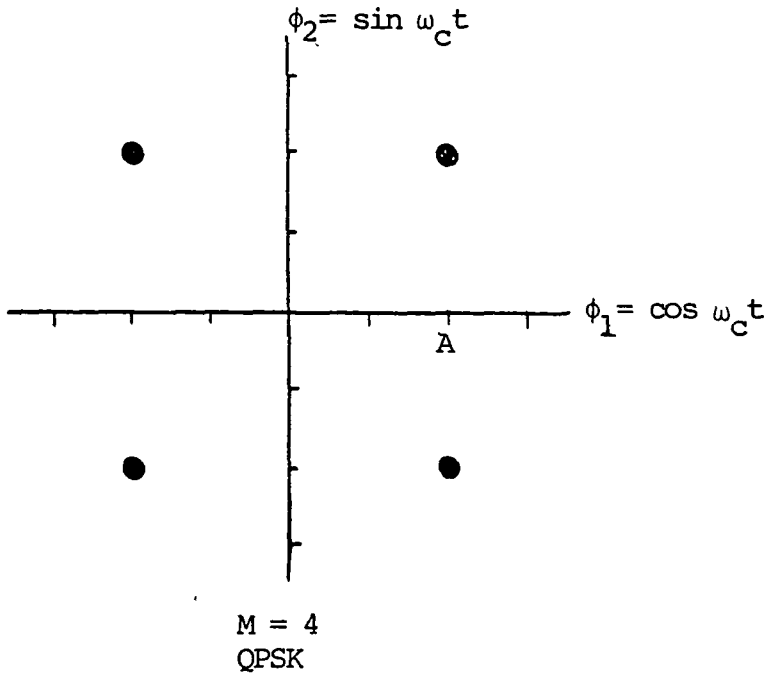
where the data $d_1(t)$ and $d_2(t) = \pm A$, and the noise component n(t) is assumed to be Gaussian noise with a two-sided spectral density $N_o/2$ $^{W}/_{Hz}$. The time-domain form of 16-QASK is of the form:

$$r(t) = \sqrt{2}(d_1(t)\cos\omega_c t + d_2(t)\sin\omega_c t) + \sqrt{2}/2(d_3(t)\cos\omega_c t + d_4(t)\cos\omega_c t) + n(t) \qquad (2.3)$$

and the noise is assumed white Gaussian (AWGN) as described above.

2.2 General Modem Configuration

A general configuration for a modem using a quadrature-modulation technique is shown in Figure 2.2. The necessary synchronization hardware is omitted at this point and is covered later in detail in Chapter Four. The operation of the modulator and demodulator for both QPSK and 16-QASK is similar. The modulator is fed a serial



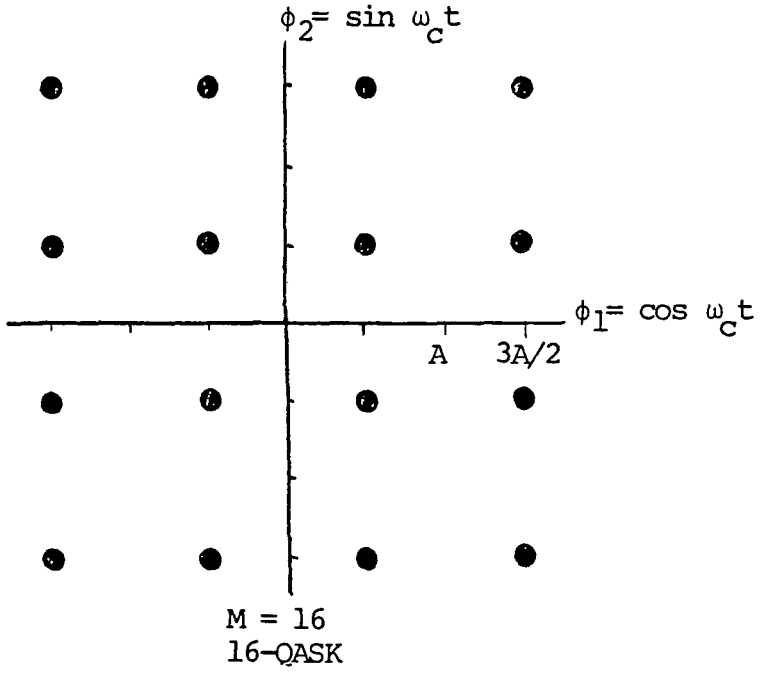
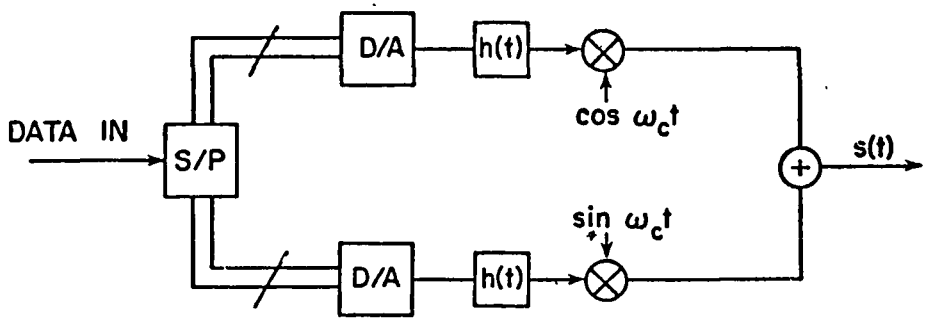
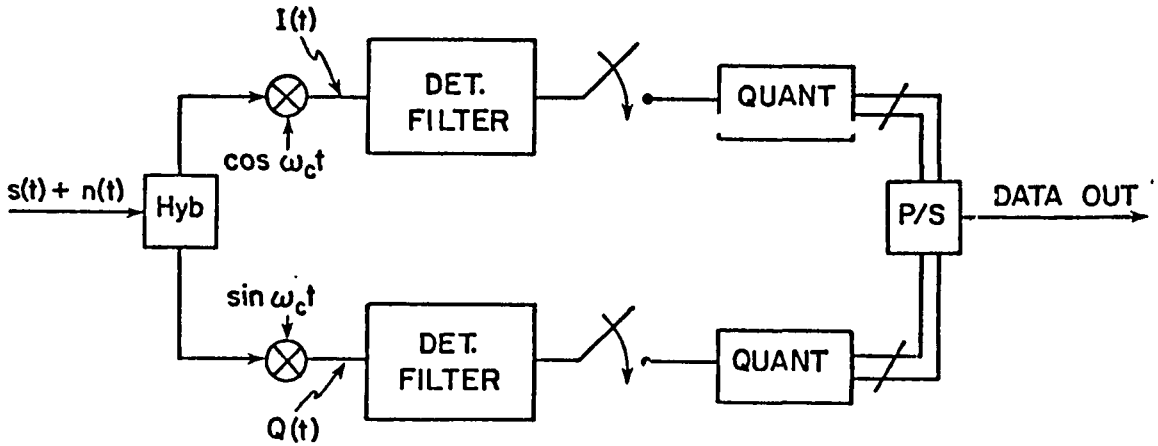


Figure 2.1 QPSK and 16-QASK Signal Constellations



Modulator



Demodulator

Figure 2.2 Block Diagram Of Basic Modem

digital data stream from the data source and a series to parallel conversion is performed. Next the parallel digital data is converted to an analog form and this analog signal may pass through an optional spectrum shaping filter (h(t)) if desired. At this point the parallel analog signals act as coefficients. The coefficients are mapped onto the set of basis functions ($\sin\omega_c t$ and $\cos\omega_c t$) and combined to generate the signal s(t). The signal s(t) then travels through a channel where it may be attenuated and/or distorted and noise n(t) is added. The signal corrupted by the channel is renamed r(t).

At the demodulator the signal is r(t) is received and split into two signals by a "hybrid." These two signals are then quadrature demodulated and filtered by the detection filters. This combined operation of demodulation and filtering act as a correlation between the received signal r(t) and the set of basis functions. Through the comparison of the correlated signal to a set of decision boundaries that partition the signal space of all the possible signals that can be sent, the signal coefficients are extracted from the signal r(t). Gaussian noise perturbs the sent signal in a circular-symmetric manner but only the component of noise that moves the signal in a perpendicular direction towards the decision boundary is harmful.

The output of the detection filter is sampled and a

decision is made by the quantizer on the sampled signal using the above criterion. The quantized decisions are then parallel-to-series converted to form the received data stream which goes to the data sink. Because of their common transmit and receive functions the QPSK and 16-QASK schemes are very similar in modem configuration, however each scheme also has its own individual traits.

2.3 Traits of QPSK and 16-QASK

QPSK is a modulation technique that has the best energy efficiency of any of the quadrature-modulation techniques. Energy efficiency is thought of in terms of the amount of average bit energy, i.e. $\overline{E}_b$, it takes to maintain a certain SER. An upper-bound expression for error probability of QPSK which is asymptotically tight for small P(e) is

$$P(e) < 2Q\left(\sqrt{2\overline{E}_b/N_o}\right) \tag{2.4}$$

where

$$Q(x) = 1/\sqrt{2\pi}\int_x^{\infty} e^{-y^2/2}\,dy \tag{2.5}$$

and $\overline{E}_b$ is average bit energy and N_o is the spectral noise density. In the QPSK case the peak energy is equal to the average energy, which may be seen from inspection of the signal constellation of figure 2.1.

An upper-bound expression for probability of error for 16-QASK is as follows:

$$P(e) < 3\,Q\left(\sqrt{0.8\overline{E}_b/N_o}\right) \qquad (2.6)$$

The peak energy in this case is 1.8 times larger than the average energy. The SER versus average energy curves for both QPSK and 16-QASK are given in Figure 2.3. It can be seen from the curves that QPSK is about 4 dB more energy efficient than 16-QASK at an error rate of 1×10^{-5}.

Bandwidth efficiency is measured in information rate per unit of bandwidth, with units of bps/Hz [2], [3]. The power spectral density relative to a center frequency for both QPSK and 16-QASK, assuming rectangular pulses is

$$S(f) = 2E_s \frac{\sin^2(2\pi f/R_s)}{(2\pi f/R_s)^2} \qquad (2.7)$$

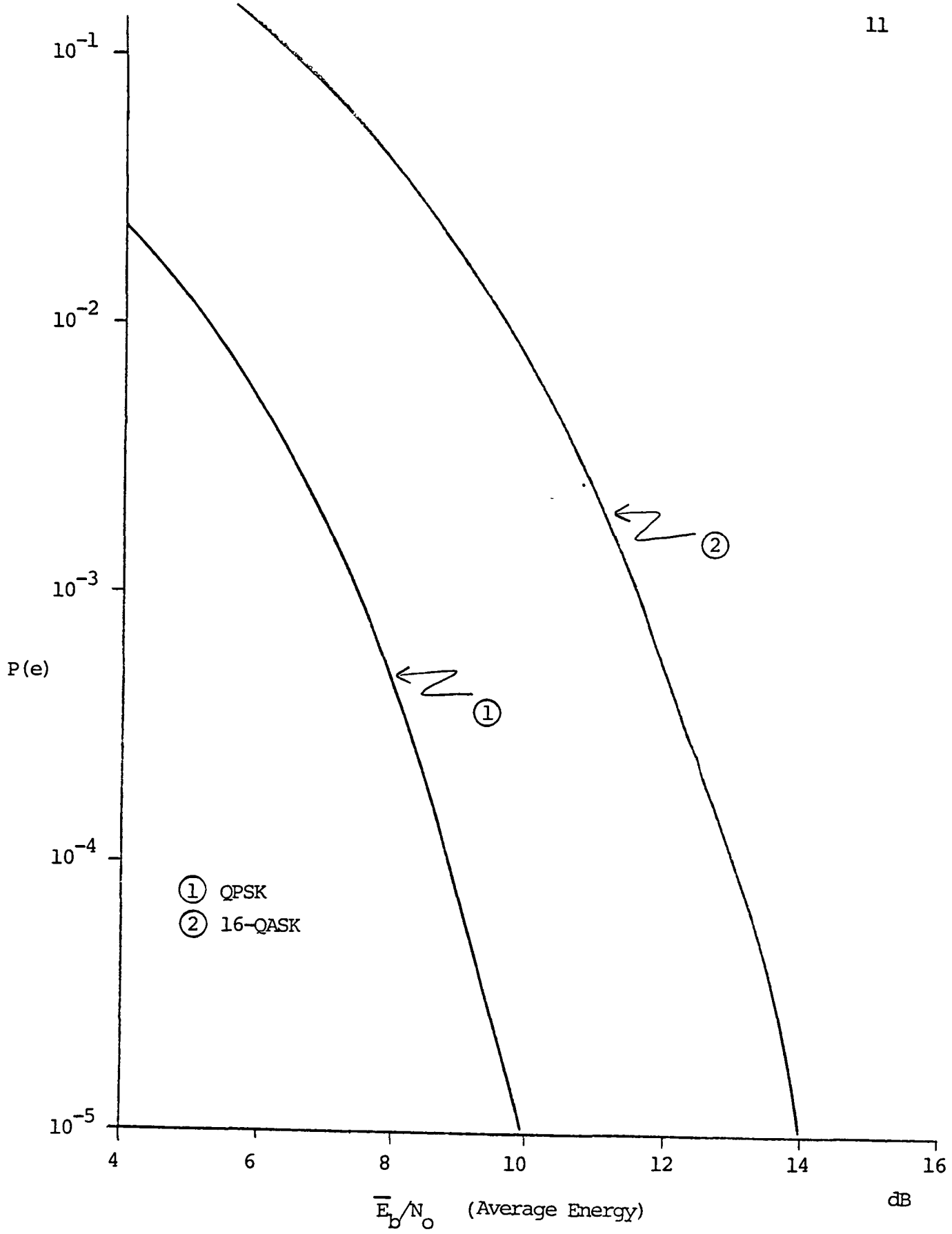


Figure 2.3 Error Performance

where E_s is symbol energy and R_s is the symbol rate. From equation 2.8 the first null is at R_s. If the bandwidth is defined null-to-null then the bandwidth (BW) is $2R_s$. The information rate for QPSK is $R_b=2R_s$ and for 16-QASK $R_b=4R_s$ so with QPSK the spectral efficiency is $2R_s/2R_s$=1bps/Hz and for 16-QASK $4R_s/2R_s$=2bps/Hz. Thus 16-QASK is twice as bandwidth efficient as QPSK. Pulse-shaping methods can actually almost double these efficiencies.

2.4 Two-Layer Constellation

By referring to Figure 2.4 it can be seen that the 16-QASK signal constellation can be thought of as a QPSK signal (first layer) with a second layer of modulation superposed [4]. The second layer is applied at a level 6 dB lower than the first. Since the 16-QASK constellation is just two layers of QPSK modulation at different levels, it can conveniently be implemented by combining in parallel two QPSK modulators. The demodulation can be handled so that the only difference in the two modes is four-level threshold decisions for the 16-QASK case and two-level decisions for the QPSK case. From this standpoint it is quite obvious that it is advantageous to implement a dual-mode modem with QPSK and 16-QASK modulation schemes. This allows the exploitation of either energy or bandwidth efficiency by simple mode switching.

A detailed block diagram of the architecture for a

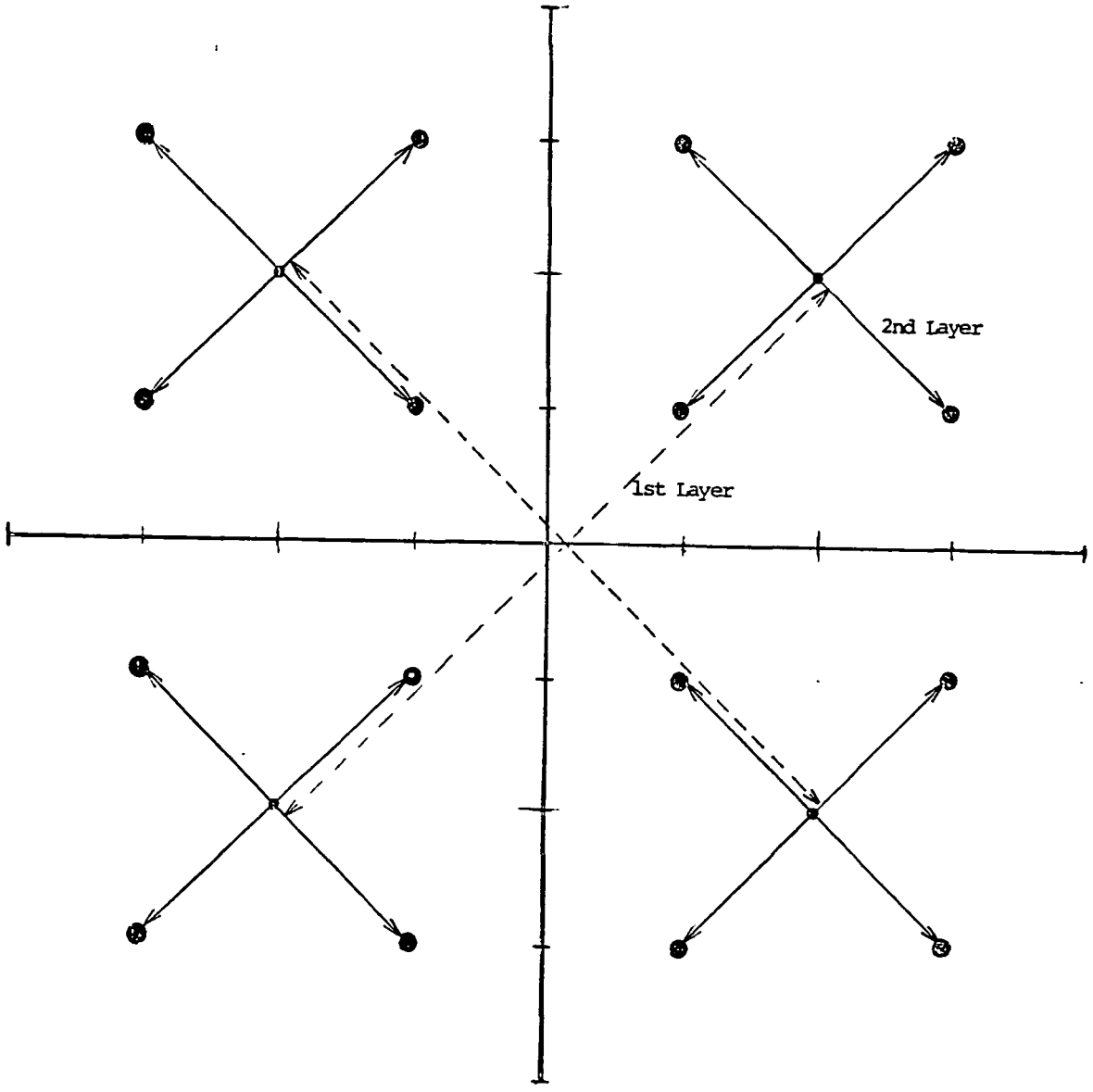


Figure 2.4 Combined Constellation

dual-mode modem is shown in Figure 2.5. The dual-mode modem designed, built, and tested as part of this research is based on this architecture.

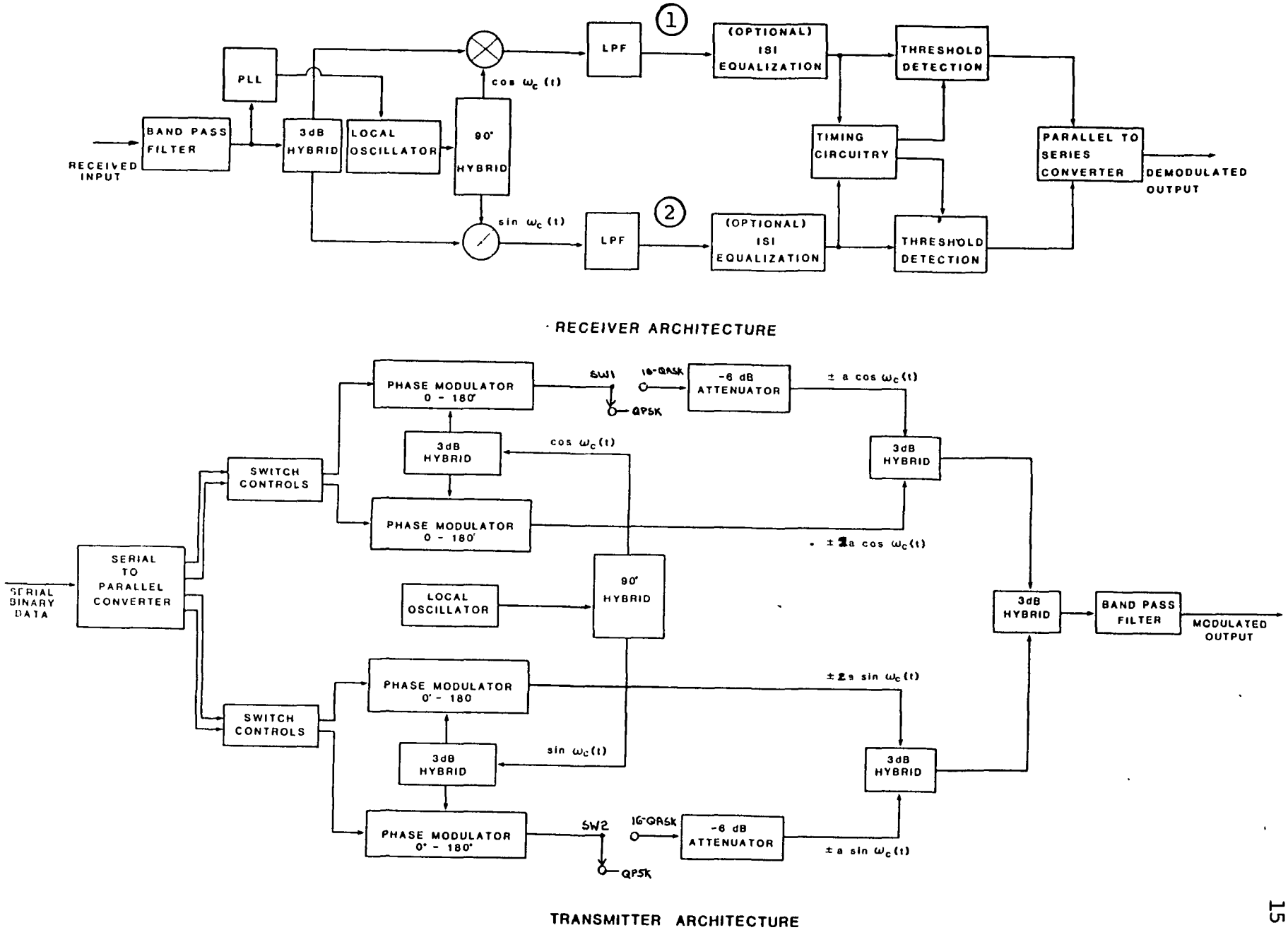


Figure 2.5 Detailed Block Diagram of Dual Mode Modem

CHAPTER THREE

EFFECTS OF PHASE ERROR ON PHASE-COHERENT DETECTION

This chapter deals briefly with the need for carrier recovery methods in a phase-coherent communication system. A analysis of the errors made in demodulation decisions caused by phase error and the degradation to the SER curves due to a fixed phase error for both QPSK and 16-QASK is also conducted. As a conclusion, preliminary specifications of a carrier recovery method for the dual-mode modem are presented.

3.1 The Need for Carrier Tracking

Accurate transmission of data through a phase-coherent communication system requires the demodulator to have knowledge of the frequency and phase of the incoming signal. Not only is there a need for initial knowledge of frequency and phase, but also a need to track these constantly changing parameters. Before an attempt is made to track the phase and frequency changes the sources of the changes and the tolerable amounts of tracking error need to be determined.

There are many sources that can contribute to an instantaneous phase difference between a demodulator and the incoming signal. They range from obvious sources such

as carrier frequency difference between the receiver and transmitter to subtle sources such as phase noise of a VCO, supply voltage fluctuation, humidity and physical vibration [6]. The two major sources of phase changes that cause this need for tracking are frequency drift of carrier oscillators, and the Doppler effect of the channel. The better oscillators available are only capable of one part in a million frequency stability over the operating temperature range. This represents a 360° phase change in 1/10 of second for a 10 MHZ oscillator. It is obvious that there is a need for a carrier tracking loop, since there are many local oscillators in the system all contributing to phase error.

3.2 Phase Error Analysis for QPSK

Due to phase error the decision regions of the receiver are considered to be perturbed relative to the constellation. Figure 3.1 shows this concept graphically. A bound for determining the SER is expressed as

$$P(e) < N\, Q\left(d_{dis}/\sqrt{2N_o}\right) \tag{3.1}$$

where N is the number of neighbors, i.e. N=2 for QPSK and $d_{dis}/2$ is defined as the minimum distance to the nearest decision boundary. Referring to Figure 3.1 it is obvious that the SER is now determined by two minimum

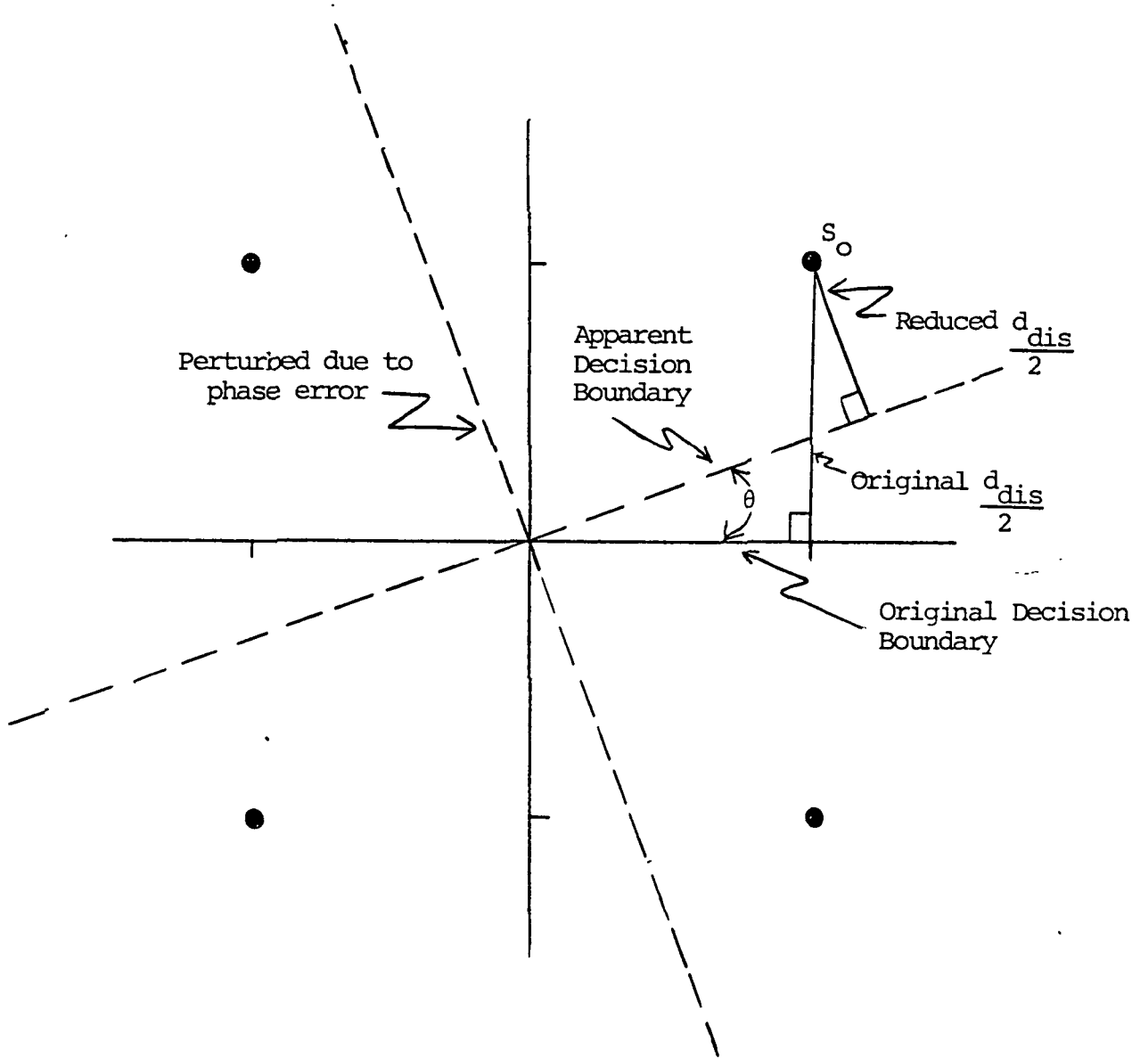


Figure 3.1 Graphical Representation of Degradation Due to Phase Error For QPSK

distances for each signal, and that the phase error reduces the $d_{dis}/2$ causing a higher error rate. A bound expression for this new error rate for QPSK is expressed as

$$P(e/S_o) = P(e) < Q\left(d_{disl}/\sqrt{2N_o}\right) + Q\left(d_{dis2}/\sqrt{2N_o}\right) \qquad (3.2)$$

The following is derivation of a bound expression for the SER rate for QPSK with a fixed phase error θ using equation 3.2, refer to Figure 3.1. and Figure 3.2. The minimum distances of the signal S_o are expressed as

$$d_{disl}/2 = \sqrt{E_s}\,\sin(\pi/4-\theta) \qquad (3.3)$$

$$d_{dis2}/2 = \sqrt{E_s}\,\sin(\pi/4+\theta) \qquad (3.4)$$

where E_s is symbol energy. Substituting for $d_{dis1}/2$ and $d_{dis2}/2$,

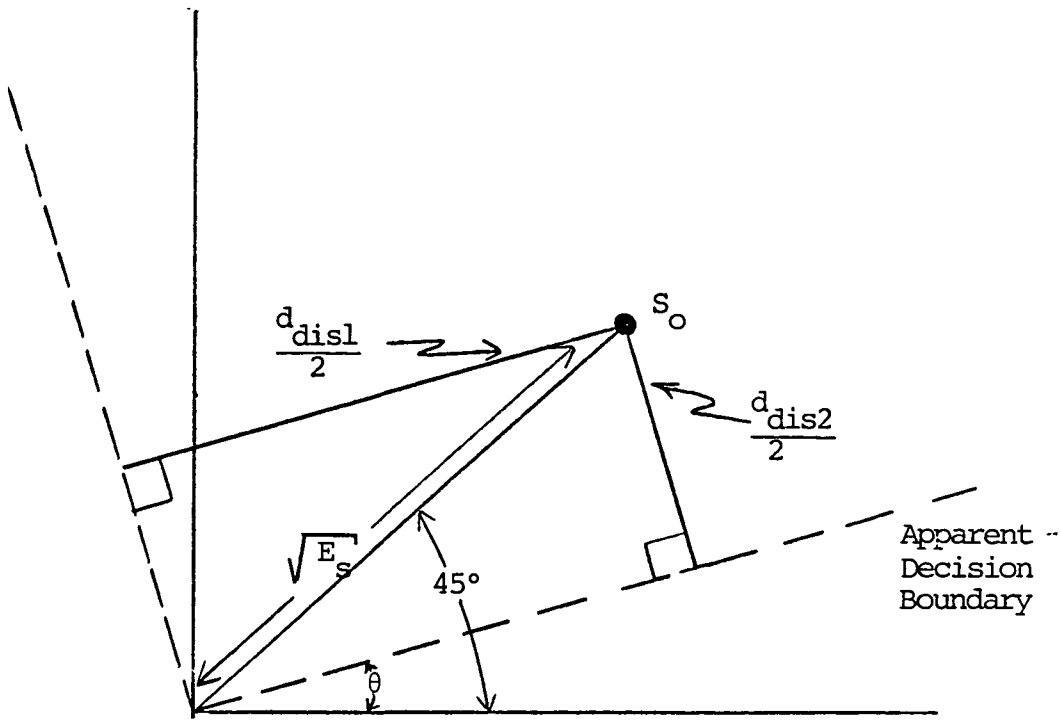


Figure 3.2 Minimum Distance Calculations due to Phase Error for QPSK

$$P(e) < Q\left((2\sqrt{E_s/2N_o})\sin(\pi/4-\theta)\right) + Q\left((2\sqrt{E_s/2N_o})\sin(\pi/4+\theta)\right) \qquad (3.5)$$

It can be found that the average bit energy is half that of the symbol energy, i.e. $E_s = 2E_b$. Using trigonometric identities

$$\sin(\pi/4-\theta) = \sqrt{2}/2(\cos\theta + \sin\theta)$$
$$\sin(\pi/4+\theta) = \sqrt{2}/2(\cos\theta - \sin\theta) \qquad (3.6)$$

and substituting, then

$$P(e) < Q\left(\sqrt{2E_b/N_o}\,(\cos\theta + \sin\theta)\right) + Q\left(\sqrt{2E_b/N_o}(\cos\theta - \sin\theta)\right) \qquad (3.7)$$

Equation 3.7 is only valid for phase error less than 45°. This is obvious through inspection of Figure 3.1. A phase error greater than 45° causes the receiver to err almost always unless differential coding is employed. Using equation 3.7, upper-bound SER curves for QPSK with fixed

phase error less than 45° were generated. The are presented in Figure 3.3. It is seen from these curves that large degradation in energy efficiency occurs with large phase errors, i.e.>30° and with only a 20° phase error roughly 4 dB more energy is needed to maintain a SER of 1 X 10^{-5}.

3.3 Phase Error Analysis for 16-QASK

It is seen from inspection of Figure 3.4 that 16-QASK is more susceptible to bit errors due to phase noise than QPSK. This is due to the 16-QASK constellation having shorter distances between neighboring signals. The phase error analysis here is treated in the same manner as in the QPSK case, the shortest distances from each signal to each neighboring decision threshold are calculated and applied to equation 3.1. Due to the complexity[1] involved with computing all the distances for each signal to all its neighboring decision thresholds only the closest threshold is considered. This simplified bound is not as tight as an expression using all the distances but is sufficient for this investigation.

A bound for the error rate of 16-QASK with phase error θ is

[1]Twelve separate calculations for minimum distance would be required.

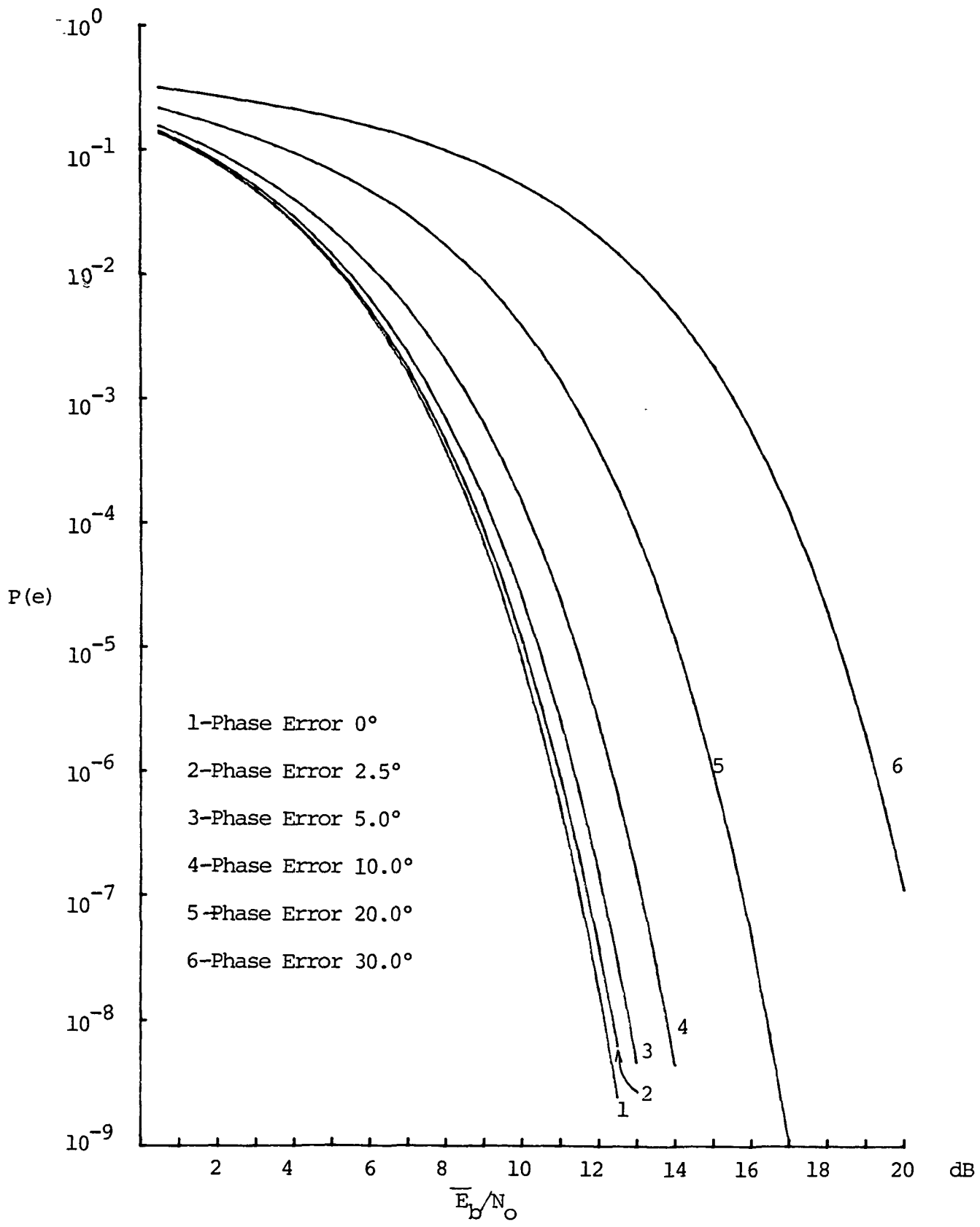


Figure 3.3 Degradation to SER Due to Fixed Phase Error for QPSK

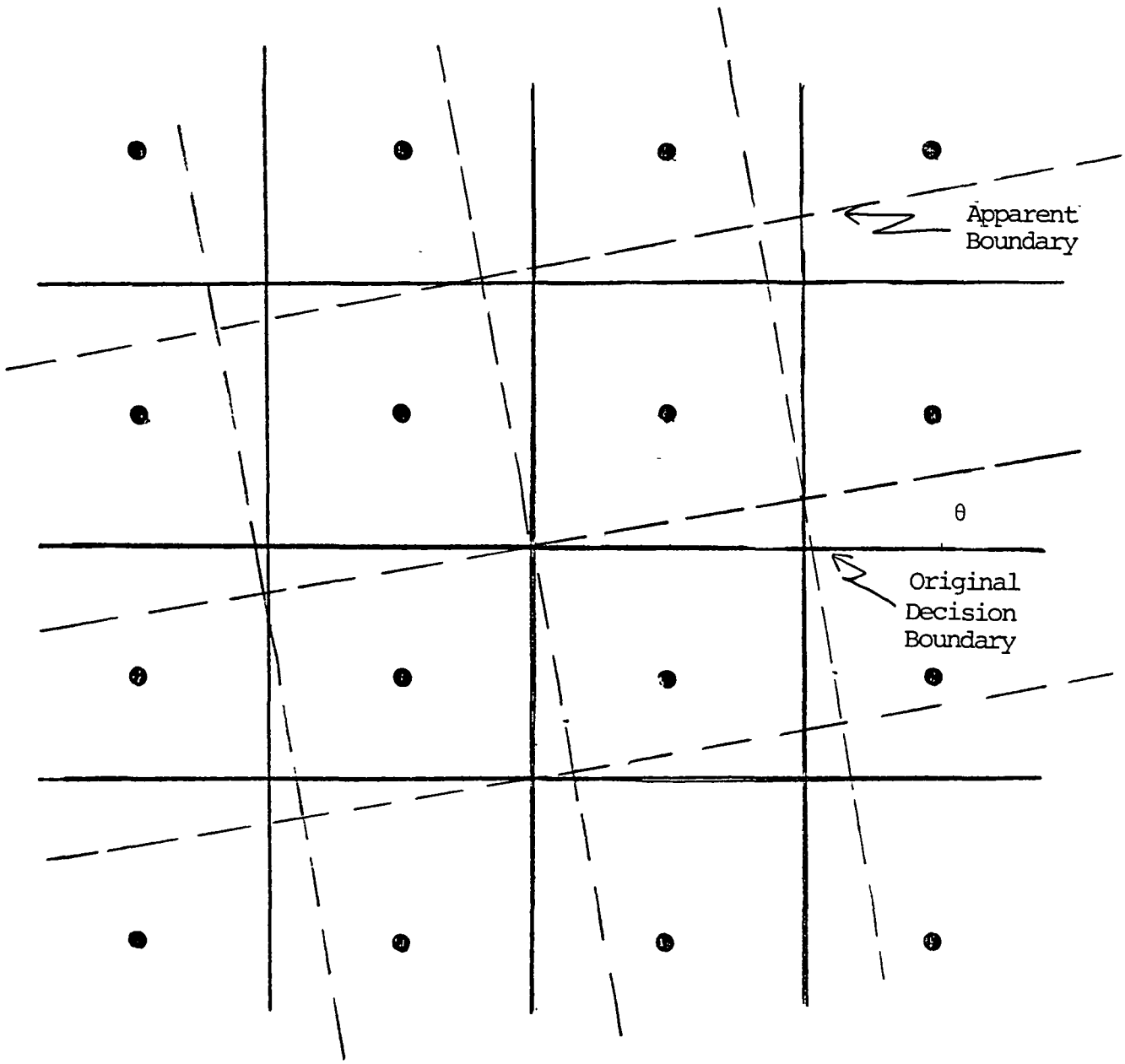


Figure 3.4 Graphical Representation of Degradation
Due to Phase Error for 16-QASK

$$P(e) < Q\left(d_{dis1}/\sqrt{2N_o}\right) + \frac{3}{2}Q\left(d_{dis2}/\sqrt{2N_o}\right) + \frac{1}{2}Q\left(d_{dis4}/\sqrt{2N_o}\right) \quad (3.8)$$

The minimum distances are found through trigonometric calculations shown below and referring to Figure 3.5.

$$d_{dis1/2} = \sqrt{2E}\,\sin(\beta_2-\theta) = \sqrt{E}(\cos\theta-\sin\theta)$$

$$d_{dis2/2} = \sqrt{10E}\,\sin(\beta_1-\theta) = \sqrt{E}(\cos\theta-3\sin\theta)$$

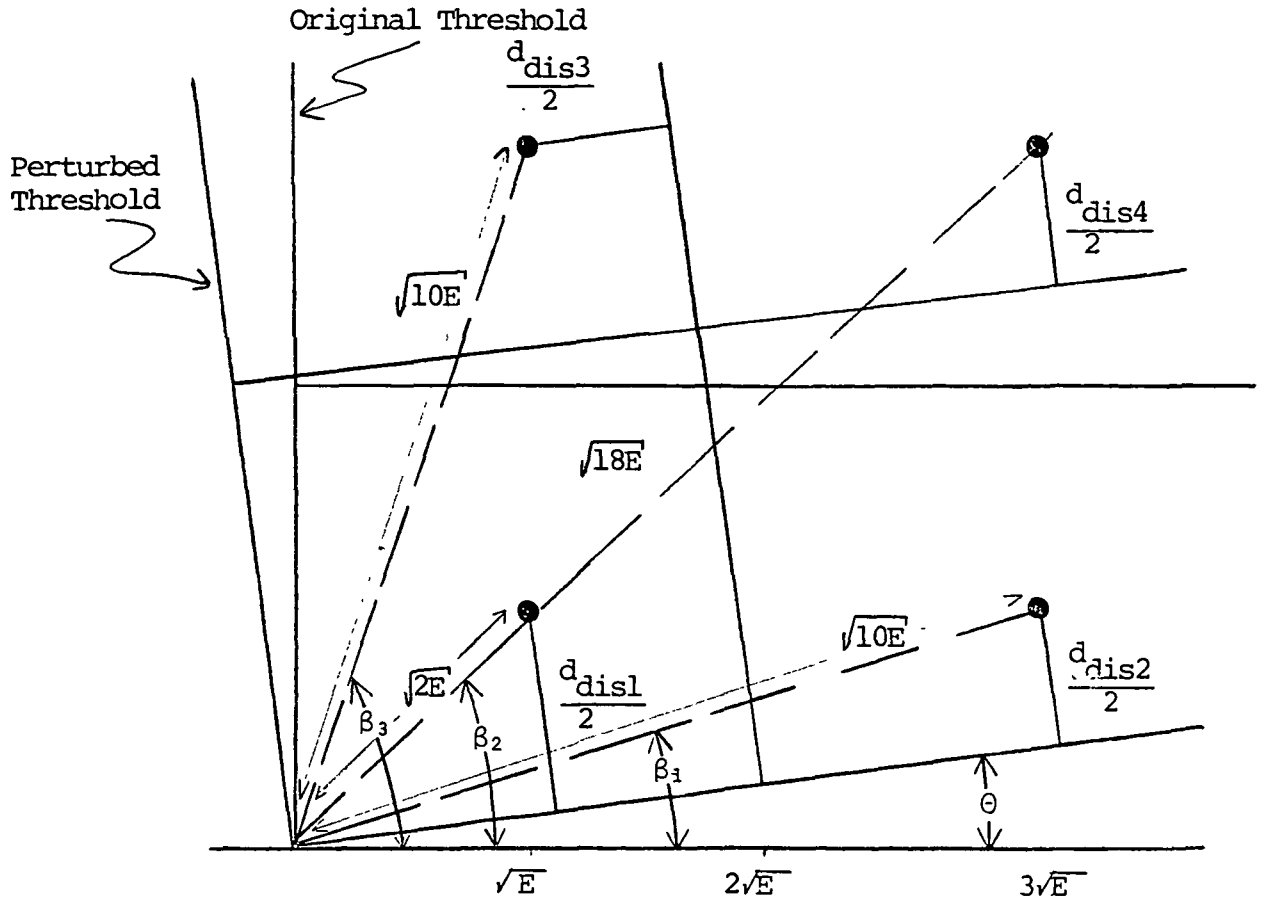
$$d_{dis3/2} = d_{dis2/2}$$

$$d_{dis4/2} = \sqrt{18E}\,\sin(\beta_2-\theta)-2\sqrt{E} = \sqrt{E}(\cos\theta-3\sin\theta)$$

Knowing the minimum distances, finding the average symbol energy, $\bar{E}_s=(2(10E)+18E+2E)/4=10E$, and using $\bar{E}_s=4\bar{E}_b$ gives

$$P(e) < \left(Q\,2\sqrt{\bar{E}_b/5N_o}\,(\cos\theta-\sin\theta)\right) + \frac{3}{2}Q\left(2\sqrt{\bar{E}_b/5N_o}\,(\cos\theta-3\sin\theta)\right) + \frac{1}{2}Q\left(2\sqrt{\bar{E}_b/5N_o}\,(3\cos\theta-3\sin\theta-2)\right) \quad (3.9)$$

Equation 3.9 is only valid for phase errors less than 16.87°. Using equation 3.9, upper-bound SER curves for 16-QASK with fixed phase error less than 10° are generated and



$\beta_1 = \tan^{-1}(1/3)$

$\beta_2 = \tan^{-1}(1)$

$\beta_3 = \tan^{-1}(3)$

Figure 3.5 Minimum Distance Calculations Due to Phase Error for 16-QASK

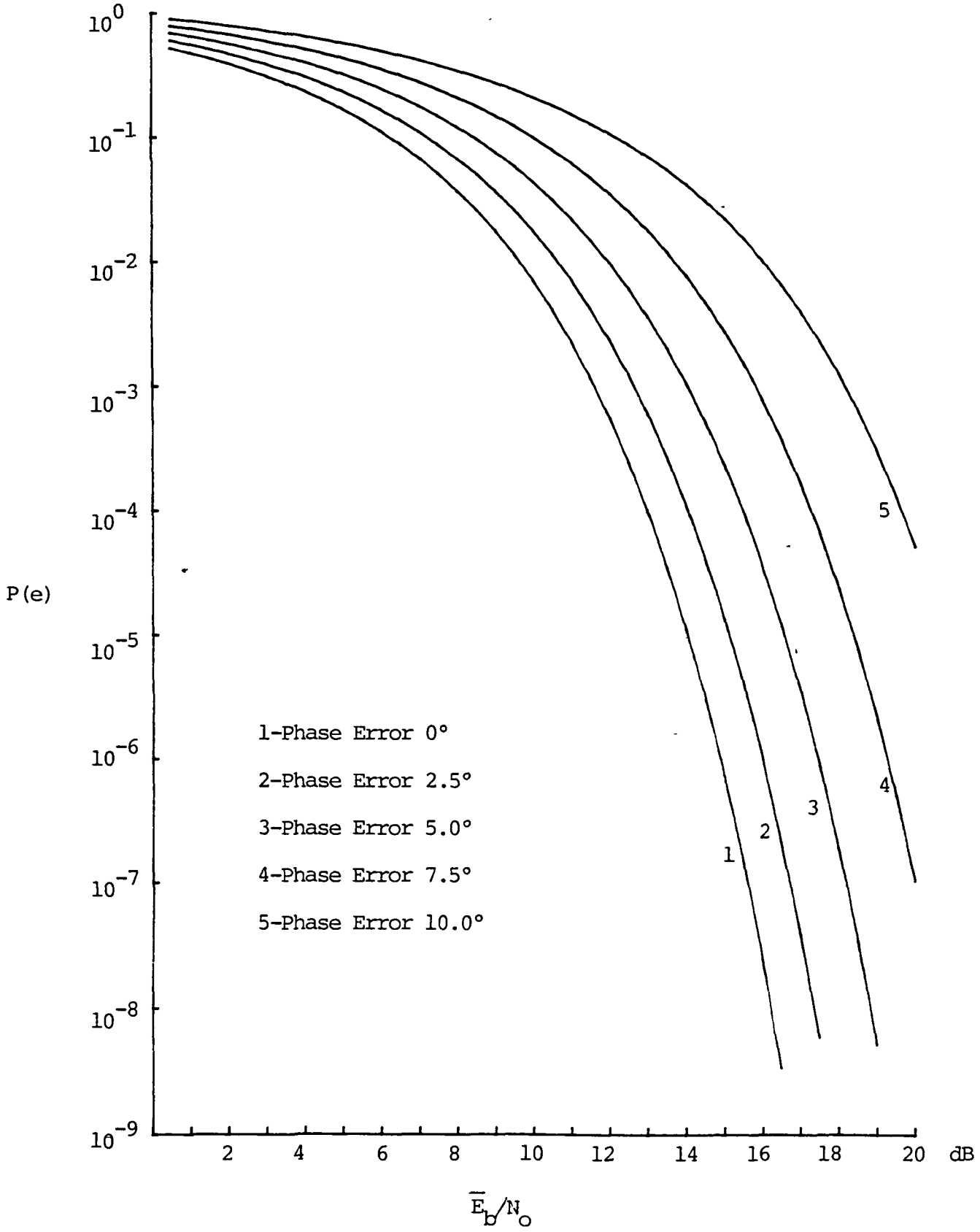


Figure 3.6 Degradation to SER Due to Fixed Phase Error for 16-QASK

the results are presented in Figure 3.6. Through inspection of these curves the large degradation in energy efficiency due to phase error is again observed, however the degradation is much more severe than with QPSK. The 16-QASK moduation technique requires a 4 dB increase in energy to maintain a SER of 1×10^{-5} with a fixed phase error of only 7° . As stated earlier QPSK is able to withstand about 20° of phase error at this level of degradation. This comparison shows the intolerance a 16-QASK scheme has to phase error and begins to outline the magnitude of the importance of the carrier recovery loop.

We conclude that the carrier phase for 16-QASK must be tightly controlled to within perhaps 2° rms. Fortunately this is assisted by the fact that 16-QASK maintains a 4dB larger E_s/N_o than QPSK to yield the same P(e). Nonetheless phase accuracy represents a significant design challenge.

CHAPTER FOUR

CARRIER RECOVERY METHODS

This chapter is concerned with the problems of carrier synchronization and in particular, methods for reconstruction of coherent references that are compatible with the two modulation schemes, QPSK and 16-QASK, at high data rates. First the problem of crosstalk is investigated and three methods to perform carrier reconstruction, (demod-remod, superposed and decision feedback) are summarized. An in-depth analysis of the decision feedback method applied to the dual-mode modem is then presented as a conclusion.

4.1 Crosstalk

A QPSK signal can be represented as in equation 2.3. The noise n(t) assumed to be bandpass noise and is represented as:

$$n(t) = \sqrt{2}(n_c(t)\cos\omega_c t + n_q(t)\sin\omega_c t) \qquad (4.1)$$

If the local reference carrier of Figure 2.5 is considered to have a phase error θ and a maximum amplitude of $\sqrt{2}$ then the two quadrature reference signals are written as

$$r_i(t) = \sqrt{2}\cos(\omega_c t + \Theta) \quad (4.2)$$

$$r_q(t) = \sqrt{2}\sin(\omega_c t + \Theta) \quad (4.3)$$

Referring to Figure 2.5 again and using the above assumptions the signals at (1) and (2) are low-pass filtered so the double-frequency products are removed and the signals are expressed as:

$$r_1(t) = d_1(t)\cos\Theta - d_2(t)\sin\Theta + n_c(t)\cos\Theta - n_q(t)\sin\Theta \quad (4.4)$$

$$r_2(t) = d_1(t)\sin\Theta + d_2(t)\cos\Theta + n_c(t)\sin\Theta + n_q(t)\cos\Theta \quad (4.5)$$

The sin θ terms are crosstalk which present an undesirable signal from the opposite quadrature channel due to the phase error θ. What is desired is to reduce the phase error to a very small angle (ideally zero) causing the sin θ terms to approach zero and the cos θ terms to go to one, leaving just the data $d_1(t)$ and $d_2(t)$ in the appropriate channels.

In order for a carrier synchronization loop to reduce the phase error of the receiver to zero, some proportional signal representation of the phase error θ must be derived. This entails removing the noise and modulation that is

contained in the incoming signal. For QPSK this is a fairly easy task, e.g. a Costas loop that is covered extensively in the literature [2], [5], [6]. For 16-QASK modulation the derivation of an error signal is not as trivial, since the complexity of the waveform that the error signal must be derived from is much greater than that of QPSK.

The incoming 16-QASK signal is represented as shown earlier by equation 2.4. The noise and quadrature reference signals are assumed the same as in equation 4.1, 4.2 and 4.3. Referring to the receiver of Figure 2.5 the signals at (1) and (2) for 16-QASK are:

$$r_1(t) = d_1(t)\cos\theta - d_2(t)\sin\theta + \frac{1}{2}(d_3(t)\cos\theta + d_4(t)\sin\theta) + n_c(t)\cos\theta - n_q(t)\sin\theta \quad (4.6)$$

$$r_2(t) = d_1(t)\sin\theta + d_2(t)\cos\theta + \frac{1}{2}(d_3(t)\sin\theta + d_4(t)\cos\theta) + n_c(t)\sin\theta + n_q(t)\cos\theta \quad (4.7)$$

Again the sin θ terms are crosstalk and disappear as θ goes to zero. The difference with this signal compared to the QPSK case is there is a second information term that is 6 dB lower. This shows up both in the desired signals (cos θ) and the undesired signals (sin θ), making the removal of the modulation and noise for phase error derivation more

complicated.

4.2 Methods of Carrier Recovery

Three methods of carrier reconstruction for QPSK and 16-QASK signals are reviewed. The basic concepts of each technique, and the manner in which they derive their error signal for phase error correction are explained. Then the best method of carrier recovery is selected based on:

1. Probability of error performance
2. Complexity of implementation
3. Compatibility for use with QPSK and 16-QASK.

The demod-remod method of carrier recovery [4], [9] is almost self explanatory from its name. A demodulation operation formulates an estimate for the first layer of modulation, which is remodulated and a phase comparison of the remodulated signal and incoming signal is made to derive the VCO control signal. A block diagram of this technique is given in Figure 4.1 and a detailed explanation follows.

A correlation is first performed with the incoming signal and two quadrature references. The outcomes at (1) and (2) of Figure 4.1, are described by equations 4.4 and 4.5 for QPSK, and 4.6 and 4.7 for 16-QASK. A two-level decision is then made on both signals forming estimates of the first layer baseband data. These estimates are then used as control signals at points (3) and (4) in the remod

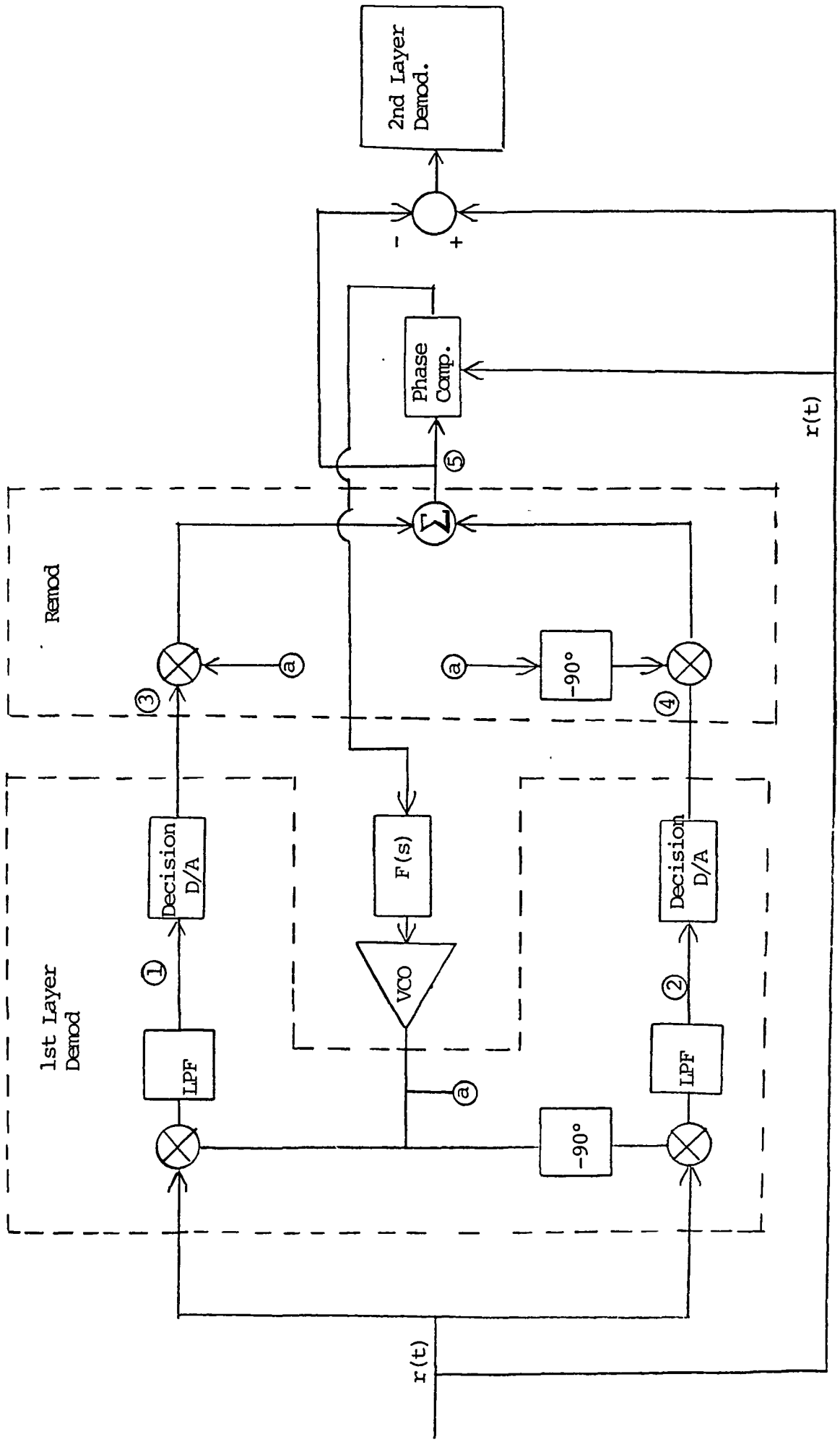


Figure 4.1 Block Diagram of Demod-Remod Method

module which outputs at (5) a replica of what the incoming signal would look like with just first-layer modulation. The signal at (5) is then subtracted from the incoming signal leaving just the second layer of data modulation. Second-layer decisions are made from this residual signal. To derive the carrier loop control voltage the replica signal at (5) and the incoming signal, r(t), are phase compared and the difference in their phases is passed through the loop filter and on to the control input of the VCO.

In this generation of an error signal proportional to the phase difference, the loop operates on an incoming signal which is regarded as a QPSK signal even though it is a 16-QASK signal. This causes the out-of-phase second layer modulation to act as pattern jitter causing degraded tracking performance which can be minimized by making the loop bandwidth small. This configuration typifies the carrier recovery loop often used to acquire synchronization without removing second-layer data modulation. From a practical standpoint the demod-remod technique is desirable only if the incoming signal is relatively low in frequency, i.e. less than 1 GHz. Controlling the phase shifts and performing remodulation/demodulation at very high frequencies, i.e., 1 to 30 GHz becomes complex and costly, therefore this technique is more applicable for low-frequency application. Lower-frequency operation implies

slower data rates which may not be an acceptable compromise for the system. Therefore, the demod-remod technique of carrier reconstruction is more suited for use in relatively low frequency systems and when the loop bandwidth can be made much smaller than the data rate to minimize pattern jitter.

A technique of carrier recovery that operates in a very similar manner to that of demod-remod but at baseband, avoiding the shortcomings that occur at high frequencies, is a method referred to as superposed [10]. Its structure is outlined in the block diagram of Figure 4.2 and a detailed explanation of operations follows.

The input signal is correlated to baseband, with the signals at (1) and (2) of Figure 4.2 being described by equations 4.4 and 4.5 for QPSK and 4.6 and 4.7 for 16-QASK. Two-level decisions are made on these signals, which are estimates of the first-layer data. At points (3) and (4) the first layer estimates are subtracted from the baseband signals leaving just the second layer modulation. The second layer signal is then processed in the same manner as the first layer, with a two-level decision being made followed by a subtraction of this estimation from the baseband signal. At this point the second layer modulation is fed to the opposite arm and multiplied with the baseband signal. These signals from each channel are subtracted, forming the error signal. This is passed

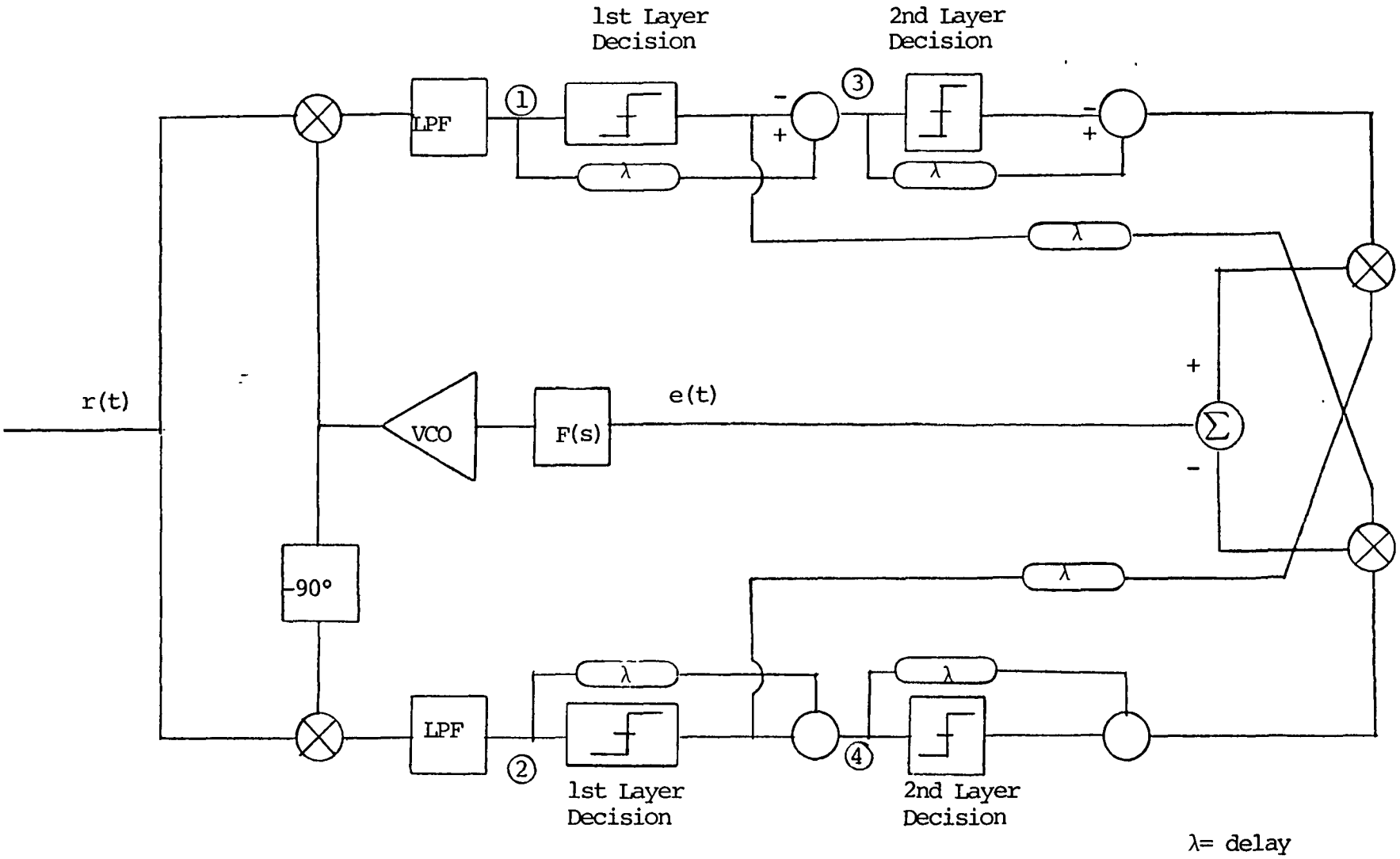


Figure 4.2 Block Diagram of Superposed Method

through the loop filter F(s), then on to the control input of the VCO closing the loop.

A shortcoming of this technique is that it also produces pattern jitter. This is evident through the results of [10], where an expression for the error signal with $E_b/N_o = \infty$ (correct estimates assumed) is given by

$$\begin{aligned} e(t) = {} & \operatorname{sgn}(d_1(t))d_1(t)+\operatorname{sgn}(d_2(t))d_2(t)\ \sin\theta \\ & - \frac{1}{2}\left[\operatorname{sgn}(d_1(t))d_4(t)+\operatorname{sgn}(d_2(t))d_3(t)\right]\sin\theta \\ & - \frac{1}{2}\left[\operatorname{sgn}(d_2(t))d_3(t)-\operatorname{sgn}(d_1(t))d_4(t)\right](\cos\theta-1) \end{aligned} \qquad (4.8)$$

Pattern jitter is present even with small phase errors, i.e., $\theta<<1$. Using small-angle approximations the error signal is

$$e(t) \simeq -2A\theta - \frac{1}{2}(j(t))\theta \qquad (4.9)$$

where j(t) is pattern jitter caused by the second layer data described by:

$$j(t) = \operatorname{sgn}\ (d_1(t))d_4(t)+\operatorname{sgn}(d_2(t))d_3(t) \qquad (4.10)$$

and $-2A\theta$ is the desired error signal that is proportional to the phase error. Even with the pattern jitter this technique can be useful if, as stated earlier, the loop bandwidth is designed to be much smaller than the data rate. These last two techniques discussed show the methods used for carrier recovery without removal of the second layer modulation and demonstrate the limitation due to

pattern jitter. The next method summarized avoids the problem of pattern jitter without a large increase in complexity. This method is referred to as decision feedback.

The decision feedback method of carrier reconstruction [11], [8], [6], [5] is shown in block diagram form in Figure 4.3. The basic operation of this loop is explained by its name, a decision on the modulated data is fed back to the opposite arm in order to remove the data to form an accurate error signal.

Synchronous detection is first performed, with the baseband outcomes at (1) and (2) of Figure 4.3 being described by equations 4.4 and 4.5 for QPSK, and 4.6 and 4.7 for 16-QASK. The signals at (1) and (2) are passed through a detection filter, which for optimum performance is an integrate-and-dump operation, assuming the data sent was square pulses. Estimates are made on these filtered signals using two-level decisions for QPSK and four-level decisions for 16-QASK. The estimates are then fed back to the opposite arm and multiplied by the delayed baseband signal. The products in each arm are subtracted, forming the error signal e(t). The error signal is passed through the loop filter F(s), then onto the control input of the VCO, thus closing the loop.

The decision feedback method is capable of avoiding the problem of pattern jitter in the 16-QASK mode when

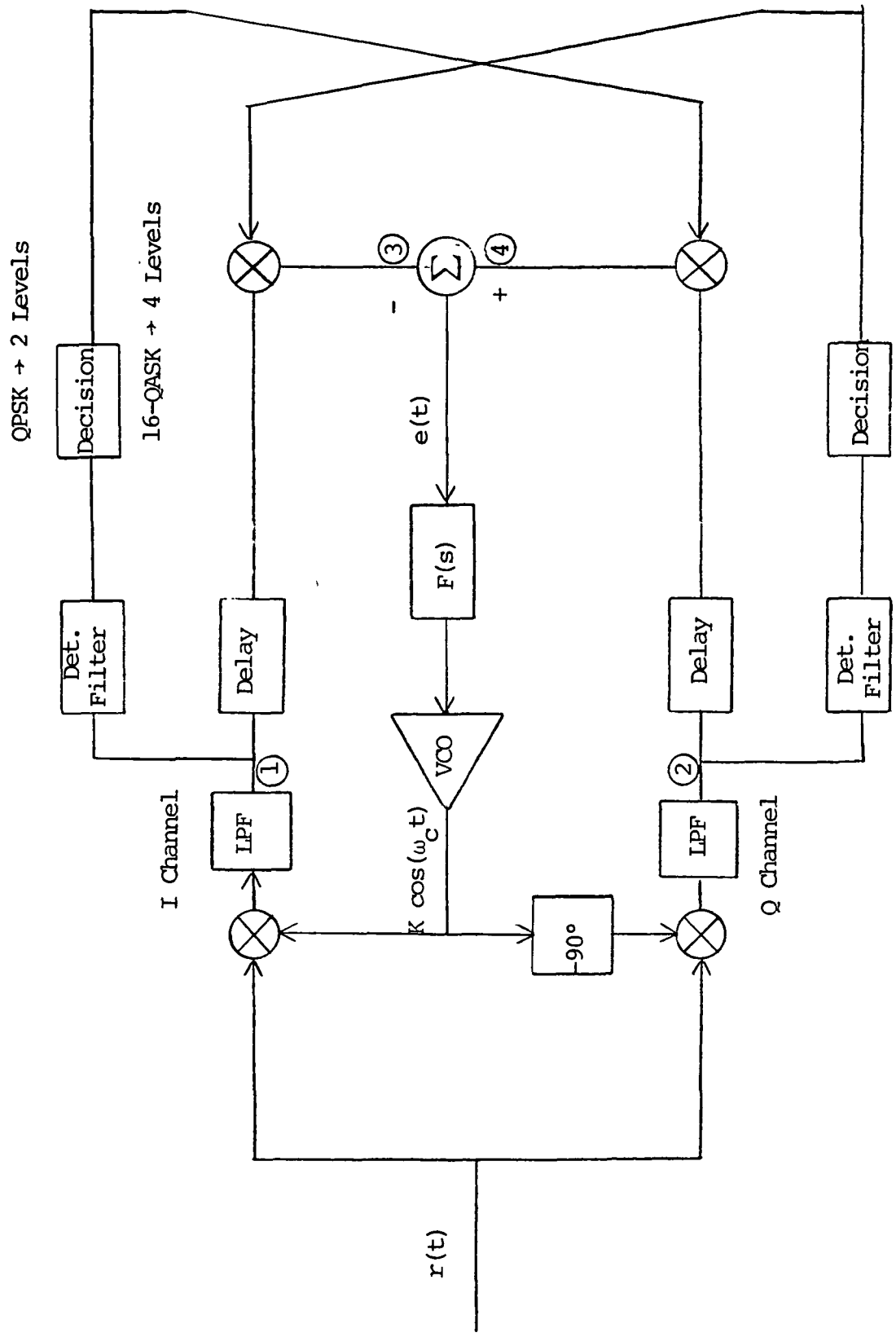


Figure 4.3 Decision Feedback Loop Block Diagram

four-level decisions are made, providing good loop tracking performance. The system complexity is not prohibitive, the signal processing is done at baseband avoiding the complication of processing at the carrier frequency, and the relatively simple configuration of the decision feed-lock loop makes this scheme more applicable to a high data rate (1 gigabit/sec) system.

The best attribute of this technique is it is very compatible for use with either QPSK or 16-QASK. The only change needed for use with either modulation scheme is the number of decision levels, two levels for QPSK and four levels for 16-QASK. The remainder of the system configuration stays the same. Two-level decisions can ever be used with 16-QASK and pattern jitter can be minimal, provided the loop bandwidth is much smaller than symbol rate, i.e. ($B_L << R_S$). Due to the positive traits and compatibility with QPSK and 16-QASK the decision feedback loop was selected for use in the dual-mode modem. In the next section the problem of pattern jitter that can occur if only two level decisions are made with 16-QASK modulation is presented.

4.3 Second-Layer Pattern Jitter

It is possible to use the decision fedback loop described above as if the signal were QPSK, even though 16-QASK modulation is present. In this configuration residual pattern jitter ocurs again.

If the decision feedback loop is used with 16-QASK than the signals at (1) and (2) of Figure 4.3 are described by equations 4.6 and 4.7 respectively. If only two-level decisions are made and $\hat{d}_1$ is decided in the I channel and $\hat{d}_2$ in the Q channel the signals at (3) and (4) are:

$$r_3(t) = \hat{d}_2 d_1(t)\cos\theta - \hat{d}_2 d_2(t)\sin\theta + (\hat{d}_2 d_3(t)/2)\cos\theta + (\hat{d}_2 d_4(t)/2)\sin\theta + \hat{d}_2 n_c(t)\cos\theta - \hat{d}_2 n_q(t)\sin\theta \quad (4.11)$$

$$r_4(t) = \hat{d}_1 d_1(t)\sin\theta + \hat{d}_1 d_2(t)\cos\theta + (\hat{d}_1 d_3(t)/2)\sin\theta + (\hat{d}_1 d_4(t)/2)\cos\theta + \hat{d}_1 n_c(t)\sin\theta + \hat{d}_1 n_q(t)\cos\theta \quad (4.12)$$

If the SNR is high, then $\hat{d}_1 = \text{sgn } d_1(t)$, $\hat{d}_2 = \text{sgn } d_2(t)$. Assuming the loop is close to phase lock, then a small angle approximation is possible and the signal at (5) is

$$e_5(t) = 2A\theta + (\hat{d}_1 d_3(t)/2 - \hat{d}_2 d_4(t)/2)\theta + \hat{d}_1 d_4(t)/2 - \hat{d}_2 d_3(t)/2 + n(t) \approx 2A\theta + (j(t)) + n(t) \quad (4.13)$$

where $n(t) = \hat{d}_1 n_c(t)\theta + \hat{d}_2 n_q(t)\theta + \hat{d}_1 n_q(t) - \hat{d}_2 n_c(t)$

and $j(t) = (\hat{d}_1 d_4(t)/2 - \hat{d}_2 d_3(t)/2)$

The pattern jitter is a zero-mean ternary random sequence with possible values of A, 0, -A produced at the symbol rate. It has a power spectrum of the form of $\frac{\sin^2(\cdot)}{(\cdot)^2}$,

with an average power of $\left(1/4((A)^2+(0)+(A)^2)\right) = A^2/2$

Thus the two-sided spectral density of the random pattern jitter at zero frequency is

$$J(0) = \frac{A^2 T_s}{2} \tag{4.14}$$

where T_s is the symbol duration. Assuming the loop bandwidth to be smaller than the symbol rate we can treat the pattern noise as wideband noise within the loop. The loop phase error variance becomes

$$\sigma^2 = \frac{J(0)\,2B_L}{4A^2} = \frac{(A^2/2)T_s 2B_L}{4A^2} =$$

$$= \frac{T_s B_L}{4} = B_L T_b \tag{4.15}$$

where B_L is the one-sided equivalent noise bandwidth of the loop and T_b is the bit duration. Ideally the phase error should be kept small to maintain good SER performance, i.e. $\theta \leq 2°$. Setting $\sigma = 2°$,

$$\sigma^2 = \left(\frac{2}{57}\right)^2 = B_L T_b = B_L/R_b \tag{4.16}$$

or $B_L \simeq .001\ R_b$, where R_b is the bit rate.

In the QPSK case, suppose we wish $P(e) = 10^{-5}$. Then $\overline{E}_b/N_o \simeq 10$dB. This means $P\ T_b/N_o \simeq 10$ or $P/N_o = 10R_b$ where P is the average power. Assuming $\sigma = 2°$ again

$$\sigma^2 = \left(\frac{2}{57}\right)^2 = \frac{N_o B_L}{P} = B_L/R_b \tag{4.17}$$

Thus the loop bandwidth should be $B_L \simeq .01\ R_b$ purely on noise consideration alone. This is roughly ten times larger than the bandwidth of the loop for the 16-QASK case as determined by pattern jitter. Thus by making the carrier recovery loop much smaller than the symbol rate the effect of the second-layer pattern jitter is averaged out and is negligible.

The degradation of the SER for 16-QASK that occurs when the bandwidth of the carrier recovery loop is not small enough to average out the second-layer pattern jitter can be expressed using the results of degradation in BER for 16-QASK with fixed phase error from Chapter 3. It is interesting to note even with large increases of average bit energy the relative degradation due to pattern jitter stays the same. The only way to decrease this degradation from pattern jitter is to reduce the bandwidth of the loop or use a loop configuration that removes the second layer modulation outright, i.e. four-level decisions.

4.4 Further Analysis of Decision Feedback Loop

Basically, the decision feedback loop estimates the modulated data, removes it from the incoming signal and forms a control error signal that is proportional to the phase error but independent of any modulated data. The QPSK case is illustrated in the following analysis.

The signals at points (1) and (2) of Figure 4.3 (assuming references with phase error θ as described in

equations (4.2) and (4.3)), are shown below:

$$r_1(t) = d_1(t)\cos\theta - d_2(t)\sin\theta + n_c(t)\cos\theta - n_q(t)\sin\theta \qquad (4.4)$$

$$r_2(t) = d_1(t)\sin\theta + d_2(t)\cos\theta + n_c(t)\sin\theta - n_q(t)\cos\theta \qquad (4.5)$$

In each channel estimates are made on the signals $r_1(t)$ and $r_2(t)$. The estimates are in the form of threshold decisions referenced to zero volts and the decision have probability of $(1-P_e)$ of being correct.

For the above case, assume a decision of $\hat{d}_1$ in the I channel and $\hat{d}_2$ in the Q channel. These estimates are multiplied by a delayed version of the baseband signal in the opposite arm, with the delay being equal to the time it takes to pass a signal through the detection filter and to make a decision. The results of this multiplication at (3) and (4) of the diagram are

$$e_3(t) = \hat{d}_2 d_1(t)\cos\theta - \hat{d}_2 d_2(t)\sin\theta + \hat{d}_2 n_c(t)\cos\theta + \hat{d}_2 n_q(t)\sin\theta \qquad (4.18)$$

$$e_4(t) = \hat{d}_1 d_1(t)\sin\theta + \hat{d}_1 d_2(t)\cos\theta + \hat{d}_1 n_c(t)\sin\theta + \hat{d}_1 n_q(t)\cos\theta \qquad (4.19)$$

Noting $e(t) = e_4(t) - e_3(t)$,

$$\begin{aligned} e(t) = {} & (\hat{d}_1 d_1(t) + \hat{d}_2 d_2(t))\sin\theta + (\hat{d}_1 d_2(t) - \hat{d}_2 d_1(t))\cos\theta \\ & + (\hat{d}_1 n_c(t) - \hat{d}_2 n_q(t))\sin + (\hat{d}_1 n_q(t) - \hat{d}_2 n_c(t))\cos \end{aligned} \qquad (4.20)$$

Assuming high E_b/N_o then
$\hat{d}_1 = \text{sgn}\,(d_1(t) = \pm 1$, $\hat{d}_2 = \text{sgn}\,(d_2(t)) = \pm 1$ and the phase error is small, i.e. $\theta << 1$, allowing small-angle approximations to hold. Therefore

$$e(t) \simeq \left[\hat{d}_1 d_1(t) + \hat{d}_2 d_2(t)\right]\theta + \left[d_1(t) n_c(t) - d_2(t) n_q(t)\right]\theta + \left(\hat{d}_1 n_q(t) - \hat{d}_2 n_c(t)\right) \tag{4.21}$$

The noise can be written as

$$n(t) \simeq \hat{d}_1 n_q(t) - \hat{d}_2 n_c(t)$$

since the first noise term is small relative to the second. Therefore as the loop approaches lock (i.e., $\theta << 1$) the expression for the error control signal is

$$e(t) \simeq \left[\hat{d}_1 d_1(t) + \hat{d}_2 d_2(t)\right]\theta + n(t) = 2A\theta + n(t) \tag{4.22}$$

To get a better intuitive feeling for the operation of this loop consider the error signal to have no noise and the data estimates to be correct. Then equation (4.22) becomes

$$e(t) \simeq 2A\sin\theta \triangleq K\sin\theta \tag{4.23}$$

The rate of phase change at the VCO output is proportional to the filtered error signal and can be expressed as:

$$\frac{d\theta_o}{dt} = K_V K \sin(\theta_i(t) - \theta_o(t)) * f(t) = K_V e(t) * f(t) \tag{4.24}$$

where we have used $(\theta_i(t)) = \theta$, K_V is the gain of the VCO, K

the gain of the rest of the loop, h(t) is the loop filter impulse response, * denotes convolution, $\theta_i(t)$ is the input phase, and $\theta_o(t)$ is the output phase of the loop. If we assume h(t) = 1 (i.e., first-order loop) then

$$\frac{d\theta_o}{dt} = K_v K \sin(\theta_i(t)-\theta_o(t)) = K_v K \sin\theta(t) \qquad (4.25)$$

If the input phase, varying with time, suddenly gets larger than the output phase, i.e., $\theta_i(t)>\theta_o(t)$, the rate of phase change at the output also increases. This can be seen by inspection of equation 4.25. This rate increase equates to an increase of $\theta_o(t)$ causing the output and input phases to start to converge, making the phase difference θ smaller.

Now if the loop is presented with a 16-QASK signal the signals at (1) and (2) of Figure 4.3 are:

$$e_1(t) = (d_1(t)+d_3(t)/2)\cos\theta-(d_2(t)+d_4(t)/2)\sin +n_c(t)\cos\theta-n_q(t)\sin\theta \qquad (4.26)$$

$$e_2(t) = (d_2(t) + d_4(t)/2)\cos\theta-(d_1(t)+d_3(t)/2)\sin\theta+n_c(t)\sin\theta+n_q(t)\cos\theta \qquad (4.27)$$

A decision of $\hat{a}$ is made in the I channel and a decision of $\hat{b}$ is made in the Q channel. Assuming high $\bar{E}_b/N_o$ leads to

$$\hat{a} = \mathrm{sgn}(d_1(t)) + \mathrm{sgn}\ (d_3(t)/2) \qquad \hat{b} = \mathrm{sgn}(d_2(t) + \mathrm{sgn}\ (d_4(t)/2)$$

and we can define

$$a = \hat{a} \quad (d_1(t)+d_1(t)/2) = \begin{cases} +3A/2 \\ +A/2 \end{cases}$$

$$b = \hat{b} \quad (d_2(t)+d_4(t)/2) = \begin{cases} +3A/2 \\ +A/2 \end{cases}$$

Multiplying the decisions by the baseband of the opposite arm yields

$$e_3(t) = ba\cos\theta - b^2\sin + b(n_c(t)\cos\theta - n_q(t)\sin\theta) \qquad (4.28)$$

$$e_4(t) = ab\cos\theta + a^2\sin\theta + a(n_c(t)\sin\theta + n_q(t)\cos\theta) \qquad (4.29)$$

$$e(t) = e_4(t) - e_3(t)$$

Assuming the loop to be near lock, i.e., $\theta << 1$,

$$e(t) = (a^2+b^2)\sin\theta + n(t) \simeq (a^2+b^2)\,\theta + n(t) \triangleq K\theta + n(t) \qquad (4.30)$$

where the noise is written as

$$n(t) = bn_c(t) + n_q(t) - (bn_q(t) - an_c(t))\,\theta$$

It is seen from inspection of equation 4.30 that the error signal becomes small as the loop approaches phase-lock. Thus the results for the error signal with 16-QASK modulation using four-level decisions are the same as those obtained with two-level decisions in the QPSK case. Also,

as predicted, no pattern jitter shows up in the error signal, showing the four-level decision feedback loop is capable of complete data removal.

After this analysis of the basic operation of a decision feedback loop its high SNR operation is clear. One question is how the loop behavior depends on the quality of the data estimates.

Assuming a phase error that is essentially constant for several bit times the product of the data and its estimation, i.e. $(d(t)\,\hat{d})$ is replaced by the expectation of the product. That is

$$E(d(t)\hat{d}) = (+1)P(d(t)=\hat{d}) + (-1)P(d(t)\neq\hat{d}) = 1-2P(e)$$

where P(e) is the error of probability conditioned on the phase error. In [5] the loop response for decision feedback is stated in the form of a steady - state stochastic integro - differential equation

$$\frac{d\theta(t)}{dt} = \frac{d\theta_o(t)}{dt} - \frac{K_1}{\sqrt{2}}(1-2P(e))\sin\theta(t) + d_1(t)n(t)$$

$$- \frac{K_2}{\sqrt{2}}(1-2P(e))\sin\theta(t) + d_1(t)n(t)$$

Thus the effect of estimation errors is regarded as a

reduction in loop gain by a factor of $(1-2P_e)$. If the loop is design to maintain a low error rate i.e. $P(e) \leq 1X10^{-2}$ (which is equivalent to SNR of 14 dB with a phase of 5° for 16-QASK) this reduction in loop gain can be ignored.

The next trait to investigate is that of false-lock points. By observing equation 4.26 and 4.27 for 16-QASK and 4.20 and 4.22 for QPSK it is seen that a general expression for the error signal can be written, ignoring noise

$$e(t) = (\hat{a}a+\hat{b}b)\sin\Theta + (\hat{a}b-\hat{a}b)\cos\Theta \qquad (4.31)$$

We desire to find the average value of e(t) conditioned on a fixed phase error which is referred to as the "S-curve." Mathematically the S-curve is

$$E(e(t)/\Theta) \triangleq G(\Theta) \qquad (4.32)$$

Then from equation 4.31 and the results of [7]

$$g(\Theta) \triangleq g_1(\Theta)\sin + g_2(\Theta)\cos\Theta \qquad (4.33)$$

where

$$g_1(\Theta) = E(\hat{a}a+\hat{b}b/\Theta)$$
$$g_2(\Theta) = E(\hat{a}b+\hat{a}b/\Theta)$$

and $g_1(\theta)$ and $g_2(\theta)$ are normalized to the slope of the function $G(\theta)$ at $\theta=0$. We must first find the expected values of the products of data and estimates conditioned on

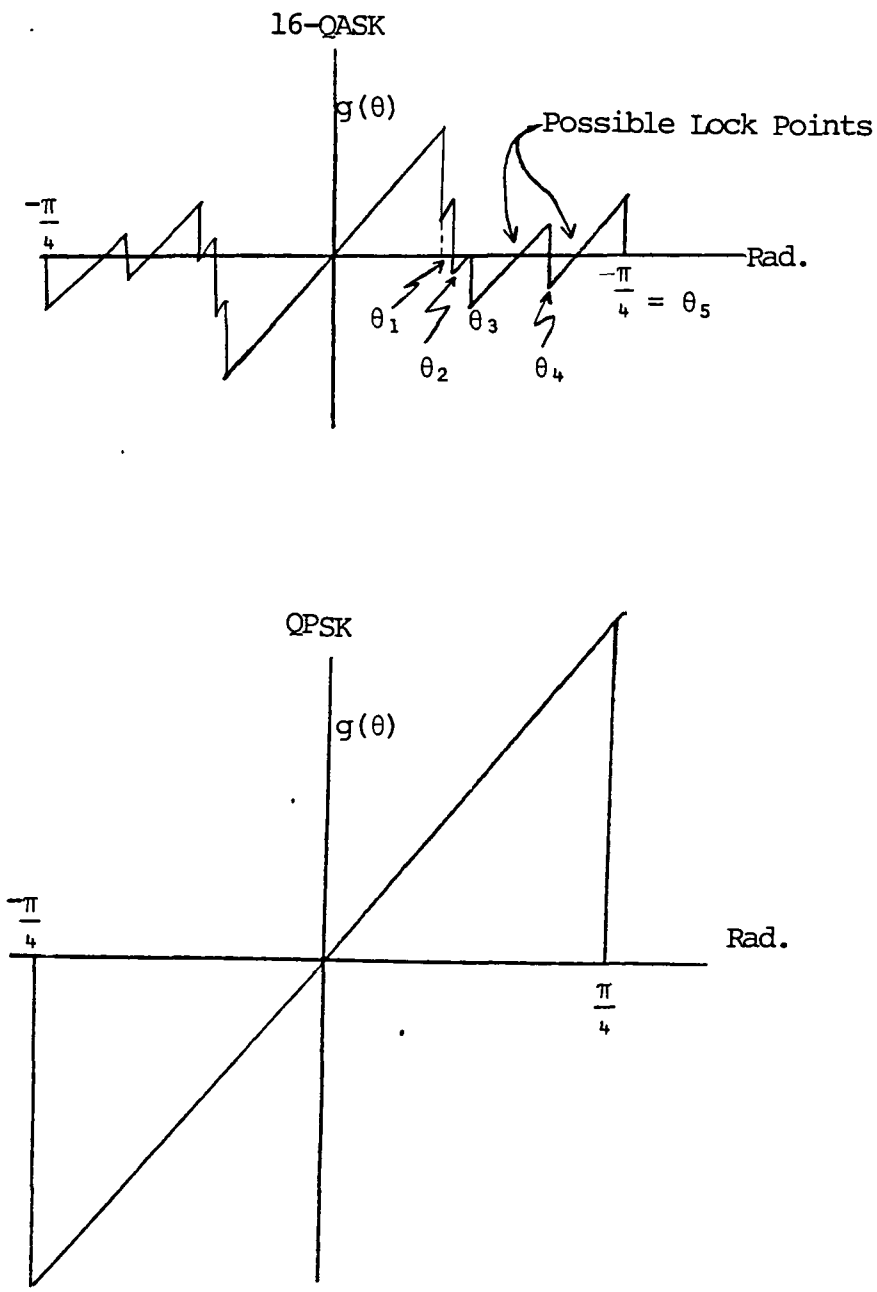
the phase error. These expected values are computed first by finding the reduction in the minimum distance from each signal to the decision boundary due to a fixed phase error, then finding all the probabilities that an estimation of any one signal was mistaken for any of the other M-1 signals. All these probabilities are summed and normalized to a unit slope. An expression for g(θ) from [5] is presented below:

$$g(\Theta)=\frac{d_{dis}^2}{M^2 G'(0)}\sum_{i,j}(i\sin\Theta+j\cos\Theta)\ \cdot\ \sum_{L} Q\left(\frac{d_{dis}}{\sqrt{2N_o}}(L-i\cos\Theta+j\sin\Theta)\right) \tag{4.34}$$

where L = 0, $\pm 2 \ldots \pm(M-1)$, and i, $j=\pm 2 \ldots \pm(M-1)$ and G'(0) is the slope of the function G(θ) at θ=0. Results for QPSK with two decision levels and 16-QASK with four decision levels are presented in figure 4.4 assuming SNR= ∞ .

Through inspection of the S curves it is observed that there is a four-fold ambiguity at $n\pi/2$ for both QPSK and 16-QASK (the 16-QASK case has several others also as shown in Figure 4.4). This can be interpreted in an intuitive manner by viewing Figure 3.1 for QPSK and Figure 3.4 for 16-QASK. As the phase error gets larger (causing errors in the estimates) the value of the second summation of

Figure 4.4 S-Curves for QPSK and 16-QASK



equation (4.34) gets smaller causing the expected value to drop. This drop in the expected value of the error signal may cause it to cross the axis, however these crossings are not stable lockpoints since they have a negative slope. Also any false lock points at $n\pi/2$ intervals can be resolved through the use of differential encoding. The lock points of concern are those shown in the S curve of the 16-QASK case that occur at points other than intervals. The error signal in this case has discontinuities at values of phase error where the four signals of the first quadrant cross decision thresholds. These values, as shown in the phase noise calculation of Chapter 3, are at

$$\Theta_1 = 16.88°,\ \Theta_2 = 18.43°,\ \Theta_3 = 20.80°,\ \Theta_4 = 32.33°,\ \text{and}\ \Theta_5 = 45.00°$$

These discontinuities do cause positive slope crosses of the axis that may cause false lock points but only in the theoretical case of SNR=∞. At lower SNRs the noise prevents these points from being stable lock points. For all practical purposes, at high SNR, the loop would stay locked at $n\pi/2$. It is only during acquisition at high SNR that false lock problems occur and methods to prevent this are discussed in Chapter 6.

CHAPTER FIVE

DUAL-MODE MODEM HARDWARE DESIGN

The original goals outlining this research came from an investigation on a high speed (1 gigabit/sec.) dual-mode modem. During this investigation it was determined to be desirable to design, build, and test a scaled model of the high-speed model which would allow testing of the basic proposed concepts. This chapter covers the design of the scale model, with only the highlights and performance specification of the hardware being covered since it would be tedious to cover all the details of the design. The basic design constraints were:

1. Carrier frequency at 10 MHz
2. Selectable QPSK or 16-QASK modulation
3. Fixed symbol rate for both QPSK and 16-QASK
4. Low-noise carrier recovery loop (narrow bandwidth) with an external control to provide frequency sweeping for acquisition

5.1 Hardware Design

The modem is broken down into four assemblies, RF front end, detection filter, decision feedback arm and oscillator. The divisions of the breakdown are illustrated in Figure 5.1 with detailed schematics of the

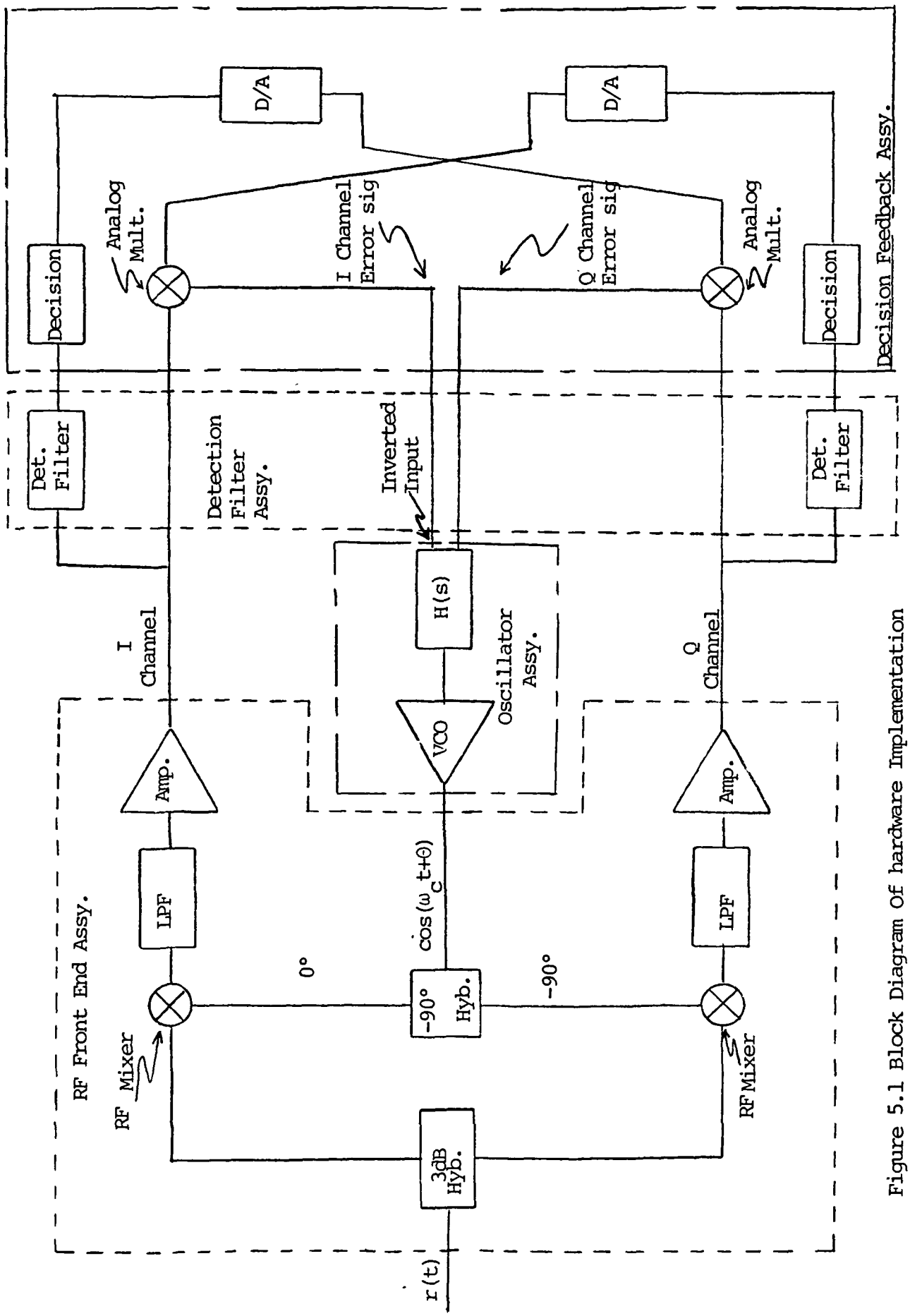


Figure 5.1 Block Diagram Of hardware Implementation

design presented in Appendix A.

The RF front end receives an incoming signals and splits it into two signals using a 3 dB "hybrid." These two signals are then mixed with two quadrature references that are generated by taking the output of the VCO and passing it through a hybrid with outputs at 0° and 90°. The products at the outputs of the RF mixers are then passed through a low-pass filter followed by a baseband amplifier that has 30 dB of gain in the passband. The measured frequency response of this configuration is shown in Figure 5.2. Some peaking is noticable in the response at higher frequencies which is caused by a feedforward network that was used to extend the operating frequency of the operational amplifier.

The outputs of the baseband amplifiers are passed through the detection filter, then on to the decision feedback arms where decisions are made on the signals, (four-level decisions for 16-QASK and two-level for QPSK). The decisions are made through the use of an A/D flash converter technique employing high-speed voltage comparators. These estimates are then D/A converted using a R-2R ladder network, producing an analog signal which is multiplied by the amplified baseband signal of the opposite arm. This multiplication function is performed through the use of a four-quadrant analog multiplier. The outputs from the analog multipliers are what determine the conversion

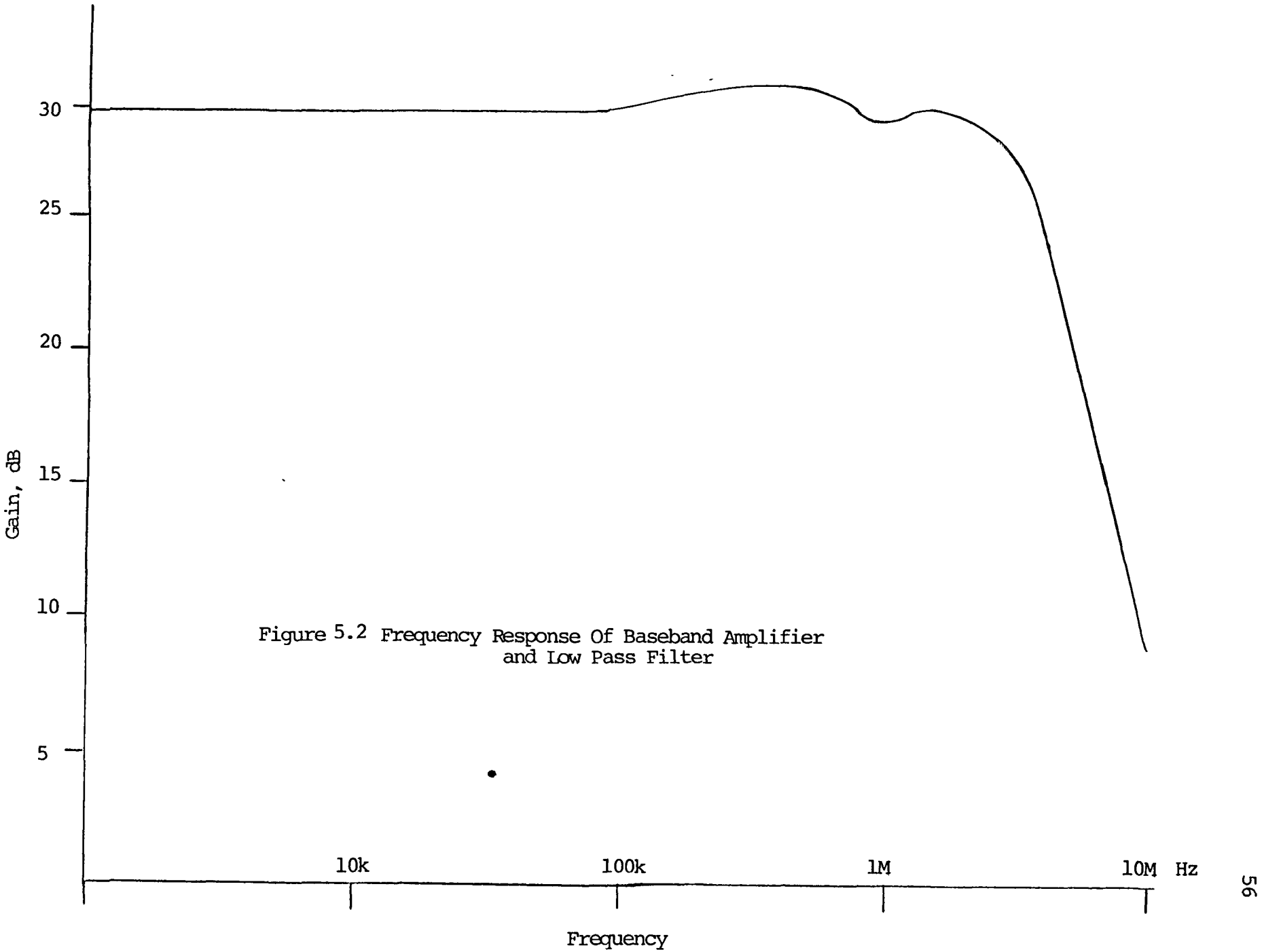


Figure 5.2 Frequency Response Of Baseband Amplifier and Low Pass Filter

gain of the phase detector.

A conventional linearized model of a PLL [12] - [17] is presented in Figure 5.3. K_1 is the phase detectors conversion gain, and F (s) is the loop filter's frequency response with any additional gain that is needed (i.e., an active filter) being labeled K_3. The parameter K_2 is the VCO sensitivity in rad/sec/V. Specifications by the vendor, with measurements to verify them, showed K_2 = 3768 (rad/sec/V) with a control voltage range of 0 to 5V.

The next step is to write the transfer function of the loop from input to output: [12]

$$H(s) = \frac{K_1K_2K_3F(s)}{s + K_1K_2K_3F(s)} \qquad (5.1)$$

It is necessary to know the fixed gain K_1 since K_3 is adjustable in our design and can be varied to obtain any desired loop gain. The gain of K_1 is determined by the RF front end and the decision feedback arm. Due to the many variables involved with these two assemblies, the easiest and most accurate means of finding K_1 is through measurement. In order to make this measurement the loop must be run open-loop. To perform this, the VCO is driven by a constant control voltage and the amplitudes of error signals out of the analog multipliers of each decision feedback arm are measured, thereby determining the value

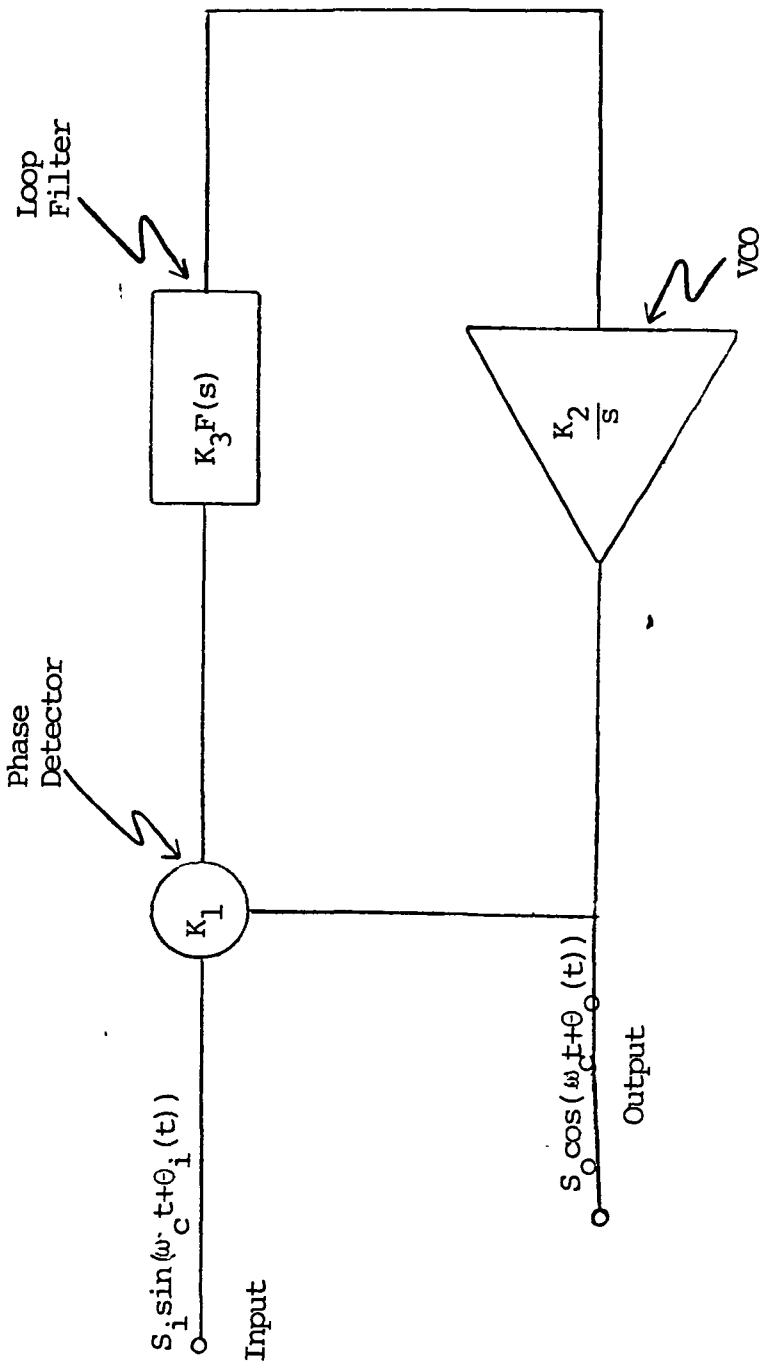


Figure 5.3 Linearized Phase Lock Loop Model

of K1. Assuming that the outputs of the baseband amplifiers are held to a constant ±2 volts, K_1 measures to be 0.7 v/rad.

The next step is to determine the desired response of the loop filter from the known parameters. From the literature [12], [13], we find that to obtain a narrow loop bandwidth to reduce noise and still maintain a large tracking range with stability, a second-order loop response is desired. If the loop is allowed to take the form of an inperfect second-order loop, the filter not only becomes practical to implement, but also permits the adjustment of the natural frequency ω_n and the damping coefficient ζ. The filter is of the form of a low-pass filter with phase lead as shown in equation 5.2:

$$F(s) = \frac{1 + s\tau_1}{1 + s\tau_2} \qquad (\tau_1 > \tau_2) \tag{5.2}$$

Using the above expression for the filter and substituting into the transfer response of the loop yields:

$$H(S) = K(\tau_1/\tau_2)\frac{(s + \frac{1}{\tau_2})}{s^2 + (\frac{1}{\tau_1} + K\frac{\tau_2}{\tau_1})s + \frac{K}{\tau_1}} \tag{5.3}$$

where $K=K_1K_2K_3$. We know from measurements that K_1 = .7 v/rad and K_2 = 3768 rad/sec/V. Then

$K = K_1K_2K_3 = 2638K_3$.

From equation 5.3 and knowing the characteristics of a second-order system we can find:

$$\omega_n = \sqrt{K/\tau_1} \tag{5.4}$$

$$\zeta = \frac{1 + K_2}{2\sqrt{K\tau_1}} \simeq \frac{\tau_2}{2}\sqrt{K/\tau_1} = \frac{\tau_2}{\tau_1}\omega_n \tag{5.5}$$

$(\tau_2 K >> 1)$

A damping coefficient of .7 was selected. Noise rejection was desired from the loop so the natural frequency was selected to be $5X10^3$ rad/sec, about one-hundredth of the symbol rate. Since the sensitivity of the VCO is relatively low, a DC gain of 30 was assumed for K_3. Therefore we calculate

$$\zeta = 0.7 \simeq \frac{\tau_2}{\tau_1}\omega_n \qquad \boxed{\tau_2 = 283\ \mu\text{sec.}}$$

$$K = 30(2638) = 79.1X10^3 \qquad \boxed{\tau_2 K = 22 >> 1}$$

$$\tau_1 = \frac{K}{\omega_n^2} \qquad \boxed{\tau_1 = 3.2\ \text{msec.}}$$

Thus the required loop filter is of the form:

$$F(s) = \frac{30(1+s283.0X10^{-6})}{(1+s3.2X10^{-3})}$$

The measured frequency response for this filter is shown in Figure 5.4. Due to the limitation on component values the following are the actual time constants:

$$\tau_2 = 270 \text{ μsec.}$$

$$\tau_1 = 2.5 \text{ msec.}$$

The closed loop transfer function for the actual loop is given by:

$$H(s) = \frac{8.6X10^3 \, s + 3.2X10^6}{s^2 + 9.0X10^3 \, s + 31.9X10^6}$$

The input step-response of this system is presented in Figure 5.5. It is obvious that the settling time is extremely slow; i.e., 1 msec. and at our symbol rate of 500 K symbols/sec. this would mean a loss of 500 symbols. However this system was designed to optimize the noise bandwidth and not response time. In systems where good response time as well as good noise rejection is desired, a two filter system is often used. One filter is wideband for fast acquisition and once initial lock up is achieved a narrow band filter is switched in to reduce the noise bandwidth. Another method is to employ a ramp generator that controls the VCO causing it to sweep to get

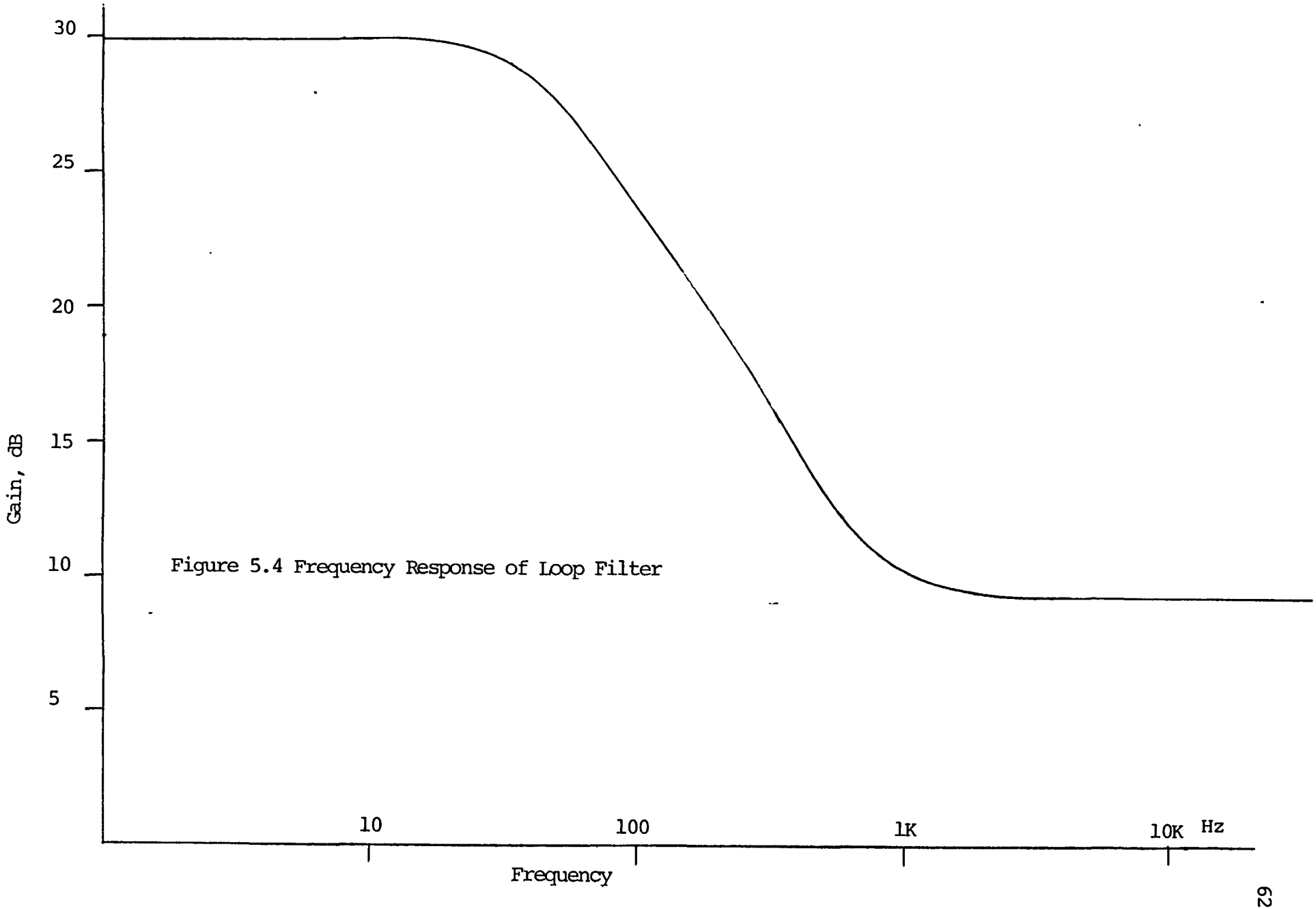


Figure 5.4 Frequency Response of Loop Filter

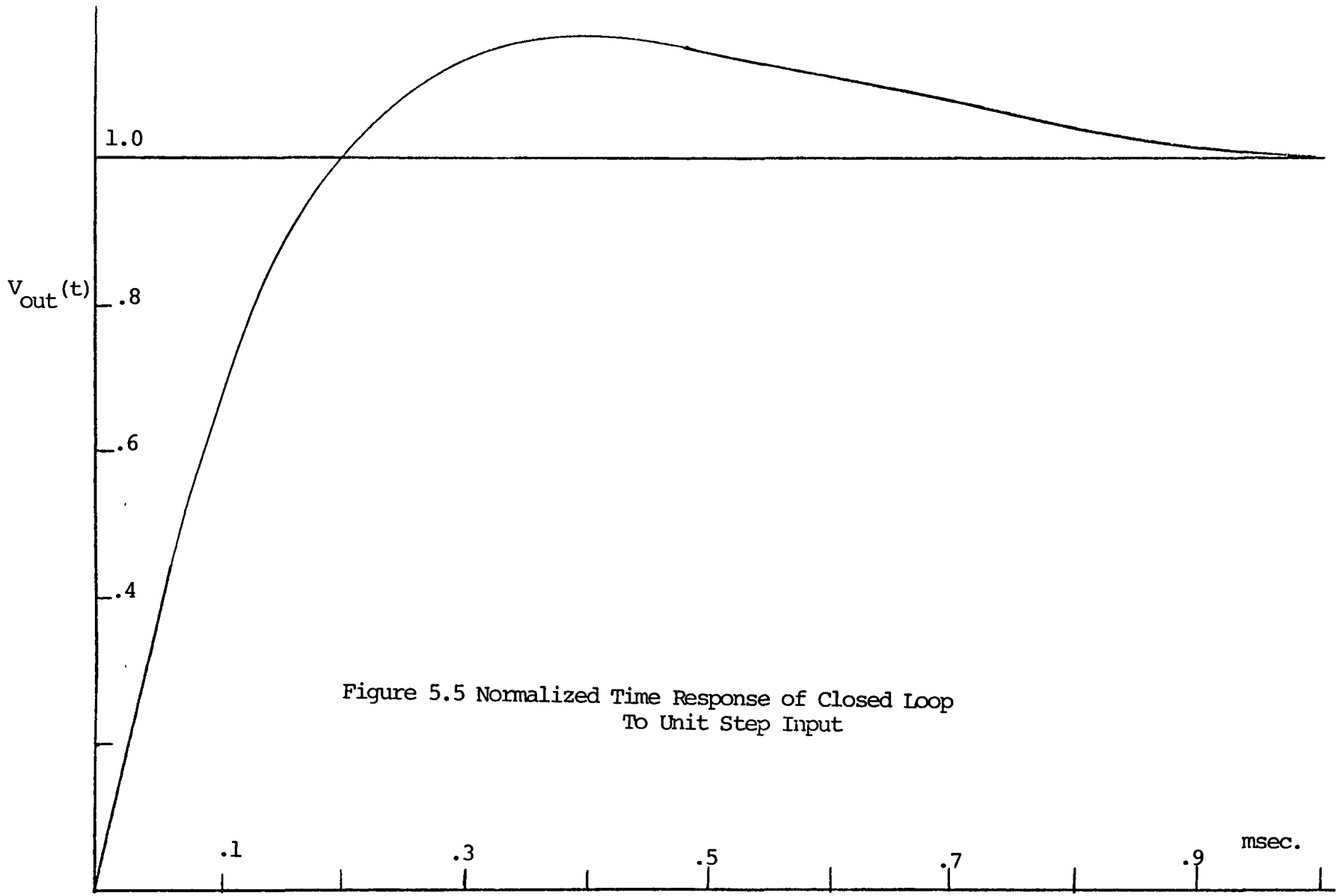


Figure 5.5 Normalized Time Response of Closed Loop
To Unit Step Input

its initial lock while still allowing a narrow bandwidth loop. The scale model system uses a sweep approach through the use of a manually-controlled potentiometer acting as the ramp generator.

The last component of the loop to be designed is the detection filter. Ideally this filter is an integrate-and-dump function operating at the symbol rate, assuming square wave data was sent. A suboptimal, but less complex, approach is to use a low pass filter with its cut-off frequency at about half the symbol rate, thus providing the integration function in a continuous manner. In this design the passive filter approach was used with a third-order gaussian filter response choosen due to its near-constant group delay through the pass band. Refer to Figure 5.6 for a measured response of the detection filter.

The design of the loop is now completed with detailed schematics of the design contained in appendix A. The next step is to calculate some of the operating parameters of the loop. The two of the most immediate interest are the acquisition range and the hold-in range. They are defined by [13] for a second-order loop as:

$$\omega_{acq} = 2\sqrt{K\omega_n + 1/2\tau_1} \qquad (5.6)$$

$$\omega_{hold\text{-}in} = K \qquad (5.7)$$

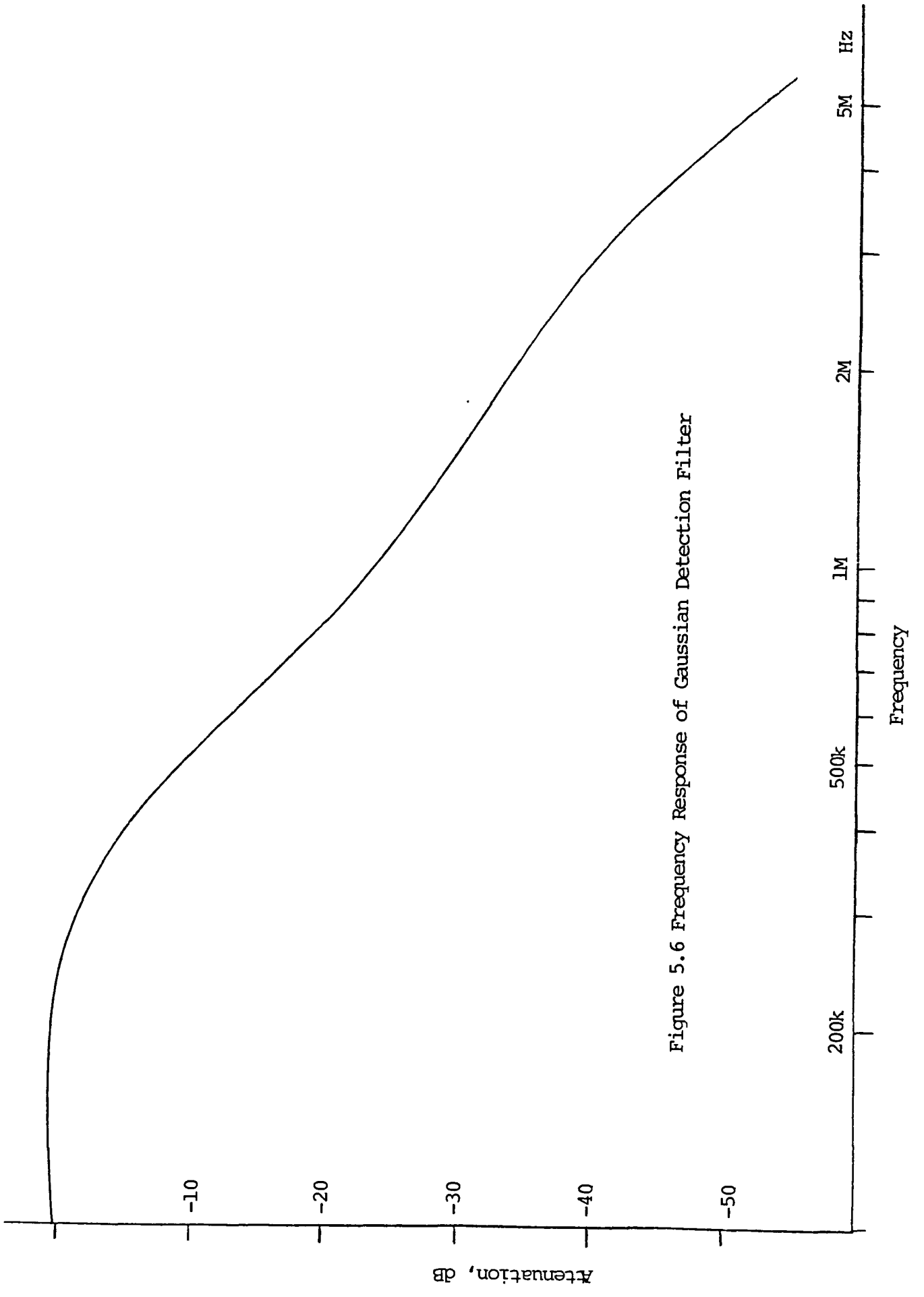


Figure 5.6 Frequency Response of Gaussian Detection Filter

Thus for the loop just designed a signal that is about 33 X 10^3 rad/sec away from the center carrier frequency can be brought into lock and will theoretically stay locked for a change of about 79 X 10^3 rad/sec as long as the VCO stays within its control voltage operating range. However, the pulling range of the VCO used is not large enough, allowing the loop to only stay locked for changes of about $33X10^3$ rad/sec.

5.2 Specifications

The following is a consolidated list of specification of the design of the dual mode modem.

Design Parameters

Carrier Frequency	10 MHz
Modulation techniques	QPSK, 16-QASK
Symbol rate	500 K symbols/sec.
Data rate	1 MBit/sec (QPSK)
	2MBit/sec (16-QASK)
Acquisition Range	5 KHz
Hold-in Range	12.5 KHz
Damping Factor	0.7

This concludes the discussion on the hardware design and in the next chapter measured results of the operation of the loop with possible design improvements are given.

CHAPTER SIX

RESULTS

6.1 Experimental Results

A working model of the dual-mode modem is pictured in Figure 6.1. To test the modem an eight -stage pseudorandom sequence is used as a data source. To simulate the transmission path an attenuator is employed allowing the SNR to be varied.

The modem for all modes of operation is held at a constant symbol rate, thus generating a spectrum described in equation 2.8 with the first null at the symbol rate, i.e. 500 KHz from the carrier for both QPSK and 16-QASK. The measured spectrum at the output of the modulator is shown in Figure 6.2 with expected first null at 500 KHz. The RF output in the time domain (upper display) and the random data stream of the I channel (lower display) of the modem in the QPSK mode are shown in Figure 6.3. Ideally the RF envelope is constant in this mode of operation but a slight variation is noticable. It is believed that this is caused by a slight inbalance in the characteristics of the RF mixers. The RF output and data input stream for one mixer of the I channel for 16-QASK modulation are shown in Figure 6.4. In this mode there should ideally be four distinct levels in the RF envelope. Figure 6.4 shows that there are generally, but with some variations. This again

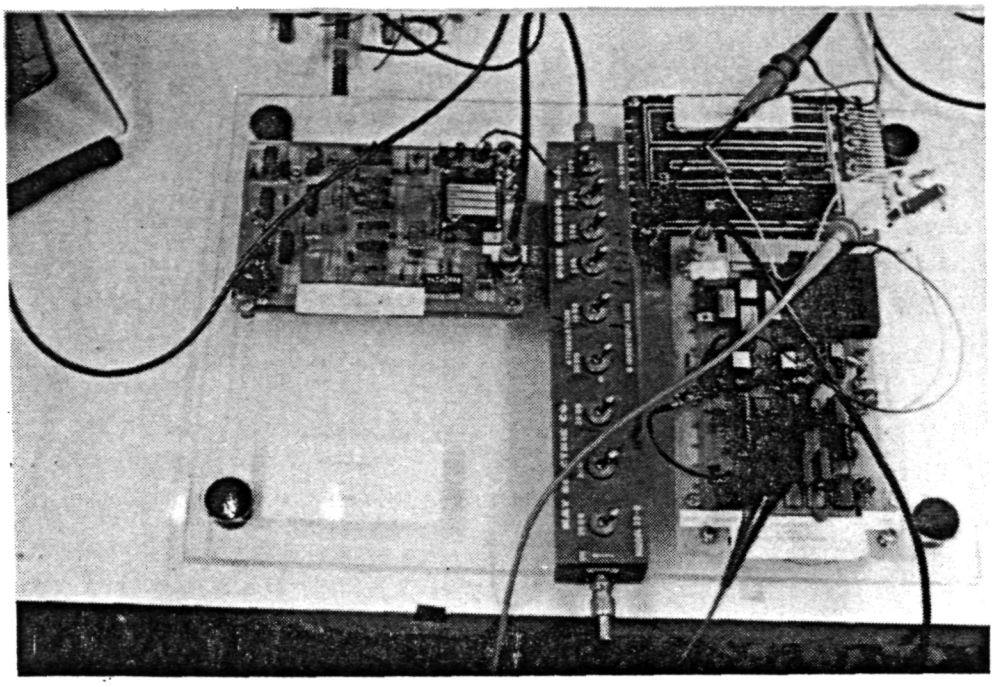


Figure 6.1 Hardware of Dual Mode Modem

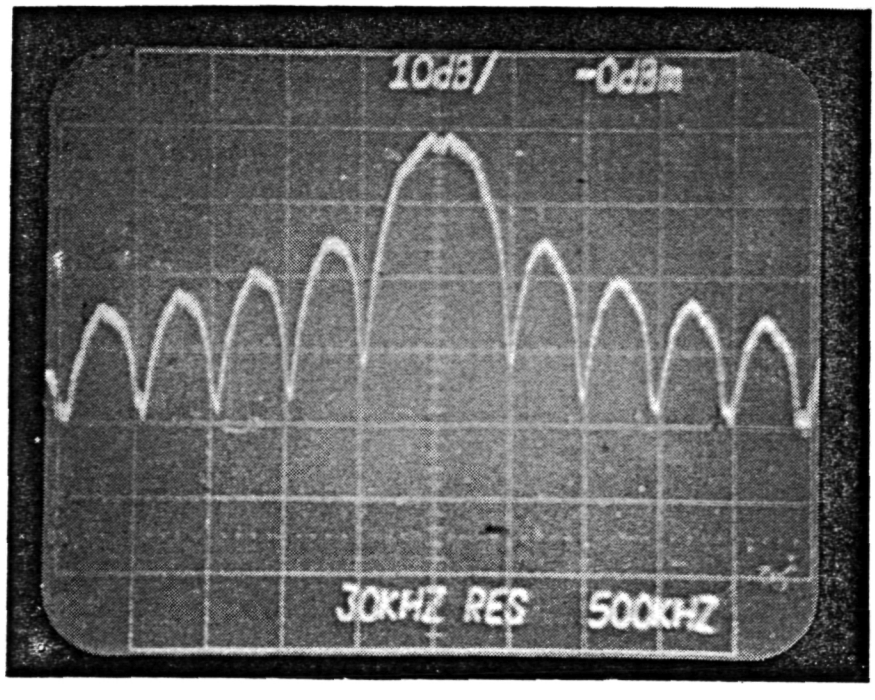


Figure 6.2 Output Spectrum of Modulator
H: 500 kHz/div.
V: 10dB/div.

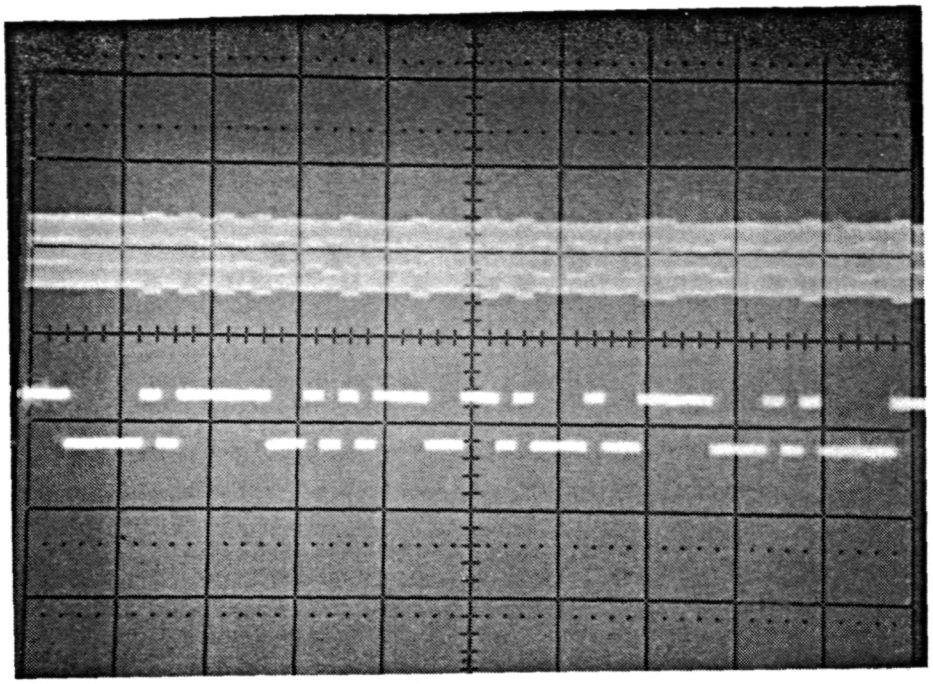


Figure 6.3 QPSK Mode Modulator Output (upper)
and Data Stream Input
H: 10 usec/div.

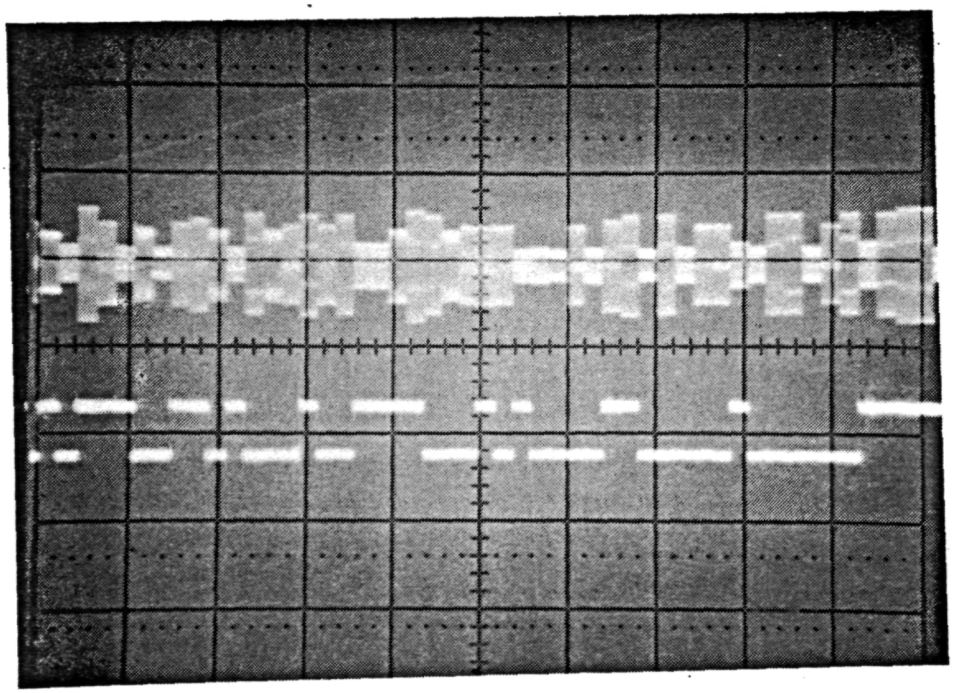


Figure 6.4 16-QASK Mode Modulator Output (upper)
and Data Stream Input, I Channel (lower)
H: 10 usec/div.

is due to the differences in the characteristics of the RF mixers used. This completes the measured results of the modulator section of the modem. Next are the results from the operation of the demodulator.

The demodulated information (upper display) before integration by the detection filter is shown with the corresponding data stream of the modulator in Figure 6.5. It appears that the data is inverted relative to what was sent, implying that the loop is locked to a false lock point of 180°, however this is not the case. The loop is locked to the proper point, and the inversion is due to the inverting nature of the baseband amplifier and is compensated for in an inversion of the output of the analog mixers. In Figure 6.6 the integration that is performed by the gaussian detection filter on the demodulated base band signal (upper trace) is displayed with the corresponding data of the modulator (lower trace). It is of interest to note the overshoot and ringing of the filter response that is quite prevalent when several bits of the same value occur in succession.

The next few figures demonstrate the problem of lock ambiguity that can occur without the use of differential coding or the use of known preamble to establish the proper initial lock point. Figure 6.7 shows the loop lock to a 90° false lock point which can be determined through comparison of the demodulated baseband (upper trace) and

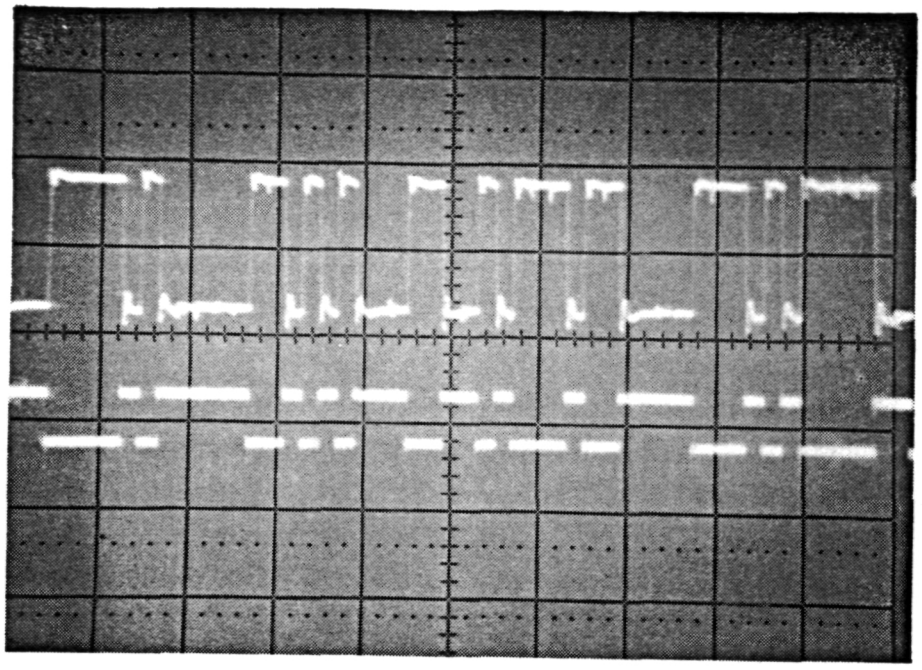


Figure 6.5 QPSK Mode Demodulated Data Before Filter (upper) and Data Stream Input I Channel (lower)
H: 10 usec/div.

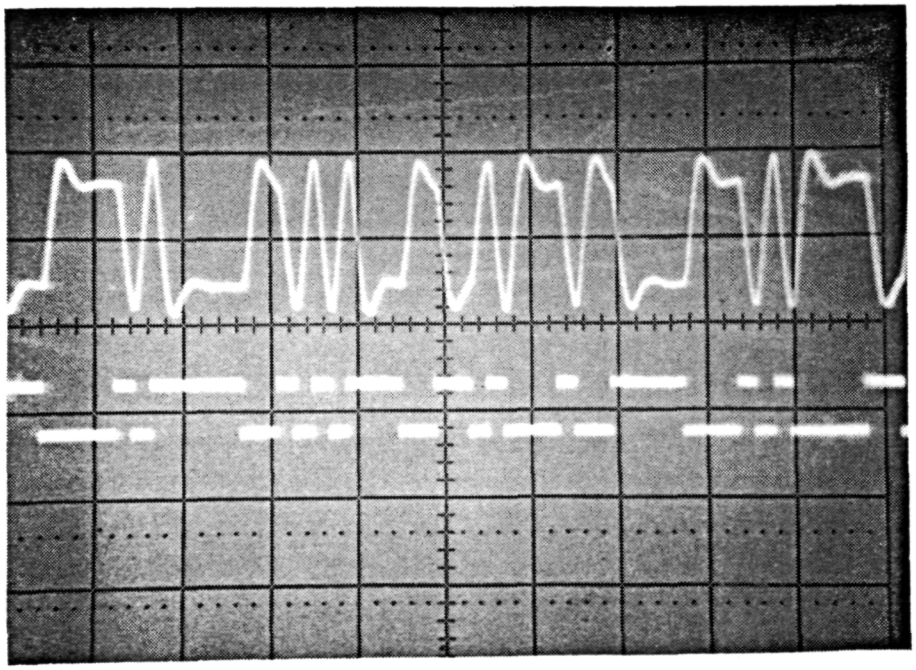


Figure 6.6 QPSK Mode Demodulated Data After Filter (upper) and Data Stream Input I Channel (lower)
H: 10 usec/div.

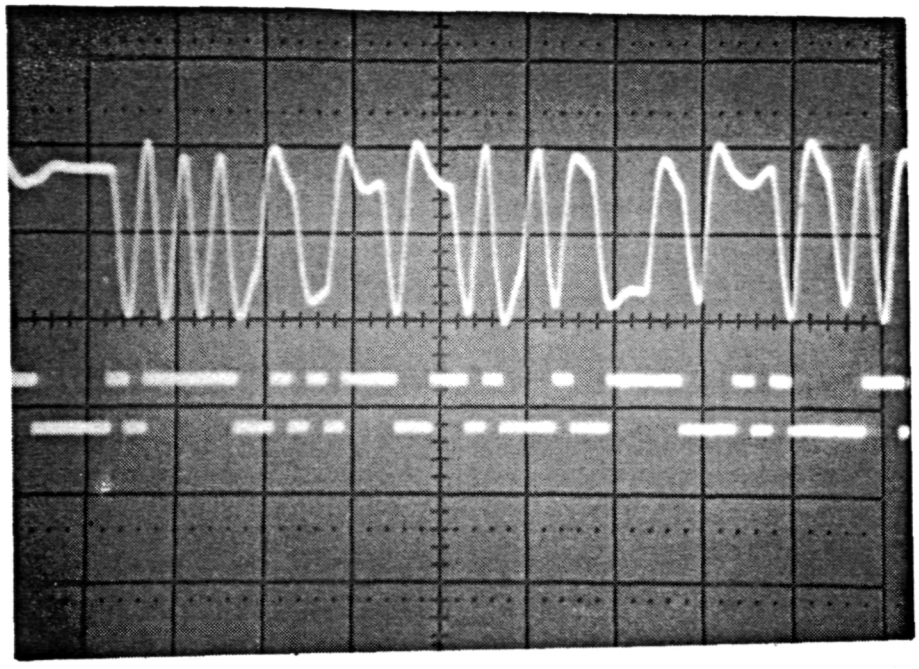


Figure 6.7 QPSK Mode 90° False Lock Point
H: 10 usec/div.

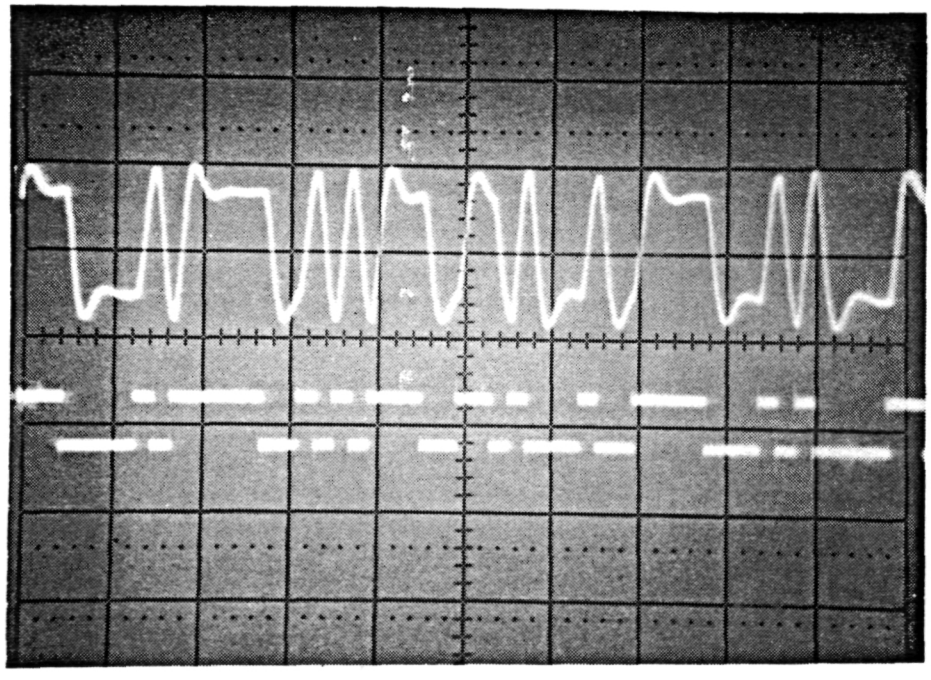


Figure 6.8 QPSK Mode 180° False Lock Point
H: 10 usec/div.

the data stream of the modulator (lower trace). Examples of 180° false lock point Figure (6.8) and the other 270° false point (Figure 6.9) are also shown. In figure 6.10 the eye pattern for QPSK is shown with the eye pattern before the filter (upper tract) showing no intersymbol interference (ISI) and the eye pattern after the filter (lower trace) showing some ISI as expected. This is due to imperfect data filtering.

The demodulated data during 16-QASK modulation is shown in Figure 6.11. The display is taken before the detection filters (upper trace) and as can be seen there are four distinct levels. In Figure 6.12 the integration operation of the detection filter is again shown and it can be seen that the overshoot response greatly distorts the four-level nature of the signal. This ISI problem is shown more vividly in the eye pattern displays of Figure 6.13. The eye pattern before the detection filter shown in the upper trace and the ISI effects of the filter are shown in the lower trace.

Figure 6.14 and Figure 6.15 summarize the operation of the modem with the QPSK and 16-QASK constellations at shown respectively. There is some noticable distrotion in the constellations. This is believed to be due to 90° hybrids of the system not being at perfect quadrature alignment.

6.2 Design Improvements

The following is a list of possible design

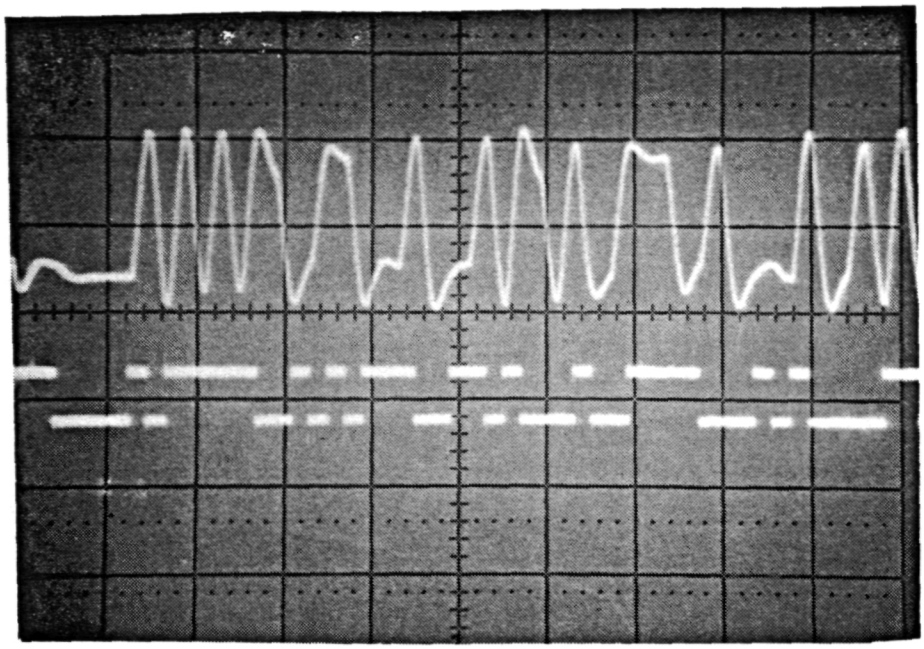


Figure 6.9 QPSK Mode 270° False Lock Point
H: 10 usec/div.

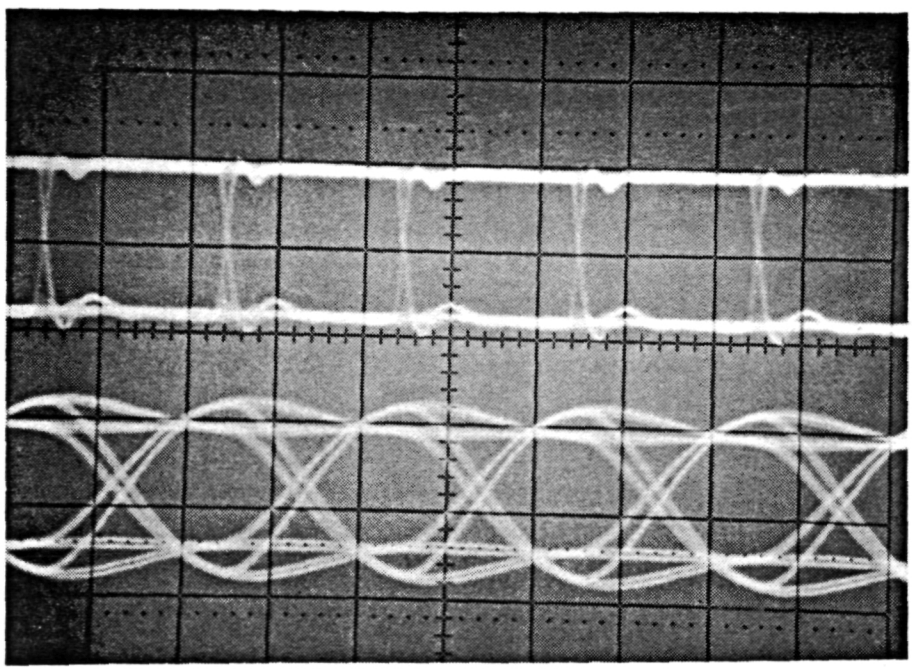
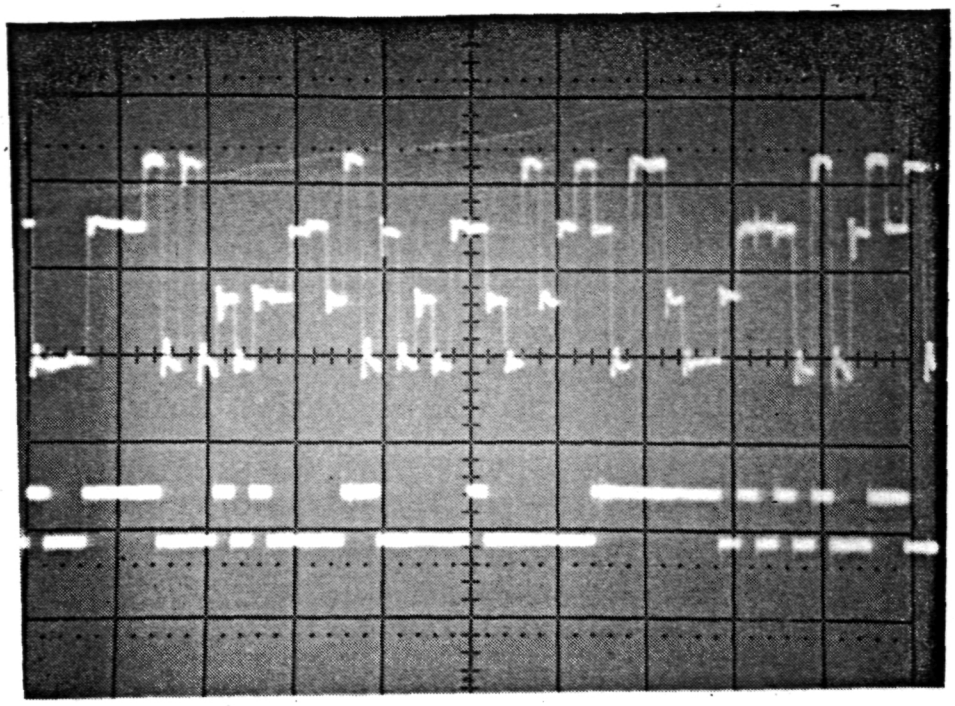
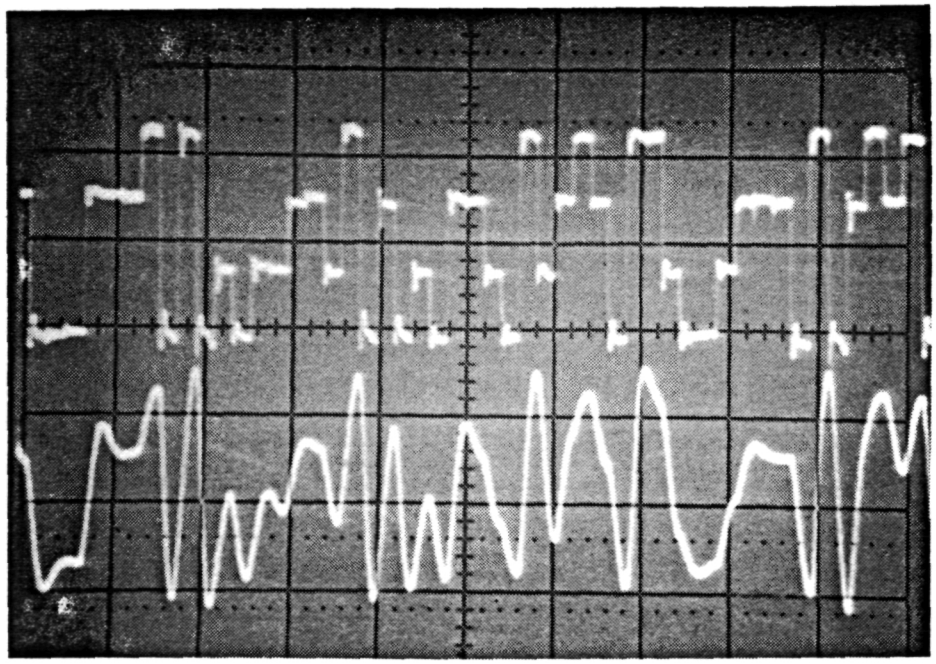


Figure 6.10 QPSK Mode Eye Pattern
Upper Trace Before Filter
Lower Trace After Filter
H: 1 usec/div.



1v/div.

Figure 6.11 16-QASK Mode Demodulated Data Before Filter (upper) and Data Stream Input I Channel (lower)
H: 1 usec/div.



1 v/div.

Figure 6.12 16-QASK Mode Demodulated Data After Filter (upper) and Data Stream Input I Channel (lower)
H: 1 usec/div.

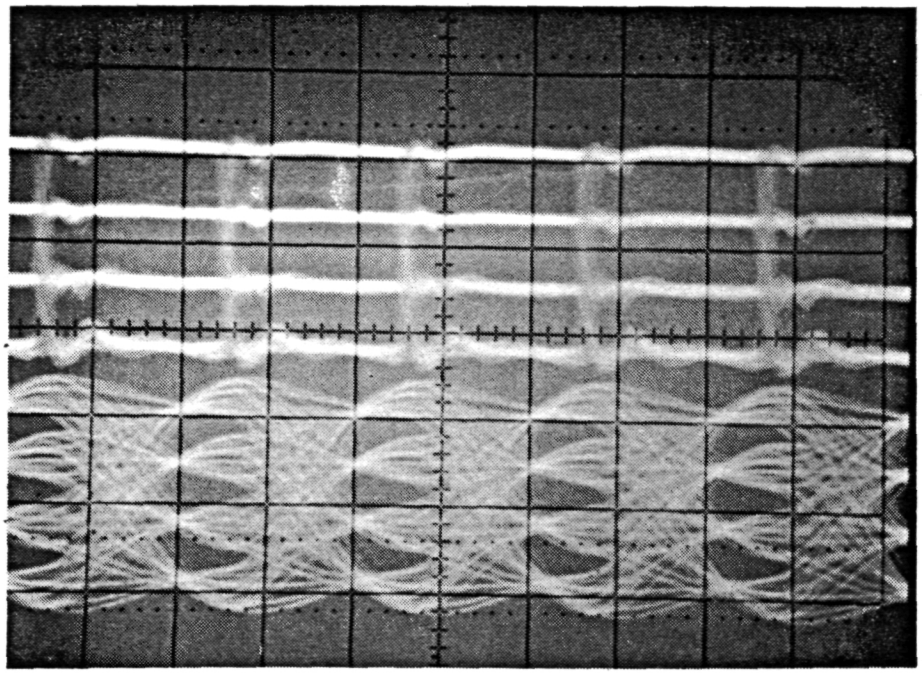


Figure 6.13 16-QASK Mode Eye Pattern
Upper Trace Before Filter
Lower Trace After Filter
H: 1 usec/div.

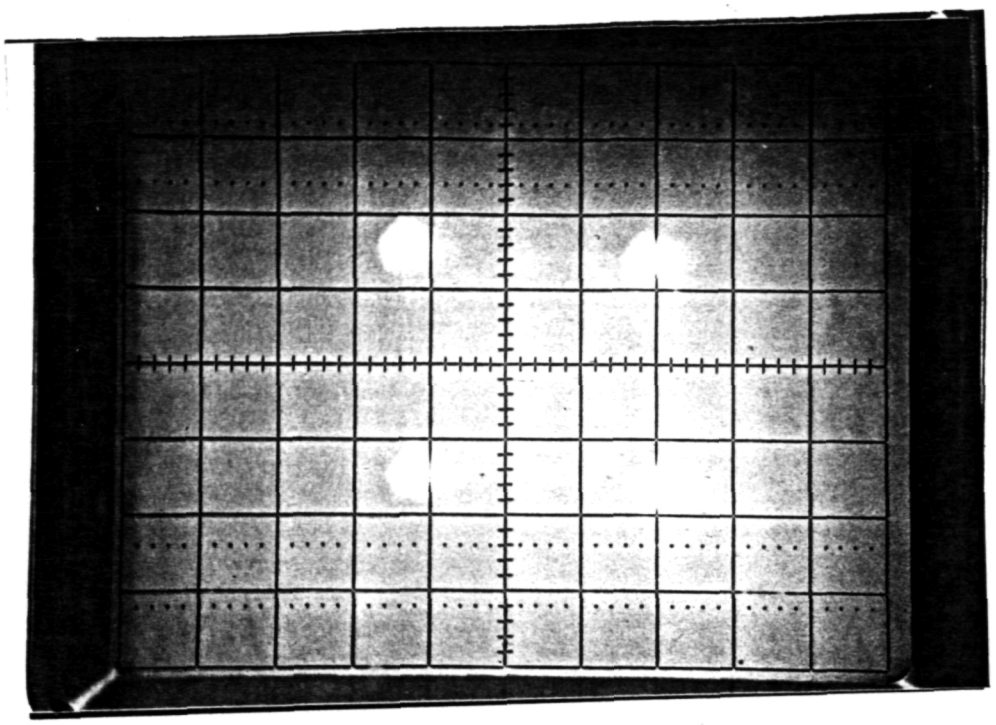


Figure 6.14 QPSK Constellation

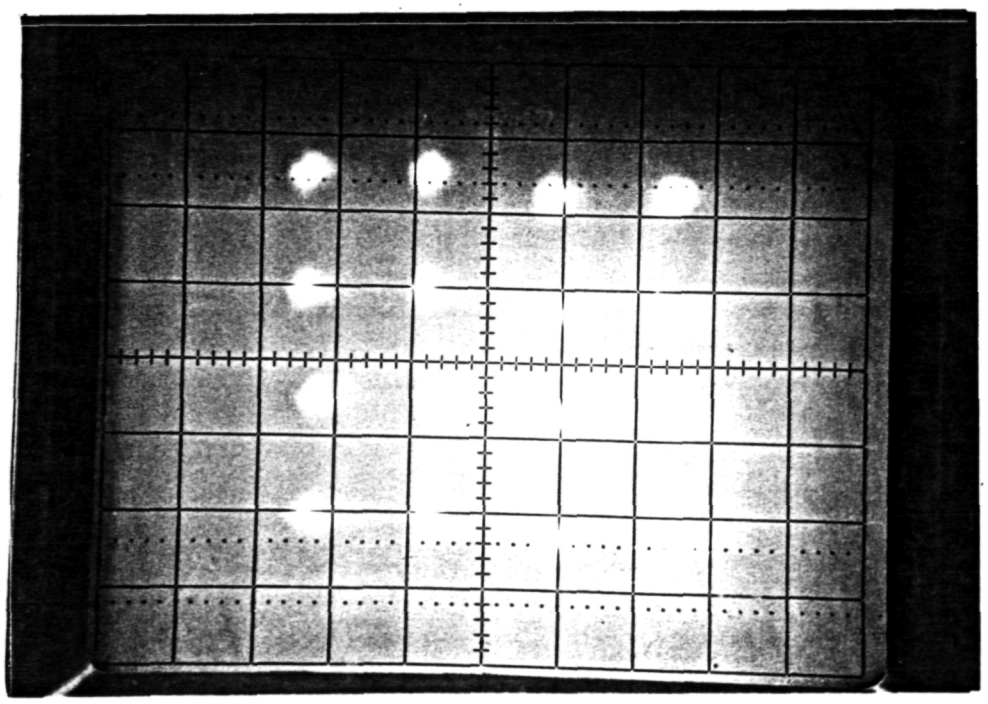


Figure 6.15 16-QASK Constellation

improvements that could be incorporated in order to improve the performance of the modem.

1. Automatic means of resolving the undesired lock points is needed. Differential coding can be employed but due to possible locking that can occur at points other than $n\pi/2$ an appropriate known prefix sequence must also be used to establish initial lock up.
2. Improve VCO frequency pulling range (now limited to $\pm$ 3kHZ) in order to allow more loop gain and increase acquisition range.
3. Incorporate a sweep generator to control the VCO for initial lock up, thus removing the need for manual control of initial lock.
4. Better control of logic levels which drive the R, 2R network for the D/A function, thus reducing quantization error in the decision feedback loop.
5. Better 90° hybrids to provide true quadrature references.
6. Gain adjustments in each channel of the transmitter and receiver in order to remove some of the amplitude differences.
7. Detection filter that produces less ISI than the present one.

CHAPTER SEVEN

CONCLUSION

The selectable use of either QPSK or 16-QASK modulation within a single modem provides the option of exploiting either energy or bandwidth efficiency. The QPSK modulation scheme provides energy efficiency while a 16-QASK scheme provides better use of bandwidth with some degradation in energy efficiency. These two modes are highly compatible for implementation in a single modem in that 16-QASK is realizable as a super-position of two QPSK signals, with one layer 6 dB weaker than the other. Due to the compatibility of the two modulation schemes, a dual-mode modem comprised of QPSK and 16-QASK is easily achieved and also provides system flexibility.

It was shown there is a need for accurate tracking of the carrier of the incoming signal. A computer analysis of the degradation in SER for QPSK and 16-QASK with fixed phase error indicated that an energy increase of roughly 4 dB is needed to maintain a SER of $1X10^{-5}$ for QPSK with 20° of phase error and 16-QASK with 7° phase error.

The decision feedback loop was selected for use in the dual-mode modem. The decision feedback method is capable of avoiding the problem of pattern jitter in the 16-QASK mode when four level decisions are made, providing good loop tracking performance. The system complexity is not

inhibiting, the signal processing is done at baseband avoiding the complication of processing at the carrier frequency. The only change needed for use with either modulation scheme is the number of decision levels, two levels for QPSK and four levels for 16-QASK. Two-level decisions can be used with 16-QASK and pattern jitter can be avoided, provided the loop bandwidth is much smaller than the symbol rate, i.e. ($B_L << R_S$).

A working model of a selectable dual-mode, QPSK or 16-QASK modem was constructed. The dual-mode operates at a carrier frequency of 10 MHz and at a fixed symbol rate of $500X10^3$ symbols per second. The carrier recovery method used is a decision feedback type and is capable of either two level decisions (QPSK) or four level decisions (16-QASK).

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APPENDIX A

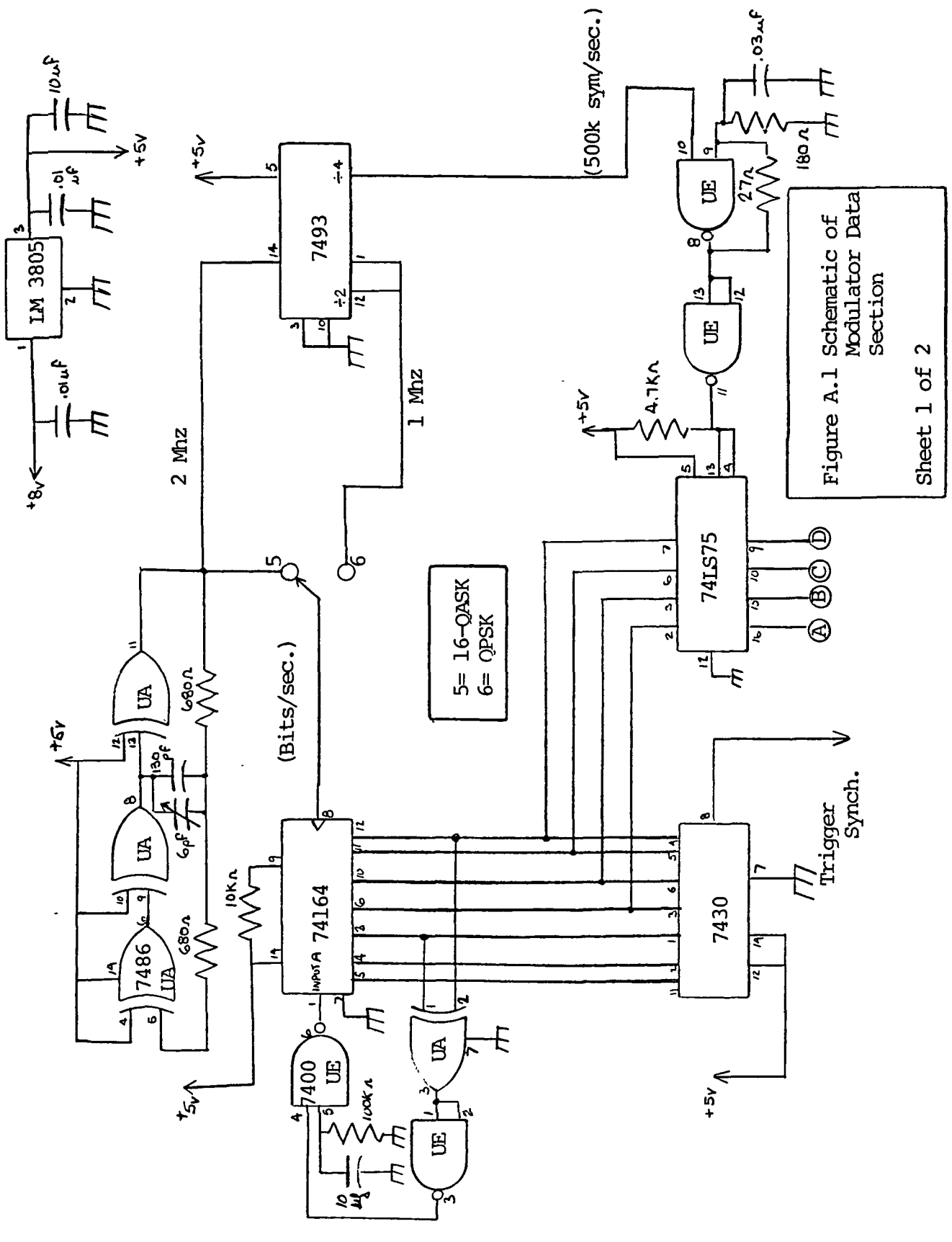
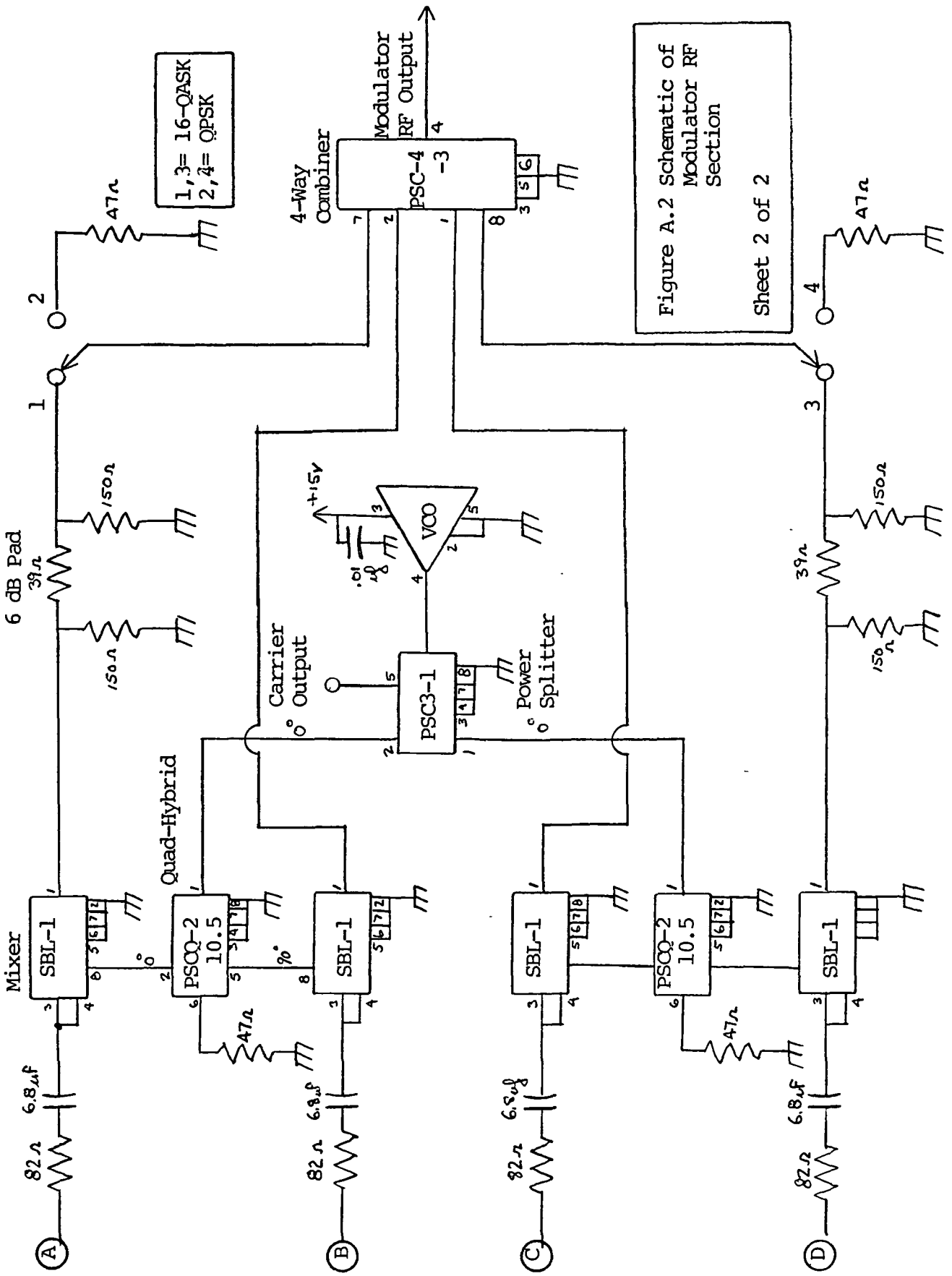
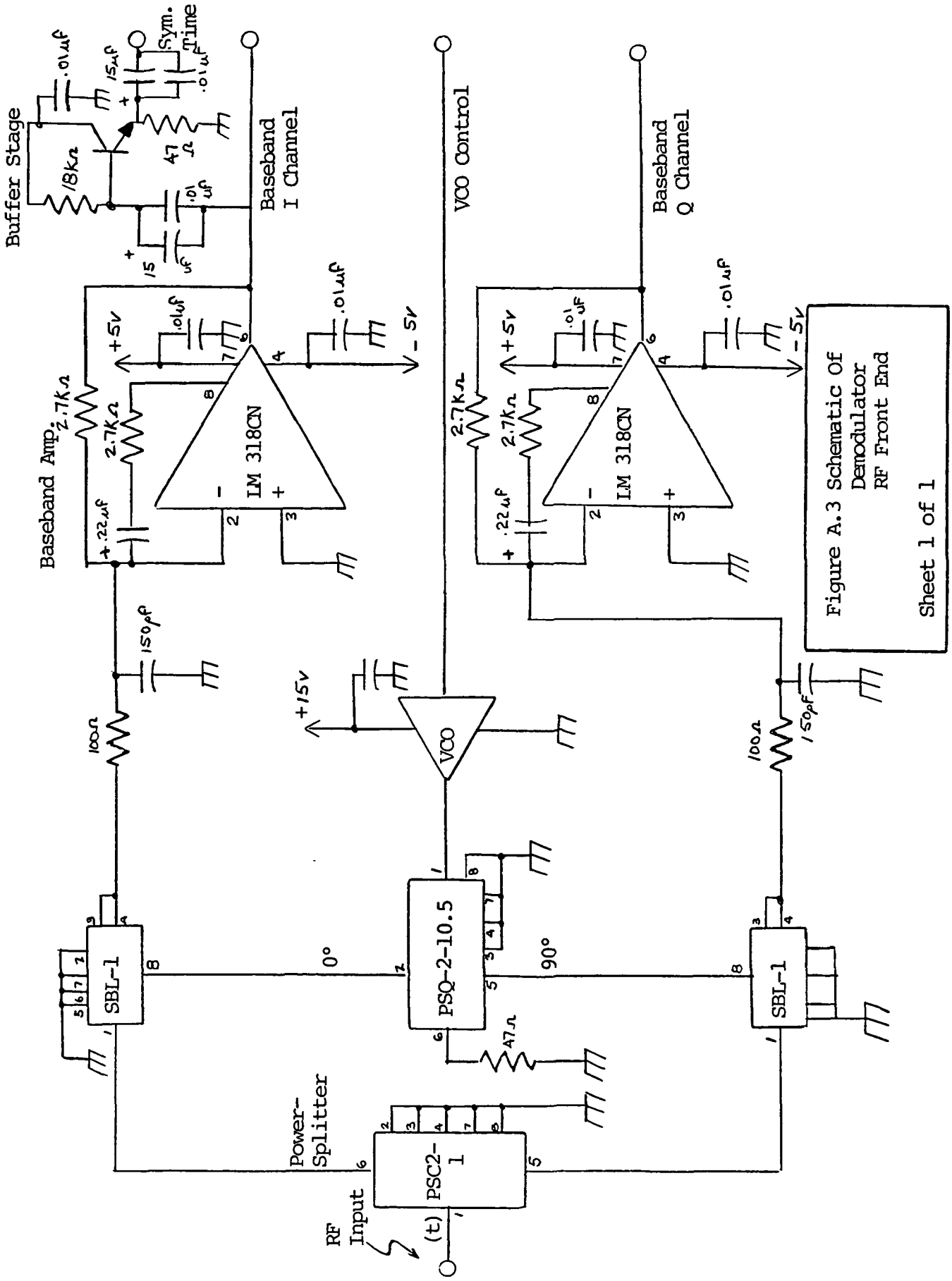
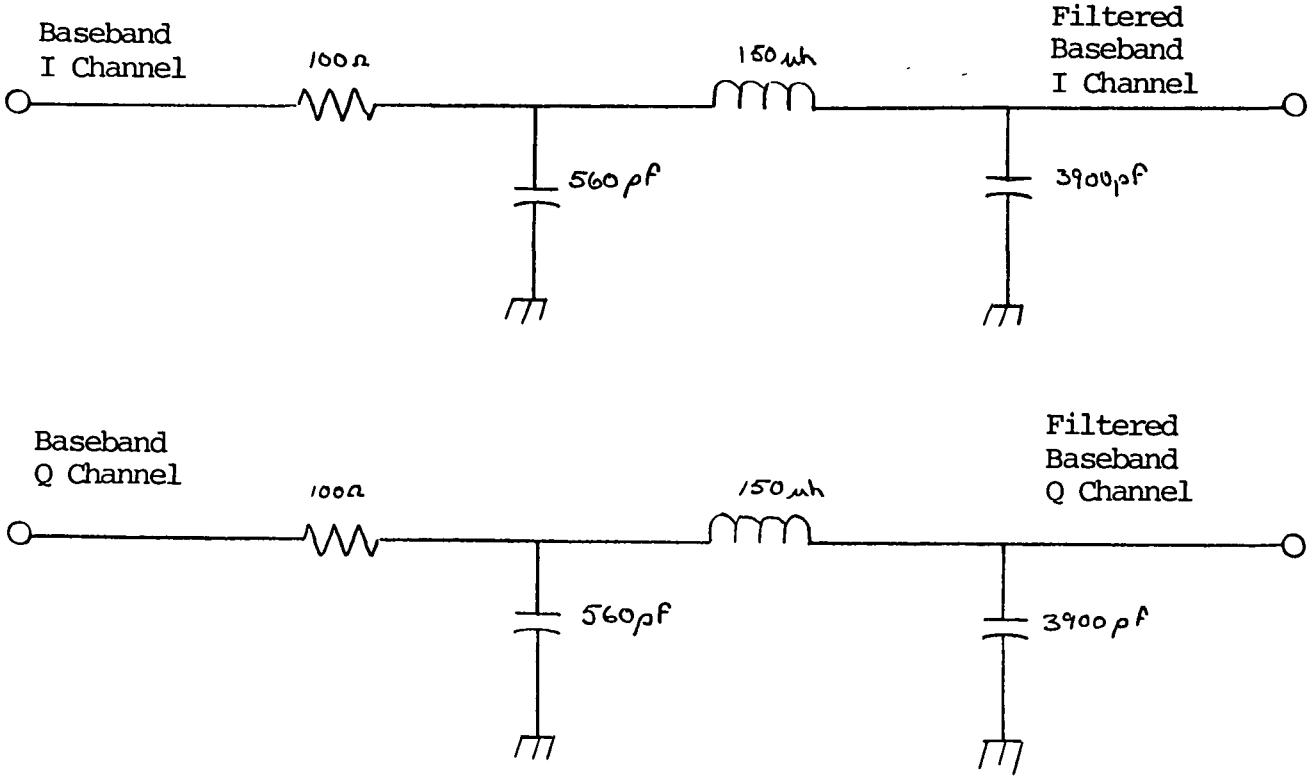


Figure A.1 Schematic of Modulator Data Section

Sheet 1 of 2


1,3= 16-QASK
2,4= QPSK
4-Way Combiner
PSC-4 -3
Modulator RF Output
Figure A.2 Schematic of Modulator RF Section
Sheet 2 of 2
6 dB Pad
39Ω
150Ω
47Ω
+15V
.01 μF
VCO
PSC3-1
Carrier Output
Power Splitter
Quad-Hybrid
Mixer
SBL-1
PSCQ-2 10.5
82Ω
6.8μF
A
B
C
D


Buffer Stage
.01μF
15μF
Sym. Time
.01μF
18kΩ
47Ω
.01 μF
15 μF
Baseband I Channel
VCO Control
Baseband Q Channel
Baseband Amp.
2.7kΩ
2.7kΩ
.22μF
.01μF
+5V
-5V
LM 318CN
150pF
100Ω
+15V
VCO
SBL-1
PSQ-2-10.5
0°
90°
47Ω
Power-Splitter
PSC2-1
RF Input
(t)
Figure A.3 Schematic Of Demodulator RF Front End
Sheet 1 of 1



Sheet 1 of 1

Figure A.4 Schematic of Demodulator Detection Filter

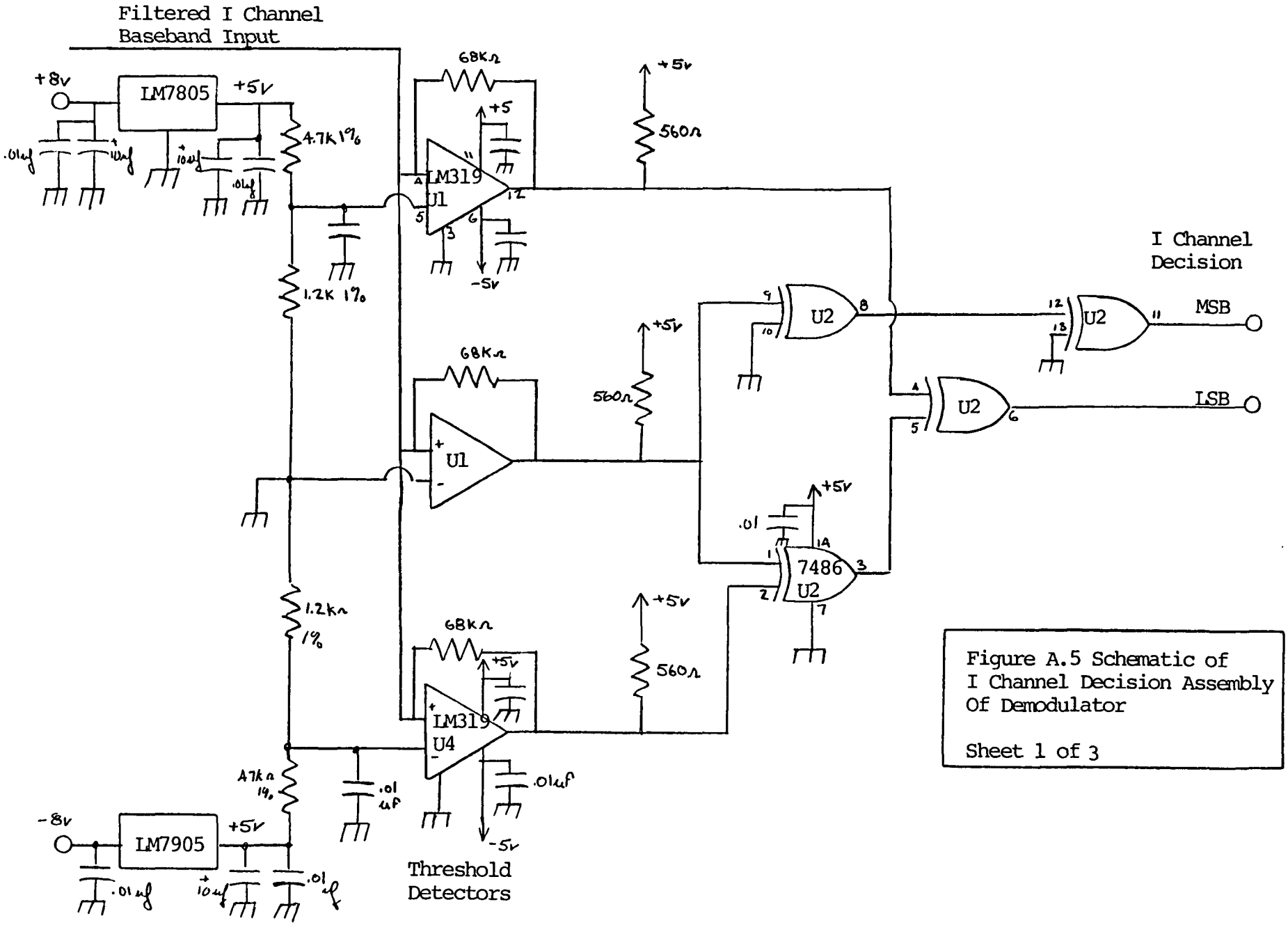


Figure A.5 Schematic of
I Channel Decision Assembly
Of Demodulator

Sheet 1 of 3

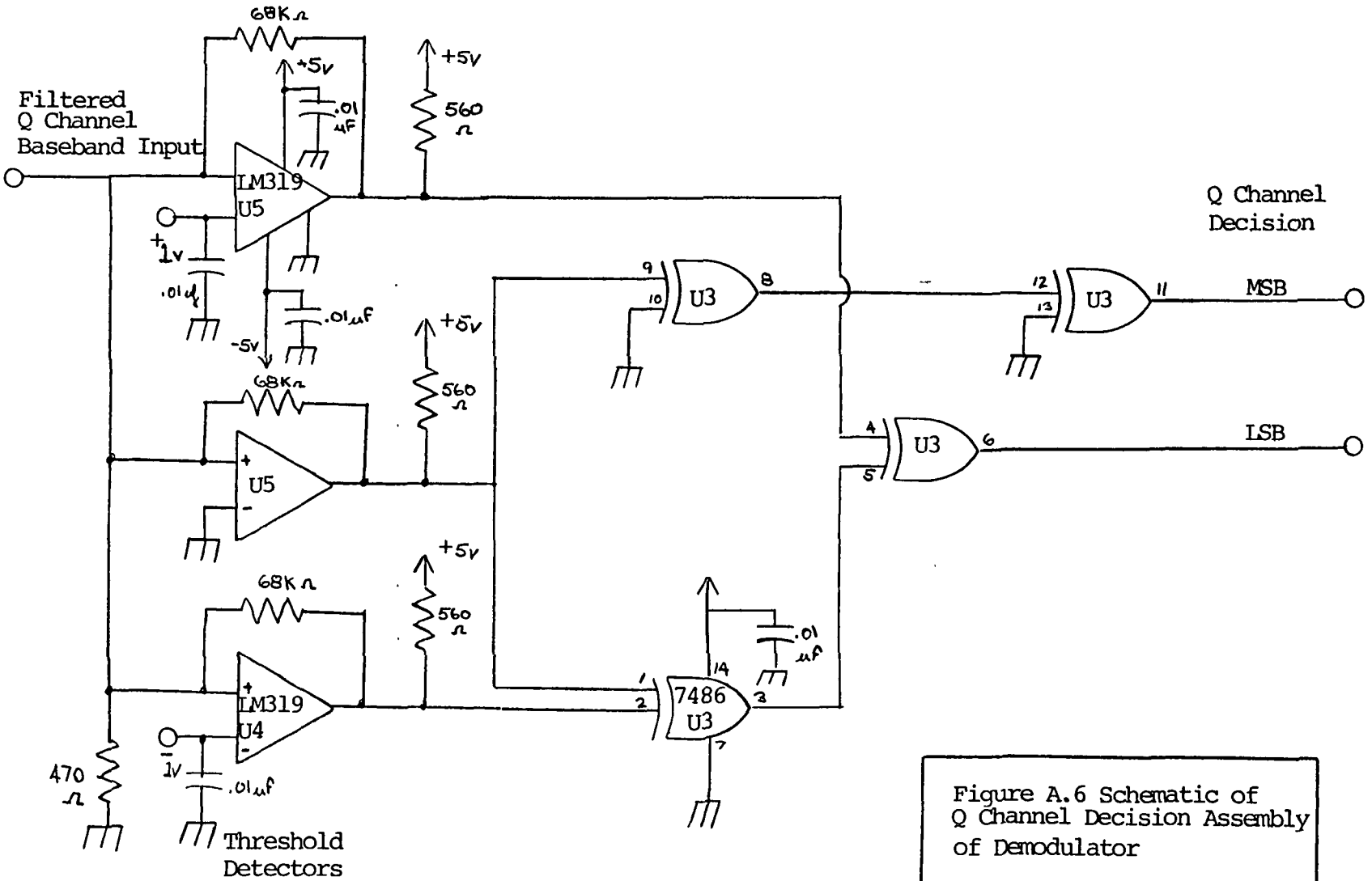


Figure A.6 Schematic of Q Channel Decision Assembly of Demodulator

Sheet 2 of 3

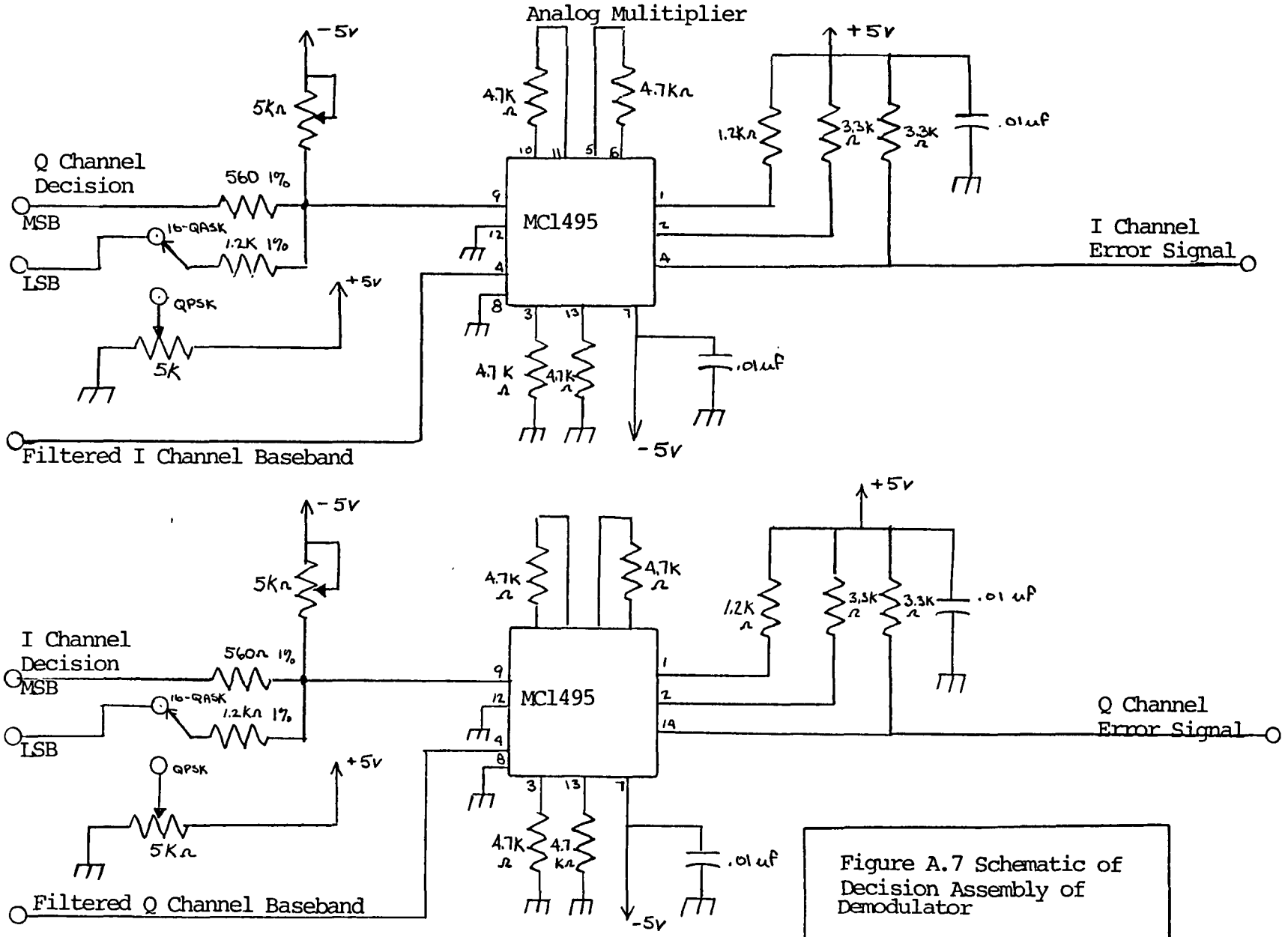


Figure A.7 Schematic of Decision Assembly of Demodulator

Sheet 3 of 3

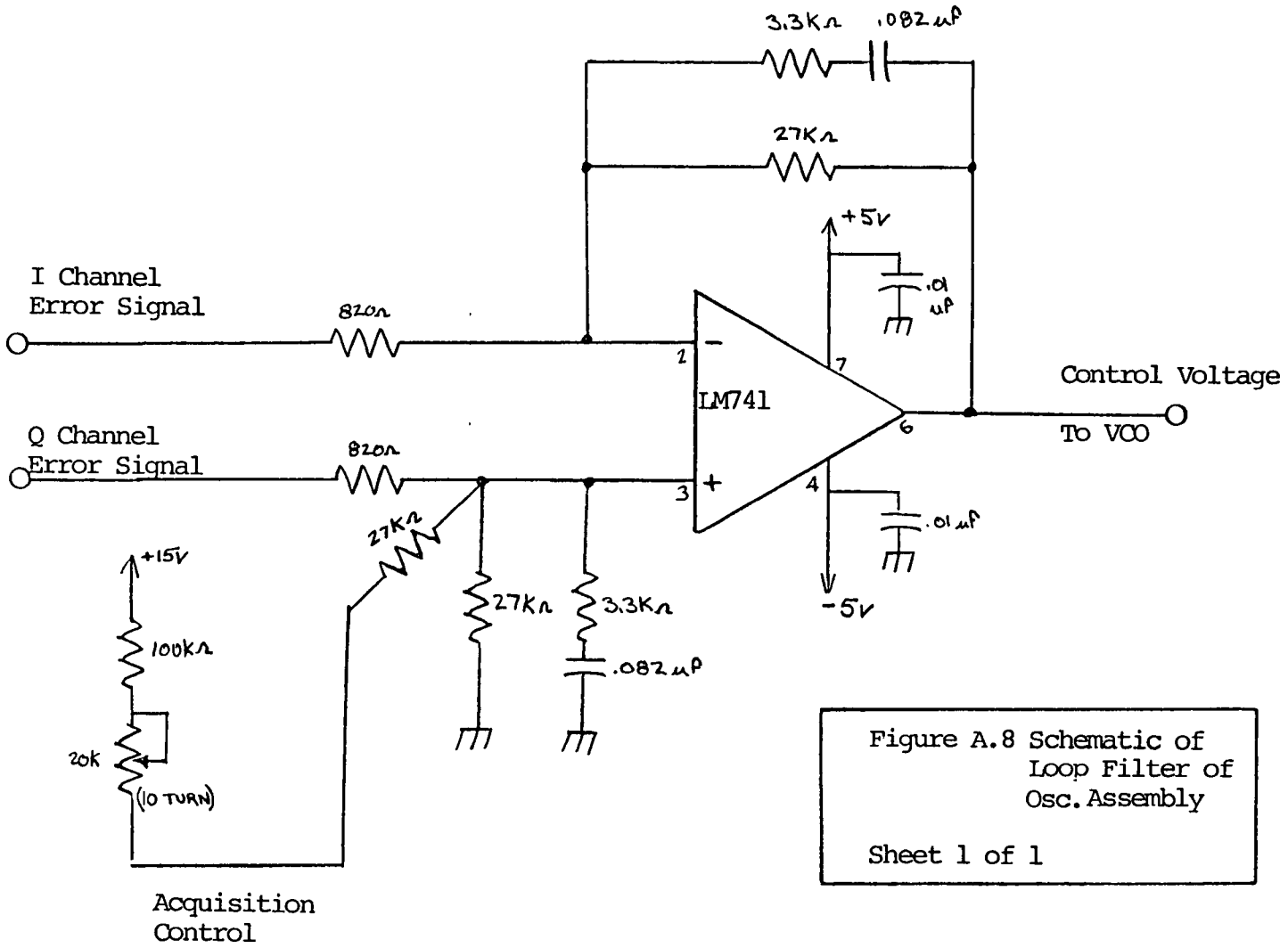


Figure A.8 Schematic of Loop Filter of Osc. Assembly

Sheet 1 of 1

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