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AN AUTOMATED STALL-SPEED WARNING SYSTEM

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Abstract

The NASA Dryden Flight Research Facility embarked upon a project with the United States Army Aviation Engineering Flight Activity (USAAEFA) to develop and test a stall-speed warning system. NASA designed and built an automated stall-speed warning system which presents both airspeed and stall speed to the pilot. The airspeed and stall speed are computed in real time by monitoring the basic aerodynamic parameters (dynamic pressure, horizontal and vertical accelerations, and pressure altitude) and other parameters (elevator and flap positions, engine torques, and fuel flow). In addition, an aural warning at predetermined stall margins is presented to the pilot through a voice synthesizer. Once the system was designed and installed in the aircraft, a flight-test program of less than 20 hr was anticipated to determine the stall-speed software coefficients. These coefficients would then be inserted in the system's software and then test flown over a period of about 10 hr for the purposes of evaluation.

Nomenclature

AICS = airborne instrumentation computer system

ASCII = American Standard Code for Information Interchange

Ax = longitudinal acceleration

Az = vertical acceleration

bit = binary digit

byte = eight binary bits

CLVCRT = critical effective coefficient of lift

DE = elevator position

DF = flap position

DFUELL = total fuel used, left engine

DFUELR = total fuel used, right engine

DG = landing gear strut compressed switch

EEPROM = electrically erasable PROM

EPROM = erasable programmable read only memory

EQL = left-engine torque

EQR = right-engine torque

Hp = pressure altitude, in. Hg

IC = integrated circuit

I/O = input/output

kbyte = 1024 bytes

LT = lift from the tail

NASA = National Aeronautics and Space Administration

OW = original gross weight of aircraft (including fuel), lb

PROM = programmable read-only memory

Q = dynamic pressure, in. Hg

RAM = random access memory

RS232C = Electronics Industry Association Standard number

ST = tail area, ft^2

SW = wing area, ft^2

TC = thrust coefficient

TSINA = total thrust, lb

TSINAT = vertical component of thrust, lb

TTL = transistor-transistor logic

USAAFFA = United States Army Aviation Engineering Flight Activity

USART = universal synchronous/asynchronous receiver transmitter

VIFPS = indicated airspeed, ft/sec

VSIKTS = indicated stall speed in knots

VTFPS = true airspeed, ft/sec

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Introduction

The United States Army Aviation Engineering Flight Activity (USAEEFA) had been aware that a stall-speed warning system was needed in the Army's OV-1C Mohawk aircraft (Fig.1). To this end, the Dryden Flight Research Facility was asked to develop an automated stall-speed warning system to be installed in the cockpit of the OV-1C. Visual indication of impending stall would be displayed to the pilot as a cursor or pointer located on a conventional airspeed indicator. Also, a voice synthesizer would provide an aural indication of stall at predetermined stall margins.

The design and development of the warning system was performed by the Measurement Section at Dryden. The installation of all aircraft sensors and their initial signal conditioning was performed by the United States Army Aviation Engineering Flight Activity (USAAEFA) at Edwards Air Force Base,

as was the initial design of the stall-speed algorithms and their associated coefficients. Also, the USAAEFA was made responsible for providing the aircraft, test crew, and the chase aircraft.

The flight-test configurations to be used in the evaluation of the warning system were designed to be flown in the Edwards AFB area. These tests were proposed by the Army in order to test the system under all feasible conditions. The Army flight-test engineer was responsible for that portion of the flight regime in which stall information was obtained for the coefficient derivations. This made it necessary to put the aircraft into stall conditions, collect the data from all sensors, and then analyze those data in order to calculate the stall coefficients for the software stored in the system.

After the coefficients were available for the software program that was to be stored in the system, the entire system was flight tested from a human engineering standpoint. This phase of the program was scheduled for about 20 flight hours, with the flight profiles chosen to verify the operations and suitability from the pilot's vantagepoint. These flights, as was the case for the previously mentioned flights, were also flown in the vicinity of Edwards Air Force Base.

General Description of Airspeed Equations

To acquire the necessary data for the project, the OV-1C was equipped with the following sensors:

Sensor	Parameter	Label	Units
S0	Longitudinal acceleration	Ax	g
S1	Vertical acceleration	Az	g
S2	Flap position	DF	deg
S3	Elevator position	DE	deg
S4	Landing gear strut compressed switch	DG	
S5	Pressure altitude	Hp	in. Hg
S6	Dynamic pressure	Q	in. Hg
S7	Total fuel used, right engine	DFUELR	gal
S8	Total fuel used, left engine	DFUELL	gal
S9	Left-engine torque sensor	EQL	$lb/in.^2$
S10	Right-engine torque sensor	EQR	$lb/in.^2$

From these sensors the following equations can be derived.

Indicated airspeed (VIFPS), ft/sec:

$$VIFPS = \left[\frac{2(70.7262)\ lb/ft^2/in.\ Hg\ Q}{\rho_o}\right]^{1/2}$$

where

Q = dynamic pressure from sensor S6, in. Hg

$\rho_o = 0.002378$ slug/ft^3 (air density at sea level)

True airspeed (VTFPS), ft/sec:

$$VTFPS = VIFPS\ (\rho_o/\rho)^{1/2}$$

where

$\rho_o = 0.002378$ slugs/ft^3

$\rho = 0.002378 - 6.84 \times 10^{-5} H + 6.4 \times 10^{-7} H^2$ slugs/ft^3

and

H = height in 1000 ft

VIFPS = indicated airspeed

Height (H), 1000 ft:

$$H = 145.442\left[1 - \left(\frac{Hp}{29.9213}\right)^{0.190262}\right]$$

where

Hp is pressure altitude from sensor S5, in. Hg

Total thrust (TSINA), lb:

$$TSINA = 744.0 + VTFPS\ (0.00642\ VTFPS - 0.0452\ EQTOT - 4.72) + H(1.219 + 0.004\ VTFPS - 0.7969\ EQTOT + 0.00122\ VTFPS \cdot EQTOT) + 32.666\ EQTOT$$

where

EQTOT = average engine torque sensor reading

= 0.5(EQL + EQR) derived from sensors S9 and S10.

Vertical component of thrust (TSINAT), lb:

$$TSINAT = (TSINA)\ \sin\ (ALPHA + C\phi)$$

where ALPHA is the stall angle of attack, deg. and $C\phi$ is the thrust angle 1.92°, at which the engines are mounted.

Thrust coefficient (TC):

$$TC = TSINAT/(SINAT \cdot Q \cdot SW)$$

where

$$SINAT = \sin\ (ALPHA + C\phi)$$

and

SW = wing area, 330 ft^2

Lift from the rail (LT), lb:

$$LT = -Q \cdot ST\ [0.78 - 0.91TC + 0.78(TC)^2 - 0.0147DF + 1.06 \times 10^{-4}\ (DF)^2 + 0.248DE]$$

where

$$ST = \text{tail area, } 85 \text{ ft}^2$$

Critical effective coefficient of lift (CLVCRT):

The value of CLVCRT is a function of flap angle and engine thrust. The parameter is shown as a polynomial with the coefficients to be derived from the first flight-test phase.

For flap angles less than 47° but greater than or equal to 17°:

$$CLVCRT = C_{L45A}\ EQTOT^2 + C_{L45B}\ EQTOT + C_{L45C}$$

For flap angles less than 17° but greater than or equal to 2°:

$$CLVCRT = C_{L15A}\ EQTOT^2 + C_{L15B}\ EQTOT + C_{L15C}$$

For flap angles less than 2°:

$$CLVCRT = C_{L\phi A}\ EQTOT^2 + C_{L\phi B}\ EQTOT + C_{L\phi C}$$

Indicated stall speed (VSIKTS), knots:

$$VSIKTS = 0.5925 \frac{\text{knots}}{(\text{ft/sec})} \left[\frac{\left(2\{W[\sin(ALPHA)(Ax) + \cos(ALPHA)(Az)] - LT - TSINAT\} \right)}{\rho_o \cdot SW \cdot CLVCRT} \right]^{1/2}$$

where Ax and Az are the horizontal and vertical accelerations derived from sensors S0 and S1,

and

W = current weight of aircraft

W = OW-DFUELL - DFUELR

Overall Description of Hardware Items

The automated stall-speed warning system is enclosed in two main electronics boxes (see Fig. 2), one of which houses the signal conditioning, processing, and input/output circuitry (including the drive circuitry for the indicator), and the aural warning circuitry. The other box houses the electronics used to drive the cockpit indicator. Not included in these two boxes, but nonetheless an integral part of the warning system, are the cockpit-mounted airspeed/stall-speed indicator and the portable visual display unit.

The box that houses most of the electronics is called the airborne instrumentation computer system, or AICS for short (Figs. 3 and 4). This AICS box is a culmination of Dryden's effort to standardize much of the system's design for ongoing and future flight-test needs. The AICS provides a standard-size box with a single-board microcomputer and standard back-plane that will accommodate commercially available or special-purpose, in-house-designed custom boards. The box itself can be configured to fit the needs of the individual projects fairly readily through the use of the standard, flexible bus. The bus used in the AICS bus is the widely used STD bus developed by Pro-Log Corporation of Monterey, California.[1]

The AICS box contains six slots. As developed and configured for this project, five slots contain a mixture of commercially available and in-house designed boards. The complement of boards used in the AICS box is:

1) Single-board processor

2) Nonvolatile memory (EEPROM) board

3) Parallel interface board

4) Analog-to-digital converter board

5) Voice synthesizer and audio power amplifier board

The single-board processor board and the voice synthesizer amplifier board were design and built at Dryden; the remaining three boards were bought commercially. The commercial boards were modified slightly, where necessary, to make them more environmentally hardened. Future plans include a redesign of these commercial boards to make them fully flight-qualified. A detailed description and analysis of each of these five boards will be presented in the following sections.

The box housing the drive circuitry for the cockpit-mounted indicator is shown in Figs. 2 and 5. This circuitry includes two separate digital-to-synchro converters with high-power transistor amplifiers. Each digital-to synchro board is capable of driving any standard load (CT or CDX passive loads, and torque receivers) of up to 3 A peak.

The indicator for visually displaying airspeed and stall speed is a modified, dual-needle radio magnetic indicator (RMI). NASA installed the same airspeed indicator dial face as is used in the OV-1C aircraft. However, along with the conventional airspeed pointer, there is mounted another pointer with a red triangle to indicate the calculated stall speed (see Figs. 2 and 6).

The portable visual display unit was purchased commercially. The capabilities of this unit are presented in the following sections. This unit interfaces to the microcomputer board through serial ASCII RS232C port. It is used to input data and commands to the AICS box, as well as displaying calculated values and raw data values. Figures 7 and 8 show two sample displays for the project.

Detailed Analysis of the Various Hardware Subsets

Each major subsystem of the automated stallspeed warning system is presented with special emphasis on circuit analysis.

Single-Board Microcomputer

The salient features of the single-broad microcomputer are as follows:

1) Utilizes an 8085A microprocessor

2) 8231A floating-point processor

3) 22 bits of parallel I/O

4) Two USARTs that are fully programmable with RS232C or TTL level signals

5) 10.25 kbytes on-board memory configured as 10 kbytes EPROM and 256 bytes RAM or 8 kbytes EPROM and 2.25 kbytes/RAM

6) Three 16-bit programmable timers

7) Address decoding utilizing PROMs

8) STD bus interface

The single-board microcomputer (Fig. 9) is a fully flight-qualified board built up on a sixlayer printed circuit board. The printed circuit board was designed so that the STD bus signals are presented at one edge of the board while the special purpose input/output signals are presented on the opposite edge. This is a standard approach allowing a more optimum segregation of the two types of signals.[1] The board contains 24 integrated circuits, as well as an assortment of miscellaneous support circuitry.

From the block diagram of the single-board microcomputer (Fig. 10), the following points can be ascertained. The 8085A microprocessor has its lower 8 bits of address/data lines (AD0-AD7), as well as its control lines (Read, Write, clock, IO/$\overline{M}$, Address Latch Enable, and Reset) inputted to an 8155 integrated circuit. The 8155 provides two 8-bit and one 6-bit parallel input/output ports (used to interface the 8085A to the digital to synchro converters), 256 bytes of static RAM, and a 14-bit programmable timer for the board. Two 2732 EPROM integrated circuits provide the board with 8 kbytes of program memory, with the remaining 2 kbytes of RAM memory being provided by an HM6116LP-2 chip.

Two USARTs are provided by two 8251 chips with their programmable baud-rate generators being supplied by two of the three 16-bit timers of an 8253 circuit. The combination of the 8251s and the 8253 circuits gives two synchronous or asynchronous ports with adjustable baud-rates from 0-19,200 baud for asynchronous modes, and from 0-64,000 baud for synchronous modes. A 75189 integrated circuit provides the input interface to the 8251s from the RS-232C terminal devices, and a 75188 IC handles the output interface from the 8251s to the RS-232C terminal devices.

All on-board address decoding is provided by three 82S131 PROMs (512 × 4 each). The use of PROM address decoders for all the I/O port address selection results in a significant reduction in chip count and circuit complexity over the more conventional discrete logic with switch-selectable addresses. The penalty, however, is that the address decoding can only be altered by programming a new PROM, and is slower than the discrete logic form.

Probably the most important factor in making this board universally applicable to many real-time instrumentation systems, is the use of the 8231A floating-point processor. The 8231A integrated circuit is a powerful arithmetic calculator that will perform single- and double-precision fixed-point, as well as floating-point, arithmetic and floating-point trigonometric operations. It is not the intent of this paper to repeat material contained in the manufacturer's publication[2] about this IC; however, a few of the more important features are presented below.

The 8231A is interfaced to the 8085A through the lower 8 bits of the address/data bus (AD7-AD0), as well as the control lines for Read and Write, clock, chip select (from the 82S131 PROMs), and the least significant address line, A0. This address line, in conjunction with Read and Write signals tells the 8231A what types of operations (e.g., whether to enter data onto its stack, or whether the data bus is to be interpreted as a command from the 8085A, etc.) it will be doing. The 8085A passes data and commands (what arithmetic operations to do) to the 8231A via the 8-bit data bus, and internally places the data into a stack that is oriented as 8 by 16 bits (or 4 by 32 bits). This stack size allows the 8085A to put eight single-precision, fixed-point operands in it or four double-precision or floating-point operands in the stack. The 8231A stores a single-precision fixed-point value in a 16-bit word with the most significant bit as the sign bit; a double-precision fixed-point value is stored as a 32-bit word with the MSB being the sign. The floating-point format utilizes a 32-bit word with the least significant 24-bits being the mantissa and the most significant 8 bits representing the exponent. Thus the range of values represented in this way is $\pm(2.7 \times 10^{-20}$ to $9.2 \times 10^{18})$.

EEPROM Board

The EEPROM board is needed on this project to allow storage of coefficients and data from the sensors during the flight-test phase of the project; however, it was necessary to save these data, even when the aircraft's power was turned off. After the flight, the data would be analyzed by the project engineer at the laboratory. The EEPROM board is a commercially available board that uses Intel 2816 nonvolatile EEPROM ICs. The board, when fully populated with eight 2816 chips will allow for 16 kbytes of memory; however, in the stall-speed warning project only 2 kbytes are being used.

The EEPROM board is essentially treated by the 8085A micoprocessor as an off-board pseudo-RAM memory interfaced through the STD bus. The reason it is viewed as pseudo-RAM is because the Write operation to the board is longer than that for normal RAM; hence, Wait states are required by the 8085A (this requires that the 8085A do nothing during this Wait period). Also, because of the nature of the Write electronics on the EEPROM board, a Read operation immediately after a Write operation is not advised since the Write electronics take several microseconds to settle.

Parallel Interface Board

The parallel interface board is also a commercially available board. The board selected for this project uses two 8255 ICs to provide 48 programmable I/O lines. The board interfaces to the single-board processor via the STD bus, and interfaces to the external world via a locking edge connector on the opposite end of the board. This connector interfaces the two engine fuel-used totalizers to the board.

Analog-to-Digital Board

The analog-to-digital board is also a commercially available board (see Fig. 11). It utilizes a precision instrumentation amplifier giving programmable gains of from 1 to 1,000. The output of the amplifier is then converted to a 12-bit

digital word (in offset binary, two's complement, or straight binary format) at a maximum rate of 25,000 channels/sec. The board is capable of accepting either 16 single-ended inputs or 8 differential inputs. With the addition of two more multiplexer ICs, the board capacity can be doubled for both cases. This project required 9 inputs and thus the board was configured with 16 inputs.

The board interfaced to the single-board processor via the STD bus, and interfaced to the analog-sensor signals through a locking edge connector on the opposite end of the board. The board is memory-mapped I/O with selectable base-page address on the board itself. The board uses three consecutive bytes in the memory-mapped space as follows: the first 8-byte is written into by the 8085A microprocessor specifying the channel number to be read; the next byte is used by the board to store the least significant 8 bits of the 12-bit converted word; the last byte is used for the most significant 4 bits of the converted word, as well as a "Busy" bit to signify to the processor that a conversion is not yet done.

Voice Synthesizer/Audio Amplifier Board

This board is an in-house design interfacing the processor board to a voice synthesizer and audio power amplifier via the STD bus. The board utilizes a Votrax SC-01 phoneme speech synthesizer which has a repertoire of 64 different phonemes (addressable through a 6-bit data word) and 2 bits governing the pitch of the phoneme. Additional pitch control is obtained by using a 5497 binary-rate multiplier. An 8755 (2 kbytes of EPROM and 16 input/output lines) is also on this board. The analog synthesized "words" are then amplified with an adjustable-gain power amplifier capable of driving approximately 0.5 W into an 8-ohm speaker, or driving a higher impedance audio intercom system (the OV-1C intercom system utilizes a Collins C-1611D which appears as an approximately 150-ohm load).

When the processor has determined that the indicated airspeed, VIKTS, is within a predetermined percentage of the stall speed, the processor outputs an aural warning to the pilot through this board. The predetermined airspeed is set by the Army project engineer as the greater of 107.5% of indicated stall speed or 7.5 knots plus the indicated stall speed. These two values can be increased or decreased in real time through the terminal. Once amplified, this synthesized message is fed into the pilot's headset alerting him to observe his airspeed. Also, an algorithm is used to increase the frequency at which this aural message is sent. This frequency is based on the difference between the VIKTS and VSIKTS values, but will not increase to more than 0.9 times a second.

Digital-to-Synchro Modules

Two separate calculated values, one for the indicated airspeed and the other indicated stall speed, are stored as 12-bit digital values. These two values are outputted to the digital-to-synchro box via the parallel port located on the single-board computer. Both values are outputted on the same 12-bit digital bus; however, the separate trigger signals to each separate synchro board loads the proper board with the proper value at the right time. This reduces the number of lines interfacing the two digital-to-synchro boards to the processor board from 27 to 15.

The digital-to-synchro converters latch the 12-bit digital values into a register with the advent of the trigger pulse. Next, the converter transforms the 12-bit signal into the sin and cosine signals of the resolver format. The resolver format signals are then converted into the conventional synchro signals S1, S2, and S3 through the use of an electronic Scott-T filter. These synchro signals are then amplified by highpower linear amplifiers to provide the 3-A peak drive capability needed for some torque receivers (see Fig. 12). The synchro receivers in the airspeed/stall-speed indicator do not need all of this drive capability; however, at the time of box design the synchro types had not been determined.

Portable Visual Display Unit

The portable display unit chosen for this project (Figs. 7 and 8) has the ability to input and output information through a serial RS-232C port located on the single-board processor board. The unit has selectable baud rates to 19,200 baud, a display of 40 characters (set up as two rows of 20 characters per row), and a buffer memory (non-volatile) of 384 lines at 20 characters per line (7.5 kbytes of memory).

Software was written for the system to allow the project engineer or the flight-test engineer to load "snapshots" of raw data or processed data into the visual display unit's buffer memory. A sample of the typical display is shown in Figs. 7 and 8. Although the unit is primarily used as a display unit, it functions as an input device to the processor, thus allowing the operator to change coefficients in the stall-warning software that may be stored in either RAM or EEPROM.

Analysis of System Software

The stall-warning system software is made up of five major sections:

1) Initialization routine

2) Input data formatting

3) Data collection

4) Data processing and velocity calculations

5) Cockpit indicator drive and aural output

In this section these major software sections are discussed as they pertain to the overall task.

The scenario for the first phase of the flight testing is to collect data at predetermined flight conditions. These data would be time-tagged with an event marker that the flight-test engineer would actuate when the flight conditions were right. At each time-tagged event, all parameters are loaded into the EEPROM circuits. This data group consists of approximately sixteen 16-bit words. A maximum of 60 separate snapshots would be obtained during the flight, thereby requiring about 2 kbytes of nonvolatile memory storage. When the flight was over, the raw data would be outputted to a printer

and analyzed on a larger computing system. The outcome of this exercise was the determination of the coefficients discussed in the section entitled General Description of Airspeed Equations. These coefficients would then be loaded back into the AICS box via the visual display unit and a new flight would be flown to check the validity of the stallspeed calculations.

During this phase of the fight testing, the visual display unit is also displaying the various parameters (see Figs. 7 and 8) to the flight-test engineer. Indicated velocity, as well as indicated stall velocity, is shown at this time; however, the validity of the stall speed is only as good as the coefficients used up to that point.

Data collection is done in about 10 to 54 msec for the entire set of parameters. This ensures that each parameter is updated at a rate of approximately 20 times per second. Approximately 44 msec of the 54 msec period is necessary for outputting to the display. The visual display is updated once every 0.5 sec, while the cockpit indicator is updated each sample. The routine takes ≈10 msec to update the sensor calibrations and the synchros. Every 0.5 sec, an additional 44 msec is needed to update the visual display.

From the flowchart in Fig. 13, the portion on the left-hand side is primarily involved with obtaining data, calculating VSIKTS and VIKTS, and displaying them, while the part on the right-hand side is dealing with the entering of the constants and the selecting of options. If no event key is selected, then the system constantly is collecting data at 10-54 msec intervals, calculating the velocities, checking to see if illegal sensor readings or an illegal velocity calculation is attempted (e.g., a negative radical), displaying these values on the indicator, as well as the visual display unit, and outputing the aural warning if necessary. If an event switch is actuated, the values of the parameters are stored in EEPROM, and then the address pointer for the current EEPROM position is updated for the next set of data.

If a key-stroke is detected from the visual display unit, the airspeed and stall-speed pointers are driven to 0, and the processor enters a routine to decode the key-stroke entry and perform that function. If an "S" is detected, the processor expects the velocity stall-margin factor to be inputted from the visual display unit. If a "W" is detected, the processor expects the original operating weight (OW) of the aircraft to be entered. A "1" sets the display up for the first page format for displaying to the flight test engineer. A "2" sets up the second page format for display. A "C" followed by two successive "#" entries displays the constants. A "P" takes the contents of the EEPROMs and outputs it to a printer. A "U" configures the display pages for uncalibrated sensor counts display. An "X" configures the display pages for calibrated parameter display. An "↑" initializes the EEPROM format. An "I" enables the aural warning output while an "L" disables this output. An "*" sets the pilot indicator to the stall margin indicator mode, while a "/" sets the indicator to the normal airspeed, stall speed mode.

The program will always revert back to the section on taking data and processing it until either a key-stroke from the visual display unit is detected or until an error in calculating occurs. These two instances will cause the processor to either decode the key-stroke and perform the task indicated by the key-stroke, or to sound an aural warning and drive the airspeed and stall speed indicator to 0, and display error information on the visual display unit. In either case, the program reverts back to normal data acquisition mode once the key stroke sequence is completed or the error condition is corrected.

Conclusions

The automated stall-speed warning system proved to be an interesting and challenging project, one in which design and development effort encompassed several aspects of flight-test, date acquisition and display technology.

The system was first set up to be a data-acquisition and data-storage system. Approximately 16 parameters and labels were collected (up to 60 snapshots could be stored in nonvolatile memory) at a rate greater than 20 "snapshots" per second. The analog signals were conditioned and converted to a digital value; then both discrete parameters, as well as the converted analog parameters, were stored in EEPROM. The stored data could then be retrieved after the flight analyzed in the laboratory through the use of the visual display unit and an attached printer.

After the data had been collected, engineering units conversion, sensor calibration (through the use of polynomial expansions), and data display were accomplished in real-time. This necessitated the need for real-time data processing through the use of a floating-point processor in conjunction with the 8085A microprocessor. Also, display technology was investigated to provide a user-operated input/output portable display.

With the calculation of the airspeed and stall-speed, a method was developed to display this information to the cockpit in a traditional format — a standard airspeed indicator was designed to enable a bug to display the current indicated stall speed. To this end, digital-to-synchro technology was explored to make it possible to use existing cockpit instrumentation. Also, an aural output to alert the pilot to the possible impending stall condition was also utilized. Human voice synthesis was accomplished through the interface of the microprocessor with the voice synthesizer board.

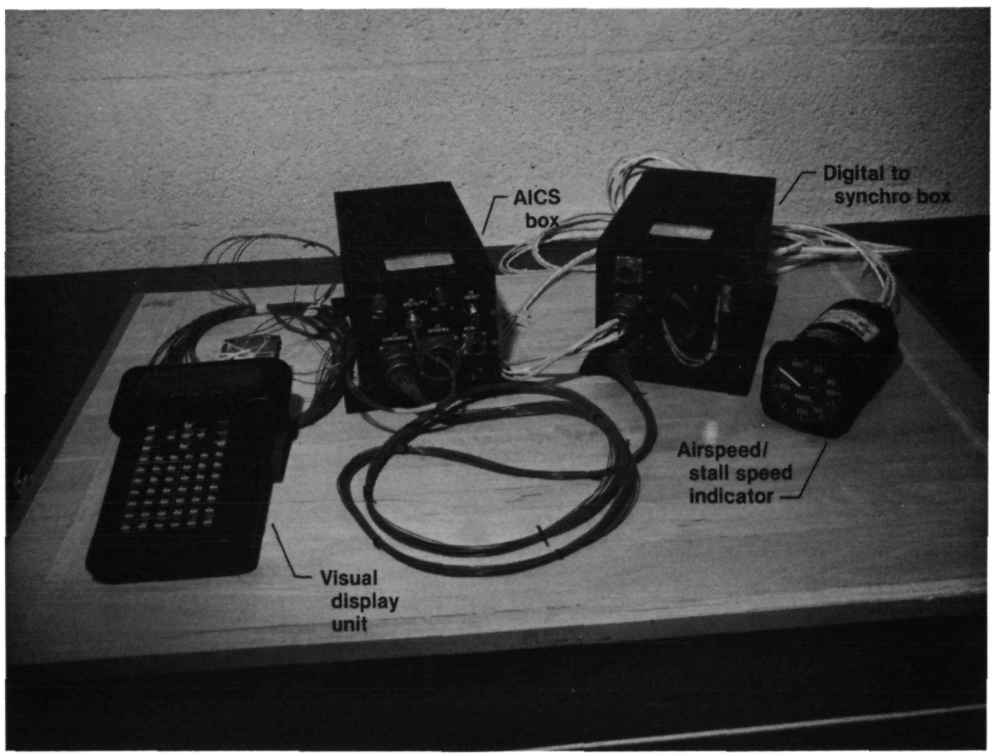
References

[1]"STD Bus Technical Manual and Product Catalog," Pro-Log Corporation, Monterey, Calif., Aug. 1982, pp. 1-1 to 2-5.

[2]"Microprocessor and Peripherals Handbook," Intel Corporation, Santa Clara, Calif., 1983, pp. 6-100 to 6-109.

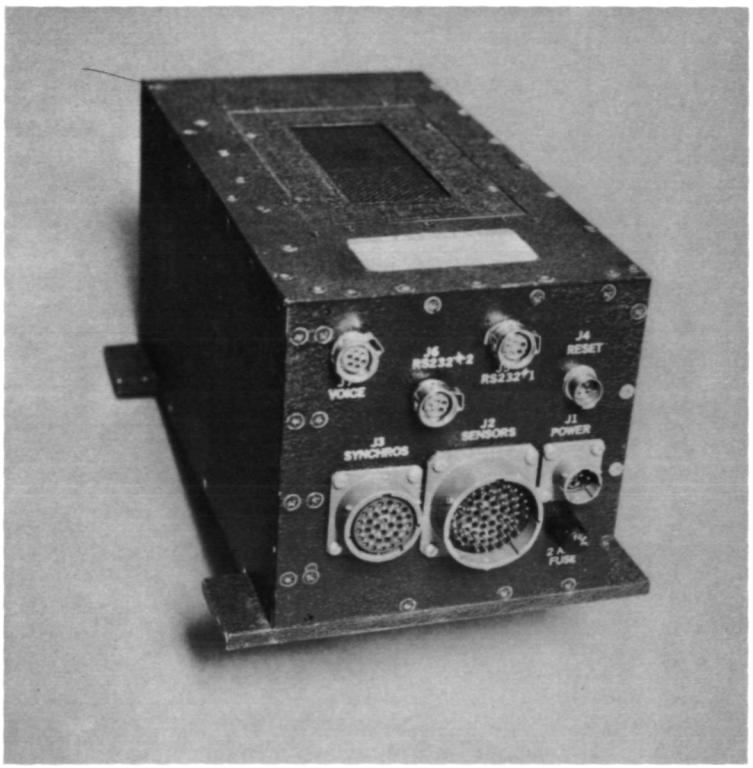
ECN 24931A

Fig. 1 OV-1C aircraft.



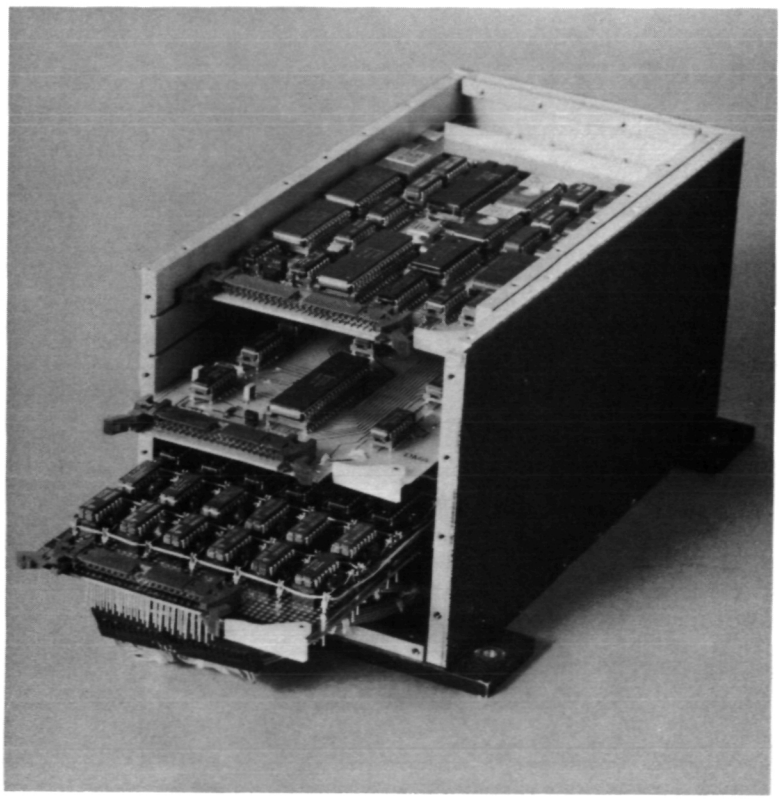
DFRF83-1437

Fig. 2 Stall-speed warning system.



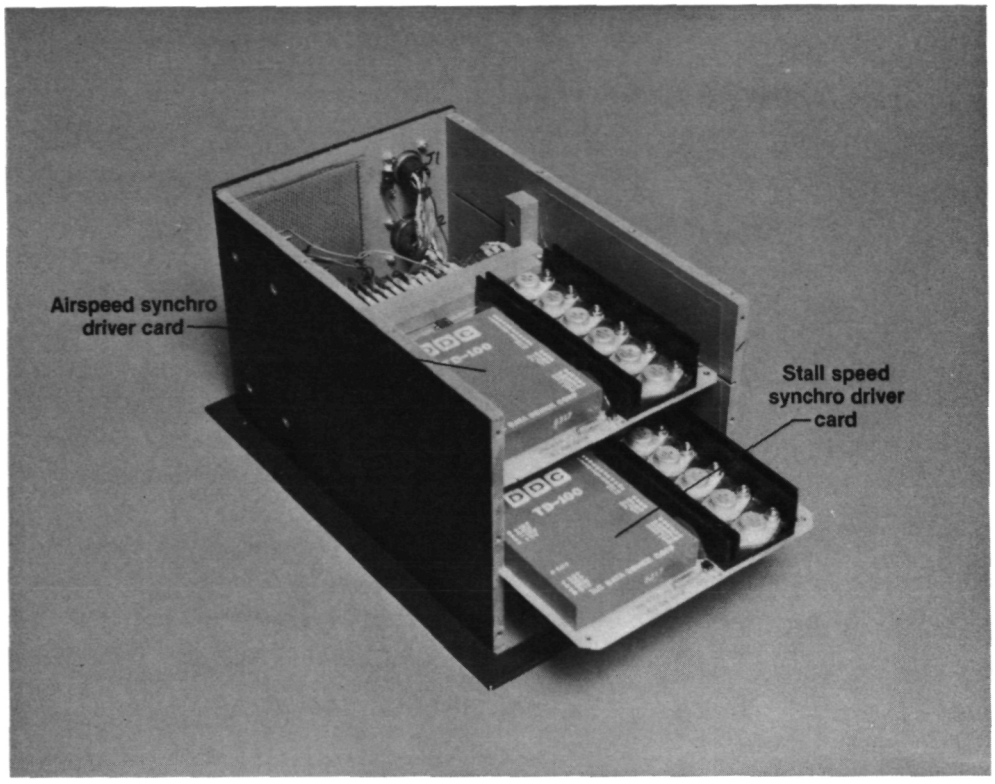
ECN 24940A

Fig. 3 AICS box (front view).



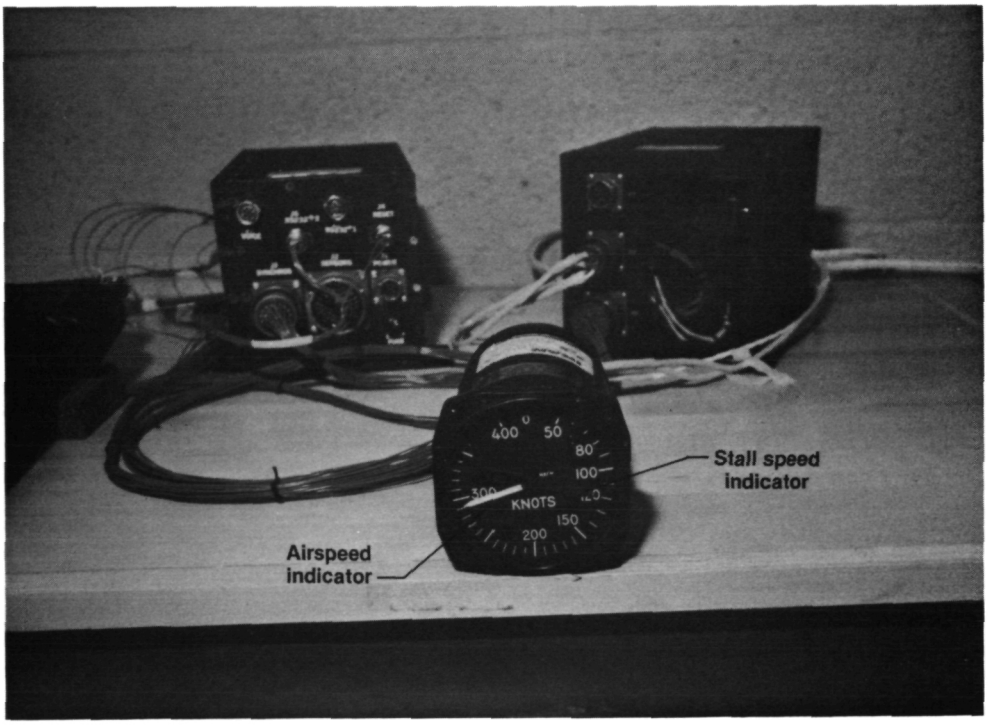
ECN 22636

Fig. 4 AICS box (internal view).



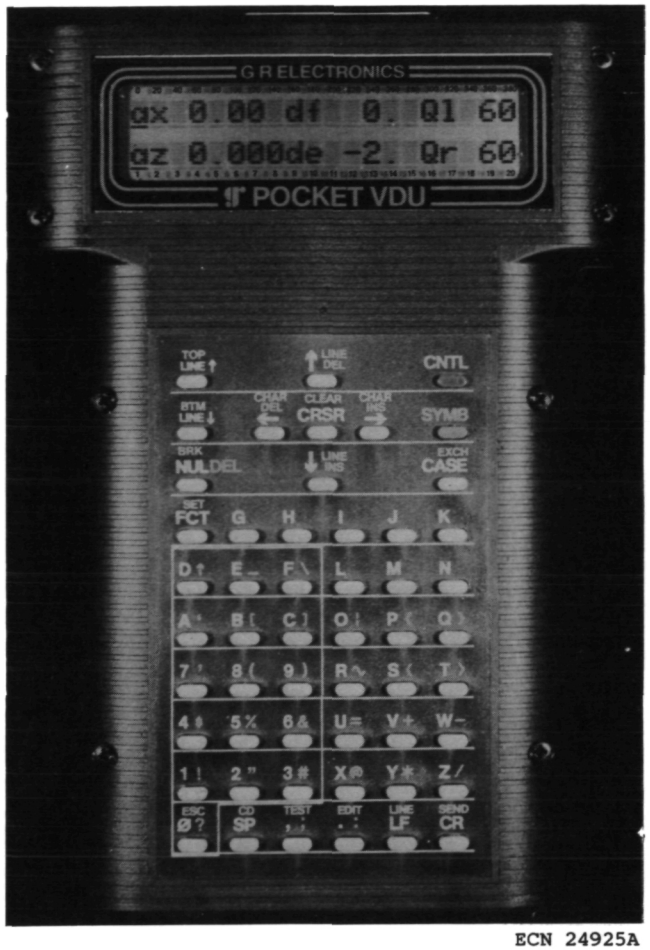
DFRF83-1430

Fig. 5 Digital-to-synchro box.



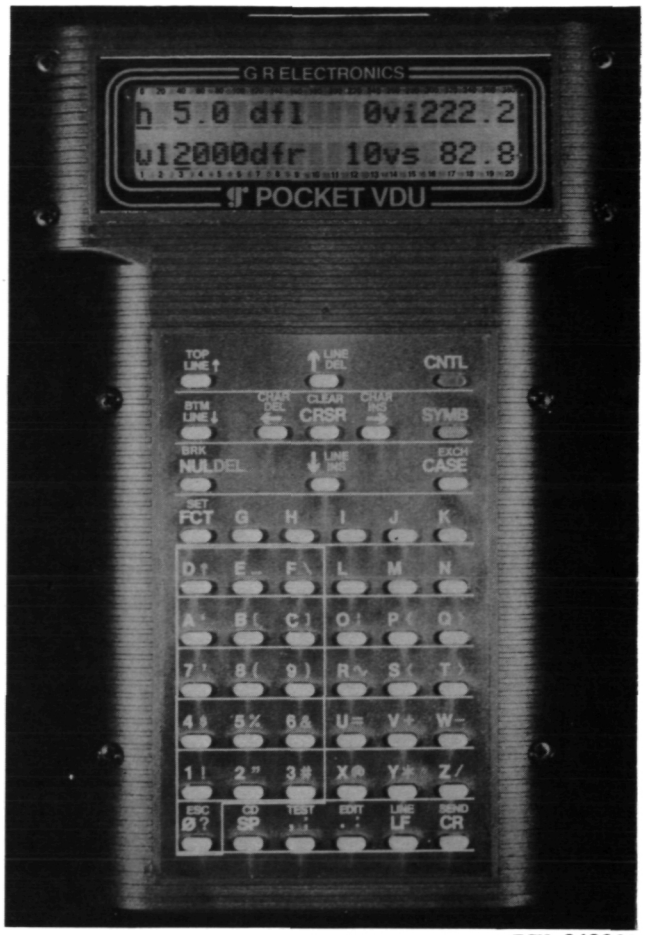
DFRF83-1436

Fig. 6 Cockpit-mounted indicator.



ECN 24925A

Fig. 7 Visual display unit (page 1 format).



ECN 24926A

Fig. 8 Visual display unit (page 2 format).

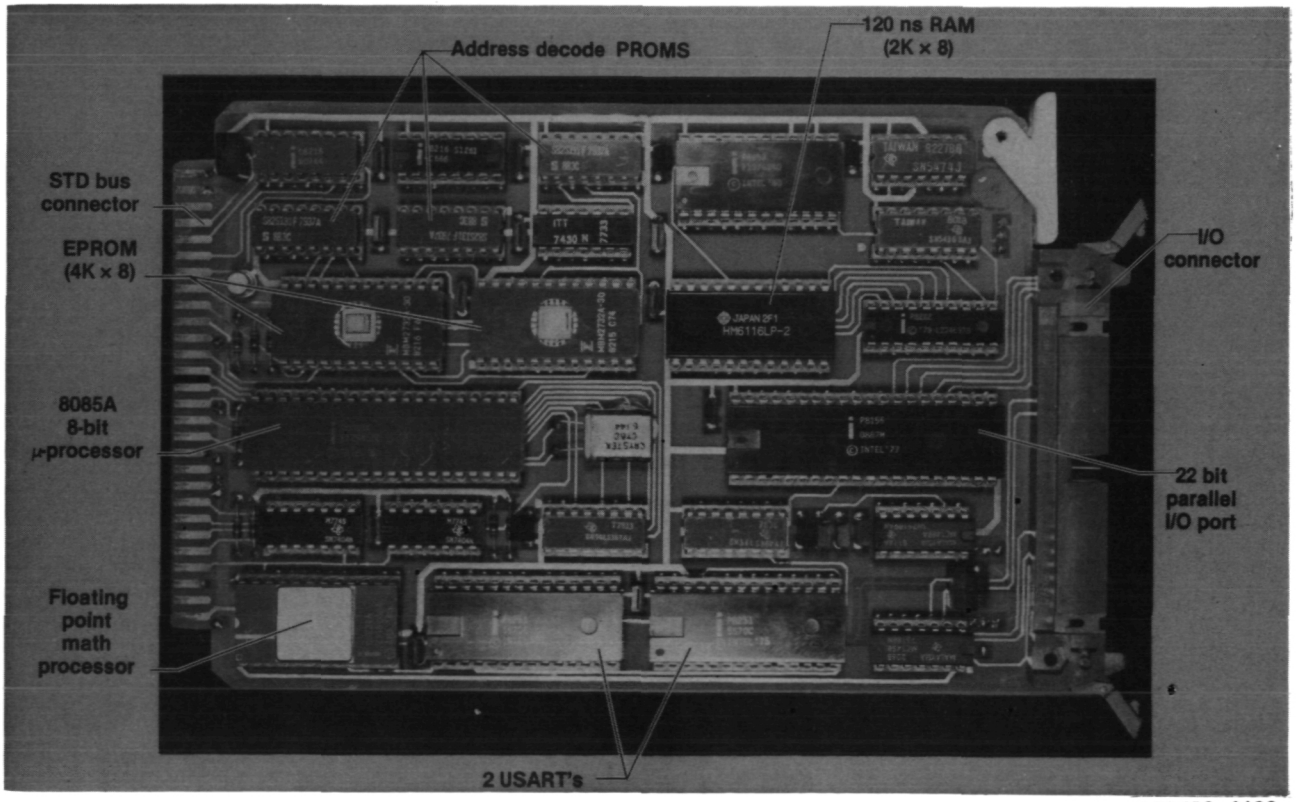


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Fig. 9 Single-board microcomputer.

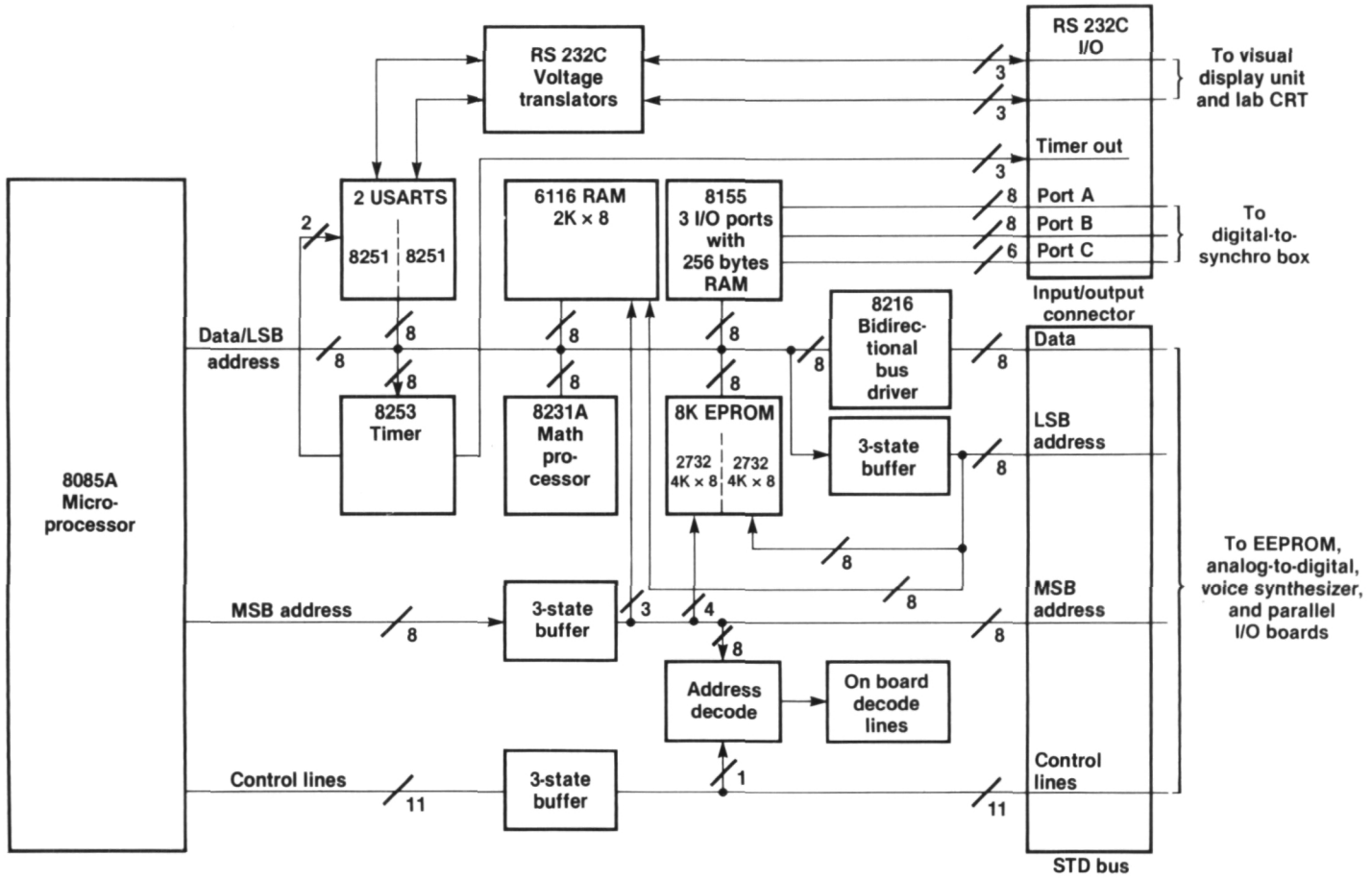

Fig. 10 Block diagram of single-board microcomputer.

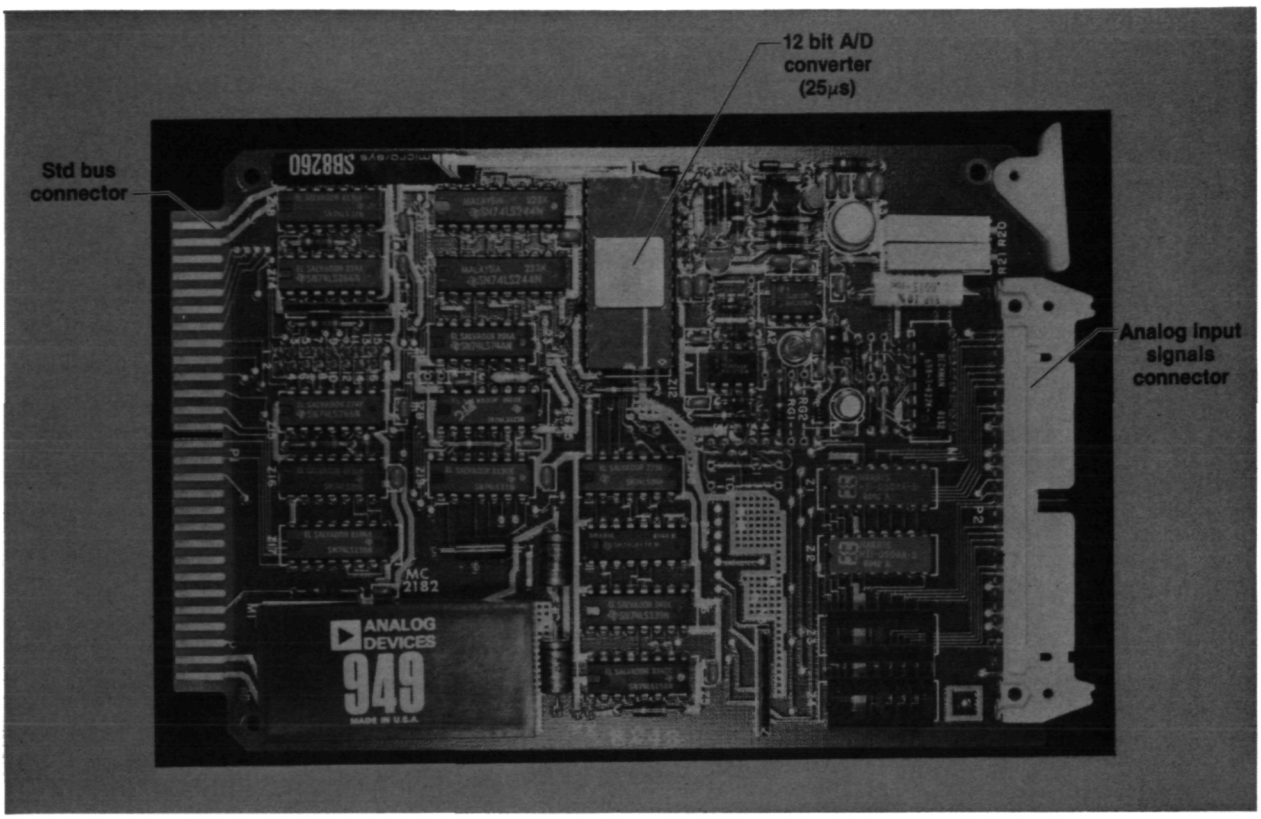

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Fig. 11 Analog-to-digital board.

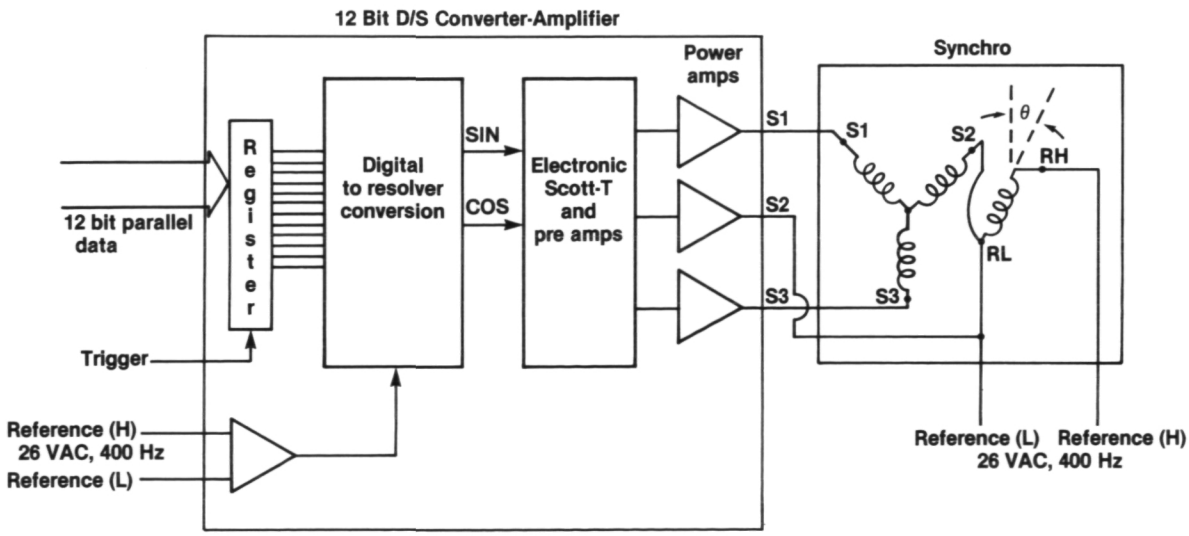

Fig. 12 Typical digital-to-synchro driver.

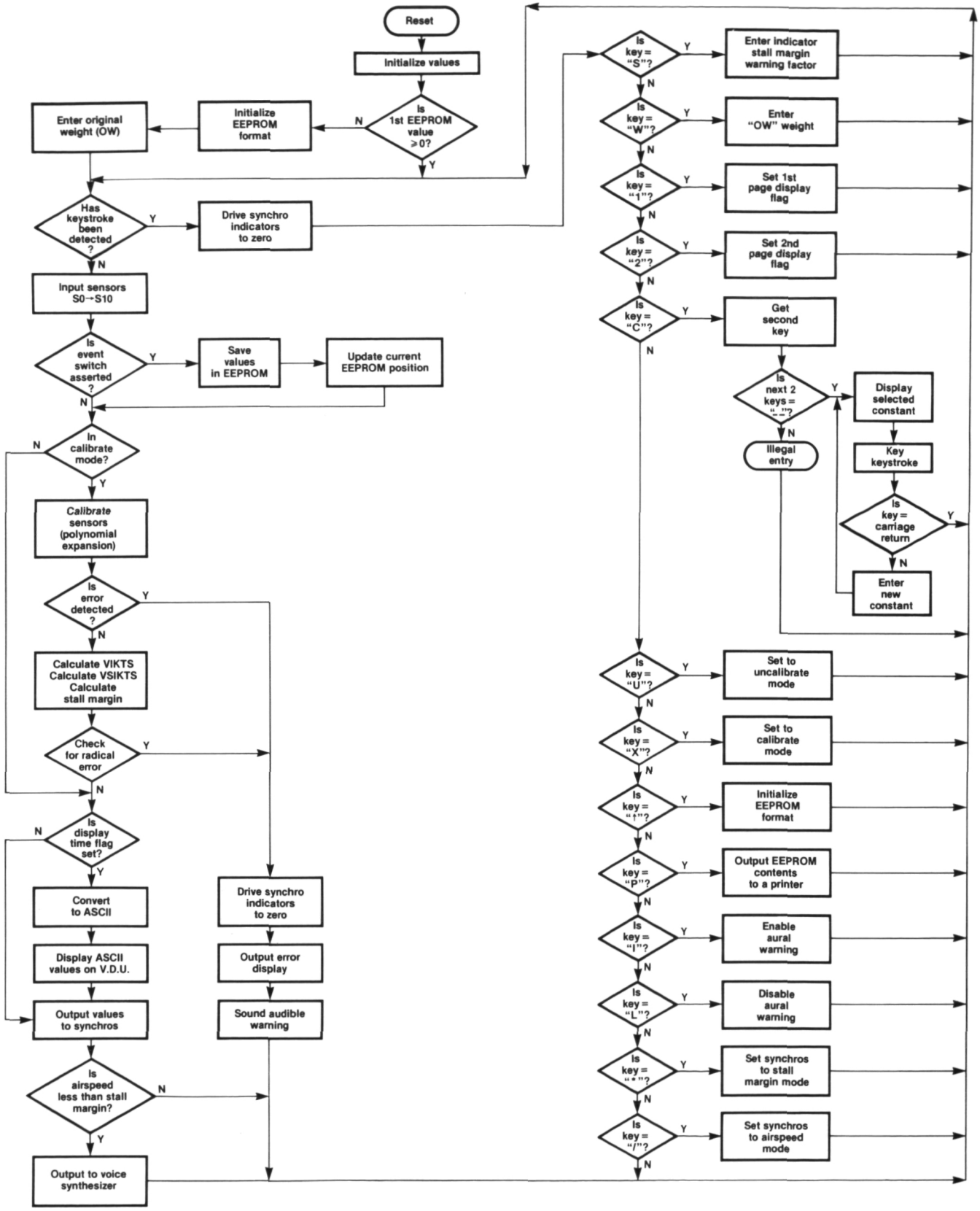

Fig. 13 Software operations flowchart.

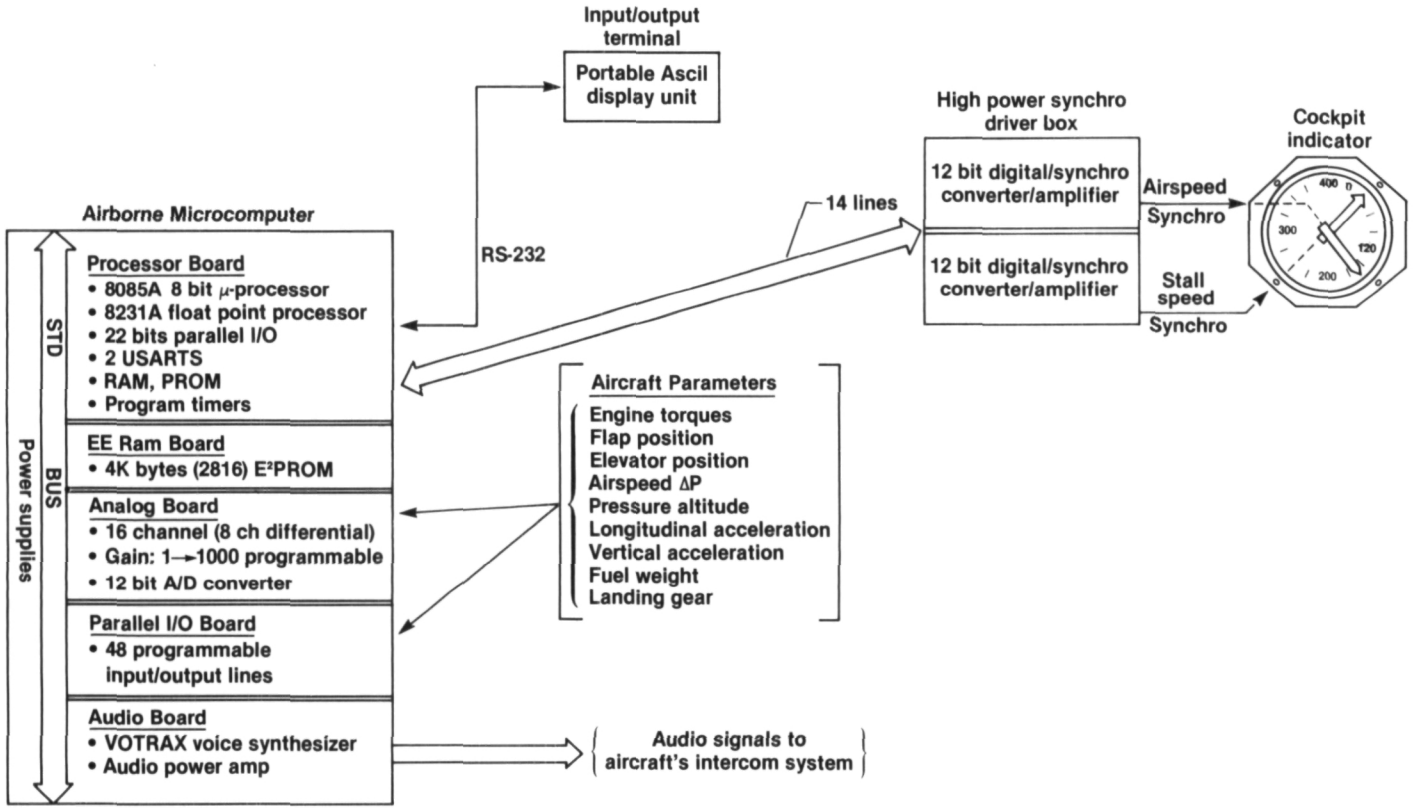

Fig. 14 Overall block diagram of stall-warning system.

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15. Supplementary Notes

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16. Abstract

The NASA Ames Research Center's Dryden Flight Research Facility embarked upon a project with the United States Army Aviation Engineering Flight Activity (USAAEFA) to develop and test a stall-speed warning system. NASA designed and built an automated stall-speed warning system which presents both airspeed and stall speed to the pilot. The airspeed and stall speed are computed in real time by monitoring the basic aerodynamic parameters (dynamic pressure, horizontal and vertical accelerations, and pressure altitude) and other parameters (elevator and flap positions, engine torques, and fuel flow). In addition, an aural warning at predetermined stall margins is presented to the pilot through a voice synthesizer. Once the system was designed and installed in the aircraft, a flight-test program of less than 20 hr was anticipated to determine the stall-speed software coefficients. These coefficients would then be inserted in the system's software and then test flown over a period of about 10 hr for the purposes of evaluation.

17. Key Words (Suggested by Author(s))	18. Distribution Statement
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