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The Effect of Diffusion Induced Lattice Stress on the Open-Circuit Voltage in Silicon Solar Cells

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THE EFFECT OF DIFFUSION INDUCED LATTICE STRESS ON THE OPEN-CIRCUIT VOLTAGE IN SILICON SOLAR CELLS

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SUMMARY

It is demonstrated that diffusion induced stresses in low resistivity silicon solar cells can significantly reduce both the open-circuit voltage and the collection efficiency. The degradation mechanism involves stress induced changes in both the minority carrier mobility and the diffusion length. Thermal recovery characteristics indicate that the stresses are relieved at higher temperatures by divacancy flow (silicon self diffusion). The level of residual stress in as-fabricated cells was found to be negligible in the cells tested.

INTRODUCTION

When a piezoresistive material such as silicon is mechanically stressed, its resistance changes. Mechanical stress applied to a silicon PN junction has been shown to have a drastic effect on the device saturation current through changes effected in the minority carrier mobility and the band gap (ref. 1). Diffusion of phosphorus into the silicon lattice during solar cell fabrication has been shown to produce stress levels in the silicon that exceed its yield point (ref. 2). While it is reasonable to expect that diffusion induced stresses should have an effect on cell output, there is no evidence in the literature showing this to be the case. The purpose of this paper is to: (1) Demonstrate that diffusion induced stresses can indeed affect device performance, and (2) Determine the degree of residual stress in finished low resistivity cells where evidence has been reported suggesting that stress induced mobility changes may suppress the open-circuit voltage below that which is theoretically possible (ref. 3).

EMITTER ETCHING EXPERIMENTS

That diffusion induced lattice stresses can have a significant effect on solar cell output can be demonstrated through an analysis of the results of an experiment in which the front face of a cell is chemically etched so as to remove thin layers of silicon from the emitter surface. The results of etching successive layers from the front face of a deep junction, 0.1 ohm cm silicon cell are shown in figure 1. As the thickness of the removed layer increases, the red (0.9 μm) response can be seen to pass through a maximum and then decrease rapidly. At the same time, the open circuit voltage is seen to decrease monotonically from its initial value. It is interesting to note that, even though we have not physically done anything to the base of this cell, the collection efficiency in that region has been drastically changed.

It also should be mentioned that throughout the etching process, the cell in figure 1 retained its ideal ($n = 1$) diode characteristic.

As severe as the degradation is, however, we have found that it is usually possible to restore the cell to, or close to, its original state by subjecting it to a thermal annealing cycle. Figure 2, for example, shows the spectral response of a 0.1 ohm cm cell before and after emitter etching. The initial junction depth was 1.2 μm and that after etching was a few tenths of a micrometer less. Also given in the figure is the response after the etched cell was annealed in air for an hour at 200° C. As can be seen, recovery is almost complete. The voltage is observed to recover in a similar manner.

In an attempt to identify the processes occurring during the etch and anneal cycles, we determined the activation energy for recovery by means of a series of isothermal heat treatments. The results are shown in figure 3. The measured value of 1.37 eV is very close to the 1.30 eV value reported for the activation energy for divacancy migration in silicon (ref. 4). Divacancy flow, it should be mentioned, has been shown to be responsible for the process of self diffusion in silicon (ref. 5).

ETCHING AND LATTICE STRESS

The fact that an etching operation performed on the emitter region can effect carrier collection in the untouched base region, and the fact that the resulting degradiation can be removed by thermal annealing both suggest the involvement of lattice stress in the etch induced output changes. That the annealing process takes place via atomic movement confirms these suspicions. It is not unreasonable, therefore, to conclude that lattice stresses are somehow created in both the emitter and the base by the etching process. However, while it is fairly clear that lattice stresses are active here, the exact mechanisms involved are apparently not very straight-forward. This is evident in the following attempt to provide a plausible, if somewhat involved, explanation for the observed facts.

The mechanism of etch induced stress generation is somewhat hard to envision. While the actual processes occurring are no doubt much more complicated, we will attempt to show in the following that the concept is feasible. Let us start by considering the schematic diagrams in figure 4.

Because the emitter has been enfused with a high concentration of misfitting phosphorus atoms, it will tend to contract. To the extent that this region is prevented from contracting because it is physically attached to lesser doped or undoped regions, it is put into a state of two dimensional tension. Accordingly, the regions adjacent to the emitter are put into compression. In order to explain the production of stress by the etching process, it appears necessary to postulate that, somewhere in the region of compressional stress, plastic deformation takes place, relieving some, if not all, of the stress between this region and the rest of the cell. It will be assumed henceforth that it is this stress between the emitter and the rest of the cell, not the stresses internal to the emitter, that cause voltage and current degradation. We can thus envision the cell (prior to etching) as consisting of a region near the surface, including the emitter, where tensional and compressional stresses are present and balanced by one another, and a

relatively stress free but plastically deformed region that connects this stress couple to the rest of the crystal.

If now the surface region that is in a state of tension is partially removed via the etching process, the adjacent compressively stressed regions will expand. This expansion places a tensional stress on the previously stress free connecting region and the regions beyond it. The unbalancing of the stress couple near the surface by the etching process can thus be seen to result in the generation of stresses in adjacent areas of the cell.

THEORETICAL CONSIDERATIONS

One of the effects of stressing a piezoresistive material such as silicon is a change in carrier mobility. In the case of diffusion induced stresses, one would expect the stresses and the resulting mobility changes to be localized in the vicinity of the emitter and the base region near the junction. If we calculate the effect of putting a region of increased mobility (10x that in rest of base) in the base adjacent to the junction, we obtain the curves shown in figure 5 (ref. 6). As the width, W, of the high μ region increases (corresponding to increased stress levels), the 0.9 μm response is seen to rise from its $W = 0$ value, to go through a maximum, and to return to its initial ($W = 0$) value when W is equal to the cell thickness, d. The open circuit voltage is seen to drop monotonically as W increases. These variations are similar to the measured changes in current and voltage as successive layers are etched from the emitter (fig. 1). There is, however, one significant difference between the measured 0.9 μm response curve and the calculated plot. While the $W = 0$ (zero stress) and the $W = d$ (maximum stress) responses in the calculated plot are seen to be identical, measured initial and final responses are not. The measured response after considerable etching is much lower than the initial, pre-etch value. This would seem to indicate that the initial state of the cell in figure 1 is one of considerable lattice stress. The data suggest further that the removal of these residual diffusion induced stresses from the as-fabricated cell should result in a significant rise in the open circuit voltage. The following section deals with our attempts to confirm the presence of diffusion induced stresses in as-fabricated devices and our attempts to remove them.

In summary, thus far, we have presented evidence that diffusion induced lattice stresses can indeed have a drastic effect on both cell voltage and base collection efficiency. We have found reason to believe that significant residual stresses exist in the as-fabricated cell which, if removed, should result in large increases in cell voltage.

RESIDUAL STRESSES

As previously mentioned, theoretical modeling of the etch induced red response variation suggests that significant voltage depressing stresses exist in the as-fabricated low resistivity cell. Further evidence for the existence of harmful residual stresses can be inferred from the fact that the two devices exhibiting the highest voltages to date for low resistivity silicon (the MINMIS and the MINP cells) are fabricated with very low doped emitters. The MINMIS cell (ref. 7) has, of course, an induced emitter and theoretically

should be completely stress free. MINP cell fabrication requires a very light diffusion that results in a total phosphorus deposition, S, of the order of $2\text{-}5 \times 10^{14}$ atoms/cm^2 (ref. 8). Ion-implanted MINP cells have also been made with depositions ranging from 10^{13} to 10^{14} atoms/cm^2 (ref. 9). Normal diffusions or ion implantations usually involve depositions that are several orders of magnitude higher than these levels.

Evidence has also been published (ref. 10) indicating that stress applied to a cell during diffusion in such a way as to reduce post diffusion stresses, can result in increased output. There appears to be sufficient evidence, therefore, to warrant an investigation of the effects of reduced phosphorus levels on the operating characteristics of 0.1 ohm-cm cells.

EFFECT OF LOW EMITTER DOPING LEVELS

In an attempt to reduce stress by reducing the amount of phosphorus deposited in the emitter, we performed a series of PH_3 diffusions at temperatures ranging from 850 to 950°, for times ranging from 15 to 30 min, and for phosphine concentrations ranging from 1 to 1000 ppm. To avoid any complications due to precipitation, the diffused cells were all subjected to rather long (16 to 65 hr) drive in cycles in the absence of a phosphorus source. Drive in temperatures ranged from 850 to 950° C.

After fabrication, the surface concentration, N_0, was determined from Irvin's curves using measured values of sheet resistance and junction depth. The values so obtained were verified by SIMS measurement on selected samples. The total phosphorus deposition, S, in the resulting gaussian distribution was then determined from the expression $S = N_0 [\pi Dt]^{1/2}$ where D and t are the drive-in diffusion coefficient and time, respectively. The product Dt was determined from a knowledge of the junction depth and the base doping level using the equation

$$N(x) = N_o \exp - \left[\frac{x^2}{4Dt} \right]$$

The open circuit voltage and the red response as a function of phosphorus deposition are given in figures 6 and 7, respectively. Although a reduction in residual stress levels at lower depositions should manifest itself as a drop in the 0.9 μm response and a rise in voltage, neither are seen in the figures. We are led to conclude, therefore, that contrary to earlier expectations, residual stress levels in these cells are either very small or are ineffective in degrading cell output.

This conclusion makes it diffucult to explain the experimentally observed etch induced degradation on the basis of mobility changes alone. To explain the large fall off in red response as etching proceeds, it appears that we must invoke the involvement of another current-affecting parameter such as the diffusion length, the variation of which with stress has been proposed by Rindner and Braun (ref. 11). Although we have no direct evidence that L changes are active in the measurements described here, such a variation would certainly be consistent with the observed facts.

SUMMARY OF RESULTS

The results of the preceding analysis can be summarized as follows:

(1) Diffusion induced stresses in low resistivity silicon solar cells can significantly reduce both the open circuit voltage and the base collection efficiency.

(2) The degradation mechanism involves stress induced changes in the base minority carrier mobility and diffusion length.

(3) Stress induced degradation can be removed by thermal annealing. Recovery characteristics indicate that the stresses are relieved at elevated temperatures by plastic deformation via divacancy flow (silicon self diffusion).

(4) The level of residual stress in as-fabricated low resistivity cells was found to be negligibly small.

REFERENCES

1. Y. Kanda: J pn. J. Appl. Phys. Japanese JAP 6 475, 1967.

2. G. H. Schwuttke, H. J. Queisser: J. Appl. Phys. JAP 33 1540, 1962.

3. M. P. Godlewski, T. M. Klucher, G. A. Mazaris, and V. G. Weizer: Conference Proceedings, 14th IEEE Photovoltaic Specialists Conference, 1980, p. 166.

4. G. D. Watkins, J. W. Corbett: Phy. Rev. 138 A 543, 1965.

5. D. L. Kendall, D. B. DeVries: Semiconductor Silicon, Electrochemical Society, NY, 1969, p. 358.

6. V. G. Weizer, M. P. Godlewski, R. J. Trivisono: Conference Proceedings, 15th IEEE Photovoltaic Specialist Conference, 1981, p. 892.

7. R. B. Godfrey, M. A. Green: IEEE Trans Electron Devices ED 27 737, 1980.

8. M. A. Green, A. W. Blakers, E. Gauja, M. R. Willison: Conference Proceedings, 16th IEEE Photovoltaic Specialists Conference, 1982, p. 1219.

9. A. W. Blakers, M. A. Green, M. R. Willison: Nucl Instrum Methods, 191 51, 1981.

10. J. Lindmayer, C. Y. Wrigley: Conference Proceedings, 13th IEEE Photovoltaic Specialists Conference, 1978, p. 450.

11. W. Rindner, I. Braun: J. Appl. Phys. JAP 34 1958, 1963.

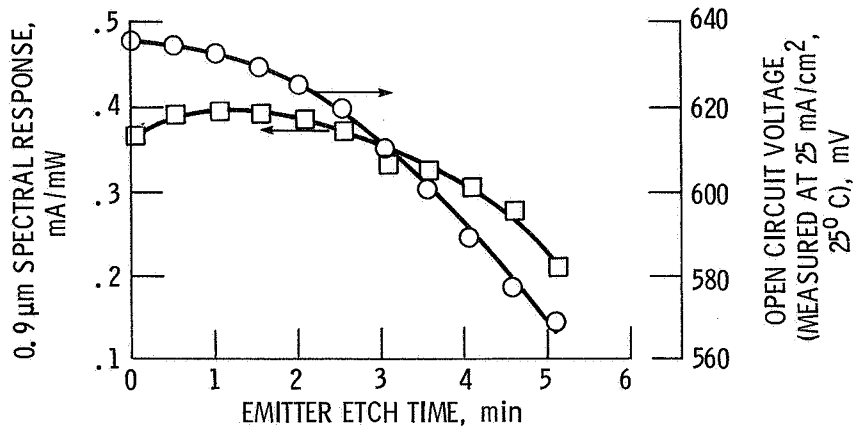


Figure 1. - Measured variation of 0.9 μm spectral response and open circuit voltage with emitter each time.

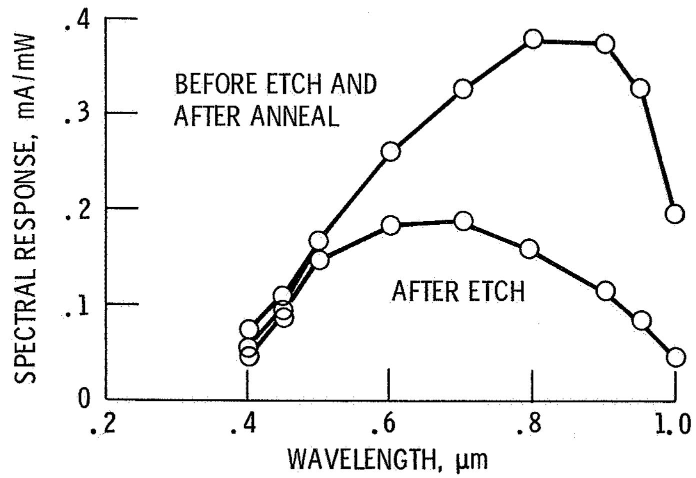


Figure 2. - Effect of emitter etching and annealing on spectral response.

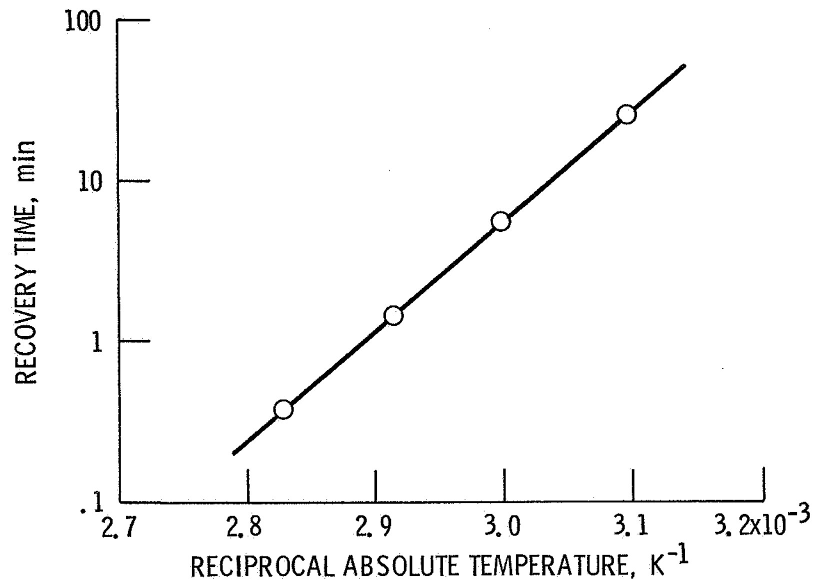
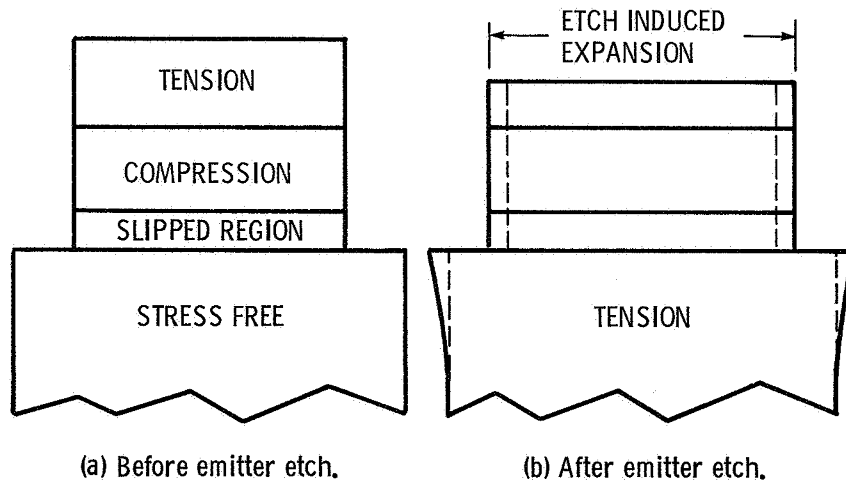


Figure 3. - Determination of activation energy for recovery from isothermal annealing data. Activation energy, 1.37 eV.



(a) Before emitter etch.

(b) After emitter etch.

Figure 4. - Schematic description of etch induced stress generation.

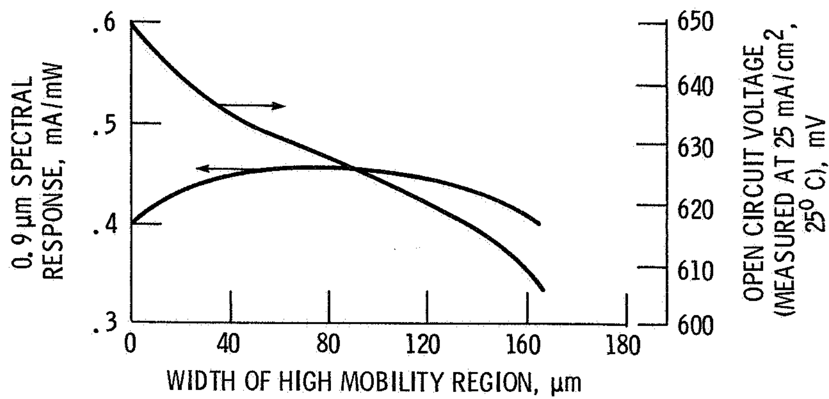


Figure 5. - Theoretical variation of red response and open circuit voltage with width of low mobility region in base adjacent to junction. Base width, 165 μm.

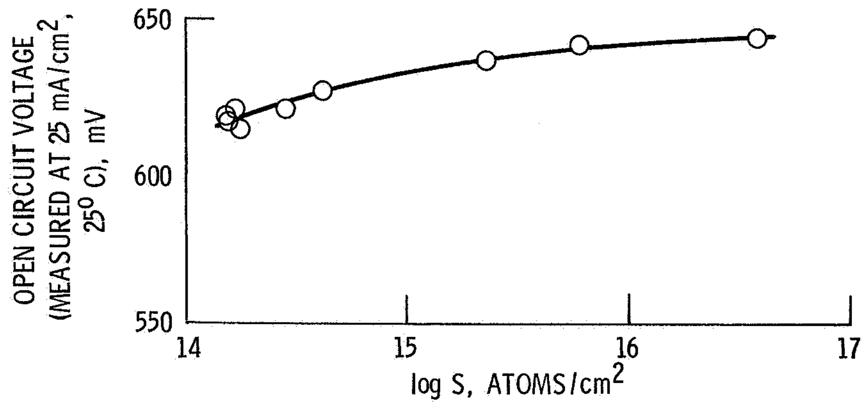


Figure 6. - Variation of open circuit voltage with total phosphorus deposition, S.

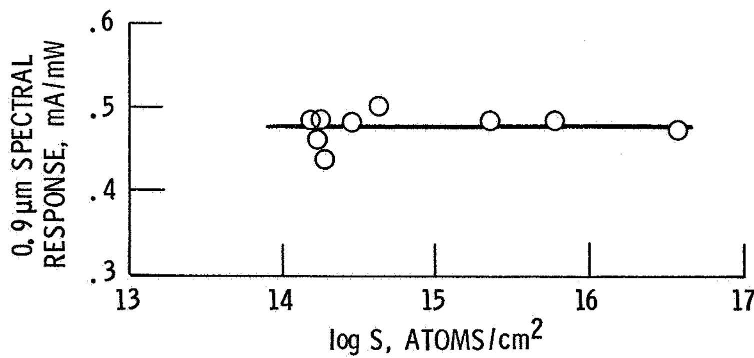


Figure 7. - Variation of red response with total phosphorus deposition, S.

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16. Abstract

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