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Technical Report

Grant No. NAG 3-316

DESIGN CONSIDERATIONS FOR A MONOLITHIC, GaAs, DUAL-MODE, QPSK/QASK, HIGH-THROUGHPUT RATE TRANSCEIVER

Submitted to:

National Aeronautics and Space Administration
Lewis Research Center
21000 Brookpark Road
Cleveland, Ohio 44135

Attention: Dr. Dennis J. Connolly
Solid State Devices and Passive Components Section

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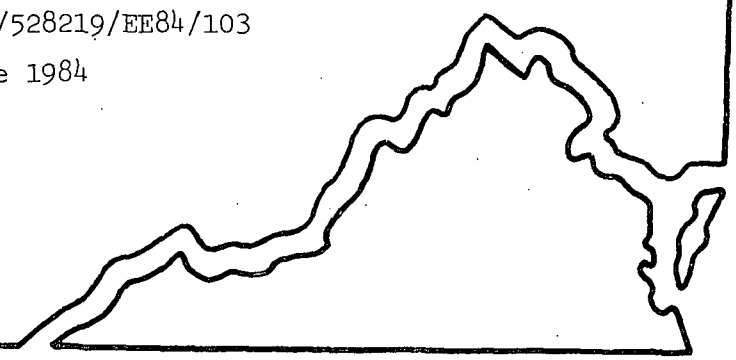
Report No. UVA/528219/EE84/103

June 1984



SEMICONDUCTOR DEVICE LABORATORY
DEPARTMENT OF ELECTRICAL ENGINEERING
SCHOOL OF ENGINEERING AND APPLIED SCIENCES
UNIVERSITY OF VIRGINIA

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May 1984

PREFACE

This report constitutes the thesis submitted for the degree, Master of Science (Electrical Engineering) of Richard A. Kot at the University of Virginia. The work was performed under NASA Contract NAG 3-316, and was supervised by Assistant Professor James D. Oliver, Jr., and Associate Professor Stephen G. Wilson.

Design Considerations for a Monolithic, GaAs, Dual-Mode, QPSK/QASK, High-Throughput Rate Transiever

A Thesis Presented to the
Faculty of the School of Engineering and Applied Science
University of Virginia

In Partial Fulfillment
of the Requirements of the Degree
Master of Science (Electrical Engineering)

by
Richard A. Kot
May, 1984

Abstract

This work constitutes a feasibility study for the implementation of a monolithic, GaAs, dual-mode, quadrature amplitude shift keying and quadrature phase shift keying transceiver with 1 and 2 x 10^9 bits per second data rate. The purpose of the study is to exploit the high-speed capabilities of gallium arsenide, so as to achieve a low power, small and ultra high-speed communication system for satellite as well as terrestrial purposes. The study includes a broad survey of recent GaAs integrated circuit achievements and evaluation of their constituent device types. Design considerations, on an elemental level, of the entire modem are further included for monolithic realization with practical fabrication techniques. Throughout this study numerous device types, with practical monolithic compatability, are used in the design of functional blocks with sufficient performances for realization of the transceiver.

List of Symbols

A	area
A_{TOT}	total area
A_d	attenuation constant
a	channel epitaxial thickness
a_1	region 1 undepleted channel thickness
a_2	region 2 undepleted channel thickness
a_3	region 3 undepleted channel thickness
B	admittance
BFL	buffered FET logic
BW	bandwidth
C_g	gate capacitance
C_{gs}	gate-source capacitance
C_{gd}	gate-drain capacitance
ΔC	changing capacitance
cm	centimeters
DCFL	direct-coupled FET logic
dB	decibells
dBm	decibells relative to milliwatt
d_o	inductor diameter
d_{min}	minimum delay line length
ϵ_r	relative permittivity
ϵ_{eff}	effective permittivity
E/DFL	enhancement-depletion FET logic
ϵ	permittivity
FET	field effect transistor
F_m	minimum noise figure
f	frequency in hertz
f_c	carrier frequency
G	conductance
Gbps	10^9 bits per second
GHz	10^9 hertz
GND	ground
GSPS	10^9 symbols per second
H	henrys
Hz	hertz
h	metalization thickness
I	current
IC	integrated circuit
I_D	drain current
I_{DSS}	drain saturation current ($V_g = 0$)
I_{dm}	maximum drain current ($V_g = 0$)
I_s	source current
I_1, I_2, I_3, I_4,	partial multiplier curents
$I(t)$	baseband signal
ΔI	available changing current
kHz	10^3 hertz
kb	10^3 bits
LPFL	low pinch-off FET logic
LSI	large scale integration
L_s	inductance

L_g	gate length
L_{gs}	gate-source separation
L_2	FET region 2 length
L_3	FET region 3 length
ℓ	delay line length
MAG	maximum available gain
MBPS	10^6 bits per second
MSL	medium scale integration
mil	10^{-3} inches
N	number of inductors
NF	noise figure
NRZ	non return zero
N_d	active donor concentration
N^+	degenerate donor concentration
n	number of inductor turns
P	power
Q	power stored/power lost
Q(t)	baseband signal
QASK	quadrature amplitude shift keying
QPSK	quadrature phase shift keying
R	resistance
R_c	contact resistance
R_d	drain resistor value
R_g	gate metalization resistance
R_L	load resistance
R_o	inactive gate channel resistance
R_{ON}	channel resistance ($V_g = 0$)
R_{op}	optimum FET matching resistance
R_S	source resistor value
SDFL	Schottkey diode FET logic
s	inductor metalization width
t	time
t_d	propagation delay
Δt	state change time
V	voltage
V_b	built in contact barrier voltage
V_{DD}	drain supply voltage
V_d	drain voltage
V_g	gate voltage
V_m	logic swing
V_s	source voltage
V_{SS}	source supply voltage
V_{SD}	source-drain voltage
ΔV	voltage change
V_P	phase velocity
V_s	saturation velocity
Z_L	comparator FET load width
Z_S	comparator FET switch width
w	inductor coil separation or height of depletion region
X	reactance
X_{op}	optimum matching reactance

Y_1, Y_2 channel current parameters
Z gate width
Z_c characteristic impedance
Z_{in} input impedance
Z_{out} output impedance
δ skin depth
λ wavelength
μ mobility

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1 Introduction

Over the past decade a new technology of monolithic integrated circuitry has been rapidly developing fabricated on gallium arsenide (GaAs) rather than silicon. Inspired by its advantages of high-speed, compared to silicon, GaAs integrated circuit technology is receiving widespread attention. The high-speed, or high frequency response, capabilities stem from the high mobility and high saturation velocity, while its low losses are due to low conductivity when in its undoped or semi-insulating state.

High-speed GaAs monolithic integrated circuitry is of particular interest in signal processing applications where nanosecond response is required. These applications include: high-speed digital logic, low-noise, high gain microwave amplifiers, amplitude and phase processing, delay lines, line switching, impedance matching, mixing and multiplying.

GaAs IC technology lags well behind silicon due to difficulties in achieving high quality GaAs crystalline material and partially due to the lack of appreciation of GaAs material qualities since, in the past, silicon has been adequate for most electronic applications. The most highly developed areas of GaAs IC technology are in high-speed logic, yet this technology still has not advanced past the early levels of silicon integration nearly 15 years ago. It is expected that GaAs IC technology will continue to develop

very rapidly with the recent advances in growth of high quality GaAs crystals, and with the modification and transfer, of the refined fabrication techniques of silicon ICs, to GaAs.

Theory of operation of GaAs devices exists in modest but unrefined form for a variety of discrete device types. Discrete device types with high performance have required exploitation, of particular GaAs capabilities, by optimization of parameters through fabrication techniques. This has been done without consideration of how the optimization of these particular parameters would determine the performance of another device type if included on the same IC with the same fabrication techniques. This comprises a significant deficiency in GaAs IC technology.

In this work the monolithic GaAs IC implementation of a dual-mode quadrature phase shift keying or quadrature amplitde shift keying (QPSK or QASK) digital transceiver, operating at high (1 or 2 gigabit/sec) data rates and with a 20 GHz carrier, is investigated. The realization of such a transceiver requires incorporating numerous device types on the same IC and thus with the same fabrication processes. This must be done with consideration of projections of practical levels of integration (complexity) attainable in the near future, limits in fabrication tolerances, acceptable whole-chip power dissipation and of course, acceptable total system performance. Again, throughout this work a solution is sought for practical realization of the

entire modem on a single GaAs integrated circuit. Many discrete functions required for this modem have been realized in various commercial and research laboratories with a wide range of device geometries and fabrication techniques. No manufacturer has ever fabricated such a system, with so many different functional units, on a single monolithically integrated circuit. The monolithic realization of this modem was a particularly challenging problem involving device type compatability. "Compatability" is defined here as the simultaneous realization of each device type with the same fabrication process. It is the purpose of this thesis to investigate the feasibility of realization of this transceiver on a single GaAs monolithic IC.

2 System Overview

The proposed system is a GaAs monolithic dual-mode QPSK/QASK transceiver. This system performs either QPSK (quadrature phase shift keying) or QASK (quadrature amplitude shift keying) to meet various communications requirements. QASK has the advantage of twice the spectral efficiency of QPSK while QPSK requires 4 dB less power for equal error probability.

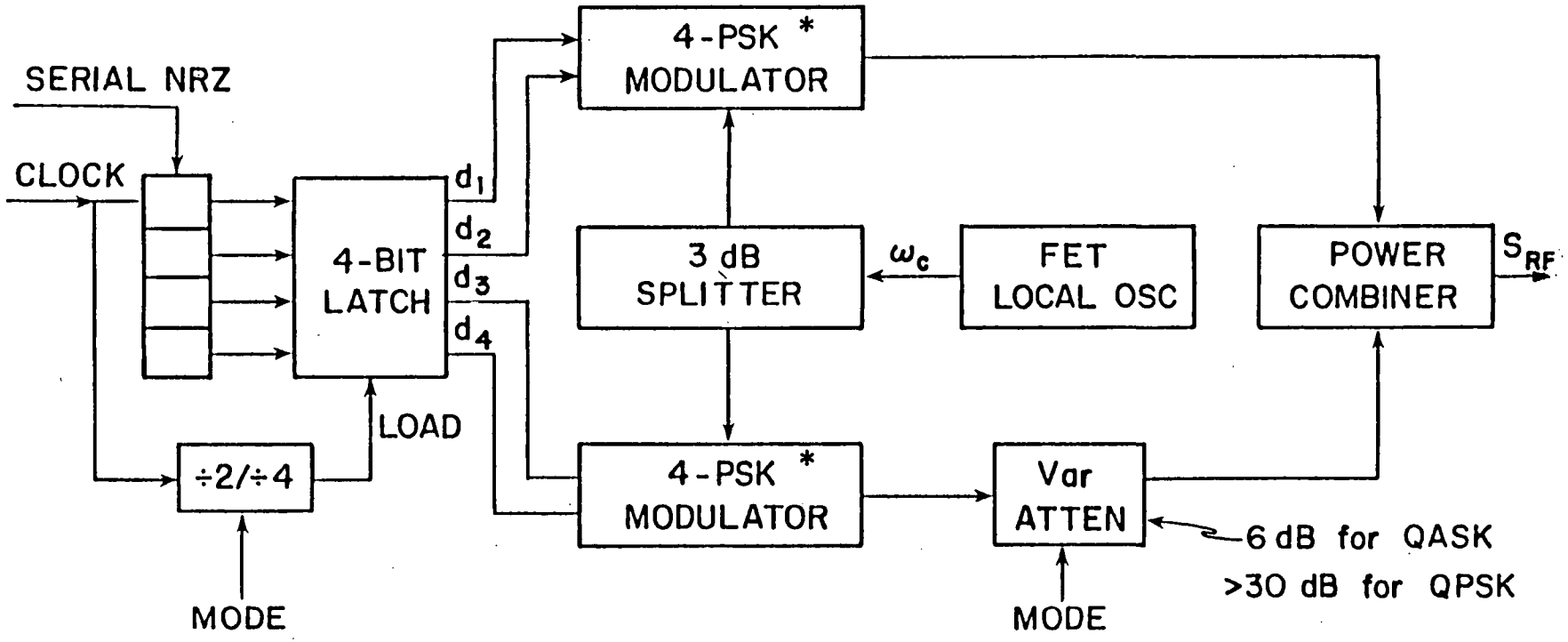
A dual mode QPSK/QASK system is chosen, rather than a single mode system, because of the similarities between the two types of signals and because of its advantage of increased flexibility. The signal similarities indicate the similarity of hardware needed for its implementation.

The QPSK signal consists of a 20 GHz carrier signal of constant amplitude modulated to four possible phases 0^{o}, 90^{o}, 180^{o} and 270^{o}, with each phase representing a two-bit word. The QASK signal consists of two QPSK signals, one attenuated by 6 dB relative to the other, added together. So, any one of four orthogonal phasors of equal amplitude are added to any one of four equal but orthogonal phasors with 6 dB relative attenuation. This gives 16 symbols (phase/amplitude combinations) each representing a 4-bit word. This indicates the similarity between hardware necessary for generating QPSK and QASK. The demodulation and processing schemes of QPSK and QASK typically differ

with QASK demodulation being much more complex than QPSK demodulation. However the dual modem demodulator and processor is negligibly more complex than the QASK demodulator though much more complex than a single mode QPSK demodulator. Selection of QPSK over QASK for the dual mode device is accomplished by switching off the lower level (6 dB attenuated) QPSK signal.

2.1 QPSK/QASK Modulator The QPSK/QASK modulator, shown in figure 2.1.1, is designed to operate at a fixed symbol rate of 500 x 10^6 symbols per second in either mode. This determines a throughput rate of 1 Gbps for QPSK and 2 Gbps for QASK. A fixed symbol rate modulator is simpler and maintains a fixed bandwidth in either mode.

The modulator inputs has serial non-return to zero (NRZ) data to a serial-to-parallel shift register which forms a word to be held by 4 latches during the modulation process (one symbol period). The mode selection capability, in part, comprises the selectability of clock on the 4 latches. QPSK requires the clock rate to be divided by two causing d_1 and d_2 (of figure 2.1.1) to be the significant word. As shown in figure 2.1.1, the 4 bit (2 bits for QPSK) word is split to control two (one for QPSK) QPSK modulators. The upper QPSK modulator is used alone for the QPSK mode, while the lower QPSK modulator's output is attenuated by 6 dB and combined with the upper for the QASK mode. The resultant signal is then amplified and transmitted. The modulator performance parameters are given in figure 2.2.1.



* 4-Phase modulator can be realized with path length modulator or dual-gate FET phase shifter

Figure 2.1.1, Diagram of Dual-Mode Modulator

TABLE 2.1.1 Modulator Performance Parameters

* 500 M symbols/sec, corresponding to 1 Gbps for QPSK, 2 Gbps for QASK
* interface logic capable of 4 GHz clock rate
* center frequency: selectable in 10-20 GHz range
* frequency stability of oscillator: $f/f_c < 5 \times 10^{-6}$ or 100 kHz at 20 GHz
* power output: 0 dBm into 50 ohms, VSWR < 1.5:1
* quadrature phase accuracy to within $\pm 2^{\circ}$, amplitude balance within 0.5 dB
* 2nd layer modulation 6 dB $\pm$ 0.5 dB lower in power
* NRZ modulation, bandpass filtering at RF assumed to reduce power spectral sidelobes, if necessary
* entire modulator on chip; possible off-chip dielectric resonator for FET local oscillator

Two parameters, listed in table 2.1.1, that are particularly important and worth discussion, are the 2 GHz clock rates and the quadrature phase accuracy of $\pm 2^{o}$, with amplitude balance of within 0.5 dB. Both of these are very demanding parameters and will especially dictate the choice of modulator designs. The 2 GHz clock rates should not be equated as the inverse logic gate propagation delay time because the fastest types of 2 GHz clocked logic circuit requires gates with twice this speed, or propagation delay of 1/4 GHz.

The $\pm 2^{o}$ phase accuracy, implemented at 20 GHz, puts very tight dimensional tolerences of about 0.5% on all RF transmission line components such as quadrature couplers and power splitters because of the possibility of added error for components in series. The 0.5 dB amplitude accuracy will tightly restrict the use of active devices used in generating the quadrature phasors because of the variability of device characteristics, of the same design, at different locations on the chip. Throughout the modulator all of the parameters are strictly considered for design and fabrication of a system with the highest likelihood of realization.

2.2 Quadrature Demodulator and Baseband Processor The receiver end of the QPSK/QASK modem consists of the quadrature demodulator, shown in figure 2.2.1, and the baseband processor, shown in figure 2.2.2. Figure 2.2.1 shows the received signal amplified and bandpass filtered.

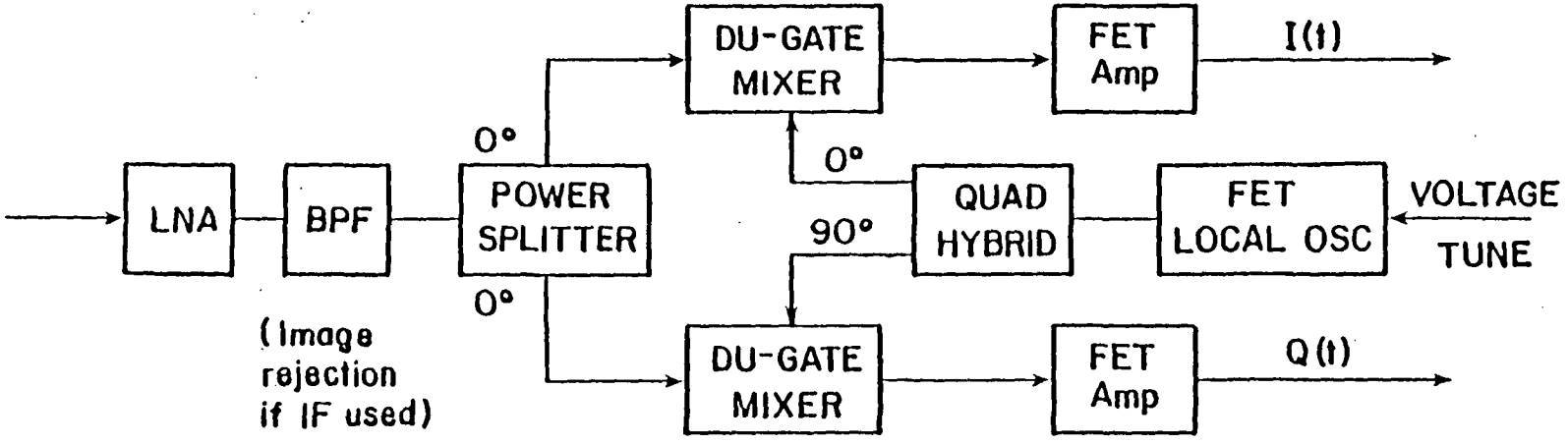


Figure 2.2.1, MMIC General-Purpose Quadrature Demodulator

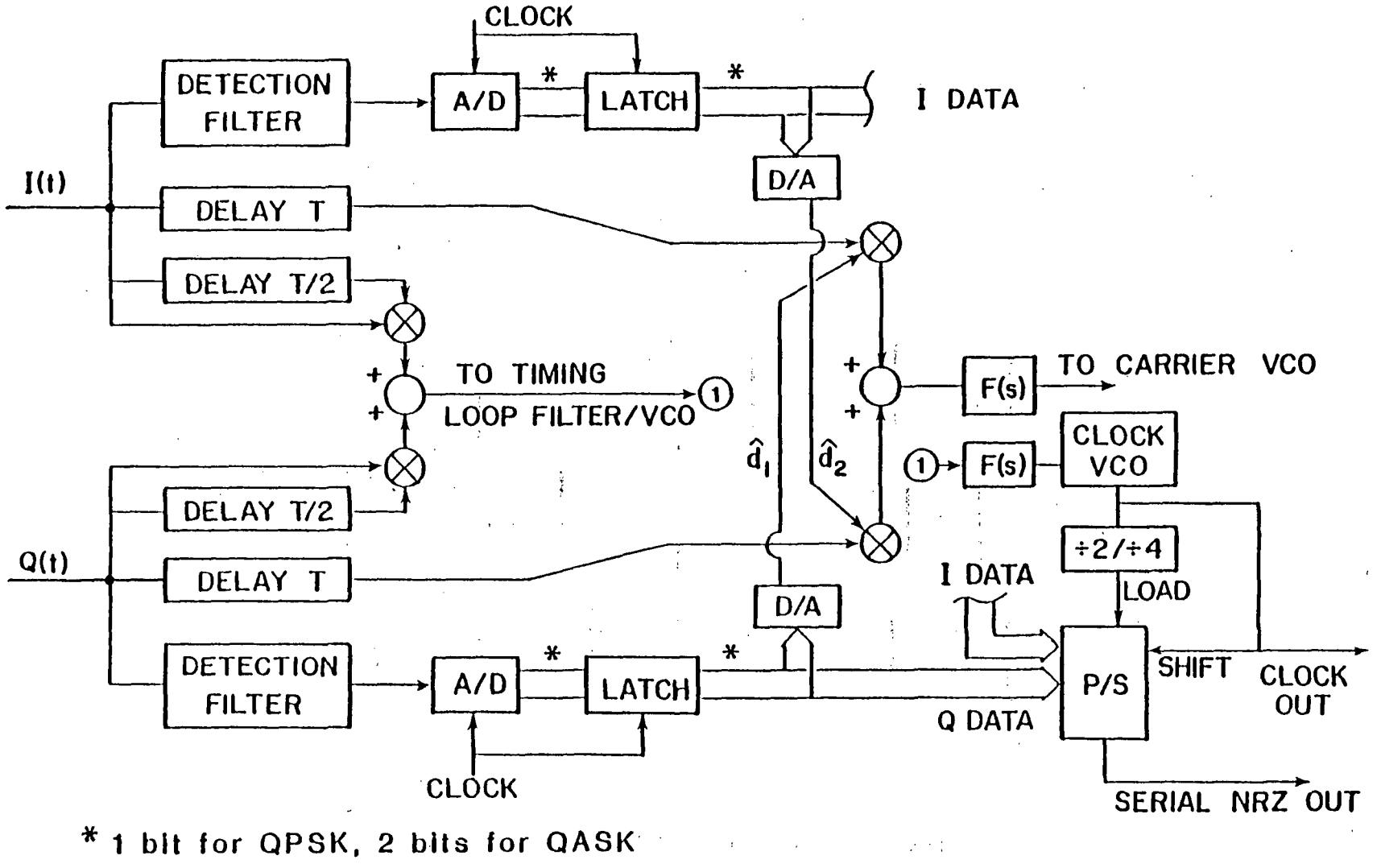


Figure 2.2.2, Baseband Processor Diagram (Detection, Carrier Synchronization, Symbol Timing)

The signal is then equally split and mixed with the LO phase locked to the received carrier. The receiver carrier has 0^{o} phase difference in the upper arm and 90^{o} in the lower arm. For QASK this mixing process can be thought of as forming, in one dimension, the 4 amplitude levels of the signal constellation. The upper mixer generates one of 4 possible levels on the x-axis of the signal constellation while the lower mixer (with 90^{o} LO shift) generates the y-axis signal levels of the signal constellation. For QPSK each mixer output (each axis) has 2 possible levels.

The demodulated and amplified signals Q(t) and I(t) are input to the baseband processor to undergo detection, carrier synchronization and symbol timing. The detection process is performed by separately filtering I(t) and Q(t) to eliminate out-of-band noise, then the resultant signals are sampled and held for digitization by a 2 bit (1 bit for QPSK) analog-to-digital converter. The analog-to-digital converter output is latched for output.

Carrier synchronization is performed by multiplying in phase I(t) and Q(t) by the quantized decision signal of Q(t) and I(t) respectively and adding the products together to give $(d_1\hat{d}_2 - d_2\hat{d}_1) \cos \theta + (d_1\hat{d}_1 + d_2\hat{d}_2) \sin \theta$ where d_1 and d_2 are the signal levels of Q(t) and I(t) and the "hatted" variables are the decision signal levels. Ideally the cosine term is zero if no decision signal errors have been made. The sine term is nominally small and represents an error voltage, indicating a phase

discrepancy. This positive or negative error voltage is used to change the phase (or frequency) of the voltage-controlled local oscillator (VCO). The VCO frequency changes so as to restore a minimal value to the term, effectively phase locking the (VCO).

Symbol timing is performed by delaying both I(t) and Q(t) by half a symbol period and multiplying by the undelayed I(t) and Q(t) respectively then summing the products together. The resulting voltage is filtered (integrated) and used to control the phase (or frequency) of the clock VCO so that the error voltage is minimized, similar to the method of carrier synchronization. The clock VCO is used to serially output the I and Q composite word using parallel-to-serial shift registers.

Tables 2.2.1. and 2.2.2 list the performance parameters of the quadrature demodulator and baseband processor respectively.

TABLE 2.2.1 Demodulator Performance Parameters

LNA:	f_c = 20 GHz noise figure: 2 to 4 dB, dependent on frequency, gain: 25 dB, 3 stages
BPF:	f_c = 20 GHz bandwidth : 2 GHz insertion loss over passband: <2 dB
Power Splitter:	power split within $\pm$0.5 dB phase equality within $\pm$ 2^o
Dual-Gate Mixer:	about 0 dB conversion loss
FET Video Amp and Base Band Data Circuit	bandwidth: 10 kHz to 2 GHz, $\pm$1 dB gain: roughly 40 dB
Quadrature Hybrid:	power split within $\pm$0.5 dB quadrature phase within $\pm$2^o
FET Local Oscillator:	f_c = 20 GHz voltage tuning range: $\pm$ 10 MHz, roughly 0.05% of f_c power output: +10 dBm into 50 ohms phase noise: -90 dBc 10 MHz from f_c frequency stability: $f/f_c < 10^{-5}$ over 0-50^{o}C VCO sensitivity: 1 MHz/volt

TABLE 2.2.2. Baseband Processor Performance Parameters

General:	Circuit uses decision-feedback synchronization for carrier with 2-level or 4-level detection in each quadrature arm as appropriate.
Delay Lines:	Bulk delay of one symbol interval, e.g. 2 nsec; delay should be "constant" over 1 MHz to 1 GHz.
Detection Filters:	For NRZ transmission, would ideally be integrate-and-dump, but at high speeds, distributed-circuit low-pass filters with $B = 1/T_s$ may be used.
Voltage Comparators:	Binary or 4-level flash converters using biased FET comparators; conversion-time on order of $1/2T_s$.
Multipliers:	Reasonable conversion loss (or gain). High performance is not very important since the product can be easily amplified.
Loop Filter:	Active filter providing $F(s) = (s + a)/(s + b)$, $b \ll a$, response. The constant a, along with loop d.c. gain, determines the loop bandwidth, typically on order of 10 MHz.

Table 2.2.1 indicates, in part, a particularly challenging technological feat in producing the 20 GHz low noise amplifiers (LNAs). The LNA parameters correspond to state-of-art developments in the field. Amplifying before mixing is chosen because of high noise and losses of integrated mixers at these frequencies and because the encouraging trends in LNA development indicate higher performance capabilities.

Another particularly important parameter is the 10 kHz to 2 GHz bandwidth of the video amplifier and baseband data circuit. This implies that no series coupling capacitor of reasonable size (of particular usefulness in DC level offsetting) can be used. This essentially determines a DC response. A DC response for the numerous functions to be performed here dictates an exceptionally challenging design problem.

One other very important design consideration required throughout the entire modem, if the modem is to be realized monolithically, is to keep the total chip power consumption under 2 watts. This parameter necessitates the modification of almost every design rule used in realization of discrete functional units presented in the literature, because most have been optimized at the expense of large power dissipation.

The performances and manufacturing requirements of the demodulator and baseband processor will be followed in this work without exception.

3 Component Discussions

3.1 GaAs Digital Logic

The logic types investigated in this study include enhancement mode field effect transistors (FETs), (E-MESFET logic), enhancement-depletion FET (E/DFL), low pinch-off voltage FET logic (LPFL), Schottky diode FET logic (SDFL) and buffered FET logic (BFL).[1] Basic circuit configurations are shown in figures 3.1.1 through 3.1.4. The propagation delays, clock frequencies, and maximum gate count are compared in table 3.1. For these devices, switching speeds are roughly inversely proportional to the gate length (L_g) for gate length larger than roughly L_g = 0.3 um [1A], whereas the gate power is roughly proportional to the gate length. A goal for the modem design is for the logic gates to operate at speeds greater than four GHz. This does not serve as a limitation with 0.5 um technology since all of the logic types operate at this frequency.

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[1] JFETs have not been considered since the technology lags that of other devices. Development is impeded by lack of a suitable p-type dopant implant, increased complexity and difficulty in fabrication [1].

TABLE 3.1. Comparison of Logic Types

FET Operation	Direct Coupled enhancement mode normally off	Low Pinch Off quasi-normally off	Schottky Diode depletion mode normally on	Buffered FET depletion mode normally on
Pinchoff voltage (V_p)	0 to +0.1	-0.3 to 0.2	-1.0	-1 to -2.5
Pinchoff tolerance	very tight	tolerant	tolerant	most tolerant
Voltage supplies (V_{SS} and V_{DD})	+1 to +1.5	+2.5	+2, -1.5	+3 to +4, -1.5 to -3.5
Power per Gate (mW)	0.01 to 1	0.5 to 2	0.5 to 2	2 to 40
Propagation Delay (ps)	100 to 500	100 to 150	70 to 120	50 to 100
Packing density (gates/mm^2)	1000 achieved LSI	400	400 achieved LSI	200
Maximum Packing Density (1 cm^2, 2 watts)	200,000	4000	4000	1000

All of the above values are for logic types with:

Gate Length L_g = 1 um

Gate Width Z = 20 um

Fan-in/Fan-out = 1

Schottky barrier height = 0.7 to 0.8 volts

Conductive layer thickness a = 0.05 to 0.2 um

Donor concentration $N_d \simeq 10^{17}$ to 3 x $10^{17} cm^{-3}$

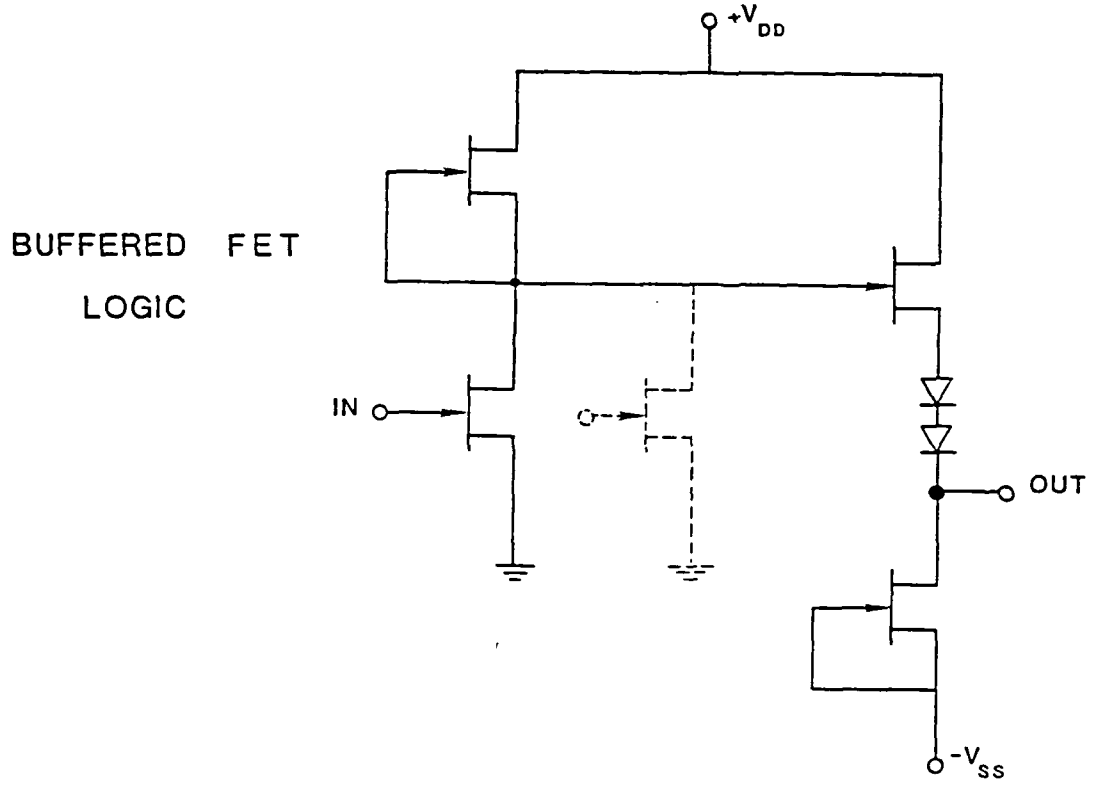


Figure 3.1.1 Inverter Gate, with Dashed FET Indicating NOR Geometry

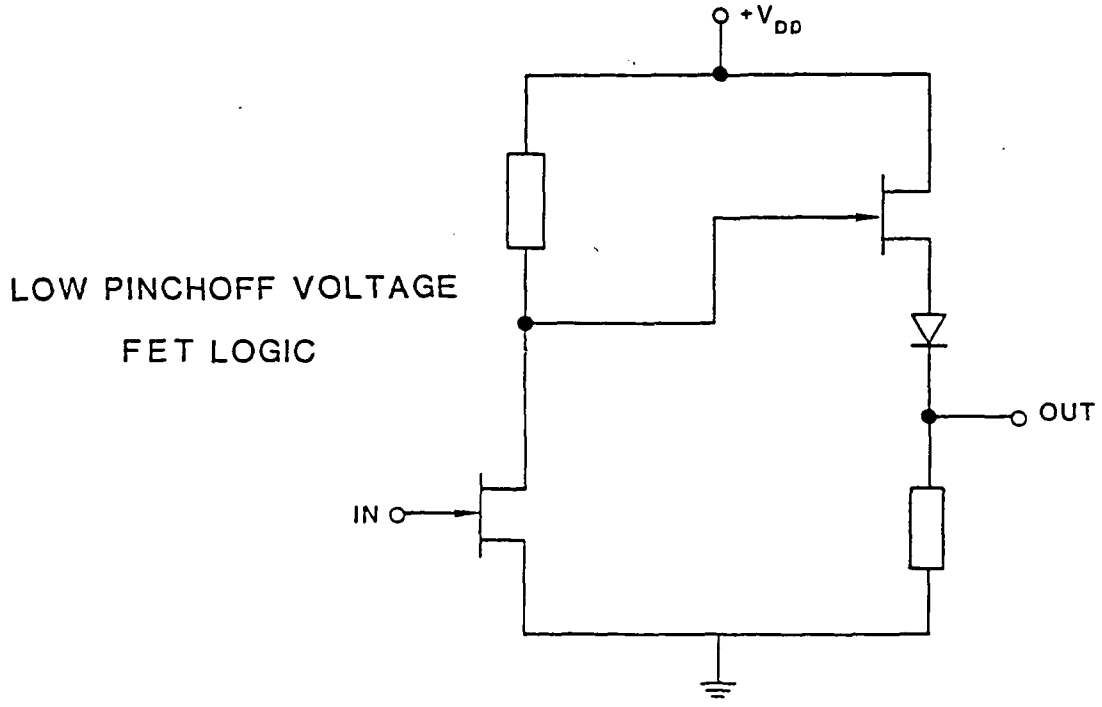


Figure 3.1.2 LPFL Inverter Gate. Boxes are typically resistors but may be active (FET) devices.

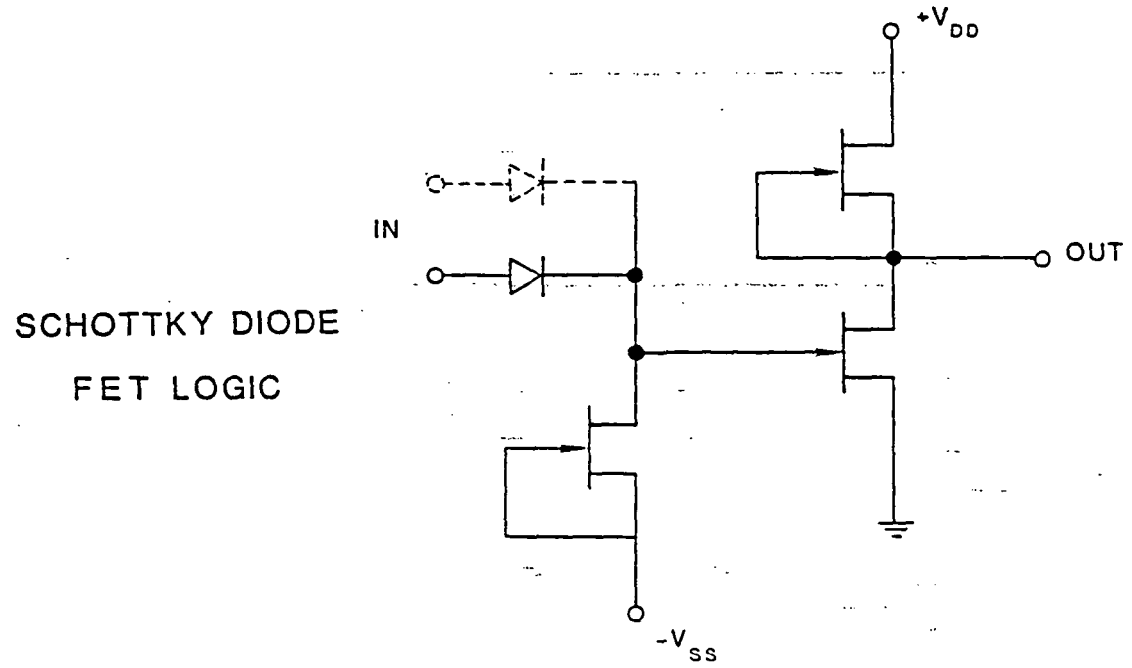


Figure 3.1.3 Schottky Diode Inverter Logic Gate where dashed diode shows NOR geometry

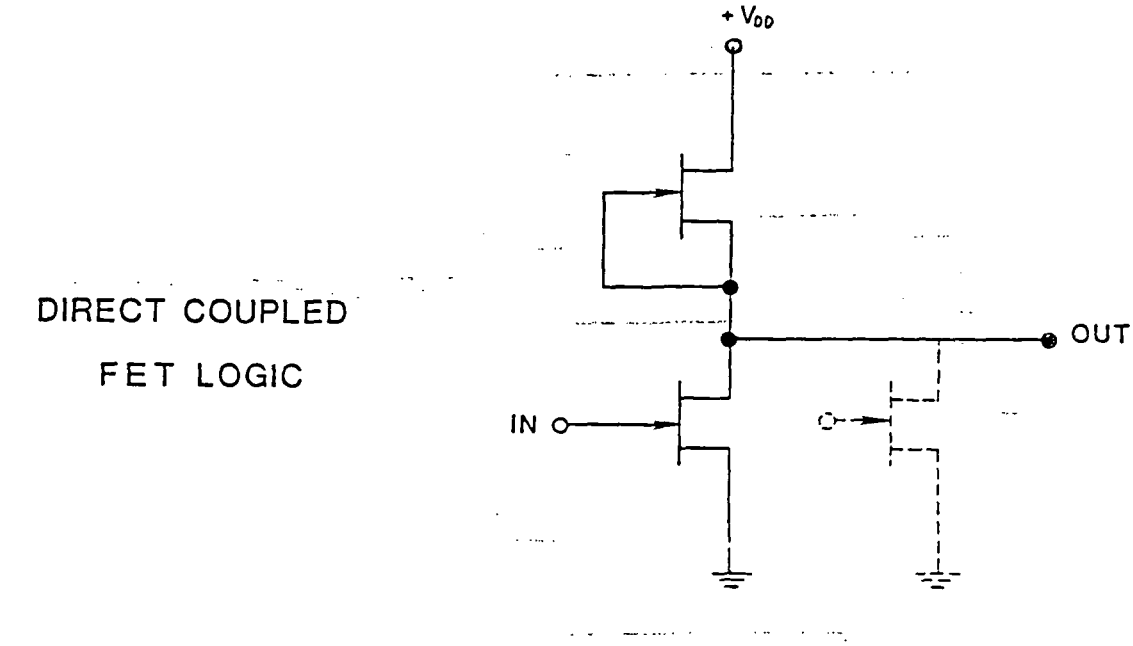


Figure 3.1.4 Direct Coupled Inverter Logic Gate with Enhancement Mode Input FET and Active (depletion FET) Load. Active load may be replaced by a resistor. Dashed enhancement FET shows NOR gate geometry.

In development of a monolithic chip containing both digital logic and microwave FETs, considerations of both feasibility and fabrication compatibility are important. The logic gate must function near 4 GHz, while the amplification, mixing and detection functions occur at 0-4 GHz for IF and 20-30 GHz for RF. While the devices for logic and microwave functions are widely different, the materials, geometries, and doping profiles must be similar and compatible if the design is to be realized monolithically on a single chip. In determining the compatibility of the various device types for monolithic IC realization, complexity and difficulty in fabrication are recognized as important restrictions. With this consideration "compatible" will be partially defined as the ability to restrict the design to having two channel types, i.e., channels with two heights or two doping profiles.

The operating characteristics of the various logic types are presented and examined for performance compatibility and current achievements. In this discussion the logic type evaluation is based on technology needed for 20 GHz LNA fabrication which requires gate lengths less than 0.5 um [2].

3.1.1 Buffered FET Logic. BFL has the distinct advantage of offering the fastest switching speed and the easiest to control fabrication [3] of all the logic types. The relative ease in fabrication stems from the less rigid control required for the large pinch-off voltages (V_p). The

relatively large voltage swing of 2.5 V also results in good noise immunity. BFL is fabricated with a minimum pinchoff voltage of approximately -1.5 volts, which is roughly the maximum V_P expected for the high frequency ≃ (20 GHz) low noise amplifier. The difference in the required pinch-off voltages renders BFL somewhat incompatible with 20 GHz low noise amplifiers and thus would require the formation of two different conductive layers, one for the logic FETs and one for the FET amplifiers. The low "on" state resistance of BFL FETs is compatible with switching FETs which may be needed in path length modulators (where high speed performance is of particular concern).

The very high speed capabilities of BFL have been shown by Liechti et al. [6]. A 5 Gbps (up to 6.5 Gbps) 8:1 parallel-to-serial converter was constructed with 600 active devices (400 MESFET and 230 diodes), utilizing the full available power budget of 2W per chip. Channels 0.25 um deep with $N_d \leq 2.5 \times 10^{17}$ cm^{-3} were formed with 500 keV Se implants at 6×10^{12} cm^{-2} through a 0.8 um thick Al mask. The channel and diode resistances were lowered with N^+ regions implanted with Si at 500 keV to 1×10^{13} cm^{-2} dose, then annealed with Si_3N_4/SiO_2 encapsulation at 850°C for 15 minutes. Ohmic contacts were formed by evaporation of NiCr, Ge and Au, and recessed, 1.0 um, Cr-Pt-Au gates were formed using liftoff. Second layer interconnects were formed with 1 um Ti-Pt metalization. The gates dissipated 10 mW of power for 60 ps propagation delay (unity fan in and fan out)

and 2.5 V logic swings. This example shows the very high speed and high power consumption of BFL.

The primary disadvantage of BFL, relative to application for this modem, is the high power consumption which limits the gate density to about 10^3 gates/chip. This is about twice the expected density of the modem design (vicinity of 500 gates). The minimum power dissipation of BFL is near the point of exceeding the maximum of the allowable power dissipation (~ 2 watts) [1B], [2], even without the inclusion of the numerous other functions to be performed on the chip.

3.1.2 Low Pinchoff FET Logic, Schottky Diode FET Logic (LPFL). The main motivation behind the development of LPFL was to avoid the fabrication problems of direct-coupled FET logic (DCFL) by allowing twice the flexibility in the range of pinch-off voltage control and yet maintain nearly the same simple circuit approach as DCFL ([7], p. 574). The threshold voltage (V_T) is -0.4 to 0.1 V where $-V_T = V_B + V_P$ and V_B is the built in barrier voltage [1A], [3]. After investigating LPFL, little advantage can be found over SDFL. SDFL is roughly 25% faster [3], [8], offers a more flexible design and fabrication scheme, and requires nearly the same power as LPFL. The gates may be designed to operate at very low pinchoff voltages and logic swings ΔV i.e. $V_P = 0.5$, $\Delta V = 0.5$, or by adding a level-shift diode, higher pinch-off voltages and higher logic swings may be used [1]. This would increase noise immunity and speed at the expense of

increased power. SDFL requires more V_P control than LPFL for a given design. The range of V_P in LPFL is 0.0 $\pm$ 0.2 volts [7].

Another important disadvantage of LPFL is the apparent lack of compatibility with line switching MESFETs of the phase modulators and with LNAs. Based on a survey of the channel characteristics of these devices, LPFL will have pinch-off voltages too small to maintain low channel resistance line switches and LNAs. LNAs with $V_T = -0.6 > (V_P = 0.1)$ have channel resistance too high for frequencies up to 4 GHz. This may not be true at higher frequencies. The channel requirements will be investigated in more detail using MESFET computer models [9]. Since the technology for tighter V_P control is developing rapidly, and since V_P control in SDFL is not a paramount problem, LPFL is not as popular as DCFL or SDFL and does not seem a likely choice in selection of a logic type for this modem.

An example of LPFL is given by Daymay, Nvzillat and Arnode [10]. Here a 2.8 GHz frequency divider has been fabricated which dissipates a power of 15 mW/gate. The FET was fabricated by vapor phase epitaxy (VPE) $N_d = 1.7 \times 10^{17}$ grown on Cr doped SI GaAs. Gates were 0.7 um delineated by direct e-beam writing and recessed by ion milling. Ohmic and Schottky contacts were made with Au:(Ge/Ni)Au and Ti/Pt/Au respectively and $V_P = 0 \pm 0.1$ volts.

3.1.3 Direct Coupled FET Logic: Enhancement MESFET, Enhancement/Depletion MESFET. Enhancement and

enhancement/depletion MESFET logic offer the convenience of requiring only one power supply (1-2 volts). Also, both have similar circuit configurations which are the simplest of all the other logic types (see figure 3.1.4). The main difference between the two is that the load in E/D-MESFET logic consists of a depletion FET while in E-MESFET logic the load consists of an ohmic, usually epitaxial, resistor. The FET load gives E/D-MESFET logic increased speed and a much sharper output voltage swing than the resistance load since its pull-up characteristics are parabolic (constant current), and thus stronger [1A], [2]. Both logic types require very precise control of the pinchoff voltage for the switching FET, i.e. $\pm$0.03 to $\pm$0.05 volts [1B]. This requires controlling the channel thickness to within $\pm$20Å. [1C], a current technological challenge. Considerations of compatibility with LNA fabrication show that no advantage is obtained with E-MESFET logic over E/D MESFET logic since the channels for the depletion mode LNA FETs are also necessary. E/D MESFET logic requires two different channel types. The pinch-off voltage of the depletion FET channel has a wide range; V_p = -0.85 to -1.5 [11], [12], and is compatible with the LNA depletion mode FET, V_p is roughly -0.5 to -2.0 V [6]. This flexibility stems from the D-MESFET's application as a constant current source. Within a wide range of V_p, the channel width (Z) is adjusted to give the required current needed to balance the gate's rise and fall times. Thus E/D MESFET logic should be chosen over E-MESFET logic

for application in this modem.

The highest level of integration of E/D MESFET logic found is a 1 kb static random access memory reported by Ino et al. [13]. The FET employed SAINT (Self Aligned Implantation for N^+ layer technology) with highly doped, N^+ Si ion implanted layers close to the gate, in order to increase the speed by decreasing channel resistances. Gate lengths for both FETs are 1 um and the driver, transfer, and depletion FET widths are 9, 4, and 4 um, respectively. Supply voltage is 0.7 to 1.5 volts and logic swing ~ 0.6 volts. The $N^+ \leftrightarrow N^+$ spacing is 1.5 um. Annealing was performed with Si_3N_4 encapsulation. SiO_2 deposition and gate-liftoff were also employed. This chip contains a total of 7084 FETs (4811 E-FETs and 2273 D-FETs).

Another example of LSI with E/D MESFET logic is presented by Fujitsu Laboratories [11]. The chip is a 6.4. ns, 6 x 6 bit multiplier comprising 408 NOR gates with 1284 enhancement and depletion FETs and dissipating 173 mW at V_s = 1.5 volts. Propagation delay per gate is 210 to 260 ps and dissipates 0.35 mW/gate at V_s = 1.5 volts. Fabrication techniques included a self-aligned gate 2 um long. The FETs were fabricated with Si^+ ion implantation at 59 keV with a dosage of 1.1×10^{12} cm^{-2} for the enhancement FETs and 2.1×10^{19} cm^{-2} for the depletion FETs. Self-aligned N^+ regions were formed with Si implantation at 175 KeV and a dosage of 1.7×10^{13} cm^{-2}. Annealing was performed with 0.1 um SiO_2 encapsulation at 850°C for 15

minutes. Gates and first level interconnects were delineated via TiW sputtering and reactive ion etching. Au-Ge-Au ohmic contacts were formed by liftoff and Ti-Au was used as a second level interconnect with a SiO_2 insulator. This example shows the low power, high integration level and speed (- 2 Gbps) capabilities of E/D MESFET logic.

An example of the high speed capabilities of E-MESFET logic is presented by Mitsui, Nishitani, Ishihara and Nakatani. [14]. Here a low power 1/256 prescaler MSI circuit with 80 gates is fabricated. The circuit consists of NOR gate implemented J/K flip flops with 40 um and 20 um gate widths for the high speed first and second stages respectively and 10 um gates for the slower stages to reduce power consumption. The maximum clock speed was 3.17 GHz and power dissipations per gate were 1.4 mW at 1 GHz and 15 mW at 2 GHz. The FET characteristics and fabrication techniques included a 0.3 to 0.35 um Su doped (1.8×10^{17} cm^{-3}) active layer with a deeply recessed (0.2 um) 1.0 um Al gate to avoid surface depletion. AuGe-Ni-Au ohmic contacts of 1.5 um thickness, were deliniated using "liftoff". Ti-Au interconnects were used with evaporated SiO_2 and plasma deposited Si_3N_4 insulators and spacers. V_T = +0.05 to -0.2 volts and V_{ds} = 1.0 volts.

3.1.4 Comparison of E/D MESFET and SDFL Further consideration of E/D MESFET and SDFL is necessary to determine applicability and compatibility with the proposed system. The switching diodes and the D-MESFETs ($V_P \simeq -1.0$,

[1C]) of SDFL do not require, but are usually implemented with two different doping profiles to optimize the speed of the switching diodes. Selective ion implantation is usually used to accomplish this optimization [1D], [2]. Although SDFL requires careful pinchoff control to obtain a low V_P, ([1B], [2]) and balanced driving capability, V_P does not have to be controlled as carefully as in DCFL ($\pm$30 to $\pm$50 mV). SDFL tolerates a deviation in V_P three times greater than for DCFL [7]. For this reason DCFL development has lagged behind SDFL technologies. However, both DCFL and SDFL have recently achieved LSI. DCFL stands to gain the most from refined fabrication technology, needed to achieve tight in pinch-off voltage control. This is expected in the near future.

Another advantage of SDFL is higher noise immunity due to larger voltage swings (0.5 to 1.4 V) [3]. The primary disadvantage of SDFL is that it uses 5 to 10 times the power of E/D logic [1C]. Doping concentrations used for both the LNAs and logic circuits are in the "typical" range of 1.2×10^{17} cm^{-3} to 2.5×10^{17} cm^{-3} (DCFL $N_d = 2 \times 10^{17}$ [1]). Both logic types have pinchoff voltages that would allow fabrication of channels with acceptably low "on" resistances needed for parallel (reflected) line switches as well as channel characteristics compatible with LNAs. The technologies involved in fabricating DCFL and LNA circuits have been closely paralleled, exchanging fabrication techniques to obtain similar channel characteristics. In

particular, the techniques involving V_p controls, channel resistances, contact resistances and gate size, have been shared [14]. This is considered an important advantage for the compatibility of SDFL and particularly E/DFL with LNAs. In conclusion both SDFL and E/D-MESFET logic should be strongly considered as compatible logic types for this modem development.

3.2 Theory of Operation for Logic Switches

The switching elements in this discussion are considered as simple FET loaded FET switches as in the enhancement mode inverter. SDFL and BFL require one and two more FETs, respectively, and diodes to compose an inverter.

The slew-rate-limited rise and fall times, i.e. switching speeds, are given by

$$t_d = 4C_L V_M/(3I_{dm}) = 4C_L/(3KV_M), \text{ [2]},$$

where V_m is the logic swing, $C_L = C_{gs}$ is the gate capacitance of the next device and $K = \epsilon uZ/(2aL_g)$ with (units in cm). Z = gate width, μ_n = mobility and L_g = gate length. GaAs has a dielectric constant of $\epsilon_r = 12.8$. This expression for t_d is based on ring oscillators where pullup and pulldown currents are equal ($I_{Load} = I_{dm}/2$). The maximum channel current is $I_{dm} = KV_m^2 = \epsilon uZV_m^2/(2aL_g)$, which is not equivalent to the channel the saturation current. The maximum channel current occurs at a lower drain-source voltage than the saturation current where the drift velocity (and current) is about twice as large [2].

For ICs with well designed layout the capacitive loading is equal to the gate capacitance of the next device, ($C_L = C_{gs}$) [1B]. A general expression for C_{gs} is: [1B]

$$C_{gs} = 2\,\epsilon L_g/Z\,(1 + (V_B - V_{gs})^{0.5}/V_o)^{0.5}/(1 + Z(V_B - V_{gs})^{0.5}/V_o^{0.5}).$$

For a one-sided junction this expression can be reduced to

$$C_{gs} = 0.3\ L_g Z(N_d/(V_B - V_{gs}))^{0.5}\ \text{pF},$$

where the gate length (L_g) is in microns, the gate width (Z)

is in microns and the doping (N_d) is in units of $10^{16}cm^{-3}$. This expression is further simplified by using the expression for the effective channel height

$$a = [7.23\ N_d/(V_b + V_g)]^{0.5} \text{ and}$$

$V_b = 0.78$ (for $N_d \simeq 10^{17}cm^{-3}$), giving

$$C_{gs} = 0.112\ L_g Z/a\ (0.78 + V_P)^{0.5}/(0.78 - V_{gs})^{0.5}.$$

Integrating C_{gs} over V_{gs} from 0 to the voltage swing (V_m) gives the average gate capacitance C_{gs}.

$$C_{gs} = 0.224\ L_g Z/(aV_M)[(0.78 + V_P)1^{0.5} - (0.78 + V_P - V_m)^{0.5}]\ pF$$

The expression for t_d then becomes

$$t_d = 4\ C_L/(3\ KV_m) = 5.4 \times 10^5/\mu(L_g/V_m)^2[0.78 + V_P)^{0.5} - (0.78 + V_P - V_m)^{0.5}]\ ps,$$

where $K = \epsilon uZ/2aL_g$ and u is the mobility.

This equation shows that short propagation delays require short gate lengths, high mobility and large voltage swings. For a typical channel of $N_d = 10^{17}cm^{-3}$, $\mu = 4000\ cm^2/V$ sec and with $L_g = 1$ um, $V_P = 1.5$ V and $V_m = 1$ V. The propagation delay is then $t_d = 51$ ps.

For maximum speed-power product we must have $V_m = E_m L_g = 0.3\ L_g$ [2], ($E_m \simeq 3$ kV/cm [2]) where E_m is the channel field strength needed for maximum channel current. The expression for the propagation delay is then

$$t_{d2} = 6 \times 10^{-7}/\mu\ [(0.78 + V_P)^{0.5} - (0.78 + V_P - 0.3\ L)^{0.5}]$$

for maximum speed-power product.

The expression for t_{d1} is independent of the source resistance (R_s) gate resistance (R_g) and only

dependent on the doping (N_d) and the channel height (a) via V_P. Although a convenient form to describe the logic circuits behavior, the equation is based on a number of significant approximations. One misleading fact is that this expression is independent of gate width. Fringing capacitance is the gate width restriction. Although this ring oscillator model does account for some fringing capacitance effects, as C_{gs}, becomes increasingly small, C_L to a larger extent becomes dominated by interconnecting line capacitance and other (source, drain) stray capacitances to the substrate or ground plane. Therefore $C_{gs} \neq C_L$. The gate width must be large so that fringing capacitances do not dominate and reduce t_d.

The expression for t_d represents operation with only the output gate loaded by another gate of equal size. In practice fanout may not equal one. For a fanout of two the load is doubled and therefore t_d is doubled if no compensation is included. The increase in capacitance can be compensated for by increasing the gate width, and therefore the driving currents of the preceeding FET [2]. But this causes increased input capacitance of the driver which in turn decreases the switching speed of its preceeding gate. A compromise then is necessary. The driver gate width must be fixed such that it only partially compensates for the increased load, likewise for the driver's driver FET in a cascading fashion.

Other assumptions made with the expression for t_d

involved neglecting partial channel resistances and gate metalization resistance. Also a fixed average gate capacitance was assumed. In order to neglect the partial channel resistances they must be small compared to the "on" channel resistance. Otherwise there would be a voltage drop across the partial channel (and active channel) which would effectively raise the voltage of the "low" state, causing the following gate not to be completely pinched off. The gate voltage can be shown to be

$$V_g = V_d(R_s + R_{ON})/(R_L + R_S + R_{ON})$$

where R_L is the effective resistance of the D-FET which carries half of the current of R_{ON} (or more precisely $R_{ON} + R_S$), to make rise and fall times identical. A large R_S can cause increased power consumption and device failure.

The gate resistance (R_g) is caused by ohmic losses in the gate metallization, and in this discussion, can also be considered as partially due to interconnect line resistances. R_g will decrease t_d by decreasing the pullup capability of R_L, by appearing in series with R_L, and decrease the pulldown capability of R_{ON}, by appearing in series as $R = R_s + R_{ON} + R_g$. R_g and the line load capacitance must be considered particularly during the circuit layout.

R_g and R_s need to be as small as possible in designing LNAs and line switching FETs. As discussed before, the primary sources of noise in LNAs are the gate metalization resistance and partial channel resistances and

therefore the LNA FET optimization serves the dual purpose of optimizing logic circuit performance.

3.2.1 FET Switches (General Considerations) A general expression for the switching speed (t_d) which is not specifically for ring oscillators is given by $t_d = C_L V_M / I_{ds}$ [1B], where C_L is the load capacitance which may consist of line capacitance, capacitors, stray capacitance and the gate capacitance of the next device. This expression will be used throughout much of this work when parasitic capacitances are considered separately.

The load capacitance may include varying amounts of stray capacitance depending on the circuit layout characteristics but more importantly, the load capacitance is determined by the gate capacitance of the following device. This gate capacitance is determined in different ways depending upon the voltage or voltage swing on the gate. The gate capacitance is a quickly increasing function of increased gate voltage. For FETs which have a gate voltage $V_g \simeq 0$, the capacitance is given by the empirical equation 6 (see table 3.1) for LNAs as $C_{gs}/Z = 0.34(N_d L_g^2/a)^{1/3}$. For FETs which have a gate voltage swing comparable to V_p, from 0 volts to roughly V_p, the capacitance is given in equation 7 (see table 3.1) for switching FETs as $C_{gs}/Z \simeq 0.06\ L_g/a$ [16].

Finding a representative expression(s) for the FET channel current I_{ds}, for any particular FET application, is a very perplexing problem and yet is of paramount importance

throughout this work. Over six different and commonly used expressions for the channel current have been found in the literature. All of these expressions have comparable form as functions of the gate and pinchoff voltage yet have magnitudes which vary, as functions of various channel parameters, varying widely in V_p by V_p *by* roughly a factor of two.

The complexity and difficulty in expressing the channel current can be better appreciated if one considers the behavior of current flow in GaAs. For low field strengths the current flow behaves like that of an ohmic conductor. As the field strength increases the current begins to lose its proportionality to the applied field and reaches a peak value of about 2×10^7cm/s at about 3 kV/cm. Further increasing field strength causes entry into a negative resistance region where current decreases with increased field strength. Beyond this region the current flow is roughly constant and considered saturated, but the current might have a slight increase or decrease with variation of the applied field depending on channel and material characteristics. For switching FETs the current flow behavior includes all of these operating regions.

The problem is further complicated by the behavior of the gate depletion region characteristics in these various operating regions. The depletion region characteristics are a function of both the applied drain-source voltage (V_{ds}), the gate-drain voltage (V_{gd}),

the gate-source voltage (V_{gs}), the gate length and channel height. The depletion region behavior is very complex. A comprehensive explanation of the depletion region behavior would be too lengthly and too much of a diversion to be given here. A few basic concepts, though, are given. When V_{gs} approaches V_P, the depletion region extends into the channel (uniformally for low V_{ds}) and completely pinches off the channel at V_P so that only a trickle of current (necessary to maintain the channel to depletion region potential difference) can flow through the channel. This defines V_P.

The depletion region elongates toward the direction of increased potential difference relative to the gate. Typically, this elongation is toward the drain which is of higher positive potential. The elongation shape is determined by the field strength along the channel which in turn is determined by the restriction of current flow by the depletion region directly under the gate. When V_{ds} becomes comparable to V_P, the elongated depletion region causes the channel to enter velocity saturation at the drain end. As V_{ds} becomes closer to V_P the depletion region elongates slightly more and the current enters velocity saturation over a longer channel region (possibly even longer than the gate itself). At suffcient V_{gd} ($\simeq V_P$) the depletion region and velocity saturation region change little with variation in V_{gd} and the FET is said to be in the "active", "pinchoff" or "linear" operation region where channel current flow is

roughly proportional to the applied gate voltage. The onset of this operation region is not sharp, and although it is generally considered occuring at $V_{gd} = V_P$, it can often be considered as occuring at substantially less than V_P particularly for large V_{ds}. Operation in the active region must be carefully considered in circuit designs for proper (linear) operation of many of the devices to be used in the dual modem.

With an understanding of the channel current characteristics the various models for I_{ds} were carefully scrutinized together with performance data of devices with devices of similar construction to that considered for this work and selected according to the device application. The selection involved finding a model for I_{ds} which would give reasonable values for the tranconductance (g_m). The selected representation for I_{ds} has the common form given by $I_{ds} = I_{DSS}(1 - V_{gs}/V_P)^2$. The transconductance ($g_m$) is then

$$g_m = dI_d/dV_g = 2\ I_{DSS}/V_P(1 - |V_{gs}/V_P|),$$

where I_{DSS} is the saturation channel current at $V_{gs} = 0$. The expression for I_{DSS} uses Fukui's expression for the saturation current with no gate depletion region (equation 4, [17]) modified by a multiplicative expression representing the extent of which the depletion region ocludes the channel, so

$$I_{DSS} = [1 - (V_b + 0.234\ L_g)^{0.5}/W_p^{0.5}]0.224ZN_da$$

For $N_d = 15 \times 10^{16} cm^{-3}$ and $V_P = 1.5V$, from figure 3.5.3,

this gives a = 0.145 um

The built in voltage V_b = 0.78V (equation 1, pg. 11)

and $W_p = V_b + V_P = 2.28V$

This gives I_{DSS} = 0.174Z for L_g = 0.7 um and I_{DSS} = 0.19Z for L_g = 0.3 um.

The expressions for I_{ds} and g_m are modified by redefining V_P to include V_b such that $V_P = V_P + V_b = 2.28V$.

So for 0.7 um gate FET devices I_{DSS} = 0.174Z and g_m = 0.149Z (0.152Z without subtle correction factor for other agreement considerations). For 0.3 um devices I_{DSS} = 0.19Z is used, but the transconductance is given by the Fukui's empirical expression (via figure 3.5.8) for RF amplifiers, rather than the above expression which gives g_m = 0.158 Z, even though both are in very close agreement. For most device applications the device can be considered as operating in the "active" region so these expressions will be used, but for some appliations the channel must be considered ohmic and device characteristics are determined by channel conductivity and depletion region depth.

3.3 Transmission Lines

Throughout this QASK/QPSK transmit and receive modem transmission lines must be used because of the high frequency signal processing required.

Some of the transmission line techniques include quarter-wave matching, power combining and dividing, phase changing and delay lines. All of these techniques, except for long delay lines, can be achieved using standard planar transmission lines.

The simplest and most easily fabricated transmission line, which is compatible with monolithic ICs, is the microstrip line (MSL). This structure consists of a conductive sheet of width (w) suspended by a dielectric of permitivity (ϵ_r) and thickness (h) over a ground plane. This geometry gives a quasi-TEM mode transmission line. The mode is not purely TEM because some of the electric field resides in the open space above the structure rather than in the dielectric.

MSL theory is standard and therefore, not discussed in detail here. Simple closed form expressions for the line characteristics are given by Bahl and Trivedi in [15]. The expressions for the most important characteristics are given as follows:

Phase velocity $v_p = C/(\epsilon_{eff})^{0.5}$, where ϵ_{eff} is the effective dielectric constant.

The wave length is given by

$\lambda g = v_p/f$

For $w/h \leq 1$ the impedance is given by

$$Z_o = 60/C_{eff}^{0.5} \ln (8\ h/w + 0.25\ w/h), \text{ where}$$

$$\epsilon_{eff} = (\epsilon_r + 1)/2 + (\epsilon_r - 1)[(1 + 12\ h/w)^{-0.5} + 0.04(1 - w/h)^2]/2$$

For $w/h \leq 1$ the impedance is

$$Z_o = 120/\epsilon_{eff}^{0.5}[w/h + 1.393 + 0.667 \ln (w/h + 1.444)]^{-1} \text{ where}$$

$$\epsilon_{eff} = (\epsilon_r + 1)/2 + (\epsilon_r - 1)(1 + 12h/w)^{-0.5}/2.$$

Other expressions for correction of error due to thick metalization are given in [15] but are not important here.

The dielectric constant for GaAs is $\epsilon_r = 12.8$. A survey of the literature on GaAs ICs employing MSLs shows standard substrate thicknesses of 100 um. This standard is adopted for this work. Thinner substrates are difficult to realize because the brittle nature of GaAs make grinding, lapping and polishing difficult. Although thinner substrates would give higher dielectric and metalization losses, the MSL circuit area decreases in proportion to decreasing substate thickness.

The expressions listed show, for $\epsilon_r = 12.8$, h = 0.1 mm and a line width of w = 0.088 mm that the line impedance is $Z_o = 50$ ohms and the guide wavelength is 5.2 mm at 20 GHz. This line width will be used often throughout this work. The highest practical impedance obtainable with MSL is about 85 ohms.

The dielectric and metalization losses, as a

function of the materials and geometry, are also given in [15]. Although semi-insulating (SI) GaAs has a low loss tangent of $\delta = 5 \times 10^{-4}$, it will be the dominant source of losses. The attenuation constant from dielectric losses is given by:

$$A_d = 27.3\ \epsilon_r/\epsilon_{eff}^{0.5}\ (\epsilon_{eff} - 1)/(\epsilon_r - 1)/\lambda_o\ \tan\delta \text{ db/cm.}$$

A wide variety of stripline techniques and impedance discontinuity analysis are available in the literature.

3.4 GaAs Fabrication Techniques

Though it is not within the scope of this work to investigate in detail the various fabrication and processing techniques, the important points are discussed briefly here.

High quality, bulk, semi-insulating (SI) GaAs is usually achieved by the Czochralski reactor process. This process, for SI GaAs, may include light chromium doping to offset the effects of impurities on the carrier concentration. The Cr doping results in lower mobilities and reproducability problems in fabrication results [18]. For this reason high purity and very lightly Cr doped SI GaAs is desirable [19].

Layer formation is achieved by a variety of epitaxial growth processes or ion implantation. Common growth processes are liquid phase epitaxy (LPE), molecular beam epitaxy (MBE) metal organic vapor phase epitaxy (MOVPE) and vapor phase epitaxy by tricloride transport (VPE). Formation of an active epitaxial layer requires introducing highly controlled levels of impurities (dopants), into the reaction, during the growth process. Common N type dopants are S, Si, Se and Te. Run-up and through-put time per slice range from 6 months, and 12 hours for LPE and 2 weeks, and 1 hour for MBE respectively [1E]. The investment expense for the short process time of MBE is about $300,000. A table of fabrication technique evaluation is given in [1E].

IC pattern definition usually employs photo-lithographic processes which have abilities to achieve gate

lengths as small as 0.5 um (with etch reduction). Electron beam lithography has also become widely used with its advantage of even smaller (0.2 um) pattern definition.

Various metals are used for Schottky barrier gate formation with the most popular being Al, TiW, (T(W,Si)) and TiPtAu. Aluminium gates are most frequently used in LNAs because of its low loss but Al gates are also popular in logic circuits. Titanium tungsten silicide (T(W,Si)) gate technology has recently received much attention in the self aligned gate process. T(W, Si) has the advantage of being very stable at the high annealing temperatures required after ion implantation, so no reaction occurs between the W(Ti, Si) and the GaAs [11]. This way is demonstrated in the fabrication of a completely planar 6 x 6 bit, 6 ns, E/D logic multiplier, employing 3 implants (N^+ region), SiO_2 encapsulation and annealing [11]. W(Ti). VS. W(Ti,Si) annealing tests show large accumulations of Ti at the GaAs interface after annealing for W(Ti) but little Ti diffusion occurs for the W(Ti, Si) [20].

3.4.1 Recessed Gate The recessed gate process has been widely used for fabrication of channels, particularly for LNAs. In this process the channel region is formed by etching (by various techniques) the epi layer (typically about 0.5 um initially) by a few tenths of a micron at the point where the gate will be deposited. The etch (recess) depth determines the channel thickness. The principle advantages of the recessed gate technique stem from the high

conductivity of the unetched area in the source-gate-drain spacing, the control of channel thickness and the high quality, undamaged, crystaline GaAs which needs no annealing (unlike ion implanted channels). The advantages of this structure are often accentuated by implanting N^+ regions under the source and drain contacts and in the inactive channel region to further reduce the source-channel and contact resistances. N^+ implantation reduces the surface depletion region which is particularly important in devices with thin epilayers, such as E-FETs [21]. This will be discussed in more detail in section 3.5.

A refined example of the recessed gate process is the fabrication of 18 GHz FET amplifiers with 8.5 to 11 dB gain and a noise figure of 1.75 dB [22]. 0.25 um Al gates were defined by e-beam lithography, with 0.3 um recess, on MOCVD epi. MOCVD is noted [22] as being superior to VPE in its ability to provide better uniformity of device characteristics and epi layers with higher mobility.

The principle limits to performance and yield are the precise gate recess etch, for reducing to the desired V_p, and the critical realignment of the gate electrode to the existing channel region [20]. These limits are surmounted by ion implantation using the self-aligned gate technique.

3.4.2 Self Aligned Gate and Ion Implantation The self aligned gate technique, along with implanted active channel regions, is used with the same advantages as the recessed gate technique with an added disadvantage of damaging the

GaAs crystal lattice during implantation. This technique has the added advantage, over the recessed gate technique, of requiring no etch process and no critical gate mask realignment. The gate metalization, or its respective deliniating resist ("T" gate), is used as a mask for defining the N^+ implant region in the source-gate-drain spacing. This is discussed in more detail in section 3.5. This technique has its highest utility in fabricating E-FETs where channel uniformity and parasitic source channel resistance reduction are the key elements.

Since ion implantation disrupts GaAs crystalline properties, repair is usually performed by annealing and to activate implants. Typical annealing temperatures are 800 to 850°C. At these temperatures GaAs disassociates at the surface necessitating surface encapsulation. Encapsulation is typically performed by rapid chemical vapor deposition of 1000 Å of silicon nitride followed by 1500 Å of sputtered silicon dioxide [23]. Cooler and longer anneals (850°C for 30 min. vs. 900°C for 30 sec.) give better carrier activation and higher mobilities [23].

3.5 High-Frequency GaAs Low-Noise Amplifiers (LNA)

The preliminary receiver modem design consists of a RF (20 GHz) amplification stage, followed by quadrature detection processes. A high-gain, low-noise RF amplification stage is necessary to minimize noise contributions from the mixing and baseband amplification.

Typical low-noise amplifiers have a channel doping $N_d = 1 \rightarrow 3 \times 10^{17}$ cm^{-3} and a height of 1000-2000Å [1G]. Noise reaches a minimum around 2.5×10^{17} cm^{-3} probably due to lack of sharpness of the doping profile at the channel/buffer interface [3], whereas gain begins to saturate near 3×10^{17} cm^{-3} for a gate length of 0.5 um.

The largest noise sources are the source contact, channel and gate metalization resistances. Gate metalization of 4000Å thickness is adequate in reducing gate resistance. Increased thickness beyond 4000Å gives only a small improvement [1H]. Source resistance may be decreased by recessing the gate (increase S-G-D channel height), increasing the doping under the source and drain region (ion implantation under contacts), increased channel doping or decreasing the source-gate separation [1]. If N^+ contacts are used the dominant channel resistance is due to undercutting, near the gate, during the channel definition process [1H]. Device geometry can be optimized to minimize these parasitics [24] and thus minimize the noise [14], [8] without changing the channel height.

The most outstanding performance of GaAs LNAs

noted to date has been reported by Watkins and Schellenberg [25]. This $\lambda/4$ x 30 um interdigitated MESFET demonstrates 5.0 dB gain at 52 to 62 GHz with a 7.1 dB noise figure (NF) at 60 GHz. The best performance at 30 GHz is 2.6 dB NF with 8.3 dB gain. These devices were formed by either ion implantation or VPE techniques with VPE showing both superior gain and noise figure.

For integrated microwave amplification, Watkins, Schellenberg and Yamasaki [22] have reported a 27.5 to 30 GHz GaAs FET amplifier with 4.6 dB NF and 17.5 dB gain. Three stages of amplification were used. The first and second stages consist of 0.25 x 75 um FETs with total gate periphery of 150 um. The third stage consists of 0.5 x 50 um FETs with a total periphery of 100 um. The gates were delineated by direct electron beam lithography. These amplifiers are employed in a receiver containing a 25-30 GHz dual gate FET mixer with a 10 dB NF and a dielectrically stabilized FET oscillator. This concept of RF amplification and establishment of the noise figure, before mixing, appears to be the most suitable process for the receiver in this work.

From the description of FET geometry for logic and microwave applications, it is noted that in all cases, the geometry is extremely similar with the exception of channel heights and widths. Low noise amplifiers typically have wider gates for smaller source-gate resistances than logic circuits. The implanted channel dopant is usually Si

(atomic number 14), occasionally Se, while S (atomic number 11) often is used for deep N^+ contact implants [7].

3.5.1 Active Channel Characterization To aid in analysis of various GaAs device types, the active channel is characterized by its geometry and composition. The geometry comprises the gate length (L) width (w) and height (a) as shown in figures 3.5.1 and 3.5.2. The Schottky barrier gate metal and channel doping density (Nd) determine the channel composition. An important, but secondary, effect of channel composition is the quality of the epitaxial GaAs, which, if poor quality, reduces carrier mobility and saturation velocity. Good fabrication techniques result in channels with high carrier mobilities and high saturation velocities which lead to low noise and high gain as will be seen later.

Throughout this work the gate metal to be considered is Aluminium. Aluminium is commonly used as a gate metal primarily because of its high conductivity. Extensive FET analysis has been made based on this metal.

Referring to table 3.5.1, equations (1) through (4) of table 3.1 ([17], [27], [28], [29], Fukui) show channel characteristics in terms of geometry and composition for aluminium gates. From equation (1), the built in Schottky barrier voltage (V_b) is a slowly increasing function of doping and V_b is 0.78 volts for typical values of N_d.

Equation (2) shows, as a function of N_d, the applied gate voltage (V_g) and the depth (w) and the extent

to which depletion region of the Schottky barrier extends into the channel. The depleted region is free of carriers that contribute to conduction. If the gate is forward biased to $V_g = V_b$, $w = 0$, so the channel is fully open (no depletion region) and can conduct a maximum current of I_s given by equation (4). I_s is proportional to both doping (N_d) and the effective channel height (a).

Equation (3) shows the relationship between the carrier concentration, the pinchoff voltage (V_P) and the effective channel height (a). This equation is plotted for a .vs. N_d for various V_P in figure 3.5.3. The pinchoff voltage is the gate voltage which completely depletes the channel of any carriers. V_P is probably the most important channel characterization that can be used to describe FETs. For this reason V_P will be constantly referred to along with figure 3.5.3 for either N_d or a.

3.5.2 Low-Noise FET Analysis In order to gain insight into particular FET characteristics both the recessed gate FET and the self-aligned N^+ implantation FET are analyzed in detail. The two structures, shown in figure 3.5.1 and 3.5.2, can be analyzed in the same way, using the same expressions to represent all of the device characteristics. To better understand this, compare the various epitaxial characteristics shown in figures 3.5.1 and 3.5.2. Notice that both structures have characteristics determined by N_d or N^+, a, a_1, a_2, a_3, h, R_g, R_1, R_2, R_3 , L_g, L_2, and L_3.

The evaluation of the channel resistances, and

RECESSED GATE FET

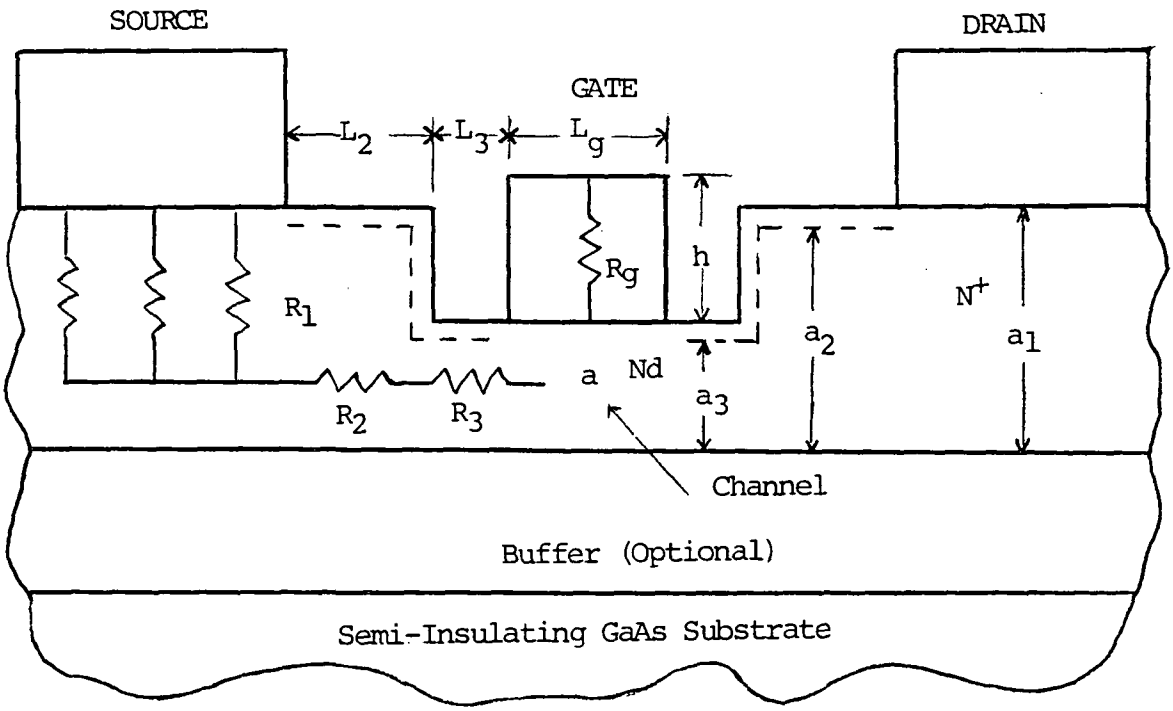


Figure 3.5.1, Recessed Gate FET Geometry

ION IMPLANTED
SELF ALIGNED GATE
FET

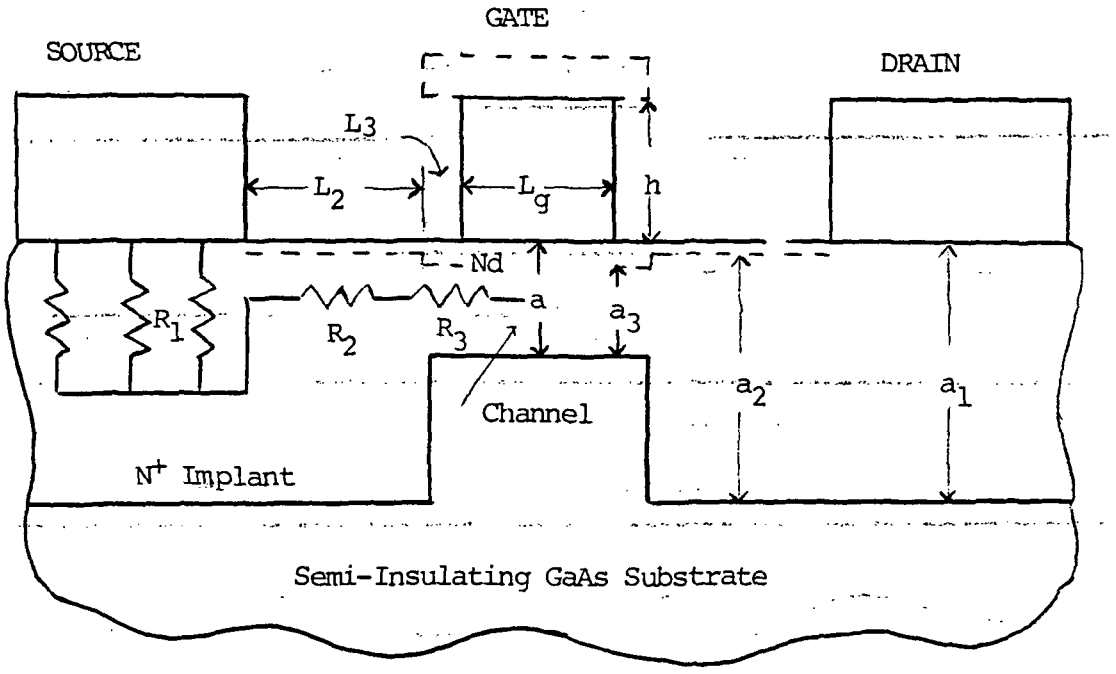


Figure 3.5.2, Self-Aligned Gate FET

Table 3.1

Equations for MESFETS

These equations are the most important equations used for determining FET device characteristics and are used extensively in this work. The computer plots are based on these equations.

1 $V_b = 0.706 + 0.06 \log N_d$

Schottky barrier built in voltage for Aluminium gates. N_d in units of $10^{16} cm^{-3}$. [17]

2 $w = [(V_b - V_g)/7.23\ N_d]^{1/2}$

Width of depletion region for $N_a >> N_d$, (0.035 um for $N_d = 100$), w in microns, N_d in units of $10^{16} cm^{-3}$. [17]

3 $a = [(V_p + V_b)/7.23\ N_d]^{1/2}$

Effective channel height under the gate in microns. N_d in units of $10^{16} cm^{-3}$. [17]

4 $I_s/Z = 0.224\ N_d a$

Maximum fully-open channel current per unit gate width. I_s (amperes), Z (mm), N_d ($10^{16} cm^{-3}$) and a (um). [17]

5 $g_m/Z \simeq 0.023\ (N_d/aL_g)^{1/3}$

Average transconductance per unit gate width (empirical). g_m (mhos), Z (mm), N_d ($10^{16} cm^{-3}$), a (um) and L_g (um). [2]

6 $C_{gs}/Z \simeq .34(N_d L_g^2/a)^{1/3}$

Average gate-source capacitance per unit gate width for Aluminium gates with zero volts average bias. C_{gs} (pF), Z (mm), N_d ($10^{16} cm^{-3}$), a (um) and L_g (um). [2]

7 $C_g/Z = 0.06\ L_g/a$

Average gate capacitance for switching FETs with Aluminium gates and voltage swing 0 to $-V_P$.
C_g (pF), Z(mm), a (um) and L_g (um) [16]

8 $$C_{gs} = L_g Z \left| \frac{q\epsilon\epsilon_o N_d}{-2(V_b - V_{gs})} \right|^{1/2} = .3Z\ L_g \left| \frac{N_d}{V_b - V_{gs}} \right|$$

Gate-source capacitance for logic circuits as a function of the gate-source voltage (V_{gs}).

C_{gs} (pF), Z (mm), N_d ($10^{16}cm^{-3}$) and L_g (um). [18]

9 $$R_s Z = R_1 Z + R_2 Z + R_3 Z$$

$$= \frac{2.1}{a_1 \cdot^5 N_d \cdot^{66}} + \frac{1.1 L_g}{a_2 N^{\cdot 82}} + \frac{1.1 L_g}{a_3 N_d^{\cdot 82}}$$

$$= 0.256 + \frac{0.033}{(a-w) N_d^{\cdot 82}}$$

Total source-channel resistance (from source to the gate for zero gate-source voltage) times the gate width (sum of partial channel resistances).

Z (mm), N_d ($10^{16}cm^{-3}$), N_1 ($10^{16}cm^{-3}$), a_x (um), and L_g (um). For this work $a_1 = 0.25$, $a_2 = 0.25 - 0.035$, $a_3 = a - w$, $L_2 = 0.47$ and $L_3 = 0.03$. [27]

10 $R_{ON}Z = (1.1L_g/a_3 N_d^{\cdot 82}) + 2R_s Z$

Total source-drain resistance times the gate width for Aluminium gate FETs with zero volts bias. The first term is for the channel resistance under the gate, and the second term is for the partial channel resistances.
Z (mm), N_d ($10^{16}cm^{-3}$), a_3 (um) and L_g (um). [16], [17]

11 $R_{gt}Z = Z_1^2 [34/L_g + (1.84(f/L_g)^{1/2})]$

Total gate resistance times the gate width as seen by a signal input to the gate. The first term is for the ohmic resistance, while the second term is due to skin effects. (Aluminium metalliztion thickness (h) is 0.5 um).
Z (mm), Z_1 (mm), L_g (um) and f (GHz). [2], [14]

12 $F_m = 1 + 0.038f(N_d L_g^5/a)^{1/6}(R_{gt}Z + R_sZ)^{1/2}$

Minimum noise figure for aluminium gate FETs (h = 0.5 um) based on empirical analyses.
Z (mm), N_d (10^{16} cm^{-3}, a (um), L_g (um) and f (GHz). [2]

13 $X_{op}Z = 0.16/fL_g$

Optimum gate matching reactance times the gate width for gates with zero volts average bias.
Z (mm), L_g (um) and f(GHz). [2]

14 $R_{op}Z = 2.2[(1/4g_m/Z) + R_{gt}Z + R_sZ]$

Optimum gate matching resistance times the gate width, for minimum noise figure.
Z (mm) and g_m (mhos). [2]

15 $MAG = (15.9v_s/fL_g)^2 R_{on}/(R_g + R_{on}/2 + R_s)$

Maximum available gain (empirical model)
v_s (10^7 cm/S), f (GHz) and L_g (um) [2], [17], [30]

16 $F_m \simeq 1 + (fL_g/4)[g_m/Z(R_sZ + R_{gT}Z)]^{1/2}$

Minimum noise figure (velocity saturated model) for $g_m/Z = v_s C/h(V_g)$, $v_s = 1.2 \times 10^7$ cm/S and at 300°K.

Z (mm), f (GHz) and L_g (um). [30]

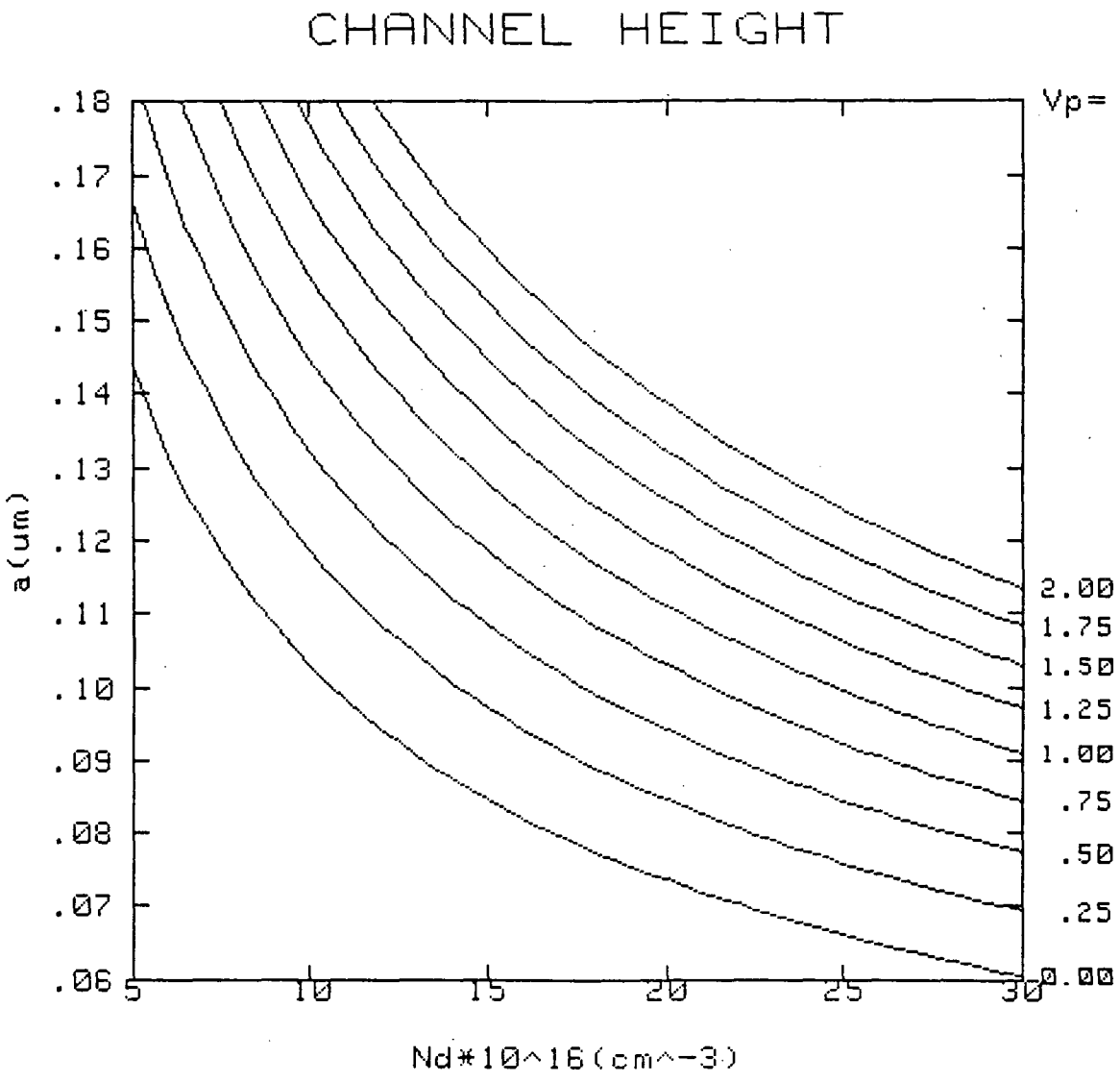


FIGURE 3.5.3, THIS PLOT SHOWS THE RELATIONSHIP BETWEEN THE GaAs MESFET ACTIVE CHANNEL EFFECTIVE HEIGHT AND THE CARRIER CONCENTRATION FOR VARIOUS PINCHOFF VOLTAGES. THIS PLOT CAN BE USED, TOGETHER WITH OTHER PLOTS OF MESFET CHARACTERISTICS, TO FIND THE CHANNEL HEIGHT FOR A GIVEN PINCHOFF VOLTAGE AND CARRIER CONCENTRATION.

subsequent evaluation of the maximum available gain and minimum noise figure, follow the empirical analysis given by Hatsuaki Fuki, with modifications such that the analysis is particularly applicable to the self-aligned implanted N^+ technology (SAINT) structure, rather than the recessed gate structure. Analysis for the structure fabricated with "SAINT" is emphasized because of the relative simplicity of fabrication of epitaxial layers that in particular give two FETs with different channel characteristics. Two different FETs are absolutely necessary if E/D FET logic is used (as discussed previously).

The recessed gate and the SAINT techniques are sufficient for reducing channel resistances. This can be seen from the noise figure results of ion implantation in [2], and results on source resistance as a function of recessed depth in [1G]. Employing recessing and N^+ implantation simultaneously gives little added benefit (~ 0.4 ohm), i.e. from 2 to 1.6 ohms [1H]. Decreasing the source-drain separation also proportionally decreases the epitaxial resistance (excluding the source contact resistance). The source contact resistance (R_1) is dramatically decreased by N^+ implantation under the contact [1G]. The active channel resistance decreases with increased doping but increased doping is limited by the gate breakdown voltage and by inactivation of carriers at even lower doping concentrations (about $3 \times 10^{17} cm^{-3}$) [1G].

The total source resistance is given by equation 9

(table 3.1). For this work choose a_1 as 0.25 um, to be consistant with both fabrication techniques, and L_2 as 0.47 as a compromise for analyzing both 0.3 and 0.7 um gate lengths and simultaneously considering their respective gate delineation tolerances. L_2 is not a critical parameter for determining the device characteristics using either fabrication technique. L_3 is chosen as 0.03 um to be particularly consistant with "SAINT" capabilities.

The length (L_s) is determined by the gate resist mask overhang shadowing the ion implantation from the channel region. L_3 should be made small to reduce the significant effects of R_3, in the lightly doped channel region, but not so small as to make the channel depletion region touch the highly doped N^+ region; this would cause increased gate-source capacitance. N^+ with a value of 100 x $10^{16}cm^{-3}$ is sufficient degenerate doping for reducing R_s.

In order to understand how this configuration does not increase the capacitance, consider the proximity of the gate to the N^+ region using figure 3.5.2. Since there exists a surface depletion of 0.035 um for the N^+ = 100 ($10^{16}cm^{-3}$) region, determined by the doping concentration via equation (2), the effective length of L_3 is increased to about 2 x 0.035 um = 0.07 um and the distance from the closest points between the gate and N^+ region is slightly more than this. Also, since the depletion region around the gate is about a_3 = 0.08 um, (eqn. (2), N_d = 10) the two regions will not significantly overlap to cause increased

gate capacitance for L_3 - 0.03 um.

The equation for R_s is a function of N_d, a, and thus V_P, via equation (3). When the source resistance is doubled to account for the symmetric drain resistance and added to the partial channel resistance under the gate the result, from equation 10, gives the total drain-source resistance (RonZ), where Z is the gate width. This result is very useful in determining the performance of line switching FETs. The gate-source voltage changes RonZ by changing the undepleted channel height under the gate. For the gate forward-biased to the built in voltage V_b the channel is fully open with height, a, and for $V_g = 0$ the channel is partially depleted to height $a_h = a - w$, where w is given by equation (2). Normally $V_g = 0$ will be considered as determining the open channel resistance later in this work. A plot of RonZ is given in figure 3.5.4.

As discussed earlier, the gate metalization resistance, R_gZ, is a major contributor to the FET noise. The noise dependence on the metalization thickness is plotted in [1H] for 14 GHz. The decrease in noise (especially at higher frequencies) is not dramatic for gate metalization thickness greater than h = 0.5. Equation (11) gives R_gZ where the first term describes the frequency independent resistance and the second term describes the skin effect. Notice how short gate finger widths (Z_1) quickly reduces the gate resistance.

The gate resistance, source resistance and channel

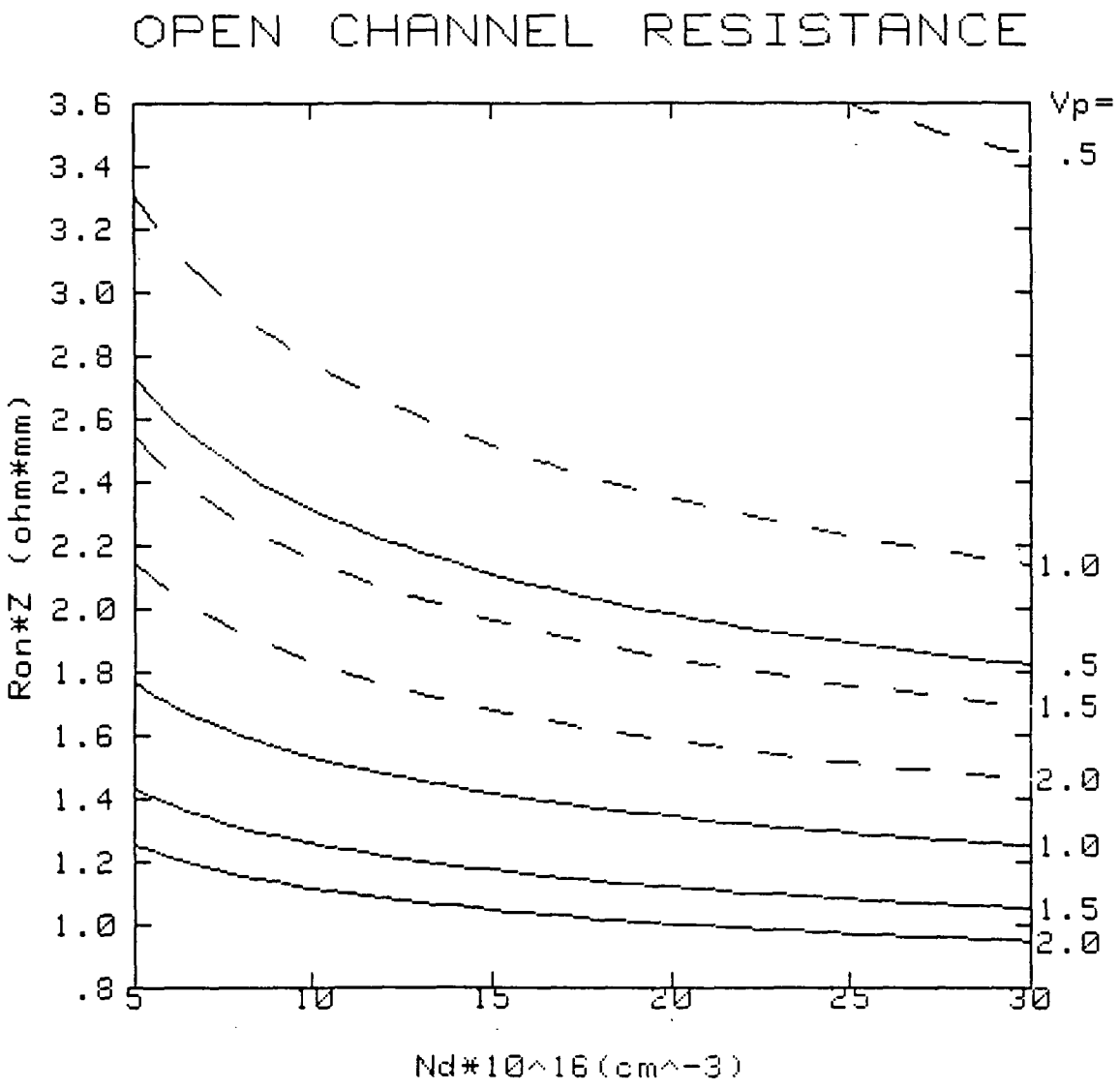


FIGURE 3.5.4, THIS PLOT SHOWS THE RELATIONSHIP BETWEEN THE SOURCE-DRAIN CHANNEL RESISTANCE ,OF MESFETS WITH GATE VOLTAGE Vg=0, .vs. CARRIER CONCENTRATION FOR VARIOUS PINCHOFF VOLTAGES AND GATE LENGTHS.

GATE LENGTH Lg=0.7um (DASHED LINE), Lg=0.3um (SOLID LINE)

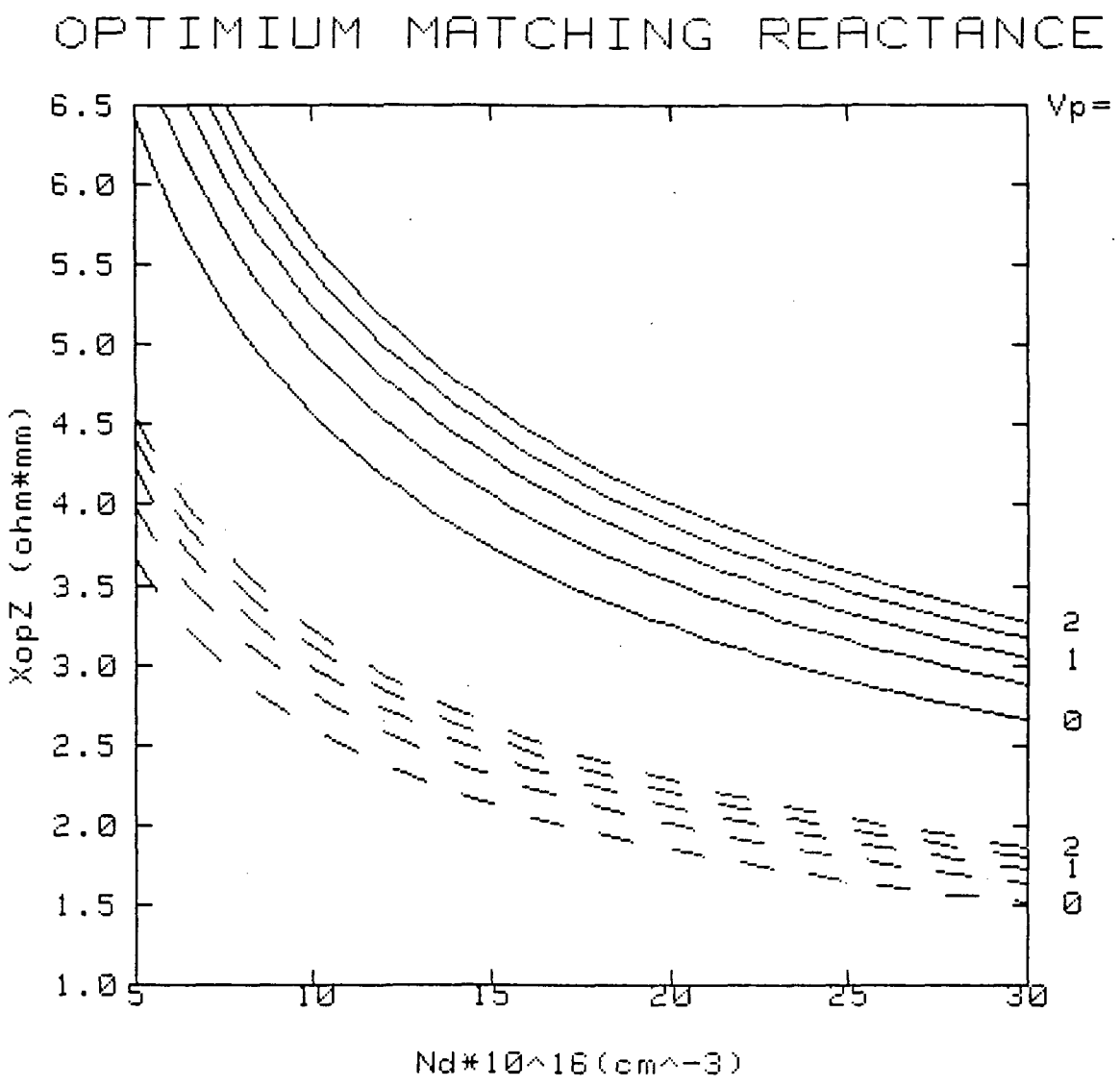


FIGURE 3.5.5, THIS PLOT SHOWS THE RELATIONSHIP BETWEEN THE LNA GATE REACTANCE (*GATE WIDTH (mm)) .VS. CARRIER CONC.,FOR PINCHOFF VOLTAGES IN STEPS OF 0.5 VOLTS AND AT f=20 GHZ.

GATE LENGTH =0.3um(SOLID LINE), =0.7um(DASHED LINE)

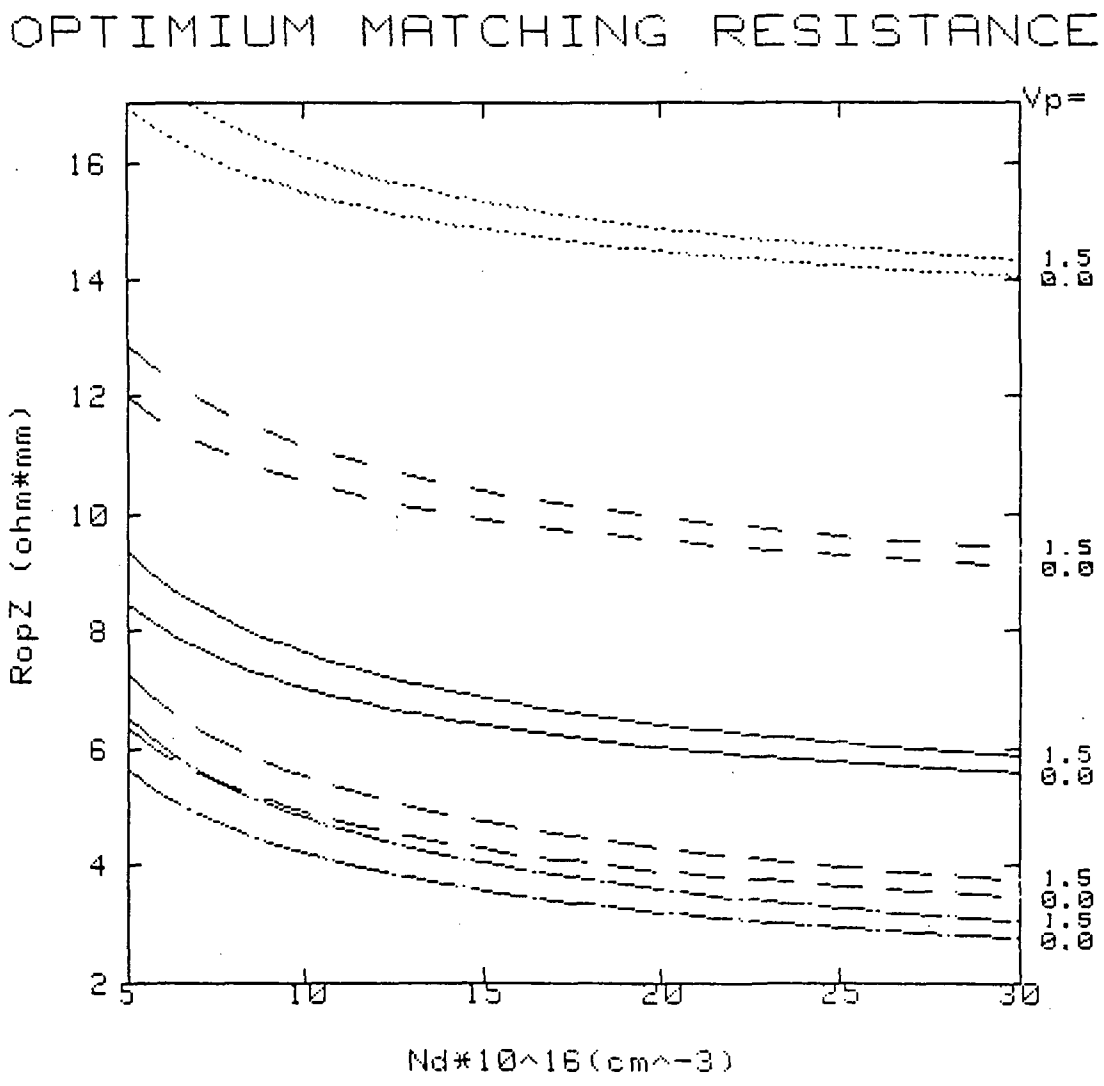


FIGURE 3.5.6, THIS PLOT SHOWS THE GaAS MESFET LNA OPTIMIUM MATCHING RESISTANCE .VS. THE CHANNEL CARRIER CONCENTRATION FOR PINCHOFF VOLTAGES Vg=0 AND 1.5, AND GATE SEGMENT WIDTHS OF Z1=0, 0.05, 0.1, 0.15 AND 0.2 (mm).
Z1= 0(BROKEN SOLID), 0.05(LARGE DASH), 0.1(SOLID) 0.15(SHORT DASH), AND 0.2(DOTTED)

L=0.3(um), h=0.5(um), f=20 GHZ, INDP. OF Z

resistance (first factor) is used to determine the minimum noise figure given by equation (12).

The optimum gate matching reactance times the gate width (XopZ) and resistance times the gate width (RopZ) is given by equation (13) and (14) and plotted in figures 3.5.5 and 3.5.6 respectively. XopZ is simply the negative of the gate reactance, determined by the gate capacitance, while RopZ is determined by the R_gZ, R_sZ and the transconductance g_m/Z. The gate capacitance is given empirically by equation (6) and plotted in figure 3.5.7. The transconductance g_m/Z is given empirically by equation (5), and plotted in figure 3.5.8. The plots of the gate capacitance and transconductance are referred to extensivly during analyses of various devices.

3.5.3 Minimum Noise figure (F_m) The previously discussed expressions for the gate resistance (R_gZ) and the source channel resistance (R_sZ), in terms of the gate width (Z), can be used to find the minimum noise figure (F_m) given by equation (12). This expression is based on empirical analysis. Examination of equation (12) shows Fm increasing nearly linearly with L_g and frequency (f). Therefore, short gate lengths at high frequencies are most important. It can also be seen that F_m increases as $(R_gZ + R_sZ)^{0.5}$, showing the importance of the gate metalization resistance and source channel resistance. It should be noted that as the gate length (L_g) is reduced as the channel resistance (R_sZ) increases. This, again, shows the importance of reducing

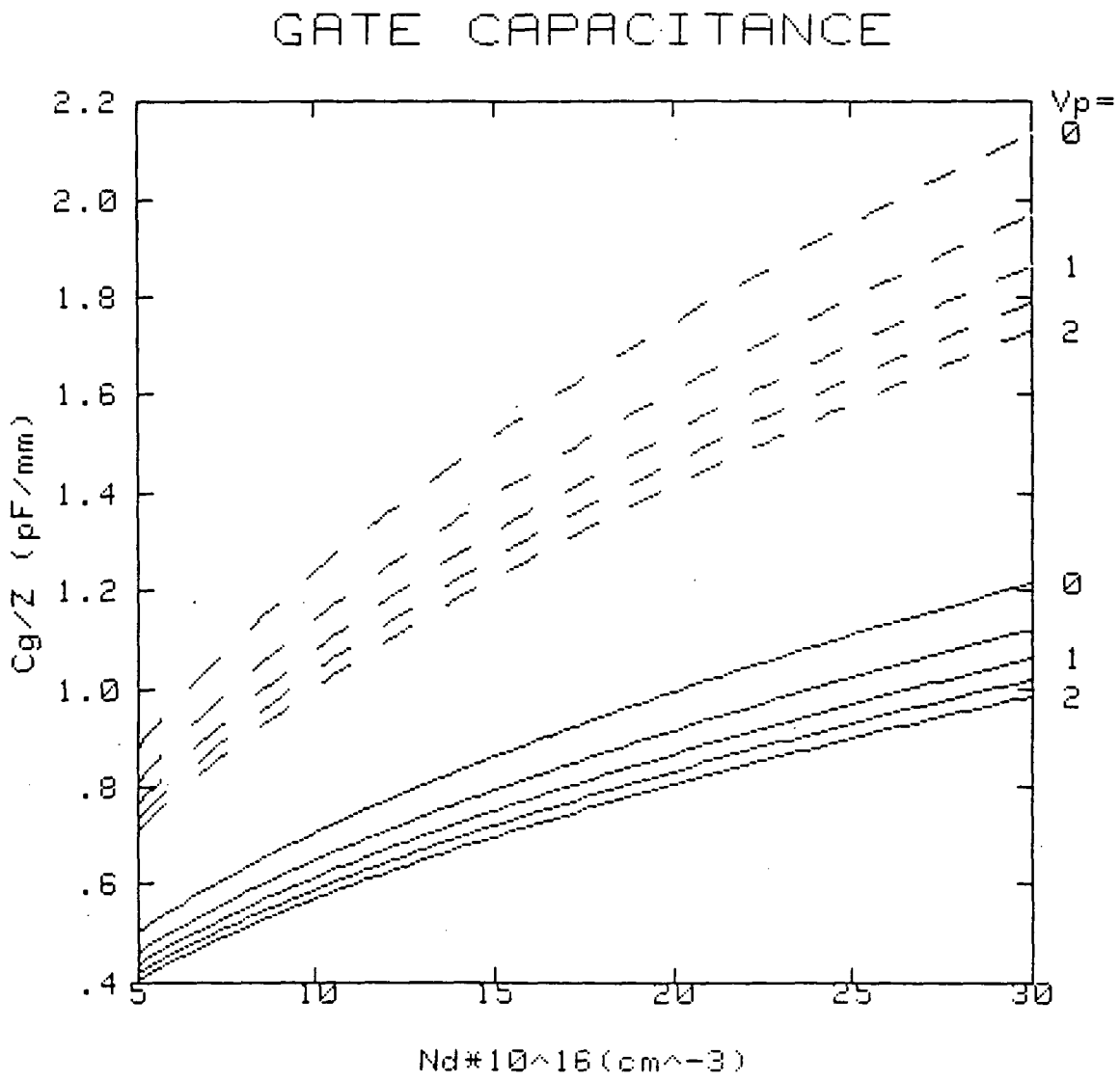


FIGURE 3.5.7, THIS PLOT SHOWS THE RELATIONSHIP BETWEEN THE GaAs MESFET LNA GATE CAPACITANCE (PER UNIT GATE WIDTH (mm)) .VS. THE CARRIER CONCENTRATION, FOR VARIOUS PINCHOFF VOLTAGES.

THE GATE LENGTH Lg=0.3(SOLID LINE), =0.7(DASHED LINE)

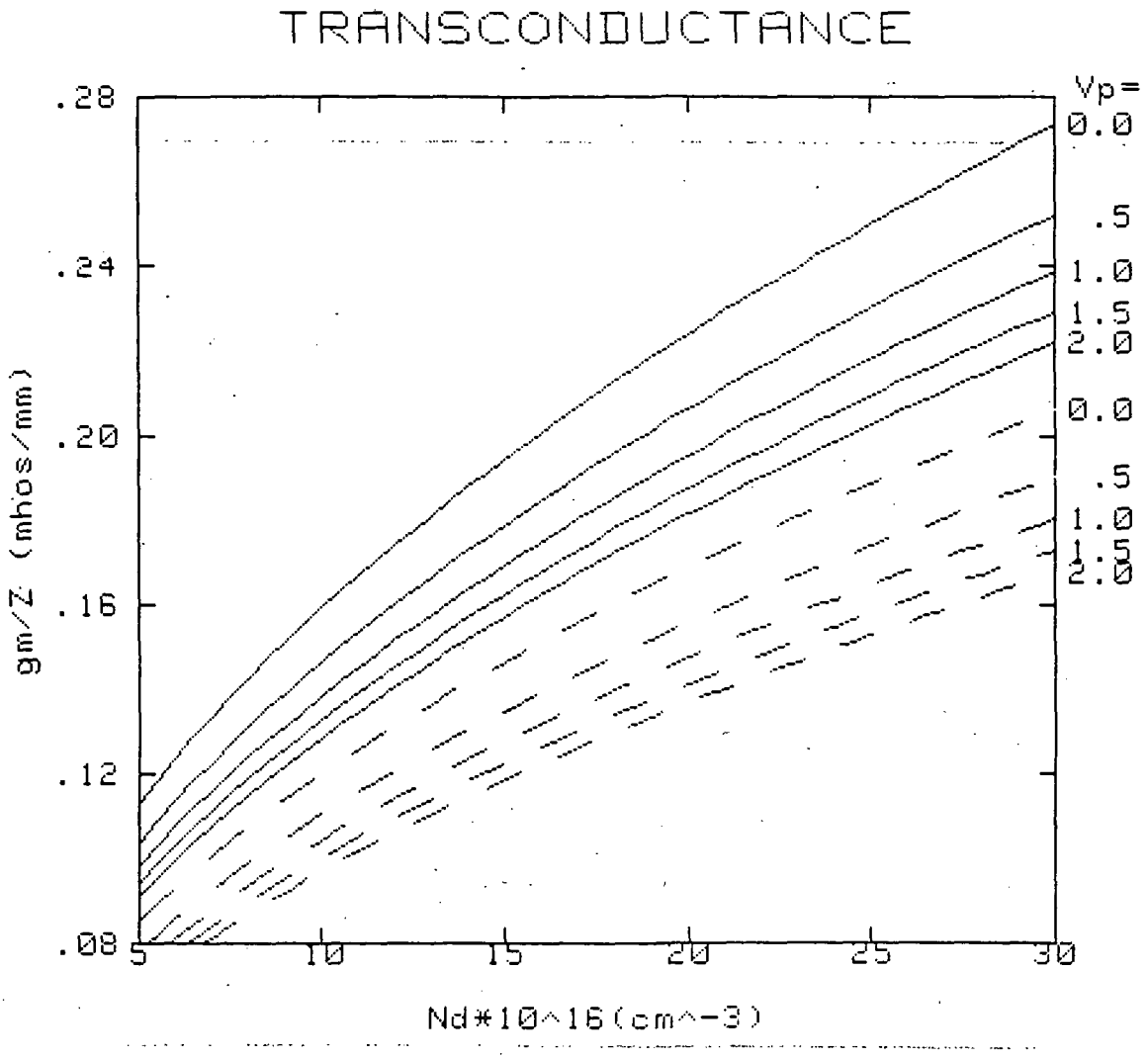


FIGURE 3.5.8, PLOT SHOWS THE RELATIONSHIP BETWEEN THE GaAs MESFET GATE TRANSCONDUCTANCE (PER UNIT GATE WIDTH (mm)) .VS. FOR VARIOUS PINCHOFF VOLTAGES AND GATE LENGTHS 0.3 AND 0.7 um.

GATE LENGTH Lg=0.3um (SOLID LINE), =0.7um (DASHED LINE)

the gate resistance (given by equation (11)) by reducing the gate finger width (Z_1) while increasing the number of gate fingers to maintain the same total gate width (Z).

The dependence of F_m on N_d, V_P, f, and Z_1, is shown in figure 3.5.9.

3.5.4 Minimum Noise Figure Models In order to gain insight into the minimum noise figure analysis, which followed Fukui's empirical analysis, the field independent mobility model and the velocity saturated model for F_m are compared. The velocity saturated model is based on velocity saturated carrier flow in the active channel region whereas the field independent mobility model is base on ohmic carrier flow in the active channel region.

A general expression for F_m is given as

$$F_m = 1 + fL_g(g_m(R_s + R_g))^{1/2}/4 \text{ [30].}$$

The difference between the models for F_m lies in the expression for transconductance (g_m).

For the field independent mobility case we have according to [30],

$g_m = 2Z\mu qN_d/L(y_2 - y_1)$ where V_D, V_g and V_b are the drain, gate and built in voltage.

$$Y_1 = [2\epsilon_s(V_g + V_b)/qN_d]^{0.5} = a[(V_g + V_{bi})/V_P]^{0.5}$$

and

$$Y_2 = [2\epsilon_s(V_P + V_g + V_b)/qN_d]^{0.5}$$
$$= a[(V_D + V_g \text{ to } V_b)/V_P]^{0.5}$$

where we have redefined $V_P = qNda^2/(2\epsilon_s)$

This gives

$$g_m/Z = 2\mu/L_g(2\epsilon_s\ qNd)^{0.5}[(V_d + V_g + V_b^{0.5} - (V_g + V_b)^{0.5}]$$

Evaluating these expressions, inserting them into the expression for F_m and rearranging gives

$$(F_m - 1)/\mu^{0.5} = 0.0866f[N_d^{0.5}L((V_d + V_g + V_b)^{0.5} - (V_g + V_b)^{0.5}(R_sZ + R_gZ)]^{0.5}$$

Notice that the noise figure depends on the drain voltage in the field-independent mobility case. This function is plotted in figure 3.5.10 with $V_d = 0.5\ L_g$. Beyond $V_d = 0.5\ L_g$ velocity saturation begins to onset.

For the velocity-saturated model we have $g_m = v_sZ\epsilon_s/h(V_g)$ [30] where $h(V_g) = 2\epsilon_s/qN_d)(V_g + V_b)^{0.5}$ [30]. Using this in the general expression for F_m and rearranging gives

$$(F_m - 1)/V_s^{0.5} = 0.136fL_g[(R_sZ + R_gZ)/(V_g + V_b)]^{0.5}.$$

In this model there is no dependence on V_d as in the field-independent mobility model, though there is still a dependence on the gate voltage V_g. This function is plotted in figure 3.5.11.

3.5.5 Minimum Noise Figure Graphical Analysis Three expressions for the minimum noise figure have been found and plotted. They are the empirical analysis, field independent mobility model and the velocity-saturated model.

To compare these plots, first consider the point $N_d = 10^{16}cm^{-3}$, $V_p = 0$ and $Z_1 = 0.05$ um in figure 3.5.9 of the empirical analysis. This gives $F_m = 1.47$. In order for

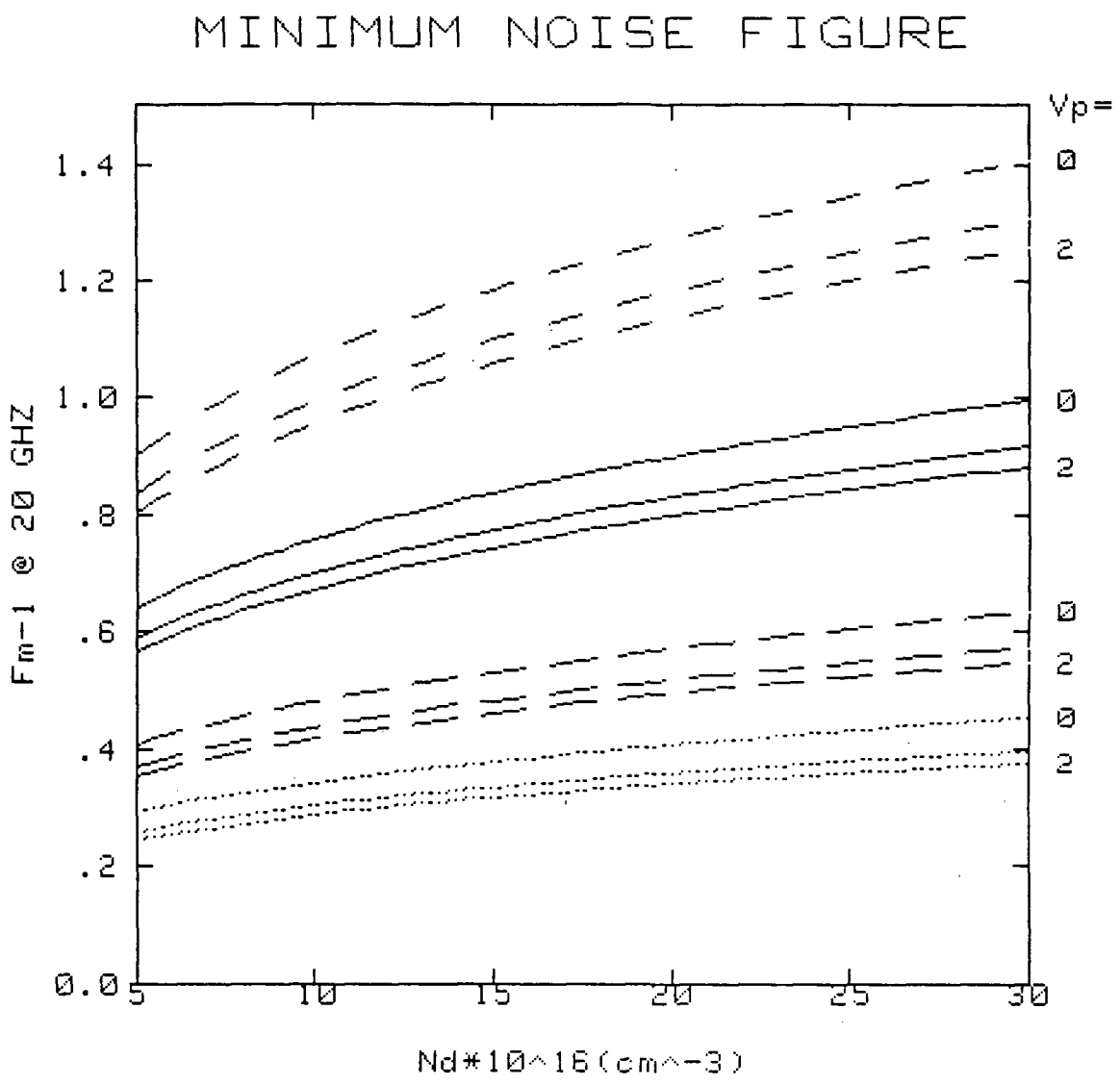


FIGURE 3.5.9, PLOT SHOWS THE GaAS MESFET LNA MINIMIUM NOISE FIGURE -1 .VS. THE CHANNEL CARRIER CONCENTRATION FOR PINCHOFF VOLTAGES Vp=0.0, 1.0 AND 2.0 AND PARALLEL GATE SEGMENT (FINGER) WIDTHS Z1=0.0, 0.05, 0.1, 0.15, AND 0.2 (mm).

Z1= 0(DOTTED),0.05(LARGE DASH), 0.1(SOLID) AND 0.15(SHORT DASH)
L=0.3(um), h=0.5(um), f=20 GHZ, INDEPENDANT. OF Z

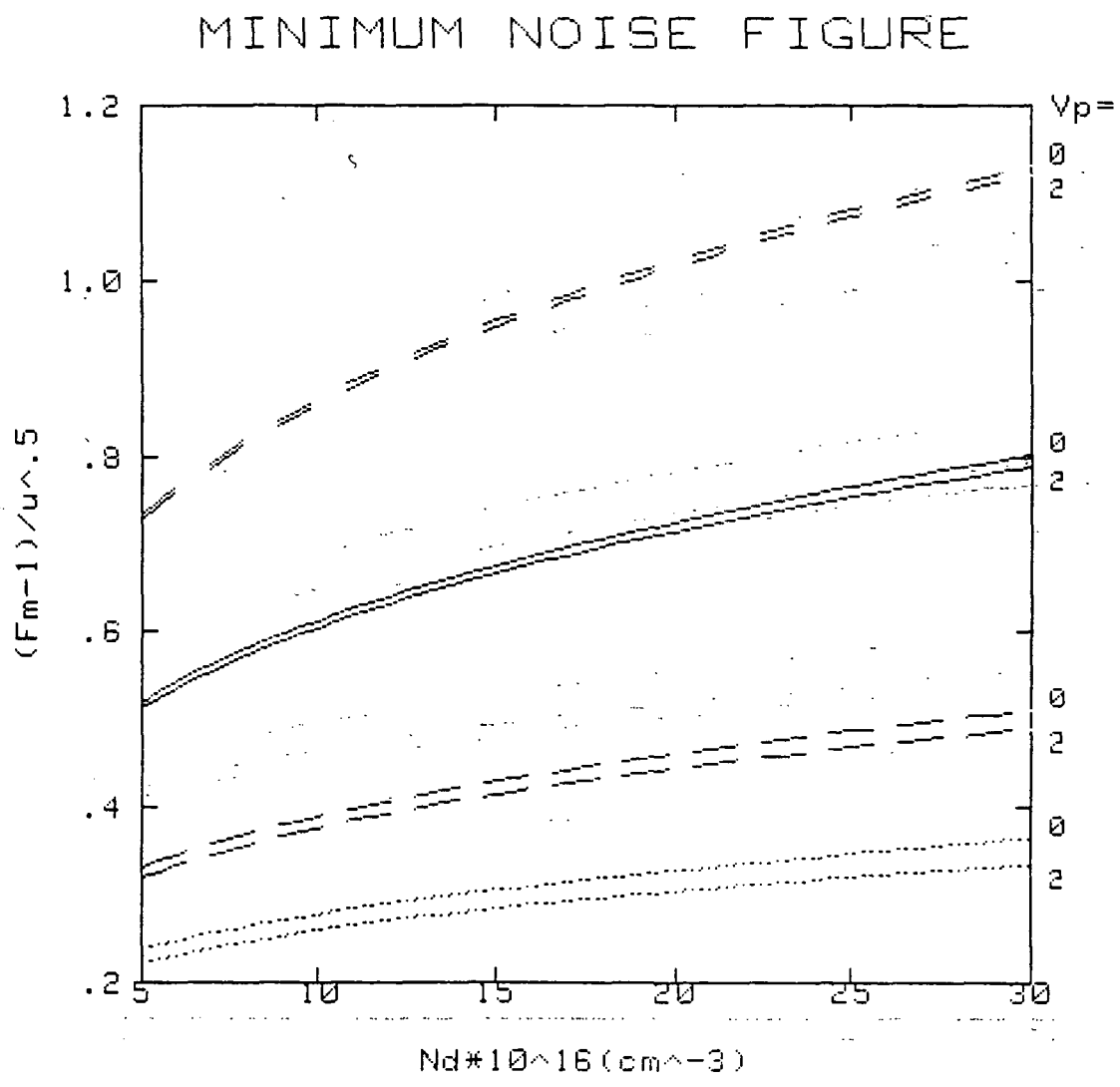


FIGURE 3.5.10, THIS PLOT IS BASED ON THE CONSTANT-MOBILITY MODEL OF THE GaAs MESFET NOISE .vs. THE CARRIER CONCENTRATION FOR PINCHOFF VOLTAGES Vp=0 AND 2.0 VOLTS AND WITH PARALLEL GATE SEGMENT (FINGER) WIDTHS Z1=0.0, 0.05, 0.1 AND 0.15 (mm).

THE NOISE FIGURE IS WEAKLY DEPENDANT ON CARRIER THE NOISE FIGURE IS WEAKLY DEPENDANT ON CARRIER CONCENTRATION BY BY INCREASED TRANSCODUCTANCE WITH INCREASED Nd (FOR A GIVEN Vp) BY INCREASED SOURCE CHANNEL RESISTANCE WITH INCREASED Nd. THE LARGE INCREASE WITH INCREASED GATE FINGER WIDTH IS DUE TO THE INCREASED GATE METALIZATION RESISTANCE.

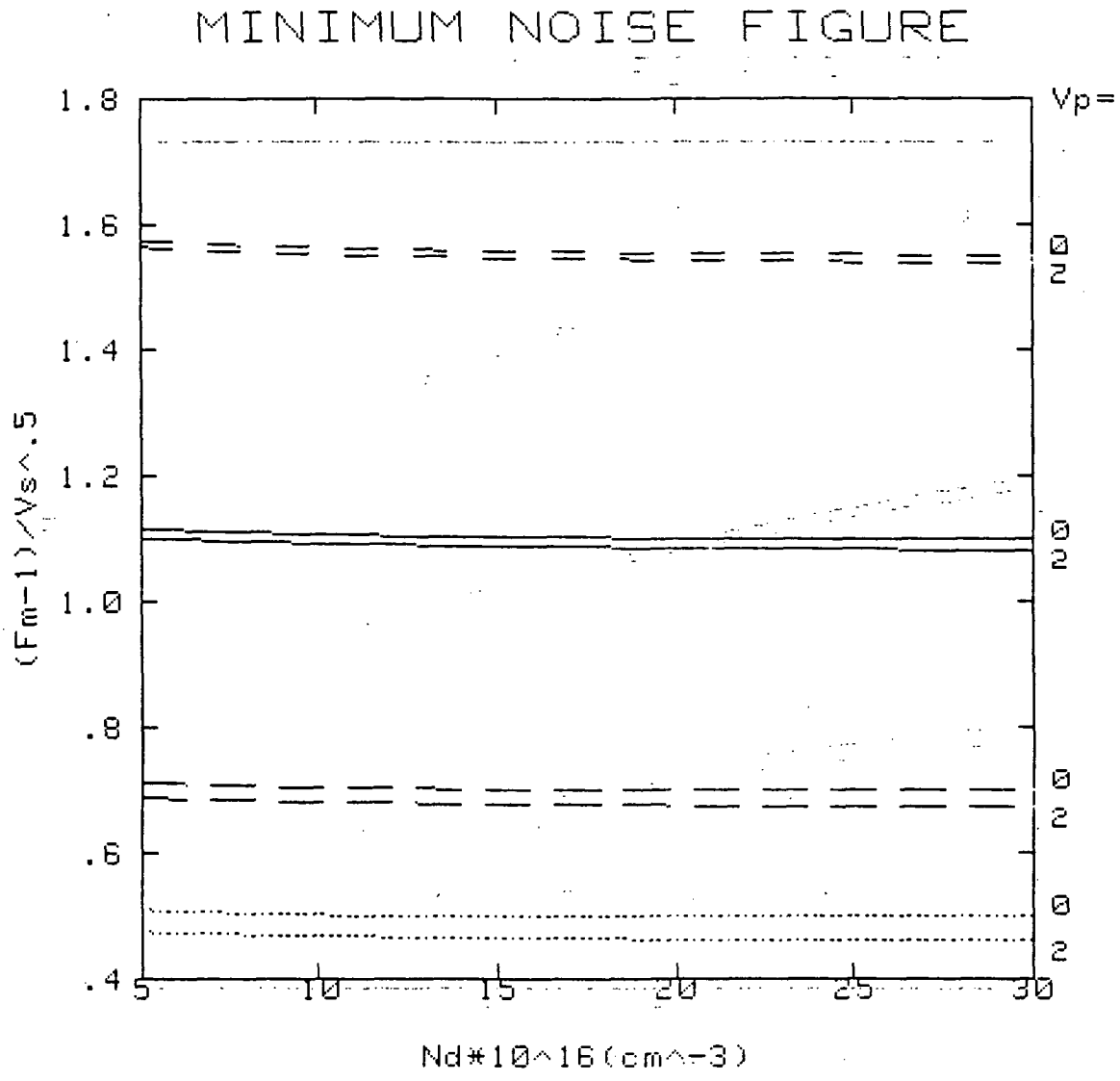


FIGURE 3.5.11, THIS PLOT IS BASED ON THE VELOCITY-SATURATED MODEL OF THE GaAs MESFET NOISE..VS. THE CARRIER CONCENTRATION FOR PINCHOFF VOLTAGES Vp=0, 0.75 AND 1.5, AND PARALLEL GATE SEGMENT (FINGER) WIDTHS Z1=0.0, 0.05, 0.1 AND 0.15 (mm). Z1=0(DOTTED), 0.05(LARGE DASH), 0.1(SOLID), 0.15(SHORT DASH). Vg=0, Vs(10^7cm/s), L=0.3(um), h=0.5(um), f=20 GHZ

THE NOISE FIGURE IS NEARLY INDEPENDANT OF CARRIER CONC. (FOR A GIVEN Vp) AND NEARLY INDEPENDENT OF PINCHOFF VOLTAGE. THE SMALL DEPENDENCE IS DUE TO THE CHANGE IN SOURCE CHANNEL RESISTANCE. THE LARGE INCREASE, WITH INCREASED GATE FINGER WIDTH, IS DUE TO THE INCREASED GATE METALIZATION RESISTANCE.

the other two graphs to have the same value for F_m, u and v_s must be

$$(F_m - 1)/u^{0.5} = 0.39 \text{ --> } u = 1.45 \times 10^3 \text{ cm/s} \quad \text{and}$$

$$(F_m - 1)/v_s^{0.5} = 0.7 \text{ --> } v_s = 0.45 \times 10^7$$

These are reasonable values for both u and v_s. Both would have values 2 to 3 times larger for high quality GaAs.

F_m increases with doping fastest in the velocity saturated model, followed by a slower increase F_m the empirical model, and the slowest increase of F_m occurs for the field independent mobility model. This suggests the Fukui's empirical model describes low-noise FETs as having both saturated-velocity and constant-mobility characteristics. Comparing the shape of the curves, one can conclude that the empirical model more closely resembles the velocity saturated model.

3.5.6 Maximum Available Gain (MAG) The MAG is generally given by

$$MAG = (f_T/f)^2[4/R_{DS}(R_i + R_s + R_g + w_tL/2) + 2w_t(R_i + R_s + 2R_g + 2w + L_s)]^{-1} \quad [2]$$

where f_T is the cutoff frequency given by

$$f_T = v_s/(\pi L_g) \text{ (or } f_T = v_s/(2\pi L_g)$$

for v_s defined as the peak velocity [2] and

$$f_T = uV_D/(2\pi L_g^2),$$

where $V_D/L_g = 5$ kV/cm [2]

for the velocity-saturated model and the field-independent mobility model respectively. To simplify the expression for

MAG we can neglect the source inductance (L_s) [2], and the drain-gate capacitance $C_{dg} = C_{FB} \simeq 1/40\ C_{sg}$ [2]. Also, the changing resistance (R_i) is given by

$$R_i = 0.5\ R_o = 0.5 \times 1.1\ L_g/(N^{0.82}az),$$

where R_o is the open channel resistance [17]. This gives

$$MAG = 0.25\ (f_T/f)^2\ Ron/(R_g + Ron/2 + R_s)$$

$$MAG/v_s^2 = 253/(fL_g)^2\ \ Ron/(R_g + Ron/Z + R_s) \text{ with } V_s \text{ in units of } \times 10^{-7} \text{cm/s and}$$

$$MAG/\mu^2 = 1580/(fL_g)^2\ \ \ Ron/(R_g + Ron/Z + R_s) \text{ with } \mu \text{ in units of } = \mu \times 10^{-4} \text{cm/V}_s$$

for the velocity-saturated model and field-independent mobility model respectively, where L_g is converted to microns and f is converted to GHz. Notice that both models for MAG are very similar and have and equally strong dependence on the saturation velocity and mobility. A plot of MAG/v_s^2 is shown in figure 3.5.12. This plot is equivalent to MAG/μ^2 if multiplied by 6.25. Also, included is a plot for MAG with v_s in units of 10^7 cm/s.

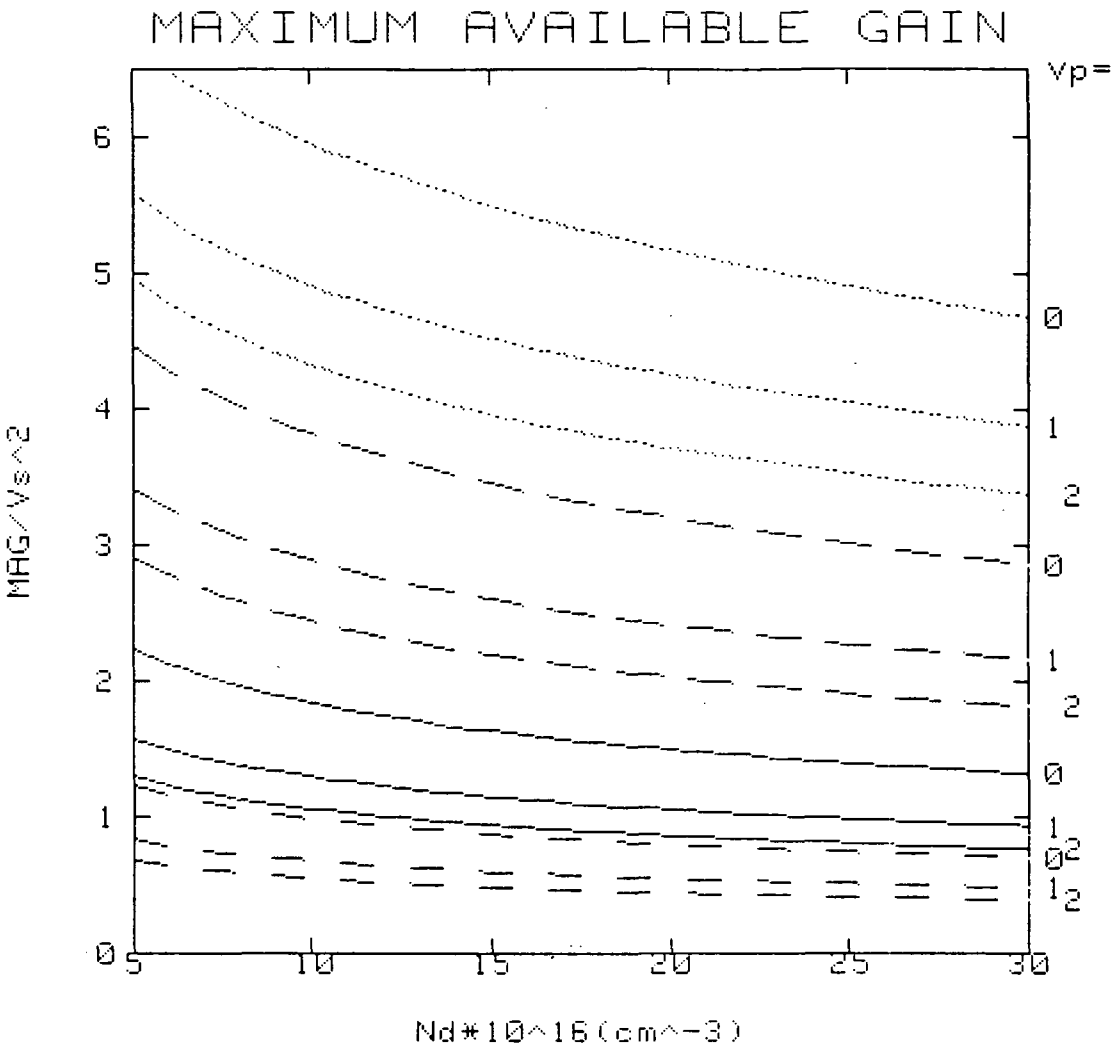


FIGURE 3.5.12 THIS PLOT SHOWS THE GaAS MESFET LNA MAXIMIUM AVAILABLE GAIN .VS. THE CHANNEL CARRIER CONCENTRATION, ASSUMING THAT BOTH THE SOURCE-LEAD INDUCTANCE AND THE DRAIN-GATE FEEDBACK CAPACITANCE ARE SMALL AND NEGLIGABLE, FOR PINCHOFF VOLTAGES Vp=0 1 AND 2, AND GATE SEGMENT FINGER WIDTHS Z1=0.0, 0.05, 0.1 AND 0.15 (mm).

Z1= 0(DOTTED), 0.05(LARGE DASH), 0.1(SOLID) 0.15(SHORT DASH)
Vs*10^7(cm/s), L=0.3(um), h=0.5(um), f=20 GHZ, NO Z DEPENDANCE

THE PLOT IS OF A GaAs MESFET MODEL WITH VELOCITY-SATURATED CARRIER FLOW (Vs), BUT ALSO CAN EQUIVALENTLY SHOW THE MAG/u^2 OF THE CONSTANT-MOBILITY MODEL VIA THE RELATION MAG/Vs^2 = 16*MAG/u^2, u(1000 cm/s).

NOTE THE STRONG DEPENDANCE ON HIGH MOBILITY OR SATURATION VELOCITY FOR HIGH GAIN. THIS INDICATES THE NEED FOR HIGH-QUALITY EPI. VIA GOOD FABRICATION TECHNIQUES, LOW IMPURITY CONCENTRATIONS OR EVEN LOW TEMPERATURES.

THE PLOT SHOWS THE NEED FOR LOW Vp AND WEAKER DEPENDANCE ON LOW DOPING, INDICATING NEED FOR A SHORT CHANNEL HEIGHT.

3.6 GaAs Digital Logic Applications

The QPSK/QASK modulator is operated by digital words of 2 bits length for QPSK and 4 bits length for QASK. With a 0.5 GHz symbol rate the highest speed logic circuits must operate at 2 GBPS. These logic operations are performed by latches, shift registers and dividers which characteristically have clock rates of less than half the speed of their respective gates. This indicates the speed capabilities of the logic elements as one of the limitations of the entire modem's throughput rate.

3.6.1 Latches, Shift Registers and Dividers A survey has been made of the most recent high speed logic functions that are applicable to this modem. The most outstanding results of latches, shift registers or dividers, for each logic type are given and discussed here. Some of the important fabrication technologies and device characteristics are also included to better understand the device requirements and potential for higher performance. Gate diagrams for the various types of flip-flops are shown in figures 3.6.1 through 3.6.4.

Three BFL devices containing flip-flops with clock speeds between 5 and 6 GHz are shown in in references [31], [32] and [33]. In [31] a 600 device, 8:1 parallel-to-serial shift register and timing generator, with control logic, were constructed dissipating less than 2 watts of power. D-type master-slave (M/S) type flip-flops with complementary clocks were constructed because they have higher speeds ($1/2\ t_p$ =

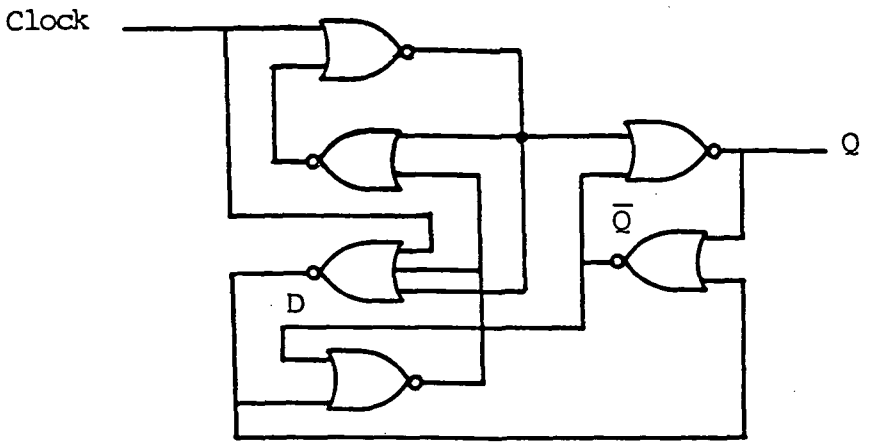


Figure 3.6.1, D Flip-Flop Connected for ÷ 2 Toggle rate = $\frac{1}{5t_d}$

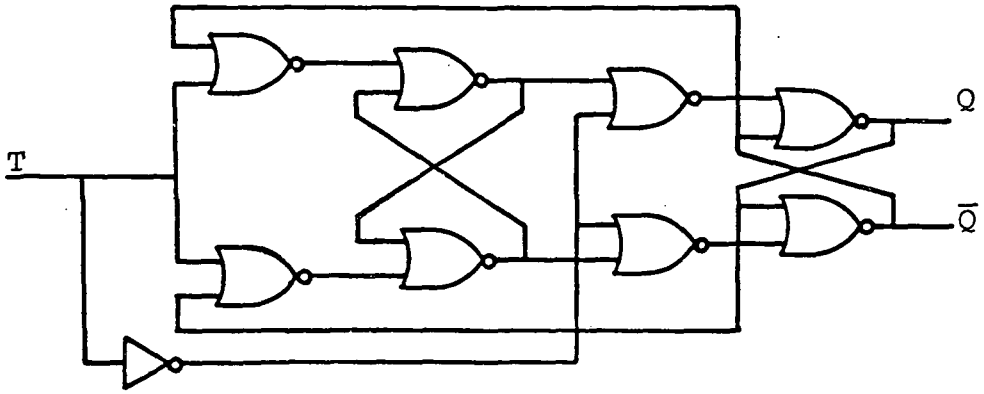


Figure 3.6.2, J K Master-Slave With "T" Connection for ÷ 2

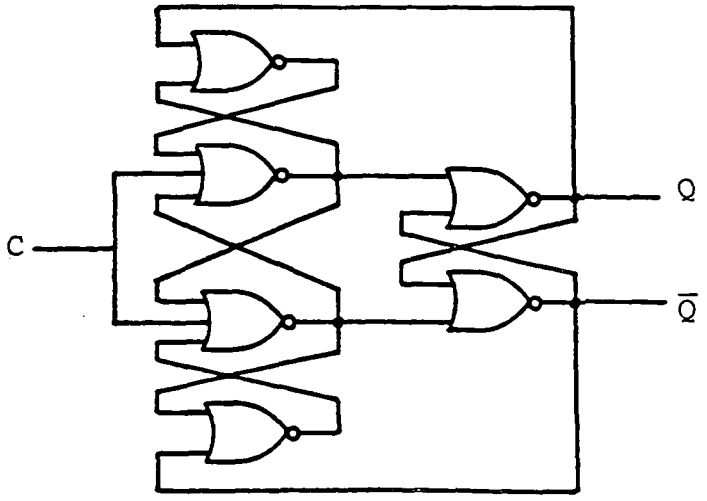


Figure 3.6.3, Edge-Triggered D Flip-Flop Connected for ÷ 2

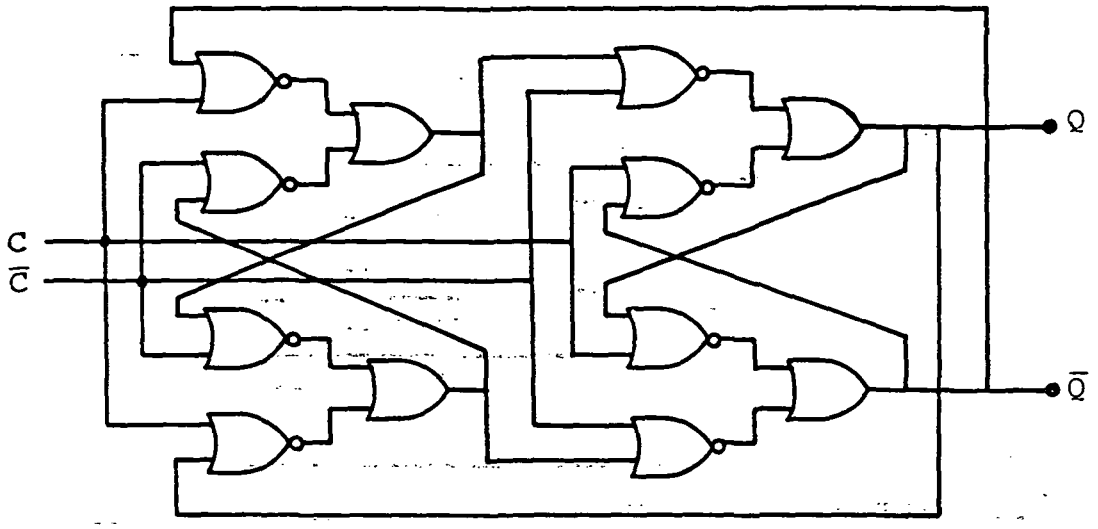


Figure 3.6.4, Dual-clocked RS Master-slave Frequency Divider ($\overline{RSTT}$)
Toggle Rate = 1/2 Td

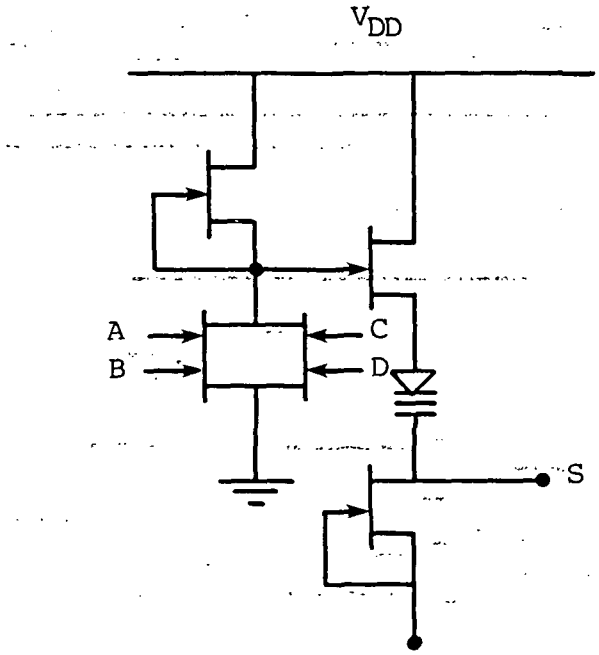


Figure 3.6.5, Circuit Performing the Function

$$S = \overline{A \cdot B + C \cdot D} = \overline{A + B} + \overline{C + D}$$

gate delay) than singly clocked flip-flops. Fabrication techniques include LPE, with a buffer layer, 0.8 um Al gates, N^+ regions using the self-aligned gate technique and 0.25 um channels with $N_d = 2.5 \times 10^{17} cm^{-3}$ giving $V_P = -1.8$ volts.

A binary frequency divider with RSTT (reset-set, single clock) M/S flip-flops with 1/2 T_d clock speeds is shown in [32]. Fabrication techniques include planar, self-aligned gate technology, 5 masks, standard photolithography, 0.6 um Al gate, 2 um source-drain spacing, and $N_d = 2 \times 10^{17} cm^{-3}$ giving $V_P = -2$ volts.

An RST$\bar{T}$ (reset-set) flip-flop using complementary clocks generated by a difference amplifier (for easy interface and increased dynamic range) is shown in [33]. Fabrication techniques include trichloride VPE, recessed gates (by dry etching for tight V_P (-2 volts) control), $N_d = 2 \times 10^{17} cm^{-3}$, 2.4 um source-drain spacing and large 200 um gate widths by direct e-beam lithography.

These three devices have similar clock speeds and comparable gate lengths and pinchoff voltages, yet all three are produced using very different fabrication techniques. The most significant differences comprise the recessed gate with and without N^+ regions and the planar geometry using "SAINT" techniques. These examples show flexibility, in choosing fabrication processes for BFL circuits, which can be generalized for other logic types as well.

An example of a LPFL, is a 2.8 GHz, dual-clocked, nor-gate implemented, RST$\bar{T}$ frequency divider as shown in

[10]. LPFL is chosen over DCFL [10] to improve yields (V_P = -0.2 to +0.2 V). Fabrication techniques include VPE with $N_d = 1.7 \times 10^{17} cm^{-3}$, a buffer layer and 0.75 um Ti/Pt/Au recessed gates by e-beam lithography.

A 1.84 GHz SDFL shift register is fabricated with planar techniques, multiple ion implants into SI GaAs, and 1.0 um gate lengths as shown in [34]. The shift register is constructed with slower, single-clocked, D - flip-flops (clockrate = 1/5 τ_d). A single-clocked flip-flop was chosen in order to avoid the complexity of fabricating a complimentary clock (requiring multilevel logic) and to increase yields. If these same gates are used in a dual-clocked flip-flops, the clock rates would be about 4.5 GHz.

Two cases of nor-gate implemented flip-flops using E-MESFET logic operating at a 3 GHz clock speed are found in [14] and [35]. In both cases fabrication techniques include recessed Al gates with $1.9 \times 10^{17} cm^{-3}$ epitaxial doping. As shown in [14], dual-clocked JKTT M/S flip-flops are used. Some fabrication specifications include V_{DD} = 2 V at 2 GHz, ΔV = 0.35 V, varying gate lengths of 1.0 and 1.2 to 1.4 um, gate widths of 40, 20 and 10 um and loads of 3, 7 and 15 kohms for the faster and slower gates respectively.

In [35] E-MESFET single clock, edge-triggered D-type flip-flops are fabricated with 0.6 um gate lengths, 5.3 kohm loads giving 30 ps gate delays at 1.9 mW/gate. This is an outstanding circuit since the single-clocked

D-flip-flops are about half as fast ($1/5t_d$) as dual-clocked flip-flops. This shows E-MESFET logic circuits with clock speeds equivalent to the highest speed BFL flip-flops.

In conclusion, this survey shows that all of the logic types are capable of producing flip-flops with speeds in excess of the 2 GHz clock speeds required for the QPSK/QASK modem. The survey also implies that either of the two major fabrication classes (self alligned gate or recessed gate) is required to maintain acceptable performances. Implementation of optimized SAINT technology is the basis for much of the analysis throughout this work.

The information presented in this section is the basis of a circuit design for the data processing required for the QPSK/QASK modulator. This circuit is shown in figure 3.6.6.

The QPSK/QASK modulator operates according to a two bit input word for QPSK and a 4 bit input word for QASK. The input words are generated by a serial-to-parallel shift register composed of one of the latch types discussed earlier. These words select the symbol to be transmitted by the modulator and therefore the word should have a duration equal to the required symbol duration. For this reason the shift registers' outputs are latched, for the symbol duration, while the shift register shifts to form the next word. The latch clock is generated from an external clock with a divider for QPSK and a ÷ 4 divider for QASK. Complementry latched output words may be required depending

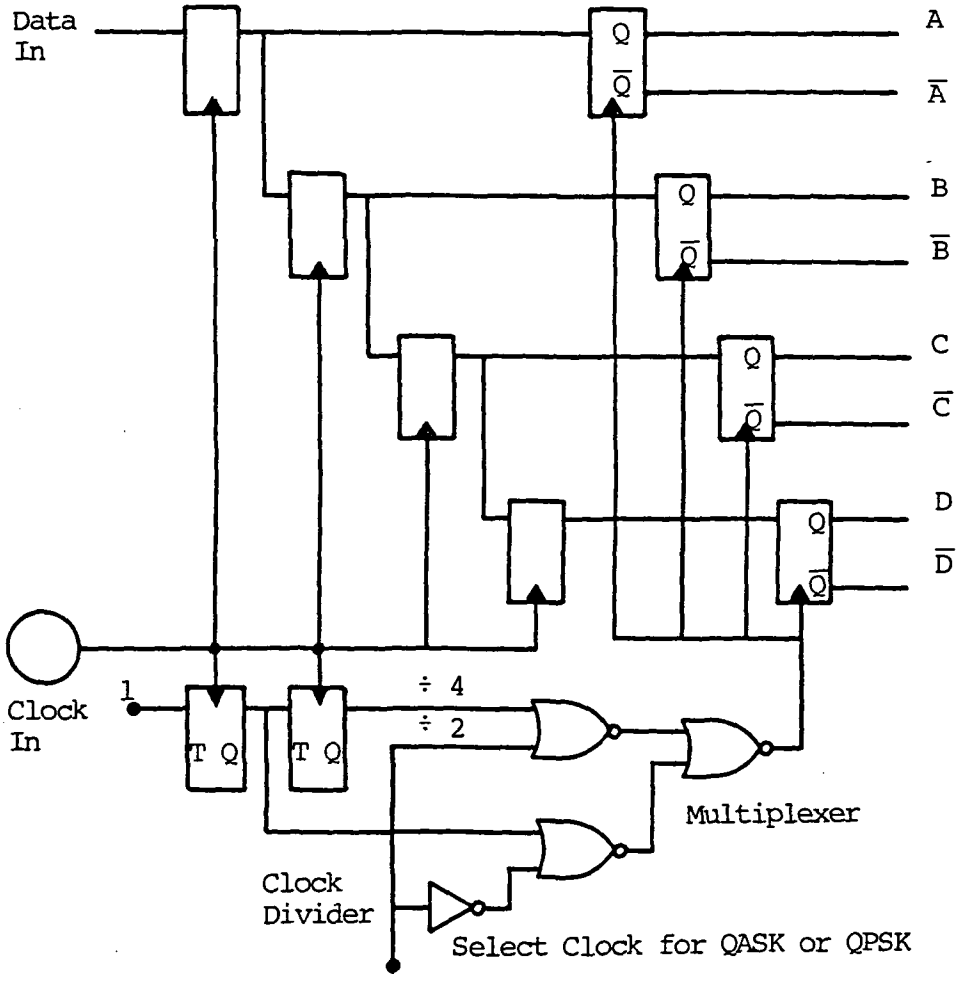


Figure 3.6.6 Serial-to-Parallell Shift Register With Output Latch Select Clock, ÷ 2 for QPSK, ÷ 4 for QASK.

Design Considerations for a Monolithic, GaAs, Dual-Mode, QPSK/QASK, High-Throughput Rate Transiever

A Thesis Presented to the
Faculty of the School of Engineering and Applied Science
University of Virginia

In Partial Fulfillment
of the Requirements of the Degree
Master of Science (Electrical Engineering)

by
Richard A. Kot
May, 1984

on the type of modulator used.

Figure 3.6.6, as drawn, indictes single clock shift register latches. Recall that singly-clocked latches have about half the speed of dual-clocked latches. Since the shift register requires the highest speed logic circuits of the entire modem, dual-clocked latches may be necessary to maintain adequate speeds. A dual-clocked shift register would require the formation of a complementary clock shift register would require the formation of a complementry clock with 180^{o} phase separation. The complementry clock can be formed by splitting the clock signal and inverting. The noninverted clock signal would require a small delay line (other means are possible) to compensate for the propagation delay of the inverting gate and guarantee 180^{o} phase separation.

3.6.2 Decoders Some digital logic applications in the QASK/QPSK modem involve multiplexing/demultiplexing and decoding operations. For all of these gating operations the circuit is represented by standard logic gate symbols, rather than gate breakdown circuit diagrams, because the form of the breakdown depends upon the logic type to be chosen. Throughout this work the functional units (or device types) are designed with consideration for compatability with any logic type. These considerations maintain flexibility in design stratagies for a practical system realization and meet the requirements of the manufacturer. These considerations specify channel characteristics required to meet the

particular speed requirements. It also specifies the output level shifting circuits needed to match the appropriate operation region of the device of concern.

The choice of gate type implementation also depends upon the logic type chosen. One logic type may perform better with a different form of gate breakdown than another logic type when considering propagation delays. For example, nor-gate implementation is usually preferred for SDFL and E/DFL (often unlike BFL) because BFL characteristically has sharper switch-off (pinchoff) capabilities with voltage swings extending beyond V_P. This gives faster and-gate operation on the second (inverting) part of the gate.

3.7 Passive Power Directors

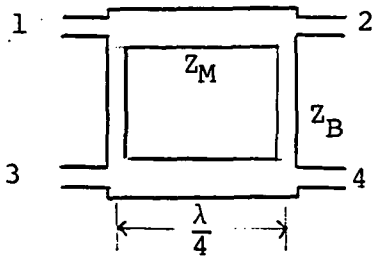
Throughout the RF section of the QPSK/QASK transceiver there is a need for power couplers and combiners with and without phase differences between the two input or output ports. For some devices their reciprocal nature make them equally useful as a coupler or combiner, but at other times this is impractical. For this reason, and because of the function (coupler or combiner) with which they are cited in the literature, they are discussed separately.

3.7.1 Couplers For our modem we need 3 dB power splitters with 90^{o} and 180^{o} relative phase shifts for construction of the QASK signal. Since the symbol rate is 500 MHz, the couplers must have roughly 1 GHz bandwidth. Also, since the signal constellation has very tight tolerances (see table 2.2.1 and 2.2.2) the phase and power splitting/combining must be realized accurately.

From a survey of coupler types, we have the following choices.

1. Broadside coupling
2. Reentrant sections (Backward wave)
3. Tandem sections
4. Branch line couplers (Rat-race, 2-branch line, 3-branch line)
5. Braided structures
6. Interdigitated couplers

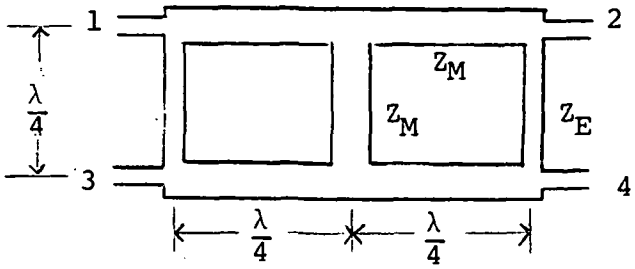
Some of these circuits are shown in figures 3.7.1 through 3.7.6.



$Z_M = Z_o / \sqrt{2}$

$Z_B = Z_o$

Figure 3.7.1, 90° 2-Branch Coupler



$Z_M = Z_o / \sqrt{2}$

$Z_E = Z_o / (\sqrt{2} - 1)$

Figure 3.7.2, 90° 3-Branch Coupler

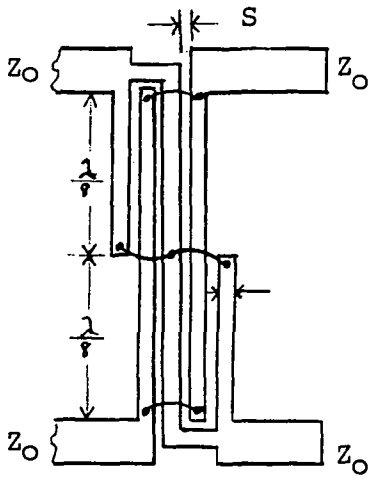


Figure 3.7.3, 90° Interdigitated Coupler

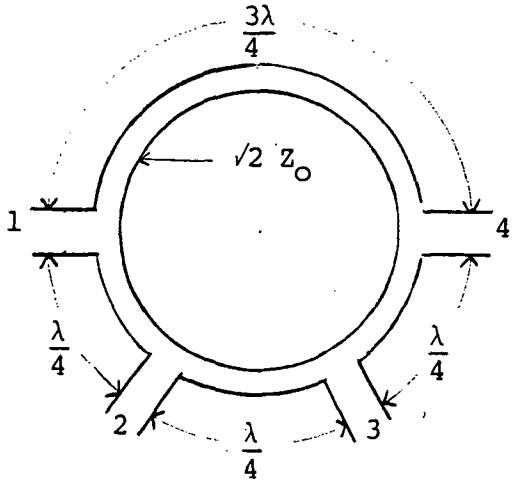


Figure 3.7.4, 180° Rat-Race

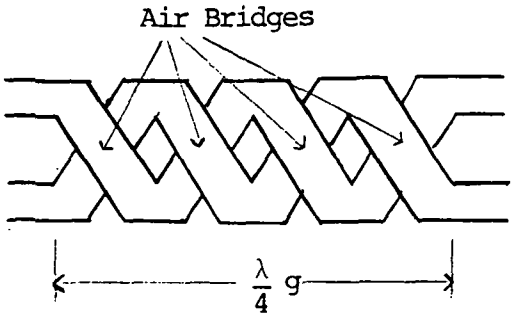


Figure 3.7.5, 90 Braided Coupler

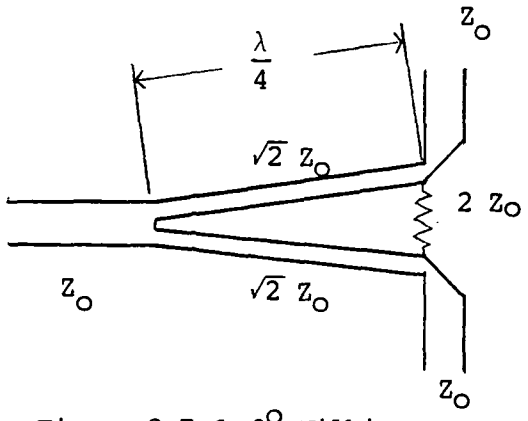


Figure 3.7.6, 0° Wilkinson Coupler

The tight coupling required has been achieved on all but the tandem sections. The 180^{o} reflection coupler has the difficulty in obtaining good open or short circuits [37]. The commercially-available 180^{o} hybrids use tandem connections with broadside coupling which necessitates multilayered structures realized by stripline [37] (3 level) therefore it is not an option for the modem. Reentrant sections [36] and braided structures require multilayer circuitry making them more difficult to realize on monolithic substrates, but two-layer metalization structures (with one of the layers required for interconnects only) will not present a problem since the transceiver IC requires two level metalization circuitry.

For the branch line couplers, including the rat-race, the signal is input at terminal 1 and the output is split equally at ports 2 and 4 with 0^{o} and 90^{o}, and 0^{o} and 180^{o} phase differences respectively. The rat-race has a bandwidth about one third that of the two branch coupler and is much less sensitive to geometric variations because of its dimensional tolerances [38]. Disadvantages of the rat-race, compared to the 2- and 3-branch line couplers are that it has both coupling and phase error with deviation from center frequency [39] (low bandwidth) and the output arms are not adjacent so crossover sections may be needed [38]. The crossover will not present a problem in our IC (as discussed earlier). The net electrical path is $3\lambda/2$ for the rat-race [39] while the net electrical path is λ for

the 2-branch line [39] and 7 $\lambda/4$ for the 3-branch line. However since the line impedances of the rat-race are higher than the 2- and 3-branch line couplers, the required substrate area is close to that of the 2-branch line coupler. The 2-branch coupler has a bandwidth limited to 5-10% since the 90° phase difference and 3 dB coupling occurs only when all the line lengths are 90° [39]. Since more branches give a wider bandwidth but higher loss [38], the 3-branch has a wider BW than the 2-branch but both have comparable sensitivity to parameter variations. The 3-branch couplers' bandwidth (BW) is comparable to the rat-race but has higher loss.

At high frequencies the linewidths become comparable to the $\lambda/4$ line lengths making the point of electrical intersection or junction effects [38] difficult to model [39], but this presents a modeling problem, not an implementation problem for this modem.

Because the rat-race, 2-branch line 3-branch line couplers require large substrate areas and have relatively high frequency dependence (narrow bandwidth) compared to single-section coupled lines [36], they are not as attractive for application in the modem as the tandem, braided and interdigitated structures.

Fabrication tolerances and the need for tight coupling make it very difficult to form the non-interdigitated edge couplers such as the tandem section coupler. Also, the crowding at the line edges result in higher losses

for these non-interdigitated couplers [36]. The tandem or backward wave hybrid coupler is a broadband device having frequency-dependent power division but the phase shift, input match, and directivity are independent of frequency. Its frequency dependence stems from the need for "T" junction connections. The total line length of this coupler is $\lambda_g/4$ [39]. The main difficulty with implementing this structure in the transceiver is the requirement of maintaining close proximity of the coupling lines. This necessitates very high tolerances for proper operation. For this reason this coupler is not as attractive as the braided and interdigitated coupler.

The braided structure (figure 3.7.5) is similar in principle to the 90° interdigitated hybrid structure but requires two level circuitry to form air-bridge interconnects. As an example of the braided structure, Tayima and Platzker in [40] present this structure fabricated on 0.1 mm thick GaAs. The substate's metalization thicknesses are 1 um (bottom) and 3 um (top) with linewidths of 50 um. The losses average 0.5 dB over 8 to 15 GHz with $90 \pm 10^\circ$ phase difference over the same range (a much wider range than is needed for the transceiver). The total coupler length is $\lambda g/4$ and has 3 dB coupling with 7 braided crossings. This structure seems very attractive for the modem because of its wide bandwidth and small substrate area but it does not seem to have an advantage over interdigitated couplers because of its fabrication

complexity and lack of investigation or standardization.

The interdigitated coupler (figure 3.7.3) on microstrip, consists of 3 or more (typically 4) thin parallel quarter-wave length lines with alternate lines tied together making it very suitable for monolithic circuits. It has the advantage of small size, and line separations that are large compared to conventional two-coupled-line devices such as the tandem or broadside couplers. Its bandwidth is very large (approximately one octave) and it can be fabricated with coupling other than 3 dB [41]. There exist a unique set of shapes for which coupling and system impedance are met simultaneously [41]. The 0 dB, 90° interdigitated hybrid has a phase difference independent of frequency although the coupled power is frequency dependent.

A few examples of these couplers are now described. Lange [36] shows a 3 dB 90° hybrid constructed on 0.040 inch alumina, operating in S-band. Here the output ports were balanced to within 0.25 dB over 2.4 to 8.6 GHz, with a 0.13 dB insertion losses (referenced to 50λ) over 2 to 3.9 GHz, 27 dB directivity over the whole band and 25 dB return loss over 2.5 to 4 GHz. The phase difference is less than 2° from 90° between ports.

In [37] a 3 dB hybrid and a 0°-90° tandem hybrid employing interdigitated coupling is presented. This circuit performs with $\pm 7^{\circ}$ phase deviation and 18 dB isolation over 4-8 GHz.

In [42] two interdigitated couplers are fabricated

(apparently on alumina) one with 4.8 dB coupling and the other 3 dB coupling. Both have a 90^{o} phase difference at 15.8 to 16.7 GHz.

In [43] a 180^{o} hybrid, 90^{o}, and 0^{o} tandem interdigitated microstrip coupler and a standard 4-way Wilkinson power combiner were fabricated (apparently on alumina) operating from 1 to 8 GHz. This circuit is shown in figure 3.7.7.

Another example of interdigitated coupling, which is most applicable for the modem, is presented by RCA in [44]. Here a 50 ohm 6 line, a 25 ohm 4 line, and a 25 ohm 6 line coupler were fabricated on 0.1 mm SI GaAs for the 4-8 GHz frequency band. 0.1 um GaAs was chosen for thermal resistance (high power) and circuit loss considerations.

The input and output impedances of power FETs are a few ohms and thus require multi-element matching networks which will consume large substrate areas. Most other FET devices tend to have fairly low impedances too. To help overcome this problem a low impedance (25 ohms) coupler is proposed. This coupler requires less matching and has lower losses (0.5 dB compared to 0.3 dB), over 4-8 GHz, than the 50 ohm coupler. Both couplers have isolation better than 18 dB. The 25 ohm coupler has wider finger widths and, since the finger metal loss is inversely proportional to its width, the loss is lower. These lines consist of 4.5 um Au, while the air-bridge interconnects are 3 um Au. The six-line coupler has the advantage over the four-line coupler of

being able to dissipate more power. (This advantage does not particularly concern us.) The power coupling and phase difference of these couplers are very wideband.

The interdigitated coupler is considered to be the best option for the modem because of its relatively simple structure. It can be easily fabricated along with, or in the same processes as, GaAs ICs without additional fabrication steps, it is very wideband, its phase and power split can be accurately determined, and its design has recently become standard.

3.7.2 Combiners The two monolithic microwave IC power combiners, that are applicable in the transceiver, are the interdigitated hybrid coupler and the Wilkinson power combiner/divider circuit. An example of interdigitated hybrid couplers used as a combiner, divider and as phase shifting elements is given by Gasit and Johnson in [42]. This circuit is shown in figure 3.7.8.

The architecture of figure 3.7.8 shows three independent output phase vectors, each of variable magnitude, (via the variable gain dual-gate FET) generating an output signal of any phase and a wide range of magnitudes (-6 to -28 dB) for any phase. The combiner circuit adds 90^{o} phase to the path which consists of a straight line in the diagram of the hybrid circuit. Both arms are isolated and any power input to these ports will be combined and output at the third port. The maximum gain of these dual-gate FET amplifiers are typically 6 dB $\pm$ 0.5 dB for 15.8 to 16.7 GHz.

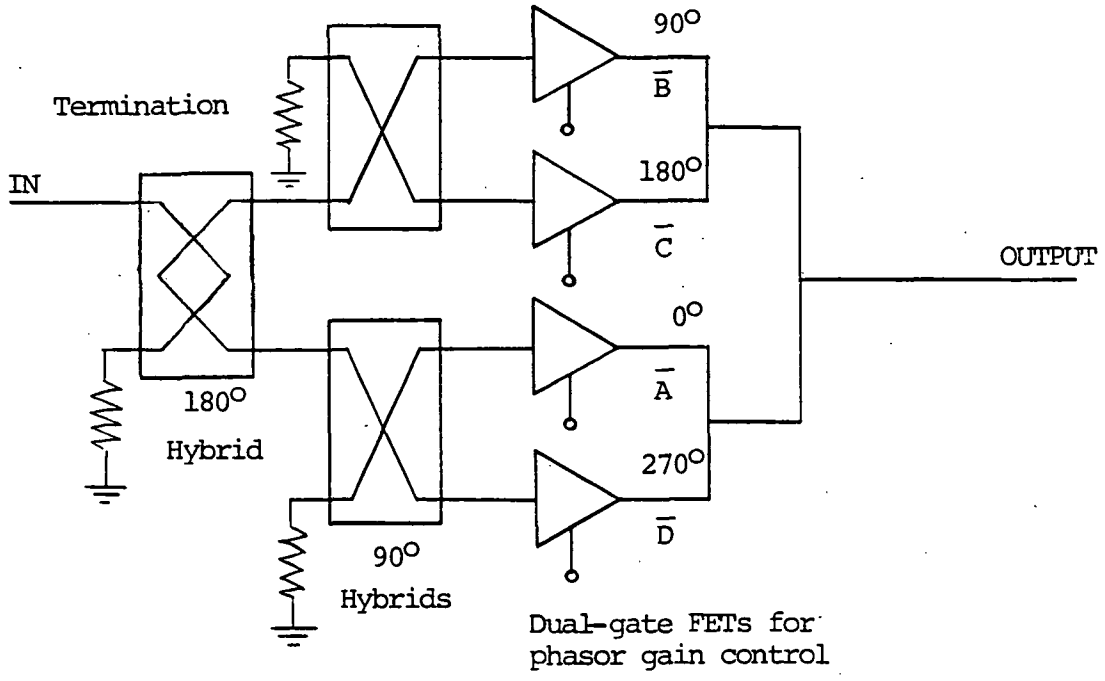


Figure 3.7.7, 360° GaAs Dual-Gate Phase Shifter, after [43]

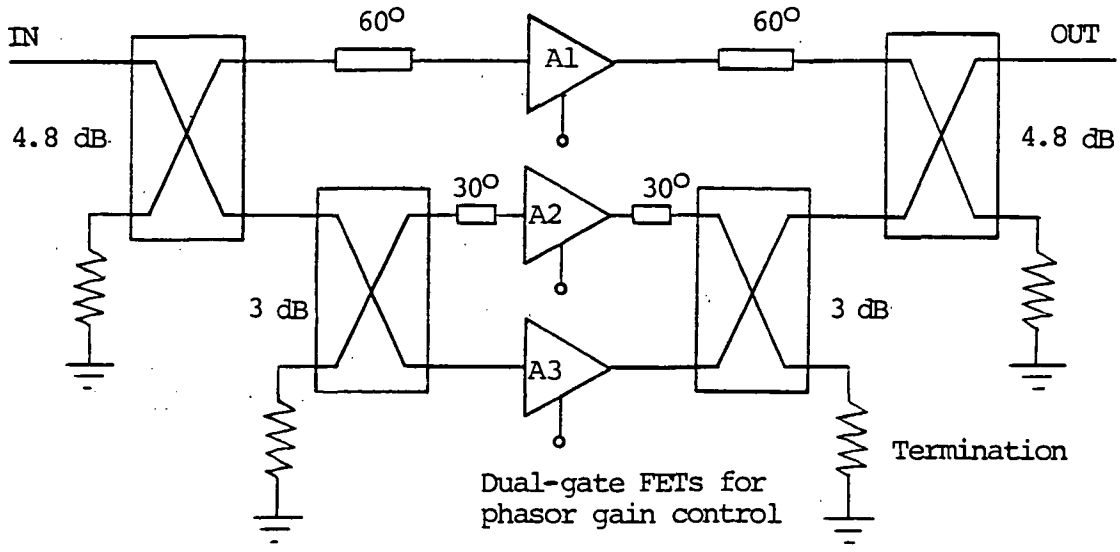


Figure 3.7.8, Continuous Phase and Amplitude Control Circuit
Circuit employs two 4.8 dB interdigitated couplers, two 3 dB quadrature interdigitated couplers, additional line lengths and three dual-gate FETs.
after [42]

The phasor amplitude is controlled by varying the voltage on the gain control gate over a 0 to -3 volt range.

The Wilkinson power combiner/divider has been used by Raytheon [45] on GaAs and by RCA [43] on alumina, with monolithic GaAs IC compatability.

The 4-way Wilkinson in-phase combiner and the phase modulator circuit in which it is implemented is shown in figure 3.7.7. The Wilkinson combiner/divider has been shown in figure 3.7.6 in the section on power combiners. A modified form of the Wilkinson combiner is the "compensated in-line combiner" which characteristically has a more frequency independent input VSWR than the uncompensated form. For a 50 ohm system, this circuit consists of the uncompensated form with the quarter-wave branch arms changed to 59.4 ohms and the circuit preceeded by a 42 ohm quarter-wave transformer. This coupler's higher bandwidth is not useful here and it requires too much substate area to be used in the transceiver.

The Wilkinson divider/combiner circuit has equal, in-phase division/combining over a wideband. Its ports are isolated and matched and the power is split equally because of the circuit symmetry. Port isolation occurs because any field that occurs on either arm will be seen by the other arm via two routes, the 100 ohm resistor and the two 70.7 ohm $\lambda/4$ sections. Both paths can be shown to split the magnitude of the field equally but with a 180^{o} path difference, therefore the fields will interfere

destructively at the second arm, essentially isolating that arm. Power input at either arm will both be coupled or combined at the bottom of the "T".

The quarter-wave structures have an impedance $Z = \sqrt{2Z_o}$ (thin lines) while the resistor has the resistance $2Z_o$ where Z_o is the characteristic line impedance of all the ports.

In comparing the interdigitated hybrid circuit to the Wilkinson circuit we note that both have the qualities of low loss, high isolation and wide-band performance and meet the performance requirements of the QPSK/QASK modem. An important disadvantage of the interdigitated circuit is that it requires a matched termination on one of the ports. This termination can be realized by a 50 ohm epitaxial resistor followed by short to the ground plane through a via hole. The formation of the via hole will increase the complexity of the fabrication processes and thus is not attractive. Another type of matched termination could be achieved by having a ground plane, on the top surface of the substrate, to which the 50 ohm resistor can be routed. If many connections to the top surface ground are required, it may be difficult to maintain wide, continuous metalization that will give a low enough impedance to act as a virtual ground. A long 1 λ lossy line could also achieve a matched termination but would require a large substrate area.

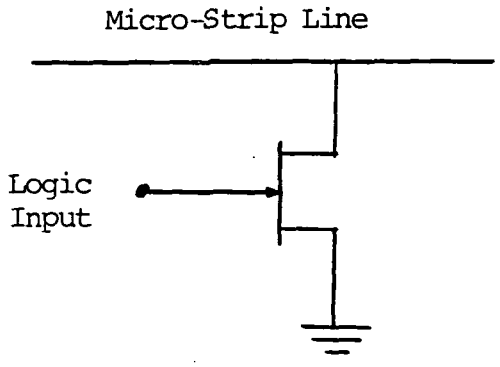
The Wilkinson circuit does not require a matched termination but does require two quarter-wave lines,

separated so as to not couple to each other, as compared to one quarter-wave structure for the interdigitated circuit. It should be noted that the width of the interdigitated circuit has a width slightly larger than that of the low, characteristic line impedance (see [41]), while the Wilkinson circuit will be about 1.5 to 2 linewidths wide since the two quarter wave lines are of higher impedance, thus thinner, and require only a small fraction of a linewidth separation. Therefore the substrate area required for the Wilkinson and interdigitated coupler are not very different, with the Wilkinson coupler using only roughly 1.5 times as much area.

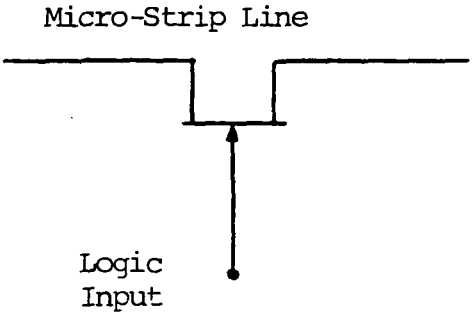
3.8 Phase Shifting

There are many methods of phase shifting only a few of which are applicable to the modem. These methods are described here.

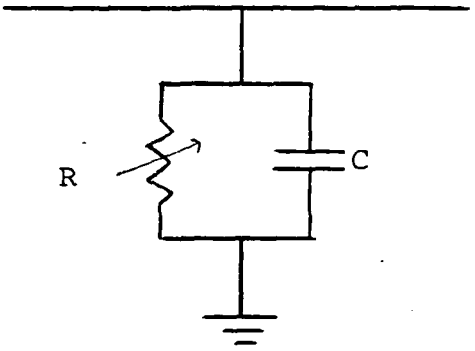
3.8.1 Phase Shifting with Line Switching FETs (Resonated) The resonated FET switch can be used to select (i.e. switch on or off) various signals on different lines similarly to the way dual-gate FETs are used as line switches. The switch can be used in series or parallel configurations as shown in figures 3.8.1 and 3.8.2. By connecting the drain to the line and source to the ground, the parallel-resonated GaAs FET switch shorts the transmission line to ground to "turn off" the line. This switch has shown an "on" state insertion loss (-0.7 dB), high isolation (-28 dB) at 10.2 GHz, and bidirectionality through Ku band (12.4 to 18 GHz) and is compatible with GaAs IC techniques [46]. In the series configuration the source and drain are in series with the line. The line is turned on or off by effectively breaking or closing the line with the FET. This switch is limited by the "on" state low channel series resistance (giving insertion loss) and the "off" state high channel resistance and source–drain capacitance (giving decreased isolation). In the parallel configuration the limitations are similar except the "on" state degradation gives decreased isolation while the "off" state degradation gives insertion loss. Generally the parallel switch would be preferred since it has higher



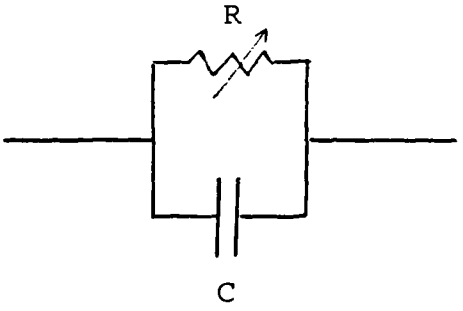
Shunt FET Switch



Series FET Switch



Equivalent Circuit



Equivalent Circuit

Figure 3.8.1,

Shunt FET Switch
when logic input is high,
the MS line is shorted

Figure 3.8.2,

Series FET Switch
When logic input is
low the MS line is
open circuited

isolation than the series switch.

In [46] a rather comprehensive discussion is given for the performance of these switches. Performance plots are given for 10 GHz frequencies, limitating factors are discussed, and examples of matching are given.

The degradation due to drain-source capacitance (C_{ds}) can be resonated out with an inductor across the source-drain capacitance. This inductor can be of the form of a short section of high impedance transmission line [46]. For this device to perform well it is clear that the FET should be designed with a very low "on" state source-drain channel resistance. Unfortunately this will increase the Q of the resonant circuit, thereby lowering the bandwidth.

$$Q = [(R_s(R_s + R_c))^{0.5}wC]^{-1}$$

where $C = C_{SG} + C_{DG}/C_{SG} + C_{DG}$ [47]. This way

$$Q = 1/wCR_s(R_s + R_c)^{0.5} \text{ where } C = C_{SG} + C_{DG}/C_{SG} + C_{DG}$$

To increase isolation, one should also minimize the undepleted channel resistance (increase gate source voltage) and minimize C_{ds}. The parallel switch can be used in place of the dual-gate FET switches in the QASK modulator. The advantage of this would be the increased likelihood of achieving consistent amplitudes on each line of different phase. This is because the gain of the dual-gate FET is very sensitive to slight variation in geometry and channel characteristics (possibly from fabrication tolerance limitations) whereas slight physical differences between FETs serving as loads would cause only slight impedance

variations. Impedance differences of a factor of 1.5 to 2 (for the "on" state) would be needed to cause line amplitude discrepancies. This would correspond to gross FET device differences i.e. an error factor of 1.5 to 2 in gate width.

Another phase modulator scheme is presented by Raytheon in [48]. Here, a monolithic four bit phase shifter is realized using both the "loaded-line" technique (for the 22.5 and 45^{o} bits) and the switched-line technique (for the 90^{o} and 180^{o} bits), where all four phase changing sections are connected in series.

In the loaded-line configurations the signal phase on the main line is a function of the load on the line. The load consists of FETs with transformed impedances and appear as lumped elements on the main microstrip line. If the two load-state impedances are transformed to give the same magnitude of admittance, then the VSWR (and insertion losses) can be made constant for the two phase states. For the 90^{o} and 180^{o} phase bits the switched-line technique is used and therefore its output phase is proportional to the frequency. Such a large phase shift (90^{o} or 180^{o}) would require large loading differences with the loaded-line technique. High VSWRs would result if few loads were used. So, many loads (thus large areas), distributed along the microstrip line would be required to achieve constant insertion loss between the two phase states. In the switched-line technique the shorter line is made with a higher impedance (more loss) than the longer line so that

each line will have roughly the same insertion loss. The line with FETs in the "off" state is the signal path. The insertion loss, due to the finite conductivity of the "on" transistor and the finite resistivity of the "off" transistor, must be considered as contributors to the total loss. The RF signal path can be considered passive and reciprocal.

3.8.2 Phase Shifting with Dual-Gate FETs The principle behind this method of phase shifting is to use the first gate of a dual-gate FET amplifier in series with each signal (phasor) followed by a circuit which sums all of the amplified output phasors. The second gate of the dual-gate FET amplifier is used to swich the amplifier on (high), giving it gain capability, or off (low) giving the amplifier very high loss. Some examples are given and details are discussed here.

The continuously variable Ku-Band phase/amplitude control module presented by Gazit and Johnson [42] employs three dual-gate FETs. The FETs are equally coupled to an input signal via three 90^{o} interdigitated couplers with 4.8 and 3 dB coupling and additional line lengths of 30^{o} for each coupler, giving 240^{o}, 120^{o} and 0^{o} phasors. These three phasors (signals) are then equally summed with 3 and 4.8 dB couplers. Varying the second gate voltage of the dual-gate FET allows variation of the amplitude of each of the phasors, which when summed together, can give the full range of phases 0 to 360^{o} which is more than needed for this

modem. The circuit diagram has already been shown in figure 3.7.8.

The difficulty with employing this type of phase modulator, when discrete phases are desired, is due to the need to precisely control the gain of each FET to insure no amplitude variations between various phases. For discrete phase modulation, say QPSK, this circuit might be modified so as to use four dual-gate FETs of 0^{o}, 90^{o}, 180^{o}, and 270^{o} independently switched and summed together. Then the control gates can be used to completely shut off all but the signal with the desired phase. The phase/amplitude performance of this type of modulator would be determined by the insertion loss (gain) equality and isolation equality of the dual-gate FETs.

A similar concept to the one just mentioned is realized for a continuously variable phase/amplitude module reported by Kumar, Menna and Auang in [43]. Here the signal is divided equally into four parts by a 180^{o} interdigitated coupler and two 90^{0} interdigitated hybrid couplers giving 0^{o}, 90^{o}, 180^{o} and 270^{o} phasors. Each signal is applied to two dual-gate FETs ($V_{p} = -4$) serving as variable gain amplifiers. The outputs of each are summed to form the desired signal. By varying the voltage on the amplitude control gate, any output phase, over a wide range of amplitudes, can be achieved similarly to the device described previously. The circuit diagram is shown in figure 3.7.7.

If this device is used as a discrete-phase modulator, say QPSK, it should perform well since in the "on" state (V_{g2} = 0) the FET has approximately 11 dB gain for 4-8 GHz and in the "off" state (V_{g2} = -3) it has roughly -20 dB isolation for 4-8 GHz. That is, the signal of interest is roughly 31 dB higher than the others. The two highly attenuated (switched off) signals, with phases orthogonal to the signal of interest, will add together destructively, essentially generating better isolation. The highly attenuated signal of antipodal phase will add destructively to the signal of interest causing a negligible decrease in its amplitude. Recall that each dual-gate FET must have equal gain if the circuit can be made to perform similarly at 20 and 30 GHz (as is likely with optimized FETs). This circuit is a likely candidate for QPSK/QASK modulation.

Another form of phase modulator is reported by Upadhyayula, Curtice and Smith [49]. This device employs a balanced multiplier circuit consisting of dual-gate FETs operating in the switching mode. The entire binary phase-shift keying (BPSK) modulator is shown in figure 3.8.3.

For BPSK it is required that the LO signal switch the polarity of the RF signal without changing its amplitude. This is accomplished by turning one pair of transistors off and the other pair on by applying a large LO signal to drive the FETs into the switching mode. The two

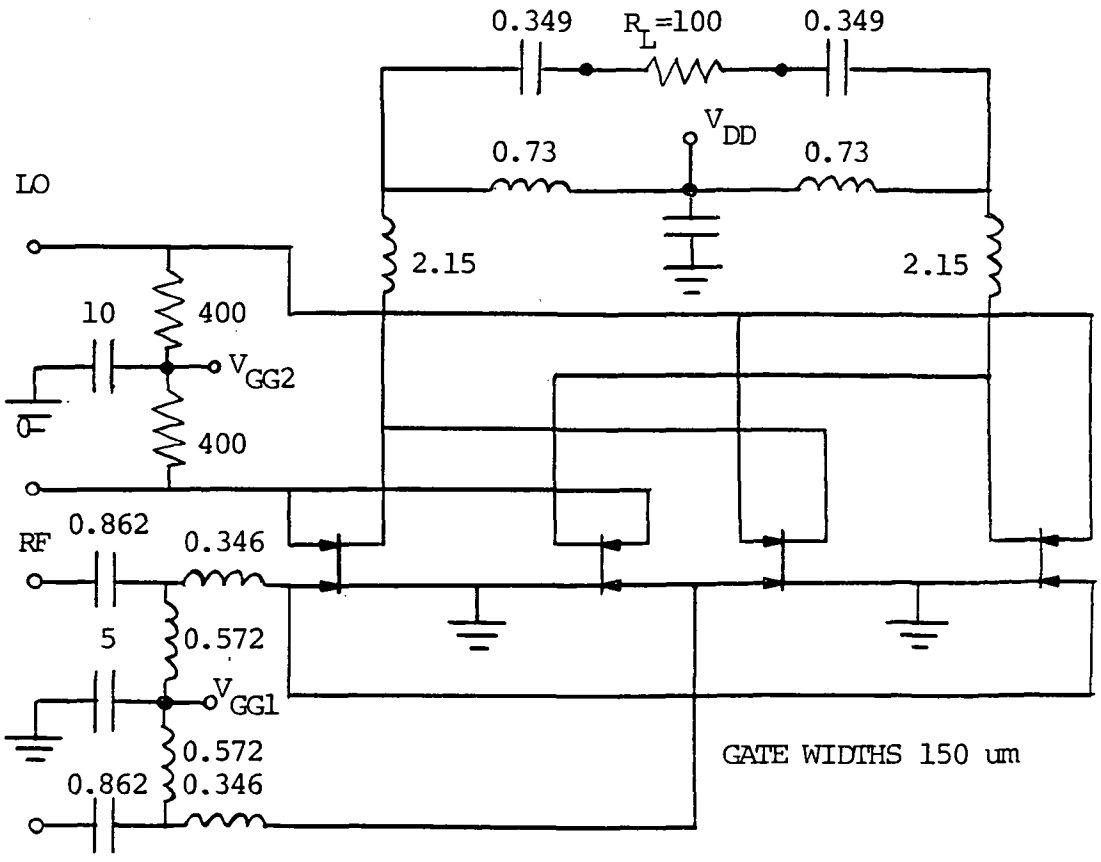


Figure 3.8.3, X-band BPSK Modulator, After [49]
Units of ohms, nH. and pF.

different states give output signals of 180^{o} phase difference.

It is useful to note how this circuit can be modified to serve as a doubly-balanced analog multiplier. When the heart of this BPSK modulator is operated at below the switching mode levels it essentially acts as a multiplier. This circuit is shown in figure 3.8.4.

At X-band this wide band circuit has less than 10 dB insertion loss and 40 dB carrier suppression.

The transconductance of the first gate is designed to be a linear function of the second gate voltage thereby producing a multiplication of the two input signals. With the four dual-gate FET configuration, only the product of the two differential inputs is transmitted, eliminating the need for filtering elements which consumes large substate areas. For example, if differential input is zero, then the second gate input applied to all four transistors is the same. Thus when the RF signal is applied the magnitude and polarity of I_1 and I_4 are the same but since these currents are applied to opposite sides of the output load (Z_L), no current can flow. The same argument holds for I_2 and I_3 and for the case where the input is at the LO port and no signal at the RF port. This circuit is a very compact, high speed and efficient multiplier and apparently, a very practical circuit for use in the modem. More performance and fabrication details can be found in [49].

Fabrication techniques include selective ion

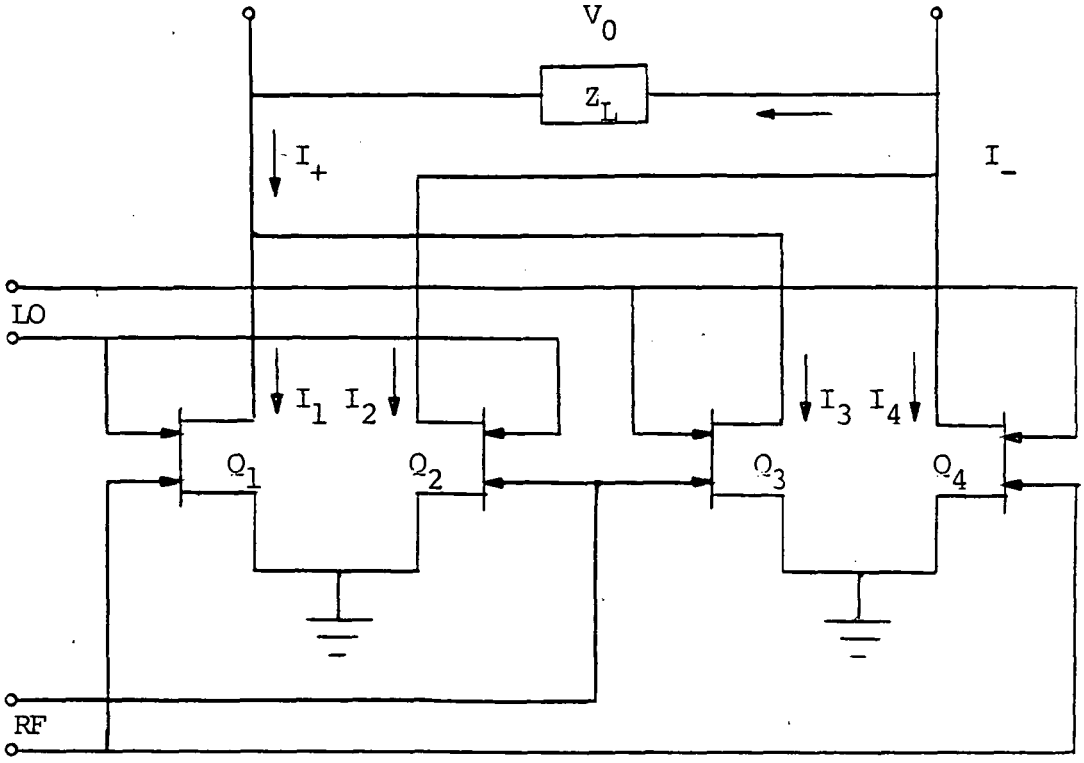


Figure 3.8.4, Dual-Gate Balanced Analog Multiplier.
After [49]

implantation through plasma deposited Si_3N_4 for the FET channels, 10 um thick AuGeNi on N^+ contact regions in SI GaAs, annealing with SiO_2 encapsulation and double resist liftoff.

4 QPSK/QASK Modulators

In figures 4.0.1, 4.0.2 and 4.0.3, three different ways of implementing the QPSK/QASK modulator are shown employing $90^{o}/180^{o}$ interdigitated hybrid couplers (rectangles) and/or Wilkinson combiner/divider (circles) circuits. The dashed lines represent the points at which the switching circuits must be introduced. In the case where dual-gate FET amplifiers are used as the switching elements, it should be understood that the RF gate input and the FET output will require matching circuitry, in the form of two quarter wave transformers and/or lumped elements, for each of the eight FETs. The matched terminations required on the fourth port of the interdigitated hybrid couplers are not shown, nor is the resistor between the two input/output ports of the Wilkinson combiner circuit. Aside from spatial factors, a primary consideration with regard to the performance of these configurations is the attainability of equal (matched) gain in all of the dual-gate FETs. This is necessary for proper signal constellation construction and therefore may require switch-gate bias ports for adjusting the gain of each dual-gate FET.

At the bottom of figures 4.0.1 through 4.0.3 are listed the number of couplers of each type, the approximate total circuit path length (neglecting interconnects and matching) and the approximate substrate area required, at 20 GHz on a 100 um thick SI GaAs substrate. The determination

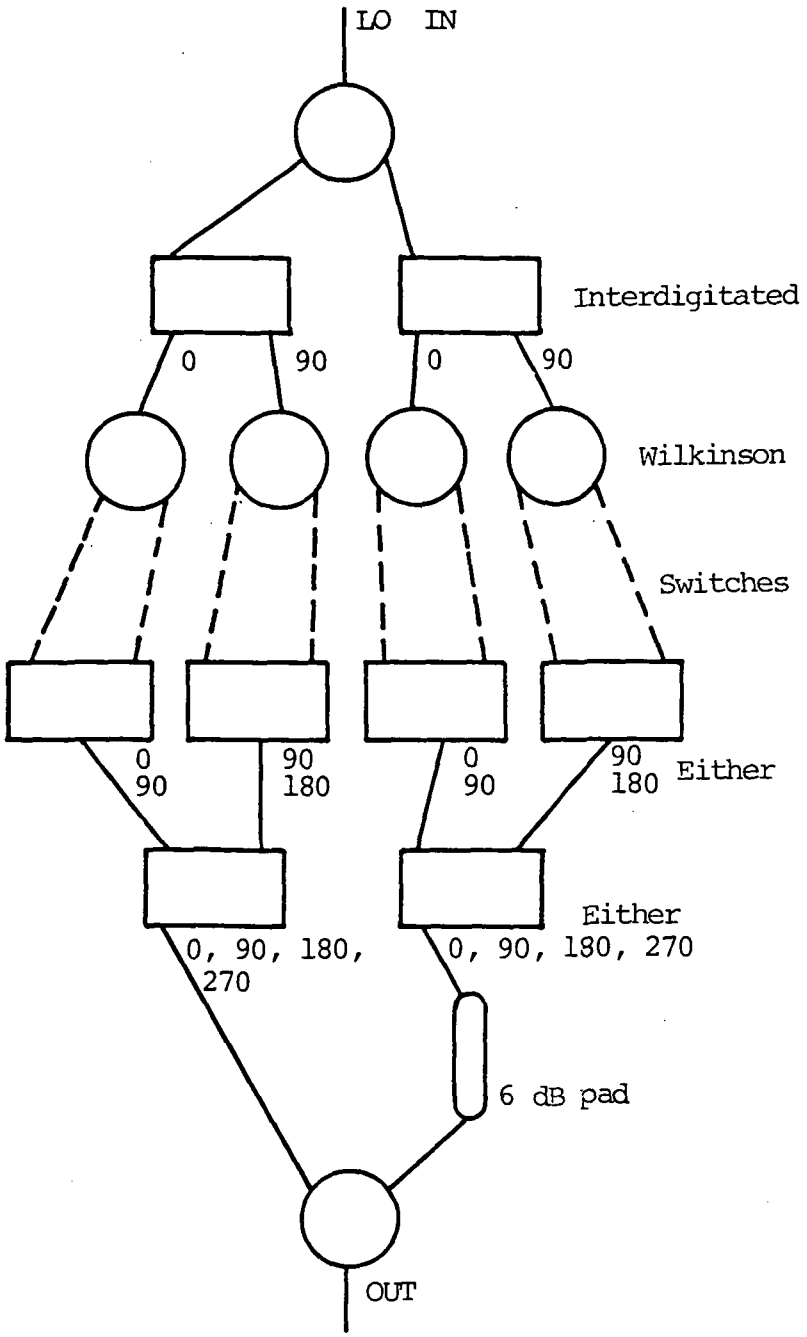


Figure 4.0.1, QPSK/QASK Modulator Type #1.
8 Interdigitated 90° couplers and 6 Wilkinson combiners.
Total line length ≃ 5λ, Area ≃ 2 mm^2.

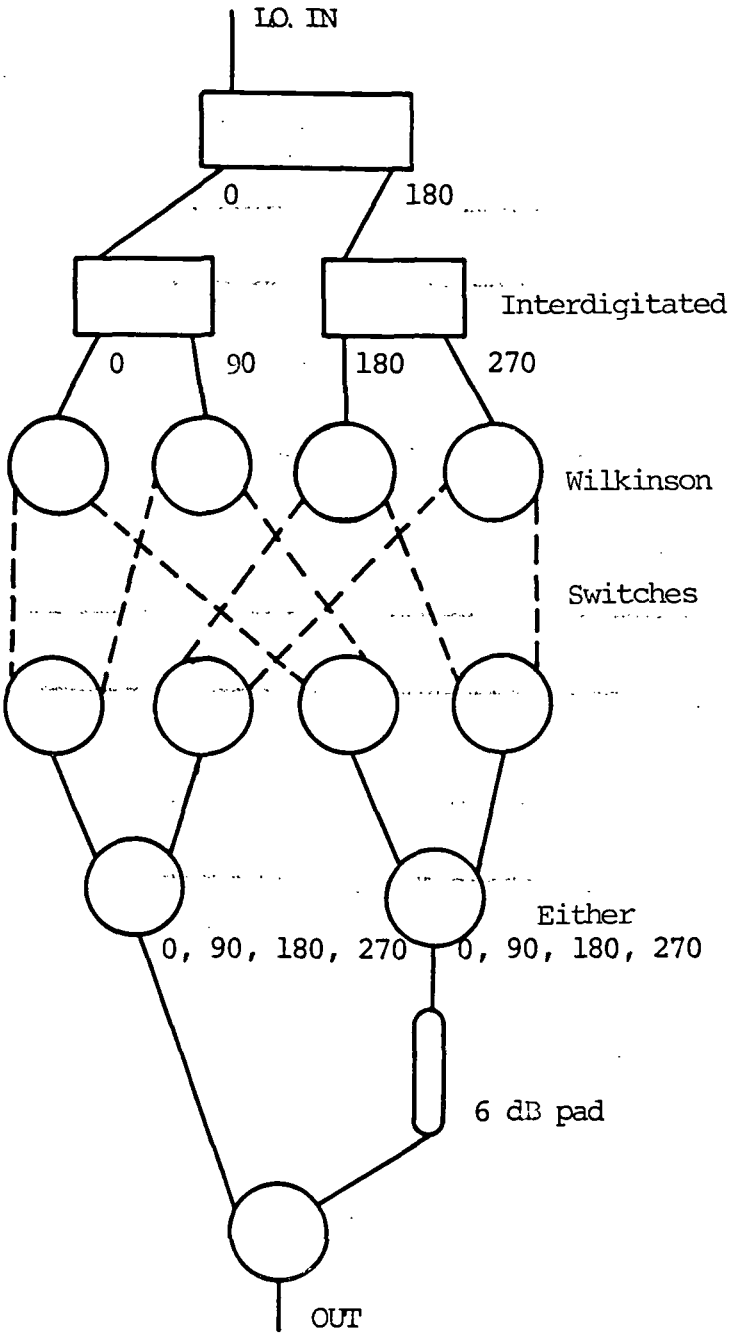


Figure 4.0.2, QPSK/QASK Modulator Type #1
3+1 Interdigitated 90° couplers and 11 Wilkinson combiners.
Total line length ≈ 6λ, Area ≈ 2.4 mm^2.
Length ≈ 5λ using 4-way combiners.

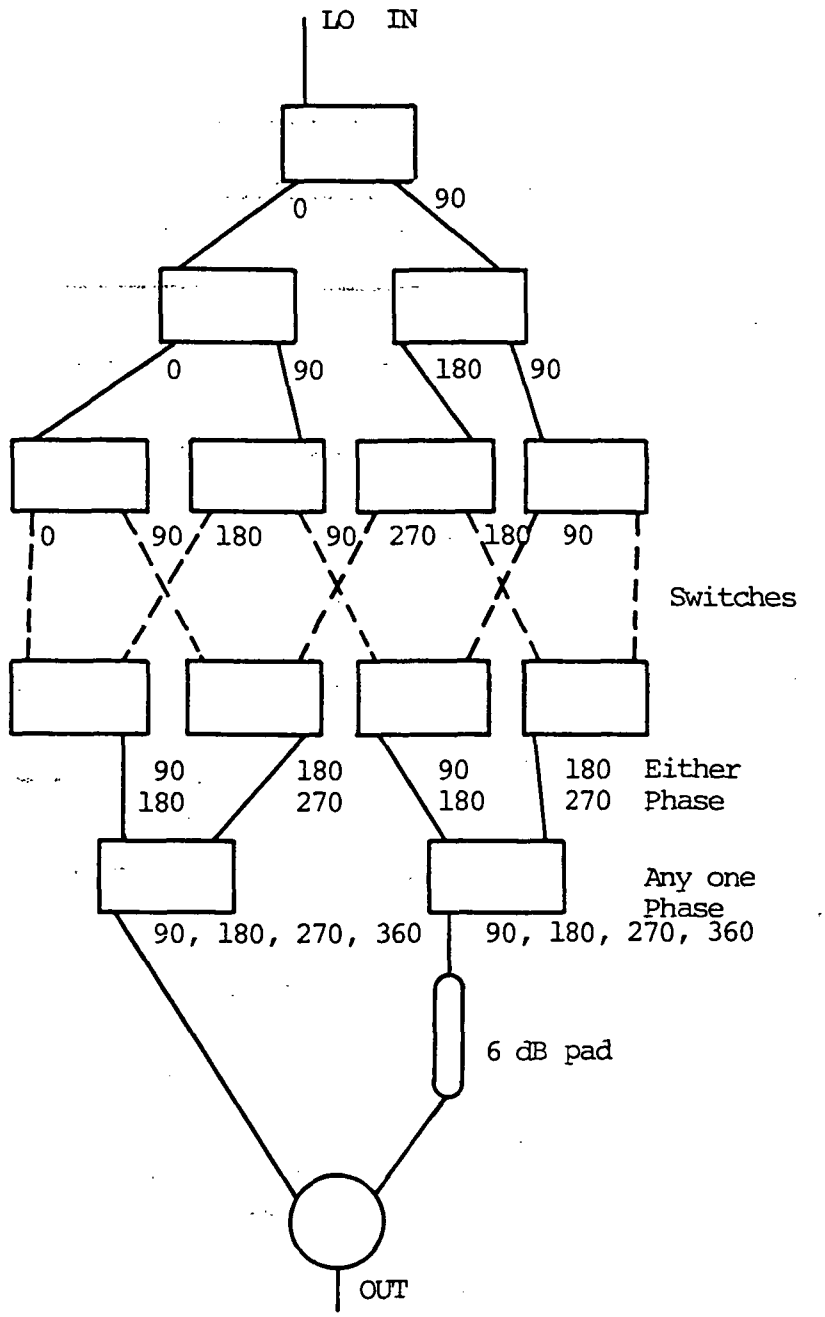


Figure 4.0.3, QPSK/QASK Modulator Type#3
13 Interdigitated 90° couplers and 1 Wilkinson combiner.
Total line length ≈ 4λ, Area ≈ 1.6 mm^2

of the areas given are based on the assumption that device spacing areas are negligible. Notice that if the circuit in figure 4.0.2 has the two sets of three Wilkinson combiners replaced by a four-way combiner (having a total path of 1 λ) then the total area consumed will be only about 25% higher than the circuit of figure 4.0.3. The circuit in figure 4.0.2 would also have the relative advantage of requiring 3 ground connections for the 3 interdigitated couplers. It seems very reasonable to assume that the 3 couplers can be arranged on the periphery of the substrate so as to make easy connection to a top surface, peripheral, virtual ground strip. The possibility of a four-way combiner seems very likely but has not been found in the literature.

Two QPSK/QASK modulators, shown in figure 4.1.1 and 4.2.1, are discussed here. Both modulators operate according the modulator option show in figure 4.0.2 and have the advantage of requiring small chip substrate area and signal phase/amplitude characteristics which promise accurate constellation characteristics. The difference between the two modulators originates from the choice of switch (dual-gate FET or shunt FET) which determines different power splitter impedances and the type of four-way power combiner circuit.

For both circuits the signal originates at the local oscillator and is split into two 0^{o} and 180^{o} components by two 90^{o} interdigitated hybrid couplers in tandem. Both components are then split by two 90^{o}

interdigitated hybrid couplers to give 0, 90, 180 and 270^{o} quadrature phasors. Each of these are split into two sets of equal magnitude and phase by four Wilkinson power splitters.

QPSK is generated by selecting one of the four phasors of the first set according to which of the four QPSK symbols is desired. QASK is generated by selecting one phasor from the first set and one phasor, attenuated by 6 dB, from the second set and adding them together to form one of the 16 QASK symbols.

The selecting of the desired phasor(s) is determined by the digital word to be transmitted. For QPSK, this is a two-bit word on lines A and B, with C and D switched off (see figures 3.6.6, 4.1.1 and 4.2.1), and for QASK it is a four-bit word on lines A, B, with C, and D. The decoder decodes this word so that the appropriate switch is thrown and cooresponding phasor transmitted. For SDFL the decoder must be equipped with standard SDFL level shifter at the output (not shown). The decoder states are shown in table 4.1.

		Decoder Input				Decoder Output 1 = High, 0 = Low							
		A	B	C	D	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
		0	0	0	0	1	0	0	0	1	0	0	0
	QPSK	1	0	0	0	0	1	0	0	1	0	0	0
		0	1	0	0	0	0	1	0	1	0	0	0
		1	1	0	0	0	0	0	1	1	0	0	0
		0	0	1	0	1	0	0	0	0	1	0	0
		1	0	1	0	0	1	0	0	0	1	0	0
		0	1	1	0	0	0	1	0	0	1	0	0
QASK		1	1	1	0	0	0	0	1	0	1	0	0
		0	0	0	1	1	0	0	0	0	0	1	0
		1	0	0	1	0	1	0	0	0	0	1	0
		0	1	0	1	0	0	1	0	0	0	1	0
		1	1	0	1	0	0	0	1	0	0	1	0
		0	0	1	1	1	0	0	0	0	0	0	1
		1	0	1	1	0	1	0	0	0	0	0	1
		0	1	1	1	0	0	1	0	0	0	0	1
		1	1	1	1	0	0	0	1	0	0	0	1

Table 4.1

This table shows the decoder input and output states, and thus switch states, controlling the QPSK and QASK modulator.

4.1 QPSK/QASK Modultor Using Single-Gate FET Switches

The FET line switch QPSK/QASK modulator technique (figure 4.1.1) operates by shorting to ground all phasors except the one desired. When the FET switch is "on", the line shorts and the phasor is reflected back into the matched termination of the hybrid coupler. The "off" switch passes the phasor to a 190 ohm resistor followed by a junction of the other 3 short circuited phasors and a Wilkinson power combiner. The resistors must be included so that the desired phasor does not see a short circuit from the other phasor microstrip line switches. By circuit analysis, the optimum value of resistance for maximum transmission to the combiner is R = 57.3 ohms. This resistor summing network characteristically gives a high signal loss of 18.8 dB. With this resistance the power combiner is not matched so the circuits beyond the combiner must not produce large reflections or standing waves will produce signal degradation from highly frequency dependent signal levels across the band. This problem is solved if R = 190 ohms but signal loss will increase slightly to 19.7 dB.

It should be noted that the entire resistor-network combiner can be replaced by six Wilkinson power combiners at the expense of about 3 mm^2 of chip substrate area but it will increase the signal level by about 19 dB. Since such amplification at these frequencies is difficult, and requires increased power dissipation, using the

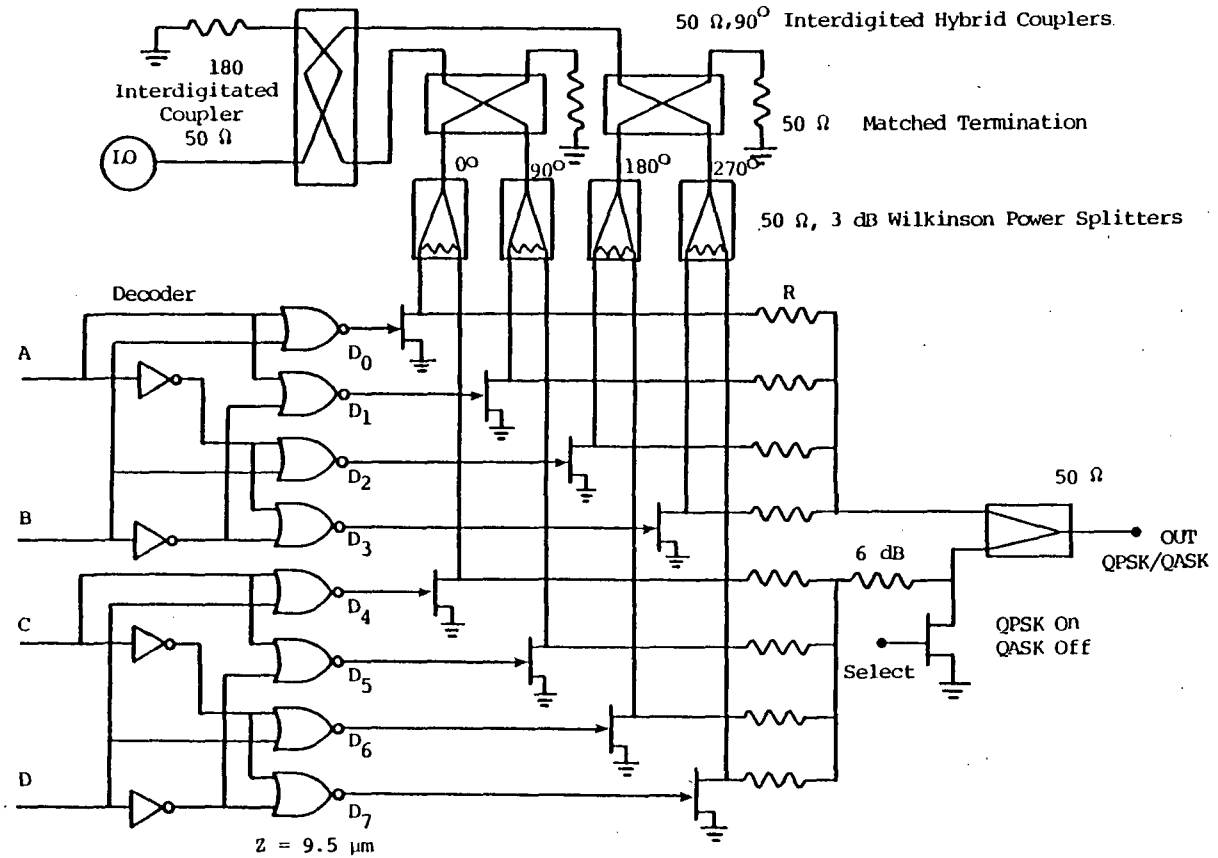


Figure 4.1.1, QPSK/QASK Modulator Using Shunt FET Switches.
Decoder outputs (with level shifting loads) switch 8 FET line switches.
Phasors are summed by a 50 Ω Wilkinson combiner. R = 57.3 Ω for minimium loss, R = 190 Ω for matched output. Each of the two sets of resistor combiners can be replaced by three Wilkinson combiners for lower loss.

additionl six combiners may be the more attractive method.

To determine the FET switch-gate width (Z) for optimum switching characteristics, the analysis given by Mcleuige and Sokolov [46] is extended. The analysis is based on FETs, compatible with other devices in the modem, with $N_d = 10 \times 19^{16} cm^{-3}$, and $V_P = 1.5$ V and $L_g = 0.7$ um. This gives $\bar{g}_m/Z = 0.12$ Z from figure 3.5.8, $C_g/Z = 0.06\ L_g Z/a = 0.29Z$ pF, from equation 7, and $R_{ON}Z = 1.97$ ohms from figure 3.5.4. As discussed in the section on Resonated FET Switches, high isolation and low insertion loss is sought. Since a flat frequency response is required, it is particularly important to reduce the frequency dependent insertion loss by reducing the drain capacitance. Reducing the gate width will reduce the drain capacitance, and thus insertion loss, but it will also decrease the isolation by increasing the "on" state drain-source impedance. A wide FET will also be difficult to drive by the decoder circuit. With these considerations a switch-gate width of Z = 0.2 mm is chosen.

If we consider the switch to be driven by SDFL and require 50 ps switch time (Δt) the decoder drive capability is determined by its output gate widths given by

$$\Delta t = 50 \text{ ps} = \Delta V\ C_g / \Delta I = \Delta V\ Cg/(\Delta V g_m) = C_g/g_m \text{ or}$$

$$50 \text{ ps} = 0.29 \times 0.2 \text{ pf}/(0.122\ Z_d) \text{ giving}$$

$$Z_d = 0.0095 \text{mm}.$$

This gate size is in the vicinity of the standard logic gate size throughout the chip.

The isolation is determined by the switch "on" state resistance (Ron) the input line impedance (50 ohms) and the output load impedance (R_L). R_L depends upon the type of combiner used. For all cases R_L is greater than 50 ohms and compared to Ron, it can be neglected for simplicity. So, the isolation is given by $20 \log[Ron||R_L)/(Ron||R_L + 50)]$ neglecting R_L gives $20 \log[(1.97/0.2)/((1.97/0.2) +50)] = 15.7$ dB. One might think that this leakage from the undesired phasors will significantly interfere with the desired phasor when added by an in phase combiner, but actually two of the leaked phasors are antipodal and will add destructively so as to cancel each other and thus they will not interfere with the desired phasor. The other leaked phasor is antipodal to the desired phasor and will add destructively to cause a rather negligible 1.57 dB loss in signal power. Since all of the phasors incur the same power degradation, and no phase alteration, the symbol constellation is formed undistorted.

The insertion loss of the switch is determined by the line impedance and the drain capacitance and not the switch "off" state resistance (since its negligibly high). The drain capacitance is roughly equal to the gate-drain capacitance. With the gate at 1.5 volts and the channel pinched off $Cg \simeq 0.29Z$ pF = 0.058 pF, or less. This capacitance on a 50 ohm line, and with a matched termination

approximation, gives an insertion loss of

$$|T|^2 = 1 - |\Gamma|^2 = 1 - [(wCZ_c)^2 + (wCZ_c)^4)/(1 + (wCZ_c)^2]^2$$

where Z_c is the 50 ohms line impedance. The insertion loss is 0.44 dB for 18 GHz, 0.54 dB for 20 GHz and 0.64 dB for 22 GHz. This result shows that the modulator has acceptable flatness over the band.

4.2 QPSK/QASK Modulation Using Dual-Gate FETs

The modulator described here is much simpler and requires less chip substrate area than the modulator using the FET line switch.

Here the switching function is performed by a dual-gate FET amplifier where the signal is applied to the gate nearest to the drain and the decoder output is applied to the other gate (as shown in figure 4.2.1). If the decoder output is high ($V_{g2} = 0$) then the dual-gate FET acts as an amplifier to the phasor. If the decoder output is low the FET amplifier channel current is completely cutoff resulting in very high insertion loss for the phasor.

The in-phase power combining is achieved by having the dual-gate FETs, for each QPSK modulator, share a common drain resistor. QASK is generated by attenuating one of QPSK modulators by 6 dB, then adding it to the other unattenuated QPSK signal by a Wilkinson combiner. QPSK is generated by switching off the attenuated QPSK signal and allowing the unattenuated QPSK signal to pass. The QPSK/QASK select switch is a 200 um single gate line switch (as described before) which can short (turn off) the lower QPSK signal for high isolation. The insertion loss is low (as described before) and can be compensated by reducing the attenuation of the 6 dB pad. A DC blocking capacitor preceeds the Wilkinson combiner to insure that the dual-gate FET bias voltage is not loaded by leakage currents of microstrip lines, pads and later matching inductors.

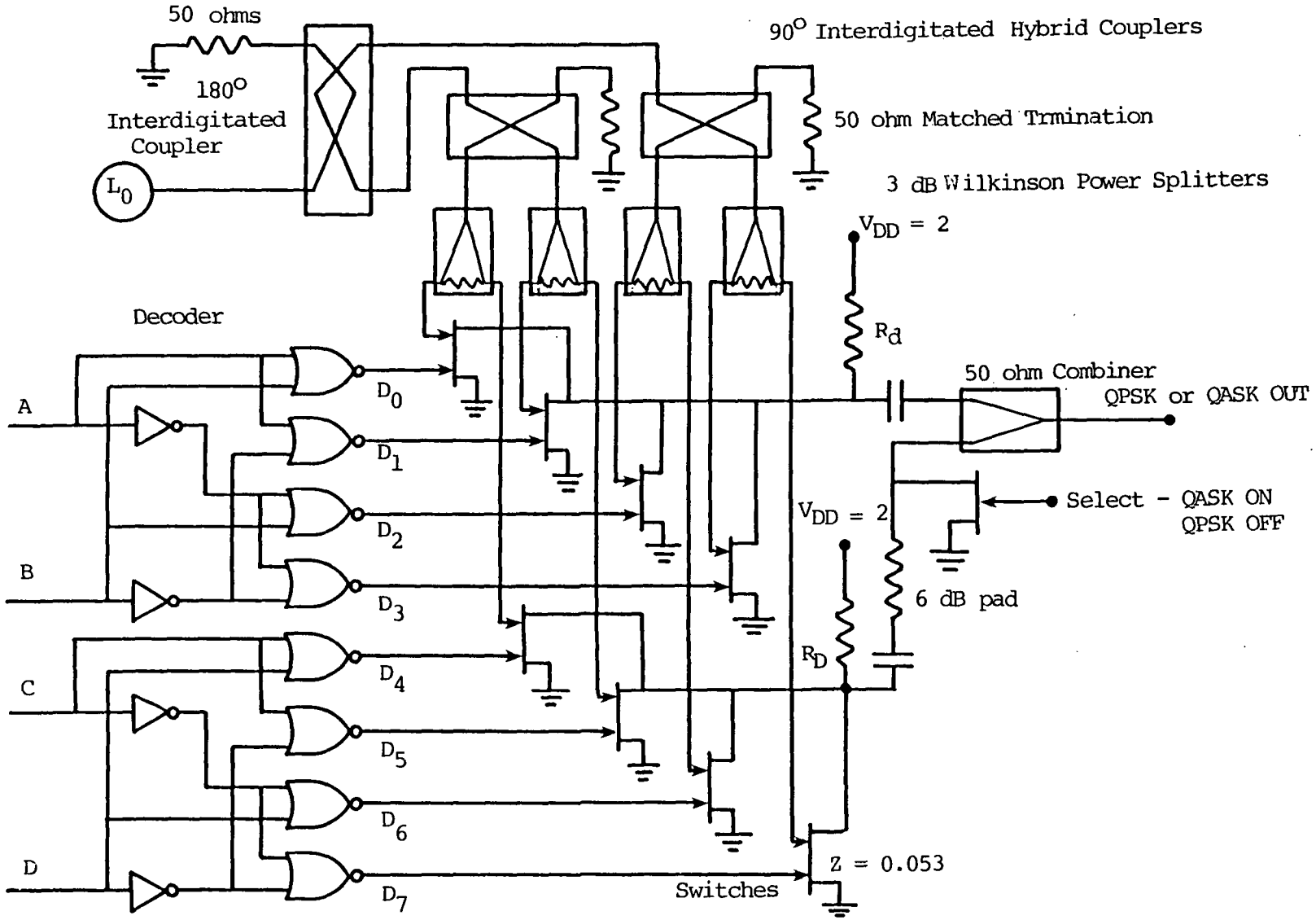


Figure 4.2.1, QPSK/QASK Modulator Using Dual-Gate FET Switches

The drain resistance (Rd) and dual-gate FET gate width (Z) are chosen by considering the amplifier gain, total power dissipation, linear operating region and matching considerations. The FET has L_g = 0.3 um, N_d = 15 x $10^{16}cm^{-3}$, V_P = 1.5 V and f = 20 GHz. This gives the following device chracteristics. From figure 3.5.2 the reactance-gate width product is jXZ = 12, from figure 3.5.5 XopZ = 2.51, from figure 3.5.6 RopZ = 4.75, from figure 3.5.8 g_m/Z = 0.162 and I_{dss} = 0.19 Z from the section on channel current analysis.

For a given power consumption, the gain is increased if the drain resistance is increased. To maintain a matched output, choose R_d = 50 ohms. This matches the signal to a rather high impedance (50 ohm) Wilkinson combiner, eliminating the standing wave problem mentioned earlier. The drain voltage (V_d) should be kept above 1.5 volts for the amplifier to operate in the linear region. V_{DD} is selected as 2 rather than 5 volts because of the large power dissipation for V_{DD} = 5. So with V_{DD} = 2, the voltage drop 1.0 volts across the drain resistor gives the current $I_p = I_{dss}$ = 1/50 = 0.02A. With $V_{ds} \simeq 1$ the operation is at the edge of the linear response region (for L_g = 0.3 um) but with small signal levels there should be no distortion. So the power dissipation for both QPSK circuits is V_{DD} (2 I_D) = 0.08 watts. The gate width which draws I_{dss} = 0.01 = 0.19 Z, is Z = 0.105 mm.

The input gate impedance is

R_{op} = 4.75/0.105 = 45 ohms and

jX = 12/0.105 = j114 ohms, so

$|T|^2 = 1 - |(45||j114 - 50)/(45||j114 + 50)|^2$.

Therefore 96% of the incident power is coupled to the gate. The rms line voltage on the gate is $V_g = V_o(1 + r) = 1.04\ V_o$. This, in effect, is a gain factor due to its high input impedance. Neglecting parasitics for brevity (only a rough approximation at these frequencies) the voltage gain is given roughly by

$G = 1.04\ (R_d||R_L)\ g_m = 1.04 \times 25 \times 0.162 \times 0.105 = 0.44$

that is, the loss is 7.1 dB. This small power loss is not difficult to recover by amplification so it is not considered as an important disadvantage for this QPSK/QASK modulator architecture.

The decoder drive capability, i.e. gate width, needs to be of sufficient width to drive the dual-gate FETs. The gate width is given (as before) by $\Delta t = 50$ ps $= \Delta V C_g/\Delta I = C_g/g_m = 0.29 \times 0.105/(0.122\ Z_D)$ therefore $Z_D \geq 5$ um.

4.3 QPSK/QASK Modulator Using FET Phase Splitters and Dual Gate Switches

This modulator (shown in figure 4.3.1) has the advantage of requiring less than half the substrate area of any of the other modulators. It does not require a 4-bit word decoder circuit and requires only two RF ground connections which allow easy connection to a peripheral virtual ground strips. The modulator has the disadvantage of rather high power dissipation and high signal loss.

The other modulators have the problem of generating balanced phasor magnitudes from possible differences between the "on" state gains of the dual-gate FET amplifiers or the "off" state insertion loss of the FET line switches. Likewise, this scheme has balancing problems due to the $0/180^{o}$ phase splitter and the dual-gate switches, but it has reduced coupler error because of the smaller number of couplers. The two FET phase splitter outputs should be of equal magnitude, if both load resistors (R_L) are equivalant, but variation of channel characteristics relative to the other FETs will generate differences between their respective outputs. For all of the modulators, phasor error will primarily be due to poor material quality or lack of fabrication control (as described earlier).

This circuit operates by equally splitting, with 0^{o} phase difference, the 20 GHz LO and attenuating one of the resultant signals by 6 dB. Both signals are then equally split by two 90^{o} interdigitated hybrid couplers.

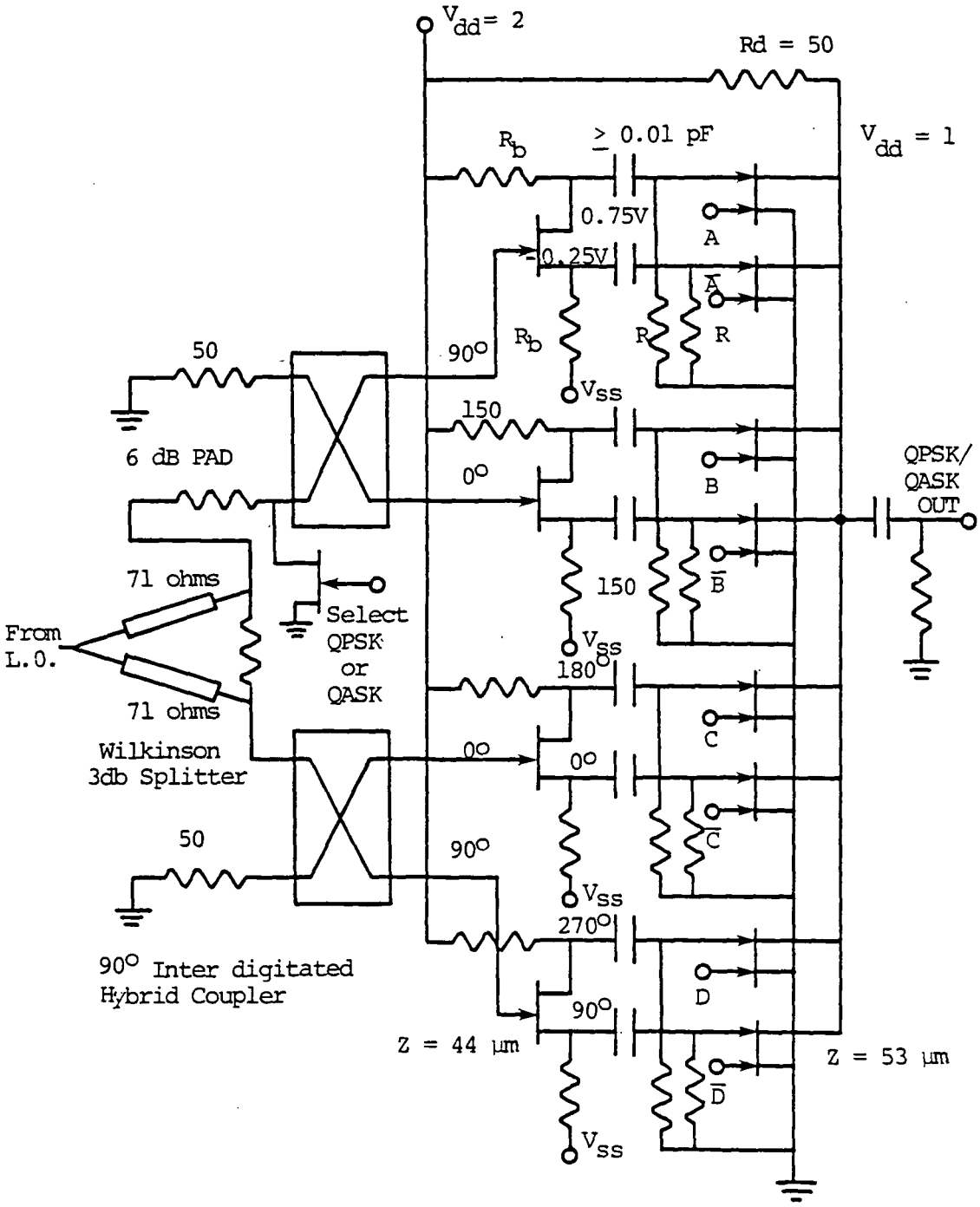


Figure 4.3.1, QPSK/QASK Modulator Using 4, 180° FET phase splitters and 8 dual-gate FET Switches. Phasor outputs are summed by Rd.

This gives four phasors of 0^o, 90^o and 0^o, 90^o (at -6dB) which are output to four $0^o/180^o$ low gain FET amplifiers. The two sets of 0^o, 90^o, 180^o and 270^o phasors are then capacitively-coupled (because of bias voltage differences) to eight dual-gate FET switch/amplifiers. The switching gates are connected to the inverted and noninverted outputs of the 4 bit latch, as labeled in figure 4.3.1 and 4.0.4. Therefore, the digital-word decoder circuit is not needed for this modulator and chip area and power dissipation is reduced. The selected output phasors are added by having all eight dual-gate FETs share the same drain resistor (as described for the previous modulator).

The circuit analysis for the dual-gate FETs follow that given for the previous modulator. For output matching R_d = 50 ohms, for power considerations V_{DD} = 2 V and for gain and linearity considerations V_d = 1 V. With two FETs on at a time the total current is

$$2\ I_{dss} = (V_{dd} - V_d)/R_d = 0.02 \text{ amps},$$

giving the total power consumption of the dual-gate FET

$$P_d = V_{DD}I = 0.04 \text{ watts}.$$

The gate width Z is given by

$$I_{dss} = 0.19\ Z = 0.02/2 \text{ or } Z = 0.0526 \text{ um}.$$

So as before, the gain is roughly

$$G = Rd||R_L g_m = 25 \times 0.162 \times 0.0526 = 0.213 \text{ or } -13.4 \text{ dB}.$$

The phase splitting FET must have equal source and drain resistors (R_b) so that each output phasor is of equal magnitude. V_{DD} is chosen as 2 V to reduce power

dissipation. There is no advantage in using large amounts of power for increased gain here, since only an equivalent of one FET will be used at any time. The source and drain voltage are chosen as -0.25 and 0.75 volts to increase the gain via small V_{ds} and larger transconductance g_m from increased V_{gs} respectively. V_{ds} is large enough (with small signal levels) to remain at a linear operating point and V_{gs} is small enough to not cause significant gate conduction.

R_b is chosen as 150 ohms by foresight of power dissipation constraints. Then the current, I_{dss} = 1.25/150 = 0.00833 A. The gate width (Z) is given by I_{dss} = 0.19 Z or Z = 0.0438 um. The power dissipation of all four FETs is $P = 4(V_{DD} - V_{SS})I_{DSS}$ = 0.117 watts. The FET input impedance is Rop = 4.75/0.00833 = 570 ohms and jX = 12/0.0083 = 1440 ohms which is very high and almost looks like an open circuit to the hybrid couplers.

Because the signal is terminated with the high input impedance of the FET, the standing wave voltage is twice that which would occur if the line were terminated in it's characteristic impedance, so we multiply the general expression for the gain by 2 for reflection gain. So the gain is $G = 2\, g_m(R_b||R_L)/(1 + g_m R_b)$ where R_L is the impedance of the dual-gate FET given as R_L = Rop||jX, where Rop = 4.75/0.0526 = 90 ohms, jX = -12/0.0526 = -j228 ohms and g_m = 0.162 x 0.0438 = 0.0071 mhos. So $G \geq 2 \times 0.0071|53 - j13.1|/(1 + 0.0071 \times 150) = 0.375$ or -8.5 dB. The coupling/DC blocking capacitor is large ($\geq$ 0.1 pF) and

of low impedance so its loss is neglected.

The signal loss for the entire modulator is 8.5 + 13.4 = 21.9 dB and the total power dissipation is 0.117 + 0.04 = 0.157 watts.

5 QPSK/QASK Demodultor and Baseband Processor

5.1 Time Delays The dual modem requires time delays of T and T/2. For a signal with a fixed symbol rate of 500×10^6 symbols per second(500 MSPS), this corresponds to delays of 2 and 1 ns. This is a very long delay if we consider that the GaAs microstrip path length required for 2 ns is roughly $\ell = v_p t = c/\sqrt{\epsilon_{eff}} \times 2 \times 10^{-9} \simeq 200$mm! Even for a thin (lossy) high impedance line of width w = 0.1d =10 um (d = 100 um substrate thickness) this will occupy a large chip area given by 200 mm x 0.01 mm (x 2 for spacing) = 4.0 mm^2, for one 2 ns delay.

Two methods for reducing the line length are achieved by using the cross-tie coplanar slow-wave structure or the lumped element technique. The first of these methods (shown in figure 5.1.1) can reduce the transmission lines physical path length by roughly a factor of 6 compared to GaAs microstrip transmission line [50]. The path length would then be 200 mm/6 = 33 mm. The area would be roughly $\ell \times w$ = 33 mm x 0.5 mm = 16.7 mm^2 + spacing, for one 2 ns delay. This is an exorbitant amount. Because of its large line width, the cross-tie structure does not reduce the required area even though the line length is shorter.

The lumped element technique employs alternately cascaded shunt capacitors and series inductors of individual electrical length much less than one wave length (say 0.1 λ or less) [45]. Here λ is the baseband signal wave length of λ = 200 mm. For half and full symbol delays, the device

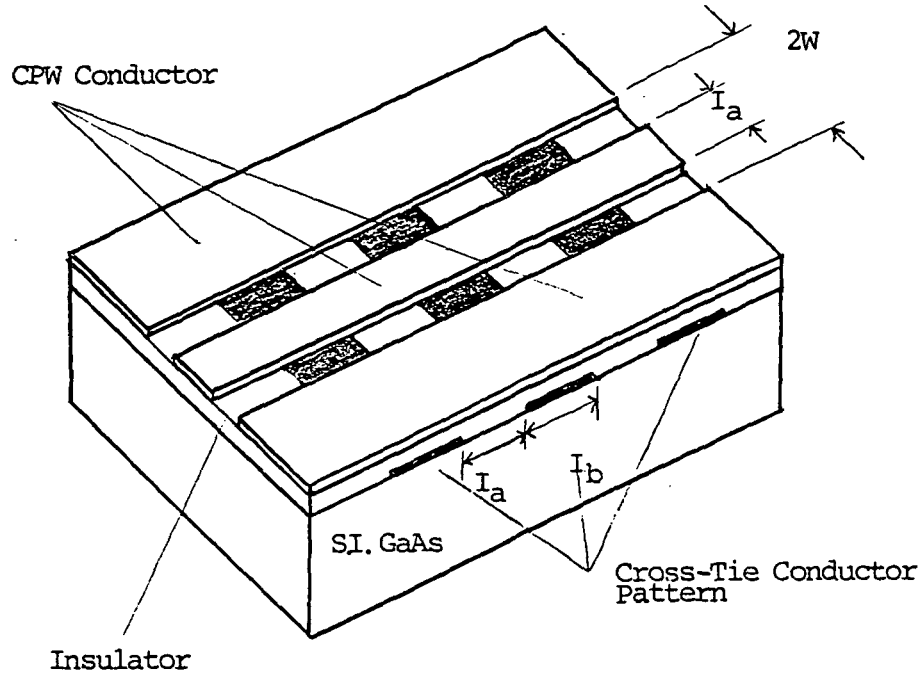


Figure 5.1.1, Cross-Tie Coplanar Slow-Wave Structure
After [46]

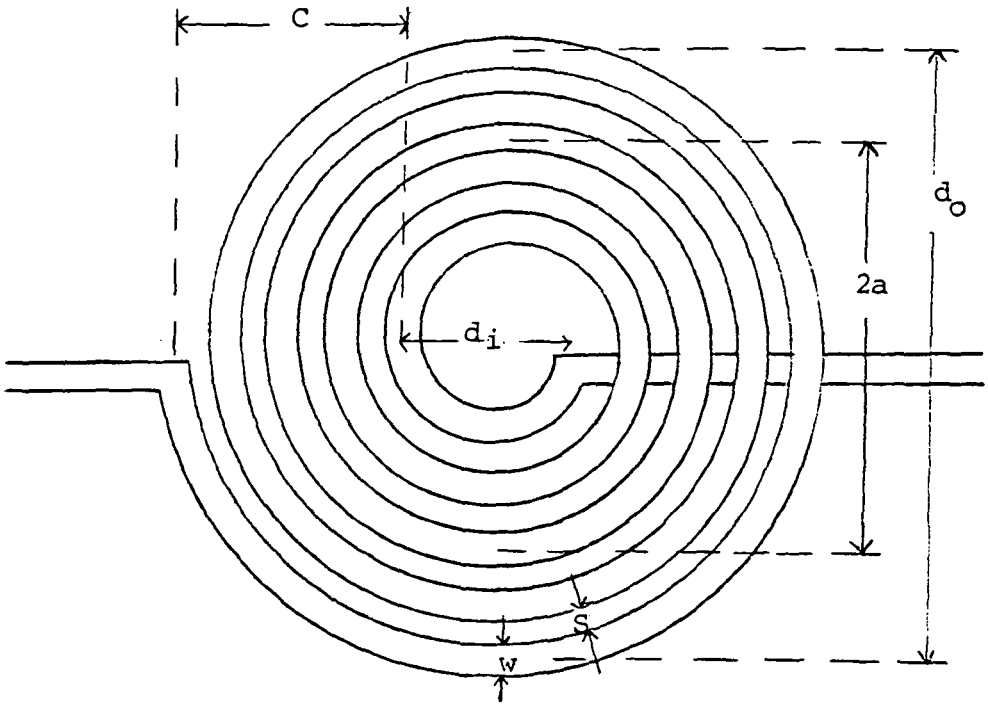


Figure 5.1.2, Spiral Inductor for Delay Lines and
and Matching Circuits

requires at least 5 and 10 (respectively) capacitor/inductor pairs to achieve this delay as, effectively, a distributed transmission line. A transmission line with low loss, or more specifically with R/L = G/C, will have a group velocity equal to the phase velocity $v_p = 1/(LC)^{0.5}$. So the physical path length $\ell = v_p t = 2 \times 10^{-9}/(LC)^{0.5}$.

In order to design a delay line, suitable for this modem, the following steps will be taken:

1) find an expression for the inductance and loss of a spiral inductor

2) find the minimum inductor area for a given inductance

3) find an expression for the capacitor's and inductor's capacitance

4) express the transmission line area as a function of the capacitors' and inductors' area, for a given delay

5) minimize the expression for the transmission line area while considering various parameters

From Gupta [47] a spiral inductor has a Q about 10% higher than the square inductors and the inductance is given by $L_S = a^2n^2/(8a + 11c)$nH [51] where a and c are in mils. The inductor is shown in figure 5.1.2.

The Q of the spiral inductor is

$$Q = 2 \times 10^{-9} fwna/(1.5\ R_s(8a + 11c))$$

where w is the line width and $R_s = 2.61 \times 10^{-7}\ f^{1/2}$ for the metal thickness appreciably greater than twice the skin

depth. The skin depth for copper is 66 $/\sqrt{f(MHz)}$ um and for aluminium is $58/\sqrt{f(MHz)}$ or 1.8 um @ 1 GHZ.

$$\text{Thus } Q = \frac{0.0051 \times (10^9)^{0.5} wN(d_o + d_o/5)/4}{(8(d_o + d_o/5)/4 + 11(d_o - d_o/5)/4)}$$

$$= 7.1\ wn.$$

Where $d_i = d_o/5$ is used for maximizing the Q [51]. Optimizing the parameters for a large inductance requires keeping w large, the line separations (s) small, and the overall diameter (d_o) small. Values of inductance higher than 10 nH are difficult to achieve because of intersegment fringing capacitance [45], so an inductance of 5 nH is sought. With $a^2 = (d_o + d_i)/4$, $c = (d_o - d_i)/2$ and $d_i = d_o/5$ we have $L_S = 0.013\ d_o n^2$ nH. For $L_S = 5$ nH this gives $n d_o^{0.5} = 19.6$.

The transmission line characteristics also depend on the line capacitance. The capacitance of a parallel plate capacitor is $\epsilon = \epsilon_r A/d$. For typical dielectrics used in GaAs IC fabrication $\epsilon_r \simeq 5$ (ϵ_r = 4 to 5 for SiO_2 and 6 to 7 for Si_3N_4 [45]), and d is roughly 3 um. This gives the capacitance per mil^2 as $C = 10^{-14}$ F/mil^2.

The total area of the transmission line with delay T_s is $A_{TOT} = \ell \times w = 2 \times 10^{-9} w/(LC)^{0.5}$ where w is the sum of the capacitor and inductor width $w_c + d_o$. Consider that the spiral inductor is also going to have a shunt capacitive component roughly as if it were a disc capacitor (assuming the line spacing is smaller than, or comparable to the dielectric thickness). The disc area is slightly smaller

than the square's area but that it will have fringing capacitance making it have a capacitance closer to that of an ideal parallel plate square capacitor (roughly d_o x d_o), the capacitance is roughly $C_{ind} = 10^{-14}\ d_o^2$ F.

so $A_{TOT} = \dfrac{2 \times 10^{-9}(w_c + d_o)}{[(.013 d_o n^2/d_o)(w_c l_c/l_c + d_o^2/d_o) \times 10^{-14}]^{0.5}}$

$$= \frac{2 \times 10^{-9}(w_c + d_o)}{(0.013\ d_o n^2 \times 10^{-9}/d_o(w_c l_c/l_c + d_o^2/d_o) \times 10^{-14})^{0.5}}$$

$$= 5574\ (w_c + d_o)^{0.5}/n\ \text{mils}^2$$

This area of the transmission line should be minimized where l_c is the capacitor length. To minimize, consider that if d_o ==> 0 the expression is meaningless since the inductor is vanishingly small, n becomes unrealistic, and the Q becomes infinite but if w_c ==> 0 we still have inductor/capacitor pairs where the only capacitance is the shunt capacitance of the series inductor over the ground plane. So with w_c = 0, this gives

$$A_{TOT} = (5547/n) d_o^{1/2} \text{mils}^2$$

We see that we must maximize n while keeping d_o small. The minimum spacings (s) of the inductor segments are about 0.04 mils (1 um). This gives the relationship

$$(d_o - d_i)/2 = n(w + s) \text{ or } n = 0.4\ d_o/(w + 0.04).$$

where $d_i = d_o/5$, n is maximized for the minimum line width deliniation of w = 0.04 mil = 1 um, so $n = 5\ d_o$. But this is restricted by the maximum inductance parameter of 5 nH so 5 nH = $0.013\ d_o n^2$ or

$$n = 19.6/d_o^{0.5} \text{ or } d_o = 13.4/(w + .04)^{2/3} \text{ and}$$

$$A_{TOT} = 5547 d_o^{0.5}/(19.6/d_o^{0.5})$$

$$= 283\ d_o \text{ mils}^2 = 3782(w + .04)^{2/3}.$$

Also

$$Q_i = 7.1\ wn = 7.1\ w\ 19.6/d_o^{0.5}$$

$$= 139w/d_o^{0.5} = 38\ w/(w + 0.04)^{0.5}$$

With the total number of inductors equal $N > 10$ we have

$$A_{TOT} = 283\ d_o = N\ d_o^2 \text{ or } d_o = 283/N \text{ or}$$

$$N = 21.1/(w + 0.04)^{2/3}$$

These expressions show that higher Q and fewer inductors are achieved at the expense of increased substrate area.

For values of $w>>5$, inductor line spacing (s) can be made larger than its fixed value of 0.04 mils (1 um) without changing any of the values of A, W, d_o, Q, h or t significantly, for a given N.

The above results are summarized and various examples for 2 ns delay lines are given in Table 5.1.

Table 5.1

For L_S = 5nH

$Q_i = 38w/(w + 0.04)^{1/3}$	for individual inductors
$A = 3792\ (w + 0.04)^{2/3}$	area ($mils^2$)
$N = 21.1/(w + 0.04)^{2/3}$	# of inductors
$w = (21.1/n)^{3/2} - 0.04$,	inductor line width
	$6.54 \times 10^{-4} mm^2/mil^2$
$n = 19.6/d_o^{0.5}$	# of turns
$Z = (L/C)^{0.5} = 707/d_o$	line impedance
	(approximate)
$d_o = 283/N$,	inductor width

For

N	w(mils)	Q_i	A(mm^2)	d_o(mils)	n	$Z_o$ohms	$P_o/P_{in} = (1 - 1/Q)^N$
6	6.55	97	8.72	47.1	2.9	15	0.94
20	1.04	38	2.61	14.1	5.2	50	0.59
40	0.343	21	1.3	7.07	7.4	100	0.13
60	0.167	17.4	0.87	4.7	9.0	150	0.029
80	0.095	9.8	0.65	3.53	10.4	200	0.00018

For L_S = 10 nH

$Q_i = 47.8\ w/(w+0.04)^{1/3}$	$n = 27.7/d_o^{0.5}$
$A = 3384(w + 0.04)^{2/3}$	$d_o = 200/N$
$w = (11.8/N)^{3/2} - 0.04$	$Z = 10^3/d_o$

For N	W(mils)	Q_i	A(mm^2)	d_o(mils)	n	$Z_o$ohms	$P_o/P_{in}=(1-1/Q)^N$
40	0.12	10.6	0.65	5	12.4	200	0.019
30	0.207	18.8	0.87	6.7	10.7	150	0.19
20	0.41	25.5	1.3	10	8.76	100	0.45

To summarize, it seems possible to fabricate 2 nS delays using the lumped element technique. The area required for the delay decreases in proportion to roughly the inverse of the number of inductors, while the total loss is inversely proportional to the area used. Since substrate real estate is very precious, it would seem practical to use the higher loss (smaller area) cases (if the group velocity does not become too frequency dependent) followed by an amplifying FET if necessary.

Both cases of L = 5nH, N = 60 and L = 10 nH, N = 30 look attractive since they use only 0.87 mm^2 and have an easily recoverable 15 and 7 dB loss respectively at these frequencies. Recall that interfringing inductor line capacitances may make the 10 nH inductor difficult to realize though larger ones have been realized. Increasing the spacing (s) will decrease this coupling problem but it would require an equal decrease in inductor line width (w) which would significantly increase the losses. Finally, the low impedance nature of these lines will make matching to the low impedance FET devices much easier than with higher impedance lines.

5.2 2-Bit Digital-to-Analog Converters (DACs)

Digital-to-analog conversion (DAC) is required in the data detection of the baseband processor. Two simple and effective DACs are discussed here.

The first method, which can be used for both SDFL and E/DFL, avoids the use of the encoder/decoder pair following the ADC and instead uses the decision signal outputs from the ADC comparators. This circuit (shown in figure 5.2.1) can be modified to operate with enhancement FETs, rather than depletion FETs, by inserting two level-shift diodes in series with V_{DD} rather than in series with the source terminals, as in figure 5.2.2. The modified circuit would have the added degradation of slightly higher open channel resistance for the FET switch, but this circuit would be the proper choice for E/DFL.

The advantage of these two DACs, over the ladder network type, is primarily minimizing the decision signal propagation delay by eliminating the encoder/decoder pair, thereby decreasing the long time delay required in the bit timing circuit (see figure 2.2.9).

The DAC in figure 5.2.1 consists of three D-FET/load pairs which when switched by the comparator outputs give four possible output states V_L, 3/4 V_L, $V_L/2$ and $V_L/4$ where $V_L = V_{DD}$ - (two diode voltage drops) = 2 - 1.56 = 0.44 volts. The two diodes shift the FET source terminal voltage by about 1.56 V so that the FET is switched off when $V_g = 0$. The E/DFL DAC circuit has two diodes in series with V_{DD} so

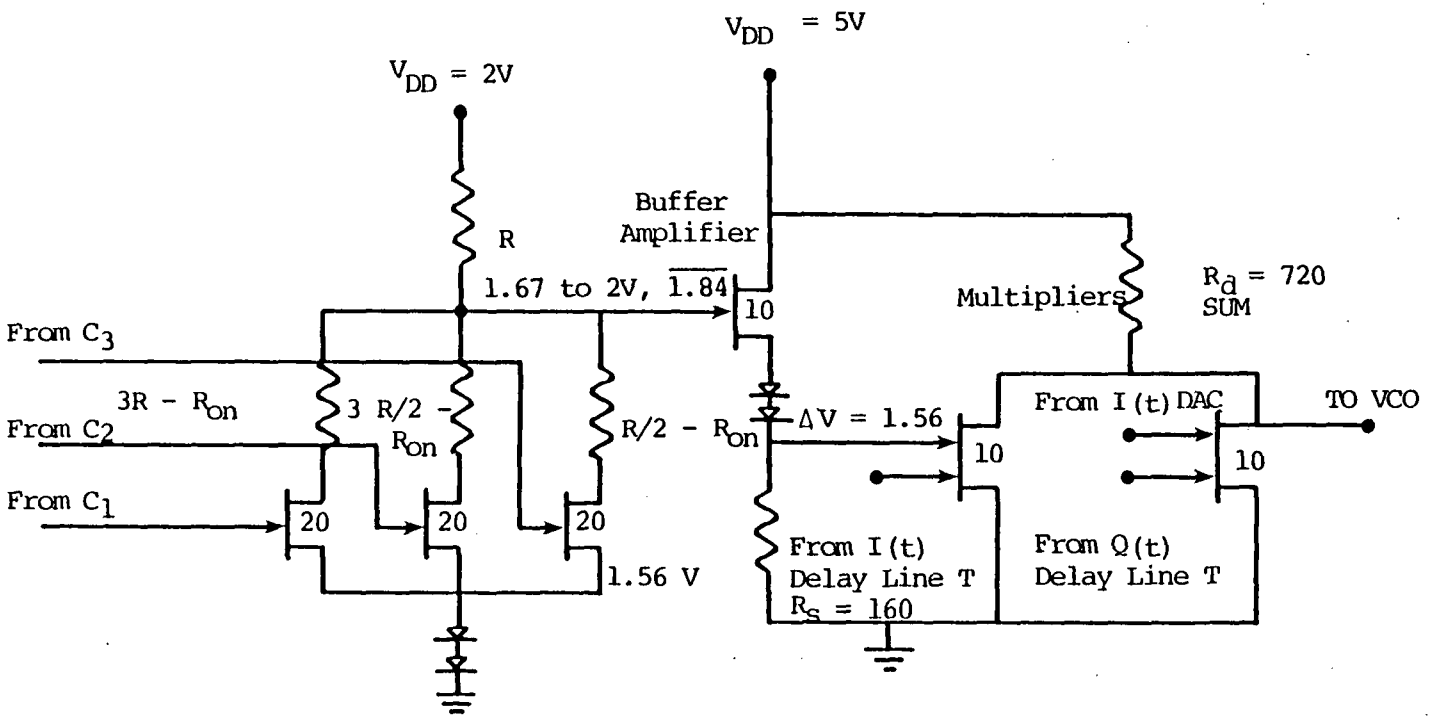


Figure 5.2.1, Digital to Analog Convertor and Dual-Gate Multiplers for SDFL or E/DFL

Figure shows decision signals (C_i) determining state of switching FETs which inturn determins the voltage division of the bridge. The resistor bridge's analog output signal is buffered before it is output to the multiplier. Multiplier outputs are summed via R_d. R_{on} = 56 ohms and R = 1000 ohms.

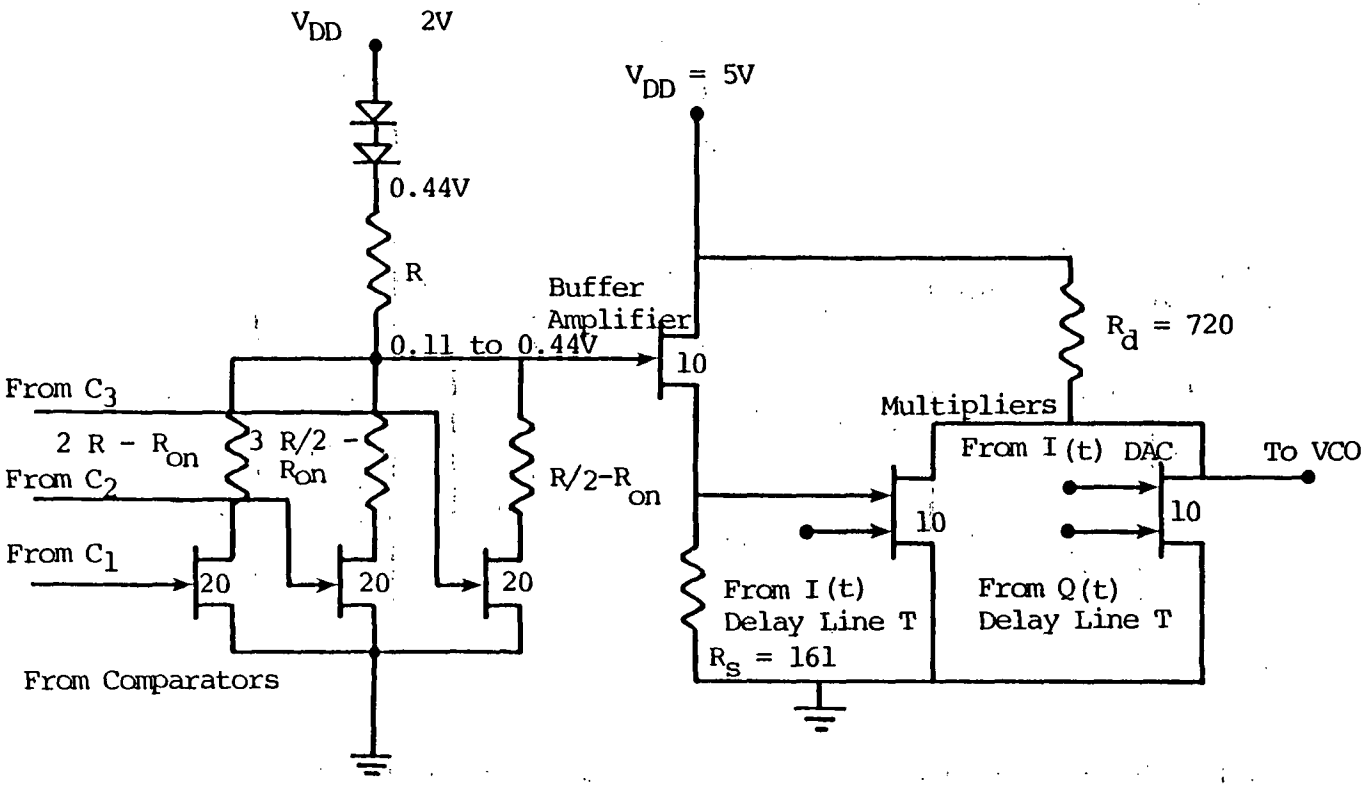


Figure 5.2.2, Digital-to-Analog Convertor and Dual-Gate Multipliers for E/DFL R = 1000 ohms, R_{on} ≈ 83 ohms

that the supply voltage to the voltage divider is 0.44 volts above ground. V_{DD} had been chosen as 2 volts so that the output signal from the DAC would have voltages compatible to the source follower buffer amplifier, that is, the voltage swings are small (less than $\pm$0.3 V), so that nonlinearities are insignificant and the gate does not become significantly (> 0.5 V) forward-biased. The states of the DAC are

Comparator Output (switch input level)			Analog Output	
C_1	C_2	C_3		
L	L	L	V_L	where
L	L	H	3/4 V_L	V_L = 0.44
L	H	H	$V_L/2$	L = Low
H	H	H	$V_L/4$	H = High

The DAC FET switch "on" resistance (R_{ON}) (discussed later) must be considered as part of the voltage divider's resistance in that arm for accurate voltage division, therefore the ideal resistance value must be decreased by R_{ON}, 3/2 R - R_{ON} and R/2 - R_{ON}. A second-order error, not accounted for here, is due to the small change in voltage drop across the diodes at different currents (switch combinations).

The DAC must be designed with small gate width so that the input capacitance does not load the comparators of the ADC or the decoder (if used). Small gate widths lead to

a higher output impedance to the buffer amplifier but this will present a problem only if the maximum DAC output impedance approaches about 4000 ohms as shown in the "Buffer Amplifier" section. But since the FET switches have an "on" resistance determined by the gate width (Z), they are not ideal switches, and thus Z cannot be arbitrarally small. The "on" resistance has further variability since the "on" imput gate voltage (ideally $V_{gs} = 0$) is not known precisely because of the complex switching characteristics of the comparator. In order to reduce the possibility improper voltage division of the DAC, the gate width (Z) and the resistor elements (R) should be chosen such that the "on" state channel resistance (R_c) is dwarfed by R. The FET's "off" resistance, and isolation at these frequencies (see 3.8.1), is very high and thus will not effect the voltage dividers performance.

As a compromise to the above factors the gate width Z is chosen to be 20 um. The "on" resistance is given according to figure 3.5.4 with $N_d = 15 \times 10^{17}$ and $L_g =$ 0.7 um, so $R_{ON}Z = 1.12$ ohm mm for SDFL ($V_P = 1.5$ V) and $R_{ON}Z$ = 1.65 ohm mm for E/DFL ($V_P = 0$ V). For a 0.02 mm wide FET this gives $R_{ON} = 56$ ohms for SDFL and $R_{ON} = 82.5$ ohms for E/DFL. To dwarf any error due to the variance of R_{ON}, R_{ON} is chosen to be 1000 ohms. Any reasonable variance in R_{ON} (< 50%) will produce a small (2%) error voltage. The output impedance range is then $(3R||(3/2\ R)||(R/2||R) = 250$ ohms (all FETs "on") to R = 1000 ohms (all FETs off).

The total average power dissipation of the DAC is half the power dissipated with all FETs on. So

$$P = (V_{DD})^2/((3R||3)(2R||R)/2 + R) = (2)^2/4000$$

$$= 1 \text{ mW}.$$

Another method of implementing the 2-bit DAC can be realized using the standard R-2R ladder network, shown in figure 5.2.3. The operation of the R-2R ladder network is based on using the digital logic levels as high impedance voltage sources on the ladder network inputs. The network is arranged such that the most significant bit (MSB) contributes twice as much voltage to the output as the least significant bit (LSB).

Figure 5.2.3 shows an R-2R ladder network DAC which can operate with either SDFL or E/D FET logic. If BFL is used all ground connections shown should be replaced by V_{SS}. With signal rates of 500 MHz (cooresponding to 500 MSPS) any of the logic types can be used since their speeds are easily in excess of 500 MSPS.

Since the logic signals are not true voltage sources but instead have output impedances determined by the drain resistance value and switch "on" resistance, the ladder network should be designed with impedances that will not excessively load these outputs or be susceptible to the logic signal drivers impedance differences between each state. The decoder logic circuit can have its gate widths cascaded from smaller (5 um) to larger (= 20 um) gate widths. For 20 um gate widths, the decoder output impedance

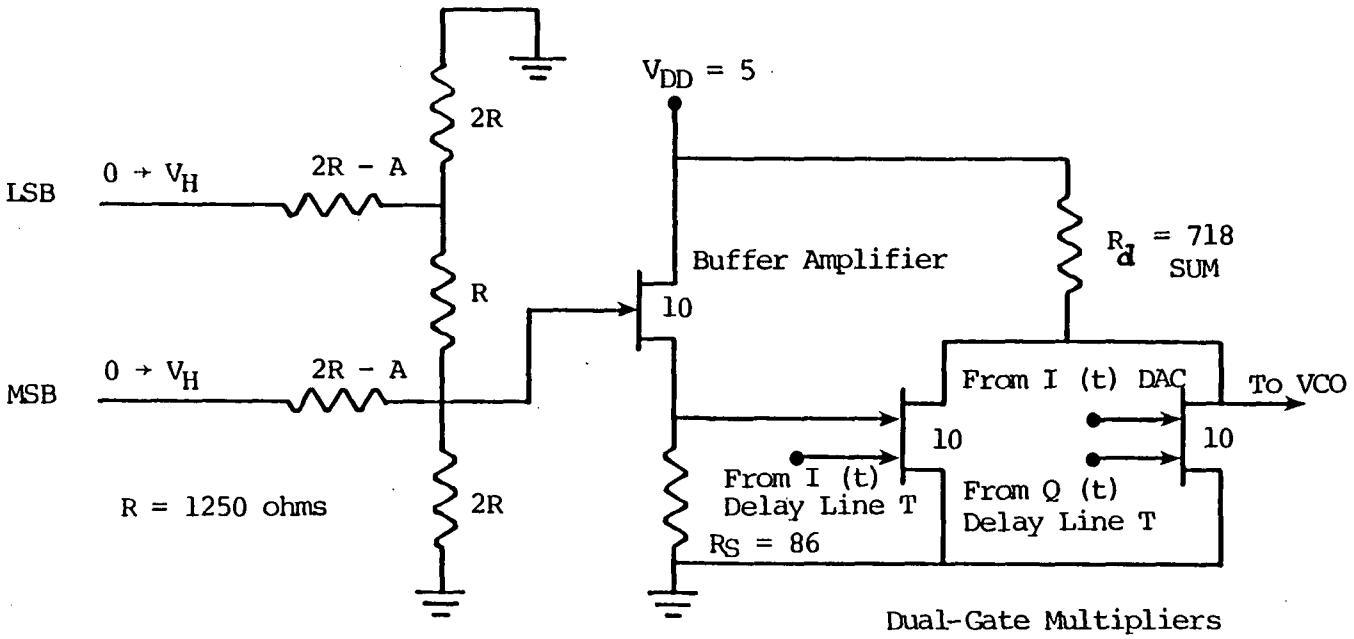


Figure 5.2.3, Ladder Network Digital-to-Analog Convertor and Dual-Gate Multipliers for E/DFL or SDFL

A = 75 ohms for SDFL, A = 100 ohms for E/DFL.

is determined by the switching FET "on" resistance given as R_{ON} = 56 ohms for SDFL and 82.6 ohms for E/DFL (as before) though here R is an estimate since the switch is not linear. Ideally, the logic outputs have equal pullup and pulldown capabilities. The "high" state impedances will be twice R_{ON} (112 or 165 ohms), while the low state impedances are two thirds R_{ON} (37.3 or 55 ohms) for SDFL and E/DFL respectively. This gives decoder output impedances of A $\pm$ B = 75 $\pm$ 19 ohms for SDFL and A $\pm$ B = 110 $\pm$ 55 ohms for E/DFL. To compensate for this source impedance the input resistors of this DAC should be decreased by A, as shown in figure 5.2.3. To further minimize the error voltages of this DAC, R should be chosen much larger than the impedance change of $\pm$ B. An R value of 1250 ohms will give maximum error voltages of about 3 and 4% for SDFL and E/DFL, which should be acceptable. The DAC output impedance is nearly a constant 625 ohms for R = 1250 ohms.

5.3 Buffer Amplifier The buffer amplifiers described here are similar to the one described in the section 5.6. The buffer amplifier for the E/DFL or SDFL DAC (shown in figure 5.2.3) and the DAC exclusively for E/DFL, are identical, except that the first case requires level-shifting diodes.

The buffer amplifier must provide the dual-gate multiplier with an input voltage swing of roughly $\pm$ 0.2 V about a nominal voltage of roughly 0 volts. This voltage is generated across the source resistor (R_S). The buffer amplifier for the SDFL case requires two level-shifting diodes (Δ V = 1.56 V) so that the nominal gate-source voltage (V_{gs}) is zero. Both amplifiers have V_{gs} given by $V_{gs} = 0 \pm 0.16$ V. This requires the nominal voltage across the source resistor to be 0.11 to 0.44 or $\overline{1.67}$ to 2 - 1.56 or $\overline{0.28}$ V (bar indicates mean).

The gate width and source resistor value are determined by first requiring that the input response correspond to less than a 50 ps time constant. The DAC has a maximum output impedance (all FETs on) of 1000 ohms while the amplifier input capacitance is $C_g = 1.26$ Z, as given in figure 3.5.7 with $V_P = 1.5$ and $N_d = 15 \times 10^{16} cm^{-3}$. So

$$RC_g \leq 50 \text{ ps} = 1000 \times 1.26 \text{ Z or } Z \leq 0.040 \text{ mm.}$$

The nominal voltage drop across the source resistor is 0.28 V. Then R_S is given by

$$0.28 = I_{DSS}R_S = 0.174 ZR_S \text{ or } R_S = 1.61/Z.$$

The gain is given by

$$G = R_s/(R_S + 1/g_m) = (1.61/Z)/(1.61/Z + 1/(0.149Z)) = 0.19$$

which is independent of the gate width. This gives an output signal of 0.28 $\pm$ 0.03 volts, which is an acceptable input to the multiplier circuit. Therefore there are no rigid constraints on the gate width. In order to reduce power dissipation, choose Z small, but not so small as to make a large output impedance for the multiplier or lead to fabrication tolerance problems. For Z = 10 um we have R_S = 1.61/0.01 = 161 ohms. The time constant is R C_g = 1000 x 1.26 x 0.01 pF = 12.6 ps. The total power dissipated is $V_{DD}I_{DSS}$ = 5 x 0.174 x 0.01 = 8.7 mW.

The buffer amplifier's gate width for the ladder network is chosen to be 10 um, for the same reasons as the two cases just mentioned. The input signal, from the ladder network, is about 0 to 0.3 volts depending on the logic types' characteristics. Therefore the average signal voltage is about 0.15 V. For the amplifier to have a nominal V_{gs} = 0 the source resistance, R_S, must generate an 0.15 volt source voltage at I_{DSS}. So,

$$0.15 = I_{DSS}R_S = 0.174 \times 0.01\ R_S \text{ or } R_S = 86 \text{ ohms.}$$

This gives the gain

$$G = 86/(86 + 1/(0.01 \times 0.149)) = 0.11.$$

The output signal voltage is then

$$0.15 \pm (0.11 \times 0.15) = 0.15 \pm 0.034 \text{ volts,}$$

which is a good output signal level and offset for proper multiplier operation. The input time constant of the buffer

with gate capacitance (C_g) and latter network resistance (R) is $RC_g = 1250 \times (1.26 \times 0.01)pf = 15.8$ pf. The total power dissipated is $V_{DD}I_{DSS} = 5 \times 0.174 \times 0.01 = 8.7$ mW.

5.4 Dual-Gate Multiplier The baseband processor carrier synchronization requires multiplication of the demodulated signal I(t) or Q(t) with the decision-based I(t) or Q(t) from the DAC (see figure 5.2.3). A dual-gate FET is used as the multiplier the same way as the dual-gate FET mixer in the bit timing circuit. See figure 2.2.2.

For proper multiplication, one gate is required to have a highly sloped, linear drain current which is a highly sloped linear function of the other gate voltage. That is, one gate is required to have a high transconductance proportional to the high transconductane of the other gate. A high transconductance allows the possibility for multiplication gain. As in the FET mixer analysis, refer to figures in Cripps et al, [2]. It can be seen that for the gate voltage at $V_{g2} = 0.22$, that there is a rather large constant slope, in drain current .vs. the gate 1 voltage (V_{g1}), for V_{g1} near zero. This operation point satisfies the above requirements.

The dual-gate FET multiplier in this work has one input from delay line "T" in (roughly) the 1 mV range and the other input (the gate closest to the drain) from the DAC with roughly 0.28 ± 0.03 volts. This is shown in figure 5.2.3. These two voltage inputs have been determined such that the multiplier would be in an adequate (wide input range, large output signal) operating region. Since the input and output voltage swings are small, the problem of having either of the gates operating in the triode region,

rather than the pinch-off region, is diminished. Analyzing the multiplier operation, via V_{gd} for each gate of the dual-gate FET, is complex. In practice the operation should involve a balancing effect on V_{gd}, making the channel current behavior .vs. change in gate voltage similar for each gate. With this in mind, the drain resistor is selected so that the drain voltage is $V_d = 2.5$, and each gate is operating at the lower end of the "active" region.

Notice that both of the multiplier FETs in the baseband processor share a common drain resistor. This is because both multiplier output products need to be summed. Summing is achieved by the voltage drop across the resistor from the sum of the two multipliers currents. The gain is independent of gate width for a fixed nominal drain voltage and fixed supply voltage (as described in sections 5.6 and 5.9). Therefore a small, and therefore less power hungry multiplier is chosen to have a gate width of 10 um which brings the total gate width of the two multipliers to 20 um. The value of the drain resistor needed for a 2.5 volt drop is given by

$$2.5\ V = I_{DSS}R = 0.174 \times 0.020\ R \text{ or } R = 718 \text{ ohms},$$

where I_{DSS} is given for a 0.7 um gate length device as described previously. The total power dissipated is

$$P = V_{PO}I_{DSS} = 5 \times 0.174 \times 0.01 = 8.7 \text{ mW}$$

for each multiplier.

5.5 Analog-to-Digital Converters (ADCs)

In the receiver end of the modem we need to convert the demodulated QASK signal into binary information using two 2-bit ADCs, one for each axis of the QPSK/QASK constellation.

Two recent papers by Upadhyayula et al and Curtice and Smith [52] present 2 and 3-bit BFL ADCs operating at GHz sampling rates. This is more than twice the sampling rate that is required in the baseband processor. The processor requires a 500 MSPS ADC (500 x 10^6 samples per second) corresponding to 1 Gbsp for QPSK mode and 2 Gbps for QASK mode. The ADC should not be expected to be the speed limiting operation (as will be shown). These high-speed BFL ADCs suggest the flexibility of using the slightly slower and less power hungry E/DFL or SDFL. The comparator and complete ADC circuit is shown in figure 5.5.1.

The principle of operation is for the output to change state when the input reaches the precise threshold level (V_T). The gate switching (threshold) voltage is determined by the gate width ratio of the switching FET to the load FET, and corresponds to the point at which both FETs can conduct equal current. This condition is met when

$$1 = I_{DS}/I_{DL} = K[(1 - n^{1/2})/(1 - n_s^{1/2})]$$

where $n_s = V_b/V_P$, $n = (V_g + V_b)/V_P$,

V_b = built-in Schottky barrier voltage;

V_P = channel pinch-off voltage;

K = width of the switch transistor divided by the

width of the load transistor and is not very sensitive to V_b.

The logic circuits respond to the comparator when the voltage crosses its threshold level (V_g). There exists a variability ΔV and Δt over which the comparators transition takes place. ΔV should be made about one-half V_t (of the LSB), or less, in order for proper state transition to occur within Δt. The rise and fall time of the comparator outputs are determined by the output node capacitance (C) and the available current (ΔI) for charging this capacitance. This capacitance is determined by the gate(s) capacitance of the next stage and the interconnect capacitance. So, $\Delta V/\Delta t = \Delta I/C$. Thus the rise and fall time is determined by the current drive capability of the comparator. For this circuit [52], ΔV ~ 3.0 V, C ~ 0.02 pF and with the requirement Δt = 100 ps, this gives ΔI = 0.6mA.

The output slope is determined by the comparator gain via $\Delta I = g_m \Delta V_g$. For the transition to occur for ΔV_g = 0.1 V with g_m = 6mS, it is required that ΔI = 0.6 mA [53]. Thus, having a large transconductance (g_m) will give higher resolution (smaller ΔV_g) for a given ΔI (or load) and that having a smaller load (node capacitance) will decrease the switching time and/or reduce the required switching current. The comparator circuits for the 2-bit ADC presented in [52] had the following parameters.

Operating Bias +7.5 V and -5.0 V

Device Pinch-Off Voltage ~ 5.0 V

Switching Speed ~ 100-150 ps

Gate Length ~ 1.0 um

Doping density ~ $1.0 \times 10^{17} cm^{-3}$

Power Dissipation/Comparator = 150-175 mW

Width of the Switching Transistor ~ 100 um

Epi thickness ~ 0.6 um

COMPARATOR DESIGN PARAMETERS FOR A 2-bit A/D

The comparators' FET width ratios [(Width of the Load FET)/(Width of the Switch FET)] are tabulated below for V_B = 0.4 V and 0.6 V and V_P = 5.0 V and 6.0 V.

Comparator	V_B =0.4 V		V_B = 0.6 V	
Threshold	V_P = 5.0 V	V_P = 6.0 V	V_P = 5 V	V_P = 6 V
0.4 V	0.837	0.856	0.845	0.865
0.8	0.711	0.745	0.720	0.756
1.2	0.606	0.652	0.612	0.661

The comparator threshold condition is given by:

$$\text{FET Load Width} = V_p^{1/2} - (V_g + V_b)^{1/2}$$

$$\text{FET Switch Width} = V_P^{1/2} - V_b^{1/2}$$

These equations, along with the above parameters, show that the effect of decreasing the pinch-off voltage, while maintaining the same gate threshold voltage, is to decrease the load to switch width ratio. This equation only restricts $V_P^{1/2}$ to be greater than $(V_G + V_B)^{1/2}$, therefore a FET with pinch-off voltages greater than 1.1 V is required for V_b ~ 0.78 V and our maximum threshold level is

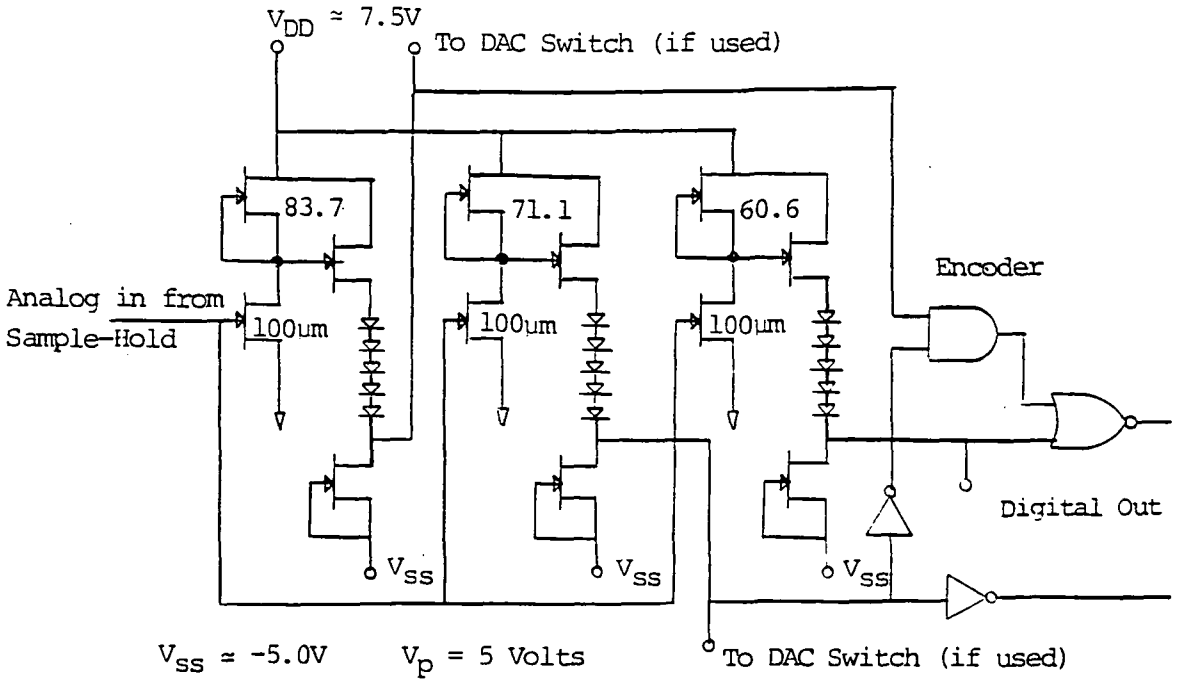


Figure 5.5.1, Analog-to-Digital Converter and Encoder for BFL
After [52]

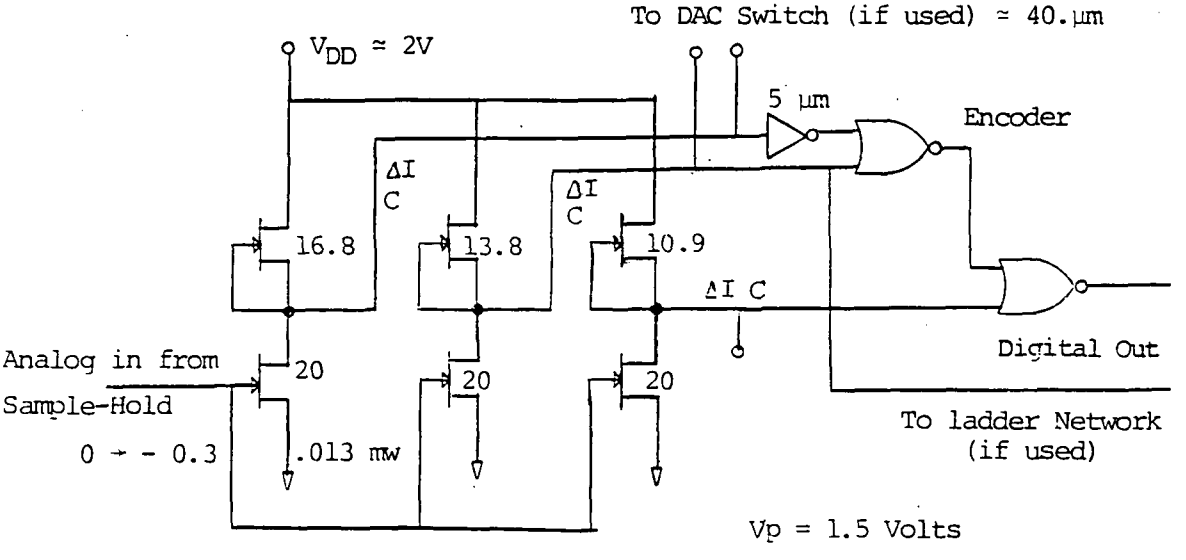


Figure 5.5.2, Analog-to-Digital Converter and Encoder for
E/DFL or SDFL

$V_T = V_g = 0.3$ V. In this work, the transceiver is expected to be fabricated with a pinch-off voltage of about $V_P \simeq 1.5$ V for either SDFL or the D-FETs of E/DFL. This satisfies the restriction on V_P. The comparator design is identical for either SDFL or E/DFL.

In considering the design of the ADC for $V_P = 1.5$ V, notice how the capacitance and transconductance varies with V_P according to the plots in figures 3.5.7 and 3.5.8. The capacitance increases by the square root while the transconductance increases by the sixth root for increasing V_P. So decreasing V_P about two thirds from 5 to 1.5 gives a switching speed degradation factor of about $1/\sqrt[3]{5/1.5} = 0.67$ for SDFL. But this degradation can be recovered by increasing the gain (width) of the switch transistor and minimizing the capacitive output load by decreasing the total gate width of the FETs of the next stage. The comparator load FET would have to be increased to maintain the desired threshold, i.e. maintain the appropriate width ratio K. The minimum output load is determined by the minimum gate width of the logic circuits, the DAC FETs (if used) and the interconnect capacitance. The minimum gate width of the logic circuits is determined by the speed constraint, that is, the point at which the interconnect capacitances become comparable to the gate capacitance (as discussed in the section on theory of operation of logic cicuits).

If we consider the output load of the comparators

to be determined by a 5 um buffer SDFL circuit and a 20 um DAC FET switch (worst case) both with V_P = 1.5 V, L_g = 0.7 mm and $N_d = 1.5 \times 10^{17}$, the effective load width is Z = 25 um, (from figure 3.5.3) for a = 0.145 um. Using equation (6), the FET switching capacitance is given by $C_g/Z \simeq 0.06\ L_g/a$ [21] so the capacitive load is

$$C_g = 0.06 \times 0.7 \times 0.025/0.145 = 0.0073 \text{ pF}.$$

Considering that there will be a minimum interconnect capacitance (C_i) roughly that of a 10 um FET (0.003 pF), a conservative estimate of the total capacitive load (C_L) on the comparators is $C_L \simeq C_i + C_g \simeq 0.01$ pF. If E/DFL is used (V_P = 0 for the 5 um FET) the capacitance will only be slightly higher.

For $N_d = 1.5 \times 10^{17} cm^{-3}$ and V_P = 1.5 we have the transconductance g_m/Z = 0.149. If a 20 um comparator switch is chosen, the transconductance is g_m = 0.003 mhos. Choosing threshold levels to be 0.1, 0.2 and 0.3 volts gives a 0.05 V transition region. The comparative switching current is then

$$\Delta I = g_m \Delta V_g = 0.003 \times 0.1 = 0.3 mA$$

for charging and discharging the load. With the comparators' available output current and load determined, the output switching time can be found as follows. The switching time is $\Delta t = \Delta V_1 C/\Delta I$ so

$\Delta t = 1.5 \times .01 \times 10^{-12}/0.0003 = 50$ ps which is an adequate switching time. The swing voltage ΔV_1 is somewhat less than the supply voltage V_{DD}.

In order to determine the threshold levels (0.1, 0.2 and 0.3 volts) for the 20 um switching FETs, the comparator loadwidths must be found. To determine the comparator load widths (Z_L) we use the threshold condition equation with switch width Z_S = 20 um, V_P = 1.5 V, V_b = 0.78 V and thresholds V_g = 0.1, 0.2 and 0.3 V.

$$Z_L = [(V_P^{1/2} - (V_G + V_B)^{1/2})/(V_P^{1/2} - V_B^{1/2})]Z_S$$
$$= 58.6\ (1.225 - (V_G + 0.78)^{1/2})\text{um}.$$

So Z_L = 16.8, 13.8 and 10.9 um for V_g = 0.1, 0.2 and 0.3 V respectively. The entire ADC, with decoders, for SDFL and E/DFL is shown in figures 5.5.2. NOR-gate implementation has been choosen for E/DFL since nor-gates are most easily fabricated with this logic type. The total average power dissiapated by the comparitors is

$$P = 0.5\ V_{DD}I_{DSS}(Z_{L1} + Z_{L2} + Z_{L3})$$
$$= 0.5 \times 2 \times 0.174(16.8 + 13.8 + 10.9) = 7.22\ \text{mW},$$

which is half the power dissipated if all the comparators are on.

5.6 Sample and Hold Circuits

In order for the quadrature demodulated signals (I(t) and Q(t)) to be properly digitized by the ADC, the ADC is preceeded by a sample/hold circuit which will hold the signal at a fixed level during the ADC process.

Barta and Rode [54] presented a GaAs sample and hold circuit (S/H) having potential application for giga-sample per second GSPS analog-to-digital conversion. This is twice the speed needed for this 500 MSPS modem. The circuit [54] consists of a cascaded 3-gate MESFET switch, a hold capacator and a wide-band feedback amplifier, as shown in figure 5.6.1. The novel three-gate switch configuration reduces the switch drive problems, when the outer two gates are grounded, by reducing the strobe blow-by (gate-drain coupling). It also has a low offset voltage when in the "on" state. The sample strobe pulse blow-by is reduced by applying the pulse to the middle gate so that the outer two grounded gates will serve as a shield (for the source terminal) for any of the strobe signal that could couple from the gate to the source and thus to the hold capacitor. The use of a rather fast 150 ps, -1.5 volt sample strobe pulse gives a rather large (35 mV) strobe blow-by even with the 5 to 10 times blow-by reduction of the two shielding gates. This blow-by can be further reduced by lengthening the transition time of the strobe pulse.

The hold capacitor is a metal-insulator-metal (MIM) structure consisting of 0.1 um of sputtered silicon

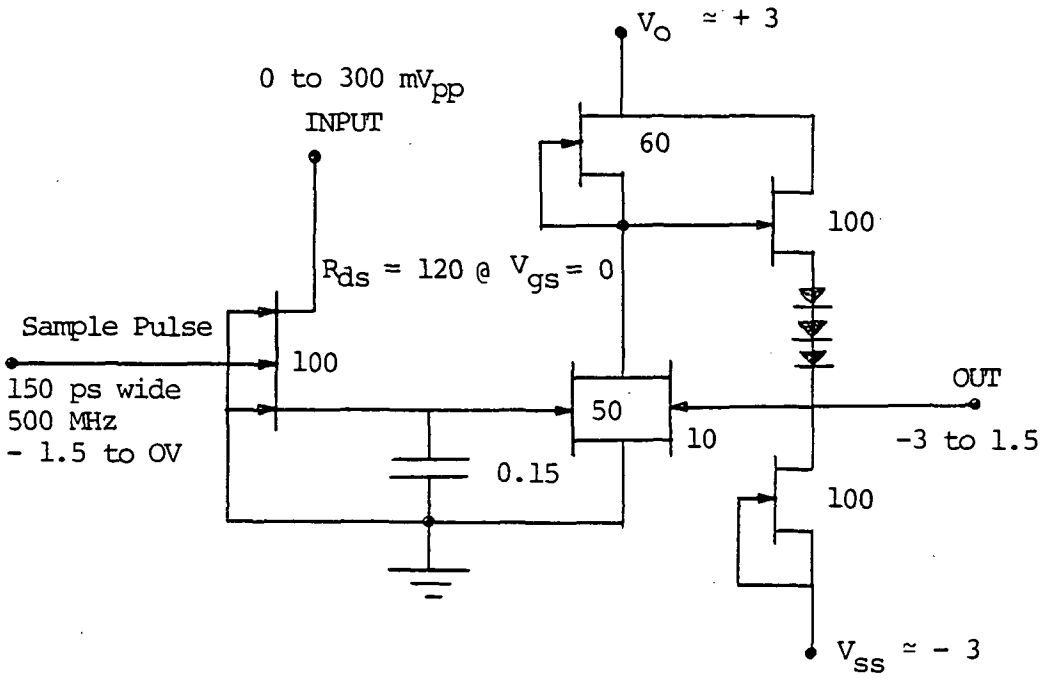


Figure 5.6.1, Sample and Hold Circuit, After [54]
Sample pulse is 150 ps wide, 500 MHz and -1.5 to 0V.
Specifications; Power = 100 mW, $V_p = -1.5V$
$I_{ds} \simeq 0.12$ A/mm and $g_m \simeq 0.132$ mhos/mm

nitride with a 20 volt breakdown voltage, 5 mA/mm^2 leakage rate to the substrate at -5 V (droop (fall) rate = 4 mV/ms), and 0.15 pF capacitance. The total hold capacitance (i.e. the hold capacitor, interconnect capacitance and amplifier gate capacitance) is 0.3 pF.

The amplifier FETs have the following characteristics. V_P = -1.5 V (ion implantation) I_{ds} = 120 mA/mm, g_m = 135 mS/mm, L_g = 1 um, R_{ON} (3 gate switch) - 120 ohms at V_{gs} = 0 and R_{off} isolation is apprpximately -40 dB. The gate widths, in microns, are labeled next to the FETs in the circuit diagram of figure 5.5.1.

A buffer amplifier is used, rather than a source follower, to eliminate the boot-straping effect of C_{gs}. Source-gate coupling can cause an error voltage on the gate and hold capacitor if the source voltage changes. With elimination of this boot-straping effect, a small hold capacitor can be used.

Two different sample and hold circuits designed for application in this work, are shown in figures 5.6.2.and 5.6.3. The first circuit is similar to the one presented by Barta and Rode with the principle difference being the gate width size (for power considerations) and DC output level tailoring of the buffer amplifier. To analyze this circuit, consider the output requirements then proceed toward the input in designing circuit elements that meet their respective output requirements. A DC return in this S/H

must be provided for long bit strings, either high or low state, therefore no coupling capacitors can be used in this circuit.

The four output signals will have voltage ranges--any positive to -0.1, -0.1 to -0.2, -0.2 to -0.3 and -0.3 to any negative. The output signal will ideally have voltage levels -0.05, -0.15, -0.25 and -0.35 volts, which are input to the comparators with the respective threshold levels -0.1, -0.2 and -0.3 volts. The circuit is designed for a mean signal level of -0.2 V with a range of 0.0 to -0.4 V.

In order for the amplifier to work properly the drain-source voltage (V_{ds}) should be kept greater than roughly $-V_p$ (1.5 V) so that the device is operating in the "pinch-off" or "saturation" region. Actually, the onset of the saturation region is slightly less than $-V_p$. But this configuration is relatively immune to these non-linearity problems because of the high gain (switch-like) nature of the feedback loop (discussed later). For this reason acceptable nominal values for V_{ds} are $V_{avg} - V_{SS} = 1.3$ V and $V_{DD} - V_{avg} = 5 - 1.56 = 3.44$ for the pulldown and pullup output FETs respectively. Two diodes are inserted to help balance the operating region (i.e. V_{dg}) of the two output FETs and to ensure that the V_{ds} of the input and feedback FETs are comparable to $-V_p$. The average voltages are shown in figure 5.6.2 at various nodes. The circuit is designed such that the average source-gate voltages (V_{sg}) are zero in

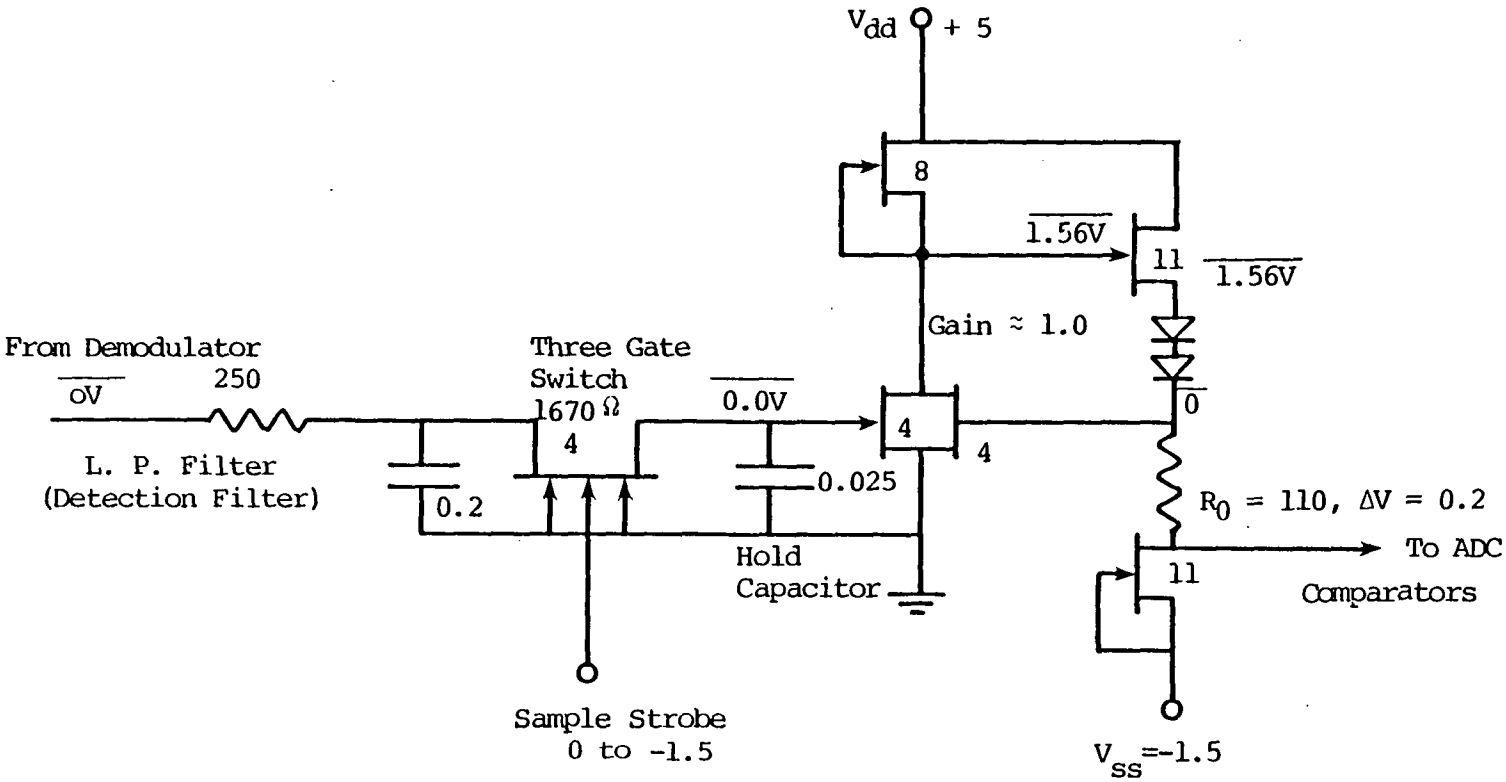


Figure 5.6.2, Sample and Hold Circuit

Figure shows from left to right, one pole of the detection filter followed by a three-gate switch and a hold capacitor for sampling and storing the analog signal while it is being digitized. This is followed by a high input impedance, low output impedance feed back buffer amplifier. Nominal output -0.3, -0.2 and -0.1 volts. Gate widths in microns.

order to help reduce nonlinear amplification effects. For this reason R_o is added to shift the output voltage from the gate feedback voltage, to -0.2 V.

The amplifier must drive a capacitive load consisting of the 20 um comparator gates of the ADC, the feedback gate capacitance (C_F) and interconnect line capacitance. The gate capacitance is determined by considering the gate similar to that of an amplifier, rather than a switch, since V_{sg} is small (0.3 V range below 0.0 V rather than a voltage swing of 0 to $-V_P$ = 1.5). The gate capacitance is a function of the gate voltage. (V_{sg} is considered zero for the amplifier analysis). So according to figure 3.5.7, C_g = 1.26 Z pF.

About L = 60 um of thin interconnect line, on h = 100 um of SI GaAs, is needed. From the section Phase Delays, this interconnect capacitance (as a line of charge) is roughly given as $C_i \simeq 10^{-6}(1/2h \times L)$ pF. The total load capacitance is then

$$C_L = 3C_g + C_F + C_i \simeq .26\ (3 \times 0.02 + 0.004) + 10^{-6}(1/2 \times 100 \times 60)$$

$$\simeq 0.0836 \text{ pF.}$$

The pullup and pulldown FET gate width Z is determined by the output switching time requirement Δt = 50 ps.

$$\Delta t = \Delta V C_L/\Delta I = \Delta V C_L/\Delta V_g g_m = C_L/g_m$$

$$= 0.0836\text{pF}/0.149Z$$

so Z = .0112 mm

For R_o to generate a 0.2 V shift

$$R_o = V_o/I_{dss} = 0.2/0.174\ Z = 109 \text{ ohms.}$$

This resistor has negligable effect on the switching speed.

The input FET and feedback FET are designed with gate widths equal to one half of pullup FET gate width so that together they draw the same current as the forward pullup FET. In the simplistic model, the channel current is ideally independent of the drain voltage for $V_{gs} > V_P$, so a small change in the input voltage would cause a full range swing of the drain-node voltage, if no feedback is provided. Further explanation is given in "Baseband Amplifier." The drain node switch time for Z = 0.008 mm is negligably small

$$\Delta t = C_g/g_m = 1.26 \times 0.0112 \text{ pF}/0.149 \times 0.08 = 1.2 \text{ ps.}$$

With equal coupling of the input and feedback voltage the gain is ideally G = 1. The gate widths were not chosen smaller because of fabrication tolerence considerations. For small gate widths, small errors in the widths would imbalance the currents through the input and feedback and forward pullup FET causing large output offset voltages.

The three-gate switch and the hold capacitor must both be smaller than that of G. Barta and A. Rode [50] so that it will not load the detection filter. Considering this, a total hold capacatance of 0.03 pF is sought. The input gate capacitance of the buffer amplifier is $C_g = 1.26 \times 0.004 = 0.005$ pF. Therefore the hold capacitor must be $C_H = 0.03 - 0.005 = 0.025$ pF. The area required for this capacitor is given by $C = 10^{-14}\text{F/mil}^2$ (determined in section

"Phase Delays"). So the area required is $.025 \times 10^{-12}/10^{-14}$ = 2.5 $mils^2$ (acceptable).

A time constant of 50 ps, for the 3-gate FET and hold capacitor, will give less than 1% error on the hold capacitor for a 250 ps sample strobe pulse. The 3-gate FET "on" resistance would be required to be R_{ON} = 50 ps/0.03 pF = 1666 ohms.

To determine the "on" resistance of the 3-gate FET switch, consider how it is designed. Assume that it is constructed similarly to that described for LNAs. The distance between all five contacts is 0.7 um and ion implantation of approximately $N^+ = 100 \times 10^{16} cm^{-3}$ is used, between and under the source and drain contacts, employing SAINT. Refering to the list of equations for MESFETs, the open channel resistance can be shown to be given by

$$R_{ON}Z = 2R_{co} + 4(R_2 + 2R_3) + 3R_C$$

$$R_{ON}Z = 2[2.1/(a_1{}^{.5}N_d{}^{.666})] + 4[(1.1 \times L_Z)/(a_2N^{+.82}) + 2[1.1L_3/(a_oN_d{}^{.82})] + 3[1.1L_g/(a_oN_d{}^{.82})]$$

where $a_1 = 0.25$, $N^+ = 100$, $N_d = 15$, $L_2 = 0.64$, $L_3 = 0.03$, $L_g = 0.7$, $a = 0.145$, $a_o = 0.0602$, $a_1 = 0.25$ and $a_z = 0.11$. This gives $R_{ON}Z = 6.61$. So for $R_{ON} = 1666$, Z = 4 um. The impedance of the sample and hold cicuit, as seen by the detection filter, is $Z_N = R + 1/sC = 1666 + j\ 10{,}600$ ohms and therefore will only slightly load the filter.

The sample strobe pulse blow-by can be estimated as follows. The gate-source capacitance of the switch is

proportional to $L_g^{2/3}$. If we assume that the differences in N_d and a, between Barta and Rodes design and the design in this work, do not cause a significant difference in C_{gs} (since V_P is the same (1.5) then the smaller gate length used in this work (0.7 um) results in $(1\text{ um})^{2/3}$ compared to $(.7\text{ um})^{2/3}$ or 0.79 reduction in $C_{gs}Z$. Since the gate width ratio is 0.004/0.1 = 0.04 and since the hold capacitance ratio is 0.03/0.3 = 10, that of G. Barta and A. Rode, then the total coupling reduction of the blow by is 0.04 x 10 = 0.4. So 0.4 x 35 mV = 14 mV of blow-by can be expected. Recall that this blow-by can also be reduced by reducing the strobe pulse edge sharpness. This blow-by should be negligible since it will last only about 150 ps [50], which is roughly the settling time of the ADC decoder.

The total power consumed by the entire sample and hold circuit is determined by the two drain currents of the buffer amplifier and the voltages across them.

So $P = I_{dss} V_{dd} + I_{dds}Z(V_{dd} - V_{ss})$

$= 0.174 \times 0.008\text{ um} \times 5\text{ V} + 0.174 \times 0.0112 \times (5 + 1.5)$

$= 19.6\text{ mV}$

This power dissipation is acceptably small.

Another form of the sample and hold circuit is shown in figure 5.6.3. This circuit is very different from the two previously described since it uses a common source amplifier followed by a source follower amplifier.

The source follower amplifier is used as an output device since it characteristically has a high input

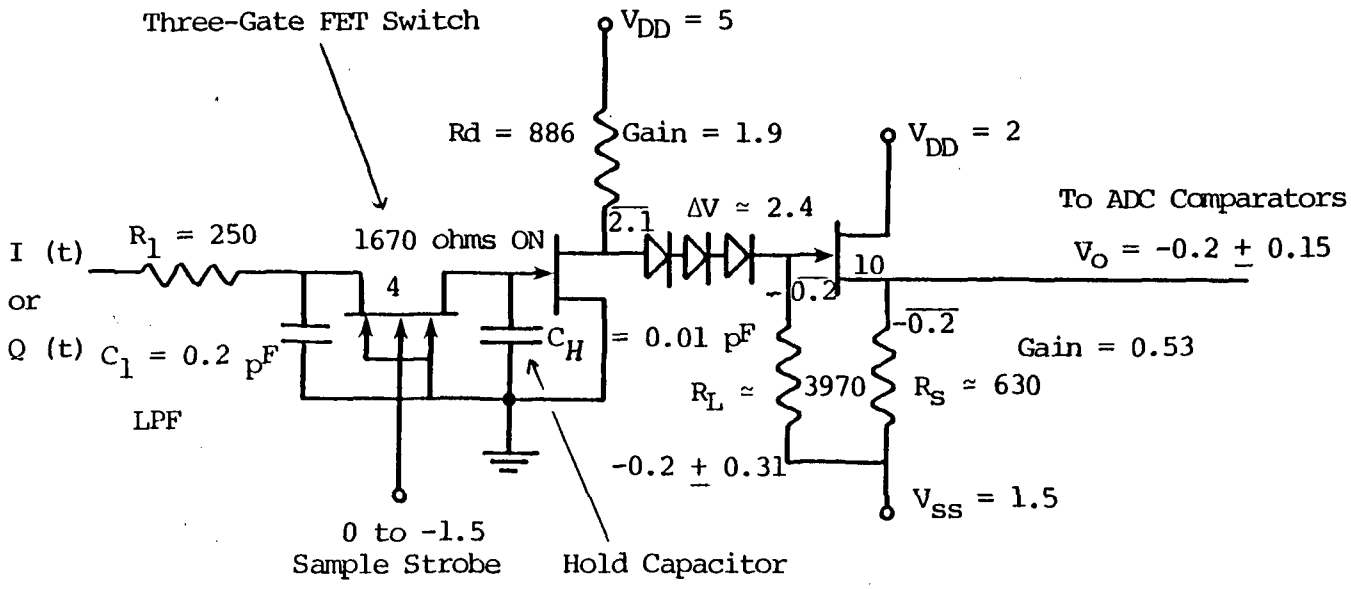


Figure 5.6.3, Sample and Hold Circuit
Figure shows another form of S/H circuit employing a source-follower rather than a feedback buffer amplifier.

impedance and a low output impedance. This amplifier can also be designed to have the DC output level match the levels of the ADC comparators unlike the common source amplifier (recall, no coupling capacitors can be used). The entire sample and hold circuit must invert the signal so the output amplifier is preceeded by the inverting common source amplifier. The common source amplifier is also necessary to eliminate the previously mentioned boot-straping effects.

The output drive and level requirements of this amplifier are the same as for the sample and hold circuit described previously.

To determining the buffer amplifier characteristics, first assume (with hindsight) that a 10 um gate width can be used. The source resistance is then determined by the average output voltage (V_o = -0.2 V) by $I_{DSS}R_s = V_o - V_{SS}$ or

$$R_s = (V_o - V_{SS})/I_{DSS} = 1.3/(0.174 \times 0.01 \text{ um})$$
$$= 747 \text{ ohms.}$$

The gain is independent of the gate width Z and is given by

$$G = R_S/(R_S + 1/g_m) = 747/(747 + 1/0.149 \times 0.01)$$
$$= 0.527.$$

The speed of this amplifier is determined by the load capacitance (C_L = 0.0836 pF as before) and output impedance. The output impedance is given by

$$R_{SF} = R_S/(R_S g_m + 1) = 747/(747 \times 0.149 \times 0.01 \text{ um} + 1)$$
$$= 353 \text{ ohms.}$$

This gives the output time constant

$$R_{SF}C_L = 353 \times 0.0836 \text{ pF} = 27.8 \text{ ps},$$

which is adequate for our signal with period 2000 ps. The error voltage is about 1% after 125 ps. This validates our original assumption that a 10 um wide gate will have sufficient drive capability.

The common source amplifier has no boot straping effects since changes in the gate voltage will not cause changes in the source voltage which would capacitively couple to the gate and thereby introduce an error voltage on the hold capacitor. The gain of this amplifier must be 1/0.527 = 1.9 to compensate for the gain lost in the source follower amplifier. The gain is given by

$G = -g_m(R_d||R_c||r_o)$ where r_o is considered infinite

So $G = 1.9 = 0.149Z(R_d||R_L)$

R_d is also determined by the requirement that $V_{gs} > V_P =$ 1.5 V for operation in the "active" region. Since the total gain is G = 1, the average gate voltage of the buffer amplifier is equal to that of the output (i.e. -0.2 V), the average output level of the common source amplifier must be shifted to -0.2 V. Three diodes in series are used to provide about 2.4 V shift. This determines the drain voltage to be -0.2 + 2.4 = 2.2 volts satisfying the condition that $V_{gd} > 1.5$.

The load resistance is determined by the switching time requirment $\Delta t = 50 \text{ ps} = R_L C_g$ where the subscript "g" indicates the buffer amplifiers 10 um wide gate. The output

resistance of the common source amplifier, looking back through the diodes, is not included in determining the switching time since the diodes will not conduct for a quickly decreasing signal. This specifies the switching time analysis as worst case. So

Δt (fall time) = 50 ps = $C_g R_L$ = 1.26 x 0.01 R_L pF or

R_L = 3968 ohms.

The expression for R_d is

V_d = 2.2 = $V_{DD} - R_d(I_{DSS} + I_L)$ or

2.2 = 5 - R_d (0.174Z + 1.3/3968) gives

R_d = 2.8/(0.174Z + 0.0003276)

Substituting this expression for R_d, into the expression for the gain, results in Z = 0.0163 mm and R_d = 886.4 ohms. The rise time =

$$\Delta V C_g/\Delta I = \Delta V C_g/(g_m \Delta V - \Delta V/R_L) = 5.8 \text{ ps.}$$

The three-gate switch and hold capacitor for this circuit are the same as for the sample and hold circuit described previously, with the exception that the hold capacitor is smaller because of the larger capacitance of the common source amplifier. The capacitance of the hold capacitor is

$$C_H = 0.03 \text{ pF} - C_g = 0.03 - 1.26 \times 0.0163 \tilde{-} 0.01 \text{ pF.}$$

The total power dissipated of the total sample and hold circuit is determined by the two amplifiers currents and voltages.

$P = \Delta V/R_d \times V_{DD}$ (common souce) + $(V_{DD} - V_{SS})I_{DSS}$ (source follower). So.

$$P = 2.8/1773 \times 5 + (2 + 1.5)0.174 \times 0.01 = 14 \text{ mW}.$$

5.7 Detection Filter

A two-pole detection filter, with a 3 dB roll off at the symbol frequency (500 MHz), is required after demodulation. This filter cannot be realized using two series RC filters immediately preceeding the sample-and-hold circuit because of both source loading problems and loading problems due to the sample-and-hold circuit. This problem is eliminated by incorporating one of the poles in the baseband amplifier and the other pole in a RC filter preceeding the sample and hold cicuit (see figures 5.6.2 and 5.6.3).

The transfer function of the filter is $H(f) = 1/(sRC + 1)^2$. At the 3 dB point $H(f) = 1/2$, $s = j2\pi f$, which gives $RC = 50.64$ ps. Values for R and C should be chosen such that the signal source loading and sample-and-hold circuit impedance is considered. Also, recall that high capacitances require precious chip real estate at about 1×10^{-14}F/(.001 in)^2. As a compromise of these factors R and C are chosen to be 253 ohms and 0.2 pF respectively. The resistance (R) should be decreased by an amount equal to the signal source impedance ($\simeq$ 40 ohms).

The capacitor area is 0.2×10^{-12}F/(1×10^{-14}F/mil^2) = 20 mils^2, which is an acceptable amount of chip area.

5.8 Baseband Amplifier

After the incoming RF signal is mixed with the LO, the resulting baseband signal level is roughly the same as the RF signal (≈ -43 dBm) and therefore requires amplification. Amplification is provided by three cascaded feedback amplifiers each with a voltage gain of about 5. The total voltage gain of the series is about 125 or $20 \log(125) = 42$ dB. The amplifier is shown in figure 5.8.1.

The amplifiers are DC-coupled so that there is no low-frequency pole. This allows for a long string of the same symbol to be received without the baseband signal voltage incuring decay of the static voltage level, as discussed in section 5.6 (Sample and Hold). Since the cascaded amplifier series and the sample-and-hold circuit will amplify any voltage relative to ground, the slightest offset from 0 volts of the dual-gate mixer's drain voltage will quickly be amplified to the point of saturating the amplifiers. This offset will also result in a large offset at the comparator of the ADC. This problem is remedied by including an offset-adjust capability via an external port. The offset-adjust is implemented by a 100 to 1 voltage divide circuit consisting of the dual-gate mixer's drain resistor (R_d) and a resistor of about $100R_d$ in series with the port. The offset-adjust sensitivity is such that the applied port voltage will roughly equal the offset appearing at the ADC comparators.

The principle of operation of the amplifiers has been shown in section 5.6. The amplifiers have an input gate width to feedback gate width ratio of five, giving a gain of roughly five. In addition to gain considerations the input and feedback gate widths are chosen according to amplifier's number of stages, power dissipation constraints, and fabrication tolerances.

The feedback amplifier described here (and in Sample and Hold) is actually a simplistic description. The gain of a common source amplifier is normally given by $G = g_m R_d$, where g_m is the transconductance of the input FET and R_d is the load resistor. A FET load resistor has non-linear source-drain resistance characteristics. The simplistic approach is based on the assumption that the load FET is a constant current source because it is operating in pinch-off region ($V_{gs} > V_P$) where the channel current is ideally independent of the source-drain voltage. This implies that R_L is infinite, giving the amplifier infinite gain (switch) if no feedback is provided. In practice R_L is usually finite, but it can even be negative, which would make the amplifier unstable. FET geometries, materials and operating point should be considered to determine R_d since it, and thus the level shift diodes, will probably cause reduced gain.

The complexity (or number of stages) is reduced with large input to feedback gate width ratios. The problem with large gate width ratios is that very small gate widths

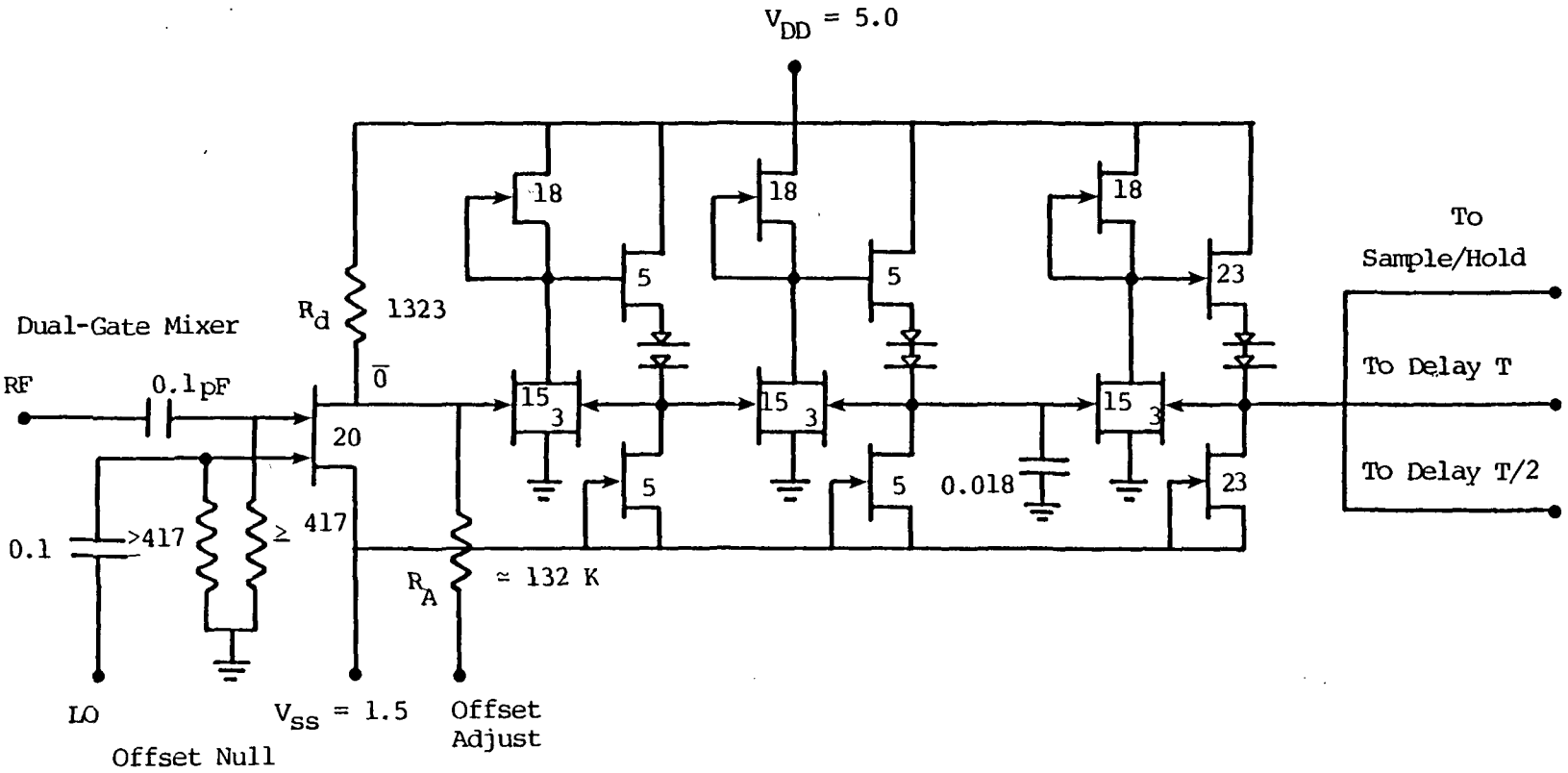


Figure 5.8.1, Baseband Amplifier and Dual-Gate Mixer

Amplifier employs 3 feedback amplifiers with total gain of ≃ 42
An offset-adjust port is included to prevent amplifier saturation
and to match the comparator input to the threshold levals.

are difficult to fabricate without introducing large chances for error in theoretical vs. actual operating characteristics and larger gate widths draw larger currents, quickly increasing power dissipation. A compromise of these factors determines the minimum gate width of 3 um and a maximum gate width of 15 um. The choice is justified by comparing by the power dissipated by a two, three, and four-stage amplifier each with a minimum gate width of 3 um and total gain of 125. The power dissipated is 81, 55 and 46 mW respectively. This includes the 21 um output FETs of the final stage. The decreased power of four-stage amplifiers compared to three-stage amplifiers is not considered worth the increased complexity.

Each stage of the amplifier's output FETs are chosen according to the desired frequency response of 25 ps (so as not to cause undesired filtering at the high end of the band). The first stage's response is determined by its output drive capability and its respective load. The load is the input gate capacitance of the second stage. The response (as previously shown) is given by

$$\Delta t = C_g/g_m \text{ or } 1.26 \times 0.015/(0.149 \times 0.005) = 25 \text{ ps.}$$

This high-speed response will not significantly effect the 500 MHz signal.

The final stage of the amplifier is required to drive two 150 ohm delay lines and the 253 + j1600 ohm detection filter. The amplifier output averages $\pm$ 0.2 V and is seen as a voltage source with a maximum current

determined by the gate width of the output FETs. With switch-like behavior, a forward biased pullup gate can supply more than twice I_{DSS} and the output can source and sink more than I_{DSS}. So for the above loads the gate width required is roughly
$Z = (0.2\ V)/((I_{DSS}/Z)(150||150||253)) = 23$ um and the power dissipation is (6.5 V) x I_{DSS} = 22mW, which is attractive. There is no standing wave problem in the delay line because of the delay line's high attenuation.

One pole of the two poles in detection filter consists of the second stage amplifier followed by capacitor C_F. The pole is inserted here because of circuit loading considerations as discussed in section 5.6. The pole must have the associated time constant of 50.6 ps given by $\Delta t = (C_F + C_g)/g_m$, where C_g is the input gate capacitance of the third stage amplifier and g_m is transconductance of the second stage's output FETs. This gives the capacitor size as

$$\begin{aligned} C_F &= \Delta t g_m - C_g \\ &= 50 \times 10^{-12} \times 0.149 \times 0.605 - 1.26 \times 10^{-12} \times 0.015 \\ &= 0.018\ pF. \end{aligned}$$

5.9 Dual-Gate Mixer

The dual-gate mixer is shown, along with the IF amplifier, in figure 5.8.1. The nonlinearity of FET mixing is the rapid change in the transconductane which allows for the possibility of conversion gain [1]. The dual-gate FET transconductance seen at the "RF" gate is a function of the LO signal applied to the "LO" gate.

In this work the dual-gate FET mixer operates in the pinch-off region since $|V_{gd}| \geq |V_P| = 1.5$ V. In the pinch-off region, the channel current is ideally a linear function of the gate voltage and is independent of the drain voltage. This implies that only one gate at a time will be predominantly controlling the channel current in the saturation mode, while the other gate will act as a small (preferably) variable resistance. The transconductance characteristics as a function of the gate voltages, and the conversion gain as a function of LO power, are given by Cripps et al 1979 [2] shown in figure 6.18. From these plots it can be seen that the maximum slope in transconductance occurs when both the RF and LO input gates have similar voltages, also, the larger V_{gs}, the higher the conversion gain. The plots [2] show that conversion gain is possible even for LO power levels as low as -20 dBm for a 10 GHz LO. The gate length is not given in [2].

The drain resistor and gate width of the dual-gate mixer is selected such that the nominal output offset voltage is zero volts. Recall that the gain of a

source-follower amplifier is

$$G = g_m(R_d||R_L||r_o) \tilde{=} g_m R_d = g_m \Delta V/I_{dss} = 4.2.$$

The transconductance g_m = 0.16 Z S/mm is given in figure 3.5.3 for $N_d = 15 \times 10^{16} cm^{-3}$, V_P = 1.5 V, L_g = 0.3 um, I_{DSS} = 0.19 Z and ΔV is the 5 volt drop across the drain resistor.

The output impedance (R_m) is required to give a 25 ps time constant with the capacitive load (C_g) of the first stage of the IF amplifier. This will also serve as a filter for any of the RF or LO signal coupled to the output. So $R_d C_g$ = 25 ps --> R_d = 25 ps/(1.26 x 0.015)pF = 1323 ohms.

The mixer gate width that gives a 5 volt drop across R_d is given by

$$R_d = 1323 = \Delta V/I_{DSS} = 5/(0.19\ Z) \text{ --> } Z = 20 \text{ um}.$$

The power dissipated is

$$(V_{DD} - V_{SS})\ I_{DSS} = 6.5 \times 0.19 \times 0.02 = 25 \text{ mW}.$$

In order for the mixer to operate properly both inputs are preceeded by DC blocking capacitors and offset nulling resistors. The capacitor size is chosen such that they dwarf the mixers gate capacitance so that most of the power is coupled to the gates and such that the capacitors do not occupy a large substrate area. According to figure 3.5.7 with V_P = 1.5, $N_d = 15 \times 10^{16} cm^{-3}$ and L = 0.3 um, the gate capacitance is 0.73 pF/mm x 0.02 mm = 0.0146 pF. Choosing a DC blocking capacitor (C_B) with 0.1 pF gives the effective mixer gate capacitance, which must be matched to,

as

$$C_m = (1/C_B + 1/C_g)^{-1} = 0.0127 \text{ pF.}$$

The offset nulling resistor is chosen such that it forms a pole at below 10 GHz.

$$\text{So } 2\pi RC = 2\pi\ 10^9\ R(C_o + C_g)$$

$$= 1 \text{ or } R \geq = 417 \text{ ohms.}$$

5.10 Oscillators

Highly stable 20 GHz local oscillators are required in both the QPSK/QASK modulator and demodulator. The demodulator's oscillator is required to have the flexability of controlled frequency variation (as a voltage controlled oscillator (VCO) enabling it to be phase locked to the incoming carrier.

Recently much attention has been given to high Q, high ϵ_r dielectrically stablized FET resonators particularly for 12 GHz satallite TV broadcasting. TV broadcasting applications require high frequency stability ($\pm$100 kHz) over a wide temperature range. This tight requirement and the need for compact, high efficiency, high Q, low FM noise oscillators has spurred investigations into dielectrically stablized FET resonators.

Typical oscillator constructions consist of suitable dielectric resonators (often ceramics) electromagnetically coupled to a microstrip line. The microstrip line is terminated in its characteristic impedance at one end and connected to the FET gate at the other end. The matched termination increases the oscillator stability by preventing spurrious oscillations from end-of-line reflections. The dielectric resonator serves as a band-reflection filter with the oscillation (reflection) frequency determined by the resonator and signal phase on the microstripline.

The resonant frequency can be adjusted by changing

the impedance (thus phase) on the microstrip line. Electronic tuning can be achieved by loading the line with the variable capacitance characteristics of varactor diodes. If a phase comparitor is used, with its output amplified and feedback to the varactor diode, the configuration is effectively a VCO.

Achieving good frequency/temperature-stability characteristics requires oscillator construction such that changes in frequency, due to temperature dependent circuit elements (almost linear), cancel with the changes in frequency due to the temperature dependent resonator characteristics. This necessitates the realization of a dielectric resonator with linear and adjustable frequency/temperature characteristics. At 10 GHz frequencies, most oscillator dielectrics have linear temperature coefficients over a wide temperature range but have minimiums or maximums at important frequencies [55]. For example, Barium Titanate (B_2Ti_9) has minimum at 0 to -10^{o} C and Titanium Zirconate has a maximum at 40-50^{o} C [55]. These deviations from linear behavior (minima or maxima) can be diminished by using resonators formed by combining (forming ceramics) or stacking two different dielectric materials. The characteristic minima or maxima, of each dielectric, is superceded by the other dielectric (in the composite resonator) which has linear frequency/temperature characteristics in that temperature region. Temperature compensation requires that the

microstrip's phase dependent coupling factor (reflection factor) be equal to the inverse power/temperature dependent coupling factor of the dielectric resonator. Complete temperature compensation is possible for only a certain spectrum of dielectric temperature coefficients with the restriction being maintaining the required output power [55]. Decreasing the coupling to the resonator increases the possibility for compensation but reduces the power at high temperatures [55]. A few examples of oscillator implementation follow.

Tsironis and Lesartre [6] have fabricated an 11.5 GHz dielectrically stablized oscillator with $\pm$120 kHz drift from -20^{o} to 80^{o} using stacked barium titanate and titanium zirconate. The resonator has 6 ppM/^{o}K frequency deviation but when used as compensating the oscillator gave an oscillator frequency stability of $\pm$0.1 ppM/^{o}K.

Komatsu, Murakami, Yamayuchi, Otobe and Hirabayashi [56] developed an 11.66 GHz, 14 mW, dielectrically stablized oscillator with $\pm$ 85 kHz drift from -20 to 60^{o}C without sacrificing power. This oscillator uses stacked zirconate ceramics and an FET with L_g = 1 um and Z = 300 um. The temperature coefficients of the zirconate ceramics are adjustable from -50 to +50 ppM/^{o}C by varying its composition. Here the resonator is fabricated using both cubic and orthrorhombic perovshite-type structure, zirconate ceramics giving ϵ_r = 30 and Q = 3000. The cubic structure tends to cancel the temperature dependence of the

orthrorhombic structure.

Mizumura, Wada, Aihasa and Haya [57] have developed a 20 GHz dielectrically stabilized FET oscillator with a frequency stablity of $\pm$15 ppM from 0°C to 50°C. The oscillator is fabricated with Ba (Zn 1/3 N_b 2/3)O_3 - Ba(Zn 1/3 Ta 2/3)O_3 (ϵ_r = 29.5, Q = 8000 unloaded and Q = 1000 loaded), an 0.5 um NE869275 (Z = 1500) and NE869475 (Z = 3000 mm) FETS. The output power is 15.6 dBm and 18.5 dBm, respectively, with 7.5% DC to RF conversion efficiency and 73 dB S/N at 1 kHz off the 10.5 GHz carrier frequency.

This oscillator (unlike that previously mentioned) operates by using the non-linear characteristics of the FET to double the fundamental dielectric resonator frequency (10 GHz) to the 20 GHz output frequency. Frequency doubling is employed because of the resonator's higher Q and higher stability at 10 GHz compared to 20 GHz.

The high frequency capabilities of FET oscillators are shown by Schellenberg, Yamasaki and Maki [58] in the development of 69 GHz oscillator. This oscillator uses a wave guide mounted FET with L_g = 0.5 um and Z = 2 x 75 um giving an output power of 2.5 mW at 57.3 GHz.

This survey on oscillators has shown that oscillators requiring high stability, as in this modem, cannot be achieved without stabilizing resonators. Although some methods of stabilizing oscillators employ wave guide cavities, they are bulky, have humidity and temperature

dependent resonance characteristics and appear to have little advantage over dielectric resonators.

Dielectrically stabilized FET oscillators are compact and have shown adequate performance, for use in the QPSK/QASK modem, but require dielectrics which cannot be manufactured along with the IC fabrication process. There appears to be no method for making stabilized resonators which are both suitable and compatable with the monolithic QPSK/QASK modem IC. This resonator is the only device type which is incompatable with the modem.

Under these circumstances, a practical way of achieving the oscillator function is to have a complete and separate oscillator external to the IC. This oscillator would require feedback circuitry (from the IC) needed to form a VCO. Another possible method involves fabricating the oscillator FET and phase control feedback circuit monolithically (along with the rest of the modem IC) while connecting the dielectric stablizer external to the IC. This method has the advantage of requiring fewer ports on the IC and a simpler external circuit. This complete system can be realized in a hybrid circuit fashion by mounting the dielectric stabilizer and the GaAs IC on a single microstrip line, dielectric substrate.

Conclusion

The material presented here has covered a wide range of monolithic GaAs applications and techniques in effort to explore the feasibility of realization of a high speed QPSK/QASK GaAs monolithic transceiver. The study began with a broad survey of recent available publishings on "state-of-art" GaAs devices applicable to the modem. The survey revealed that most GaAs device types had been achieved by exploiting GaAs capabilities to achieve that particular device with little consideration for compatability with other device types. Yet the realization of these achievements enabled a stratagy for modification of the device parameters to be made for multiple device type compatability.

Investigation of logic types revealed the potential compatability of both E/DFL and SDFL (and possibly a low pinch-off voltage BFL, if it is designed for very low power consumption). Further pursuit outlined the nature and performance requirements of the logic types and applicable logic circuit implementations.

A detailed look at FET channel characteristics showed that the common requirements of FET devices is low channel parasitic resistances through two primary techniques, N^+ ion implantation or the recessed gate technique. The channel characteristics, FET device composition, and device requirements were studied in depth

by formatting a comprehensive discussion including analytic expressions and performance plots with particular regard for LNAs. The results were applicable to other FET device types and allowed optimization by variation of the device constituencies.

With an understanding of the fundamental parameters for proper FET device operation, the functions compatible with monolithic implementation and required for realization of the modem, were sought, found and explored individually. It was shown that all of the functions, with the exception of a dielectrically-stablized L.O., could be achieved monolithically with lumped elements, distributed transmission lines, diodes and FETs. Not only were solutions found, but together they appear to form the best possible system implementation even compared to alternative hybrid forms.

Three QPSK/QASK modulators were designed, each having particular advantages over the other, but all showing acceptable performance potential to meet the requirements of the modem for throughput rates of 1 and 2 Gbps, and beyond. The three modulators were designed using transmission line couplers and either single-gate line switching FETs, switched dual-gate amplifiers or switched dual-gate BPSK modulators.

The receiver and baseband processor were designed on an elemental circuit level with each functional unit having an alternative form to add flexability for manufac-

turing requirements. All current and voltage levels are derived explicitly for each form. The system was explored using FETs with a pinch-off voltage of 1.5 V and power supplies of 2 and 5 volts. With these common parameters all device types were proven realizable.

Although the purpose of this work was not to explicitly design a complete system to such an extent as to be ready for layout and manufacture, the contents will serve as a guide or resource for a realizable design. The contents incorporates flexibility in fabrication techniques and circuit design approaches in order to accommodate most GaAs IC manufactures.

Throughout this investigation, exclusive emphasis is placed on finding recent published material to support any ideas involved in the design of this modem and to enhance the credibility of this work in the scientific community. Since the scope of this work is very broad, many details could not be included. For brevity, the most important references are cited though over 100 others were reviewed for better understanding of the subject matter. Likewise, not all the details in the discussion of each function type could be presented without lengthy repetition and so familiarization was assumed. But together with discussions of other functions, the contents of this work constitutes a comprehensive study of monolithic implementation of many device and functional unit types for implementation of a 1 or 2 Gbps QPSK/QASK transceiver.

Appendix

A summary of the required chip substate area and power follows. The values pertain to functions for use with 0.7 um SDFL, 2 V and -1.5 V supplies and $I_{DSS'} = 0.174$ Amperes/mm.

The areas occupied by FETS and diodes are determined by the gate width times 0.01 mm or by the maximum power dissipation of 0.02 Watts/mm^2. 50 ohm lines are 0.088 mm wide and have a 5.2 mm wave length at 20 GHz. Values which are given without specifications as to their origin are obtained explicitly from within the text. Capacitor areas are determined by 15.3 pF/mm^2.

The list shows that the chip substrate area is predominantly determined by the maximum power dissipation per unit area (particularly for the logic circuits) followed by areas occupied by couplers and capacitors.

Function	Devices	Derivation	Area (mm)	Power (watts)
Input logic	83 gates	83 x 0.5 x 0.008 x 0.174 A/mm x 3.5 V		0.200
		0.2 w/(0.02w/mm^2)	10	
Output logic	83 gates	same	10	0.200
Decoder	12 gates (5um)	12 x 0.005 mm x 0.174 A/mm x 3.5 V		0.027
		0.027w/(0.02w/mm^2)	1.35	
Modulator	4 hybrid couplers	4 x 1.5 $\lambda/4$ x 5.2mm/λ x 0.088 mm	0.686	
	5 power splitters	5 x 2 $\lambda/4$ x 5.2mm/λ x0.088	1.144	
	8 dual-gate FETs	0.08w/(0.2w/mm^2)	0.4	0.08
	switch capacitors	0.2mm x 0.01mm 2x2pF/(15.5pF/mm^2)	0.258	
	pads	5.2mm x 0.088mm	0.458	
RF Output Amplifiers		not determined	large	large
RF Input Amplifiers		not determined	large	large
Delay lines	2T + 2T/2	(T=2ns, 0.87mm^2), 3 x 0.87 mm^2	2.61	
2 DACs	gates & diodes	2 x 0.07mm x 0.01	0.0014	0.002
Buffer Amplifier	gates & diodes	2 x 0.02mm x 0.01	0.0004	0.017
2 Multipliers		2 x 0.02mm x 0.01	0.0004	0.017
2 Sample and Hold	source follower	2 x 0.035mm x 0.01	0.0007	0.028
	capacitors	$\frac{2(0.2pF+0.01pF)}{15.5\ pF/mm^2}$	0.027	

2 Baseband Amplifiers	gates & diodes	$0.11w/(0.02w/mm^2)$	5.5	0.11
	capacitors	$\frac{(0.1pF+0.1pF)x2}{15.5\ pF/mm^2}$	0.026	
2 Mixers	dual-gate	$0.05w/(0.02w/mm^2)$	2.5	0.05
	capacitors	$0.2pF/(15.5pF/mm^2)$	0.013	
		Total	34.97	0.531

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