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DATA AND RESULTS OF A LABORATORY INVESTIGATION OF MICROPROCESSOR UPSET CAUSED BY SIMULATED LIGHTNING-INDUCED ANALOG TRANSIENTS

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DATA AND RESULTS OF A LABORATORY INVESTIGATION OF MICROPROCESSOR UPSET CAUSED BY SIMULATED LIGHTNING-INDUCED ANALOG TRANSIENTS

by

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ABSTRACT

Advanced composite aircraft designs will include fault-tolerant computer-based digital control systems with high reliability requirements for adverse as well as optimum operating environments. Since aircraft penetrate intense electromagnetic fields during thunderstorms, onboard computer systems may be subjected to field-induced transient voltages and currents resulting in functional error modes which are collectively referred to as digital system upset. A methodology has been developed for assessing the upset susceptibility of a computer system onboard an aircraft flying through a lightning environment. Laboratory tests were performed to study upset error modes in a general-purpose microprocessor. The upset tests performed involved the random input of analog transients which model lightning-induced signals onto interface lines of an 8080-based microcomputer from which upset error data was recorded. The program code being executed on the microprocessor during tests was designed to exercise all of the machine cycles and memory addressing techniques implemented in the 8080 central processing unit. For specific processing states and operations, correlations are established between upset occurrence and transient signal inputs. The application of Markov modeling to upset susceptibility estimation is discussed and a stochastic upset susceptibility model for the 8080 microprocessor is presented to demonstrate stochastic model development.

INTRODUCTION

LIGHTNING STRIKES TO AIRCRAFT CAUSE transient voltages and currents to be induced on internal electrical cables throughout the aircraft. These transient signals can propagate to interface circuitry, power lines, etc., of onboard electronic equipment despite shielding and protection devices. Advanced composite aircraft provide less shielding than all metal aircraft and will utilize computer-based digital control systems that are inherently sensitive to transient voltages and currents. Since these digital systems will be performing flight-critical functions, highly reliable performance must be maintained in adverse environments such as thunderstorms. Therefore, techniques for assessing the susceptibility, performance, and reliability of digital systems when subjected to analog electrical transients must be developed.

Digital system upset collectively refers to functional error modes without component damage in digital computer-based systems and can be caused by lightning-induced electrical transients. An upset test methodology was developed and described in detail in (1)* along with initial data and results. In this paper, more extensive data and results of upset tests performed using this methodology are presented. The purpose of these tests is to statistically investigate the upset susceptibility of a general-purpose microcomputer executing an application program in a simulated lightning environment. The objective of the statistical analysis is to identify correlations between the occurrence of upset and the processing activity of the system (which includes software as well as hardware) that is in progress when input of an analog transient signal occurs. In addition, the analysis serves

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* Numbers in parentheses designate References at end of paper.

to demonstrate the application of upset susceptibility assessment techniques. These techniques could be used as an aid in identifying system weaknesses that could be hardened to upset but may be especially useful during the design phase of system development. The application of Markov modeling to upset susceptibility prediction for an upset tolerant system is discussed viewing upset caused by lightning as a random process and using test observations as a basis to demonstrate the development of an upset susceptibility model for the general-purpose microcomputer.

UPSET TEST METHODOLOGY

The upset test methodology is based on the comparison-monitoring of two synchronized Intel Intellec 8/Mod 80 microcomputers (μCs) executing identical program code concurrently. The Intellec 8 Mod/80 is a modular system based on the 8080 microprocessor (μP) and is configured for 8K bytes of random access memory (RAM), 4K bytes of programmable read-only memory (PROM), 4 input ports, and 4 output ports. The comparison monitor compares the 8-bit data bus, 16-bit address bus, and eight control lines from each Intellec 8 microcomputer and indicates that an error has occurred if a difference on any line is detected. One of the microcomputers is designated as the μC under test (μC UT) and the other microcomputer serves as a reference (REF μC) on which the comparison is made. A third microcomputer provides input data to the μC UT and REF μC, initiates interrupt requests, and is referred to as the I/O μC. The upset test hardware configuration is shown in figure 1.

The μC UT is perturbed by an analog transient signal. The analog electrical transient is a 1 MHz damped sinusoid of negative polarity, and was designed to model an electrical signal that could be induced by electromagnetic fields associated with lightning discharges. The waveshape of the transient signal is an approximation of a waveform recommended for lightning-induced

effects testing (2). The analog transient is directly coupled through a normally open relay onto a single line within the μC UT and its amplitude, therefore, is restricted to the damage threshold of components within the test unit. Input of the transient signal occurs pseudo-randomly in that it is controlled using the output of a counter that is initialized with a pseudo-random number generator. Randomness is desired so that the transient signal input is not synchronized with processing activity of the test unit. This establishes a more realistic laboratory simulation of the random process that might take place in the actual lightning environment than inputting transient signals during a processing activity that is established a priori. Therefore, data recorded from upset tests in which transient signal inputs occurred randomly during program execution, rather than by an a priori determination, should provide the best solution to a Markov upset susceptibility model.

Two types of data are obtained during each upset test--error data and the error detection time. Bit patterns from the data bus, address bus, and control lines of the μC UT are acquired with a Tektronix 9103 Digital Analysis System (DAS), which is triggered when the analog transient is input to the μC UT. If the comparison monitor indicates that an error occurred, the acquired error data is stored on magnetic tape. The DAS is then reset for another data acquisition. The error detection time is determined by counting the number of clock cycles that occur in the Intellec μC's from the input of the transient signal to the detection of an error. Since the Intellec μC's have a 2 MHz clock, the number of clock cycles is multiplied by 500 ns to obtain the error detection time. The error detection time is a function of the processing delay times within the system under test as well as the speed and efficiency of the comparison monitor, or error detector. Although there is very little literature on upset testing, work has recently been done on the development of monitors for upset detection (3).

UPSET TEST DESCRIPTION AND DATA SUMMARY

The program being executed on the μC UT and REF μC during upset tests was stored in PROM and a flow chart of this program and that of the I/OμC is shown in figure 2. The μC UT and REF μC set the stack pointer, initialize variables, output a preset constant to an I/O port, and input an 8-bit data word from the I/O μC. This 8-bit word is checked to see if it lies within a certain range. If the data word is not within the range, it is stored in memory and another 8-bit word is input to be checked. If the 8-bit word is in the range, it is divided by a constant and stored in memory. During these upset tests, the 8-bit data word was a constant within the desired range. The μC UT and REF μC then output another preset constant to an I/O port, retrieve from memory the 8-bit word resulting from the division, subtract a constant from it, and store this final value in memory. A loop in which no operations are performed is then executed until the I/O μC initiates an interrupt request which causes an RST 6 instruction (single-byte jump to memory location 0030) to be executed. The interrupt routine causes the final 8-bit value to be output to an I/O port. Once this is done, the μC UT and REF μC halt until the I/O μC initiates a second interrupt request which causes an RST 7 (single-byte jump to location 0038) to be executed. The second interrupt routine causes the μC UT and REF μC to reexecute the test program which, therefore, operates in a continuous loop. This test program was not written for efficiency or to perform some real application but to be representative of a typical application program and include instructions from all five 8080 instruction groups (table 1) that collectively require all ten 8080 machine cycles (table 2) and utilize all four memory addressing modes available in the 8080 (table 3).

The analog transient signal was input to the memory data input bus of the μC UT a total of 120 times--30 times each on the four least significant lines of the input data bus from memory (MDI0, MDI1, MDI2, MDI3). The memory data input bus is multiplexed onto the bidirectional data bus of the 8080 CPU (along with input data from the I/O ports and interrupt instructions from a peripheral device) and was chosen as the transient signal input site because transient signal inputs on this bus resulted in a large number of errors during the upset tests reported in (1). The specific lines within the bus as well as the number of transient signal injections per line were arbitrarily selected. Each of the 120 transient signal injections to the μC UT produced either upset or benign errors. Benign errors caused no divergence from correct flow between the main program and subroutines but included incorrect values read from or written to memory, repeated or erroneous states within an instruction cycle, and could be a potentially serious anomaly. For these tests, any divergence from correct program flow was classed as upset whether or not correct program execution was reestablished. Upsets recorded during testing occurred as a result of program execution returning from a subroutine to the wrong memory location, which in some cases was the second or third byte of a multibyte instruction. In some instances, program execution continued to the location at which the return should have occurred, and correct program flow resumed with or without benign errors for the duration of the data acquisition. In other cases, program execution went back and forth between two routines in an erroneous loop that was not exited within the time frame of the data acquisition. These findings are consistent with the upset characterization described in (4). The number of upsets and benign errors that occurred as a result of transient signal inputs at each of the four injection points is shown in table 4. Tables 5-7 show the number of upsets and benign errors that resulted from transient signal inputs during processing of the various instructions within each of the instruction

groups, the various memory addressing modes, and the various 8080 machine cycles, respectively.

STATISTICAL ANALYSIS

A statistical analysis was performed to identify processing modes of the 8080 μP that contain some types of activity which may be more critical than other types to the overall susceptibility of the μC system to upset caused by analog transients. A hypothesis test for each processing mode was performed in which the hypothesis being tested was that upset and benign errors occur with equal probability regardless of the processing activity underway when the transient signal is input to the μC UT. This hypothesis is tested by arranging in tabular form the number of observed upsets and benign errors resulting from transient inputs during each processing activity under consideration. A calculation of the expected value for each entry, assuming the hypothesis is true, is then performed which enables the chi-square statistic of the sample population to be calculated. If the calculated chi-square statistic is less than the actual value of an appropriate chi-square distribution, then the hypothesis is true. Otherwise, the hypothesis is not true and must be rejected.

Tables 8-10 show the observation tables, associated joint probabilities and conditional probabilities, and chi-square statistics for several instruction groups, addressing types, and machine cycles, respectively. Since, in each of these tables, the calculated chi-square statistic exceeds the value of the chi-square distribution, the hypothesis being tested in each of these cases must be rejected. This means that differences in the indicated probabilities are statistically significant rather than being due to chance. That is, it cannot be assumed that upset and benign error occurrences are equiprobable for transient signal inputs during execution of the various

instruction type, addressing modes, or machine cycles. The data base accrued during these tests is insufficient to identify which instruction groups, addressing modes, and machine cycles are most critical to upset vulnerability. This is because of the diversity in the relative frequency with which activities in each processing mode occurred during execution of the test program. There were activities in each processing mode that occurred so infrequently that they were underway few or no times when the transient signal was input to the μC UT. Identification of critical activities in each mode could be accomplished by additional tests using one or more specially written programs in which the relative frequencies of occurrence are more uniform.

To test the hypothesis that upset and benign error occurrences are equiprobable for transient signals injected on each of the four least significant lines of the memory data input bus, the chi-square statistic shown in table 11 was calculated. Since the calculated chi-square statistic is less than the value of the chi-square distribution, the hypothesis cannot be rejected. That is, upset and benign error occurrences are equally probable regardless of the line (among the four least significant bits of the input data bus from memory) on which the transient signal is injected.

The overall performance of the 8080-based microcomputer can be conveniently summarized in a Markov chain of discrete states as shown in figure 3. The state transition probabilities θ_{ij} are defined as

$$\theta_{ij} = P(i \rightarrow j \mid \text{state } i) = \frac{N_{ij}}{N_i} \qquad <1>$$

where N_{ij} is the number of observed transitions from state i to state j and N_i is the number of times state i was observed. The quantities θ_{ij} represent the probability of transition along the indicated path and do not represent state probabilities or provide information regarding transition sequence.

STOCHASTIC MODELING

In order to obtain a probabilistic time history of the 8080-based system response to the analog transient, a stochastic Markov model could be constructed consisting of discrete states in continuous time. The states and transition paths would be the same as those shown in figure 3. However, the transition paths would be defined in terms of transition rates λ_{ij} rather than probabilities θ_{ij}. If constant transition rates were assumed, λ_{ij} would be the inverse of the mean transition time from state i to state j, which would have to be determined experimentally or using computer simulation (5). Transition time between states could be evaluated by counting the elapsed number of clock cycles and dividing by the clock frequency. Transition rates λ_{ij} could also be estimated with the θ_{ij} by solving the simultaneous equations:

$$\frac{\hat{\lambda}_{12}}{\hat{\lambda}_{12} + \hat{\lambda}_{13}} = \theta_{12} \qquad \langle 2 \rangle$$

$$\frac{\hat{\lambda}_{13}}{\hat{\lambda}_{12} + \hat{\lambda}_{13}} = \theta_{13} \qquad \langle 3 \rangle$$

$$\frac{\hat{\lambda}_{21}}{\hat{\lambda}_{21} + \hat{\lambda}_{13}} = \theta_{21} \qquad \langle 4 \rangle$$

$$\frac{\hat{\lambda}_{23}}{\hat{\lambda}_{21} + \hat{\lambda}_{23}} = \theta_{23} \qquad \langle 5 \rangle$$

$$\frac{\hat{\lambda}_{31}}{\hat{\lambda}_{31} + \hat{\lambda}_{32}} = \theta_{31} \qquad \langle 6 \rangle$$

$$\frac{\hat{\lambda}_{32}}{\hat{\lambda}_{31} + \hat{\lambda}_{32}} = \theta_{32} \qquad \langle 7 \rangle$$

Once all transition rates have been determined, a transition rate matrix Q would be formulated:

$$Q = [q_{ij}] = \begin{bmatrix} -(\lambda_{12} + \lambda_{13}) & \lambda_{12} & \lambda_{13} \\ \lambda_{21} & -(\lambda_{21} + \lambda_{23}) & \lambda_{23} \\ \lambda_{31} & \lambda_{32} & -(\lambda_{31} + \lambda_{32}) \end{bmatrix} \quad \langle 8 \rangle$$

The transition rate matrix Q would then be used to determine the probability, $P_{ij}(t)$, of occupying state j at time t given that the process was in state i. This probability is the solution to the following system of differential equations (6):

$$P'_{ij}(t) = \sum_k q_{ik} P_{kj}(t) \quad \langle 9 \rangle$$

with initial conditions

$$P_{ij}(0) = \begin{cases} 1 \text{ if } i = j \\ 0 \text{ if } i \neq j \end{cases} \quad \langle 10 \rangle$$

The time-varying state probabilities $P_{ij}(t)$ for the Markov model constructed as in figure 3 represent a characterization of the upset susceptibility of the 8080-based microcomputer. Since this system was not designed for upset tolerance, upset detection and recovery states cannot be added to the model for a reliability characterization. However, stochastic modeling could be used to characterize the susceptibility of the digital system to upset.

SUMMARY AND CONCLUSIONS

A laboratory experiment was conducted, using a general-purpose microcomputer, to investigate upset caused by analog electrical transients similar to those that could be induced by lightning. Data was obtained from 120 tests in which 85 upsets and 35 benign errors were detected. Error modes involving a divergence from correct program flow was classed as upset. Benign errors caused no divergence from correct flow between the main program and subroutines but included incorrect values read from or written to memory,

repeated or erroneous states within an instruction cycle, and could be a potentially serious anomaly. A statistical analysis was performed in which it was determined that upset and benign error occurrences are not equiprobable for transient signal inputs during execution of the various instruction types, addressing modes, or machine cycles. Additional testing would have to be performed to identify which instruction groups, addressing modes, and machine cycles are most critical to upset vulnerability. This type of analysis could be used as an aid in identifying system weaknesses that could be hardened to upset but may be especially useful during the design phase of system development. A stochastic model, based on upset test data, was defined for the general-purpose microcomputer assuming constant transition rates. Solution of this model would provide time-varying state probabilities that represent an upset susceptibility characterization of the test system. Thus, the application of stochastic modeling for upset susceptibility prediction seems very promising. However, the optimum transition rate distribution must be determined.

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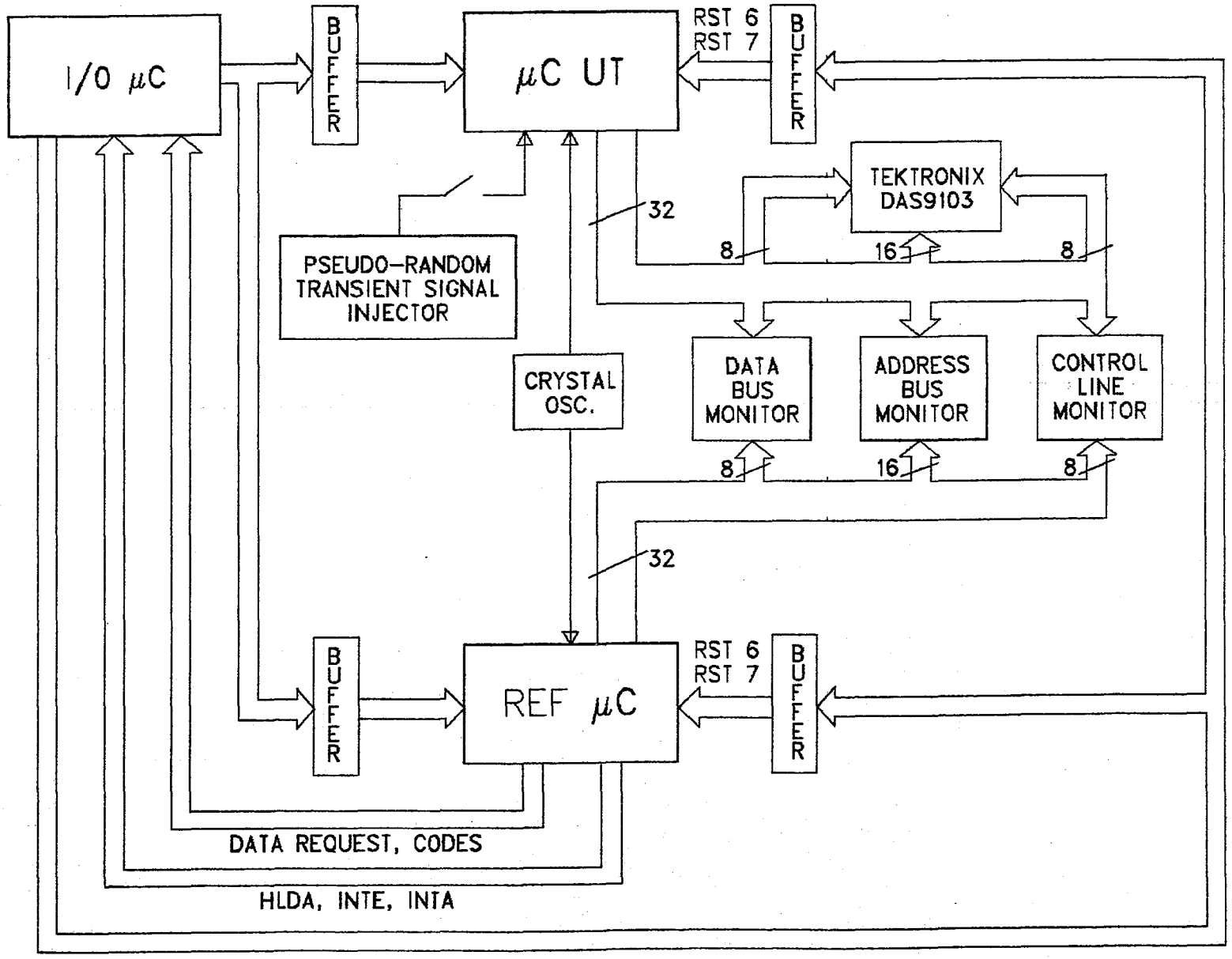
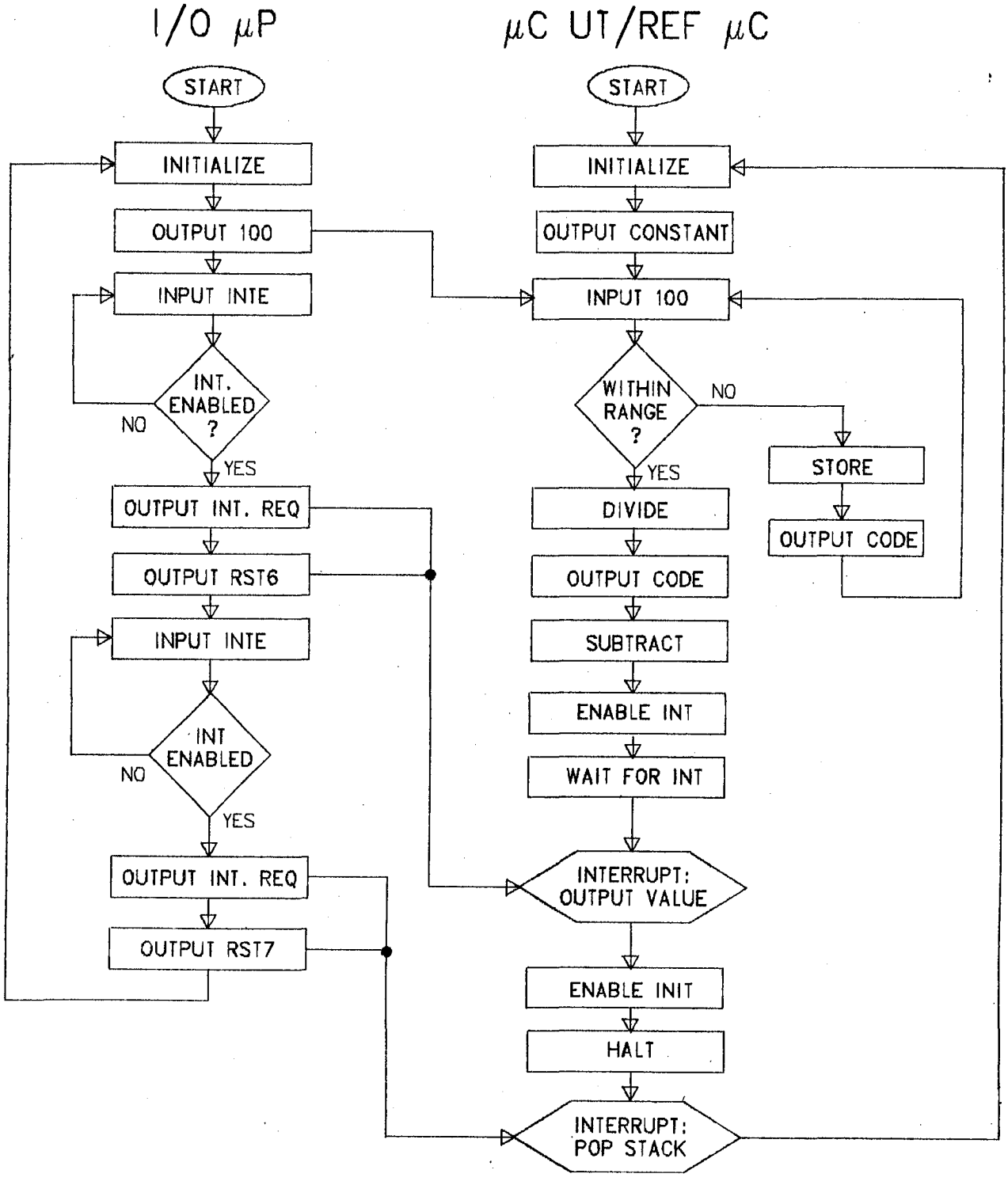
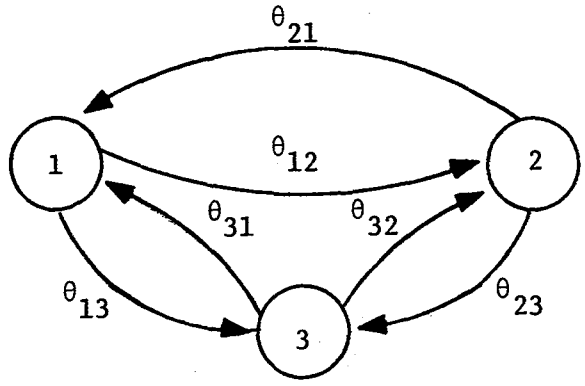


FIGURE 1: UPSET TEST HARDWARE CONFIGURATION

FIGURE 2: FLOW CHART OF UPSET TEST µC PROGRAMS





STATE 1: SYSTEM IS FAULTED BY TRANSIENT SIGNALS

STATE 2: UPSET HAS OCCURRED

STATE 3: BENIGN ERRORS HAVE OCCURRED

$\theta_{12} = 0.017$ $\theta_{21} = 0.024$ $\theta_{31} = 0.153$

$\theta_{13} = 0.983$ $\theta_{23} = 0.224$ $\theta_{32} = 0.606$

FIGURE 3: STATE MODEL FOR INTELLEC 8/MOD 80 SYSTEM RESPONSE
RESPONSE TO ANALOG TRANSIENT SIGNAL

TABLE 1: 8080 INSTRUCTION GROUPS

GROUP	DESCRIPTION
DATA TRANSFER	MOVE DATA BETWEEN REGISTERS OR BETWEEN REGISTERS AND MEMORY
ARITHMETIC	ADD, SUBTRACT, INCREMENT, DECREMENT DATA IN REGISTERS OR MEMORY
LOGICAL	AND, OR, EXCLUSIVE-OR, COMPARE, ROTATE, COMPLEMENT DATA IN REGISTERS OR MEMORY
BRANCH	CONDITIONAL/UNCONDITIONAL JUMP, SUBROUTINE CALL, RETURN
STACK, I/O, AND MACHINE CONTROL	INPUT, OUTPUT, MAINTAINING STACK AND INTERNAL CONTROL FLAGS

TABLE 2: 8080 MACHINE CYCLES

MACHINE CYCLE	DESCRIPTION
INSTRUCTION FETCH	READ INSTRUCTION FROM MEMORY; INCREMENT PROGRAM COUNTER; DECODE INSTRUCTION
MEMORY READ	READ BYTE FROM MEMORY; INCREMENT PROGRAM COUNTER
MEMORY WRITE	WRITE BYTE TO MEMORY
STACK READ	READ BYTE FROM STACK; INCREMENT STACK POINTER
STACK WRITE	WRITE BYTE TO STACK; DECREMENT STACK POINTER
INPUT READ	READ BYTE FROM INPUT PORT
OUTPUT WRITE	WRITE BYTE TO OUTPUT PORT
INTERRUPT ACKNOWLEDGE	READ INSTRUCTION ON DATA BUS; DECODE INSTRUCTION
HALT ACKNOWLEDGE	CPU ENTERS HALT STATE
INTERRUPT ACKNOWLEDGE WHILE HALTED	READ INSTRUCTION ON DATA BUS; DECODE INSTRUCTION

TABLE 3: 8080 ADDRESSING MODES

MODE	DESCRIPTION
DIRECT	BYTES 2 AND 3 OF THE INSTRUCTION CONTAIN THE EXACT ADDRESS OF DATA
REGISTER	THE INSTRUCTION SPECIFIES THE REGISTER OR REGISTER-PAIR CONTAINING DATA
REGISTER INDIRECT	THE INSTRUCTION SPECIFIES THE REGISTER-PAIR CONTAINING ADDRESS OF DATA
IMMEDIATE	THE INSTRUCTION CONTAINS THE DATA ITSELF

TABLE 4: NUMBER OF UPSETS AND BENIGN ERRORS THAT OCCURRED PER INJECTION POINT

INJECTION POINT	NO. OF INJECTIONS	NO. OF UPSETS	NO. OF BENIGN ERRORS
MDI0	30	22	8
MDI1	30	25	5
MDI2	30	21	9
MDI3	30	17	13
	120	85 (71%)	35 (29%)

TABLE 5: NUMBER OF UPSETS AND BENIGN ERRORS THAT OCCURRED PER INSTRUCTION GROUP

INSTRUCTION GROUP	NO. OF UPSETS	NO. OF BENIGN ERRORS
DATA TRANSFER	7	3
ARITHMETIC	3	4
LOGICAL	0	2
BRANCH	52	14
STACK, I/O, AND MACHINE CONTROL	23	12

TABLE 6: NUMBER OF UPSETS AND BENIGN ERRORS THAT OCCURRED PER ADDRESSING MODE

ADDRESSING MODE	NO. OF UPSETS	NO. OF BENIGN ERRORS
DIRECT	1	4
REGISTER	1	2
REGISTER INDIRECT	15	6
IMMEDIATE	47	12
NONE	21	11

TABLE 7: NUMBER OF UPSETS AND BENIGN ERRORS THAT OCCURRED PER MACHINE CYCLE TYPE

TYPE OF MACHINE CYCLE	NO. OF UPSETS	NO. OF BENIGN ERRORS
INSTRUCTION FETCH	27	10
MEMORY READ	36	8
MEMORY WRITE	4	1
STACK READ	2	1
STACK WRITE	5	2
INPUT READ	0	0
OUTPUT WRITE	1	0
INTERRUPT ACKNOWLEDGE	0	0
HALT ACKNOWLEDGE	10	9
INTERRUPT ACKNOWLEDGE WHILE HALTED	0	4

TABLE 8: STATISTICS FOR UPSET AND BENIGN ERROR OCCURRENCE PER INSTRUCTION GROUP

	C_1 BRANCH	C_2 STRK, I/O, MC	C_3 OTHERS	TOTAL
BENIGN ERRORS	14	12	9	35
UPSET	52	23	10	85
TOTAL	66	35	19	120

$P_{B,U}(C_i)$: PROBABILITY THAT A CATEGORY i INSTRUCTION IS BEING EXECUTED WHEN THE UPSET/BENIGN ERROR-CAUSING TRANSIENT SIGNAL IS INPUT

$P_B(C_1) = 0.117$ $P_B(C_2) = 0.100$ $P_B(C_3) = 0.0750$

$P_U(C_1) = 0.433$ $P_U(C_2) = 0.192$ $P_U(C_3) = 0.0833$

$P(B, U/C_i)$: PROBABILITY OF UPSET/BENIGN ERROR OCCURRENCE GIVEN THAT A CATEGORY i INSTRUCTION IS BEING EXECUTED DURING TRANSIENT SIGNAL INPUT

$P(B/C_1) = 0.212$ $P(B/C_2) = 0.343$ $P(B/C_3) = 0.474$

$P(U/C_1) = 0.788$ $P(U/C_2) = 0.657$ $P(U/C_3) = 0.526$

CALCULATED CHI-SQUARE STATISTIC: $X^2 = 5.51$

(TABLE VALUE: $X^2_{\alpha = 0.10} = 4.61$)

TABLE 9: STATISTICS FOR UPSET AND BENIGN ERROR OCCURRENCE PER ADDRESSING MODE

	C_1 IMMEDIATE	C_2 NONE	C_3 OTHERS	TOTAL
BENIGN ERRORS	12	11	12	35
UPSET	47	21	17	85
TOTAL	59	32	29	120

$P_{B\ U}(C_i)$: PROBABILITY THAT THE CATEGORY i ADDRESSING MODE IS BEING EXECUTED WHEN THE UPSET/BENIGN ERROR-CAUSING TRANSIENT SIGNAL IS INPUT

$P_B(C_1) = 0.100$ $P_B(C_2) = 0.0917$ $P_B(C_3) = 0.100$

$P_U(C_1) = 0.392$ $P_U(C_2) = 0.175$ $P_U(C_3) = 0.142$

$P(B, U/C_i)$: PROBABILITY OF UPSET/BENIGN ERROR OCCURRENCE GIVEN THAT THE CATEGORY i ADDRESSING MODE IS BEING EXECUTED DURING TRANSIENT SIGNAL INPUT

$P(B/C_1) = 0.203$ $P(B/C_2) = 0.344$ $P(B/C_3) = 0.414$

$P(U/C_1) = 0.797$ $P(U/C_2) = 0.656$ $P(U/C_3) = 0.586$

CALCULATED CHI-SQUARE STATISTIC: $X^2 = 4.72$

(TABLE VALUE: $X^2_{\alpha= 0.10} = 4.61$)

TABLE 10: STATISTICS FOR UPSET AND BENIGN ERROR OCCURRENCE PER MACHINE CYCLE TYPE

	C_1 INST. F	C_2 MEM. R.	C_3 OTHERS	TOTAL
BENIGN ERRORS	10	8	17	35
UPSET	27	36	22	85
TOTAL	37	44	39	120

$P_{B,U}(C_i)$: PROBABILITY THAT THE CATEGORY i MACHINE CYCLE IS BEING EXECUTED WHEN THE UPSET/BENIGN ERROR-CAUSING TRANSIENT SIGNAL IS INPUT

$P_B(C_1) = 0.0833$ $P_B(C_2) = 0.0667$ $P_B(C_3) = 0.142$

$P_U(C_1) = 0.225$ $P_U(C_2) = 0.300$ $P_U(C_3) = 0.183$

$P(B, U/C_i)$: PROBABILITY OF UPSET/BENIGN ERROR OCCURRENCE GIVEN THAT THE CATEGORY i MACHINE CYCLE IS BEING EXECUTED DURING TRANSIENT SIGNAL INPUT

$P(B/C_1) = 0.270$ $P(B/C_2) = 0.182$ $P(B/C_3) = 0.436$

$P(U/C_1) = 0.730$ $P(U/C_2) = 0.818$ $P(U/C_3) = 0.564$

CALCULATED CHI-SQUARE STATISTIC: $X^2 = 6.51$

(TABLE VALUE: $X^2_{\alpha = 0.05} = 5.99$)

TABLE 11: STATISTICS FOR UPSET AND BENIGN ERROR OCCURRENCE PER TRANSIENT SIGNAL INPUT POINT

	C_1 MDI0	C_2 MDI1	C_3 MDI2	C_4 MDI3	TOTAL
BENIGN ERRORS	8	5	9	13	35
UPSETS	22	25	21	17	85
TOTAL	30	30	30	30	120

$P_{B,U}(C_i)$: PROBABILITY OF UPSET/BENIGN ERROR OCCURRENCE GIVEN THAT THE INPUT POINT OF TRANSIENT SIGNAL BELONGS TO CATEGORY i

$P_B(C_1) = 0.267$ $P_B(C_2) = 0.167$ $P_B(C_3) = 0.300$ $P(B/C_4) = 0.433$

$P_U(C_1) = 0.733$ $P_U(C_2) = 0.833$ $P_U(C_3) = 0.700$ $P(U/C_4) = 0.567$

CALCULATED CHI-SQUARE STATISTIC: $X^2 = 5.28$

(TABLE VALUE: $X^2_{\alpha = 0.10} = 6.25$)

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16. Abstract

Advanced composite aircraft designs will include fault-tolerant computer-based digital control systems with high reliability requirements for adverse as well as optimum operating environments. Since aircraft penetrate intense electromagnetic fields during thunderstorms, onboard computer systems may be subjected to field-induced transient voltages and currents resulting in functional error modes which are collectively referred to as digital system upset. A methodology has been developed for assessing the upset susceptibility/reliability of a computer system onboard an aircraft flying through a lightning environment. Laboratory tests were performed to study upset error modes in a general-purpose microprocessor. The upset tests performed involved the random input of analog transients which model lightning-induced signals onto interface lines of an 8080-based microcomputer from which upset error data was recorded. The program code being executed on the microprocessor during tests was designed to exercise all of the machine cycles and memory addressing techniques implemented in the 8080 central processing unit. A statistical analysis is presented in which possible correlations are established between the probability of upset occurrence and transient signal inputs during specific processing states and operations. A stochastic upset susceptibility model for the 8080 microprocessor is presented. The susceptibility of this microprocessor to upset, once analog transients have entered the system, is determined analytically by calculating the state probabilities of the stochastic model.

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