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# HIGH DENSITY

# CIRCUIT TECHNOLOGY

# PART II



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16. ABSTRACT

Polyimides for use as interlayer dielectrics and passivation layers look very promising. They provide excellent step coverage, a degree of self-levelling, via resolution of at least 3 microns (1.5 microns reported), gradual interface slope change to enhance overlying metal continuity and high resistivity with a good dielectric properties.

Process development utilizing both Dupont and Hitachi polyimide types has been undertaken. A number of potential problem areas have been presented with regard to the process, however, once these have been overcome, an easily executed and reproducible process may be realized.

In addition, a new process for double layer metal interconnect via formation has been investigated which should allow for the following to be realized: a very low temperature process if the photo-chemical vapor deposited oxide is used with polyimide as the interlayer dielectric materials, a decrease in capacitive coupling effects for thick polyimide layers, an increase in packing density for both first and second level metal layers, the absence of oversized pads for vias to facilitate computer-aided design techniques, and a process which can be realized using either wet chemical or dry plasma processing.

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FORWARD

This report describes a portion of the work performed from July 1980 to March 1982 under Contract NAS8-33448 for the George C. Marshall Space Flight Center, National Aeronautics and Space Administration, Marshall Space Flight Center, Alabama. The technical managers for MSFC were Mr. B. R. Hollis, Jr., Mr. R. F. Dehaye and Mr. J. M. Gould. This report was prepared by the Microelectronics Research Laboratory of the Department of Electrical Engineering, Mississippi State University, under the direction of the principal investigator Dr. Thomas E. Wade. The principal participants in the program were Mrs. Rebecca A. Hamilton, and Mrs. Mildred N. Sellars. Typist was Mrs. Jerrie McIngvale.

This final report has been divided into four areas of emphasis, with a separate comprehensive report for each area. These four areas represent the following subject groupings:

PART I. Emphasis in on the realization of very dense metal interconnection for VLSI systems utilizing the lift-off process. Both a survey of lift-off techniques is presented as well as experimental and novel lift-off methods which have been investigated by the author.

PART II. Emphasis here is on multilevel metal interconnection system for VLSI systems utilizing polyimide as the interlayer dielectric material. A complete characterization of polyimide materials is

presented as well as experimental methods accomplished using a double level metal test pattern. A novel double exposure polyimide patterning process is also presented.

PART III. Emphasis is on dry plasma processing including a characterization of and an equipment survey for plasma etching, reactive ion etching, (reactive) ion milling and plasma deposition processes. Also included is an indication of future microelectronic trends, including patterning technology, lithography, materials deposition, packaging, etc.

PART IV. Emphasis here is on an evaluation of dielectric material for use in VLSI metal interconnection systems. A number of dielectric material types (or combination of materials) are experimentally evaluated using a second test pattern. Recommendations are presented based on these findings.

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# I. INTRODUCTION

As the density of VLSI circuits continues to increase for decreasing design dimensions, resulting from improved lithography and associated patterning technology, it becomes imperative that a multilevel interconnection system be employed which can be realized using low temperature processing techniques. The dielectric material must be of good quality (i.e., high dielectric strength and resistivity; low pinhole density, particulates, and dielectric constant; good thermal expansion coefficient, etc.) and one which can be deposited at low temperatures (to prevent lateral and out-diffusion of dopant impurities and degradation of radiation-hard characteristics). It is also desirable to use a dielectric material which will minimize stray interconnect capacitance effects and render a planar surface for subsequent metal layer coverage. In addition, the use of over-sized via's to minimize contact resistance, metal pitch (line width and spacing) and registration requirements for dense VLSI is very important.

## A. Organic Dielectrics

The use of organic materials such as polyimides for inter-level dielectric offers numerous advantages over the conventional chemical vapor deposited doped oxides. Polyimide films of 0.5 to 5 microns thickness can be spun on a wafer like photoresist and have virtually planar surfaces. Improved device performance can be achieved by reduction of the interlevel lead capacitances. In

addition, the conventional phosphorous doped silane oxide require reflow at temperatures as high as 1000°C after the deposition to achieve favorable contours if the oxide layer is very thick. In the case of polyimide, however, a final cure at temperatures as low as 200-250°C will render a dielectric layer having a dielectric strength of 100 to 300 volts/micrometer, a dielectric constant of 3.0 to 3.4, a bulk resistivity of $10^{16}$ ohm-cm, and a pinhole density of less than 4 $cm^{-2}$ and 0.1 $cm^{-2}$ for 1 and 3 μm thick films, respectively. The completely cured (or imidized) form of polyimide is resistant to attack by all chemicals but hydrazine, hot bases and plasma excited oxygen.

B. Other Dielectrics

Atmospheric oxides (400°-450°C, $SiH_4/O_2$) have been used during the past ten years for both final passivation and interlayer dielectric applications. Such films are primarily undoped oxides ($SiO_2$) and phosphosilicate glass (PSG) and they are characterized by high growth rates and relatively low quality. For dense VLSI, atmospheric oxides may meet the basic electrical requirements in terms of dielectric strength and breakdown voltages, however, the mechanical properties of step coverage, pinholes, particulates, and film integrity cannot be met by these films.

Low pressure chemical vapor deposition (LPCVD) oxides have definite advantage over their atmospheric counterparts in the area of step coverage, particulates and pinhole densities. They are normally deposited at 375-425°C and generally experience a relatively low [59] deposition rate of 75-150 Å/min. Low deposition rates have detrimental

effects in terms of throughput and hillock promotion (at a given temperature for a long time). An increase in deposition rate typically results in film quality degradation.

Plasma deposited oxides of the $N_2O/SiH_4$ variety, deposited at 250-300°C, have most of the good qualities which LPCVD oxide exhibit in terms of dielectric constant, breakdown voltage, density, particle and pinhole count, step coverage and adhesion to underlying metal [60]. In addition, typically the stress of the plasma oxide film is compressive in nature, which inhibits cracking tendencies. The deposition rate can be considerably better than that of the LPCVD oxides (400-500 Å/min), and is a function of the rf power applied.

Recently, an additional low pressure oxide process has been reported which allows films to be deposited at temperatures in the range of 50-300°C [61]. This photochemical vapor deposited oxide relies on neutral atomic oxygen being photogenerated from nitrous oxide by the appreciation of ultraviolet light, and then reacting with silane to form a silicon dioxide layer. The electrical and mechanical qualities of this low temperature oxide (typically $\leq$ 200°C) are said to be better than or at least comparable to those of LPCVD and plasma oxides. The deposition rate of the photo-CVD silicon dioxide process is principally dependent on the intensity of the UV radiation source and typically ranges from 100-400 angstroms per minute. This low deposition rate may prove detrimental to this process unless thin oxide layers are desired.

C. Report Context

This report consists of three separate though inter-related portions. The first portion will present an exhaustive treatment of polyimides and their application to high density circuit technology. The second portion will deal with double level metal interconnect process development using polyimides as a dielectric. The third portion will present a novel low temperature double-exposed polyimide/oxide dielectric type for utilization in VLSI multilevel metal system.

## II. POLYIMIDES FOR USE AS VLSI INTERCONNECT INTERLEVEL DIELECTRIC AND PASSIVATION LAYER

### A. INTRODUCTION

Polyimide resins as a class of chemical compounds have been available since 1926 [1]. Their usefulness to the electronics industry, as a plastic insulator which retained electrical and mechanical characteristics at temperatures in excess of 250°C, was recognized early [2]. Harada and coworkers at Hitachi Central Research Laboratories reported on a Polyisoindolo-quindzolinedione, given the acronym PIQ, which was suitable as an insulator for multilayered interconnections on large scale integrated (LSI) circuit surfaces as well as final passivation overcoat films [3]. R. Rubner and coworkers described a photosensitive polyimide which should shorten the semiconductor processing steps [4]. L. Zielinski (nee' Brosthman) is the first author to evaluate and compare commercially available polyimide resins by testing for characteristics vital to their use in LSI and very LSI (VLSI) circuits [5]. Recently, polyimides have been utilized as adhesive materials [6] as well as conductive paste for the hybrid industry [7].

Today, VLSI is experiencing several technological barriers as circuit density and complexity continues to increase. The most predominant of the barriers include existing lithography, patterning techniques and interconnection processes. It is felt that the use of polyimides as the insulator for multilevel interconnection systems could be a breakthrough for the interconnection processing barrier.

This section of the report will summarize all available information (literature, personal communications as well as conferences and short courses) concerning polyimides for applications as semiconductor interconnect interlevel dielectric and passivation layers. This will include defining the polyimide material, indicating its advantages, uses, limitations, characteristics, electrical and mechanical properties, and long term reliability.

## B. DIFFERENT TYPES OF POLYIMIDES AVAILABLE

A brief description of some of the more commonly used polyimide materials used in the semiconductor industry is listed in Table 1. There are considerable differences in these materials, including solvent systems, solid contents, and viscosity. Some of the materials may be obtained in powder form, which is an advantage in terms of shelf-life. Materials obtained in solution form, such as polyamic acid, typically have a shelf-life of one year when stored at 4°C.

While Dupont is a vendor for several different polyimides by number (i.e., PI 2545, PI 2555 and PI 2565 most common types used today), they represent different classes of chemical composition even though all of them are totally aromatic.

## C. DEFINITION OF POLYIMIDE

Polyimides are prepared from the polycondensation reaction between an aromatic dianhydride and an aromatic diamine, typically represented by the reaction of pyromelletic dianhydride and

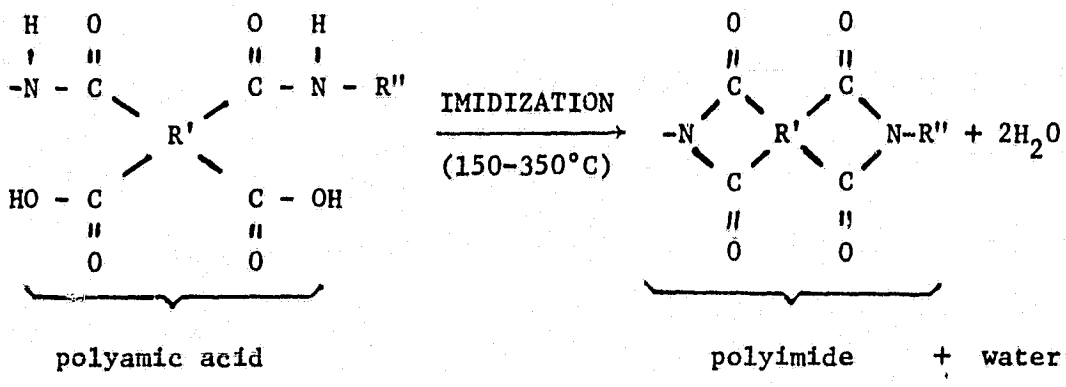
TABLE I

Commercially Available Polyamic and Polyimide Resins

| RESIN | TYPE | SOLVENT | % SOLIDS | VISCOSITY(cps) |
|---|---|---|---|---|
| Hitachi PIQ | Polyamic Acid | NMP* +Aromatic Hydrocarbon | 14 | 1100** |
| Dupont PI2540 | Polyamic Acid | NMP + Aromatic Hycrocarbon | 15 | 4000-7000 |
| PI2545 | Polyamic Acid | NMP + Aromatic Hydrocarbon | 14 | 1100 |
| PI2550 | Polyamic Acid | NMP + Acetone (3/2) | 25 | 4000-7000 |
| PI2555 | Polyamic Acid | NMP + Aromatic Hydrocarbon | 20 | 1100 |
| PI2560 | Polyamic Acid | NMP + Xylene | 37 | 3000-4000 |
| Ciba-Geigy XU218 | Polyimide | None*** (powder) | 100 | - |
| Monsamto Skybond 703 | Polyamic Acid | NMP | 63-67 | 3000-7000 |
| Rhodia Nolimid 605 | Polyamic Acid | NMP + Methanol (4/1) | 55 | 4000 |
| Rhodia Kermid | Polyimide | None*** (powder) | 100 | - |
| Upjohn 2080 | Polyimide | None*** (powder) | 100 | - |

* NMP = N-Methyl-2-pyrrolidone
** Can be ordered to any specified viscosity
*** Usually soluble in NMP, dimethyl formamide, etc.

and oxydianiline [21]. They are purchased in a pre-imidized form known as a polyamic acid which are readily soluble in polar organic solvents. The polyamic acid converts to the polyimide at temperatures high enough to remove the solvent and initiate the imide ring closure, as example:




The degree of imidization and completeness of reaction depends upon the nature of the R' and R'' groups (i.e., aromatic rings) as well as the type and amount of residual solvent from which the polyamic acid is cast [30]. As such, the mechanical, electrical and reliability properties of the resulting polyimide will depend on the nature of the above reaction. Also, as indicated by the above typical reaction, water loss during the imidization process represents a significant solvent loss during polyamic acid cure and anneal. This will be addressed further in section F-3 where curing characteristics of the polyimide are discussed.

As previously mentioned, photosensitization of polyimides was realized by Rubnen of Siemens [4] and Kerwin and Goldrick of Bell Laboratories [8]. The Siemens formulation depended upon a cross linking reaction to increase the molecular weight of the polymer during exposure to ultraviolet light, hence lowering the solubility in developing solvents (negative resist action). This resist was trial tested by Ciba Geigy. It was found to have a low photosensitivity and a resolution limit of 5 to 10 microns. The Bell Laboratory solution (marketed as Dupont RK-692) consisted of a 3 part Pyre-ML to 1 part 2% potassium dichromate in dimethylsulfoxide sensitized solution and had a shelf-life of 4 to 8 hours. This is not commercially appealing.

A unique feature of the Hitachi variety polyimide is that it consists of a ladder type polymer composed of both isoindoloquinazolinedione and imide structures. This structure is said to have additional thermal stability compared with general polyimide structures [19]. Graphical illustration of Hitachi's polyimide (called isoindroquinazoline - dione polyimide, or PIQ for short) compared to regular polyimide is shown in Figure 1 [2]. Also, Hitachi claims to be the first company to purify the raw materials in synthesizing the PIQ precursor such that a sufficient reduction in impurity content of the resulting polyimide could be realized, thus making them applicable to semiconductor type applications [9].

As will be discussed later, the completely cured or imidized form of polyimide is resistant to attack by all chemicals except hydrazine [10], hot bases and plasma excited oxygen.

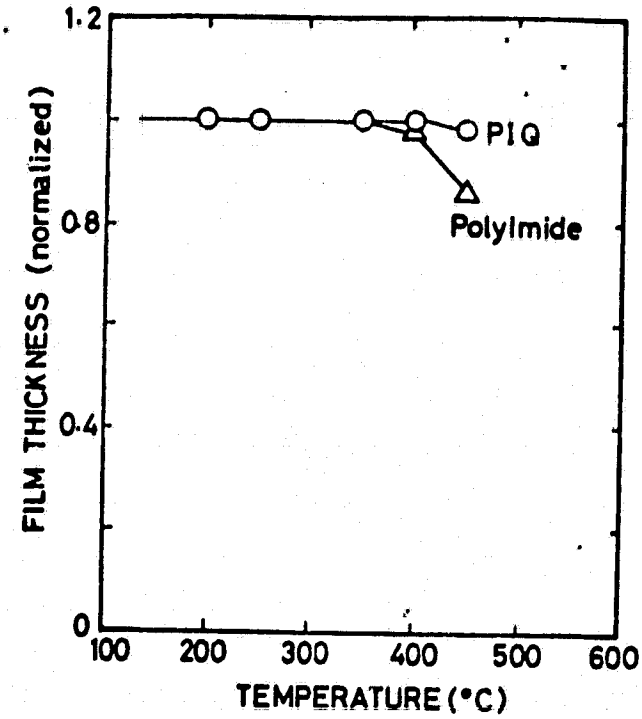



Figure 1. Thermal degradation of polymers

D. USES AND ADVANTAGES OF POLYIMIDE MATERIALS

Polyimides are experiencing a wide variety of uses in the semiconductor industry. The more prominent uses include:

a. As a protective or passivation overcoat

b. As an interlayer dielectric for multilevel metal processes

c. As an alpha particle barrier

d. As an ion-implant and metal lift-off mask

e. As the support structure of a X-ray mask.

Some of the semiconductor companies who have utilized polyimides in their products include the following:

- Hitachi's development of a linear IC having 320 elements for use as a TV chroma system. Layers of 3.5 μm thick PIQ were used for the interlevel dielectric and final protection. A 40 percent reduction in chip size was achieved in comparison to the standard single-level interconnections with the same functions. This reduction was attributed to bonding pads placed over the active region of the device and to two-level interconnection itself [11].

- IBM announced the introduction of a 64K RAM designed to optimize yield and reliability which incorporates polyimide as the inter layer dielectric [12]. IBM has more recently announced the use of polyimides in more complex silicon and aluminum MOS technology [15].

- Texas Instruments has reported development of a VLSI-MOS process which features $MoSi_2$ gates and polyimide interlevel insulation [13].

- Plessey Research Limited has used polyimide as an interlevel dielectric between two layers of Al/Si interconnection in its 400 gate Uncommitted Logic Arrays (ULA) or "Standard Diffused Slice" [14].

- Tektronix has used polyimide to passivate thin microwave hybrid circuits [8].

- MIT Lincoln Labs have investigated polyimides for use in a 64K MNOS memory array (16).
- Intel (and Texas Instruments) have used polyimide as a passivation layer to protect 64K dynamic and 16K static RAM's from alpha particle failures (17).
- Hitachi has recently reported the use of polyimide material for metal lift-off applications in realizing minimum pitch interconnection as well as an interlevel connection (between first and second level metal) through exposed via holes (18).

Polyimides possess many characteristics that make them attractive candidates for application as multilevel insulators and passivation layers in the fabrication of VLSI devices. The more predominant advantages are listed as follows:

1. Application. The polyimide precursor (or polyamic acid) is applied in a liquid form much like photoresist. Variation in viscosity (using solvent thinners) and chuck spin speed and time will deposit reproducible thicknesses of polyimide on the wafer. Also, since photoresist dispensing equipment can be used, the application can be easily automated resulting in flat quality films at low cost.
2. Planarization. The fluid properties of the polyamic acid upon deposition tends to planarize the underlying topography. This is especially true for films exhibiting

a final cure thickness in excess of 2-3 microns of polyimide. A comparison of the topography obtainable using the conventional interlayer insulations (i.e., $SiO_2$, $Si_2N_4$, etc.) and polyimides is shown in Figure 2.

Uniform thickness insulator coatings as shown in Figure 2a tend to generate discontinuities in the deposited aluminum film, a reduction in precision of photo-etching, and defects such as cracks in the insulating material tend to occur because of this stepped structure, reducing the yield of the interconnection. Because of these effects, semiconductor devices produced by this method are generally limited to a maximum of two levels and a minimum width of 7-10 microns for the aluminum patterns if high yield is to be maintained.

Figures 2b and 2c show two different procedures of planarizing the surface using polyimide. The first (Figure 2b) uses through holes or 'vias' cut in the polyimide so that the deposited top metal layer may contact the lower level metal. The second (Figure 2c) uses metal "bumps" formed on top of the metal layer to contact upper levels of metal after uniformly removing the polyimide from over the bumps [3]. This latter process renders a strictly planar top surface. The fine pattern of metal layers which are obtainable on

these planar surfaces coupled with the freedom to use as many levels as desired are necessary conditions for realizing denser VLSI circuitry.

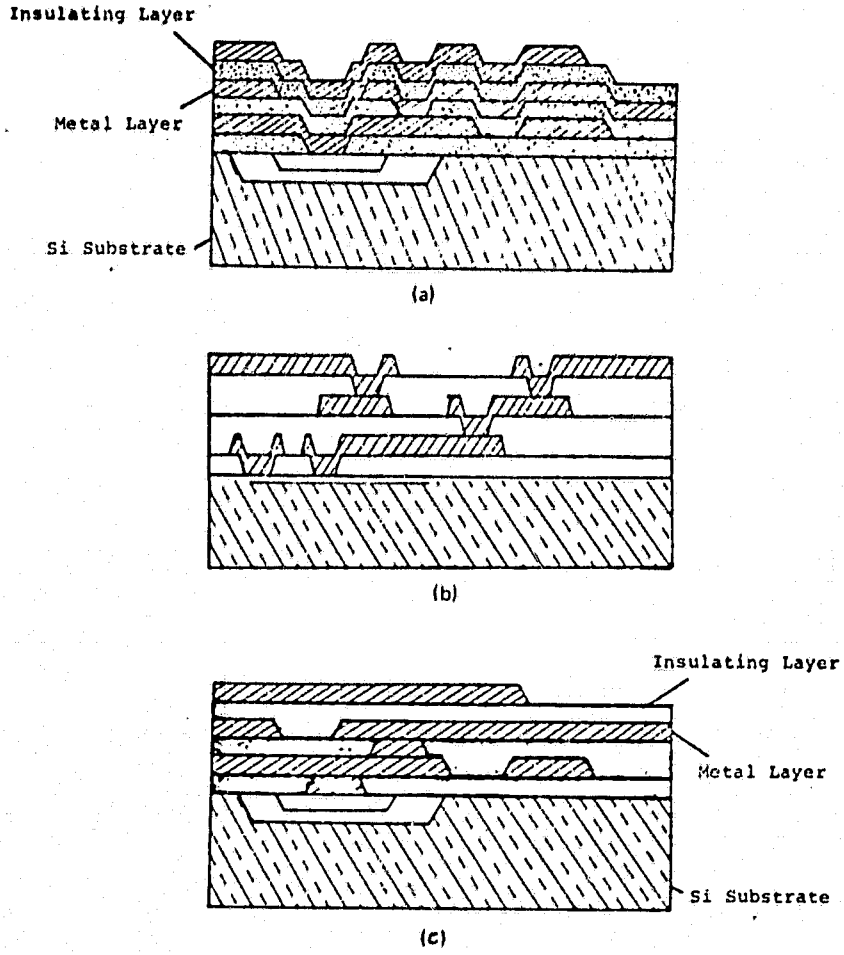



Figure 2. Comparison of surface topography obtainable using interlayer insulator of a) inorganic $SiO_2$, $Si_xN_y$, etc. b) polyimide using through holes or via's, and c) polyimide using the 'bump' technology.

3. Low Temperature Processing. Most chemical vapor deposited inorganic insulation layers are deposited within the temperature ranges of 400-800°C. In fact, some processes like the conventional phosphorous doped silane oxides require reflow at temperatures as high as 1000°C after deposition to achieve favorable contours. For polyimides, a final cure temperature of less than 350°C will render a tough and resilient film. This low cure temperature minimizes effects like dopant redistribution in VLSI circuits, etc. which occur during high temperature processing.

4. Patternability. Polyimides may be patterned for via-holes (connect points between metal levels) and bonding pads either in a partially cured (or pre-imidized) state using an aqueous alkaline solution, or in a final cured state using dry plasma etching techniques. Well defined opening in the polyimide having sloped side-walls and dimensions equal to or less than the film thickness can be easily realized (i.e., can etch via's 2x2 μm in 1.5 to 2.5 μm thick films with good pattern definition). No acid solutions, like HF, are required in patterning polyimide.

5. Mechanically advantageous. The stress, either tensile or compressive, experienced by cured polyimide films is nearly non-existant. Thus, very thick films can be realized without the cracking and adhesion problems characteristic of CVD films. Also, since films can be deposited relatively thick (ie, 2-5 microns for interlevel insulators as opposed to 1 micron or less for other insulating materials) and/or two or more thin polyimide layers can be deposited on each other, the pinhole density achievable is very small if not zero. With near zero pinhole density, the use of alkaline solution instead of acidic solution for patterning, and the absence of phosphorous-doped oxide films commonly used, the tendency for corrosion of underlying metal interconnect is practically eliminated. Polyimides are excellent barriers for water vapor and sodium ion migration [42]. Also, their shock absorption capacity allows protection against external forces.

6. Electrically advantageous. Polyimides possess a dielectric constant, volumn resistivity and dielectric breakdown strength comparable to silicon dioxide films at room temperature. Also, since thick films can be realized, this results in reducing the parasitic capacitance of the interconnection.

7. Thermal stability. Cured polyimide films are thermally stable up to 450-500°C. This is very important in hot metal deposition processes, sputter etching and die bonding operations. In fact, polyimides are experiencing many uses for replacing photoresist as a masking material. At temperatures in excess of 200°C,

most conventional resist undergo degradation, cross-linking and hardening (in fact, PMMA tends to flow above 95°C). Because of their thermal stability, polyimides should find additional uses as metal lift-off patterns, mask for high energy ion implantation steps, etc. It has been reported that laser trimming of hybrid resistors through polyimide passivation coating can be accomplished and still not degrade the protective property of the layer [8].

8. Alpha particle barrier. Alpha radiation emitted by trace amounts of naturally occuring thorium and uranium isotopes in packaging materials is a source of nondestructive soft error problems in charge coupled devices and dynamic memories. As the device geometries shrink and critical charge levels diminish, this problem becomes much more acute (ie, the chance for a soft error to occur increases greatly from 16K to 64K RAM). A coating of polyimide with a thickness of no less than 3 mil over the memory chip will practically eliminate this problem as illustrated in Figure 3.

9. Wafer rework. It is possible to remove fully cured polyimide coatings using solutions of hot ethylenediamine, hydrazine, plasma $O_2$, etc. without adversely affecting any underlying structure of the wafer. This cannot be accomplished with other deposited insulating materials.

10. X-ray mask fabrication. Recently, polyimides have been proposed to act as a membrane in the formation of X-ray mask (54,55). To fulfill this role, the membrane must have the following requirements:

(1) transparent to ordinary light; (2) transparent to X-rays; (3) dimensional stability; (4) ruggedness; (5) surface flatness; (6) low defect density; (7) high resolution; (8) ease of fabrication; and (9) low cost.

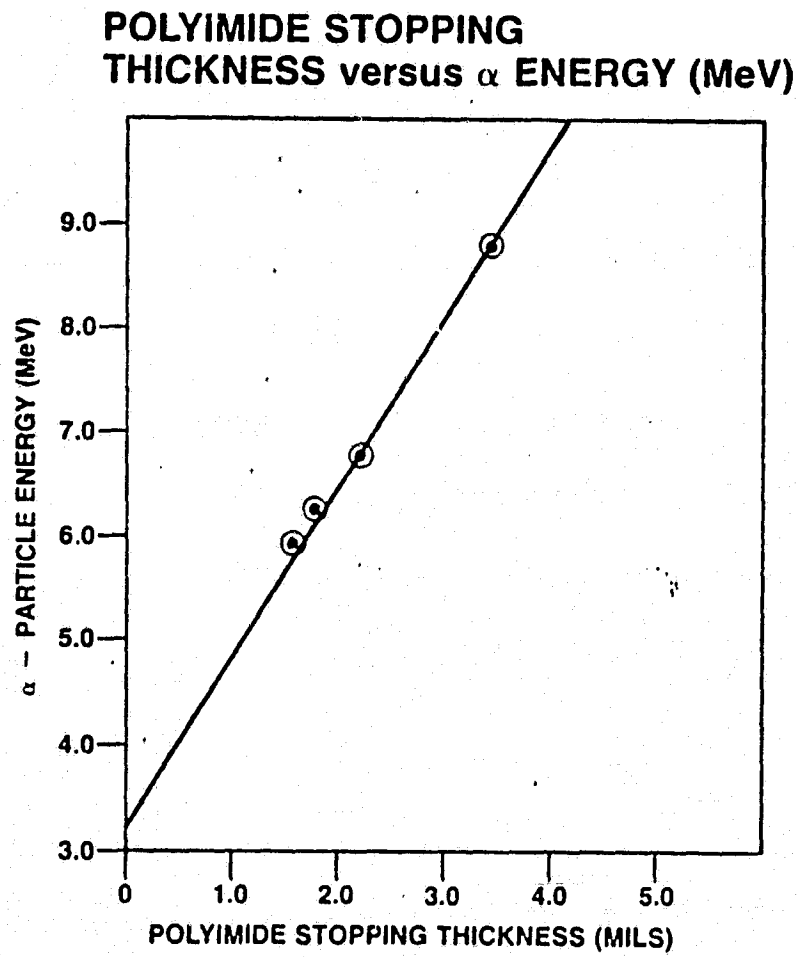



Figure 3. Polyimide thickness required to totally stop α-particles as a function of particle energy.

E. PROCESSING STEPS - AN OVERVIEW

The following are typical processing steps involved in applying polyimide coatings to a wafer.

1. Priming the wafer: To obtain good adhesion between the wafer and the polyimide coating, a dilute solution of an organic silane or organoaluminum complex is applied to the wafer and spun to dryness. A 10 minute 130°C bake is optional but preferred.

2. Applying polyimide coating: Polyamic acid solution (12-40% solids at 5 - 20 poise) is spun on the wafer.

3. B-Stage cure of film: The wafer must be prebaked to be almost dry and in the process the polyamic acid coating is partially imidized. The degree of this bake determines the conditions for etching and stripping.

4. Photoresist: A solution of positive or negative photoresist is spun on top of the polyimide coating and prebaked at a temperature and time characteristic of the resist used (but less than the B-stage cure temperature).

5. Align and expose: Use contact, proximity or projection alignment (projection preferred).

6. Etching and developing: The etching of the polyimide coating and developing of the positive photoresist can be accomplished in one step with a dilute aqueous alkaline solution. Negative photoresist must first be developed and

postbaked prior to etching. Typical etchants for both resists are dilute solutions of NaOH, KOH and tetra-alkyl ammonium hydroxide, etc.

7. Neutralization and rinse: It is imperative that alkaline metal ions are totally removed from the system. This can be accomplished by an acetic acid solution wash followed by rinsing with deionized water.

8. Stripping of Photoresist: Positive photoresist can be stripped with solvents such as acetone, isopropanol, butyl acetate, etc. Negative resist can be stripped with J-100 "microstrip", 712D, etc.

9. Final cure: The polyimide coating is given a bake of 300-350°C to complete the imidization and obtain the full film properties.

10. Etching final cured polyimide: For patterning final cured polyimide using dry plasma etching techniques (ie, oxygen or $O_2$ + $CF_4$) or caustic aqueous basic solutions (ie, hydrazine), steps 4 through 8 are postponed until after step 9 with the etchants mentioned in step 6 replaced with those mentioned here.

To minimize pinhole density and/or to apply a thicker polyimide coating, a second layer may be spun on the wafer after partial or final curing.

F. PROCESSING - A FULL CHARACTERIZATION

An overview of the pertinent processing steps were presented in the last section. A complete characterization of these and auxiliary procedures will be presented in this section.

1. Coupler for adhesion promotion:

Polyimides adhere well to aluminum or synthetically created alumina surfaces, exhibiting peel strengths in excess of 100 gms/cm (19). Adhesion to clean bare silicon surfaces is also quite good after curing in excess of 350°C, however, adherance to silicon dioxide surfaces are typically poor, especially under high moisture at elevated temperature conditions. Hence, the application of an alumina or an amino siloxane coupler is generally required.

Hitachi and others promote a coupler which is an aluminum organic chelate in an organic vehicle that readily spins on the wafer and converts to $Al_2O_3$ layers 50 to 150Å thick after curing at temperatures in excess of 300°C in air (20).

Dupont and others recommend using organic silane couplers like gamma-glycidal amino propyl trimethoxysilane or surface bonded siloxanes with amine terminal groups like α-glycidoxyl-propyltrimethoxy silane (19). These couples deposit a silane monolayer on the silicon dioxide surface which is much thinner than the deposited $Al_2O_3$ layer mentioned above and ties the Si in $SiO_2$ to the polymer chain in the polyimide.

Hitachi's "PIQ Coupler" is deposited in liquid form as received much like hexamethyldisilazane (HMDS). Approximately 0.5 to 1.5 cc of this liquid coupler is dispensed statically and followed by a 4K rpm spin for 20 seconds (20). It is then baked at 325°C for 30 minutes in air.

Dupont's coupling agent VM-651 must be reduced to a 0.01 to 0.1% solution in a 95/5 methanol/water mixture and allowed to stabilize for about eight hours at room temperature prior to use (21). One cc is dispensed on the wafer statically and spun to dryness at 5000 rpm for 30 seconds. Point of use filtration is often practiced and the amino silane solution is stable for some five to ten days. The coupler container should be tightly sealed since water will cause VM651 to polymerize slowly.

Other commercially available aliphatic amino siloxane couplers include Dow Chemical Z-6020, organaluminum couplers include Duponts "Baymal" solution (22), and a Union Carbide coupler A-1100 (53).

2. Polyimide Liquid Characteristics and Application

Perhaps the best way to characterize the liquid properties of polyimides (polyamic acids) is to select a couple of more commonly used types and present typical properties of each. Tables II and III represent typical properties for Dupont and Hitachi polymides, respectively.

| | PI-2540 | PI-2545 | PI-2550 | PI-2555 |
|---|---|---|---|---|
| Solids (2 gms, 2 hours @ 200°C) | 15% | 14% | 25% | 20% |
| Viscosity (LVF #3 @ 12 RPM) | 40-70 poise<br>4-7 Pascal second | 10-12 poise<br>1-1.2 Pascal second | 40-70 poise<br>4-7 Pascal second | 10-12 poise<br>1-1.2 Pascal second |
| Weight per gallon<br>per liter | 8.80 lbs.<br>1.06 kg | 8.78 lbs.<br>1.06 kg | 8.95 lbs.<br>1.08 kg | 8.80 lbs.<br>1.06 kg |
| Solution Density | 1.06 g/cc | 1.06 g/cc | 1.08 g/cc | 1.06 g/cc |
| Solvent | NMP[1]/aromatic hydrocarbon | NMP[1]/aromatic hydrocarbon | NMP[1]/acetone | NMP[1]/aromatic hydrocarbon |
| Flash Point (Closed Cup) | 64°C | 64°C | -7°C | 64°C |
| Filtration | 5 micron | 1 micron | 5 micron | 1 micron |

[1]NMP - N-methyl-2-pyrrolidone

** Typical properties: not to be used for specification purposes.

TABLE II. Typical Properties of Dupont Polyimide Liquids For Types PI2540, 2545, 2550, and 2555.

| TEST ITEM | | CONDITION | UNIT | PROPERTIES |
|---|---|---|---|---|
| COLOR (GARDNER COLORIMETER) | | - | - | 13 > |
| VISCOSITY | | 25 ± 0.5°C | CPS | 1100 ± 200 |
| REDUCED INTRINSIC VISCOSITY | | 25 ± 0.5°C | DL/G | 0.3 < |
| NON-VOLATILE CONCENTRATION | | 200°C/2 HOURS | % | 14.5 ± 0.5 |
| WATER CONTENT | | KARL-FISHER TITRATION | % | 1.0 > |
| SOLVENT SYSTEM | | NMP/DMAC | WEIGHT RATIO | 50/50 ± .5 |
| IMPURITIES CONTENT | Na | ATOMIC EXTINCTION ANALYSIS | PPM | 2.5 > |
| | K | | | 1.0 > |
| | Cu | | | 0.5 > |
| | Fe | | | 0.5 > |
| FILTRATION CONDITION | | TO BE PASSED THROUGH A FILTER OF 1 MICRON | | |

TABLE III. Typical Properties of Hitachi PIQ Liquid

The color of most polyamic acids as received is dark amber or brownish in nature. Liquids are free from floating matters, sediment, foreign bodies and the like of more than typically 1 micron. The refractive index of a typical polyimide liquid is approximately 1.5 at 25°C, and its specific gravity is approximately 1.04 (for a viscosity of 1100 cps) (20).

Filtration of the liquid just prior to dispensing is recommended. A number of filter types have been reported in the literature for this purpose, like platimum (23), silver membrane (24) etc. Filter size varies from 0.25 μm to 1-2 μm.

Storage of polyimides in liquid form is very important if a long shelf-life is to realized. These liquids are very sensitive to heat and should be refrigerated at 4°C maximum. Freezer storage (-18°C) will practically eliminate any viscosity drift and prolong shelf life significantly. As an example, Dupont PI-2540 will gradually drop in viscosity when exposed to temperature above freezing, and then reverse direction and eventually gel. Gelation occurs in approximately 90 days at 25°C, 30 days at 40°C and 14 days at 50°C.

Moisture contamination of the liquid is detrimental to stability and must be avoided. Containers should be brought to room temperature before opening to avoid moisture of condensation.

Semiconductor device characteristics are very sensitive to alkali metal ions, especially sodium ions (11). The sodium ion content of a polyimide made using raw materials or purified

materials can be monitored by atomic absorption spectroscopy. For example, for Hitachi PIQ, the sodium content of the resulting liquid for both generation from raw materials and from purified materials is given in Table IV (9).

| MATERIALS | | SODIUM CONTENT (ppm) | |
|---|---|---|---|
| | | RAW | PURIFIED |
| AMINES | AM | 185.0 | 4.5 |
| | AMC | 792.0 | 1.2 |
| ACID DIANHYDRIDE | DA-1 | 2.0 | 0.6 |
| | DA-2 | 1.9 | 1.1 |
| SOLVENTS | NMP | 0.56 | 0.07 |
| | DMA | 0.55 | 0.07 |
| PIQ VARNISH | | 54.0 | 0.51 |

TABLE IV. Sodium Content in Starting PIQ Material and PIQ Varnish (Polyamic Acid)

The reason for so many sodium ions in diamines can be explained as follows. Diamine is prepared by reduction of dinetro-compounds (III). The diamine then reacts with hydrochloric acid forming hydrochlorides in order to separate organic impurities. Then hydrochloride is neutralized by sodium hydroxide to form diamine and sodium chloride. Therefore, many sodium ions from sodium hydroxide and sodium chloride are contained in raw amine materials, yielding 54 ppm in the varnish. However,varnish formed from purified materials (obtained in the same manner as dehydration) include less than 1 ppm sodium ions.

As mentioned earlier, polyamic acids are soluble in several organic solutions such that the viscosity of the liquid may be adjusted. The more commonly used solvents include N-methyl-2-pyrrolidone (NMP), Dimethyl formamide (DMF) or Dimethylsulfoxide (DMSO). Adjustment of viscosity permits either spray or spin coating. Some vendors handle viscosity specifications by either adjusting the viscosity of the polyamic acid to a set of specifications prior to shipment (Hitachi) or furnish a purified thinning solution which allows for viscosity adjustment (Dupont). For example, for Dupont polyimides PI-2540 and 2550, thinner T-8035 is recommended, whereas for PI2545 and 2555, a more refined thinner T-9035 is used.

In applying the polyamic acid to the wafer, several processing parameters are involved: dispense volume, wafer spin speed during dispense (often referred to as dispense speed), angular acceleration, and final, dry-cycle, spin speed. Accurate studies have been made of polyimide thickness and thickness uniformity as a function of dispense volume, dispense speed and final spin speed (20). The application of a coupler to the wafer prior to depositing the polyamic acid does not affect either the thickness or thickness uniformity across the surface of the wafer. Accurate thickness measurements can be accomplished using a Tallystep, a Film Thickness Analyzer and/or SEM analysis of cross-sections.

The average polyimide film thickness is pretty much independent of polyamic acid dispense volume and dispense speed, but

depends predominately on the wafers final spin speed. However, the thickness uniformity is a function of all three parameters and is found that for a 3 inch wafer using polyamic acid of viscosity 1100 cps, as an example, optimum uniformity is obtained if the dispense volume is 0.5 cc, the dispense speed is static (0 rpm), and the final spin speed is $\geq$5K rpm (20).

Typical thickness of cured polyimide as a function of final spin speed for two different viscosity liquids is shown in Figure 4 (19). Here, the polyamic acid is dispensed statically, spinning was then accelerated at a 1K rpm/sec$^2$ rate to the final spin speed for 20 seconds.

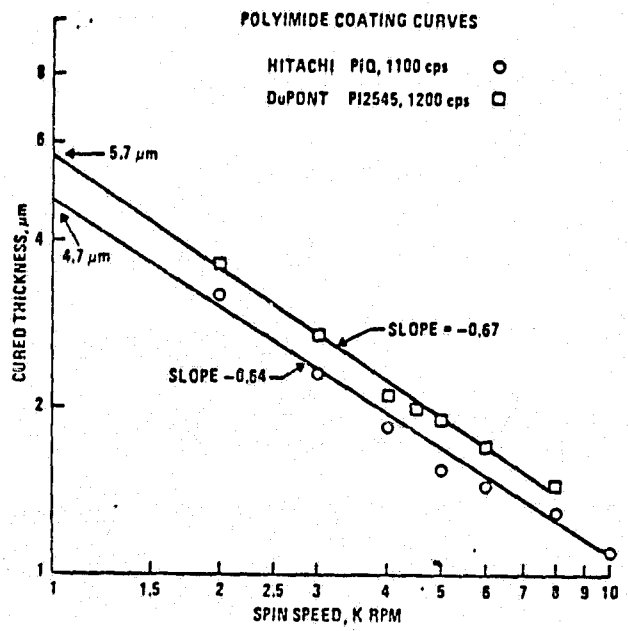



Figure 4. Polyimide coating curves. Thickness of final cured polyimide as a function of final spin speed.

It has been reported (16) (as well as experienced in our lab) that at times after depositing the polyamic acid on the wafer (especially low temperature imidizing solutions like PI2566), if the wafer is not placed in the B-stage cure oven immediately, there is a tendency to form "fisheyes" (small sharp swells on the surface which can be a few microns in height). The use of an IR lamp mounted over the spinner, or the placing of the wafer directly into a low temperature oven from the spinner will eliminate this problem.

### 3. B-Stage Cure

As indicated in the last section, after spinning on the polyimide coating, the wafer is baked immediately. This B-staged film is then protected from excessive moisture by the use of a dry box if a delay in processing is experienced.

Probably the single most important variable in the processing of polyimide coatings is the cure cycle. During the heating of the film, solvant evaporation takes place simultaneously with imide formation. The amount of solvent remaining after bake and the degree of imidization determines the solubility and solvent resistance of the film.

During the B-stage bake cycle, with increasing temperature, an increasing number of amic acid groups become thermally dehydrated to form imide and the film becomes increasingly insoluble. During the process, a condition must be defined so that the film is baked sufficiently to withstand the stripping solvent but not too advanced to cause difficulty during etching. Thus, information on the rate of cure is needed in defining the process conditions.

A number of methods have been used to monitor the rate of imidization. These include differential IR absorption spectrum (21), dissipation factor (25), mass spectral analysis and dielectric constant (26), and thermal gravimetric analysis and differential scanning calorimetry analysis (19). Of these, monitoring of the "dissipation factor" or "measure of dielectric loss" is one of the simplest and most frequently used methods, and thus will be discussed here.

Any lossy dielectric may be modelled by an ideal capacitance, C, in parallel with a resistor, R, whose value is dependent upon orientational polarization or permanent/quasi-permanent dipole moments. Further, consider this parallel combination to have impressed a voltage V, as shown in Figure 5. Also shown in the relationship between apparent power, Pa, imaginary power, Pim, and real power, $P_{real}$.

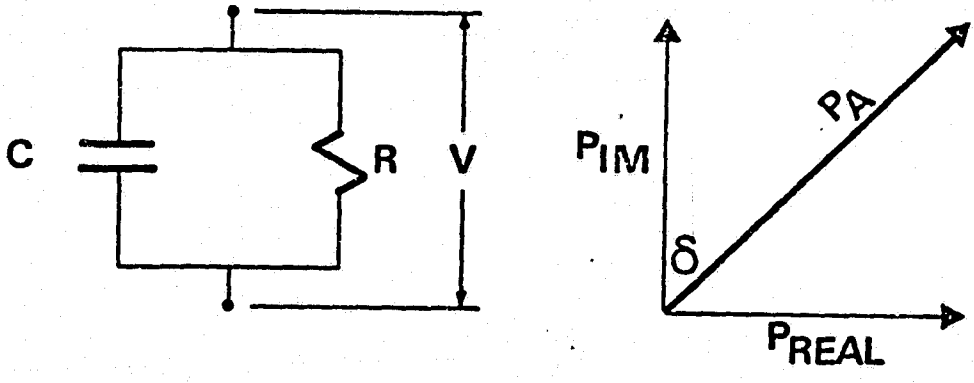



Figure 5. Lossy dielectric model(a) and power diagram (b)

The dissipation factor is defined as the ratio of the real to imaginary power, or from Figure 5(b)

$$\text{Dissipation factor} = \frac{P_{real}}{P_{im}} = \tan \delta$$

and from Figure 5(a)

$$P_{real} = \frac{V^2}{R} \quad \text{and} \quad P_{im} = \frac{V^2}{(\frac{1}{\omega C})}, \text{ thus } \tan \delta = \frac{1}{\omega RC}$$

when R and C are measured values, and $\omega$ in the frequency of measurement.

Typical measurement procedure involves depositing a metal dot on top of a polyimide layer and measurements taken between this top metal dot and a bottom metal signal plane. A more accurate method replaces the top metal dot with a mercury probe, and measurement taken between it and the bottom metal plane.

If it is arranged such that the area of the plates of this capacitor (top and bottom metals) are much greater than the electrode spacing, $\ell$, (polyimide thickness), then

$$R = \frac{\rho \ell}{A} \text{ and } C = \frac{\varepsilon A}{\ell}, \text{ thus } \tan \delta = \frac{1}{\omega \rho \varepsilon}$$

where $\rho$ and $\varepsilon$ are the resistivity and dielectric constant of the "lossy" dielectric.

Typical data obtainable using dissipation factor measurements is given in Figure 6 (25).

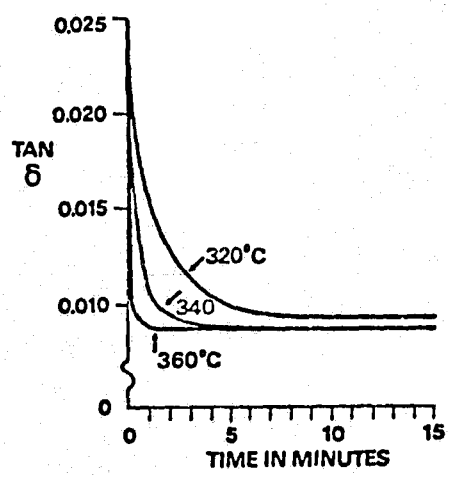



Figure 6. Measured dissipation factor as a function of time for 2 micron thick polyimide at three temperatures.

Using dissipation factor and other monitoring procedures, indications are that the cure cycle for polyamic acid resins is complicated by the simultaneous evaporation of the solvents, the closure of the imide ring, the loss of highly bound water and internal polymer chain rearrangements. Due to the high volatility of its primary solvent (typically NMP) at low temperature, significant weight loss occurs at or below 100°C but continues up to the boiling point (205°C for NMP). A typical thermal gravimetric analysis curve for polyimide which had been cured for 20 minutes at 70°C and 30 minutes at 105°C is shown in Figure 7.

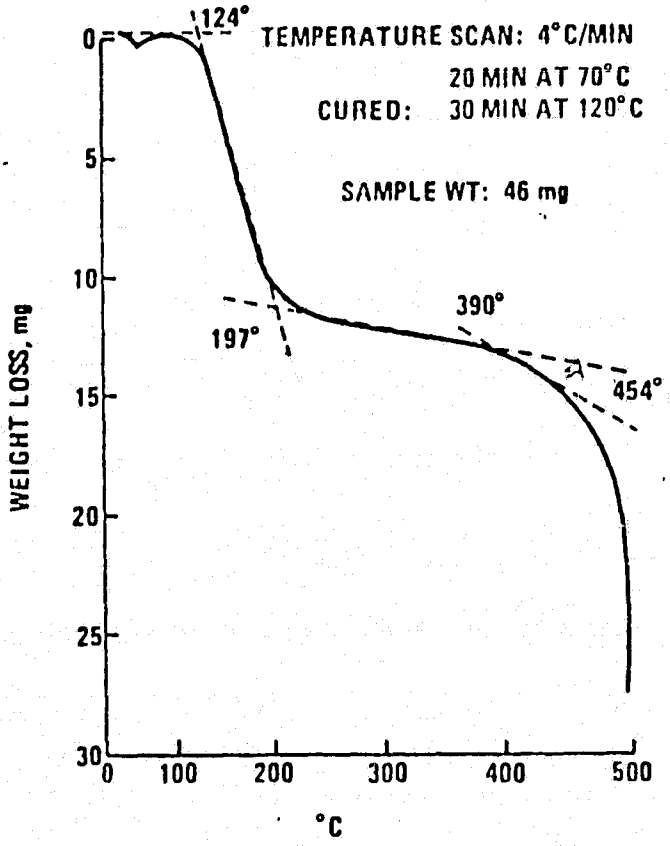



Figure 7. Thermal gravimetric analysis of a typical polyimide indicating ranges of weight loss (19).

Three major weight loss regions are observed: 20-25% is loss between 124-197°C, another 5-10% is lost between 350-454°C and beyond 454°C the film oxidizes and destructively decomposes.

Another way to follow the rate of imidization (and more accurate) is by monitoring the change in IR absorption. The I.R. spectrum of a polyamic acid differs significantly from that of the corresponding polyimide. Typical results are given in Figure 7a for Duponts PI-2550 (30).

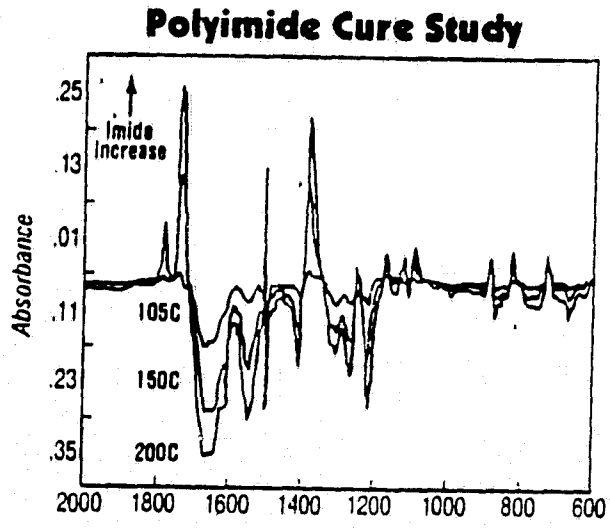



Figure 7a. Imidization rate of polyimide PI2550 as measured by I.R. absorption methods.

A recommended B-stage curing cycle schedule might consist of 50°C - 1/2 hour, 80°C - 1/2 hour, 100°C - 1/2 hour and 135°C for 1/2 hour. When the solvent is driven off slowly, the resulting films surface is smooth and good adhesion between the film and wafer is obtained. A 90°C for 1/2 hour followed by 135°C for 1/2 hour B-stage cure will also render acceptable films, however, too fast drying leads to poor adhesion (22) and the elimination of low temperature B-stage cures result in crumbly, non-adherent films (8).

After B-stage curing, the solvents have been driven off and a limited degree of imidization has taken place such that photoresist can be applied, exposed, developed, stripped and the film can be easily etched without altering the final film properties.

B-stage curing (as well as final curing) can be accomplished on a hot plate (24,25) in a convection oven (21), a forced-air oven (19) or a furnace. The hot plate cure renders lower dissipation factors due to the thermal gradient realized across the wafer which tends to migrate the molecular water formed during linkage formation toward the wafer surface and, hence, into the atmosphere. No such gradient is present in an oven.

4. Patterning of Partially Cured Polyimide

Patterning completely cured polyimide films using conventional photo-etching processes is difficult due to the excellent chemical resistance of these cured films which make them impervious to most wet chemical etchants. Even though the films do display solubility in hot basic solutions, these solutions also destroy the photoresist. It is possible to pattern completely cured films and this will be discussed later.

The B-stage cured films are much easier to pattern using wet chemical etchants and allow good etch rate and profile control. The etch rate and profile depend on the degree of cure or imidization which in turn, is a function of temperature and time for B-stage formation. It should also be noted that different polyimides will imidize at a faster (or slower) rate than others when

(partially) cured at the same temperature and time. As an example, Dupont PI 2550 and PI 2555 or PI 2525 imidize more quickly at the same temperature than does PI 2540 or PI 2545. Also, PI-2566 imidizes even faster than any of these.

1. Positive Photoresist Process: A number of different positive photoresist types have been employed to pattern the partially imidized polyimide layer. These include Shipley's AZ111, AZ1350J, AZ1375 and KTI's positive II or 809, to name a few. The resist is normally applied statically, ramp at 800-1000 rpm/sec$^2$ to the final spin speed for 20-30 seconds. Prebake is conducted between 75-95°C for 20-35 minutes, followed by wafer alignment and exposure.

   Development of the positive photoresist and etching of the underlying pre-imidized polyimide layer is accomplished at the same time. Once the caustic basic developer solution penetrates the photoresist layer it then begins etching of the polyimide. The polyimide etch rate is a function of the degree of imidization and the strength of the etching solution, both of which are controllable parameters. Typical developer solutions used include Shipley's AZ351, AZ303, MF-312 or other basic solutions as aqueous potassium hydroxide, DE-3, aqueous sodium hydroxide, tetralkyl ammonium hydroxide, 50% β-phenylethylamine in water, and the like. Most basic concentrations range from 0.05N to 0.5N mixtures (21).

After etching, the photoresist must be removed with a substance which does not affect the polyimide layer. Typical resist strippers include Shipley AZ Thinner (excellent), acetone, and a mixture of butyl acetate and isoproponal (6:4 ratio).

2. Negative photoresist process: Patterning the polyimide using a negative resist process involves a few more steps than the positive resist process, but allows somewhat more freedom in patterning. Typical negative resist types include Waycoat HR-200 and Type 3 No. 43, IC 359CPS, KTFR and Microresist. These resist are applied, prebaked, aligned and exposed, developed and rinsed, and postbaked prior to polyimide etching.

All of the etchants used for the positive photoresist process also apply for the negative resist. Since the negative resist undergoes a postbake at an elevated temperature (ie, 100-135°C), the underlying polyimide will have imidized more resulting in a slower etch rate for the same etchant used in the positive resist process. In addition to the etchants listed in the positive resist process, another etchant for use in a negative resist process has gain popularity, this being an aqueous solution of ethylenediamine (27). Ethylenediamine, when reacted with polyimide, gives a water soluble product which contains no carbonyl.

After polyimide patterning, the negative resist is removed typically using J-100, CB-1, and 712D.

After etching, these strong bases in aqueous media leave base residues which can cause serious polymer flow during elevated temperature cures (21). These residues can be removed by quenching in 1% acetic acid rinse solution.

Patterning polyimide films in the pre-imidized state have yielded sloped vias as small as 2 microns square in a double level interconnect structure using 2 micron thick polyimide as the interlevel dielectric (13).

5. Complete Imidization of Polyimide

Complete imidization of most polyimides can be accomplished by a one hour bake at 250°C followed by a one-half hour bake at 325-375°C in air or nitrogen depending on the polyimide type. After a complete cure, films can withstand exposure to high temperatures such as 450°C for one half hour, a condition that may be reached during the aluminum to silicon annealing step.

As indicated earlier, films may be cured at temperatures as low as 200°C for several hours and still exhibit excellent electrical and mechanical characteristics. The dissipation factor of these films will be higher due to small residual amounts of solvent (ie, NMP) retained in the film.

There are a few techniques available which will monitor the percent imidization such that optimum curing temperatures may be determined. One of these involves monitoring the dissipation factor of the polyimide as it is cured. Figure 8 presents two curves of dissipation factor as a function of cure temperature for two different types of polyimides (24). The dissipation factor decreases with increasing cure temperature until full cure is reached and

then increases as decomposition starts to occur. Curing in nitrogen and air were investigated. Figure 8b shows that for polyimide D there is a substantial difference in the dissipation factor between curing in air and nitrogen where as polyimide A does not exhibit this effect. Hence, it is good practice to conduct all final cures in nitrogen atmosphere.

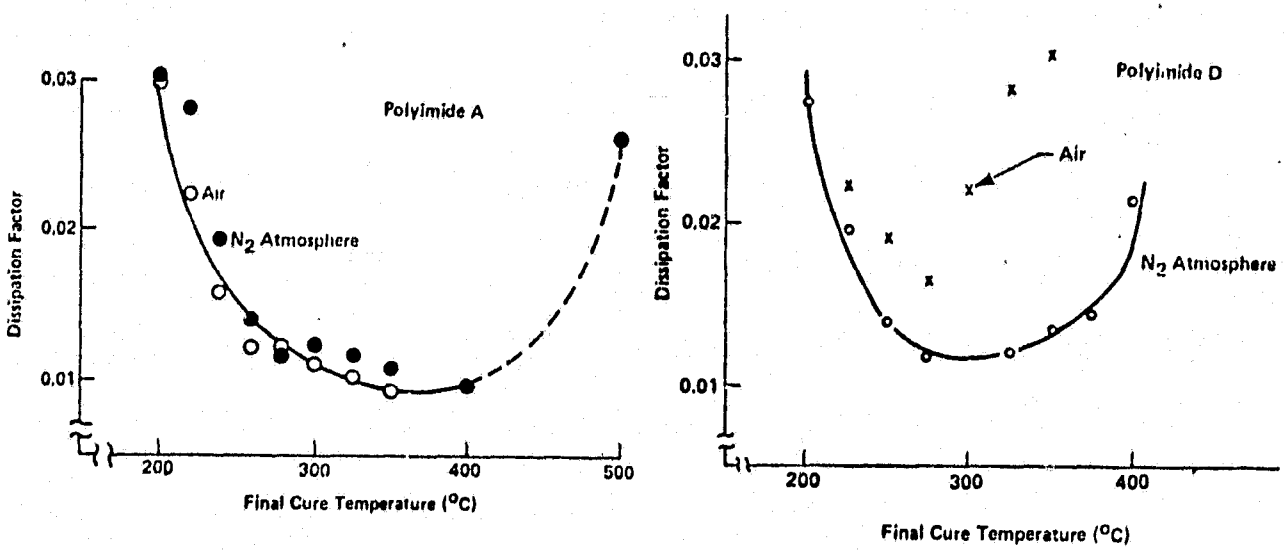
Another method used to monitor curing trends of polyimide involve measuring the moisture permeability of the films as a function of final curing temperature (19).

The water permeability data shown in Figure 9 shows the optimum cure temperature to be 350°C for Hitachi PIQ for both $O_2$ and $N_2$ atmospheres. Dupont PI 2545 and PI 2555 optimum anneal temperatures are a function of the atmosphere.

A similar technique as described has also been reported which monitors the water and chemical resistance of the polyimide as a function of curing temperature (28). They conclude, as above, that the optimum final curing temperature for Hitachi PIQ should be 325-350°C.

Chronogravimetric analysis of polyimide films is another method useful in defining optimum anneal conditions (19), where as differential scanning calorimetry, scanned thermal gravimetric analysis and differential IR spectroscopy are of little assistance.

By looking at the mass spectral analysis of outgassing products from a polyimide as curing temperature is increased, information about the imidization reaction can be learned. Figure 10 shows the mass spectral information for Dupont PI 2562 over the temperature




(A) (B)

Figure 8. Dissipation factor as a function of final cure temperature for (a) 1.5 μm film of Polyimide A, (b) 1.5 μm films of Polyimide D. Time at final cure temperature was 30 min.

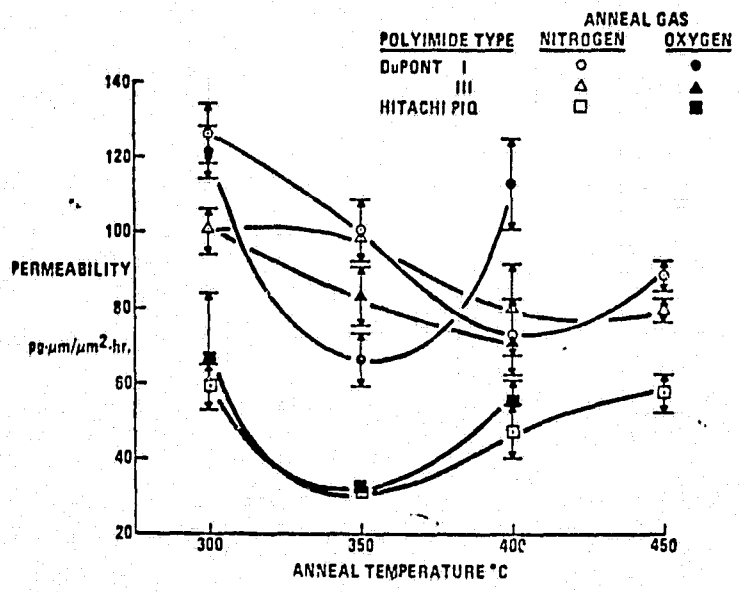



Figure 9. Moisture permeability properties of polyimide.

range of 100-450°C for water and solvent NMP(26). The solvent NMP is apparently bound to polymer since traces are observed at temperatures as high as 350°C despite its boiling point being 205°C. Water is released in two temperature ranges of 100-200°C and 300-450°C. The water released in the latter range might well correspond to H-bonded water proposed by Sasher and Susko (29).

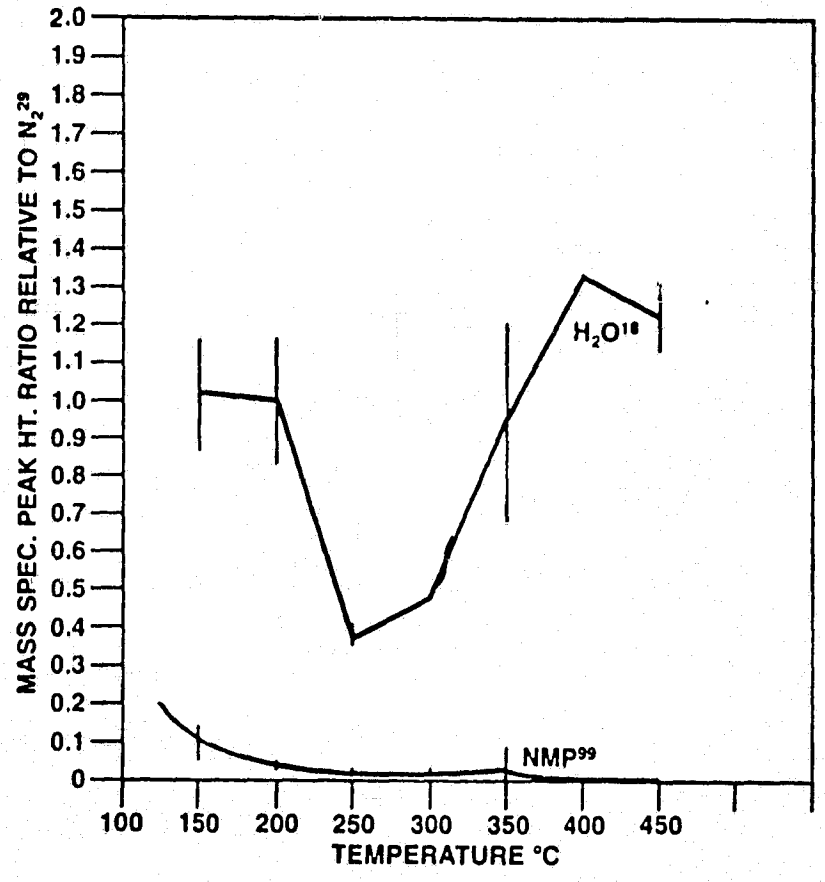



Figure 10. Mass Spectral peak height ratio for NMP and $H_2O$ vs. temperature (26).

As seen in Figure 7 relative to the weight loss by the polyimide during curing, this weight loss also represents a sizeable film shrinkage with curing temperature. It has been observed that almost all shrinkage after final cure is in the vertical dimension with negligible change in the lateral pattern dimensions (ie, vias) which were established before final cure (16).

6. Application of Additional Polyimide Coatings

It is often desirable to apply additional coats of polyimide over the initial cured coat as a means of decreasing pinhole density of the composite films and/or to realize thicker films such that parameters like parasitic capacitances may be reduced.

The intercoat adhesion obtainable between two layers of polyimide is a function of the polyimide type used and certain processing conditions. For example, the application of a coat of Dupont PI 2550 or PI 2555 over another fully cured coat of the same material renders excellent adhesion properties (as does PI-2525 and PI-2566). In fact mixing polyimide types for each coat still renders good results. However, coatings of PI 2540 or PI 2545 exhibited poor adhesion over fully cured layers of the same material. Better results are obtainable if the first coat is not fully cured prior to applying the second coat (31).

A procedure has been proposed for increasing the adhesion between two polyimide layers (32). In consist of treating the first fully cured layer in an aqueous solution of tetra-alkyl ammonium hydroxide (TAAH) salt, rinsing in water, and exposing to a dilute aqueous solution of acetic acid, followed by a second

water rinse. The second polyimide layer is then applied and cured. It is believed that this process enables a chemical rather than a physical bond between the two layers, thus increasing the adhesion.

7. Patterning of Fully Cured Polyimide

It is often more desirable to fully cure the polyimide layer (or multiple layers) before patterning instead of performing this step in the partially cured (or imidized) state as described earlier. If the polyimide is being used as an interlayer dielectric for a double level metallization process, via holes must be defined within it having bevelled edges to avoid step coverage problems where the upper metal crosses the via edge. If used as a passivation layer, bonding pad locations must be opened up to facilitate bonding operations.

As mentioned earlier, fully cured polyimides are impervious to essentially all acidic solutions, all known resist strippers and even hot sulfuric acid-hydrogen peroxide (PIRAHNA) solution (19). There are, however, a few caustic solutions which will effectively etch these fully cured materials.

If it is desired to completely strip the fully cured polyimide off the wafer without affecting any other component of the wafer (ie, for rework purposes), this can be accomplished using one of several possible solutions. (This is an advantage which polyimide has over most other insulating layers.) A solution of ethylenediamine heated to 60-90° will remove fully cured polyimide (27) but renders some side effects. An alternate procedure uses a

volumetric mixture of 10% oleic acid, 20% isobutylamine and 70% n-butylamine heated to 75°C. The wafer is placed in this solution for 4 hours and then soaked in isopropanol (33). A third solution consists of 50% N-methyl - 2-pyrrolidone and 50° n-butylamine by volume, heated to 78°C for one hour. The wafer is then soaked in toluene for 5 minutes and then isopropanol for 5 minutes (34).

For selective etching of fully cured polyimide using a wet etch, typically a negative photoresist layer is deposited and patterned, and etching is accomplished with a hydrazine-hydrate (11,9). Even though hydrazine is a toxic and highly pyrophoric liquid (it has been used in a rocket fuel), when used under controlled conditions it renders an excellent isotropic wet etch for these materials. The etch rate of hydrazine is not linearly dependent upon etch time, however, making it somewhat difficult to use. By adding an aminio-compound solution to the hydrazine-hydrate, Hitachi (35) has developed an etchant for their PIQ polyimide whose etch rate is linearly dependent on etch time as shown in Figure 11.

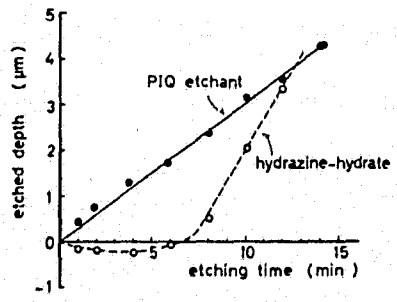



Figure 11. Chemical etching characteristics of 4μm fully cured polimide using hydrazine and PIQ etchant.

According to the model, with hydrazine, first a bloating or swelling of the polyimide takes place prior to polyimide removal where as with the PIQ etchant, amino-bonds are dissolved upon contacting the etchant.

Plasma etching is the most popular means of patterning completely cured polyimide films. A number of etching gases have been attempted, including $CF_4$, $CF_4 + O_2$, $CHF_3$, $BCl_3$, and $O_2$ (16). Of these, only $CF_4 + O_2$ and $O_2$ were effective in etching the polyimide. In fact, an etch rate of approximately 2000Å/minute can be realized in an $O_2$ plasma at a pressure of $500 \times 10^{-3}$ torr and a power of 300 watts for a barrel reactor. This turns out to be essentially the same etch rate for most positive photoresist types under the same etching conditions. Hence, if a positive photoresist is used as a mask, as is typically done, the resist layer must be considerably thicker than the polyimide layer. However, if both polyimide and resist layers are essentially the same thickness, then at the end of the etch cycle, most if not all of the resist layer will have been removed by the plasma thus eliminating the photoresist strip step. Figure 12 shows the oxygen plasma etch rates of partially and fully cured polyimide PI-2545 as well as positive resist AZ1350J and negative resist KTI-30. (36). It might be noted that due to the large differential in ash rate between the negative resist and the fully cured polyimide, plasma clean-up of negative resist is possible after wet etch patterning with negative resist.

In order to obtain good sloped via's in the polyimide layer for use in double layer metal applications, a positive resist layer of slightly greater thickness than the polyimide may be used. After

patterning the via's in the positive resist layer, a heat treatment may be used to bevel the resist profile (resist reflow) at the via edge. During etching, this profile is replicated into the polyimide since both are etched at the same rate during the plasma ashing sequence (14).

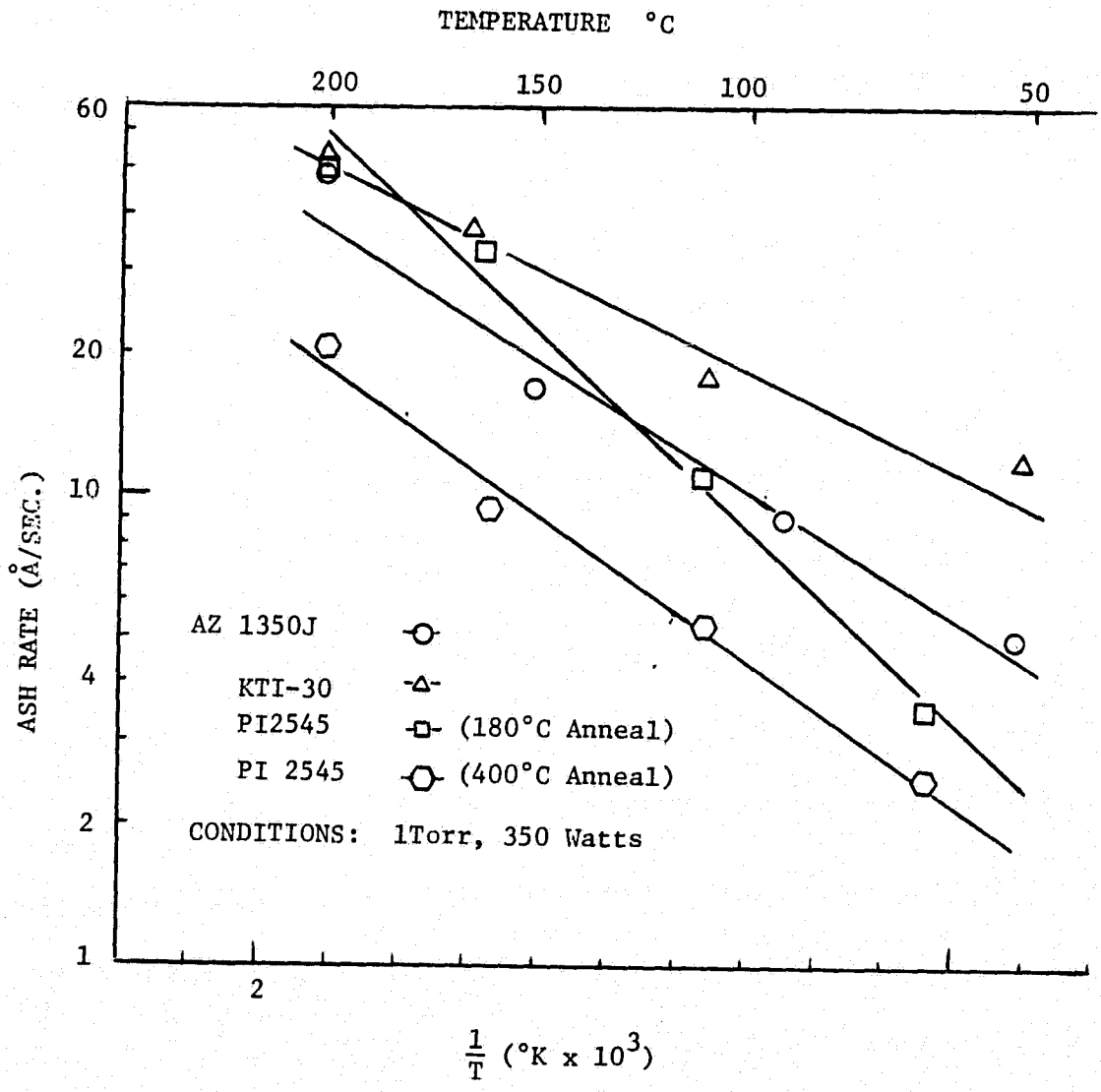



Figure 12. Oxygen plasma ash rate of polyimides and resists in a barrel reactor.

In addition to plasma ashing, reactive ion etching (R.I.E.) and reactive ion milling (R.I.M.) have also been used to pattern polyimides (26, 37, 38). Here, the degree of resolution desired determines the masking material. For large geometries (ie, 4-6 microns), hard-baked positive photoresist will suffice. A resist thickness approximately twice that of the polyimide is normally used, thus the resolution achievable is limited by the resist thickness necessary to maintain mask integrity. For smaller

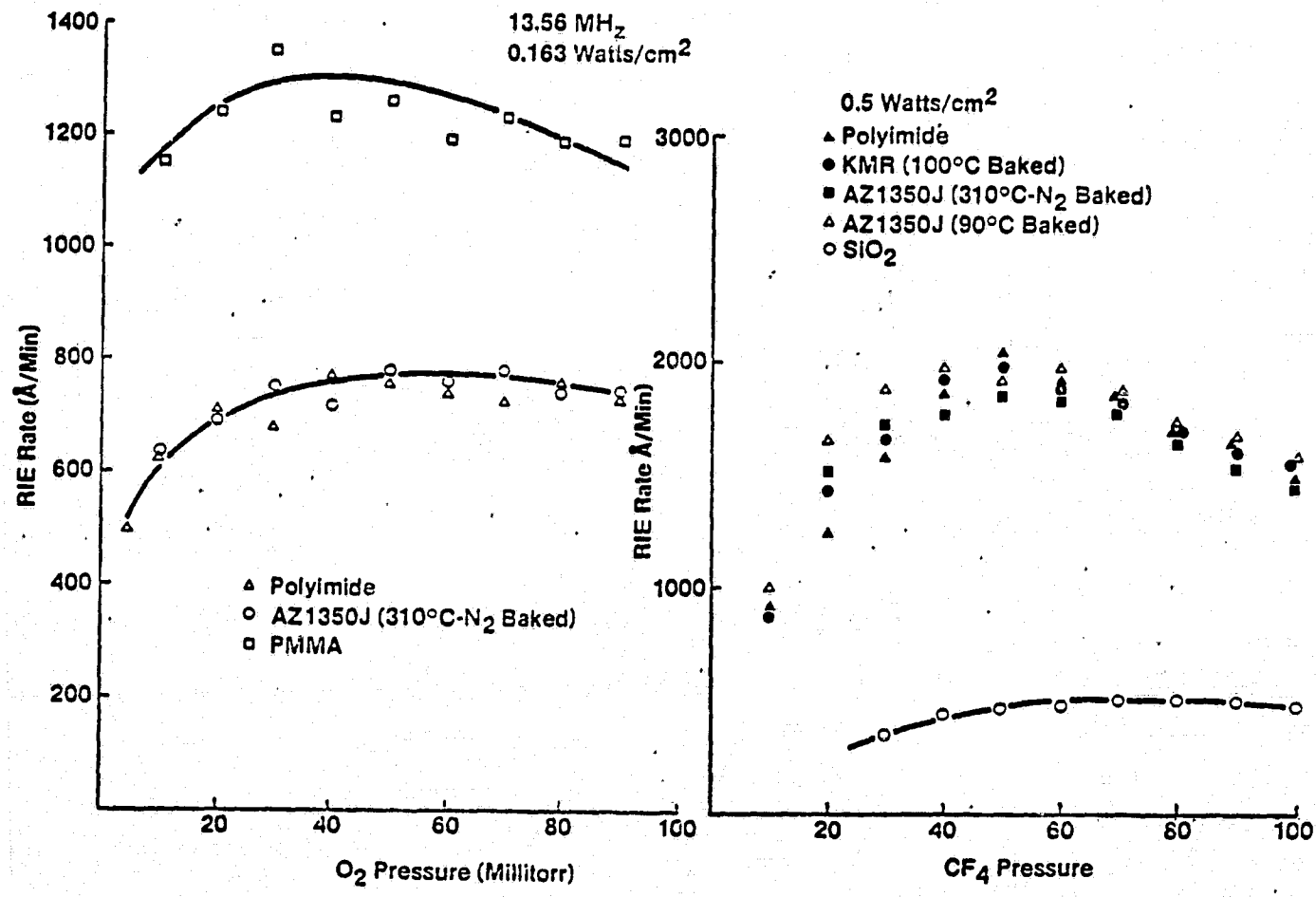



Figure 13. Reactive ion etch rate curves for a number of organic films.

geometries (ie, 0.5-3 microns), a thin layer of metal or inorganic insulator like plasma enhanced CVD SiN or $SiO_2$ may be first patterned using photoresist and then after stripping the resist, use the thin layer as a mask for RIE or RIM of the polyimide.

Reactive ion etching curves for a number of organic materials and $SiO_2$ are presented in Figure 13 (37). As seen in this Figure, the etch rates are considerably lower in $CF_4$ than in the $O_2$ plasma when at the same power levels. Also, it was observed that in an $O_2$ plasma, undercutting of the mask was observed as a function of pressure whereas for $CF_4$ plasma only vertical profiles resulted (37).

It has been proposed that only the directional etch techniques of reactive ion etching and reactive ion milling can be used to achieve 1 micron resolution and vertical walls in fully cured polyimide films (38).

G. POLYIMIDE PROPERTIES - MECHANICAL

A number of mechanical properties of fully cured polyimide have been published and/or empirically determined. These include (but not limited to) their physical, thermal, stress, adhesive, planarization and pinhole properties. In this section, these properties will be described.

1. Physical Properties

A listing of representative physical properties is presented in Table V for Dupont and Hitachi polyimide types (31, 28, 39, 20).

| | PI2540(PI2545) | PI2550(PI2555) | PIQ |
|---|---|---|---|
| Tensile Strength (ultimate) | 17,000 psi | 19,000 psi | 10.2 $kg/mm^2$ |
| Elongation | 25% | 10% | 9.5% |
| Density | 1.42 gm/cc | 1.39 gm/cc | 1.4 gm/cc |
| Refractive Index | 1.78 | 1.70 | 1.62 |
| Flexibility | 180°bend. no cracks (same for all polyimide types) | | |

TABLE V. A Comparison of Polyimide Physical Properties

The residual stress evaluated by measuring silicon wafer curvature on which the films are formed is compared to other inorganic dielectrics in Figure 14 for Hitachi PIQ (35). It is seen that the polyimide has relatively low tensile stress even for thick films. Hence, polyimides do not experience the cracking problems inherent in most thick inorganic films. Also, flexibility can be monitored as shown in Figure 15. It is found that polyimide films can endure 30 percent tensile strain which is one order larger than other dielectric films. These two properties of polyimides are advantageous for IC fabrication because, as mentioned, thick film formation, placing bonding pads over active regions of the device (11), and direct resin molding without cracks can be achieved.

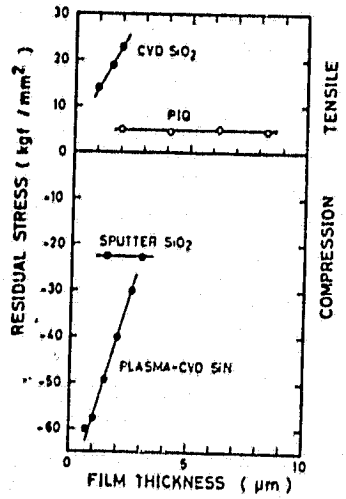



Figure 14. Residual stresses of inorganic and polyimide PIQ films.

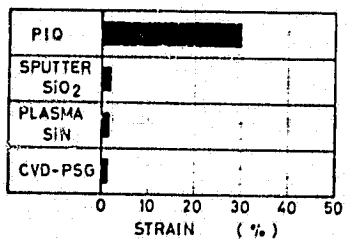



Figure 15. Breaking strain of dielectric films for film thicknesses between 1 and 2 microns

2. Thermal Properties

A listing of representative thermal properties is presented in Table VI for Dupont and Hitachi polyimides (31, 39)

| | PI2540 (PI2545) | PI2550 (PI2555) | PIQ |
|---|---|---|---|
| Melting Point | None | None | None |
| Weight Loss at 316°C in air after 300 hours | 4% | 4% | 0% |
| Final decomposition temp. | 560°C | 560°C | 575°C |
| Coefficient of thermal expansion | $2x10^{-5}$/°C | $4x10^{-5}$/°C | $2-7x10^{-5}$/°C |
| Coefficient of thermal conductivity | $37x10^{-5}$ $\frac{cal.}{cm\text{-}sec\text{-}°C}$ | $35x10^{-5}$ $\frac{cal.}{cm\text{-}sec\text{-}°C}$ | $40x10^{-5}$ $\frac{cal.}{cm\text{-}sec\text{-}°C}$ |
| Flammability | Self-Extinguishing | Self-ext. | Self-ext. |
| Specific heat | 0.26 cal/gm/°C | 0.26 cal/gm/°C | |

TABLE VI. A Comparison of Polyimide Thermal Properties

Also, it is instructive to compare these polyimide thermal properties with other commonly used inorganic materials. This is accomplished in Table VII (36). As indicated here, PIQ (and most other polyimides) matches the thermal expansion coefficient of aluminum better than any inorganic dielectric. Thus, it should serve admirably as an insulator for multilevel interconnection systems.

Another method of evaluating the heat resistance of polyimide is to monitor their weight loss and film thickness loss while under an elevated temperature ambient. Curves for these properties are shown in Figure 16 and 17 (39). In these figures, the commercially available polyimide resin is manufactured by Toray Industries, Inc.(3).

| ITEM<br>MATL | COEFFICIENT OF TERMAL EXPANSION<br>(1/°C), $10^{-6}$ | YOUNG'S MODULUS ELASTICITY<br>(GM/CM$^2$) $10^4$ | TENSILE STRENGTH<br>(GM/CM$^2$) $10^6$ | HEAT CONDUCTIVITY<br>$\frac{\text{mcal}}{\text{cm}\cdot\text{sec}\cdot{}^\circ\text{C}}$ | MELTING POINT<br>(°C) |
|---|---|---|---|---|---|
| PIQ | 20-70 | 300 | 1.7 | 0.4 | 500-550 |
| Si | 2.3 | 1.6 | 120 | 72-340 | 1420 |
| $SiO_2$ | 0.3-0.5 | 0.7 | 1.4 | 5 | 1710 |
| $Si_3N_4$ | 2.5-3 | 1.6 | 6.4 | 28 | 1900 |
| $Al_2O_3$ | 9 | 3.7 | 28 | 78 | 2050 |
| Al | 25 | 70 | 0.7-1.4 | 570 | 660 |

TABLE.VII. Comparison Between Thermal Properties of Polyimide PIQ and Inorganic Materials.

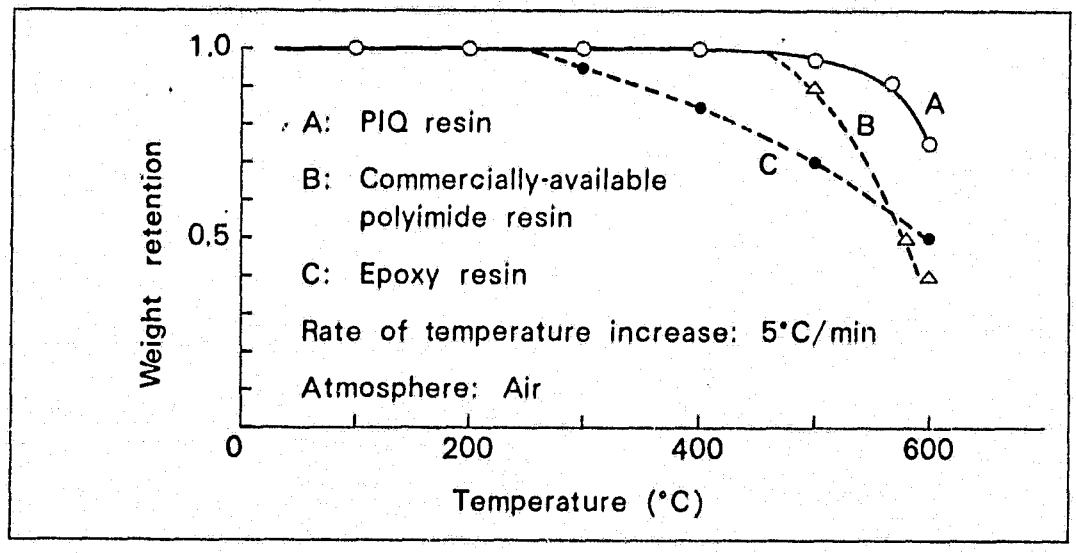



Figure 16. Weight loss under heat for polyimides and epoxy resins.

Due to the heat resistant additive of Hitachi PIQ, it normally exhibits better high temperature properties than other polyimides, not showing any initial weight loss until 460°C (28).

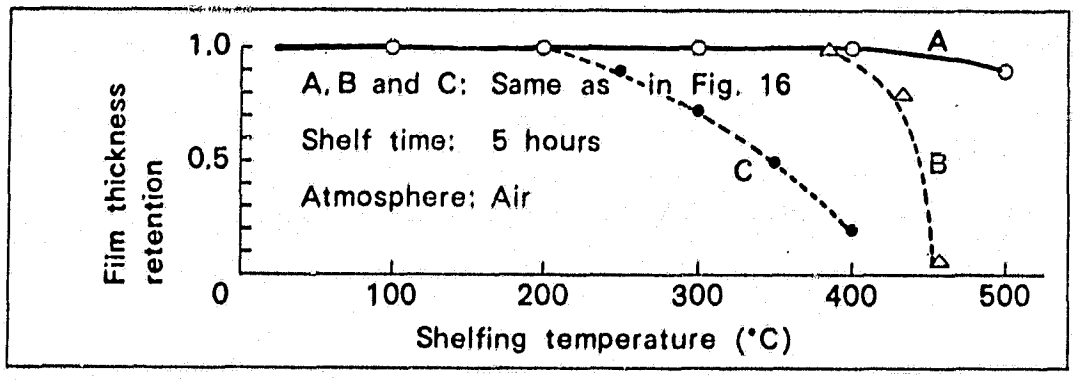



Figure 17. Film thickness loss under heat for polyimides and epoxy resins.

The thermal decomposition activation energy of PIQ films in nitrogen is 69 kcal/mole. Hence, cured aromatic polyimide films can withstand temperatures encountered in thermal compression bonding, eutectic die bonding and aluminum metallization and annealing.

As seen in Table VII, the thermal conductivity of polyimide at room temperature is rather low compared to other dielectric materials. While this is not detrimental for applications like interlevel insulator for multilevel metallization devices, it should be considered when using polyimide as a passivation material.

3. Adhesion properties:

As indicated in section F.1 on polyimide adhesion promoters, the use of a coupling agent greatly improves the adhesion properties of polyimides to silicon, silicon-dioxide, silicon nitride and phosphosilicate glass. Since one of the most important properties of these thin films is their adhesion to semiconductor substrates and metallurgy, as well as the adhesion of other materials to the polyimide film,considerable research has been undertaken to evaluate this parameter (24, 35, 21, 30).

A variety of procedures can be used to monitor polyimide adhesion to the substrate surface. One of the simplest (and crudest) methods involves the "Scotch tape" strip test. After applying the polyimide, scribe lines are etched in the polyimide and a very sticky Scotch tape is depressed down on top of the wafer. Moving in a direction perpendicular to the wafer, the tape is sharply stripped off of the wafer. If the polyimide adheres well to the substrate (ie, use of a coupler), then no polyimide squares are removed from the substrate. Similar test can be conducted after exposing the wafer to moisture or even a pressure cooker ambient (85°C, 80-100% relative humidity for a number of hours). It has been reported that no polyimide lifted using the scotch tape test for films using an organoaluminum coupler and exposed to 13 psi steam for 700 hours for substrates of aluminum and silicon nitride (40).

As indicated earlier, priming the wafer surface with an aluminum alcoholate, a collodial alumina or an organosilane promotes excellent adhesion of polyimide films. Dupont employees

(21) have used an organosilane of the type α-amino-propyltriethoxysilane (as used in VM-651) to study adhesion. They found a) equally good adhesion is obtained whether the coupler is air dried or baked at 130°C for 10 minutes, b) water must be present (95/5 methanol/water 0.01-0.05% solution of VM651 after setting for 8 hours at room temperature) to hydrolyze the silane and c) even though the final cure temperature of the polyimide (350-400°C) causes thermal decomposing of the organic segment of the silane, it has served its purpose of bringing the polyimide coating into intimate contact with the substrate surface. Films exposed to 230°F, 15 psi for several hours maintained good adhesion.

A more sophisticated method of monitoring adhesion involves using a peel force test apparatus (24). Using this apparatus, a constant peeling force may be applied to the film at an angle of 90° with respect to the plane of the substrate surface.

A typical peel force as a function of polyimide film strip width that the apparatus pulled on (and as attached to the substrate) is given in Figure 18. The slope of these curves (in gms per mm) is a relative measure of polyimide adhesion.

Figure 18 shows that adhesion tends to degrade after exposure to temperature-humidity stressing. Also, initial adhesion of polyimide to Si and $SiO_2$ surfaces was good; long exposure to stressing, however, tended to degrade the interface. It was found that silane adhesion promoters improved the long-term stability of the bond.

These test also indicated that the adhesion of aluminum over polyimide was satisfactory beforestressing with temperature



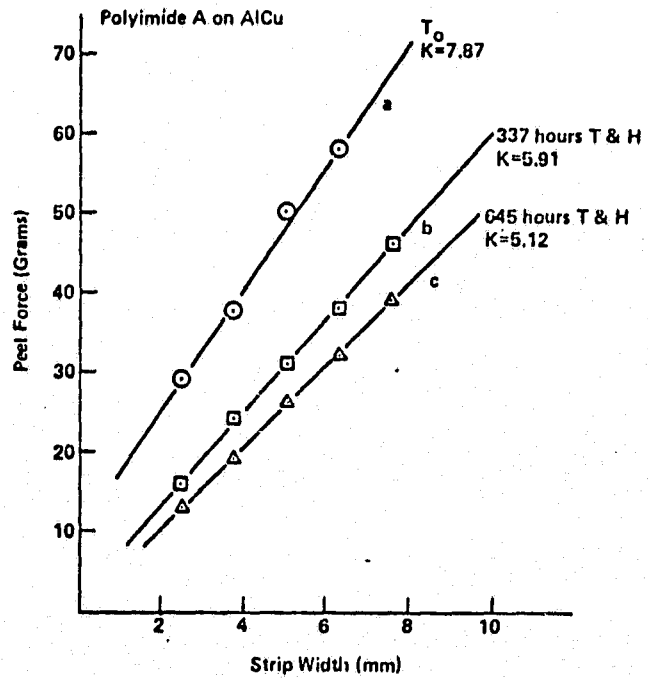


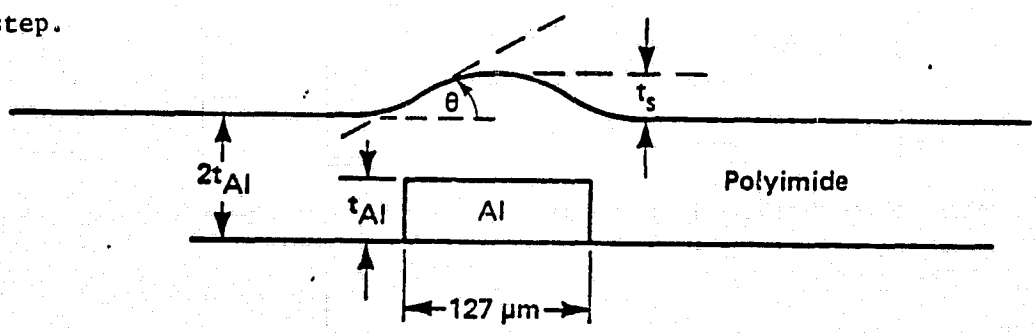

Figure 18. Peel force vs. strip width for polyimide A (PI-2540) on aluminum-copper alloy deposition, as a function of time in a temperature/humidity chamber. (a) initially K = 7.87 gm/mm, (b) after 337 hrs. at 85°, 80% relative humidity K = 5.9 gm/mm, (c) after 645 hrs. K = 5.12 gm/mm.

and humidity, but severely degraded after the stress cycle. An annealing cycle in dry nitrogen at 350°C would considerably improve this aluminum-polyimide adhesion.

4. Planarization:

For high density multilevel metal-insulator structures it is desirable to have a planar surface. It has been reported in the literature (3,11) that polyimides can be used as the insulator to provide such a planar structure. During the cure cycle for the polyimide film there is a tendency for flow to occur. Also, during the cure cycle there is a great deal of shrinkage due to solvent loss. It is the combination of shrinkage and flow during the cure cycle which provides polyimide films with the ability to planarize or smooth out any topological structures on a substrate.

The degree of planarization is determined by the ratio of the step height resulting with the polyimide film to the initial step height of the metal pattern as shown in Figure 19 (24). Another factor in the degree of planarization is the slope of the resulting step.




Degree of Planarization = $1 - \frac{t_s}{t_{Al}}$

Slope = θ

Figure 19. Degree of planarization for polyimide over a metal step.

In general, the degree of planarization is directly dependent on the thickness of the polyimide films. The slope of the polyimide over the metal land decreases with increasing polyimide thickness as shown in Figure 20.

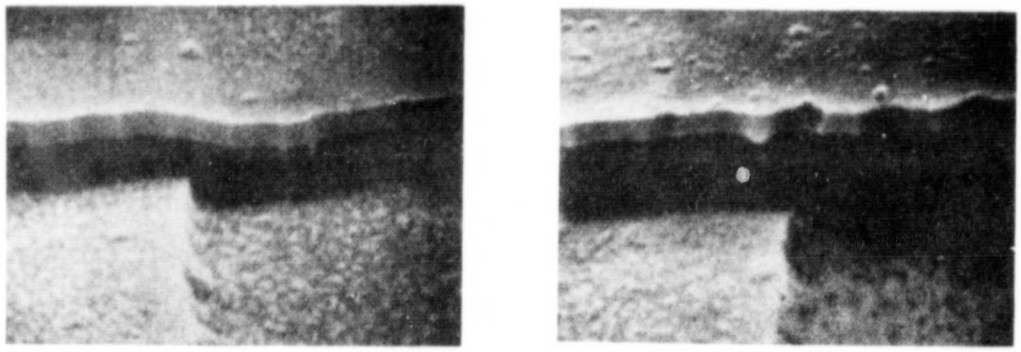


Figure 20. SEM pictures comparing the degree of planarization of two different polyimides having different thicknesses and different solid content. Magnification is approximately 6000X.

The degree of planarization is also dependent on both the width and spacing of the metal lines which the polyimide is covering, where better planarization is obtained for decreasing line width. In addition, there appears to be a correlation between the solid's content of the coating solution and the degree of planarization, where the higher solids content material provides more planarization,

Good edge or step coverage is obtainable with all types of polyimide films even when planarization is not achieved. This good edge coverage of polyimide films is an advantage over standard sputtered $SiO_2$ films deposited with a re-emission coefficient (41).

Typically $SiO_2$ films are somewhat conformal but have a tendency to cusp at the edges of metal lines resulting in poor edge coverage.

5. Pin-hole density:

An important property of an interlayer dielectric or a passivation coating is that it should be free of pin-holes. A couple of different methods may be employed in determining pin-hole density. One method deduces the pinhole density from the number of shorts in a statistical number of die each consisting of a fixed number of crossovers of first and second metal separated by a given thickness of polyimide (26). Another method involves an aluminum etch decoration technique to visually determine pin hole density (19). Here, the polyimide film is cast on a substrate comprised of a layer of 2000Å thick aluminum on blue colored field oxide with grid pattern for area computation. Replicate holes are etched in the aluminum (through the pinholes) by a hot phosphoric acid solution. With the polyimide film removed, good visual contrast of etched locations are achieved. Still another method of pin hole determination involves depositing a metal dot pattern on top of cured polyimide films and making electrical leakage to substrate measurements for pinhole density estimation (19).

As mentioned in an earlier section, by using a double layer of polyimide, pinhole density can also be reduced.

Figure 21 presents a measure of pinhole density of polyimide films prior to filtration as a function of film thickness (19). Other reported pinhole densities include 5 $cm^{-2}$ and 0.1 $cm^{-2}$ in 1 and 3 μm thick films respectively (13), less than 0.05 $cm^{-2}$ for 3.5 μm thick film (35), etc.

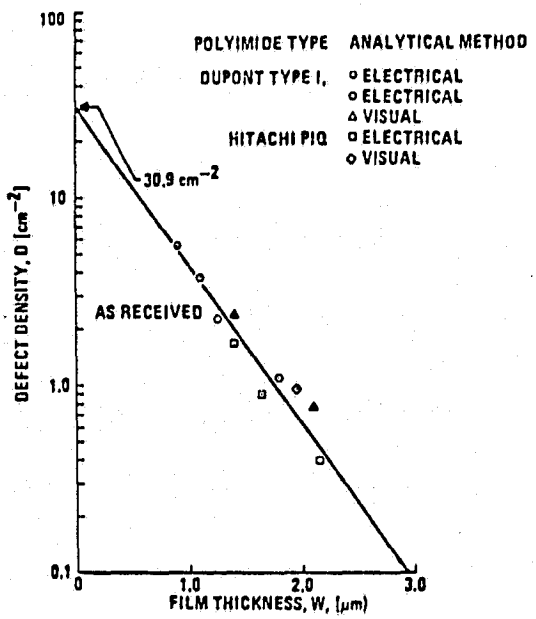



Figure 21. Film thickness dependence of polyimide pinholes

It has been reported (14) that for multilevel metal applications, the main cause of pinholes is not inherent in the polyimide but results from hillocking of the underlying aluminum during the heat treatment when curing the polyimide. Figure 22 shows the pinhole density when deposited on a copper-silicon doped aluminum. It is seen that pinhole density is more than two orders of magnitude lower than as deposited on pure aluminum, showing that the metallurgy which produces very little hillocking also produces low pinhole density.

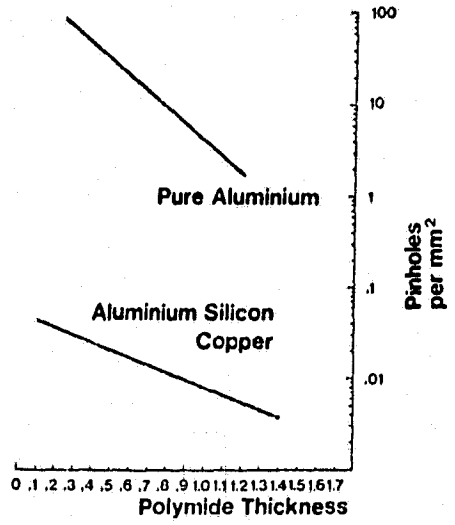



Figure 22. Pinhole density of polyimide films deposited over pure aluminum and silicon-copper doped aluminum.

## H. POLYIMIDE PROPERTIES - ELECTRICAL

The electrical properties of polyimide films have been thoroughly characterized. These include such items as dielectric strength, resistivity (volume and sheet), via resistance (contact resistance), DC conduction, mobile polar-ionic charge transfer, current-voltage characteristics, and the like. In this section, these properties will be described.

### 1. Electrical parameters - general

A listing of representative electrical parameters is presented in Table VIII for both Dupont and Hitachi polyimide types (31, 39, 35).

| | PI2540 (PI2545) | PI2550 (PI2555) | PIQ |
|---|---|---|---|
| Dissipation Factor (1kHz) | .002 | .002 | .002 |
| Dielectric Strength | 4000v/mil | 4000v/mil | 350v/μm |
| Volume Resistivity | $10^{16}$ohm-cm | $10^{16}$ohm-cm | $2x10^{17}$ohm-cm |
| Surface Resistivity | $10^{15}$ohms | $10^{15}$ohms | — |
| Dielectric Constant (1KHz)<br>(1MHz) | 3.5<br>3.75 | 3.5<br>3.75 | 3.45<br>3.8 |

TABLE VIII. Cured Polyimide Electrical Parameters

In addition, a comparison between Hitachi PIQ and other inorganic materials is presented in Table IX. Little fluctuation in dielectric constant is observed for these polyimide materials up to temperatures of 200°C (3).

| Item<br>Material | Dielectric Constant | Dielectric Breakdown Strength (V/cm) | Volume resistivity (Ωcm) |
|---|---|---|---|
| PIQ | 3.5-3.8 | $10^6$ | $10^{16}$ |
| Si | 11.7-12 | $10^5$ | - |
| $SiO_2$ | 3.5-4.0 | $10^6$-$10^7$ | > $10^{16}$ |
| $Si_3N_4$ | 7-10 | $10^6$-$10^7$ | $10^{12}$ |
| $Al_2O_3$ | 7-9 | $10^5$ | $10^{14}$ |
| Al | - | - | $2.5x10^{-6}$ |

TABLE IX. A Comparison of Electrical Properties Between Hitachi PIQ and typical inorganic materials used in the semiconductor industry (39).

2. Polyimide dielectric breakdown strength:

Normally, this breakdown strength is measured using a silicon-polyimide-Al dot structure on a given thickness of polyimide material. Also, the voltage applied to the structure is usually ramped at a 1-3 volts/sec. rate until breakdown occurs. Dielectric breakdown strength for filtered polyimide materials range from 5 to $7 \times 10^6$ volts/cm (24) depending on the type of polyimide used. This compares favorably with sputtered $SiO_2$ which renders a breakdown strength of $8.6 \times 10^6$ volts/cm. It should be noted that unfiltered raw materials render a breakdown strength in the low $10^5$ volts/cm range.

3. Dielectric constant:

As indicated above, the dielectric constant for most polyimide film which are fully cured is 3.4-3.5 when measured at 1K hertz and 3.7-3.8 when measured at 1M hertz. However, it has also been shown that dielectric constant (as well as dissipation factor) is a function of polyimide thickness as shown in Figure 23 (26).

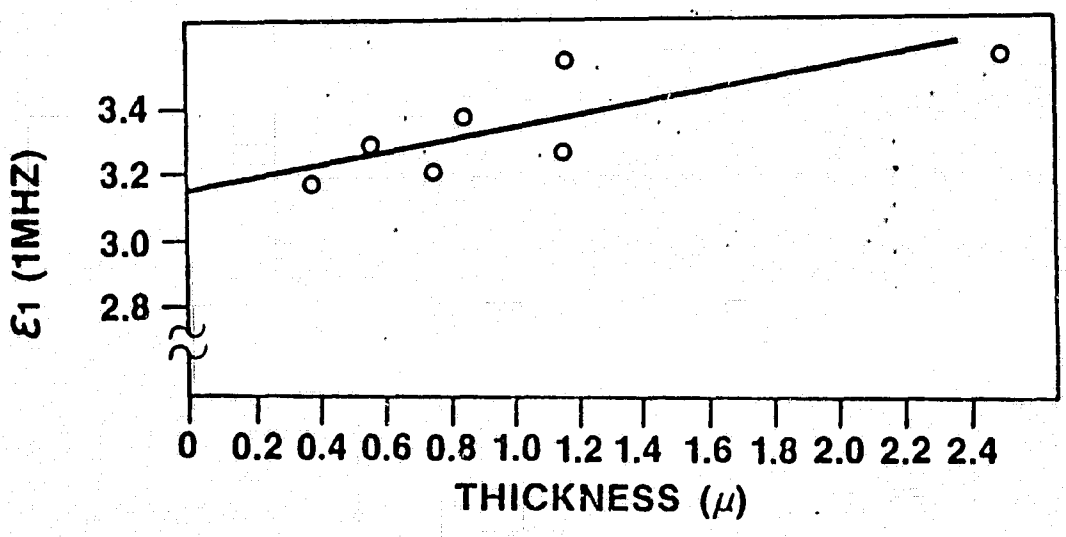



Figure 23. Dielectric constant ($\varepsilon_1$ at 1MHz) as a function of thickness for Hitachi PIQ films processed under constant cure conditions.

The films in Figure 23 were cured one-half hour each at 130°C, 200°C, and 350°C.

4. Bulk DC Electronic Conduction:

For measurements of conductivity, an Al-polyimide-Al dot structure is normally employed over a range of applied electric fields and temperatures. Raw log-current versus voltage data taken on low sodium-content Dupont PI2545 polyimide of one-micron thickness is shown in Figure 24 (42).

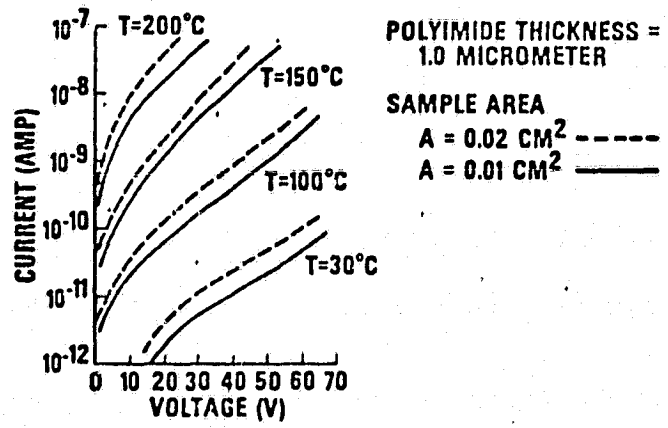



Figure 24. DC conduction in polyimide: Raw I-V data

The close factor-of-two relationship between the curves at each temperature is suggestive of a uniform bulk limited mechanism, as opposed to surface leakage. Reasonable reproducible data is obtained after an initial current passage apparently associated with contact formation. The data is characterized by two regimes, an ohmic region at low fields, below $10^5$ volts/cm, and a superlinear regime above that point. It is tempting to interpret this latter regime in terms of a Schottky emission mechanism for three reasons. First, the data fits a log I-$V^{\frac{1}{2}}$ dependence rather well, as shown in Figures 25 and 26.

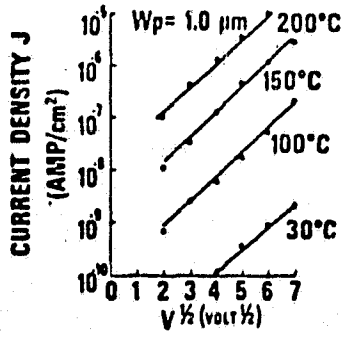



Figure 25. DC conduction of Duponts PI-2545 polyimide; Log $I-V^{\frac{1}{2}}$ dependence.

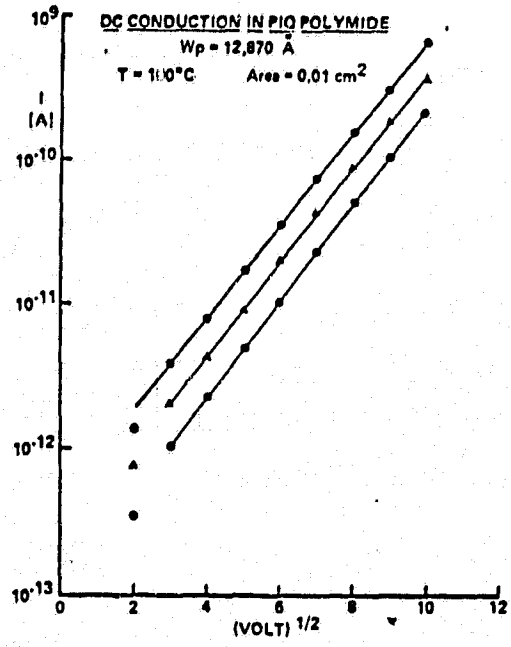



Figure 26. DC conduction of three different Hitachi PIQ polyimide thickness. Log $I-V^{\frac{1}{2}}$ dependence (43).

temperature. The upper curve (right hand) represents data from Figure 25 and lower curve from Figure 26. The thermal activation energy for this data is about 0.7 eV.

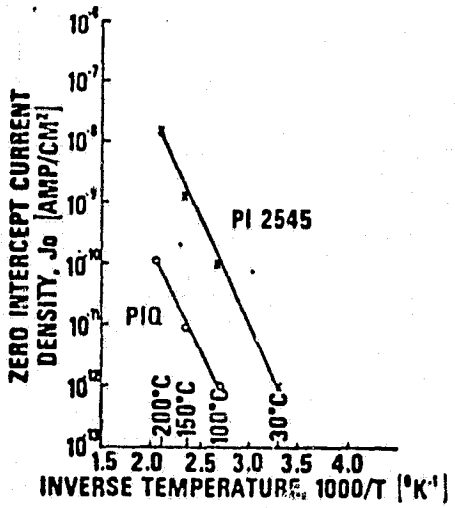



Figure 27. Temperature dependence of polyimide high field DC conduction.

While the bulk resistivities quoted in Table VIII are quite high, especially for organic polymers, they are none-the-less considerably lower than that of thermally grown silicon dioxide, particularly at low electric fields. For this reason, multilevel structures of polyimide over silicon dioxide biased under steady electric field stress will be subject to differential-conductivity-related charge transport and storage effects similar to those encountered in metal-silicon nitride-silicon dioxide-silicon devices (44). Such charge storage at the polyimide-oxide interface can potentially cause conductivity-type inversion of the silicon

Similar results have been reported for a large variety of polyimide films (24). Second, the slopes of the characteristics, particularly at lower temperatures, agree closely in magnitude with those predicted for the Schottky effect, that is (42)

$$\beta_s/kT = \frac{q}{kT}\left[\frac{q}{4\pi\varepsilon_o n^2 d}\right]^{\frac{1}{2}} \approx \frac{4.39}{n\, d^{\frac{1}{2}} T}$$

where

$\beta_s/kT$ = slope of the log $I\text{-}V^{\frac{1}{2}}$ plot

n = index of refraction of the film ≈ 1.4 from data

d = film thickness (cm)

T = absolute temperature (degrees K)

q = electronic charge

k = Boltzmann's constant

T = temperature .

The third, more subjective factor is the demonstrated sensitivity of the conduction to surface contact effects. On the other hand, the slopes of the higher-temperature curves in Figures 25 and 26 do not decrease following the 1/T dependence predicted by the above equation and the assumption of a uniform potential distribution through the film is questionable. The temperature dependence of the high-field conductance is described by the Arrhenius plot given in Figure 27, which shows the ordinate intercept current densities of the data of Figures 25 and 26 plotted versus inverse absolute

surface underlying second-level leads, posing a reliability hazard.

Figure 28 is a plot of low field polyimide resistivity versus inverse temperature in the range 100°C to 290°C. The data was taken from a large group of wafers, and shows considerable spread, reducing the confidence level in the 1.1 eV activation energy.

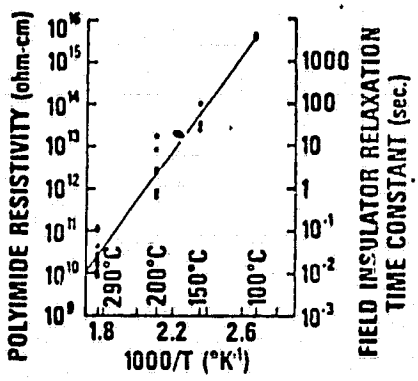



Figure 28. Temperature dependence of ohmic regime resistivity and field insulator relaxation time.

The resistivity values were derived from the simple relationship

$$\rho_p = R\,A/d$$

where

R = measured resistance of a unit

A = area of that unit ($cm^2$)

d = polyimide thickness (cm) .

The same curve may be used to describe the field insulator relaxation time constant using the scale shown at the right of Figure 28. The scale is derived from the equivalent circuit for a two-level field insulator structure, having a time constant given by

$$\tau = \rho_p \varepsilon_p \left[ \frac{C_o}{C_p} + 1 \right]$$

where

$\rho_p$ = polyimide resistivity

$\varepsilon_p$ = polyimide dielectric constant

$C_o, C_p$ = oxide and polyimide capacitances

and the values:

field oxide thickness = 1.0 micrometer

polyimide thickness = 2.13 micrometers .

It is seen that this relaxation will occur in only minutes at typical circuit test temperatures like 150°C.

Such dielectric relaxation would not necessarily be deleterious to device reliability if the system were completely linear and operated at constant temperature.

Under static bias stress, the field oxide interface will charge to the potential of the second-level leads on the polyimide surface, but a device might well be designed to withstant this inversion potential if the stored charge were removed completely when the bias was removed. However, if charge storage occurs in the polyimide or at the polyimide-oxide interface, or if the device is cooled under bias, charge will be trapped in the insulator, shifting the field threshold voltage of the device surface beneath

the lead. This effect is observed in Figure 29, where the shift in field threshold voltage of an NMOS field oxide test transistor incorporating 9000Å of field oxide and about 2 micrometers of Dupont PI2545 polyimide in its gate insulator (and aluminum gate electrodes) is plotted versus stress time with ±15 volts applied at temperatures between 100°C and 300°C and various times up to 1200 minutes.

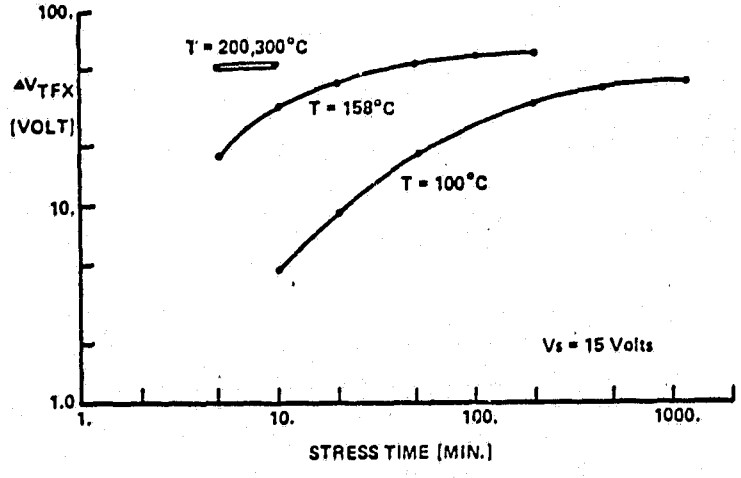



Figure 29. Field threshold voltage instability in polyimide multilevel MOS devices

The data shows that localized field inversion could occur in a matter of minutes under these conditions. Saturating shifts of approximately 50 volts is observed for all temperatures. Assuming ohmic conductance for the polyimide, negligible conductance for the oxide and complete polyimide-oxide interfacial charging, the field threshold voltage shift can be described by the relationship

$$\Delta V_{TX} = -\frac{C_o}{C_p} V_S \left[ 1 - \exp - \left( \frac{(C_o + C_p)}{R_p C_o C_p} t \right) \right],$$

where

$C_p, C_p$ = oxide and polyimide capacitances

$G_p$ = polyimide conductance

$V_s$ = stress voltage

$t$ = time under stress

The effective bulk polyimide resistivity can be extracted from comparison of the measured curves with this model, and values at 100°C and 158°C are plotted in Figure 30 versus inverse temperature. It is seen that both the values of the resistivity and the temperature dependence are in good agreement with those obtained from the dc conduction measurements. In addition, the saturated value of the measured threshold instability is well predicted by the model (43).

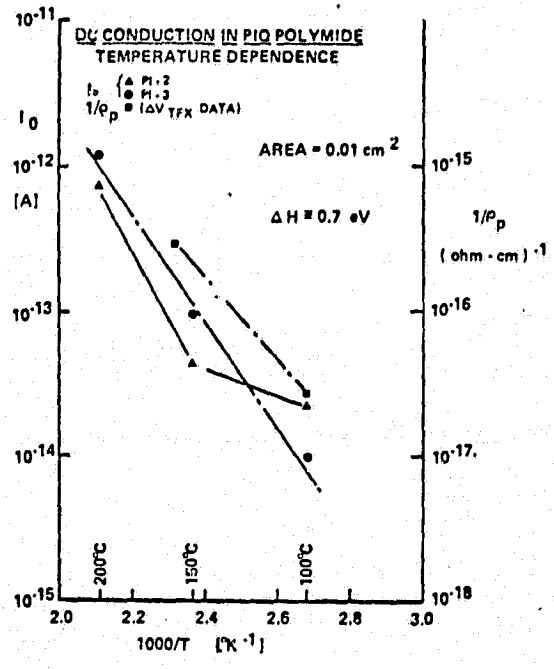



Figure 30. DC conduction and bulk resistivity for Hitachi PIQ polyimide as a function of temperature.

This electronic charge transport and trapping is by far the most serious problem in the application of polyimide films to multilevel interconnection structures. This liability can be limited by careful lead routing in circuit design and layout, limiting the use of polyimides to low voltage circuits (as is the present trend in VLSI), or by the use of electric field shield concepts in device processing (15). Other investigations into bulk DC donductance (38) have indicated the following:

a. Room temperature I-V characteristics are not consistent with classical conduction models in field range $10^5$ to $10^7$ volts/cm. Also, electrical reproducibility of I-V characteristics for thin polyimide films (<0.5 μm) appears to be a function of polymer/solvent chemistry.

b. In plotting the log of current density divided by electric field as a function of the square root of the electric field applied, a field induced irreversible shift in the I-V characteristic of both Hitachi PIQ and Dupont PI 2545 is observed. Neither characteristic is consistent with Frenkel-Poole or Schottky conduction, whereas they did follow a simple power law expressed as $J=aE^n$ for constant 'a'. The magnitude of the exponent 'n' is a function of the degree of stress applied to the polyimide.

5. Interface conductivity:

Lateral charge spreading at overcoat-field insulator interfaces has been recognized as a potential reliability problem in integrated circuit operation. A standardized test for this effect

has been proposed (45) which makes use of a MOS field test transistor commonly found on MOS integrated circuit chips. This test structure is shown in Figure 31, along with a plot of the initial drain conductance-gate voltage characteristics of the device as the solid curve. Stress is applied by raising the potential of the gate electrode above the threshold voltage at elevated temperature giving charge an opportunity to spread at the overcoat-oxide interface as indicated by the arrows. If such charge spreading does occur, a subthreshold drain conductance characteristic like the dashed curve will be apparent after stress. The zero-bias drain conductance shift, $\Delta g_{DO}$, for the polyimide are comparable to those seen with silicon nitride and phosphorus doped silicon dioxide overcoats, as seen in Table X.

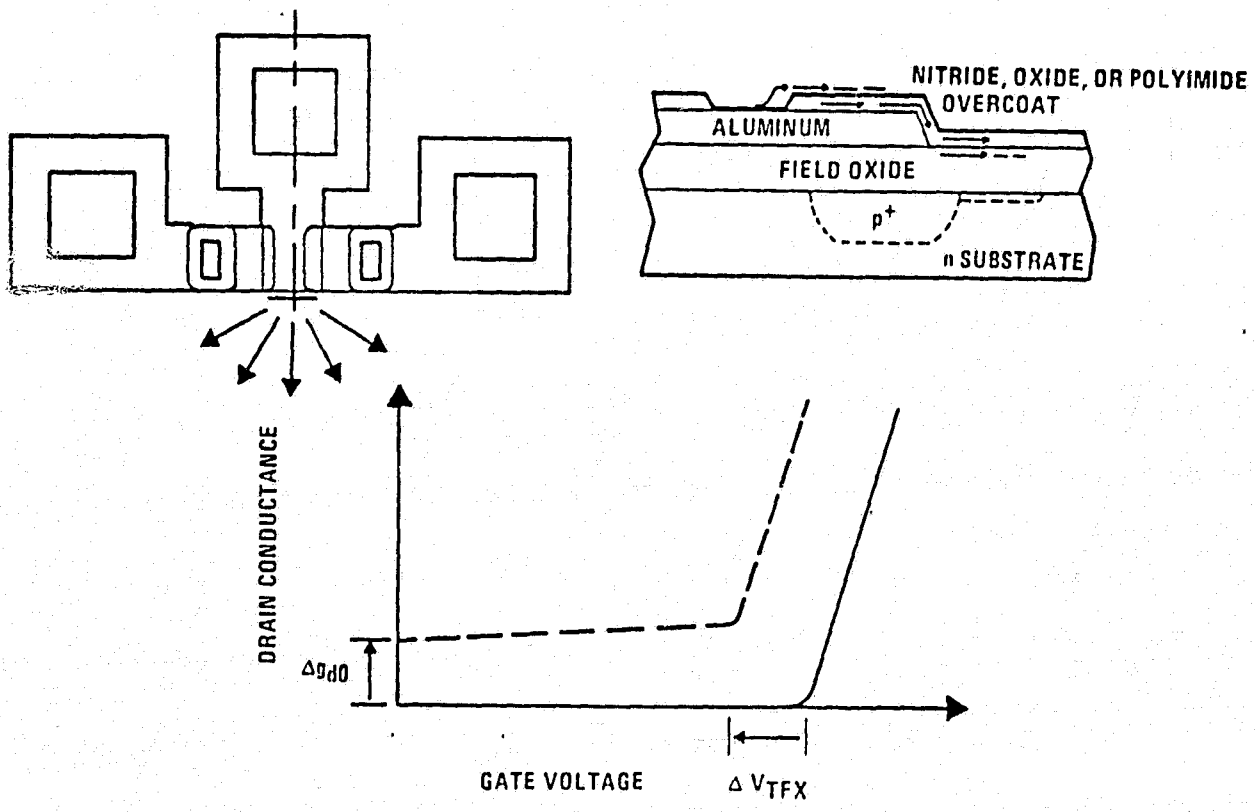



Figure 31. Lateral interface charge spreading test setup.

| OVERCOAT MATERIAL | $\Delta g_d(0)^*$ [μmho] |
|---|---|
| Polyimide (PIQ or PI2545) | $10^{-5}$ - $10^{-1}$ |
| Silicon Nitride | $10^{-5}$ - $10^{-3}$ |
| Silicon Dioxide (Phosphorus Doped) | $10^{-5}$ - $10^{-2}$ |
| Sputtered Quartz | 1 - 10 |

*Stress condictions: $T_A$ = 300°C, t = 15 min, $|V_s| = |V_{TFX}|$ +10 volts

TABLE X. Lateral Interface Conductance Test Results (43)

6. Contact resistance in polyimide vias:

Very often, a via (physical contact between top and bottom metal levels through an opening in the dielectric) will experience a high resistance due to poor ohmic contact between the two metals. This high contact resistance (sometimes referred to as an 'invisible shield') is believed to be due to a contamination layer generated on the bottom metal surface during either wet chemical or dry plasma etching of the via in the dielectric layer. This contact resistance can be broken down if the interconnect system is sintered at a temperature exceeding the 'via temperature' (14), which typically is in the range of 350° to 450°C as seen in Figure 32.

For plasma etched dielectrics, the high contact resistance is believed to be due to a thick aluminum-oxide which is chemically protected by a redeposited carbonaceous film. In the case of wet etching, the contamination appears to be a residue of polyimide and/or adhesion promoter.

To eliminate this invisible shield, it has been proposed (46)

a. for dry processing, first remove the protective carbon film by placing wafers in a low pressure plasma (i.e., 50 microns, 100 watts for 2 minutes), and then removing (or at least thinning) the oxide using buffered HF or phosphoric acid to achieve a clean surface.

b. for wet chemical processing, remove the organic layer by a sulfamic acid treatment or a low pressure plasma as above.

c. prior to depositing the second level metal, do an in-situ back sputter to clean out the vias.

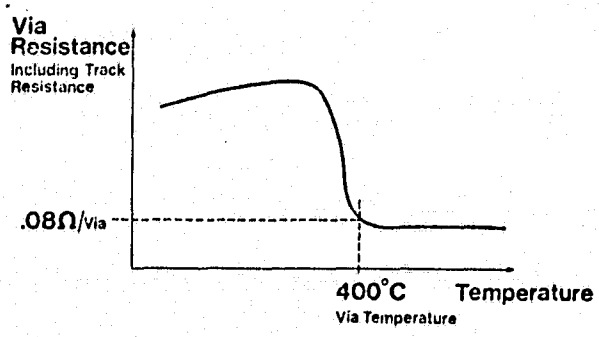



Figure 32. Typical characteristic of a via resistance vs. sinter temperature.

## I. POLYIMIDE PROPERTIES - RELIABILITY

Long term reliability of polyimide dielectrics for use either as an interlayer dielectric in multilevel metal applications or as a passivation layer must at least be comparable to if not superior to those materials presently used in the industry today, the most common being atmospheric CVD deposited $SiO_2$. In this section, reliability relative to environmental testing, moisture penetration and retention, contamination and thermostability of polyimide parameters will be discussed.

### 1. Environmental Testing

a. Effects of moisture: Some of the first environmental testing reported on polyimide materials was conducted on covering nichrome resistors with a polyimide protective coating (8). Even after laser trimming of the resistor through the polyimide coating, test lasting 4000 hours in a 95% relative humidity (R.H.) at 50°C showed little to no detrimental effect to the resistors (uncoated resistors exhibited dissolution of the nichrome in the resistor yielding large resistance changes). Hitachi has published results of humidity testing on a three level interconnection test pattern for 300 hours in steam at 120°C under two atmospheres of pressure (47). While unexposed aluminum areas experienced severe corrosion, area covered by their PIQ polyimide exhibited no corrosion. Also, testing of their multilevel color TV chroma chip at 90% R.H. and 80°C for 1000 hours indicated no failures by using polyimide as interlayer dielectric and as passivation coating.

A second Hitachi publication (48) compared the hygroscopicity

properties of polyimide and CVD $SiO_2$ and found them to have similar properties, both absorbing $10^{20}$ to $10^{21}$ molecules/$cm^3$ of water (from mass spectrometer data). In terms of moisture permeation (to attack underlying structures), polyimide exhibited better characteristics even under pressure cooker testing. It is difficult to discern whether material permeability or density of pinholes, cracks and other defects in the two materials was being tested.

In comparing polyimides with other insulating materials (27), polyimides moisture-vapor transmission is 0.54 g/mil ($in^2$) in 24 hours, as compared to 1.0 for Parylene C, 1.9 for Mylar, 14 for Parylene N, and 121 for RTV (room-temperature-vulcanizing silicon rubber). Also, polyimide films are an effective barrier to gases. For example, oxygen permeation through silicones is about 60-440 Barrer, compared to 5.9 for Teflon FEP, 0.68 for cellulose acetate, 0.18 for Parlene N, and 0.15 for polyimide.

Another accounting reports that the application of two coats of polyimide passivation (3 microns) over linear devices subject to pressure-temperature-humidity-bias (PTHB) conditions provides twice the mean time to fail compared to one micron of phosphosilicate glass (26).

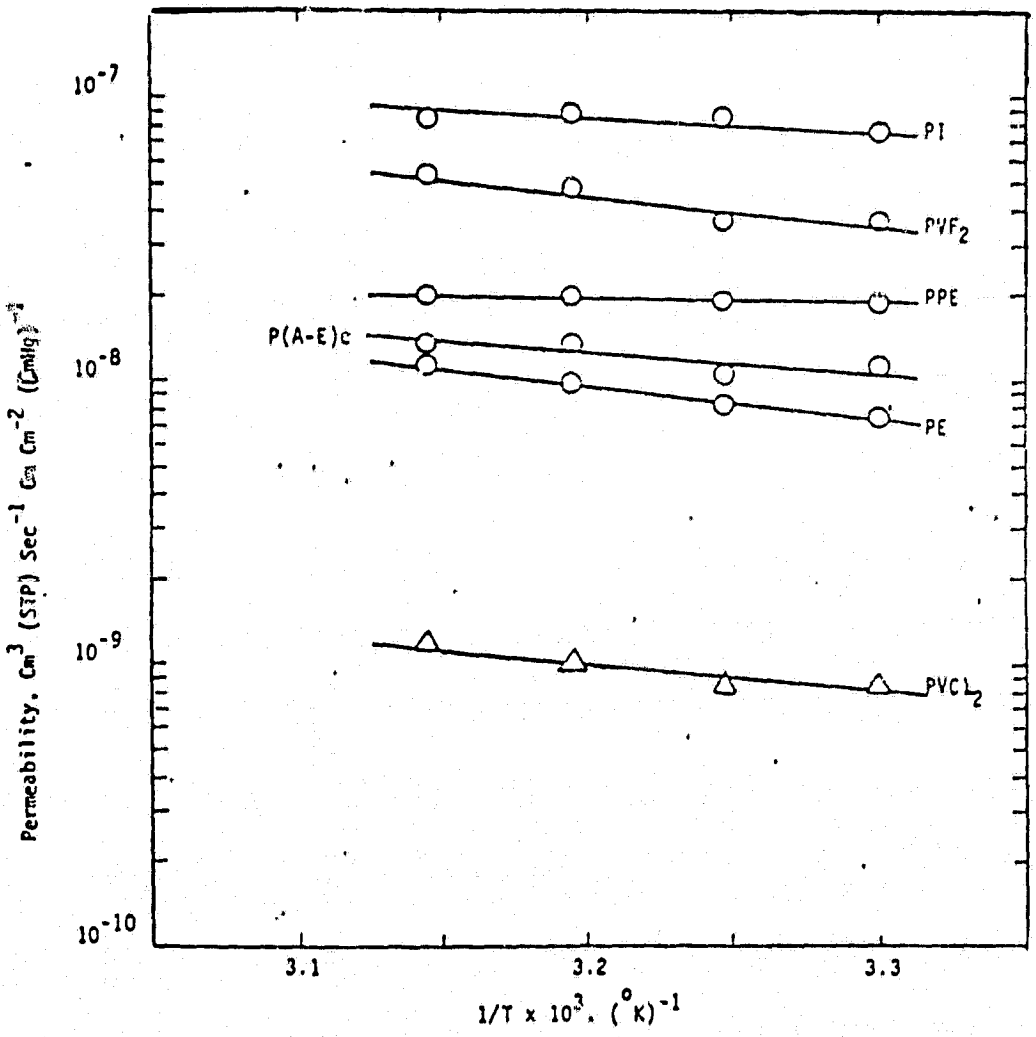
The influence of moisture on packaged components is shown in Table XI, which considers the combined influence of passivation layers and plastic encapsulants on aluminum corrosion at 110°C, 90% relative humidity and 30 volts bias (52).

| ENCAPSULANT | PASSIVATION | MEDIAN LIFE (HOURS) FAILURE MECHANISM | |
|---|---|---|---|
| | | ANODIC | CATHODIC |
| NONE | NONE | 250 | 500 |
| | NONE | 270 | 1600 |
| | $SiO_2$+ 0%P | 550 | 3000 |
| EPOXY NOVOLAC | $SiO_2$+ 1.8%P | 900 | >1250 |
| | SILICON NITRIDE | 70 | 75 |
| | POLYIMIDE | >1500 | 1150 |

TABLE XI. Corrosion of Aluminum Due to Moisture Penetration Through Encapsulation and Passivation Layer at 110°C, 90% Relative Humidity and 30 Volts Bias.

In considering polyimide as a passivation layer, the permeability of polyimide films has been compared to other polymer coatings as shown in Figure 33A. Notice that the permeability of polyimide film is about two order of magnitude higher than polyvinylidene chloride (53). The straight line characteristics observed in Figure 33A clearly indicate that the transport of water molecule through polyimide film is diffusion controlled.

Also, moisture transmission through a polyimide film depends on how the polyimide is cured as seen in Figure 33B. Here, a plot of water loss versus time for three different cure processes A, B, and C indicate that process C is superior in resisting moisture permeation as compared to that of process A and B. Coatings which can prevent or reduce corrosion is always of interest to device fabrication. Results of Table XII show that polyimide is an effective coating in this regard. Three sets of chip samples were separately passivated with $SiO_2$, $SiO_2$ + polyimide and $Si_xN_y$ + polyimide.




PI = Polyimide
$PvF_2$ = Polyvinylidene Fluoride
PPE = Plasma Polymerized Ethane
PE = Polyethylene
P(A-E)C = Polyacrylic acid-ethylene Copolymer
$PVCl_2$ = Polyvinylidene Chloride

Figure 14.

Figure 33A. Permeability of several thin film polymers.

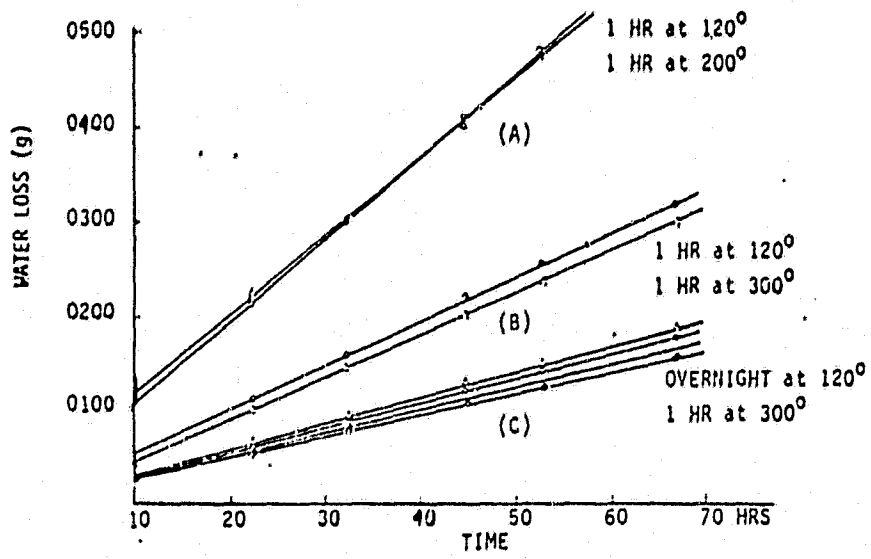



Figure 33B. Effect of curing process on the moisture transmission of polyimide coatings for Duponts PI-2540. Measurements are carried out at 41°C and 81% relative humidity.

They were tested in a salt atmosphere for 6 hours. The ratio of the number of failures to the number tested (Fail/Sample) was 36/36, 6/49 and 0/52 respectively (53). It is clear that the combination of $Si_xN_y$ and polyimide provides the most effective passivation to an integrated circuit chip in this experiment.

| | |
|---|---|
| Test Conditions | Salt Atmosphere |
| Test Time | 6 Hours |
| Results (Fails/Sample) | 0/52 ($Si_xN_y$ + Polyimide) |
| | 0/49 ($SiO_2$ + Polyimide) |
| | 36/36 ($SiO_2$) |

TABLE XII. Corrosion Test Results for Salt Atmosphere at 6 Hours Duration.

A chemical procedure has been developed which will reduce the susceptability of polyimides to moisture permeability (49). This process involves grafting a surface layer on top of the polyimide coating after it is fully cured. This grafting operation has minimum effect on the properties of the polyimide layer.

b. Contamination

i) ionic contamination due to incompletely cured polyimide: For incompletely cured polyimide coatings, one may postulate that dipoles associated with the unformed polymer linkages will align themselves under E-field application such that the positive dipole species is closest to the silicon. This would lead to inversion of the surface of p-type silicon (n-channel devices) and hence, produce unwanted leakage.

Special n-channel FET memory chips with non-random, purposely etched passivation defects have been used to ascertain the effect of incomplete cured polyimide on the products functional reliability (25). Figure 34A illustrates the basic FET flip-flop memory cell, where the dashed resistor (and associated leakage current) is a direct function of the polyimide induced inversion layer.

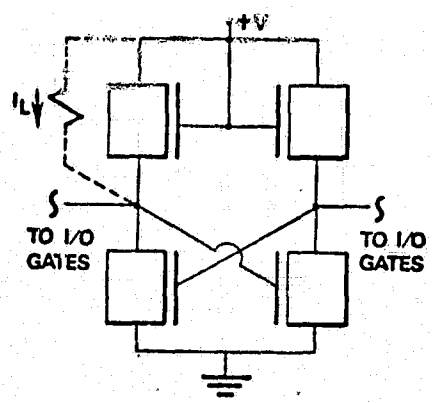



Figure 34A. Cell with inversion-induced resistor due to incompletely cured polyimide.

The polyimide was cured at 300°C (hot plate) for five minutes (insufficient temperature and time to result in "fully" cured polyimide) and then stressed at 40, 85 and 130°C. The results are presented in Figure 34B, where the 40°C cell showed no failures and the 130°C failure decrease with time due to the curing tendency of the polyimide at that temperature and time.

For completely cured polyimide layers (as determined by dissipation factor data), the failure rate for these cells was less than 10 percent when stressed at 85°C for 10,000 hours even though the sodium content in this polyimide type was in the 7 to 10 ppm range (i.e., sodium must be practically immobile in fully cured polyimides).

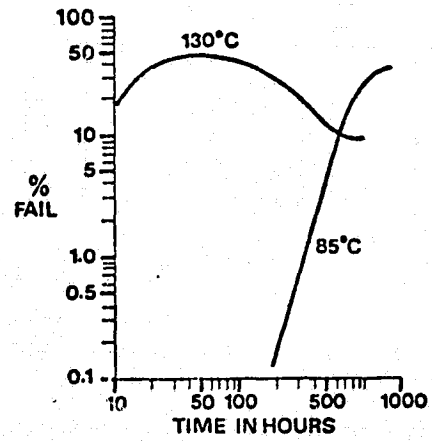



Figure 34B. Percent fail (cell non-functional) versus time under stress on 85 and 130°C.

C-2

ii) Sodium barrier characteristics:

Sodium ion conductivity is difficult to measure in polyimide-on-oxide structures because under static bias, the electronic conductivity of the polyimide rapidly bucks out the electric field driving the ion drift in the film. To circumvent this, a ramp voltage-integrated charge technique has been adopted, which establishes a small but steady electric field in the polyimide for an extended period and permits separation of electronic and ionic components of conductivity (42). Figure 35 shows the test structure for the sodium ion barrier measurements. Figure 36 displays the operation of the method. If a voltage ramp is applied to a composite polyimide-$SiO_2$ capacitor at room temperatue (25°C) where conductivity components are negligible, a linear charge-voltage relation is seen having a slope equal to the series combination of the oxide and polyimide capacitances. At elevated temperatures, the slope increases, approaching the value of the oxide capacitance, which indicates that the polyimide is now acting as a resistor charging the underlying oxide capacitance. If the sample is free of mobile ionic contaminant, the Q-V plot will follow the curve A-B-C'. To measure sodium ion conductivity, a contaminant layer is applied between the polyimide surface and the metal electrode, and the sample is held under bias at point A while heating to test temperature and until the voltage across the polyimide layer is reduced to zero. When the ramp is started, a positive bias develops across the polyimide permitting ion drift toward the oxide-polyimide interface. At point B near zero volts,

field reversal occurs in the oxide, and any ions collected from the polyimide or the oxide will drift rapidly toward the silicon surface as the curve goes to point C. Reversal of the ramp reverses the process. Key to the technique is the fact that field reversal occurs in the polyimide at points A and C and in the oxide at points B and D. Such experiments have been performed on samples built with 1060Å of $SiO_2$ coated with 1-2 μm of Hitachi PIQ or DuPont 2540 polyimide cured at 300°C for 4 hours in air. For comparison, samples were also prepared with silicon nitride coatings plasma deposited in both tensile and compressive modes. Samples from each coating group along with oxide pilots were contaminated using a sodium lauryl sulfate spin-on solution calibrated for a sodium contamination level of about $2 \times 10^{13}$ ions/cm$^2$. Aluminum electrodes were applied to all units. Table XIII gives the results of charge-vs-voltage drift measurements at 250°C on control and contaminated samples. While the polyimide samples displayed fairly large values of ion drift, the contaminated samples were overall not significantly higher than the controls, and both were well below the contamination level. It is thus concluded that the polyimide, once cured, provides an effective ion barrier under these conditions, but that the underlying oxide may become contaminated during film application and curing. The silicon nitride samples also displayed good ion barrier properties in this test, and showed much less evidence of process-induced contamination. Static-bias MOS C-V stress testing was done on some of the samples to demonstrate potential errors in interpretation of this type of data.

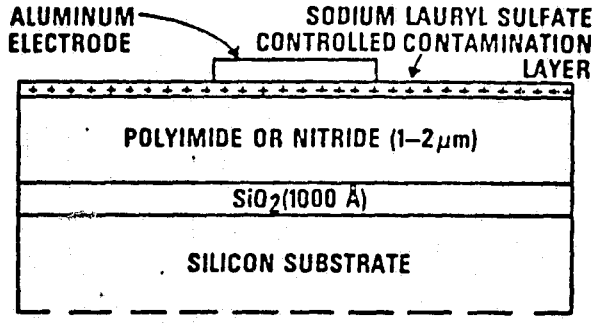



Figure 35. Test structure for sodium ion barrier measurement.

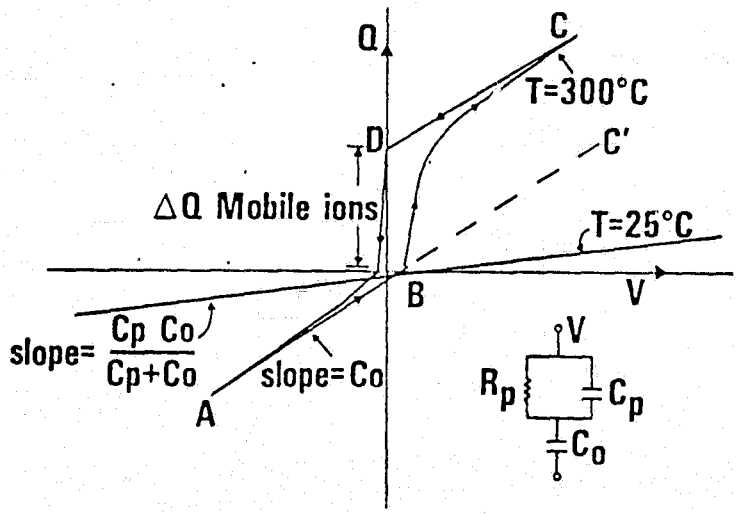



Figure 36. Ramp voltage-Integrated charge measurement technique [Q-V plot] (42).

| PROCESSING | $W_{INS}$ (Å) | Δ Q DRIFT (IONS/CM$^2$) | |
|---|---|---|---|
| | | CONTROL | CONTAMINATION |
| Oxide Only | 1,060 | 1.3E11 | 2.4E13 |
| PIQ on Oxide | 18,500 | 1.4E12 | 3E12 |
| DuPont 2540 on Oxide | 13,800 | 8E12 | 7E12 |
| Compressive Nitride on Oxide | 7,400 | <1E11<br>8E12(C-V) | <1E11<br>2.8E12(C-V) |
| Tensile Nitride on Oxide | 3,000 | <1E11<br>3E12(C-V) | <1E11<br>3E12(C-V) |
| ALL DRIVE MEASUREMENTS AT 250°C USING SLOW RAMP Q-V TECHNIQUE<br>CONTAMINATION: SODIUM LAURYL SULFATE SPIN-ON | | | |

TABLE XIII. Charge Transport Data on Polyimide and Silicon Nitride Overcoat Structure

2. Thermostability

The thermal life of a particular material cannot be described in simple numbers because each particular application has its own criteria for failure. For example, dielectric breakdown is the mode of failure for an electrical insulation in motors but loss of elongation is the cause for flexible cable failures. The thermal breakdown of polyimide is known to proceed according to at least three different mechanisms. The deterioration in air can be attributed to a radical-initiated oxidation (above 300°C). At lower temperature and high humidity, the predominating reaction is hydrolysis. In the absence of air and moisture, the polyimide degrades through a pyrolytic reaction. The principle constituents of out gassing are CO and $CO_2$. Since radical-initiated oxidation can be catalyzed by the presence of transition metals, the nature of the substrate will have a profound effect on the thermal life of the film in air.

Thermogravimetric analysis, though not necessarily indicative of all high temperature properties, is a convenient way to indicate the degree of thermal reaction occurring at a particular temperature.

The weight loss of polyimide coatings at thicknesses of 6-12 μm on wafers and on aluminum (sputtered on) at 450°C and 500°C in air and in $N_2$ were determined. Weight loss data on the same films stripped off from the wafers may be used as controls. Figure 37 lists the experimental results. These results show that the thermal life of the polyimide film is not affected by the presence of $SiO_2$. The aluminum coated polyimide actually showed a lower weight loss in air even assuming all the aluminum has been oxidized to

aluminum oxide. One possible explanation is that at 500°C, the oxygen in air reacts with aluminum preferentially, thus reducing the concentration available to attack the polyimide film.

As expected, the weight loss in $N_2$ is much less than in air. This is consistant with the expectation that the pyrolytic reaction of polyimide should have a much higher activation energy than the radical-initiated oxidation.

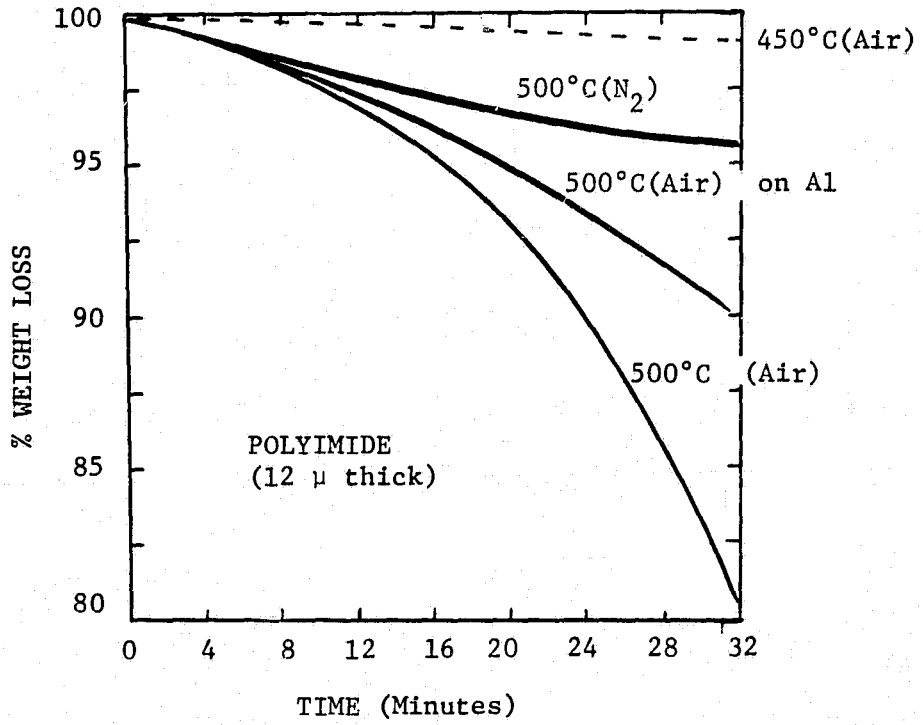



Figure 37. Weight loss of polyimide under different curing conditions (30).

In addition, Figures 38, 39, 40 present results of thermal aging on dielectric strength, volumn resistivity, elongation and tensile strength for polyimides (50).

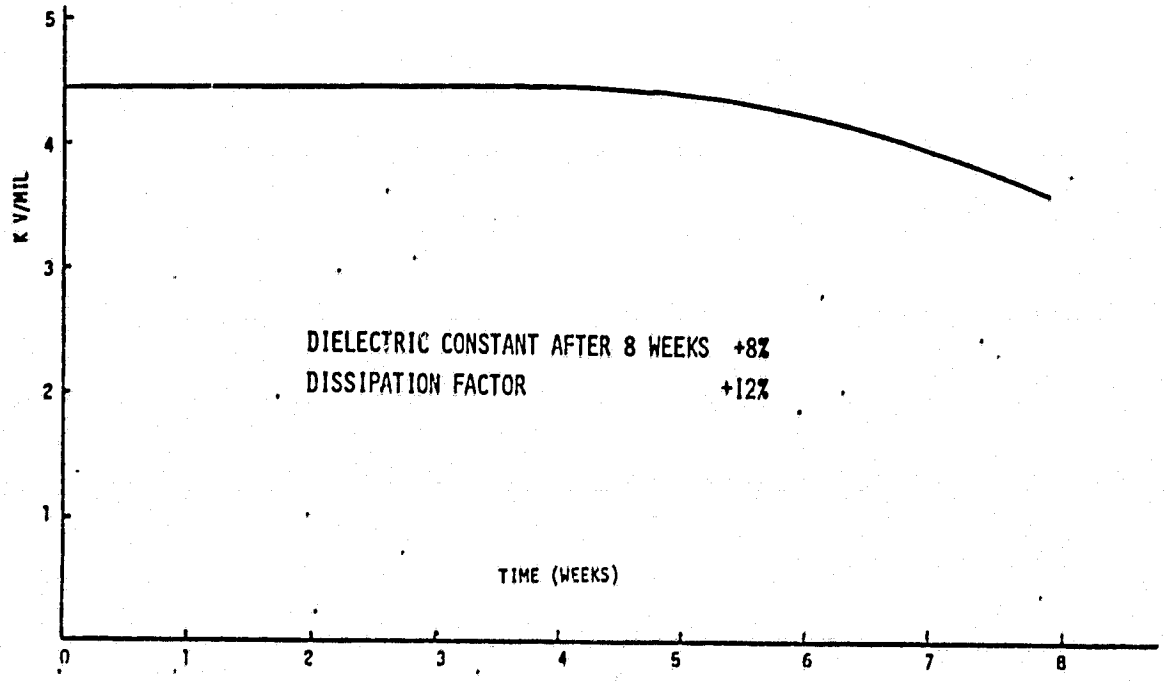



Figure 38. Effect of thermal aging on dielectric strength of polyimide films, 1 mil thick at 300°C.

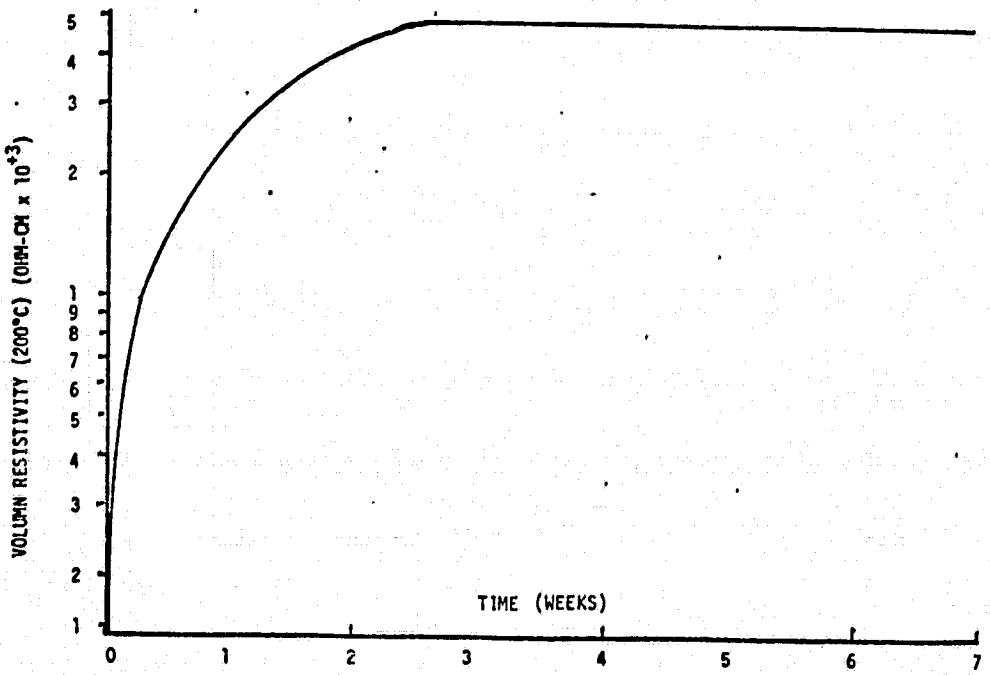



Figure 39. Effect of thermal aging on volumn resistivity, 1 mil film at 300°C.

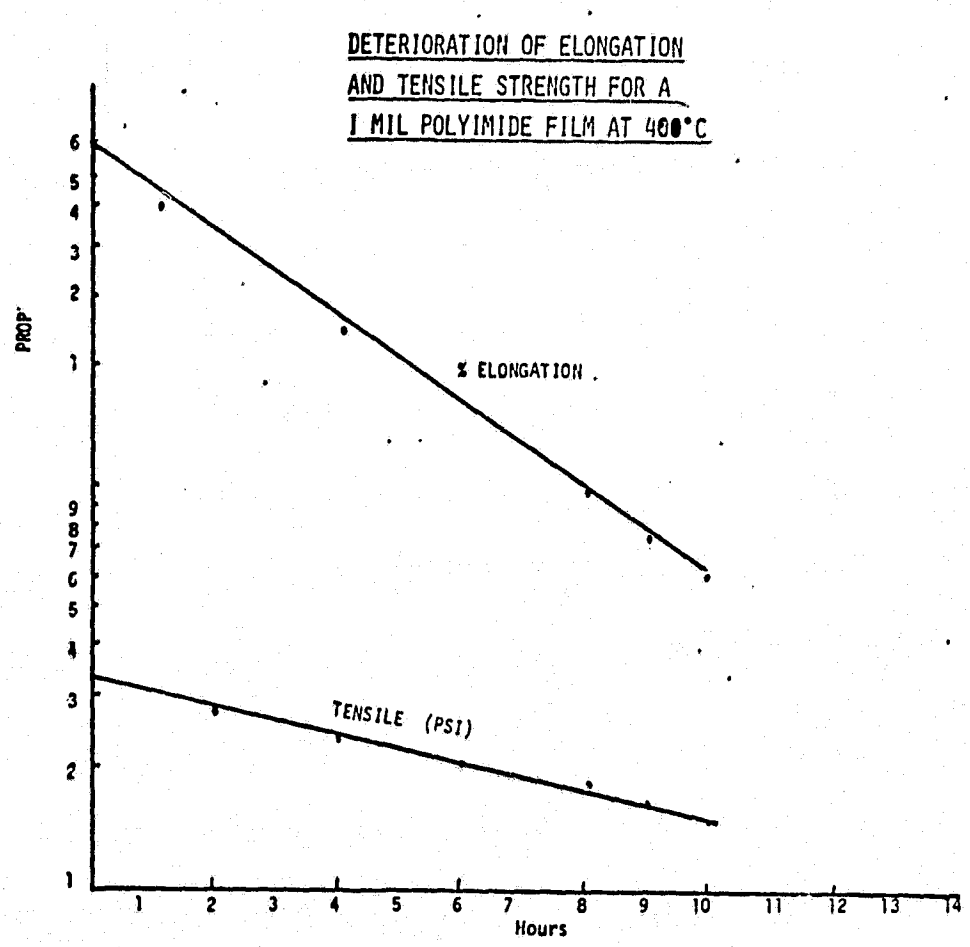



Figure 40. Deterioration of elongation and tensile strength for a 1 mil polyimide film at 400°C.

As indicated earlier, special care must be taken of the starting polyamic acid material such that water is not absorbed, even though these prepolymers are known to reduce their viscosity by absorbing small amounts of water (51). Only a very small amount of water absorbed in the starting material will greatly decrease the thermal properties of polyimides (9). A mass spectrometer can be used to determine water content in a cured polyimide film. As seen in Figure 41, water molecules contained in a typical polyimide is about $0.6 \times 10^{21}$ $H_2O$ molecules/$cm^3$ (Figure 41 as measured at 500°C), while that in CVD silicon dioxide is about $2.5 \times 20^{21}$ molecules/$cm^3$ (53).

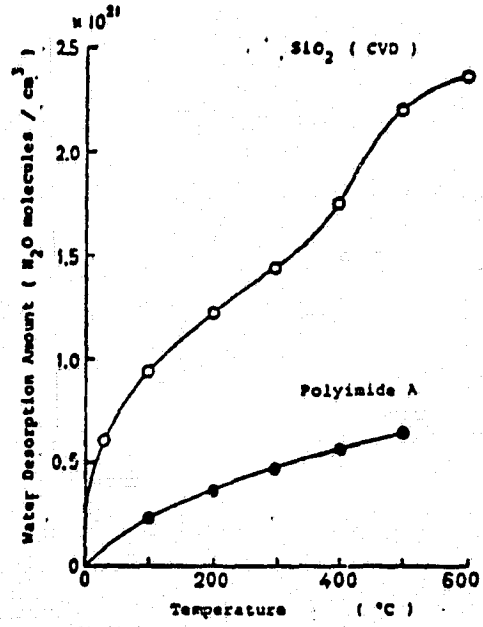



Figure 41. Water desorption amount versus temperature by mass spectrometer. Water molecules contained in polyimide is less in number than those in the silicon dioxide (CVD).

3. Stress Test

The stress test conditions on polyimide (primarily for use as a passivation layer) compared to conventional $SiO_2$ passivation are presented in Table XIV. As seen, polyimide coatings are superior in scratch test, punch-through test, HCl/salt water stress and disruption at bump area as compared to conventional $SiO_2$ passivation (53).

| STRESS | TECHNOLOGY | |
|---|---|---|
| | POLYIMIDE | $Si_xN_y$ |
| Bond Pull | No Difference compared to standard | No Difference compared to standard |
| Scratch Test | Approximately 2x improvement compared to $SiO_2$ only | - |
| Punch Through Test | 5x improvement compared to $SiO_2$ only | 1.5 improvement ($Si_xN_y$ vs $SiO_2$)<br>2.5 improvement ($Si_xN_y/SiO_2$ vs $SiO_2$) |
| HCL/Salt Water Stress | Significant improvement compared to $SiO_2$ only | -- |
| SEM Analysis of Bump Area | No disruption of polyimide due to tab bonding | No cracking of $Si_xN_y$ under bump due to tab bonding. |

TABLE XIV. Stress Test Conditions For Polyimide and Silicon Nitride as Compared to Conventional Silicon Dioxide as a Passivation Layer.

J. TOXICITY AND HEALTH HAZARDS

Polyimides are chemically inactive when completely cured, and consequently, are not harmful to the person handling them. However, an extremely sensitive person may contract dermatitis from the dust of cured polyimide fragments. Also, solvents such as dimethylacetamide, N-methyl-2-pyrrolidone, etc., contained in the polyimide varnish may cause dermatitis, if the varnish comes in contact with the skin, or liver or kidney trouble if the vapor from the polyimide varnish is inhaled. To avoid this, full care must be taken not to touch the varnish or inhaled the vapor while handling. The following precautions should be taken:

- To avoid direct contact with polyimide varnish during application, workers should wear work clothes which can be fastened securely at the neck and cuffs as well as rubber gloves.
- During work in which polyimide varnish may splash, protective glasses and a mask should be worn in order to protect the eyes and face.
- Should polyimide varnish come in contact with the skin, it should be washed off immediately with warm water and neutral soap. A solvent should not be used as it may cause skin irritation.
- Should the polyimide varnish enter the eyes, immediately wash it out with running water, and consult a doctor.
- Polyimide varnish should be applied in a proper work area enclosed with partitions and well ventilated.
- The heating oven for curing the polyimide varnish should be provided with a duct to remove the gas generated during curing so that it does not enter the working room.

- Be careful not to spill the polyimide varnish. If it is spilled accidentally, wipe it up immediately.

- The flash point of polyimide varnish is 80°C approximately. Be very careful of fire when using it.

- Data supplied by the General Aniline and Film Corporation indicate that animals exposed to air saturated with N-methyl-2-pyrrolidone for six hours daily for ten days tolerated the conditions of the experiment and gained weight normally. Other animals subjected to 20 day dermal toxicity studies had no specific degenerative changes and did not have a remarkable degree of skin irritation.

- Adhesion promoters can cause eye damage and skin burns. In case of skin contact flush with water and then wash thoroughly in soap and water. In case of eye contact, immediately flush eyes with water for 15 minutes. Consult a physician.

- Since polyimide varnishes are hygroscopic, the container should be well sealed right after use.

## III. DOUBLE LEVEL METAL INTERCONNECT PROCESS DEVELOPMENT USING POLYIMIDES

### A. Experimental Setup

Polyimide process developments for double level interconnect was investigated using Dupont polyimides PI-2540, 2545, 2550 and 2555, as well as Hitachi's PIQ polyimide. All experiments were conducted using two inch silicon n-type phosphorous doped wafers typically of <111> orientation and having a resistivity of 5-20 ohm-cm. A via test pattern as developed at NASA Marshall Space Flight Center was utilized in this process development. This test pattern consisted of a chain of 560 via's with via size ranging from 0.5 mils square to 0.2 mils square for a given chain. Metal interconnects between vias were typically 0.7 mils wide although a second mask was also available having interconnect widths of 0.4, 0.5, 0.6 and 0.7 mils corresponding to 0.2, 0.3, 0.4 and 0.5 mil square via chains, respectively.

A field oxide was thermally grown on the precleaned wafers in dry $0_2$ for 15 minutes, steam for 45 minutes and dry $0_2$ for an additional 15 minutes at 950°C resulting in an oxide thickness of $10\text{-}12^{K}$ Å. Prior to depositing the first layer metal, a cleaning step was performed, consisting of a one-minute dip in dilute HF (1:10 - $HF:H_2O$) at room temperature and a 10 minute rinse in deionized water. The first metal layer was d.c. sputter deposited using Al/Si/Cu alloy targets of 0.2 to 1.0 micron thick. This metal

was patterned using conventional photolithographic techniques and Waycoat-31 type 3 negative photoresist.

The polyimide after deposition was patterned using a positive (or negative) photoresist mask and a caustic basic developer solution as described in the last section. In order to gain adequate control of the process, it was necessary to monitor the thickness of the deposited polyimide layers as a function of deposition spin speed for different polyimide compositions (ratio of polyamic acid as received to thinning solution) and on surfaces of bare silicon and silicon dioxide. Also, since photoresist was used as the polymide masking material, and since the surface properties of smooth fully cured polyimide (or partially cured polyimide) was suspected to be different than a silicon or a silicon-dioxide surface, the thickness of deposited photoresist layers on polyimide surfaces was also determined empirically.

The thickness of post baked photoresist films as a function of spin speed for Shipley AZ1350J and AZ111, plus Waycoat Type 3 No43 IC resist is shown in Figure 42. Measurements of these film thicknesses were made using a laser based ellipsometer and an IBM film thickness analyzer (located at American Microsystems, Inc.). As expected, the final post baked thickness is linearly related to starting photoresist viscosity. All of the film thicknesses recorded in Figure 42 were for photoresist deposited on bare silicon wafers. These same films deposited on oxidized wafers exhibited essentially the same results as these.

As a comparison, the thickness of Shipley AZ1350J positive photoresist as deposited on cured Dupont PI-2550 polyimide (with the

THICKNESS OF POST BAKED PHOTORESIST
VS
SPIN SPEED

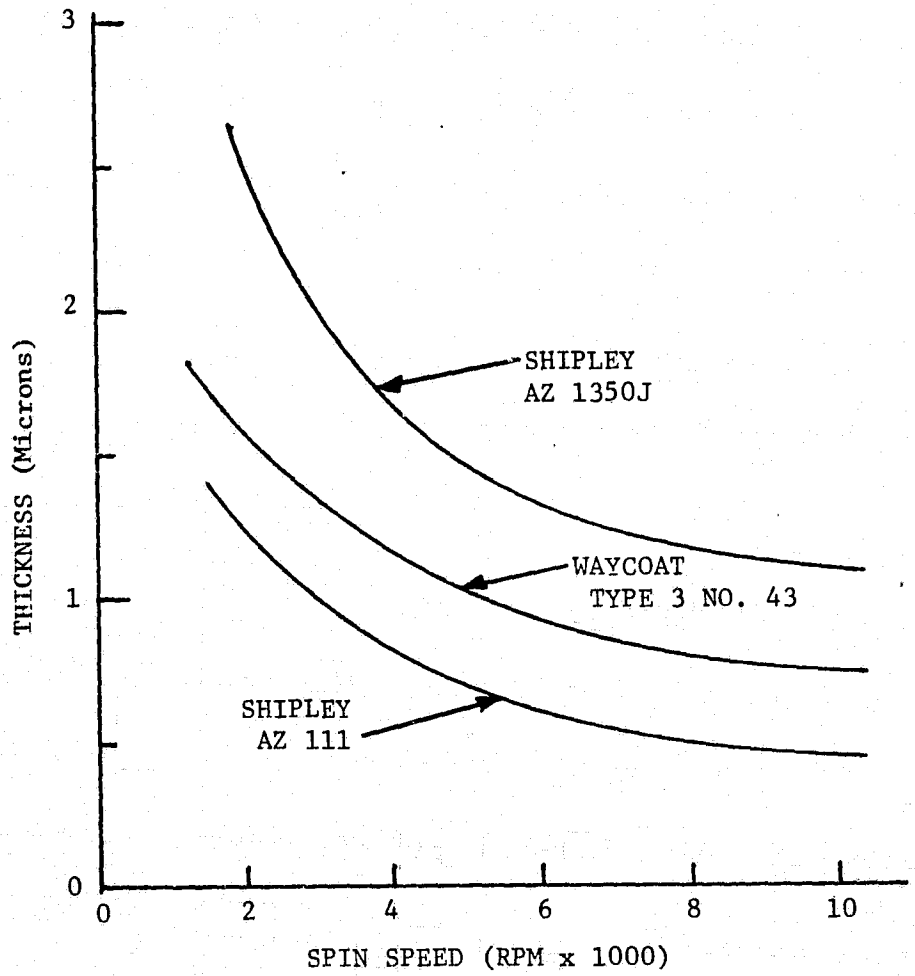



Figure 42. Post baked photoresist film thickness as a function of spin speed for Shipley AZ1350J and AZ111, plus Waycoat Type 3 No. 43 I.C. resist as deposited on bare silicon wafers. Measurements taken from ellipsometer data and an IBM film thickness analyzer.

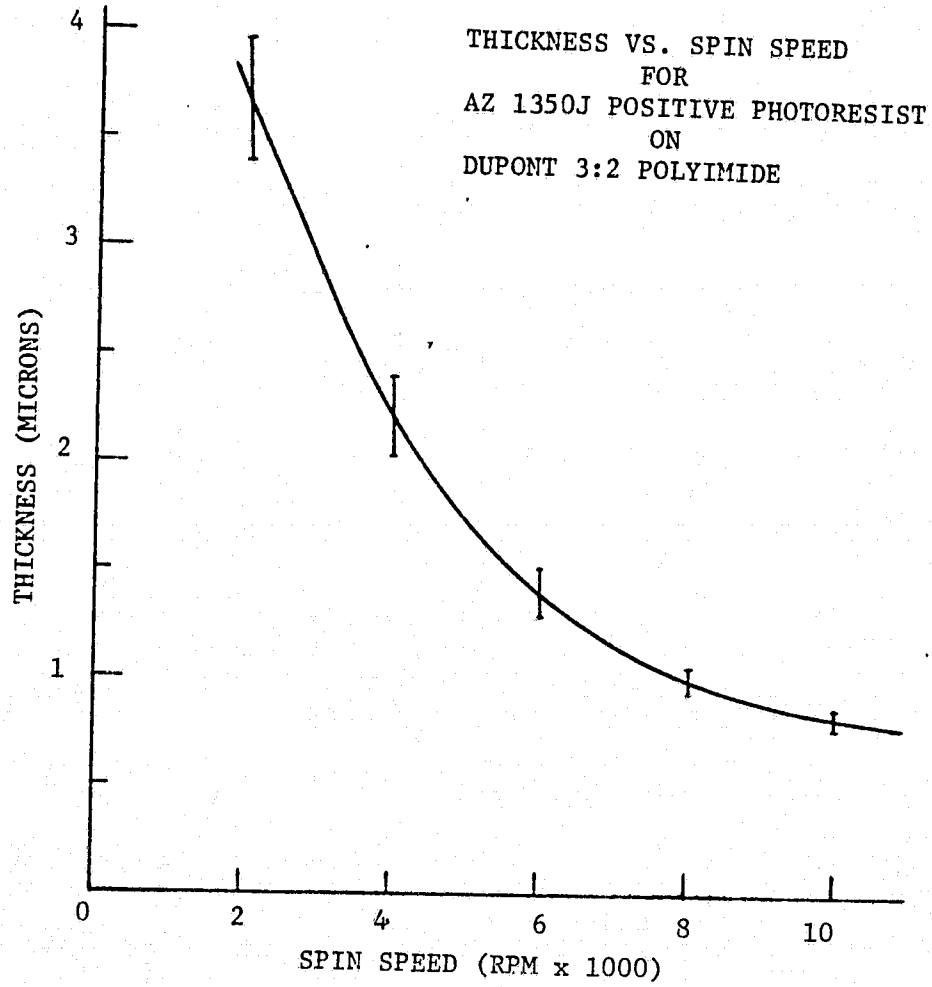



Figure 43. Thickness as a function of spin speed for Shipley AZ1350J positive photoresist deposited on cured Dupont polyimide mixed 3 parts PI-2550 to 2 parts T-8035. Measurements taken by SEM.

polyamic acid viscosity adjusted by mixing three parts PI-2550 to two parts Dupont thinner T-8035) is shown in Figure 43. Analysis of Figures 42 and 43 indicates that AZ1350J positive photoresist is slightly thicker when deposited on polyimide than on bare silicon at lower spin speeds (3.7 microns compared to 2.6 microns at 2000 rpm spin speed) where as at higher spin speeds deposition on polyimide is slightly thinner than on bare silicon (1.0 microns compared to 1.2 microns at 8000 rpm spin speed). Between 5000 and 7000 rpm, no noticable difference in thickness is discernible.

A typical scanning electron micrograph showing thicknesses of thermally grown $SiO_2$ (5300Å), Dupont PI-2550 polyimide (8000Å) and Shipley AZ1350J positive photoresist (19,000Å) is shown in Figure 44. Calibration of the scanning electron microscope was accomplished prior to these measurements.

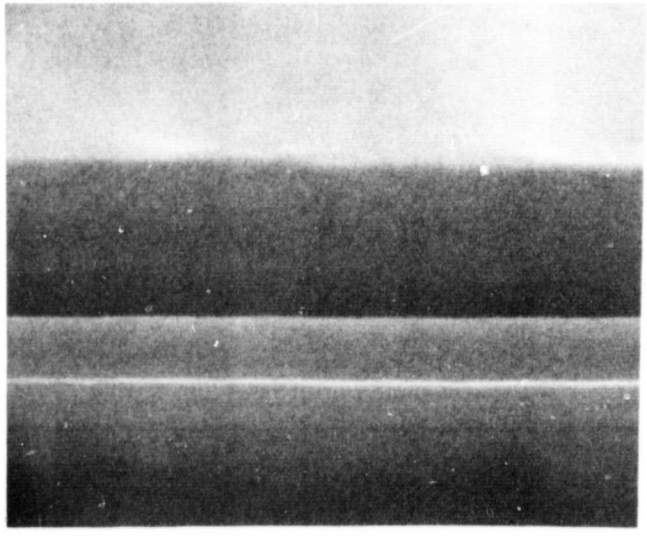


Figure 44. A typical SEM illustrating thicknesses of positive photoresist (top), polyimide (middle) and thermally grown $SiO_2$ on top of a <100> two inch silicon substrate. Magnification is 11,300X.

Thicknesses of deposited polyimides on both bare silicon and silicon dioxide as a function of spin speed for two different polyimide viscosities (3 parts PI-2550 polyimide to 2 parts T-8035 thinner and 1 part polyimide to 1 part thinner) are shown in Figures 45 through 48. The thickness of Waycoat negative photoresist as deposited on completely cured Dupont 1:1 polyimide is shown in Figure 49 as a function of spin speed. Also, thickness of completely cured Hitachi polyimide on both bare silicon and silicon dioxide are shown in Figures 50 and 51.

As was indicated in the last section on polyimides, during the curing or imidizing process, much weight is lost due to solvent and water products being driven from polyamic acid. This weight loss also results in a considerable verticle shrinkage of the polyimide film. This can be monitored by measuring the film thickness at various curing times and temperatures as shown in Figure 52. These measurements were obtained from a series of carefully prepared microslices used in SEM analysis. As implied from this figure, an approximately one micron thick layer of final cured film is more than four to five microns thick upon application of the polyamic acid. From this and other experimental results, it is seen that the majority of the film shrinkage is realized between the temperatures of 150 to 200°C.

B. Patterning - Positive Photoresist

In the first experimental endeavors with etching via's in polyimide, both Dupont PI2550 (thinned with Dupont thinner T-8035) and Hitachi PIQ (no thinner) were attempted. The Dupont polyimide was mixed three parts polyimide to two parts thinner and deposited

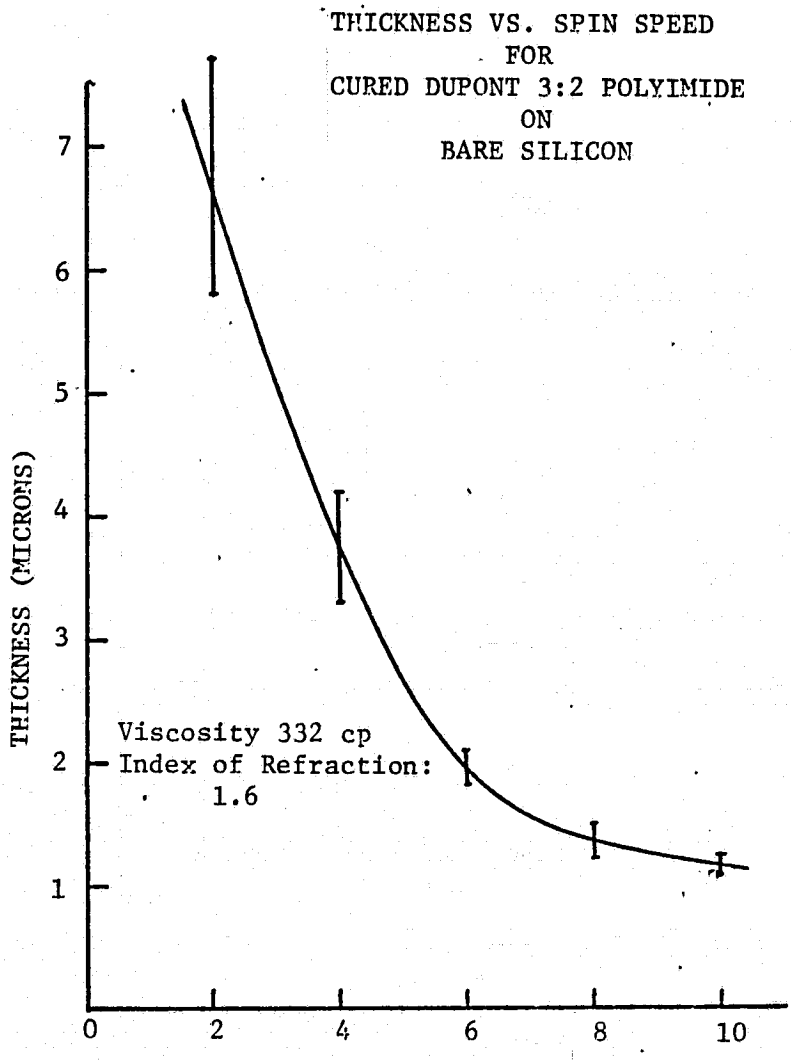



Figure 45. Thickness as a function of spin speed for Dupont polyimide mixed 3 parts PI-2550 to 2 parts T-8035 thinner on bare silicon. Measurements taken from SEM and ellipsometer.

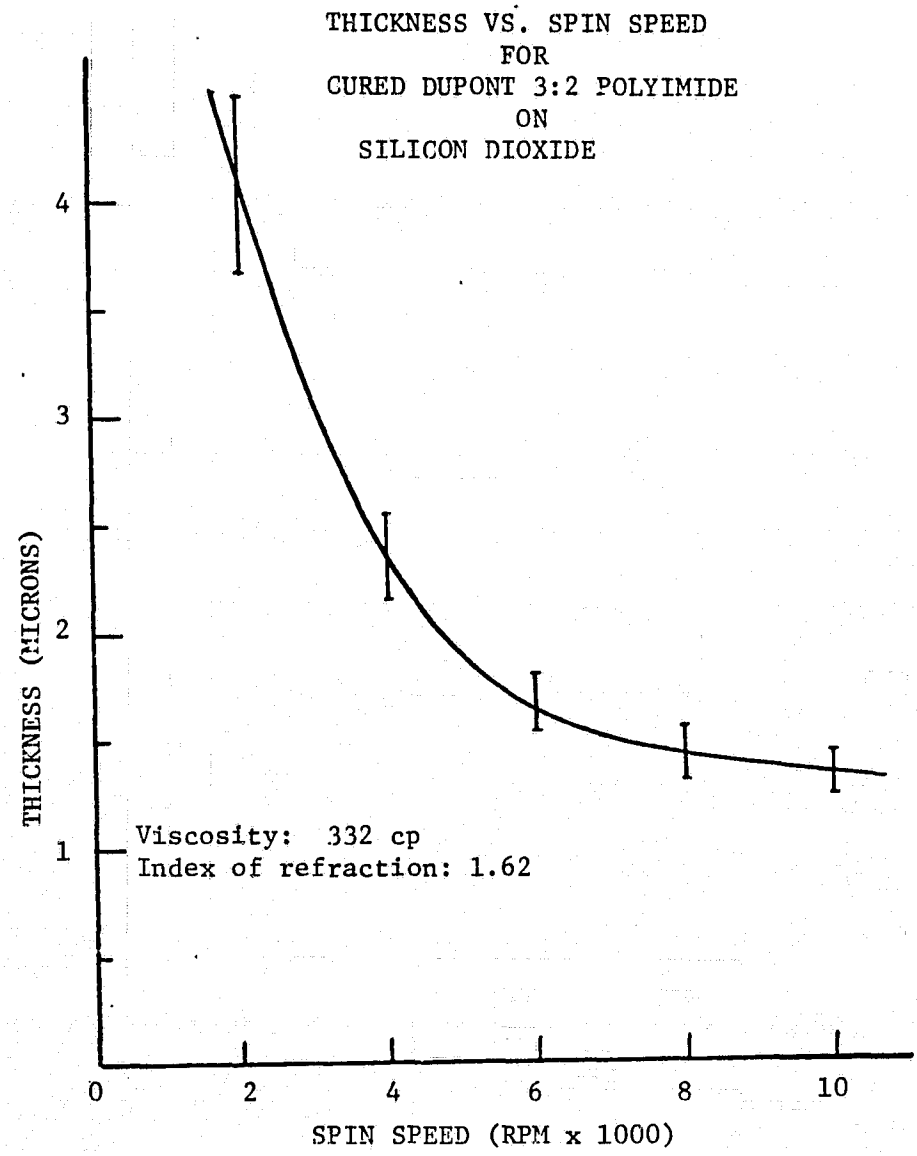



Figure 46. Thickness as a function of spin speed for Dupont polyimide mixed 3 parts PI2550 to 2 parts T-8035 thinner on silicon dioxide. Measurements taken from SEM and ellipsometer.

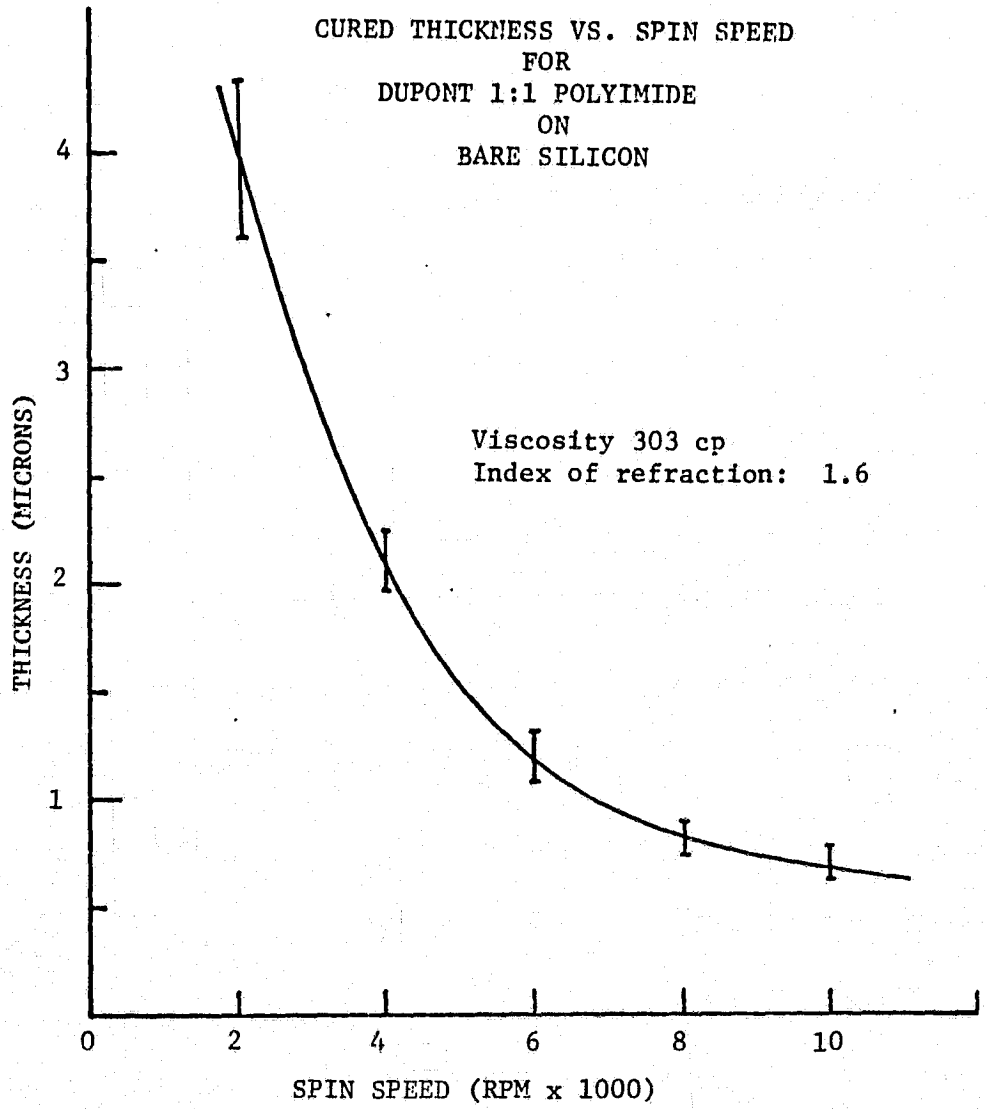



Figure 47. Thickness of cured Dupont polyimide as a function of spin speed deposited on bare silicon. 1:1 implies equal parts of PI-2550 polyimide and T-8035 thinner. Measurements taken from SEM analysis.

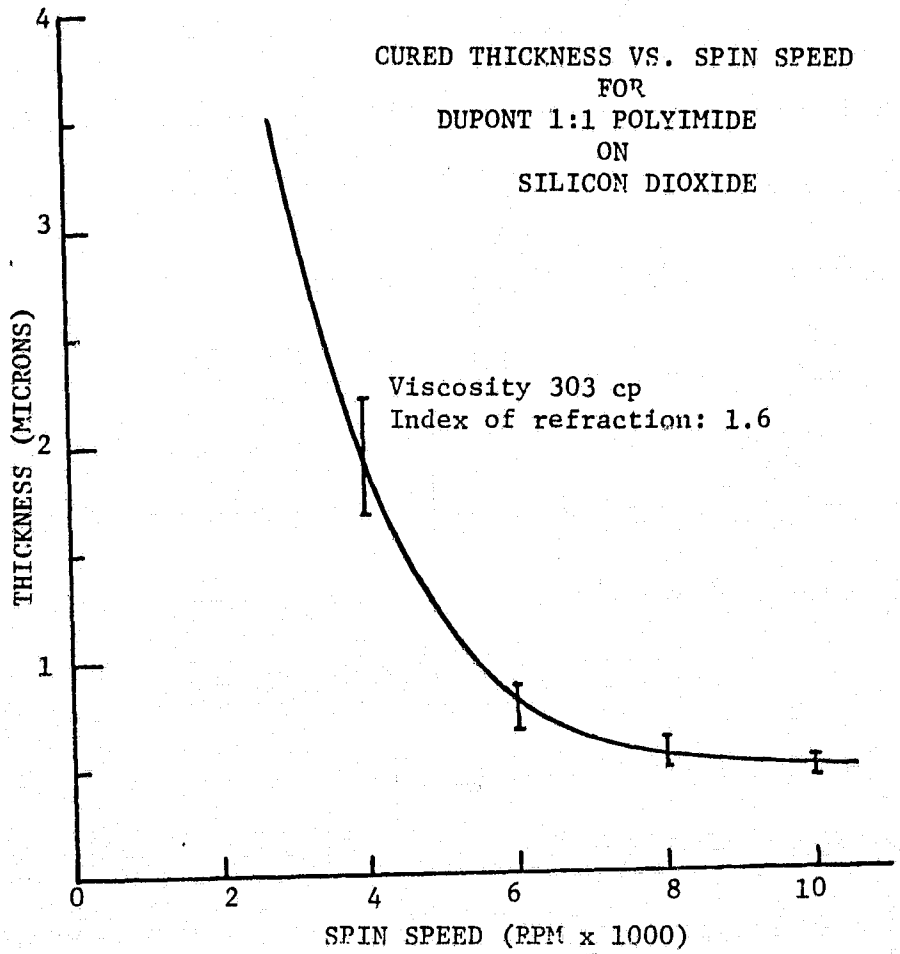



Figure 48. Thickness of cured Dupont polyimide as a function of spin speed deposited on silicon dioxide (thermal). 1:1 implies equal parts of PI-2550 polyimide and T-8035 thinner. Measurements taken from SEM analysis.

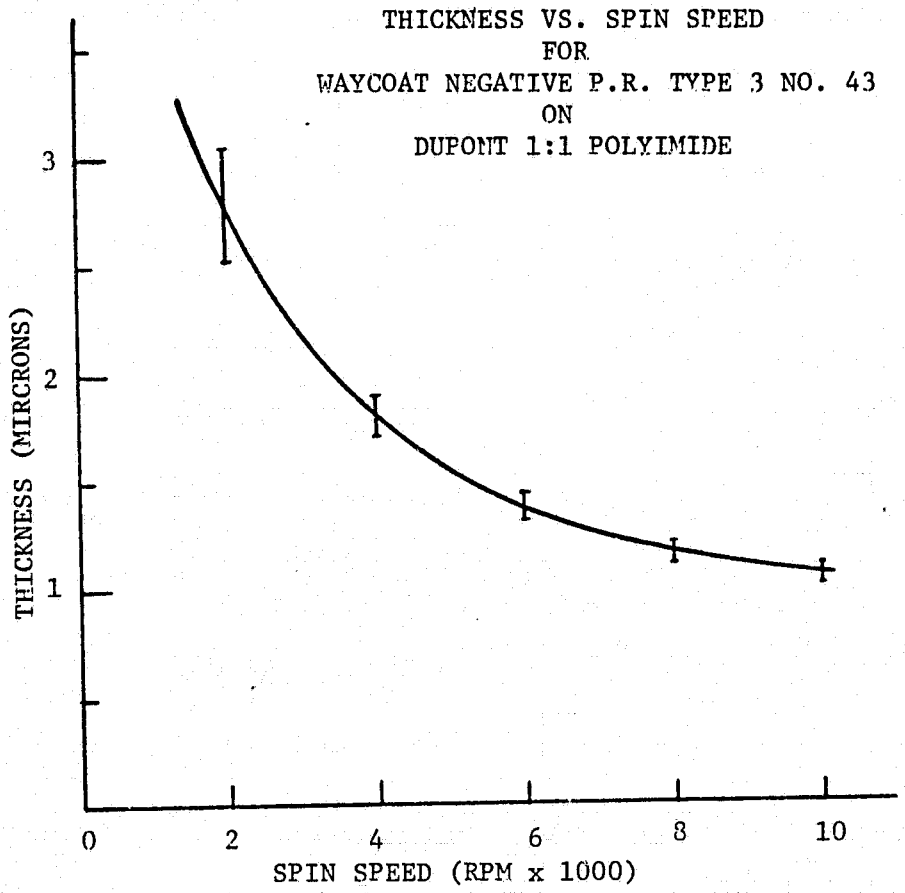



Figure 49. Thickness of Waycoat negative type 3 IC photoresist 43 as a function of spin speed on Dupont polyimide prepared by mixing equal parts PI-2550 polyimide to T-8035 thinner. Measurements taken from SEM and ellipsometer analysis.

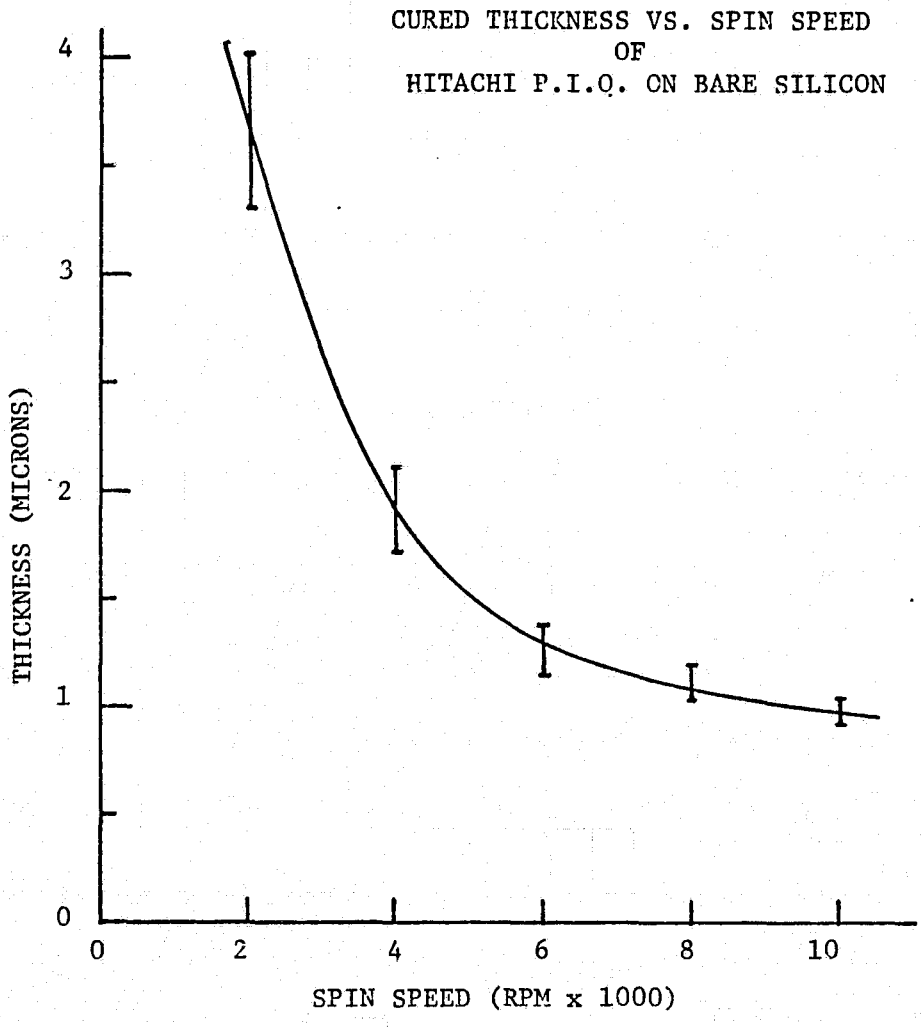



Figure 50. Thickness vs. Spin Speed for Hitachi PIQ on bare silicon. Liquid PIQ viscosity was 1125 cps and cured PIQ index of refraction was 1.58. Thickness data taken from ellipsometer and SEM measurements.

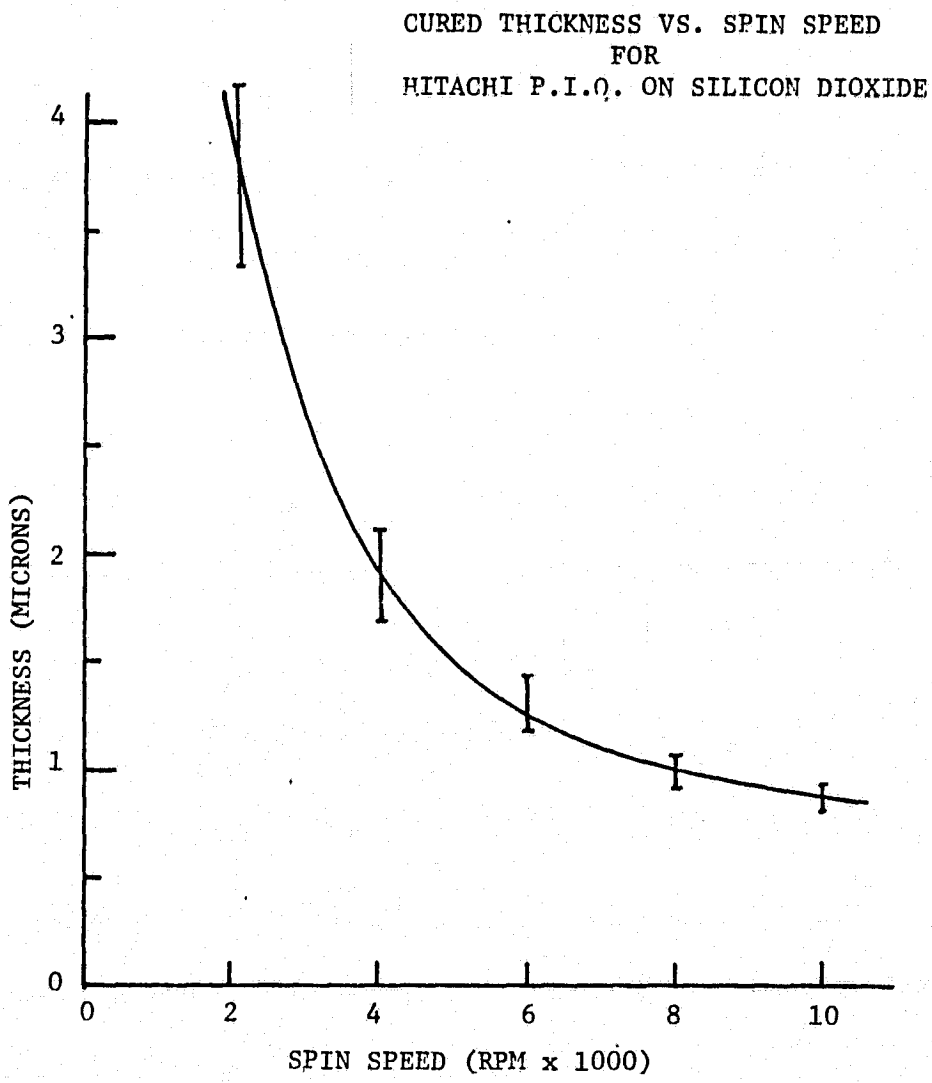



Figure 51. Thickness vs. Spin Speed for Hitachi polyimide on silicon dioxide. Liquid PIQ viscosity was 1125 centipoise and cured PIQ index of refraction was 1.58. Thickness data taken from ellipsometer and SEM measurements.

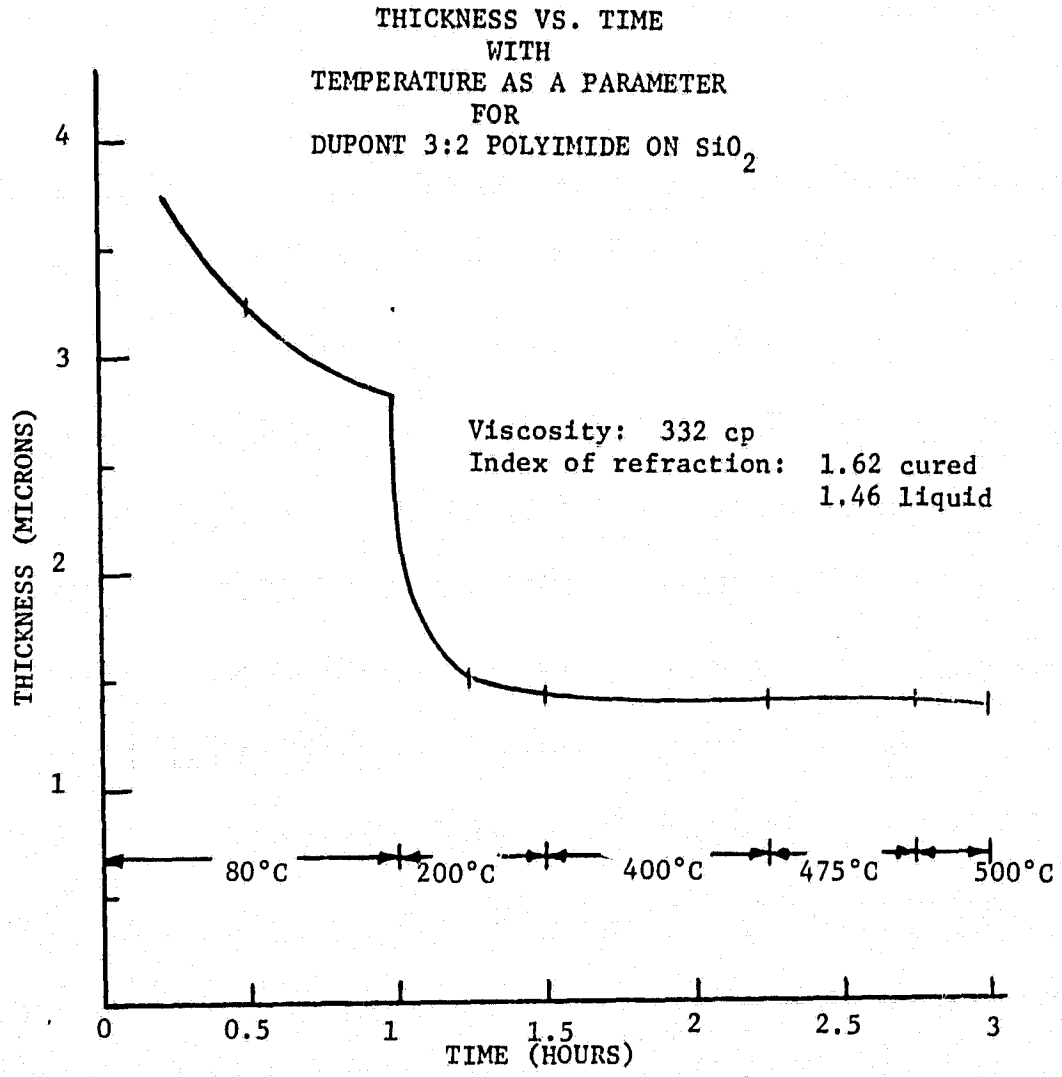



Figure 52. Thickness and temperature dependence as a function of time for Dupont 3:2 polyimide (3 parts PI 2550 to 2 parts T-8035 thinner) deposited on silicon dioxide (thermally grown) at 8000 rpm. Measurements taken from SEM.

statically, then spun at a final spin of 8000 rpm. The pre-imidization curing cycle consisted of a 15 minute prebake at 50°C, followed by a 15 minute bake at 80°C. Shipley AZ1350J positive photoresist was deposited, prebaked 80°C for 30 minutes and exposed using the via test pattern mask. Shipley developer AZ312 was used to develop the positive resist and etch the pre-cured polyimide at the same time. This developer proved to be much too strong for this precure cycle since it caused excessive etching of the polyimide layer thus undercutting the photoresist layer and rendering poor via definition as can be seen in Figure 53. Here, 0.5 mil square via's as replicated in the photoresist layer ended up as large etched circular patterns in the polyimide layer. The Al metal bars shown here are 0.7 mils wide and constitute the first metal layer for this test pattern.

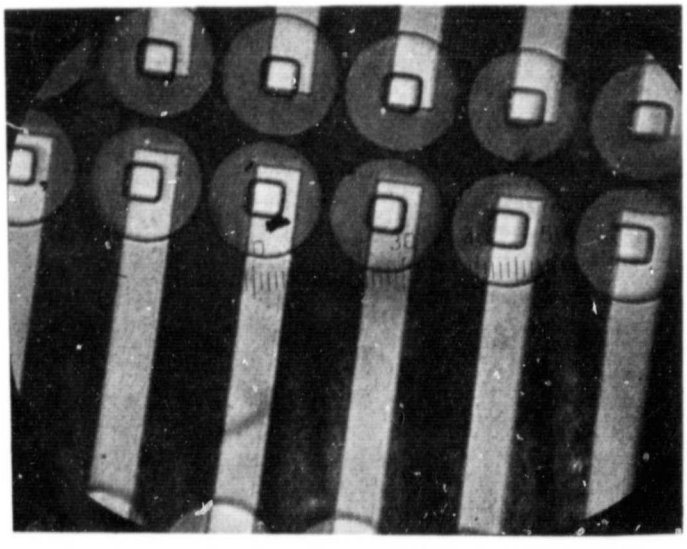


Figure 53. A composit layer of AZ1350J positive photoresist over Dupont polyimide PI2550 mixed 3:2 ratio with thinner T-8035. After prebake cycle, development of photoresist and etching of polyimide in AZ312 developer resulted in over etch of polyimide layer.

Hitachi polyimide, having undergone the same preparation as described above, yielded considerably better results as shown in Figure 54.

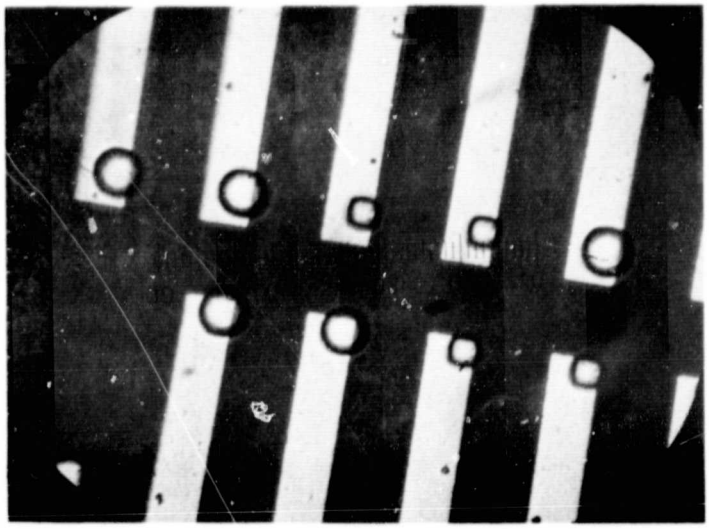


Figure 54. A composit layer of AZ1350J and Hitachi PIQ polyimide after developing (of PR) and etching (of polyimide) process for 0.4 mil square via's. Notice irregular size and shape of via's.

However a large degree of irregularity in via size and shape was observed across the wafer surface.

Several preliminary experiments were conducted using different positive photoresist and developer solutions in defining via's in the polyimide for the double layer test mask structure. The use of AZ1350J for the photoresist and a slightly weaker developer AZ351 tended to consistantly give better results in via formation. The use of AZ311 positive photoresist and companion developer AZ303 was attempted but did not tend to render as good a results as did the AZ1350J and AZ351 combination.

The Hitachi polyimide tended to imidize considerably faster than the Dupont PI2550 did at the same pre-cure temperature and time. Thus, either a stronger developer (ie as AZ311 or AZ312) or a shorter pre-cure cycle had to be instigated to effectively etch this polyimide in the 30 to 90 second time frame (the positive photoresist would allow exposure to the developer solution up to approximately 3-4 minutes before deformation occured).

In removing the photoresist from the polyimide layer using acetone, it was found that letting the photoresist-polyimide composit sit over night allowed a much easier photoresist removal. It is felt that the sitting process allowed the photoresist (and polyimide) to absorb moisture thereby decreasing the adhesion between these two layers. Later it was found that by using AZ Thinner instead of acetone to remove the resist, this photoresist stripping could be accomplished immediately following via formation and quite easily.

Even when the weaker developer AZ351 was used, having been thinned even more with dionized water, the etch process rendered poor via definition, especially for small (0.2 mil square) via's as seen in Figure 55. This 'rounding' of the small via's and the formation of a raised 'ring' around the via will be discussed later.

A cross sectional microslice illustrating the profile of the polyimide undercut is shown in Figure 56 for Dupont 3:2 polyimide PI-2550 deposited at 8000 rpm and still having the AZ1350J photoresist on top. Notice that the fastest undercut etching occurs in the middle of the polyimide layer as opposed to the polyimide-photoresist or polyimide-silicon dioxide interface. An enlargement

of the left hand side of this via is shown in Figure 57. The films layers are indicated as photoresist (PR), polyimide (PI) and silicon dioxide ($SiO_2$) having a scale as shown.

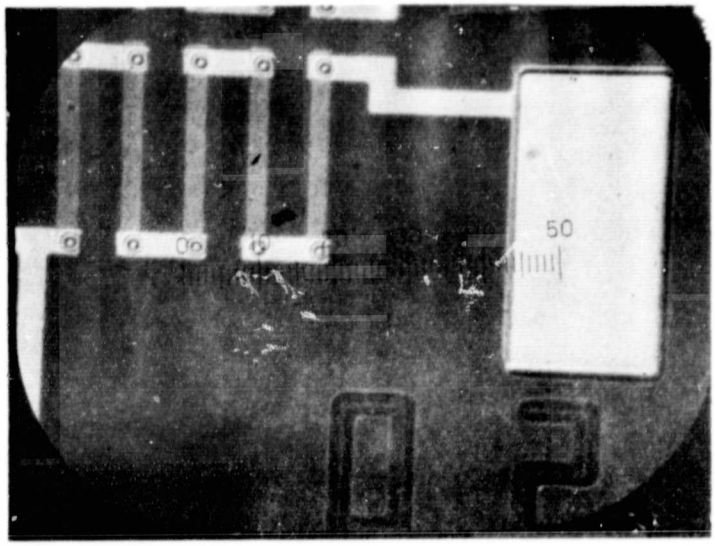



Figure 55. Dupont 3:2 polyimide deposited at 8000 rpm and patterned using AZ1350J photoresist and AZ351 developer (two parts developer to one part DI water). Notice via rounding and poor definition for these 5 micron via's.

C. Polyimide Residue

An additional difficult problem encountered in via formation had to do with removing all of the polyimide from the bottom of the via such that ohmic contact could be realized between the two metal levels upon depositing the second level metal. An extreme case observed of both rendering an undercut and not cleaning all of the polyimide out of the via is illustrated in Figure 58.

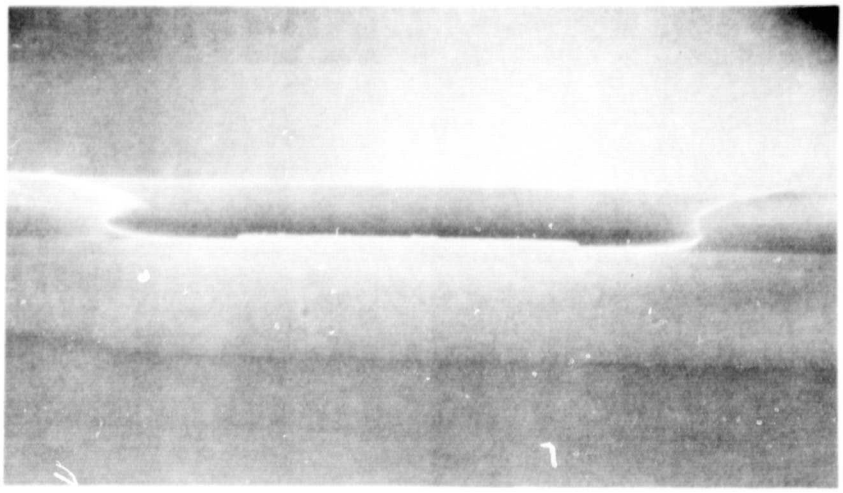


Figure 56. Cross section of a SEM microslice illustrating the undercut profile of polyimide under AZ1350J photoresist. Magnification is 3450X.

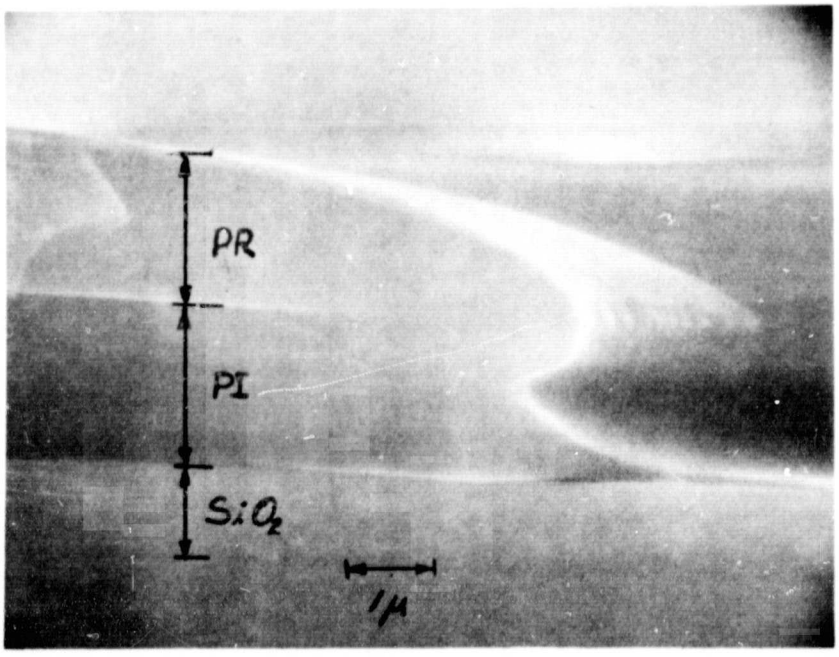



Figure 57. Magnification of the left hand side of the via shown in Figure 56. Magnification is 11,860X.

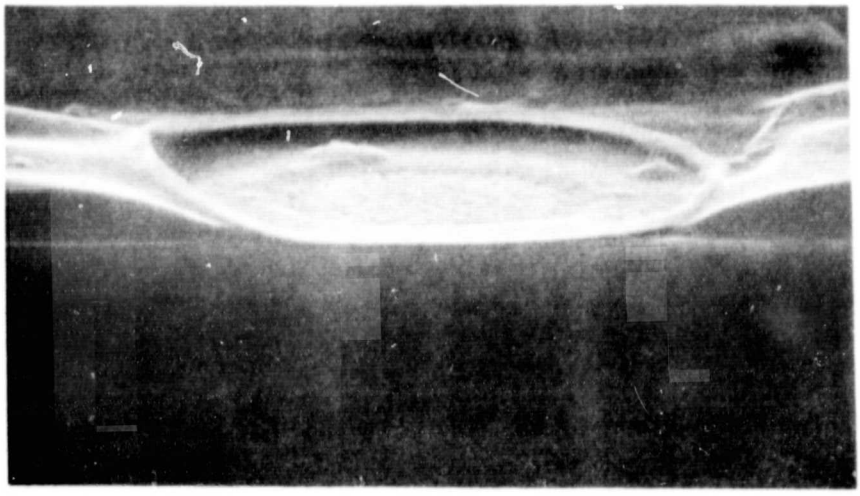


Figure 58. Micrograph showing both undercut and the presence of a thick polyimide residue in the bottom of the via.

In order to remove this thick polyimide residue from the via, two separate solutions were utilized. The first solution was hydrazine in an ultrasonic bath at room temperature for 10-60 seconds. The second consisted of a 5% aqueous solution of sulfamic acid at approximately 60°C for 10 minutes in an ultrasonic bath. Of these two, hydrazine rendered the best results.

D. Patterning - Negative Photoresist

The patterning of via's using a negative photoresist was also attempted. Using the Waycoat Type 3 negative resist, the polyimide was pre-cured at a slightly higher temperature (ie, 125°C for 15 minutes) prior to spinning on the resist (this higher temperature effectively hardened the polyimide coating such that the negative resist stripper would have less detrimental affect on it). A positive resist developer was used to etch the polyimide (ie, dilute AZ311 or AZ351) and the negative resist was removed using Hunt Microstrip stripper.

Via formation for both 0.4 and 0.2 mil square via's are shown in Figure 59a and b for one micron thick polyimide. (Similar results were obtained in PI2545, PI2555 and PIQ).

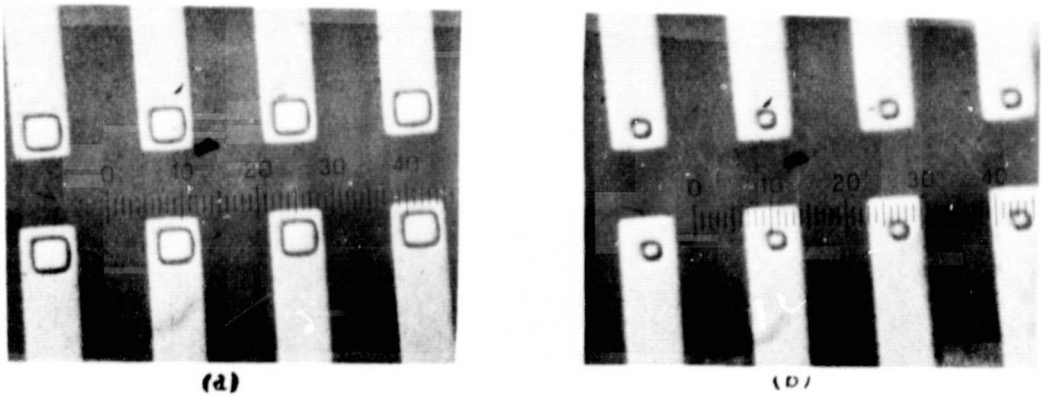



Figure 59. Via formation in one micron thick polyimide using negative photoresist as mask and positive developer as etchant. Hunt Microstrip removed the resist.

The Microstrip did not cause any unusual damage to the polyimide upon removing the negative photoresist.

Even though good via formation could be realized using negative resist, with some consistent process development, just as good a results were realized with positive photoresist and required fewer process steps and precautions.

E. Typical Process

A typical positive photoresist process utilizing Dupont PI-2550 polyimide, as an example, might include the following:

1. Preclean wafers with RCA clean
2. Grow 5000-6000 Å thermal oxide usual dry $O_2$/HCl-$H_2O$ steam/dry $O_2$ process at 1100°C
3. Deposit first level metal and pattern
4. Mix Dupont polyimide (3 parts PI-2550 to 2 parts T-8035 thinner, viscosity 332 cp)
5. Spin on wafer at 5000-8000 rpm for 20 seconds
6. Prebake at 50°C for 15 minutes, then 80°C for 30 minutes in nitrogen ambient
7. Apply positive photoresist for patterning polyimide, using Shipley AZ1350J applied at 7000 rpm for 20 seconds
8. Prebake photoresist 20 minutes at 80°C
9. Expose composite for 10-12 seconds at approx. 24 $mJ/cm^2$ light intensity (mercury vapor).
10. Develop in 3:1 DI water: AZ 351 developer and rinse (polyimide develops at the same time as the photoresist)
11. Rinse in acetone or AZ Thinner to remove photoresist
12. Cure polyimide 30 minutes at 240°C, then 30 minutes at 400°C
13. Via preclean for polyimide residue and first metal aluminum oxide prior to second level metal deposition

14. Deposit second level metal and pattern
15. Anneal aluminum at 425°C for 15 minutes in nitrogen ambient
16. Test

Using this process, via's having sloped sidewalls for good step coverage may be realized as shown in Figure 60. Here, a 5 micron via in a 1.2 micron thick polyimide shows good side slope contour

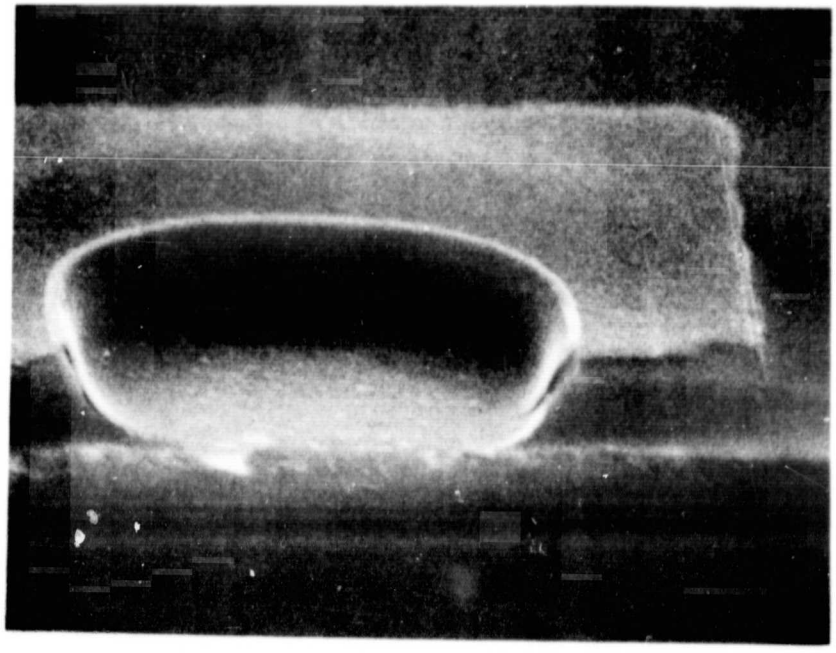


Figure 60. Via formation in 1.2 micron thick polyimide showing good side slope contour. Width of the via is 5 microns.

Similar results have been obtained in much thicker polyimide layers. Figure 61 illustrates a 0.5 mil via formed in a polyimide layer which is 2.7 microns thick.

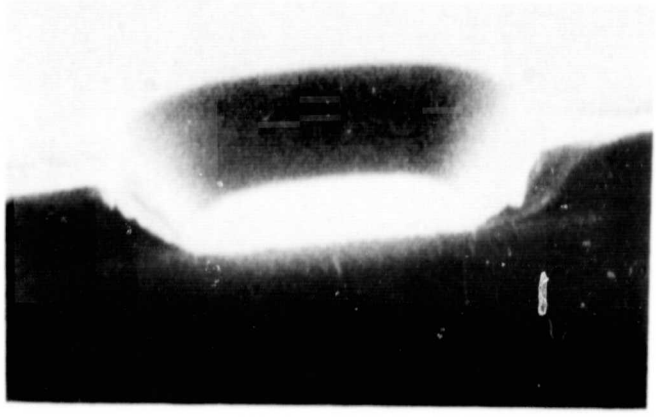


Figure 61. Via formed in 2.7 micron thick polyimide layer. Width of the via is 0.5 mils.

F. Step Coverage and Planarization

Examples of step coverage of either thermally evaporated or dc sputtered aluminum (or aluminum alloys) are shown in Figure 62 and 63. In both of these examples, the metal consist of Al/Si and is dc sputter deposited. The sample shown in Figure 62 is Duponts polyimide PI-2555 approximately 1.2 microns thick, where as the sample shown in Figure 63 is Hitachi polyimide PIQ approximately 1.5 microns thick.

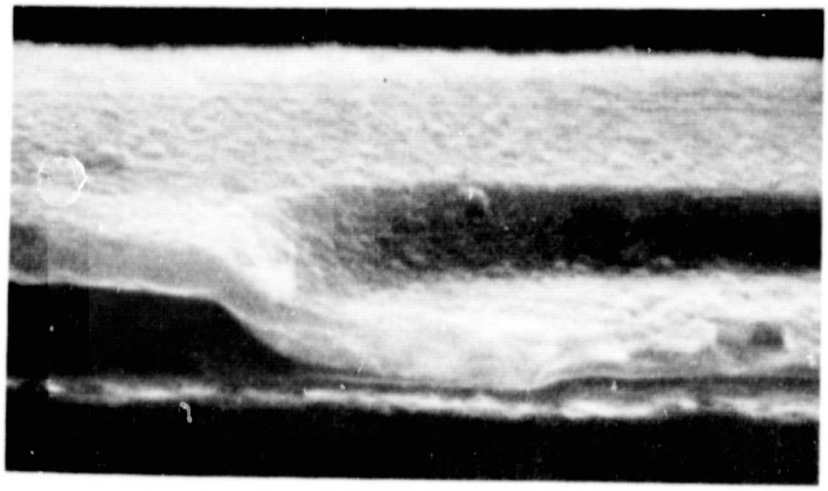


Figure 62. An example of metal step coverage obtainable in a via of 1.2 micron thick PI-2555 polyimide.

Also, to illustrate the planarizing capabilities of polyimide, the right hand side of Figure 63 is amplified and shown in Figure 64. Notice how the polyimide smooths out the step caused by the patterned first level metal.

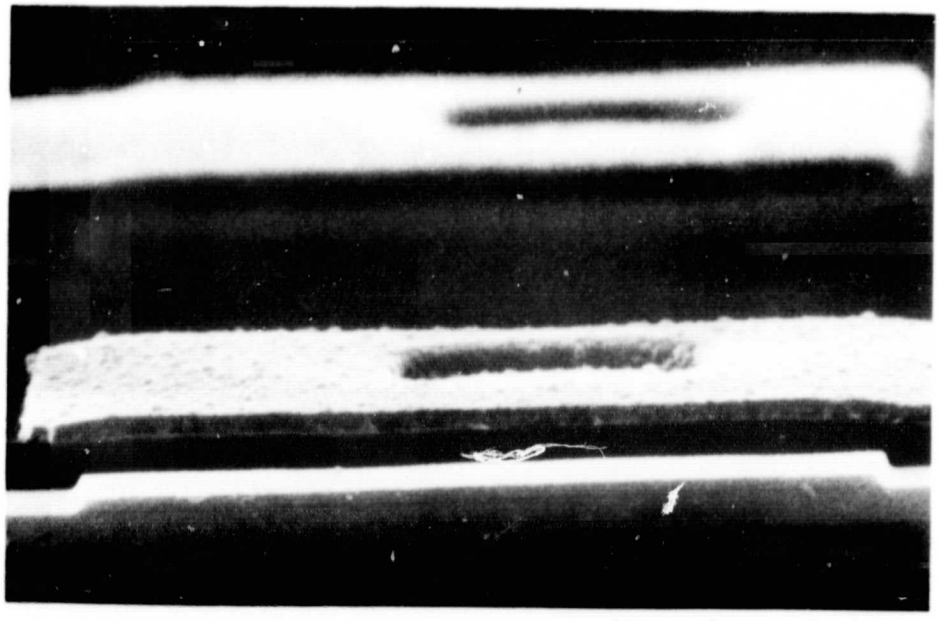


Figure 63. Second level metal formation and via step-coverage for 1.5 micron thick PIQ polyimide.

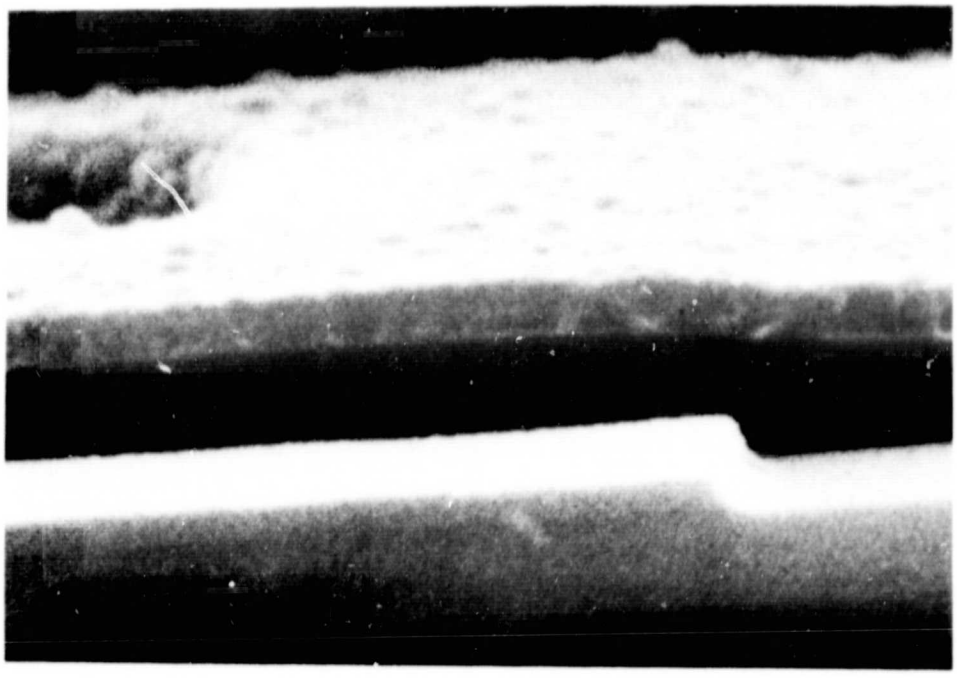


Figure 64. Amplification of the right hand side of Figure 63 illustrating the planarizing characteristic of polyimides.

G. High Temperature

Temperature processes on wafers having polyimide as a dielectric should not exceed 450°C in a nitrogen ambient, and preferably should not exceed 400°C. Exposing a wafer having a double level test pattern on it to temperatures in excess of 450°C results in a severe 'pull-back' or shrinkage at the patterned via's as shown in Figure 65.

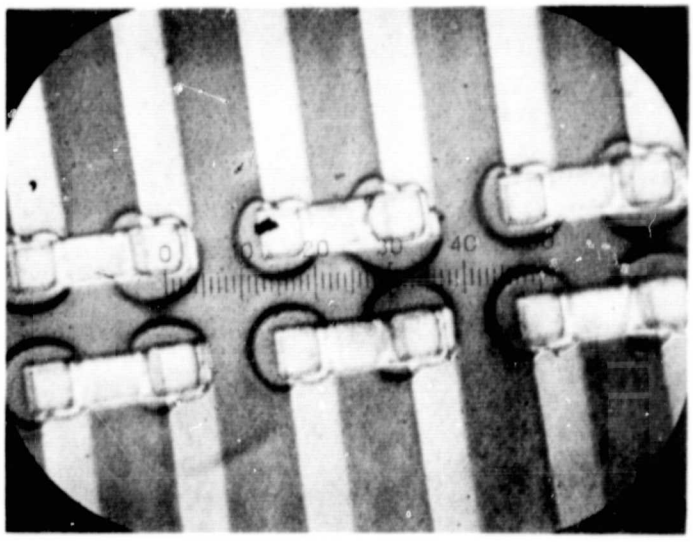


Figure 65. Example of polyimide pull-back at the via's when exposing the wafer to 490°C for 15 minutes.

For this sample, an attempt to sinter the Al at 490°C for 15 minutes was made. The polyimide type was PI-2550 mixed 3:2 with thinner. The gross pull-back tendency illustrated here occured only for the larger via's (ie, 0.5 mil), the smaller via's showed much less temperature affects. In fact,for the 0.2 mil vias on this same wafer, no pull-back could be detected by microscope inspection.

In some cases, the polyimide pull-back at high temperatures actually pulls the second level metal back with it, creating an open-circuit condition.

Even at 450°C for 30 minutes, a degree of pull-back can be observed under SEM analysis as shown in Figures 66 and 67. The sample shown in Figure 66 exhibits only a slight pull-back affect which could not be detected by microscope inspection, whereas at

certain locations on the sample in Figure 67 (where the polyimide has pulled from under the metal), this phenomena could be detected using a microscope .

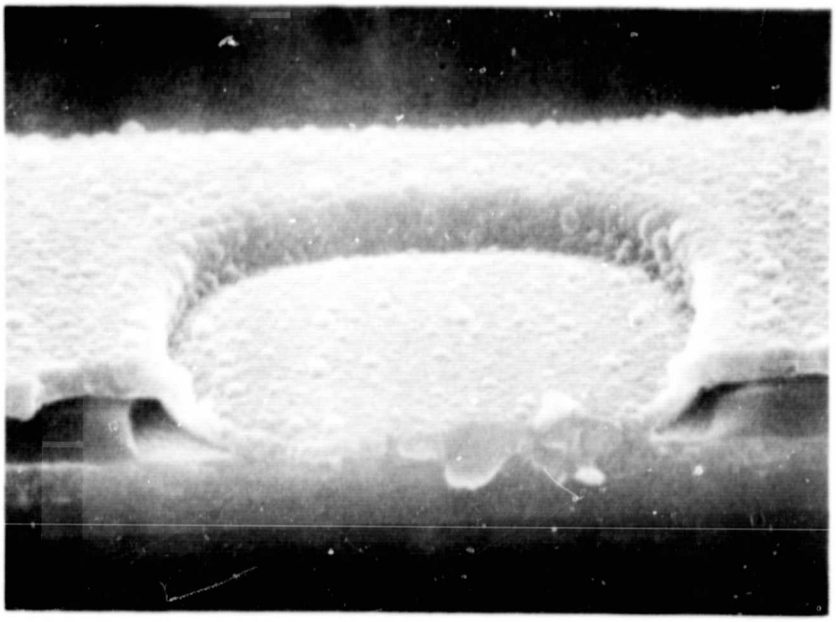


Figure 66. Sample which has been exposed to temperature cycle of 450°C for 30 minutes. Notice the pull-back under the metal at the via. Magnification is 10,000X.

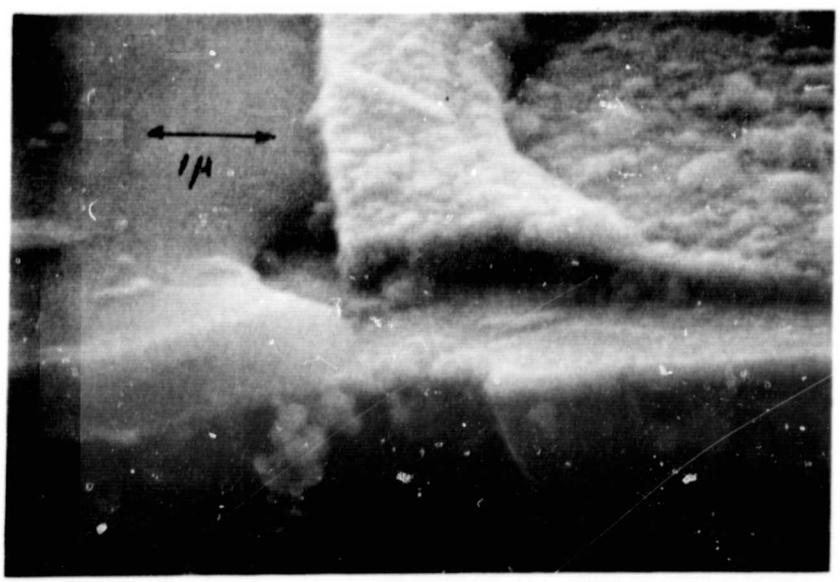



Figure 67. Sample exposed to 450°C for 30 minutes exhibiting polyimide pull-back from under the metal pattern. Magnification is 17,250X.

In some instances, the metal pattern tends to wrinkle for temperature processes greater than 470°C as shown by the sample in Figure 68. It might be noted that this particular sample was exposed to a hydrazine dip to clean out the via's prior to depositing the second metal layer. It is possible that the hydrazine altered the surface characteristics of the polyimide sufficiently to cause this stress related wrinkling effect.

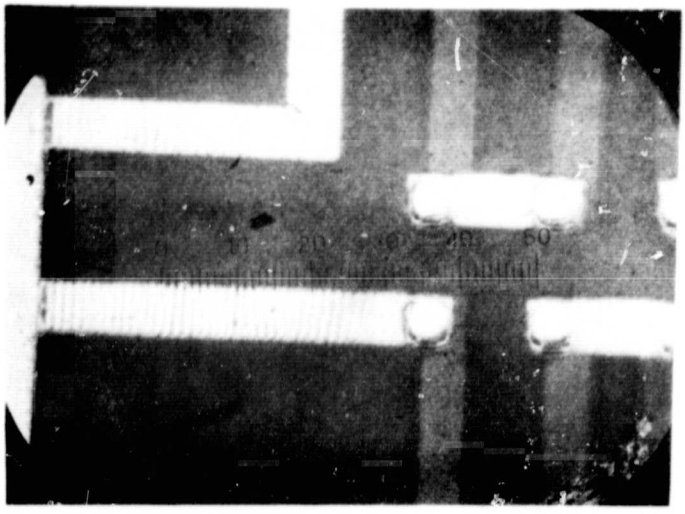


Figure 68. Interconnect wrinkling effect observed after the sample had been exposed to high temperature processing.

It should be noted that all samples shown in Figures 65 through 68 which exhibited high temperature detrimental effects did not have a coupling agent or an adhesion promoter applied to the wafer before depositing the polyimide. In an effort to minimize these problems, both Duponts coupler VM651 and Hitachi coupler were experimented with. The Hitachi couple is applied to the wafer as received and after a brief heat treatment, yields a thin $Al_2O_3$ layer over Si and $SiO_2$ surfaces - as indicated in the last section

of this report. The VM651 must be mixed with methanol (95%) and water (5%) in a very dilute solution (ie, 0.02% VM651). By using an adhesion promoter, the pull-back and other high temperature problems can be considerably improved. However, where possible, thermal cycling of polyimide materials should not exceed 400°C.

H. Raised 'Rings' Around Via's

Another interesting phenomena has been observed in the research which needs reporting. In adjusting the viscosity of Duponts PI-2550 polyimide, one part thinner T-8035 was mixed with one part PI-2550. This polyimide mix rendered excellent via formation, however, upon viewing SEM micrographs of via's formed in this material after the double layer aluminum sintering cycle at 400°C, a raised 'ring' around the via's were observed as shown in Figure 69.

To determine the cause of this raised 'ring', samples were prepared at various stages of polyimide cure. The three micrographs shown in Figure 70 illustrate the formation of this 'ring' as a function of temperature, SEM analysis indicated that the polyimide was still under the metal at these raised locations, but that the polyimide had appeared to swell.

To insure that this 'ring' behavior was characteristic of the polyimide only, polyimide layers were deposited on clean silicon wafers and patterned using positive photoresist AZ1350J and developer AZ351. Part of the wafers were then heat treated and the results observed via SEM analysis. Figure 71 illustrates the findings.

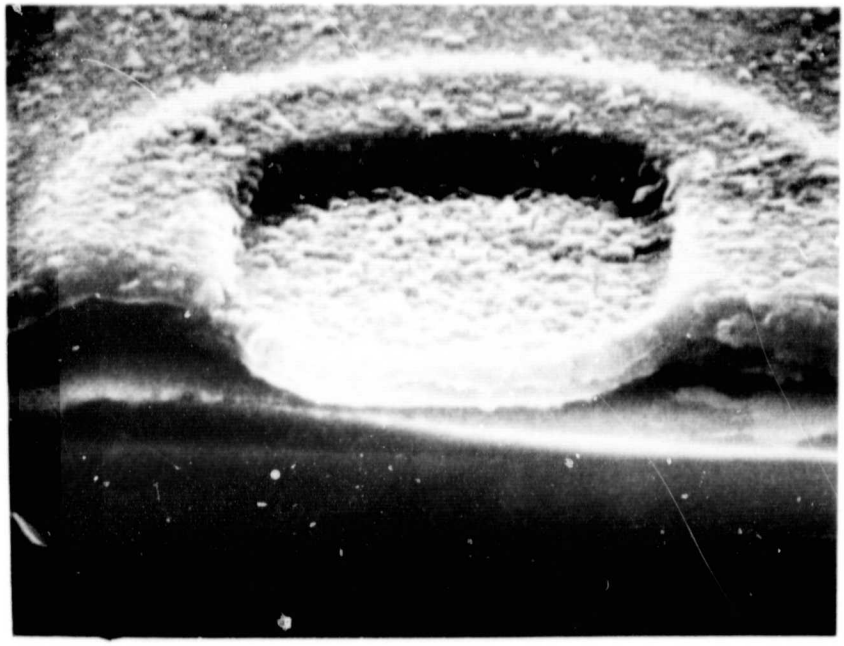
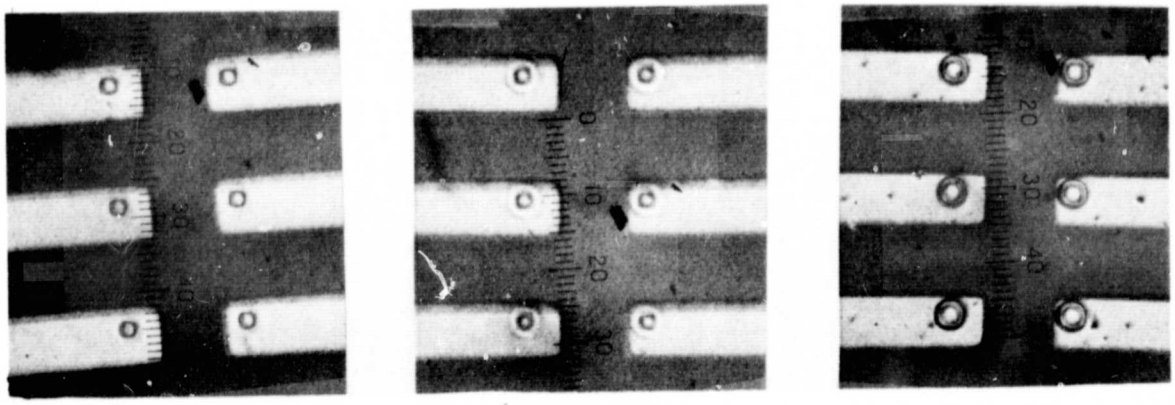
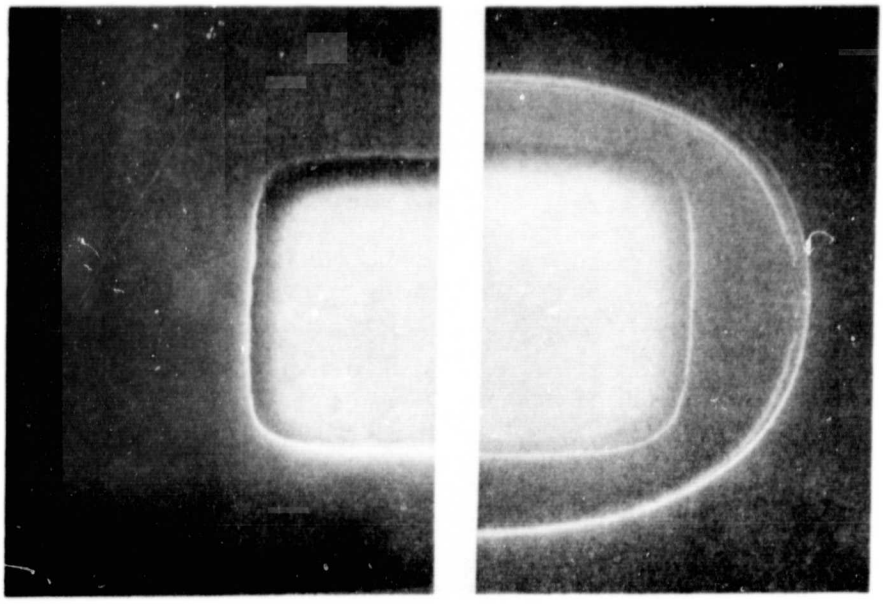


Figure 69. SEM micrograph of 1:1 PI-2550: T-8035 thinner after 400°C - 15 minute aluminum sinter. Notice the raised 'ring' around the via. Magnification is 11,300X.



(a) (b) (c)

Figure 70. Formation of raised 'ring' around via's of 1:1 PI-2550: T-8035 thinner as a function of temperature. (a) exposed to no temperature cycling, (b) exposed to 200°C for 30 minutes, and (c) exposed to 200°C for 30 minutes and 400°C for 15 minutes.



(a) (b)

Figure 71. SEM micrograph of 1:1 polyimide directly on silicon before any heat treatment (a), and after 30 minutes at 200°C and 15 minutes at 400°C (b).

A thoroughal knowledge of polymer chemistry would be required to explain this phenomena. It is speculated that with a high concentration of thinner solution (solvent) in the polyimide, the normal curing cycle for the polyimide is not sufficient to drive this excess solvent out of the polyimide. Its presents promotes some type of chemical reaction either with the strong basic developer solution used to etch the polyimide, or with water used to rinse away the developer solution, such that at elevated temperatures, swelling of that polyimide exposed to the developer solution or water (diffused from the via outward) is experienced.

I. High Via Contact Resistance

Even after developing the polyimide process such that good step-coverage and via formation could be realized and reproduced, monitoring of the via test pattern in terms of total via resistance for a chain of 560 via's varying in size from 0.2 to 0.5 mils square yielded undesirable results. The measured via chain resistance was very high, often open circuited. It is desired to have a total via chain resistance less than 1000 ohms, preferably approaching 1-30 ohms.

It is believed that there are at least two sources of contamination left in the via prior to depositing the second metal layer which result in poor to no contact between the two metal layers. These are an unremoved polyimide residue or a rather thick layer of $Al_2O_3$ as formed on top of the first Al metal layer and cannot be penetrated by sintering processes. To remove any polyimide residues, the 30 second ultrasonic room temperature hydrazine clean or the 10 minute 60°C ultrasonic sulfamic acid solution (15 gm sulfamic acid to 250 ml $H_2O$) clean mentioned earlier is undertaken. To remove an oxide layer from the first layer metal, the following $Al_2O_3$ oxide etches were attempted:

1. Dip in $H_2PO_4$: $H_2O$:$CrO_3$ (22 ml $H_2PO_4$-15%; 280 ml $H_2O$; 1.0 gm $CrO_3$) at 80°C for 8-12 minutes in ultrasonic bath [56]

2. Dip in BHF:EG:$H_2O$ (100 ml of buffered HF; 100 ml ethylene glycol; 100 ml $H_2O$) for 30 seconds at room temperature in ultrasonic bath. BHF consist of 41 gm $NH_4F$; 62 cc $H_2O$; 8.8 cc HF. [57]

3. Dip 5 seconds in concentrated $H_3PO_4$ at 70°C. [58]

Utilization of the above cleaning procedures yielded varied results in terms of via chain resistance yield (less than 1000 ohms). The most consistant results were obtained with the hydrazine dip followed by the ethylene glycol etch. Yields as high as 68% across the wafer for via's of 0.3 mil square or larger have been obtained.

The use of a rf plasma ion back sputter to clean out vias prior to depositing the second layer metal in situ by far renders better results. Using the via test pattern and both Dupont and Hitachi polyimides, yields in the 90 to 99% range have been obtained for all via sizes across the wafer when a back sputter step (as accomplished at MSFC IC Laboratory) was realized. The average via chain resistance for 0.5 mil vias was 55 ohms, and for the 0.2 mils vias, 310 ohms.

# IV. LOW TEMPERATURE DOUBLE-EXPOSED POLYIMIDE/OXIDE DIELECTRIC FOR INCREASING DENSITY

## A. Oversized Via's

In the design of a conventional two-level interconnection system, a "nested via" is employed. Expanded first-level metal pads are used for two reasons: (a) to provide a tolerance for the level-to-level registration at the via definition step and (b) to provide an etch stop so that the passivation layer beneath the first-level metal is not attacked while etching the insulator ($SiO_2$) for via formation. Also, the second metal overlaps the via to protect the first level during the second-level etching.

As seen in Figure 74 (a), in the conventional Al/$SiO_2$/Al system - with nested vias - the Al pad is larger than the via on all four sides. Use of expanded metal pads increases the effective spacing between first-level leads and lowers the packing density. Furthermore, the placement of nested vias for a complex VLSI circuit make the chip layout operation somewhat more cumbersome. Absence of oversize pads for via locations are more attractive for computer-aided designs of interconnection layout and they allow the maximum packing density of first-level interconnections permissible with patterning capabilities.

When polyimide is used as the interlevel dielectric, no attack of the underlying substrate material is experienced so that "over-sized" vias as illustrated in Figure 72(b), can be realized.

B. Double-Exposed Polyimide/Oxide Dielectric

If a thin layer of low temperature oxide is deposited over the first level metal prior to applying the polyimide coating, then this thin oxide layer will act as an etch stop in patterning the second level metal for the "over size" via case. This will alleviate the need for an overlapping second level metal as shown in Figure 72(c), thereby increasing the packing density of the second level metal pattern as well as the first level.

This thin low temperature oxide layer, which could very well be the recently reported photochemical vapor deposited oxide [61] mentioned in the Intrdocution, must be removed from the top of the first level metal in the via such that ohmic contact may be established with the deposited second level metal. Also, it is desirable to deposit a thick layer of polyimide dielectric in order to minimize capacitive coupling between metal levels. The etching of vias in the thick polyimide dielectric layer is a critical step. Sloped via sidewall contours are desirable in order to achieve continuity of the second-level metal. A method which allows removal of the thin oxide from the top of the first level metal and also forms the "over-sized" via with sloped contours utilizes the 'double-exposure' process illustrated in Figure 73. The method uses two via masking steps. The first step allows exposure of the photoresist and subsequent etching of the partially cured polyimide directly over the region for which the thin oxide layer is to be removed as shown in Figure 73(a). A dilute buffered HF solution is used to etch the exposed thin oxide layer with negligible effect to the polyimide layer and underlying substrate. Next, a second via mask is used to expose a larger via

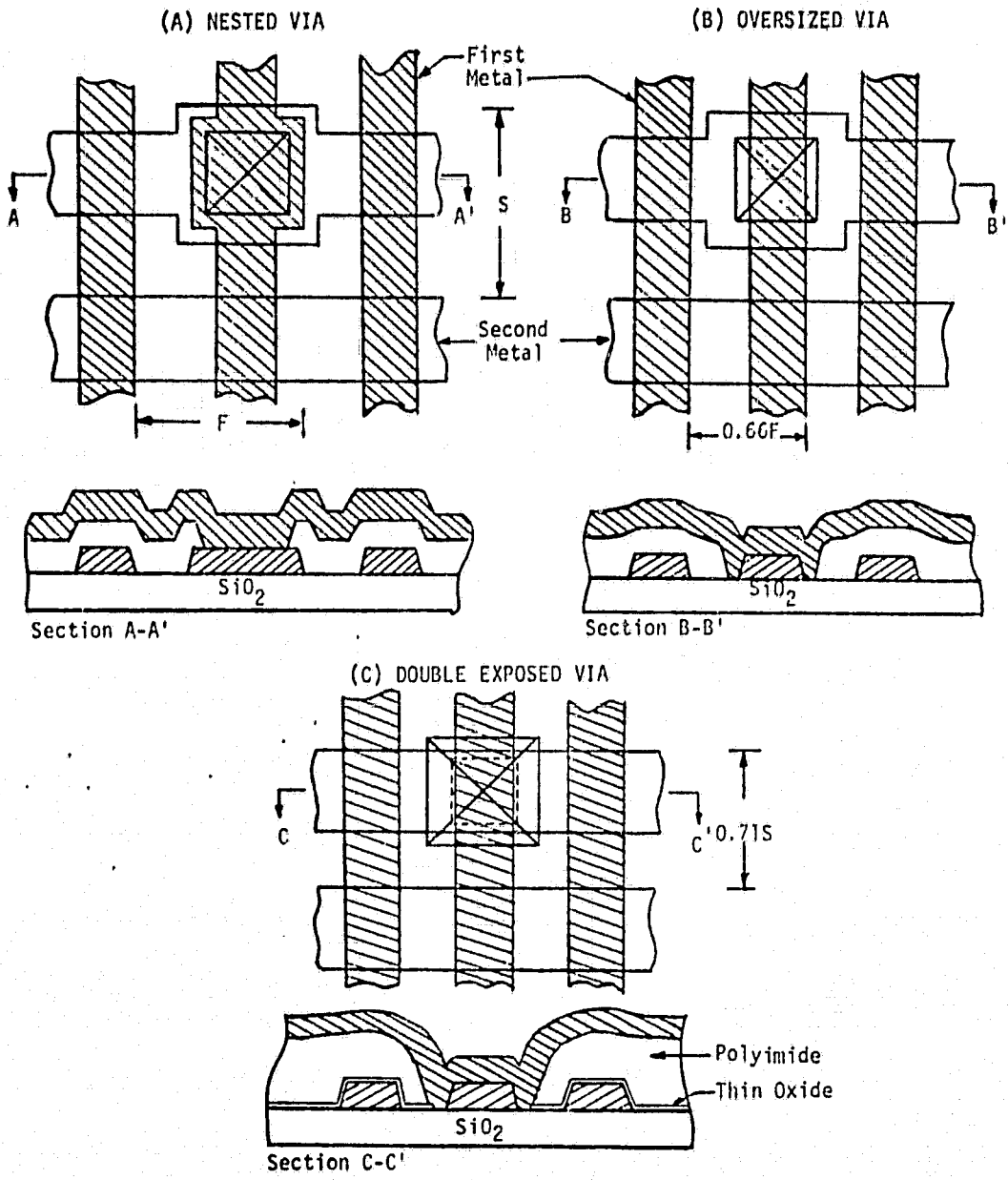



Figure 72. Via interconnect layouts for increasing packing density; (A) the conventional nested via having enlarged first and second level metal, (B) the 'oversized via' allowing increased packing density of first level metal, and (C) the 'double etched via's allowing increased packing density for both metal levels (the dotted outline indicates the oxide etch pattern).

area, resulting in the "over-sized" via having contoured sidewalls as shown in Figure 73(b). Finally, the second level metal is deposited and patterned as shown in Figure 73(c) and 72(c).

In order to study the process variables involved in the double-exposure (and subsequent dielectric delineation) process, a layer of Dupont PI 2555 polyimide was deposited on a silicon wafer having 2000 Å of thermally grown $SiO_2$ on it. A smaller via test pattern mask was used to expose the AZ 1350J photoresist on top of the polyimide layer and then the polyimide was etched at the same time the photoresist was developed. The wafer was then dipped in buffered HF solution to etch the $SiO_2$ layer and dehydrated. A second exposure is realized using a larger size via test pattern. Again, the photoresist and polyimide patterning occurs at the same time. The polyimide is then fully cured (imidized) and the results inspected using a scanning electron microscope as shown in Figure 74. For this test run, the process steps involved the following:

1. Wafer clean and oxidized
2. Deposit Dupont VM651 coupler (.02% in methol alcohol and water)
3. Dehydrate at 50°C - 15 minutes
4. Spin deposit Dupont PI 2555 polyimide on wafer (final cure thickness of 0.5 micron)
5. Partially imidize at 100°C for 30 minutes
6. Spin deposit Shipley AZ1350J at 6000 rpm
7. Prebake photoresist at 90°C - 30 minutes
8. Expose using small via mask in contact aligner

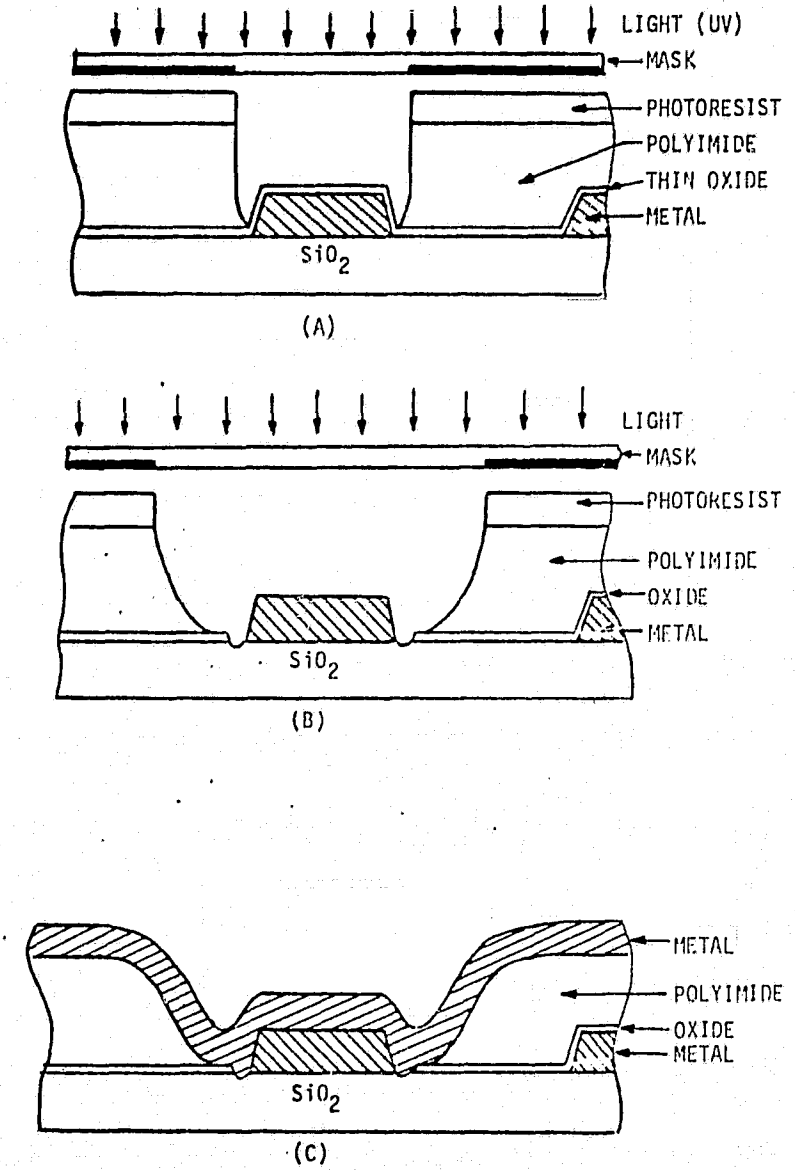



Figure 73. Process steps associated with the double exposure procedure: (A) small via mask opening to etch thin oxide layer, (B) larger via mask opening to realize sloped contours and over-sized via, and (C) deposition of second level metal.

9. Develop in Shipley AZ351, rinse and dehydrate at 50° - 5 min.
10. Dip in BOE to etch oxide
11. Rinse and dehydrate at 50°C - 10 min.
12. Expose using large via mask
13. Develop in AZ351
14. Rinse and dehydrate at 50°C - 5 min.

It should be noted that it is not necessary to use the double exposure process in order to pattern the polymide and the underlying thin oxide layer as shown in Figure 73(c). The etching procedure could be reversed, i.e. pattern the thin oxide layer and then deposit the polyimide and pattern it. The reasons for not using this latter procedure are as follows:

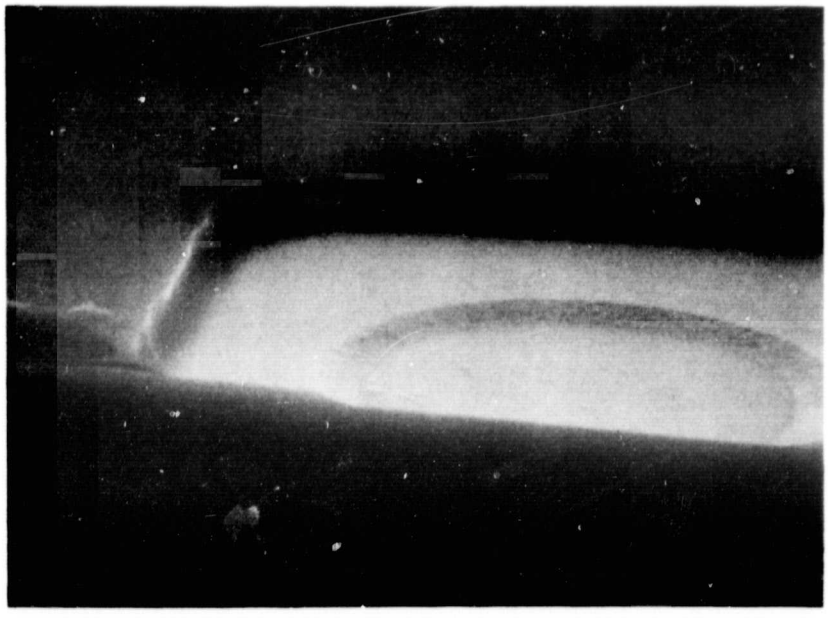


Figure 74. Scanning electron micrograph of test wafer illustrating the double exposure, oxide etch process. Small via mask oxide etch dimension is 3 microns, and larger via mask polyimide etch dimension is 5x8 microns.

(a) Patterning the thin oxide layer first requires extra processing steps (i.e., deposit resist, prebake, mask alignment, develop and rinse, post-bake resist, strip resist, dehydrate and then repeat the process for the polyimide layer).

(b) It is found that by using the process illustrated in Figure 73, often good ohmic contact between first and second level metal in the via can be obtained without the need for a "back-sputter" clean-up step just prior to depositing the second level metal. This back-sputtering can be detrimental to circuit performance, especially for MOS type technologies. In the reverse process, however, when polyimide contacts the first level metal (through the patterned thin oxide) during the pre-cure (pre-imidize) stages before patterning, a back-sputter clean-up step is almost always required in order to gain continuity between metal levels. It is believed that the polyimide resin reacts with the aluminum (or aluminum oxide) to form an "invisible shield" which cannot be easily penetrated with wet chemicals.

As illustrated in Figure 72(c), the use of polyimide as an interlevel dielectric allows a much thicker dielectric to be realized without encountering severe tensile stresses which are commonly characterized by other dielectric materials. As mentioned, a thicker dielectric is highly desirable in terms of decreasing capacitive coupling effects between metal levels.

A SEM micrograph showing the cross-section of one side of the large mask via is illustrated in Figure 75 to demonstrate the sidewall slopes attainable in thick (2 micron) polyimide films. Metal step coverage over such thick layer edges is very good so long as adequate slopes are realized. While Dupont variety polyimide (PI-2555) was used for this particular test wafer, Hitachi PIQ-13 has also been investigated and yields similar results.

In Figure 76, a cross section of a double exposed via is shown after deposition of the second level metal. Very good step coverage is obtained here by using a one-micron thick Al/Si metal layer and 1.5-2 micron thick polyimide. The thin CVD oxide used as an etch stop in patterning the second level metal is approximately 1500Å thick. Contact resistance for a 5x5 micron small via mask dimension is approximately 250 milliohms per via for 7 micron wide interconnect.

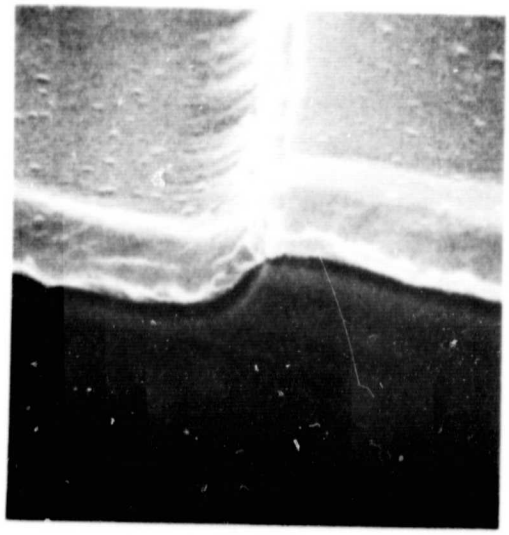


Figure 75. Slope of via sidewall for thick (2 micron) polyimide layer indicating step-coverage realized.

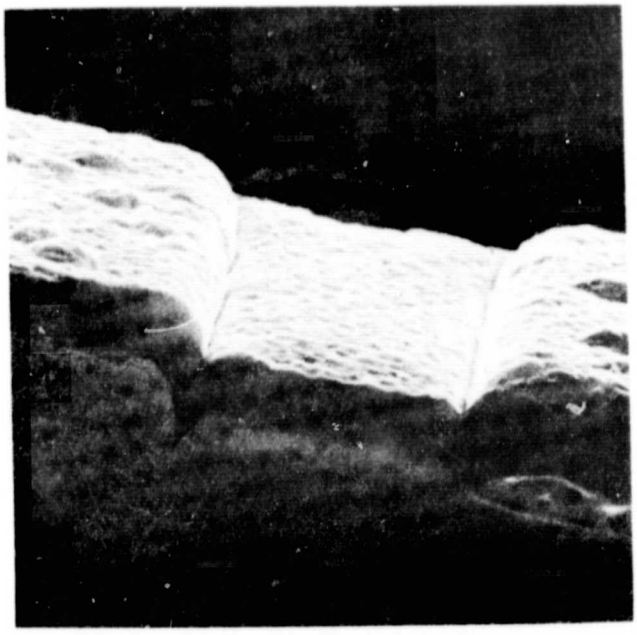


Figure 76. SEM micrograph of double exposed via after deposition of second level metal. Second level metal is approximately one micron thick and seven microns wide. First level metal is one micron thick and five microns wide.

## V. CONCLUSION

Polyimides for use as interlayer dielectrics and passivation layers look very promising. They provide excellent step coverage, a degree of self-levelling, via resolution of at least 3 microns (1.5 microns reported), gradual interface slope change to enhance overlying metal continuity and high resistivity with a good dielectric properties.

Process development utilizing both Dupont and Hitachi polyimide types has been undertaken. A number of potential problem areas have been presented with regard to the process, however, once these have been overcome, an easily executed and reproducible process may be realized.

In addition, a new process for double layer metal interconnect via formation has been investigated which should allow for the following to be realized: a very low temperature process if the photo-chemical vapor deposited oxide is used with polyimide as the interlayer dielectric materials, a decrease in capacitive coupling effects for thick polyimide layers, an increase in packing density for both first and second level metal layers, the absence of oversized pads for vias to facilitate computer-aided design techniques, and a process which can be realized using either wet chemical or dry plasma processing.

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