General Disclaimer

One or more of the Following Statements may affect this Document

- This document has been reproduced from the best copy furnished by the organizational source. It is being released in the interest of making available as much information as possible.

- This document may contain data, which exceeds the sheet parameters. It was furnished in this condition by the organizational source and is the best copy available.

- This document may contain tone-on-tone or color graphs, charts and/or pictures, which have been reproduced in black and white.

- This document is paginated as submitted by the original source.

- Portions of this document are not fully legible due to the historical nature of some of the material. However, it is the best reproduction available from the original submission.

Produced by the NASA Center for Aerospace Information (CASI)

Contract NAS8-34644
SRD-84-016

IMPROVED CHARGE INJECTION DEVICE AND A FOCAL PLANE INTERFACE ELECTRONICS BOARD FOR STELLAR TRACKING

Final Technical Report
(August 17, 1982 to January 31, 1984)

G.J. Michon and H.K. Burke

(NASA-CR-171066) IMPROVED CHARGE INJECTION DEVICE AND A FOCAL PLANE INTERFACE ELECTRONICS BOARD FOR STELLAR TRACKING Final Technical Report, 17 Aug. 1982 - 31 Jan. 1984 (General Electric Co.) 64 p

N84-29092

Unclas
G3/33 19883

January 1984

General Electric Company
Corporate Research and Development
Signal Electronics Laboratory
Schenectady, New York 12301

AUG 1984
RECEIVED
NASA STI FACILITY
ACCESS DEPT.

NASA
National Aeronautics and Space Administration

George C. Marshall Space Flight Center
Huntsville, Alabama 35812

1 Report No. 84SRD016	2 Government Accession No.	3 Recipient's Catalog No.
4 Title and Subtitle: Improved Charge Injection Device and a Focal Plane Interface Electronics Board for Stellar Tracking		5 Report Date: January 1984 6 Performing Organization Code
7 Author(s): G. J. Michon, H. K. Burke		8 Performing Organization Report No.
9 Performing Organization Name and Address: General Electric Company, Corporate Research and Development, Signal Electronics Laboratory, Schenectady, New York 12301		10 Work Unit No. 11 Contract or Grant No. NAS8-34644
12 Sponsoring Agency Name and Address: National Aeronautics and Space Administration, George C. Marshall Space Flight Center, Huntsville, Alabama 35812		13 Type of Report and Period Covered: Final Technical Report (August 17, 1982 to January 31, 1984)

15 Supplementary Notes

16 Abstract

The objectives of this program were to develop an improved Charge Injection Device (CID) stellar tracking sensor and to deliver an operating sensor in a control/readout electronics board. The sensor consists of a shift register scanned, 256×256 CID array organized for readout of 4×4 sub-arrays. The 4×4 sub-arrays can be positioned anywhere within the 256×256 array with a 2 pixel resolution. This allows continuous tracking of a number of stars simultaneously since nine pixels (3×3) centered on any star can always be read out.

A number of basic CID image sensor improvements have been developed at the General Electric Company as a result of on-going CID programs. These improvements include increased quantum efficiency resulting from reduced electrode masking and anti-reflection coatings, reduced fixed pattern noise levels, increased dynamic range, reduced on-chip temporal noise, and on-chip scanner operating margin improvements.

Organization and operation of this sensor and the improvements in design and semiconductor processing are described. A hermetic package incorporating an internal thermoelectric cooler assembled using low temperature solders has been developed. The electronics board, which contains the sensor drivers, amplifiers, sample-hold circuits, multiplexer, analog-to-digital converter, and the sensor temperature control circuits, is also described. Packaged sensors have been evaluated for readout efficiency, spectral quantum efficiency, temporal noise, fixed pattern noise, and dark current. Eight sensors along with two tracker electronics boards have been completed, evaluated, and delivered under this contract.

17 Key Words (Suggested by Author(s))	18 Distribution Statement
CID Imaging, Star Tracking, Solid State Imaging, Stellar Tracking Sensor	

19 Security Classif. (of this report)	20 Security Classif. (of this page)	21 No. of Pages	22 Price*

For sale by the National Technical Information Service, Springfield, Virginia 22161

IMPROVED CHARGE INJECTION DEVICE AND A FOCAL PLANE INTERFACE ELECTRONICS BOARD FOR STELLAR TRACKING

G.J. Michon and H.K. Burke

1. INTRODUCTION

The objectives of this program were to develop an improved Charge Injection Device (CID) stellar tracking sensor and to deliver an operating sensor in a control/readout electronics board. The sensor consists of a shift register scanned, 256×256 CID array organized for readout of 4×4 sub-arrays. The 4×4 sub-arrays can be positioned anywhere within the 256×256 array with a 2-pixel resolution. This allows continuous tracking of a number of stars simultaneously, since nine pixels (3×3) centered on any star can always be read out. Star centroids have been located to a resolution of 2 percent of the pixel spacing of 20 microns using a previously developed CID sensor with the same organization [1].

A number of basic CID image sensor improvements have been developed at the General Electric Company as a result of on-going CID programs. These improvements include increased quantum efficiency resulting from reduced electrode masking and anti-reflection coatings; reduced fixed pattern noise levels through the development of fine grain polysilicon electrodes and a reduction in electrode cross-over area; increased dynamic range for extended objects through the use of a clamp scanner to maintain voltage of unselected array row electrodes; reduced on-chip preamplifier transistor low frequency (1/f) noise through the use of the <100> crystal orientation and improved row and column select scanner design. The control/electronics board provides the interface between the sensor and a microcomputer. The board contains the drivers to convert TTL logic levels to the MOS voltage levels, amplifiers and sample and hold circuitry for signal conditioning, an analog multiplexer to route the four parallel output channels through one analog-to-digital converter, and the analog-to-digital converter. The sensor is mounted on a thermoelectric cooler that is within the hermetically-sealed package. Temperature control circuitry for the sensor is on the electronics board. Low noise power supply regulators are also mounted on this board.

2. PROGRAM HISTORY

A 128×128 CID imager organized for 4×4 sub-array addressing and using multiple nondestructive readout for low noise operation was developed under NASA sponsorship in 1978 [2]. Subsequently, the first 256×256 CID star tracker sensor was designed and fabricated using General Electric internal funding. This program was initiated in August 1982 to fabricate a sensor incorporating improvements in design and silicon processing and to supply the interface control electronics required to operate the sensor.

The sensor, designated ST256E, was designed and the topological layout completed in 1982. An internal topological layout design review was held on November 30, 1982, and after changes were made to increase the aluminum conductor spacing to a more conservative value, the final pattern generation tape was written.

The mask fabrication facility at the Syracuse, New York, General Electric plant had been shut down and was being moved to a new location in late 1982. This facility had been used to fabricate most CID imager masks in the past. An outside mask vendor was consequently needed and Qualitron of Danbury, Connecticut, was chosen. This mask set was the first CID imager set fabricated by this vendor, but there were no problems with mask quality. The

design of the sensor and the identification of an outside mask vendor, however, had taken longer than expected. The delay was caused, in part, by a move of the design group and computer aided design equipment (Calma computer graphics and a VAX super minicomputer) to a new electronics building at Corporate Research and Development. Masks were ordered on January 11, 1983. The completed mask set was received on February 9, 1983, and a 16-wafer lot, designated STS-3 was started into processing on February 16, 1983. The design of the focal plane electronics was also completed during February. Lot STS-3 was lost during processing because of phosphorus contamination during an N^+ doping step and a replacement lot, numbered STS-4, was started on March 8, 1983. Lot STS-4 was completed during the last week of June and probe testing was promptly started.

About this time, the contract was extended to include the delivery of a second focal plane electronics board and an additional sensor.

All the parts needed to assemble an all-solder joint, hermetically-sealed sensor package with an integral thermoelectric cooler were received. The maximum temperature the thermoelectric cooler can withstand is 130° C. It was necessary to develop an assembly procedure, using low temperature solders, that would allow soldering the cooler to the header, the imager chip carrier to the cooler, and hermetically seal the package cover to the header and the cover glass.

Imagers selected at probe test were bonded and wired into chip carriers and then screened for low cosmetic defects, mainly localized pixels with high dark current (bright spots). The best five sensors were then assembled with thermoelectric coolers into the final package.

The sensors were then evaluated for spectral quantum efficiency, temporal noise, fixed pattern noise, and dark current prior to delivery.

3. SENSOR DESIGN

3.1 Organization and Operation

A block diagram of the sensor is shown in Figure 1. During operation, the Vertical Select Scanner is used to address four adjacent rows for readout. These rows, and the compensation row, at the top of the array, are routed to five on-chip transistors. The Clamp Scanner is a duplicate of the Vertical Select Scanner. Clamp Scanner outputs are inverted so that all rows but the addressed rows are connected to the row clamp voltage, RE. The Horizontal Select Scanner is used to address four array column electrodes which are driven by the four enable inputs, EN1 through EN4. This sensor organization allows 4×4 sub-arrays of pixels to be addressed for readout.

The array is cleared of charge by injecting all sensing sites in parallel. This is accomplished by energizing the CVG input to connect all column electrodes to the CVD terminal. When the clamp scanner is cleared (all zeros), all row electrodes are connected to the row clamp terminal, RE. All rows and columns are then driven to their minimum voltage level to effect injection.

A schematic diagram of the array is shown in Figure 2. The vertical select, clamp, and horizontal scanners are two-phase, bootstrapped, ratioless MOS shift registers. The last stage register outputs are brought out to pads for probe testing only; they are not normally wired to package pins. Decoders have been placed between each register stage output and the array selection switches so that the 4×4 sub-array addressed can be positioned with two pixel resolution. The control inputs for these decoders are labelled U and D (up and down) for the vertical decoders, and R and L (right and left) for the horizontal decoder.

ORIGINAL PAGE IS
OF POOR QUALITY

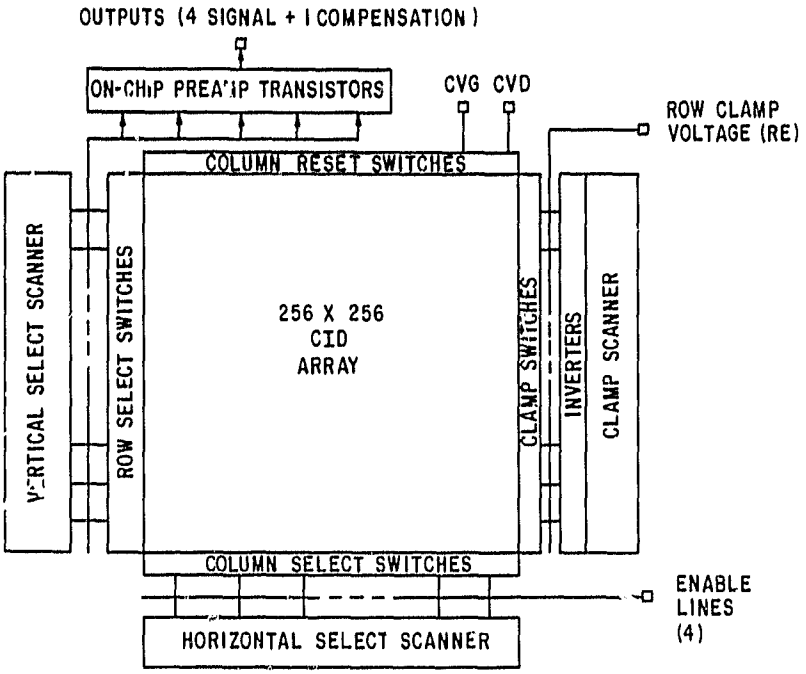

Figure 1. ST256E Block Diagram

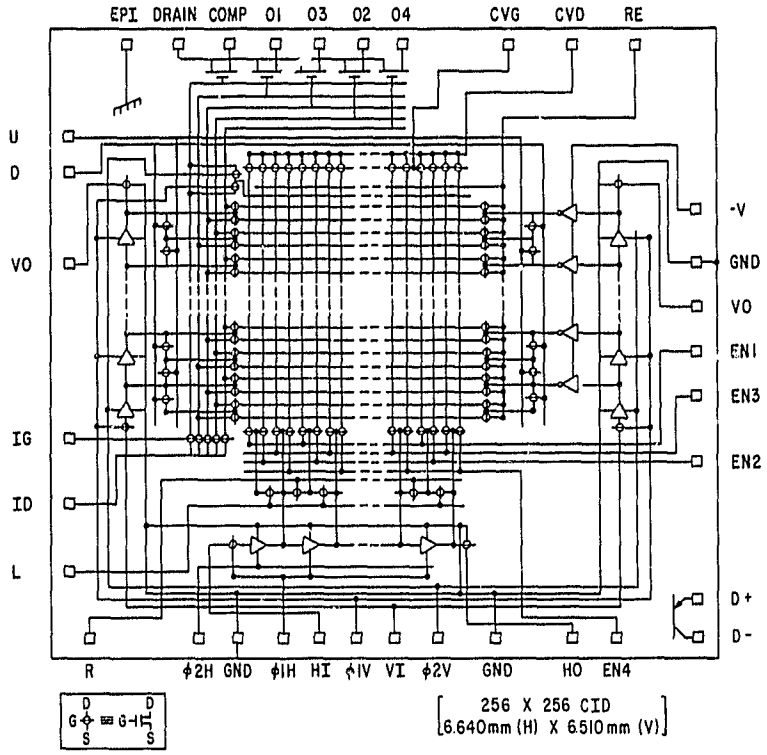

Figure 2. ST256E Schematic Diagram

3.2 Improvements

The major electrical design improvements made in this sensor over the previous ST-256D design are detailed below:

1. Scanner Design - The internal node capacitance of the scanners has been trimmed to increase the parameter margins (clock voltage, transistor threshold voltage, etc.) over which reliable operation can be obtained.

2. Clamp Scanner - The clamp scanner has been added so that voltage can be maintained on all unaddressed array row electrodes. This improves dynamic range when extended objects are being imaged by preventing the photocurrent at unaddressed pixels from discharging the row conductors.

3. On-Chip Preamplifier Transistor - MOS transistors, connected as source followers, have been added in series with each output line. This change should greatly reduce interference from associated electronic circuits by keeping the sensitive signal lines completely within the sensor chip. The topological layout of the sense lines has been balanced to maintain equal capacitance on all signal output lines.

4. Compensation Line - The 257th row, at the top of the array, is used as a compensation line to reduce the dynamic range requirements of the off-chip amplifier, sample-hold circuitry. This line is connected to the negative input of the four signal differential amplifiers. In previous designs, there have been problems in obtaining completely satisfactory operation using this compensation technique. If the compensation line is made identical to all other array rows, it is photosensitive and can cause interference when illuminated. If there is no charge storage region provided for the compensation line pixels, the line capacitance is different than other array lines. In this design, the compensation line is made identical to other array lines but a drain (collector) region has been added adjacent to each compensation line pixel so that any charge collected is drained off. The drain line is connected to RE (Figure 2). In order to completely balance the capacitance of the compensation channel with the signal channels, two row selection switches have been added in series with the compensation line. When either switch is energized by either ϕ1V or ϕ2V, the compensation line is connected to the compensation output bus. The topological detail of this circuitry is shown in Figure 3. In addition, extra row selection switch transistors with total transistor capacitance equal to the active row selection switch transistor capacitance have been added to the compensation output bus to achieve a total capacitance balance.

5. Narrow Electrodes - The primary cause of fixed pattern noise in CID imagers has been traced to variations in the crossover capacitance between row and column electrodes. Since the charge storage capacity of the row and column electrodes is a direct function of electrode width, and the crossover capacitance is a function of the electrode width squared, the signal-to-fixed-pattern noise ratio improves as electrode width is reduced. The electrode size chosen for this design is shown in Figure 4. This structure has $\approx$55 percent of the storage capacitance of the ST-256D design with a field oxide isolation; 80 percent with channel stop isolation. The row-column crossover capacitance has been reduced by a factor of 4.

The major semiconductor process improvements planned for device fabrication are detailed below:

ORIGINAL PAGE IS
OF POOR QUALITY

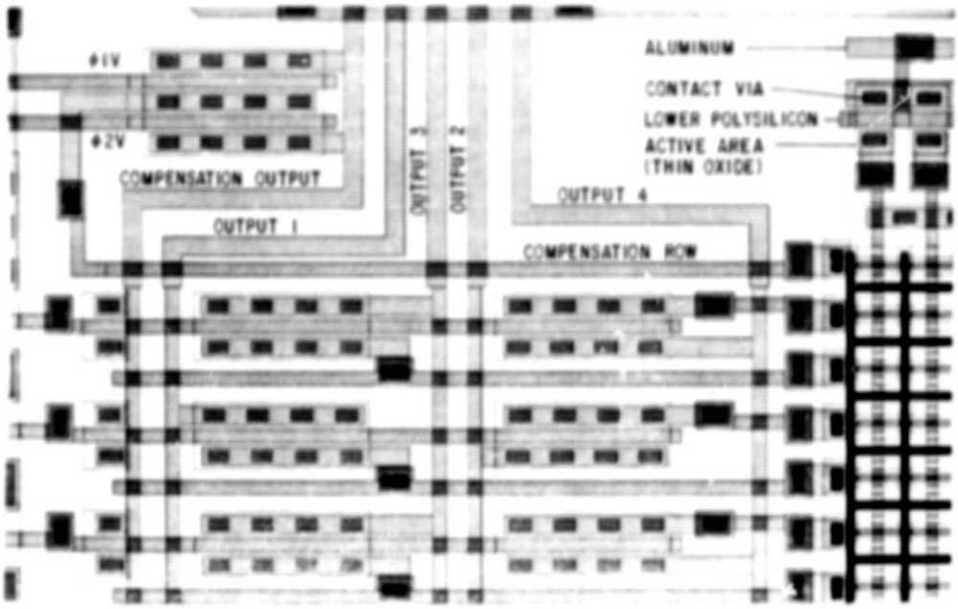

Figure 3. Signal Compensation Bus Topological Layout

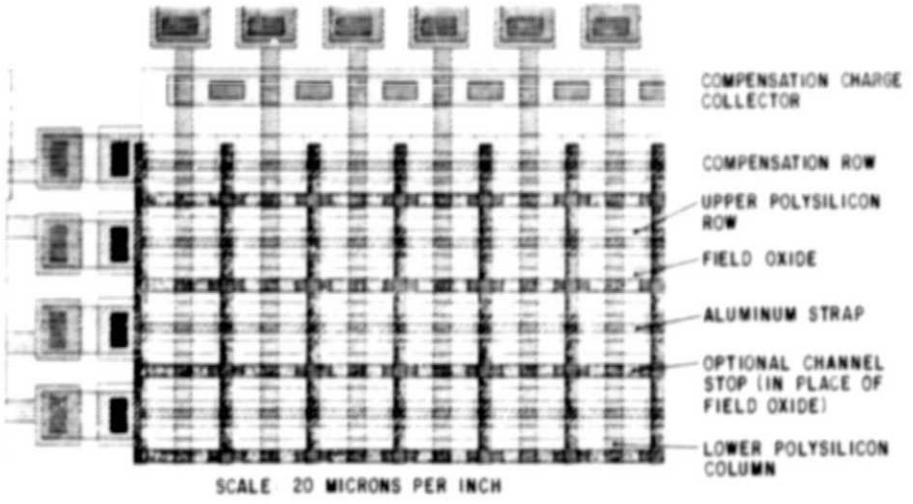

Figure 4. Array Topology

1. Thin Oxide Implant - The exposed thin oxide regions in the array (the thin oxide not covered with electrodes) will be implanted to set the threshold voltage of these regions above the electrode operating voltages. This prevents any surface charging from affecting array operation.

2. Fine Grain Polysilicon - Processes developed to achieve fine grain polysilicon electrodes will be used. This fine grain structure reduces the row-column crossover capacitance variations and, as a result, reduces fixed pattern noise.

3. Channel Stops - Mask levels have been included in this imager design to retain the option of using implanted channel stops in place of the thick field oxide to provide isolation

between adjacent sensing sites. The use of channel stops to achieve a higher, more uniform spectral responsivity is presently being explored at the General Electric Company on other programs. If this approach proves successful, this option can be exercised at a later date.

4. Anti-Reflection Coating - An aluminum patterning process which does not result in a lift-off glass residue layer is planned for these sensors. An anti-reflection silicon nitride layer can then be applied directly on the upper polysilicon electrode to enhance responsivity.

4. SENSOR PACKAGE DESIGN

In order to obtain maximum performance from these CID sensors, it is necessary to cool the devices to reduce dark current levels. At room temperature, dark current shot noise is the dominant temporal noise. Spatial variations in dark current are a significant fixed pattern noise source, particularly localized regions of high dark current (bright spots). If the sensor is cooled below the dew point of its atmosphere the moisture that condenses on the surface of the chip will cause a malfunction. The sensor will recover from a short exposure to a small amount of moisture. In at least one case, however, where the chip was operated for an extended period with liquid water condensed on its surface, the aluminum conductors were destroyed. A hermetically-sealed package is clearly called for in this application.

The sensor packaging procedure has to satisfy a number of requirements. We have not been able to evaluate the sensor low light level performance at wafer probe. It has been necessary to package chips that pass wafer probe in chip carriers so they can be screened prior to assembly onto the thermoelectric coolers. The thermoelectric cooler has been placed within the sensor package to minimize convection heat loss and to keep the glass window free of condensation. An all-solder joint assembly has been chosen to insure that the package is hermetic. The maximum temperature that the thermoelectric cooler can withstand is 130° C. It was necessary to develop an assembly procedure, using low temperature solders, that would allow soldering the cooler to the header, the imager chip carrier to the cooler, and hermetically seal the package cover to the header and to the cover glass.

Normal chip carriers have their contact points on the rear surface and a sealing ring for the cover on the front (chip mounting) side. A custom chip carrier was designed with the contact points on the front surface and the rear surface metallized for solder mounting on the thermoelectric cooler. The drawing of this carrier is shown in Figure 5; the wiring diagram from the chip to the chip carrier, and from the chip carrier to the Tekform header is shown in Figure 6. After the imager is bonded and wired into the chip carrier, the rear of the carrier is tinned with 118° C solder (Indalloy* #1). The Marlow type thermoelectric cooler (purchased with pretinned surfaces) is then reflow soldered to the chip carrier. The Tekform type header is then pretinned in the thermoelectric cooler mounting region with Indalloy #1 solder and reflow soldered to the cooler/chip carrier assembly. The outer edge (cover attaching region) is pretinned at this time with the same solder. An electric discharge technique was used to cut out the window without distorting the cover. After deburring, the edge of the cutout and the Millis metallized glass lids are pretinned with Indalloy #2 (142° C) solder, reflow soldered and given a helium leak check. The edge of the cover is then tinned with Indalloy #1. The parts are then vacuum backed at 100° C for 1 hour and the cover is reflow soldered to the header in a glove box containing 90 percent forming gas and 10 percent helium. The sealed package is then given a helium leak check.

The assembled sensor is shown in Figure 7 before the cover is attached. A heat sink must be used in contact with the rear surface of the Tekform header to remove the heat generated by the thermoelectric cooler, about 5 watts maximum.

* Trademark of Indium Corporation of America, Utica, NY, for low melting point alloys.

ORIGINAL PAGE IS
OF POOR QUALITY

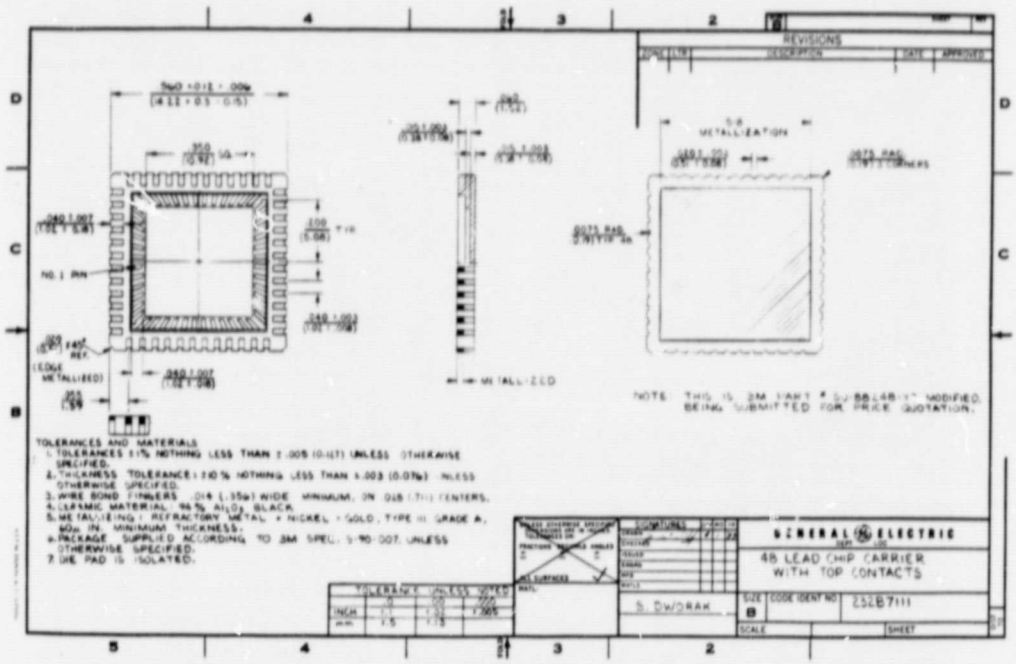

Figure 5. Custom 48 Lead Chip Carrier

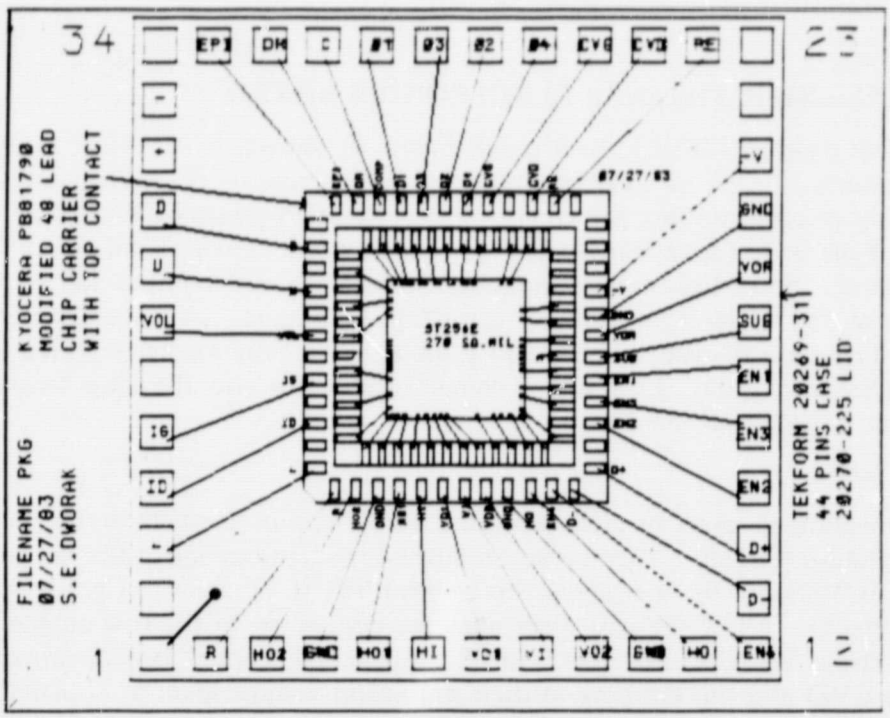

Figure 6. Imager and Chip Carrier Wiring

ORIGINAL PAGE IS
OF POOR QUALITY

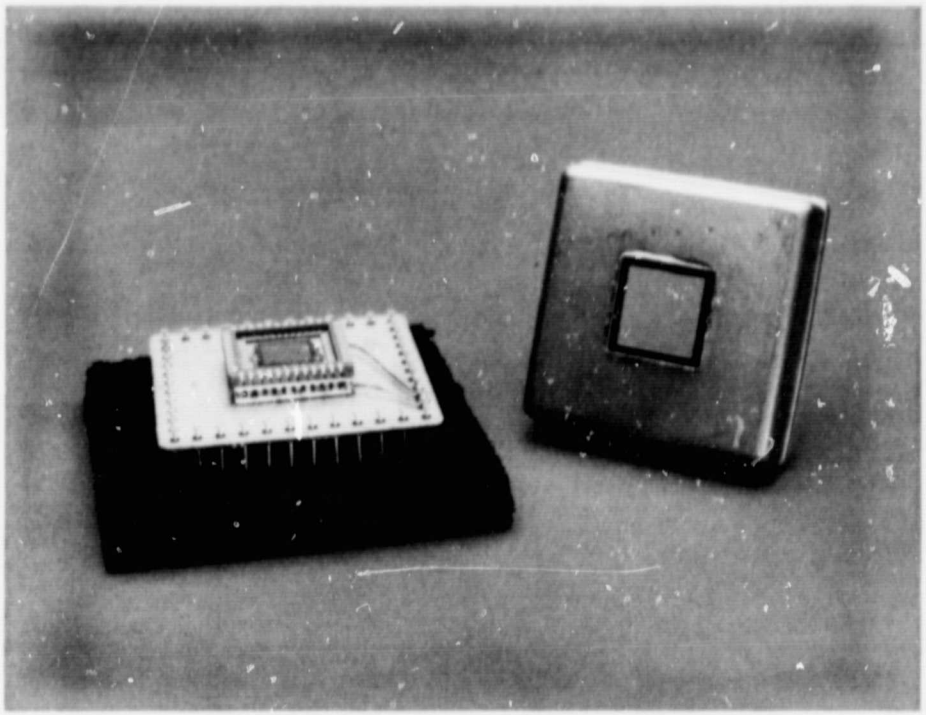

Figure 7. Sensor Assembly

5. FOCAL PLANE INTERFACE ELECTRONICS BOARD

An overall diagram of the electronics board is shown in drawing number 152D6254 (ST256E Camera), a copy of which is appended to this report. TTL level timing signals from the controlling microcomputer are converted to the appropriate MOS voltage levels to drive the sensor. Type 139CJ level converters along with series resistors and clamp diodes are used for this purpose. Four differential amplifiers boost the sensor output signals which are then sampled using the correlated double sampling technique. A programmable operational amplifier, with a gain of unity, is used to multiplex the four analog sampled signals into the analog-to-digital converter. Low noise voltage regulators and the chip temperature control servo are also included on this board.

5.1 Sensor Drive

Frame injection is used to clear all array pixels simultaneously at the beginning of the charge integration period. This is accomplished by connecting all array columns to the column VD (CVD) pin by energizing the column VG (CVG) control pin with a -20 volt signal (see Figure 2). All of the row electrodes are connected to the row enable (RE) pin since the clamp scanner was cleared at the end of the previous frame. Injection is effected by driving both the CVD and the RE pins to their minimum voltage level of -2 volts. At the end of the injection pulse (about 100 μsec), the columns and rows are returned to their charge integration levels, CVD to -17 volts and RE to -8 volts. The CVG pin is then switched off (to 0 volts).

Column and row shift registers, in conjunction with the right/left (R/L) and up/down (U/D) control lines, are then scanned to select the desired 4×4 sub-array. The shift registers use non-overlapping 2-phase clock signals, that switch between -2 and -17 volts. Horizontal

and vertical input pulses (HIN and VIN) are clocked into the registers by the 01H and 01V clock pulses respectively. The R/L and U/D pins are driven between 0 and -20 volts.

The 4×4 sub-array is read out by driving the four enable lines (E1 through E4) in time sequence. Each enable line can be driven as many times as required, with each pulse effecting one non-destructive readout operation. The IG pin is pulsed to -14 volts at the beginning of each column drive cycle to reset the signal lines to the ID reference level of -8 volts.

At the end of the readout interval, the shift registers are cleared by driving the horizontal and vertical phase lines with the proper number of pulses. The next frame can commence at this time.

5.2 Low Noise Amplifiers

A schematic of the low noise amplifiers is given in drawing number 196C4204, which is appended to this report. The sources of the five on-chip transistors are connected to source load resistors (8.2K each) at inputs C and 1 through 4. These signals are capacitively coupled to four 2N5565 junction fet pairs connected as differential source followers. The difference signal between the four input signals (1,2,3,4) and the compensation signal (C) is taken by the four AD818/NE5534 differential amplifiers. The gain of each channel is set to 100 by selecting the AD818 emitter-to-emitter resistors.

5.3 Post Amplifiers/Sample and Hold

Readout of the CID sensor requires the use of correlated double sampling to control KTC noise. During each readout cycle, the imager row and output multiplex signal line (on-chip) is reset by the IG pulse and allowed to float. Since this line has a capacitive source impedance, this reset operation introduces a KTC offset noise after each reset pulse. A sample of this offset, after amplification, is stored on the 0.01 ufd input capacitor to the LF298 sampler when the RESTORE pulse is applied (see drawing 152D6254). Since this sample of the KTC offset is in series with the signal, it is automatically subtracted from the imager output. The selected column is then driven to transfer charge from the column to the row electrode. The resulting signal is then sampled by the HA2425 sampling circuit. This sampling circuit has a gain of 10 to give an overall signal processing gain of 1000 before the analog-to-digital converter.

5.4 Multiplexer, Analog-to-Digital Converter

A programmable operational amplifier, HA2405, has been connected as a unity gain, non-inverting follower to multiplex the four parallel output samples into one analog-to-digital converter. A Micronetworks type MN5245 12 bit analog-to-digital converter, connected for a 0 to +5 volt input range, is connected to the output connector with type SN74365 non-inverting drivers. The SN74366 inverting drivers can be used if an inversion is needed at the digital output.

5.5 Sensor Temperature Control

The schematic of the temperature controller, drawing number 179C4307, is appended. An on-chip silicon diode is used to measure sensor temperature. This diode is forward biased at 100 microamps to generate approximately 600 millivolts at 25° C. Its temperature coefficient is very close to -2 millivolts per degree celsius. The 5K temperature set potentiometer output voltage is compared with the temperature sensing diode voltage using a fet input operational amplifier (TL081) connected as an integrator. A 5 second time constant lead has been inserted in the feedback path to stabilize the system. The amplifier output has been clamped to +5

volts maximum to keep the integrator from going to its internal voltage limit of +12 volts when in saturation. The system would have a very long saturation recovery time at the higher saturation voltage. An optocoupler, type 6N139 connects the amplifier output to the power transistor that drives the thermoelectric cooler. A second TL081 is used to generate a -10 mv/° C for data logging purposes. Finally, a 741 operational amplifier with a gain of 0.1 and proper offset is used to indicate chip temperature. Its scale is 1 millivolt per degree celsius, with 25 °C equal to +25 millivolts.

6. TEST RESULTS

6.1 Wafer Probe Tests

The first three wafers from lot STS-4 were probe tested using an existing probe camera. The functional yield was high. Wafer #6 yielded 24 imagers; wafer #8 yielded 9 imagers; and wafer #9 yielded 21 imagers. This is an overall functional yield of 23%. Fourteen imagers were selected for packaging into chip carriers. The main cosmetic defect encountered was localized regions of high dark current, i.e., bright spots.

6.2 Chip Carrier Mounted Sensor Screening

The imagers mounted in chip carriers were operated in the Focal Plane Interface Electronics Board to further screen these devices so that the better ones could be assembled onto thermoelectric coolers in the final package for evaluation and delivery. These devices were operated at room temperature. The dark field image produced by one of these devices is shown in Figure 8; the bright spots visible at room temperatuare normally cool out when these sensors are operated below 0° C. The image is broken into six segments because the microcomputer used to operate the Focal Plane Interface Electronics Board did not have enough memory available to store the complete image.

Temporal noise and histogram data on bright spots was used to select the best devices for final packaging.

6.3 Packaged Sensor Evaluation Results

In order to properly evaluate the performance of these sensors, it was necessary to calibrate the transfer function of the system from the incident photon flux to the digital output. A block diagram of the system is shown in Figure 9. Spectral quantum efficiency defines the ratio of the charge (expressed in electrons) collected and stored in the CID image sensing array to the incident photons, as a function of wavelength. The readout efficiency is the fraction of the collected charge that appears on the CID output capacitance upon readout. The total gain is the product of the on-chip source follower gain and the differential amplifier gain. Once the transfer function from stored charge in the array to the output is known, spectral quantum efficiency can be measured, and noise and dark current levels can be measured in terms of either incident photons or photoelectrons.

6.3.1 Readout Efficiency

Charge is stored in a CID imager in inversion layers of MOS capacitors as diagrammed in Figure 10. Prior to readout, with -17 volts applied to the column electrodes and -8 volts applied to the row electrodes all of the signal charge is stored under the column electrodes, Figure 10a. During readout, when the column voltage is switched from -17 volts to -2 volts, the signal charge transfers from under the column electrode to under the row electrode, Figure 10b. A capacitive charge divider exists between the silicon surface and the row electrode (oxide capacitance), and the silicon surface and the substrate (silicon depletion capacitance), Figure 10c. Most of the transferred charge appears on the row electrode as a displacement

ORIGINAL PAGE IS
OF POOR QUALITY

Figure 8. Typical Dark Field Image

charge because the oxide capacitance is larger than the silicon depletion capacitance. The fraction that appears on the row electrode is called the readout efficiency. In the absence of edge fringing effects, this fraction is .94 for the structure used in these imagers (910 angstrom equivalent oxide thickness, 10 ohm-cm N-type substrate doping level). Readout efficiency can be calculated taking edge fringing effects into account, but certain details concerning the edge effects (surface doping of the silicon, shape of the field oxide-thin oxide interface, etc.) are not well known with the result that this calculation is not very accurate. The readout efficiency can be measured directly on the ST256E sensor because a drain was placed adjacent to the compensation line. This drain, the compensation charge collector in Figure 4, can be used to directly transfer charge to and from the compensation row inversion layers, and the fraction of this charge that appears on the compensation line can be measured. The measured readout efficiency of device STS-4-6-30 was .747.

The output capacitance (on-chip) was measured to be 10.8 pf, and the on-chip source follower gain, with an 8.2K load resistor, was 0.907. The full scale capability of this system is 500,000 electrons, and the scale factor is 122 electrons/LSB.

ORIGINAL PAGE IS
OF POOR QUALITY

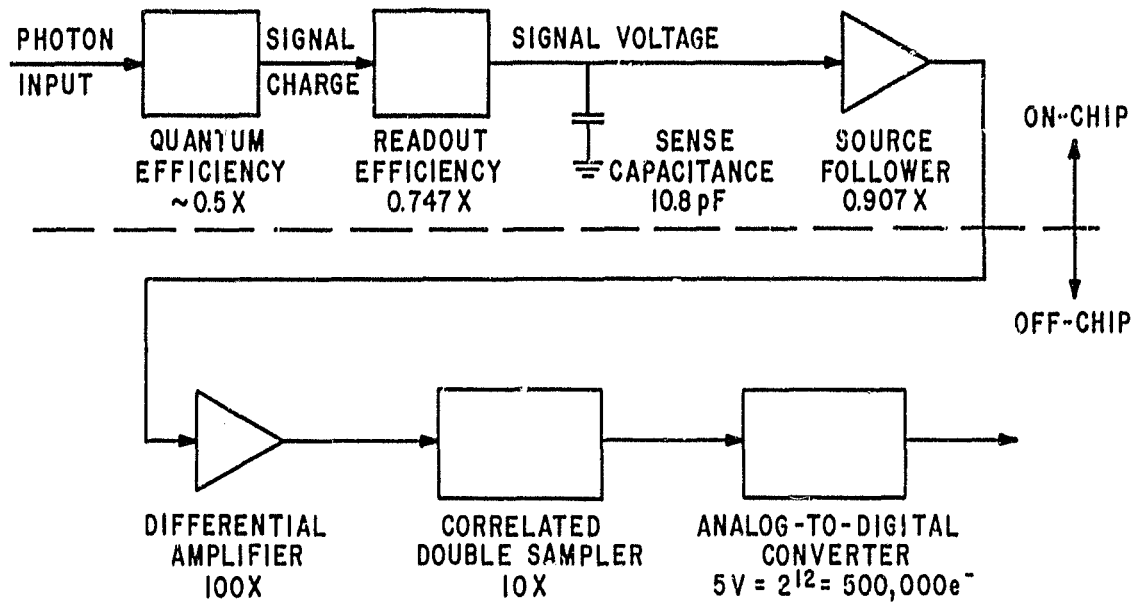

Figure 9. System Transfer Function

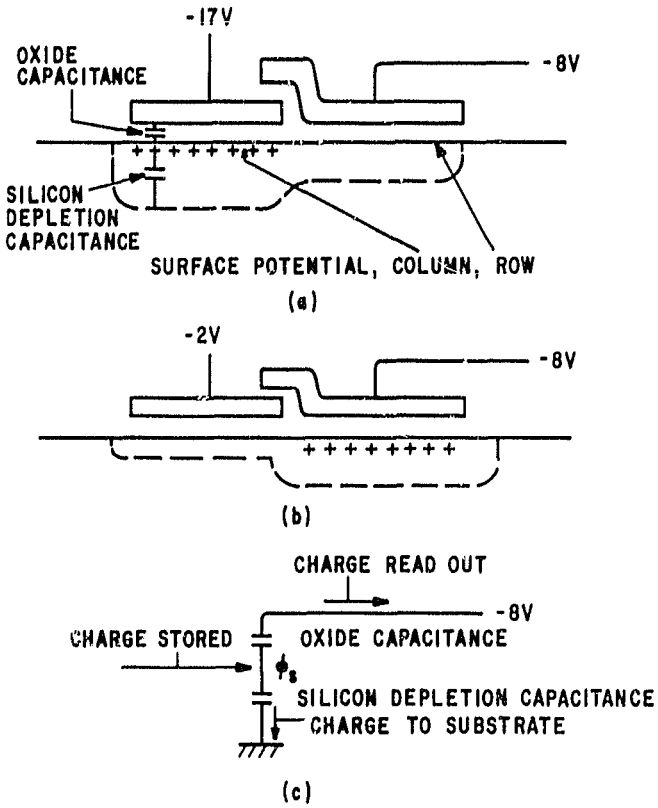

Figure 10. Readout Efficiency

ORIGINAL PA
OF POOR QUALITY

6.3.2 Spectral Quantum Efficiency

Spectral quantum efficiency was measured using a Bausch and Lomb grating monochromater and a UDT silicon diode detector as a reference. This silicon reference diode was calibrated against a reference diode calibrated by the National Bureau of Standards. Figure 11 shows measured spectral quantum efficiency for two sensors from lot STS-4, wafer 6, one without the package cover glass (#24), and one with cover glass (#26). The cover glass is not anti-reflection coated and causes about an 8% reflection loss. One device from wafer 9 (#STS-4-9-26) was given an extended spectral response measurement, from 200 nM in the UV, to 1100 nM, Figure 12. A vacuum photodiode was used as a reference in the uv region, from 200 nM to 400 nM.

6.3.3 Temporal Noise

The temporal noise sources in CID imagers have been evaluated in a previous study [3]. The significant noise sources in this device are KTC noise introduced by reseting the sense line capacitance, the row selection switch resistive noise, and amplifier noise. Noise generated in the row conductors is neglible because the polysilicon rows have been strapped with high conductivity aluminum. Correlated double sampling is used to surpress the KTC noise [4] The Johnson noise contributed by the row select switch and amplifier transistors is given in Table 1. Each noise voltage has been refered to the on-chip sense line.

In addition to Johnson noise, the on-chip MOS source follower transistors exhibit excess low frequency noise commonly called 1/f noise. The mean value of on-chip transistor noise measured on two devices from each of wafers #6, 9, and 11; lot STS4, is plotted in Figure 13. The 1/f model of this noise is shown dashed in this figure.

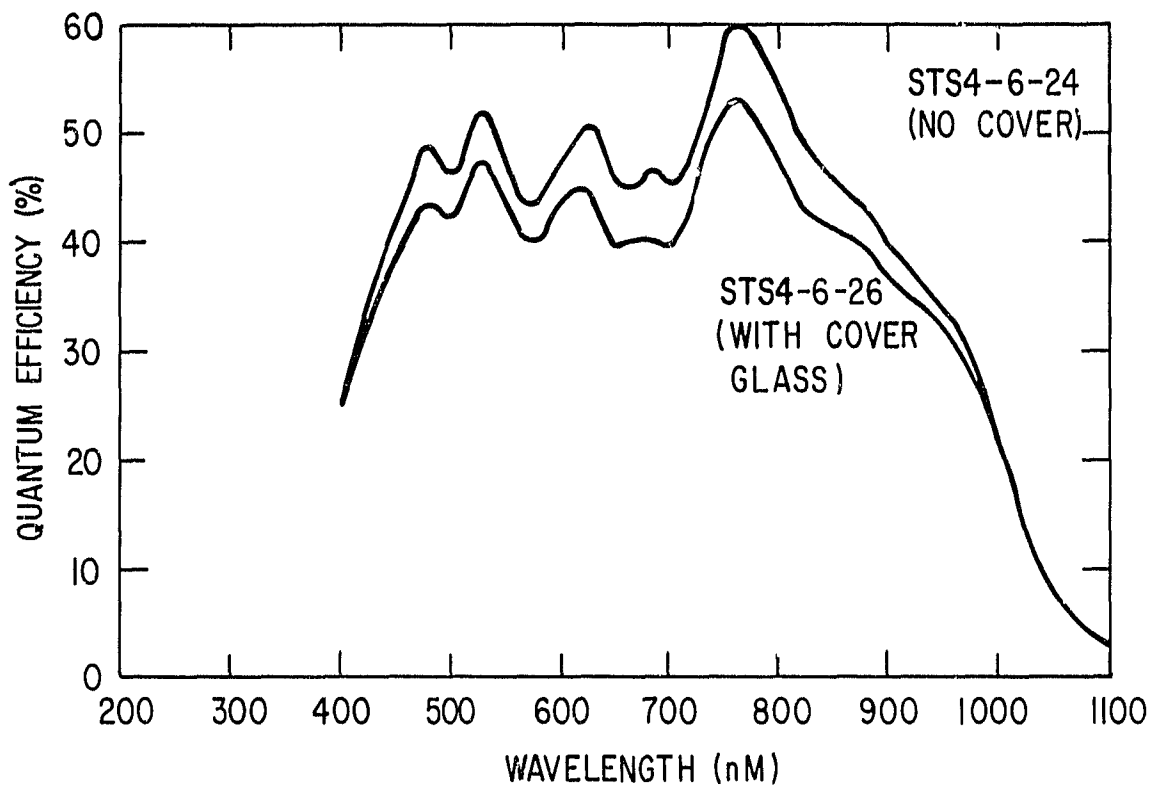

Figure 11. Spectral Quantum Efficiency

ORIGINAL PAGE IS
OF POOR QUALITY

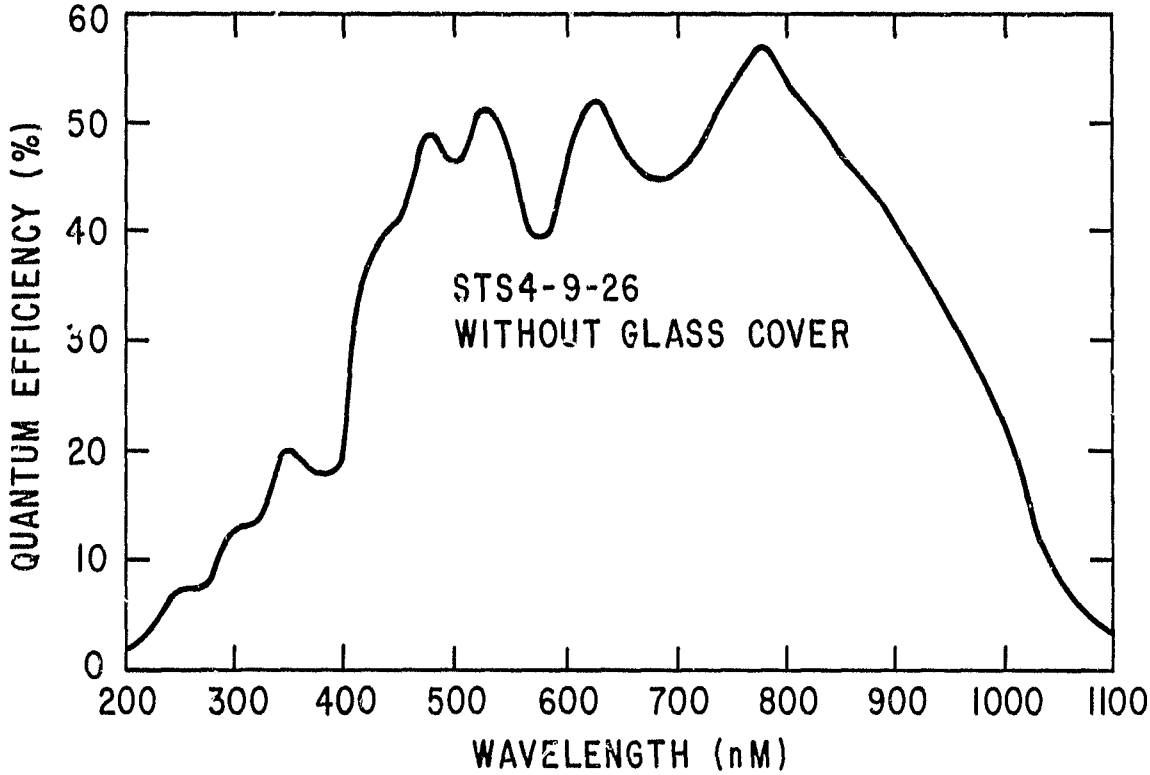

Figure 12. UV Extended Spectral Quantum Efficiency

Table 1

Temporal Noise Source	Equivalent Input Noise (Nanovolts/root Hertz)
Row Select Switch	1.5
On-chip Source Follower	2.3
2N5565 J-Fet Source Follower	1.9
AD818 Amplifier Transistor	2.6
RMS Total	4.2

The total noise can be calculated by integrating the noise power spectral density multiplied by the system transfer function. The noise power is given by:

$$e_n^2 = \int_0^\infty \left[\frac{K}{f} + e_j^2\right]\left[1 - Cos\ (Pi\ \frac{f}{f_s})\right]\left[\frac{1}{1 + (\frac{f}{f_c})^2}\right] df \qquad (1)$$

where:

$\left[\frac{K}{f} + e_j^2\right]$ is the noise power spectrum

ORIGINAL PAGE IS
OF POOR QUALITY

$\left[1 - Cos\ (PI\ \frac{f}{f_s})\right]$ is the correlated double sampling transfer function

$\left[\frac{1}{1 + (\frac{f}{f_c})^2}\right]$ is the amplifier bandwidth limiting

and:

K = 1/f noise constant = $1.2 \times 10^{-12} v^2$
e_j = total Johnson noise = $4.2 \times 10^{-9} v/Hz^{1/2}$
f_s = sampling frequency = 5000 Hz
f_c = amplifier cutoff frequency = 8000 Hz

A plot of the noise spectral density before and after signal processing is shown in Figure 14. A numerical integration of equation (1) from 10 Hertz to 1 MegaHertz results in a noise voltage of 1.7 microvolts. Since a differential amplifier and frame differencing are used, the noise voltage is doubled. The noise charge at the on-chip sense line is simply the noise voltage times the sense capacitance. In terms of noise electrons referred to the charge packet in the array,

$$n = \frac{C_s \times v_n}{(q \times E_{ro})}$$

where:

C_s = Sense capacitance = $10.8 \times 10^{-12} fd$
v_v = noise voltage = $3.4 \times 10^{-6} V$

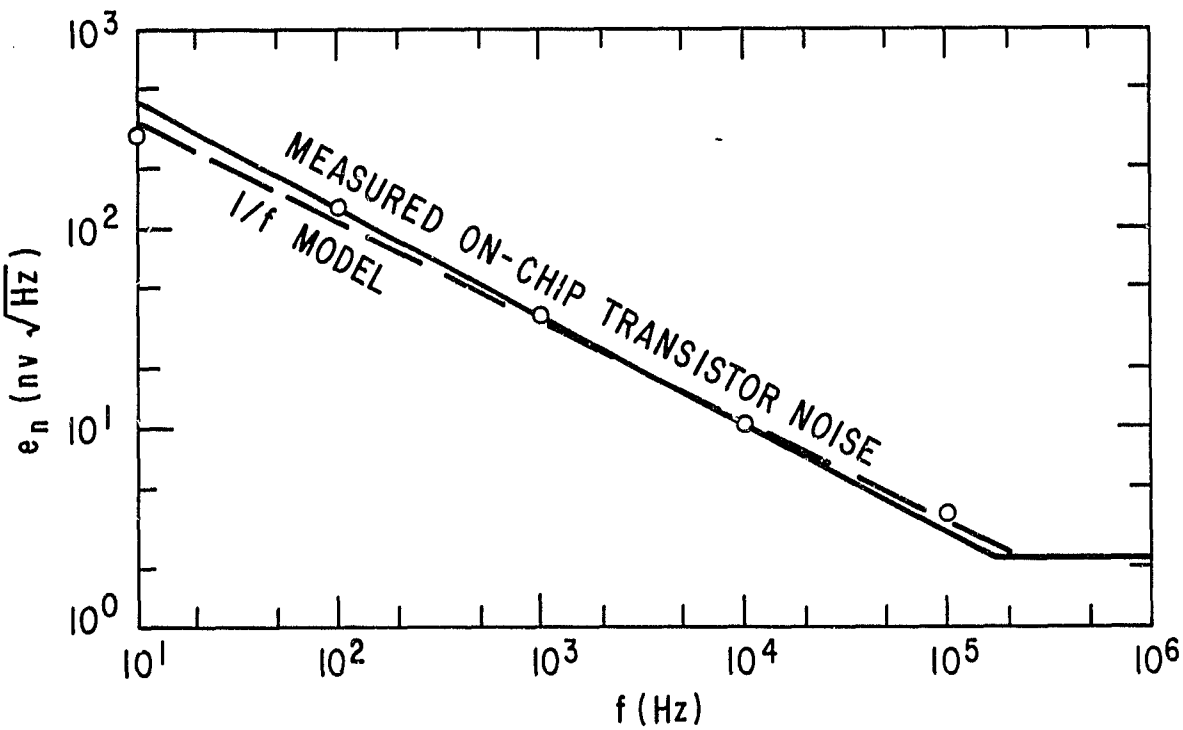

Figure 13. Transistor Noise Spectral Density

ORIGINAL PAGE IS
OF POOR QUALITY

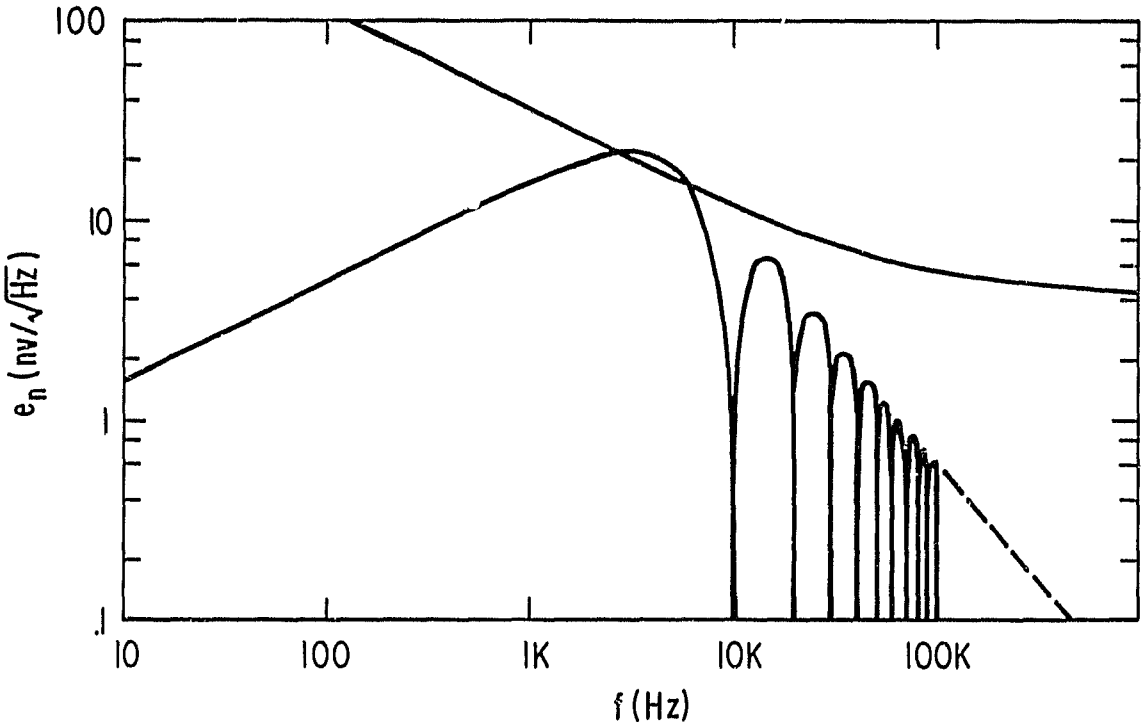

Figure 14. Total Noise Spectral Density Before and After Signal Processing

q = electronic charge = $1.6 \times 10^{-19} C$
E_{ro} = readout efficiency = .747

The calculated number of noise electrons refered to the charge packet in the array is 296 for a single read, and 37 for 64 nondestructive readout operations. The measured values for a 4×4 sub array read out in the track mode are given in Table 2.

6.3.4 Fixed Pattern Noise

Spatial variations in row-column crossover capacitance and in bias charge at sensing sites (pixels) in the CID array result in a background pattern in the absence of signal called fixed pattern noise. Two components of this noise have been observed in the ST256E output signals. The first component is column oriented and is the result of unequal coupling of the four column enable drive lines (E1 through E4) to the sense lines. This component repeats for each 4×4 subarray readout and can be subtracted from the outputs. The second component varies from pixel-to-pixel across the array and is removed from the data when the frame difference is taken. The magnitude of the second component varies from 0.2 volts peak-to-peak (4,000 electrons rms) adjacent to the compensation row to 0.8 volts peak- to-peak (16,000 electrons rms) elsewhere in the array. The main effect of this fixed pattern noise is to reduce the range available for signal at the analog-to-digital converter.

6.3.5 Dark Current

The average room temperature dark current measured on arrays from lot STS4 ranged from .37 to .77 nanoamps per square centimeter except for device STS4-6-24 which had an average dark current of 2.6 nanoamps per square centimeter. Localized regions of high dark current (bright spots) are present to varying degrees with this lot of imagers and is attributed to defects in the starting silicon.

Table 2
Device ST84-6-13

Temporal Noise (T=23.5 C):

Mean (Carriers)

1824.74	1588.13	1812.06	1533.74
1808.81	1490.57	2117.11	1637.58
1802.28	1527.81	1556.85	1565
1966.06	1589.65	1733.86	1503.3

RMS Noise (Carriers)

63.3628	68.1849	69.068	61.7789
66.0552	73.8415	82.3465	59.3831
63.5482	62.588	63.6022	64.8868
68.2364	69.7306	61.6028	58.4498

Avg. Mean	Avg. Noise
1691.1	66.0416

Temporal Noise (T=.1 C):

Mean (Carriers)

847.492	452.057	261.156	304.572
838.705	267.191	273.421	305.318
879.335	441.549	436.615	386.222
930.011	449.128	451.613	344.652

RMS Noise (Carriers)

44.3039	52.8901	46.9923	47.6504
54.2826	52.1647	49.5088	51.3946
46.8922	44.3037	45.9558	46.7094
50.7872	47.4062	47.357	53.7509

Avg. Mean	Avg. Noise
491.815	48.8969

Temporal Noise (T= -10C):

Mean (Carriers)

826.547	438.407	411.037	274.273
665.519	372.945	238.276	259.15
984.948	474.671	330.541	208.492
923.71	479.623	304.697	319.376

RMS Noise (Carriers)

47.7512	53.0035	49.9027	40.6375
52.221	55.0489	62.7751	57.1029
49.7957	43.6554	46.5069	42.6541
41.5405	46.0072	44.6672	46.2975

Avg. Mean	Avg. Noise
469.513	48.7173

7. GENERAL PROGRAM ASSESSMENT

The intent of this program was to improve the performance of the CID 256×256 star-tracking sensor. The improvements sought are detailed in section 3.2 and the results achieved are assessed here.

1. Scanner Design - The basic scanner design has been improved and reliable operation has been achieved.
2. Clamp Scanner - A row clamp scanner has been added such that extended objects (general scenes) can be imaged.
3. On-chip Preamplifier Transistors - Preamplifier transistors have been incorporated in the sensor and immunity from external intefering signals has been greatly improved. The ST256E sensor has been operated at the end of 8 inches of cable with no performance degradation. The low frequency noise (1/f noise) of these transistors is somewhat higher than expected. The expected noise level of 30 electrons has not been achieved. The noise level calculated using the achieved 1/f noise spectrum is 37 electrons; the measured noise levels range between 48 and 71 electrons for various arrays.
4. Compensation Line - The compensation line drain has been added as described is section 3.2. This P^+ drain is in the N^- thin oxide implant region and the resulting P^+N^+ diode has as avalanche breakdown voltage of 8 volts. This breakdown voltage is very close to the 7.5 volt operating level. A mask change has been made to eliminate the offending junction in future lots processed. The desired capacitive balance of the compensation line with the four signal lines was not achieved with this lot. A change in the aluminum mask was made to improve the capacitive balance in future lots of imagers.
5. Narrow Electrodes - Narrow electrodes have been used successfully in this design. These narrow electrodes, coupled with the thin oxide implant, fine grain polysilicon and anti-reflection coating have resulted in quantum efficiencies in the 50 percent range; usable response from 200 to 1100 nanometers, and reduced fixed-pattern-noise. The 500,000 electron storage capacity design goal for the narrow electrode structure has been achieved.

The most obvious problem with this lot of imagers is the large number of bright spots encountered. This has been a problem with lots previously processed on bulk silicon and is attributed to defects in the wafers as received from the vendor. We know of no way to screen wafers for bright spots short of fabricating imagers on sample wafers. If bulk imagers were processed on a regular basis, this sampling could be done and silicon vendors could be qualified as is the case with our commercial, epitaxial CID imagers. It may also be possible to improve the in-process gettering of silicon defects.

8. CONCLUSIONS

The objectives of this program have, in general, been achieved. Problems that were encountered with capacitance balance and avalanche breakdown voltage did not degrade performance significantly, and the sensor photomasks have been changed to correct these problems. The temporal noise level is somewhat higher than desired, but well within the high performance range needed for star-tracking applications. The spectral quantum efficiency achieved is considered outstanding. The design of a hermetic package with integral thermoelectric cooler and the use of on-chip preamplifiers has resulted in a sensor that should be reliable and easy to incorporate in tracking systems.

9. REFERENCES

[1] Jones, C., and Kollodge, J.C., "An Advanced Tracker Design for Pointing and Control of Space Vehicles Using the Charge Injection Device," AAS 82-031, January 1982.

[2] Burke, H.K., Michon, G.J., Tomlinson, H.W., Vogelsong, T.L., Grafinger, A., and Wilson, R., "Design, Fabrication, and Delivery of a Charge Injection Device as a Stellar Tracking Device," Contract NAS8-32801, SRD-78-171, April 1979.

[3] Michon, G.J., Burke, H.K., Vogelsong, T.L., and Wang, K., "Study of Noise in CID Array Systems," Contract N00173-77-C-0054, SRD-78-156, November 1978.

[4] White, M.H., Lampe, D.R., Blaha, F.C., and Mack, I.A., "Characterization of Surface Channel CCD Image Arrays at Low Light Levels," *IEEE Journal of Solid State Circuits SC-9*, 1-13.

APPENDIX

Microcomputer Assembly Language Program

```
CROMEMCO CDOS Z80 ASSEMBLER version 02.15                    PAGE 0001
                    0001 ; 7/21/83 STARS
                    0002 ;
                    0003 ; STAR TRACKER CONTROLLER
                    0004 ; FOR THE ST256 DEVICE
                    0005 ;
                    0006 ; B=PIXEL ROW LOCATION
                    0007 ; C=PIXEL COLUMN LOCATION
                    0008 ; D,E=DELAY TIME
                    0009 ; H,L=MEMORY LOCATION
                    0010 ;
                    0011 ; I/O PORT DEFINITIONS:
                    0012 ;   04H    =FRONT PANEL LED'S AND SWITCHES
                    0013 ;   20-22H=CONTROL SIGNALS TO CAMERA BOARD
                    0014 ;   24-26H=A/D CONTROL AND DATA
                    0015 ;   28H    =A/D START CONVERSION STROBE
                    0016 ;
0800  C30008        0017 STARS:  JP      START
0803                0018         ORG     2340H
2340  10            0019 COL:    DEFB    16        ;PIXEL COLUMN LOCATION
2341  10            0020 ROW:    DEFB    16        ;PIXEL ROW LOCATION
2342  40            0021 NSUM:   DEFB    64        ;NUMBER OF SUMS PER PIXEL
      (2300)        0022 BASE:   EQU     2300H     ;TEMPORARY STORAGE MEMORY
      (0004)        0023 LED:    EQU     04H       ;SWITCH/LED PORT
      (0028)        0024 STROBE: EQU     28H       ;A/D START CONVERSION STROBE
2343                0025         ORG     800H
                    0026 ;
                    0027 ;******************************
                    0028 ; THIS SECTION CONTAINS THE
                    0029 ; MACRO DEFINITIONS
                    0030 ;******************************
                    0031 ;
                    0032 GETDATA:MACRO               ;SUM AND STORE DATA MACRO
                    0033         IN      A,20H     ;GET LOWER 8 BITS OF DATA
                    0034         ADD     (HL)
                    0035         LD      (HL),A    ;SUM AND STORE LOW 8 BITS
                    0036         INC     L
                    0037         IN      A,21H     ;GET UPPER 4 BITS OF DATA
                    0038         OUT     STROBE,A;START NEXT CONVERSION
                    0039         ADC     (HL)
                    0040         LD      (HL),A    ;SUM AND STORE MID 8 BITS
                    0041         INC     L
                    0042         LD      A,0
                    0043         ADC     (HL)
                    0044         LD      (HL),A    ;SUM AND STORE TOP 8 BITS
                    0045         INC     L
                    0046         MEND
                    0047 ;
                    0048 ;*********************************************
                    0049 ; THIS SECTION PERFORMS THE INJECT SEQUENCE
                    0050 ; TIMING, AND CALLS THE "BLOCK" SUBROUTINE
                    0051 ; TO READ THE BACKGROUND AND SIGNAL
                    0052 ;*********************************************
                    0053 ;
0800  C31908        0054 START:  JP      INIT
0803  C32308        0055         JP      INIT2
0806  C32F08        0056         JP      CID
0809  C3E609        0057         JP      MOVE
```

PRECEDING PAGE BLANK NOT FILMED

```
080C  C3EF09          0058           JP      CLEAR
080F  C3FC09          0059           JP      PICT
0812  C33E0A          0060           JP      COPY
0815  C3470A          0061           JP      SUBBKG
0818  C9              0062           RET
0819  0610            0063 INIT:     LD      B,16     ;INITIALIZE ROW
081B  0E2B            0064           LD      C,43     ;INITIALIZE COLUMN
081D  114000          0065           LD      DE,64    ;INITIALIZE NO. OF SUMS
0820  C32F08          0066           JP      CID
0823  3A4123          0067 INIT2:    LD      A,(ROW) ;INITIALIZE ROW
0826  47              0068           LD      B,A
0827  3A4023          0069           LD      A,(COL) ;INITIALIZE COLUMN
082A  4F              0070           LD      C,A
082B  3A4223          0071           LD      A,(NSUM);INITIALIZE NO. OF SUMS
082E  5F              0072           LD      E,A
082F  7B              0073 CID:      LD      A,E
0830  324223          0074           LD      (NSUM),A
0833  3E01            0075           LD      A,1
0835  D304            0076           OUT     LED,A    ;LIGHT GREEN LED
0837  3E47            0077 C0:       LD      A,47H    ;REST,RVG,CVG,IG ON
0839  D325            0078           OUT     25H,A
083B  3E67            0079           LD      A,67H    ;CVD ON
083D  D325            0080           OUT     25H,A
083F  3E77            0081           LD      A,77H    ;RVD ON
0841  D325            0082           OUT     25H,A
0843  113200          0083           LD      DE,50
0846  CDDF09          0084           CALL    DELAY
0849  3E67            0085           LD      A,67H    ;RVD OFF
084B  D325            0086           OUT     25H,A
084D  3E47            0087           LD      A,47H    ;CVD OFF
084F  D325            0088           OUT     25H,A
0851  110500          0089           LD      DE,5
0854  CDDF09          0090           CALL    DELAY
0857  212F23          0091           LD      HL,BASE+47
085A  3EFF            0092           LD      A,0FFH
085C  77              0093 C1:       LD      (HL),A   ,CLEAR TEMPORARY MEMORY
085D  2D              0094           DEC     L
085E  F23C08          0095           JP      P,C1
0861  CD8408          0096           CALL    BLOCK    ;READ BACKGROUND
0864  212F23          0097           LD      HL,BASE+47
0867  7E              0098 C2:       LD      A,(HL)   ;NEGATE BKG IN TEMP MEMORY
0868  2F              0099           CPL
0869  77              0100           LD      (HL),A
086A  2D              0101           DEC     L
086B  F26708          0102           JP      P,C2
086E  CD8408          0103 C3:       CALL    BLOCK    ;READ SIGNAL
0871  3E02            0104           LD      A,2      ;LIGHT RED LED
0873  D304            0105           OUT     LED,A
0875  DB04            0106           IN      A,LED    ;CHECK SWITCHES
0877  E603            0107           AND     3
0879  C23708          0108           JP      NZ,C0    ;REPEAT SEQUENCE?
087C  3E67            0109           LD      A,67H    ;CVD ON, RVD OFF (IDLE)
087E  D325            0110           OUT     25H,A
0880  AF              0111           XOR     A,A      ;TURN OFF LED'S
0881  D304            0112           OUT     LED,A
0883  C9              0113           RET
                      0114 ;
```

ORIGINAL PAGE IS
OF POOR QUALITY


```
                        0115 ;*****************************************
                        0116 ; THIS SECTION RUNS THE PHASE LINES TO CHOOSE
                        0117 ; THE PIXEL SPECIFIED BY THE B,C REGISTERS,
                        0118 ; CALLS THE "READ" SUBROUTINE TO READ EACH
                        0119 ; COLUMN 64 TIMES, AND RUNS THE PHASE LINES
                        0120 ; TO CLEAR BOTH SCANNERS
                        0121 ;*****************************************
                        0122 ;
0884  CD7509              0123 BLOCK:  CALL    PHASIN   ;RUN REGISTERS TO CHOOSE BLOCK
0887  3E44                0124         LD      A,44H    ;REST,IG ON; CVG,RVG OFF
0889  D325                0125         OUT     25H,A
088B  C5                  0126         PUSH    BC
088C  210023              0127         LD      HL,BASE
088F  011000              0128         LD      BC,10H   ;READ COLUMN 1
0892  CDBA08              0129         CALL    READ
0895  012000              0130         LD      BC,20H   ;READ COLUMN 2
0898  CDBA08              0131         CALL    READ
089B  014000              0132         LD      BC,40H   ;READ COLUMN 3
089E  CDBA08              0133         CALL    READ
08A1  018000              0134         LD      BC,80H   ;READ COLUMN 4
08A4  CDBA08              0135         CALL    READ
08A7  C1                  0136         POP     BC
08A8  3E47                0137         LD      A,47H    ;REST,IG,RVG,CVG ON
08AA  D325                0138         OUT     25H,A
08AC  1642                0139         LD      D,66
08AE  3E0A                0140         LD      A,0AH
08B0  210A05              0141         LD      HL,050AH
08B3  CDC909              0142         CALL    PHASE    ;RUN OUT BOTH REGISTERS
08B6  AF                  0143         XOR     A        ;TURN OFF BOTH PHASES
08B7  D326                0144         OUT     26H,A
08B9  C9                  0145         RET
                        0146 ;
                        0147 ;*************************************
                        0148 ; THIS SECTION READS THE 4 ROWS BY
                        0149 ; 1 COLUMN, SUMS EACH PIXEL 64 TIMES,
                        0150 ; AND STORES THE 4 18-BIT SUMS IN RAM
                        0151 ; LOCATIONS 2300-232FH
                        0152 ;*************************************
                        0153 ;
08BA  1602                0154 READ:   LD      D,2      ;USE D AS A COUNTDOWN
08BC  78                  0155 R1:     LD      A,B      ;TURN E LINES OFF
08BD  D324                0156         OUT     24H,A
08BF  3E05                0157         LD      A,5
08C1  3D                  0158 D1:     DEC     A        ;DELAY
08C2  C2C108              0159         JP      NZ,D1
08C5  3E04                0160         LD      A,04H    ;IG ON; RESTORE OFF
08C7  D325                0161         OUT     25H,A
08C9  3E00                0162         LD      A,00H    ;IG OFF
08CB  D325                0163         OUT     25H,A
08CD  3E40                0164         LD      A,40H    ;RESTORE ON
08CF  D325                0165         OUT     25H,A
08D1  3E21                0166         LD      A,0FH
08D3  3D                  0167 D2:     DEC     A        ;DELAY
08D4  C2D308              0168         JP      NZ,D2
08D7  AF                  0169         XOR     A        ;REST OFF
08D8  D325                0170         OUT     25H,A
08DA  79                  0171         LD      A,C      ;DRIVE E LINE
```

ORIGINAL PAGE IS OF POOR QUALITY

```
08DB  D324          0172          OUT     24H,A    ;AND GET CHANNEL 0
08DD  3E11          0173          LD      A,0DH
08DF  3D            0174 D3:      DEC     A        ;DELAY
08E0  C2DF08        0175          JP      NZ,D3
08E3  15            0176          DEC     D
08E4  C2BC08        0177          JP      NZ,R1    ;DONE STARTUP YET?
08E7  3A4223        0178          LD      A,(NSUM);LOAD NUMBER OF SUMS
08EA  57            0179          LD      D,A
08EB  E5            0180 R2:      PUSH    HL
08EC  3E80          0181          LD      A,80H    ;SAMPLE
08EE  D325          0182          OUT     25H,A
08F0  3E00          0183          LD      A,0      ;DELAY
08F2  3E00          0184          LD      A,0
08F4  3E00          0185          LD      A,0
08F6  D325          0186          OUT     25H,A    ;HOLD
08F8  D328          0187          OUT     STROBE,A;START A/D CONVERSION
08FA  D324          0188          OUT     24H,A    ;TURN E LINE OFF
08FC  3E04          0189          LD      A,04H    ;IG ON; RESTORE OFF
08FE  D325          0190          OUT     25H,A
0900  3E00          0191          LD      A,00H    ;IG OFF
0902  D325          0192          OUT     25H,A
0904  3E40          0193          LD      A,40H    ;RESTORE ON
0906  D325          0194          OUT     25H,A
0908  78            0195          LD      A,B
0909  F601          0196          OR      1        ;GET CHANNEL 1
090B  D324          0197          OUT     24H,A
090D                0198          GETDATA          ;SUM AND STORE DATA
090D  DB20          0199+         IN      A,20H    ;GET LOWER 8 BITS OF DATA
090F  86            0200+         ADD     (HL)
0910  77            0201+         LD      (HL),A   ;SUM AND STORE LOW 8 BITS
0911  2C            0202+         INC     L
0912  DB21          0203+         IN      A,21H    ;GET UPPER 4 BITS OF DATA
0914  D328          0204+         OUT     STROBE,A;START NEXT CONVERSION
0916  8E            0205+         ADC     (HL)
0917  77            0206+         LD      (HL),A   ;SUM AND STORE MID 8 BITS
0918  2C            0207+         INC     L
0919  3E00          0208+         LD      A,0
091B  8E            0209+         ADC     (HL)
091C  77            0210+         LD      (HL),A   ;SUM AND STORE TOP 8 BITS
091D  2C            0211+         INC     L
091E  78            0212          LD      A,B
091F  F602          0213          OR      2        ;GET CHANNEL 2
0921  D324          0214          OUT     24H,A
0923                0215          GETDATA          ;SUM AND STORE DATA
0923  DB20          0216+         IN      A,20H    ;GET LOWER 8 BITS OF DATA
0925  86            0217+         ADD     (HL)
0926  77            0218+         LD      (HL),A   ;SUM AND STORE LOW 8 BITS
0927  2C            0219+         INC     L
0928  DB21          0220+         IN      A,21H    ;GET UPPER 4 BITS OF DATA
092A  D328          0221+         OUT     STROBE,A;START NEXT CONVERSION
092C  8E            0222+         ADC     (HL)
092D  77            0223+         LD      (HL),A   ;SUM AND STORE MID 8 BITS
092E  2C            0224+         INC     L
092F  3E00          0225+         LD      A,0
0931  8E            0226+         ADC     (HL)
0932  77            0227+         LD      (HL),A   ;SUM AND STORE TOP 8 BITS
0933  2C            0228+         INC     L
```

ORIGINAL PAGE IS
OF POOR QUALITY

```
0934  AF          0229          XOR     A,A
0935  D325        0230          OUT     25H,A     ;RESTORE OFF
0937  79          0231          LD      A,C       ;DRIVE E LINES
0938  F603        0232          OR      3         ;GET CHANNEL 3
093A  D324        0233          OUT     24H,A
093C              0234          GETDATA           ;SUM AND STORE DATA
093C  DB20        0235+         IN      A,20H     ;GET LOWER 8 BITS OF DATA
093E  86          0236+         ADD     (HL)
093F  77          0237+         LD      (HL),A    ;SUM AND STORE LOW 8 BITS
0940  2C          0238+         INC     L
0941  DB21        0239+         IN      A,21H     ;GET UPPER 4 BITS OF DATA
0943  D328        0240+         OUT     STROBE,A;START NEXT CONVERSION
0945  8E          0241+         ADC     (HL)
0946  77          0242+         LD      (HL),A    ;SUM AND STORE MID 8 BITS
0947  2C          0243+         INC     L
0948  3E00        0244+         LD      A,0
094A  8E          0245+         ADC     (HL)
094B  77          0246+         LD      (HL),A    ;SUM AND STORE TOP 8 BITS
094C  2C          0247+         INC     L
094D  79          0248          LD      A,C
094E  F600        0249          OR      0         ;GET CHANNEL 0
0950  D324        0250          OUT     24H,A
0952              0251          GETDATA           ;SUM AND STORE DATA
0952  DB20        0252+         IN      A,20H     ;GET LOWER 8 BITS OF DATA
0954  86          0253+         ADD     (HL)
0955  77          0254+         LD      (HL),A    ;SUM AND STORE LOW 8 BITS
0956  2C          0255+         INC     L
0957  DB21        0256+         IN      A,21H     ;GET UPPER 4 BITS OF DATA
0959  D328        0257+         OUT     STROBE,A;START NEXT CONVERSION
095B  8E          0258+         ADC     (HL)
095C  77          0259+         LD      (HL),A    ;SUM AND STORE MID 8 BITS
095D  2C          0260+         INC     L
095E  3E00        0261+         LD      A,0
0960  8E          0262+         ADC     (HL)
0961  77          0263+         LD      (HL),A    ;SUM AND STORE TOP 8 BITS
0962  2C          0264+         INC     L
0963  E1          0265          POP     HL
0964  15          0266          DEC     D
0965  C2EB08      0267          JP      NZ,R2     ;DONE ALL SUMS YET?
0968  3E00        0268          LD      A,0       ;TURN OFF E LINES
096A  D324        0269          OUT     24H,A
096C  3E47        0270          LD      A,47H     ;RESTORE,RVG,CVG,IG ON
096E  D325        0271          OUT     25H,A
0970  010C00      0272          LD      BC,12
0973  09          0273          ADD     HL,BC
0974  C9          0274          RET
                  0275 ;
                  0276 ;************************************
                  0277 ; THIS SECTION RUNS THE PHASE LINES
                  0278 ; TO ADDRESS THE CHOSEN PIXEL
                  0279 ;************************************
                  0280 ;
0975  C5          0281 PHASIN:  PUSH    BC        ;SAVE PIXEL ADDRESS
0976  1E00        0282          LD      E,0
0978  04          0283          INC     B         ;WORK ON ROW ADDRESS
0979  CB38        0284          SRL     B
097B  04          0285          INC     B
```

ORIGINAL PAGE IS OF POOR QUALITY

```
097C  CB38        0286          SRL     B
097E  D28609      0287          JP      NC,F1     ;CHECK UP/DOWN
0981  CBF3        0288          SET     6,E       ;SET TO UP
0983  C38B09      0289          JP      F2
0986  CBB3        0290 F1:      RES     6,E       ;SET TO DOWN
0988  C38B09      0291          JP      F2
098B  0C          0292 F2:      INC     C         ;WORK ON COLUMN ADDRESS
098C  CB39        0293          SRL     C
098E  0C          0294          INC     C
098F  CB39        0295          SRL     C
0991  D29909      0296          JP      NC,F3     ;CHECK LEFT/RIGHT
0994  CBFB        0297          SET     7,E       ;SET TO LEFT
0996  C39E09      0298          JP      F4
0999  CBBB        0299 F3:      RES     7,E       ;SET TO RIGHT
099B  C39E09      0300          JP      F4
099E  3E82        0301 F4:      LD      A,130
09A0  90          0302          SUB     B
09A1  91          0303          SUB     C
09A2  57          0304          LD      D,A
09A3  AF          0305          XOR     A
09A4  210000      0306          LD      HL,0      ;RUN NEITHER PHASE LINE
09A7  CDC909      0307          CALL    PHASE     ;(TO BALANCE TIMING)
09AA  3E35        0308          LD      A,35H     ;VIN,HIN,P1V,P1H ON
09AC  D326        0309          OUT     26H,A
09AE  3E30        0310          LD      A,30H     ;VIN,HIN ON; P1V,P1H OFF
09B0  D326        0311          OUT     26H,A
09B2  50          0312          LD      D,B
09B3  3E01        0313          LD      A,01H
09B5  210102      0314          LD      HL,0201H;RUN VERTICAL REGISTER
09B8  CDC909      0315          CALL    PHASE     ;TO CHOOSE ROW BLOCK
09BB  51          0316          LD      D,C
09BC  F604        0317          OR      04H
09BE  210408      0318          LD      HL,0804H;RUN HORIZONTAL REGISTER
09C1  CDC909      0319          CALL    PHASE     ;TO CHOOSE COLUMN BLOCK
09C4  C1          0320          POP     BC        ;BRING BACK BLOCK ADDRESS
09C5  B3          0321          OR      E         ;CHOOSE U/D AND L/R
09C6  D326        0322          OUT     26H,A
09C8  C9          0323          RET
                  0324 ;
                  0325 ;*****************************
                  0326 ; THIS SECTION PERFORMS THE
                  0327 ; TIMING OF THE PHASE LINES
                  0328 ;*****************************
                  0329 ;
09C9  AD          0330 PHASE:   XOR     L         ;PHASE LINE SUBROUTINE
09CA  D326        0331          OUT     26H,A     ;PHASE 2 ON
09CC  AC          0332          XOR     H
09CD  D326        0333          OUT     26H,A     ;PHASE 2 OFF
09CF  15          0334          DEC     D         ;DONE YET?
09D0  C2D409      0335          JP      NZ,PH1
09D3  C9          0336          RET
09D4  AC          0337 PH1:     XOR     H
09D5  D326        0338          OUT     26H,A     ;PHASE 1 ON
09D7  AD          0339          XOR     L
09D8  D326        0340          OUT     26H,A     ;PHASE 1 OFF
09DA  15          0341          DEC     D         ;DONE YET?
09DB  C2C909      0342          JP      NZ,PHASE
```

ORIGINAL PAGE IS
OF POOR QUALITY

```
09DE  C9          0343          RET
                  0344 ;
                  0345 ;*************************************
                  0346 ; THIS SUBROUTINE PERFORMS A DELAY
                  0347 ; OF ABOUT 4 MICROSECONDS PER LOOP
                  0348 ;*************************************
                  0349 ;
09DF  1B          0350 DELAY:   DEC     DE
09E0  7B          0351          LD      A,E
09E1  B2          0352          OR      D
09E2  C2DF09      0353          JP      NZ,DELAY
09E5  C9          0354          RET
                  0355 ;
                  0356 ;*************************************
                  0357 ; THIS ROUTINE MOVES THE DATA FROM
                  0358 ; TEMPORARY STORAGE TO A PERMANENT
                  0359 ; STORAGE LOCATION SPECIFIED BY THE
                  0360 ; DE REGISTERS
                  0361 ;*************************************
                  0362 ;
09E6  210023      0363 MOVE:    LD      HL,2300H
09E9  013000      0364          LD      BC,48
09EC  EDB0        0365          LDIR
09EE  C9          0366          RET
                  0367 ;
                  0368 ;*************************************
                  0369 ; THIS ROUTINE CLEARS THE CONTENTS
                  0370 ; OF MEMORY STARTING AT DE AND
                  0371 ; PROCEEDING TO BC+DE
                  0372 ;*************************************
                  0373 ;
09EF  62          0374 CLEAR:   LD      H,D
09F0  6B          0375          LD      L,E
09F1  1600        0376          LD      D,0
09F3  72          0377 CL1:     LD      (HL),D
09F4  23          0378          INC     HL
09F5  0B          0379          DEC     BC
09F6  79          0380          LD      A,C
09F7  B0          0381          OR      B
09F8  C2F309      0382          JP      NZ,CL1
09FB  C9          0383          RET
                  0384 ;
                  0385 ;*************************************************
                  0386 ; THIS ROUTINE TAKES THE DATA FROM TEMPORARY
                  0387 ; STORAGE, PICKS OUT THE 8 BITS/PIXEL TO BE
                  0388 ; DISPLAYED (SPECIFIED BY BC), AND STORES
                  0389 ; THEM IN MEMORY (SPECIFIED BY HL) FOR
                  0390 ; PICTURE DISPLAY
                  0391 ;*************************************************
                  0392 ;
09FC  210023      0393 PICT:    LD      HL,2300H
09FF  78          0394          LD      A,B       ;LOAD LSB CHOICE
0A00  FE09        0395          CP      9         ;GREATER THAN EIGHT BIT SHIFT?
0A02  DA080A      0396          JP      C,P1
0A05  23          0397          INC     HL        ;IF SO SHIFT ONE BYTE
0A06  D608        0398          SUB     8
0A08  2F          0399 P1:      CPL
```

ORIGINAL PAGE IS OF POOR QUALITY

```
0A09  D6F7        0400          SUB     247     ;8 MINUS LSB CHOICE
0A0B  47          0401          LD      B,A     ;SAVE NUMBER OF SHIFTS
0A0C  E5          0402 P2:      PUSH    HL
0A0D  D5          0403 P3:      PUSH    DE      ;SAVE PICTURE STORAGE ADDRESS
0A0E  5E          0404          LD      E,(HL)  ;PULL DATA OUT OF TEMP STORAGE
0A0F  23          0405          INC     HL      ;AND STORE IT IN DE REGISTERS
0A10  56          0406          LD      D,(HL)
0A11  78          0407          LD      A,B     ;BRING BACK NO. OF SHIFTS
0A12  B7          0408          OR      A
0A13  CA1D0A      0409          JP      Z,P5    ;IF NO SHIFTS, JUMP AHEAD
0A16  EB          0410          EX      DE,HL
0A17  29          0411 P4:      ADD     HL,HL   ;SHIFT RIGHT
0A18  3D          0412          DEC     A
0A19  C2170A      0413          JP      NZ,P4
0A1C  EB          0414          EX      DE,HL
0A1D  79          0415 P5:      LD      A,C     ;ADD ZERO LEVEL BIAS TO PICTURE
0A1E  82          0416          ADD     D
0A1F  D1          0417          POP     DE      ;BRING BACK PICT STORAGE ADDR
0A20  12          0418          LD      (DE),A  ;STORE PIXEL
0A21  13          0419          INC     DE      ;NEXT COLUMN DATA
0A22  7D          0420          LD      A,L
0A23  C60B        0421          ADD     11
0A25  6F          0422          LD      L,A
0A26  FE2F        0423          CP      47      ;DONE ALL 4 COLUMNS YET?
0A28  DA0D0A      0424          JP      C,P3
0A2B  E1          0425          POP     HL      ;NEXT ROW DATA
0A2C  23          0426          INC     HL
0A2D  23          0427          INC     HL
0A2E  23          0428          INC     HL
0A2F  7D          0429          LD      A,L
0A30  FE0C        0430          CP      12      ;DONE ALL FOUR ROWS YET?
0A32  D0          0431          RET     NC
0A33  3E7C        0432          LD      A,124   ;SET MEM ADDR FOR NEXT BLOCK
0A35  83          0433          ADD     E
0A36  5F          0434          LD      E,A
0A37  3E00        0435          LD      A,0
0A39  8A          0436          ADC     D
0A3A  57          0437          LD      D,A
0A3B  C30C0A      0438          JP      P2
                  0439 ;
                  0440 ;************************************
                  0441 ; THIS ROUTINE COPIES THE PICTURE
                  0442 ; FROM ONE LOCATION IN MEMORY
                  0443 ; INTO ANOTHER LOCATION
                  0444 ;************************************
                  0445 ;
0A3E  62          0446 COPY:    LD      H,D
0A3F  6B          0447          LD      L,E
0A40  7A          0448          LD      A,D
0A41  C640        0449          ADD     40H
0A43  57          0450          LD      D,A
0A44  EDB0        0451          LDIR
0A46  C9          0452          RET
                  0453 ;
                  0454 ;************************************
                  0455 ; THIS ROUTINE SUBTRACTS THE BACKGROUND
                  0456 ; PICTURE FROM THE MAIN PICTURE
```

ORIGINAL PAGE IS
OF POOR QUALITY

```
                        0457 ; REGISTERS DE CONTAIN THE START ADDRESS
                        0458 ; OF THE MAIN PICTURE, BC IS THE NUMBER OF
                        0459 ; PIXELS, THE BKG PICTURE IS OFFSET
                        0460 ; FROM THE MAIN PICTURE BY 4000H
                        0461 ;*********************************
                        0462 ;
0A47  62                0463 SUBBKG: LD      H,D
0A48  6B                0464         LD      L,E
0A49  7C                0465         LD      A,H
0A4A  C640              0466         ADD     40H
0A4C  67                0467         LD      H,A
0A4D  1A                0468 S1:     LD      A,(DE)
0A4E  96                0469         SUB     (HL)
0A4F  C620              0470         ADD     20H
0A51  12                0471         LD      (DE),A
0A52  23                0472         INC     HL
0A53  13                0473         INC     DE
0A54  0B                0474         DEC     BC
0A55  79                0475         LD      A,C
0A56  B0                0476         OR      B
0A57  C24D0A            0477         JP      NZ,S1
0A5A  C9                0478         RET


Errors                  0


end of assembly

A.
```

```
LIST 0-9999

' CID STAR 8/18/83
' DEFINT A-F:DEFDBL S-T
120 A=&H800
130 B=8
140 NS=4
150 A1=A+6:A2=A+9:A3=A+12:A4=A+15
155 DIM RM(3,3),RS(3,3)
160 PRINT
170 PRINT "CID STAR TRACKER"
190 INPUT "STORE PICTURE (1), TEMPORAL NOISE (2), TOTAL NOISE (3)";WP
200 ON WP GOTO 1000,2000,3000,5000,6000
210 GOTO 190
1000 INPUT "FIRST PIXEL: ROW,COLUMN (0-255,0-255)";FR,FC
1010 INPUT "LAST PIXEL";LR,LC
1020 IF (LC-FC)<128 THEN 1050
1030 PRINT "TOO MANY COLUMNS ( >128)"
1040 GOTO1000
1050 IF (LR-FR) <92 THEN 1090
1060 PRINT "TOO MANY ROWS ( >92)"
1070 GOTO1000
1090 INPUT "SPECIFY LSB LOCATION (0-10)";P1
1100 BP=B+256*P1
1130 CALL A3,&H9000,&H2F7F
1140 FOR I=0TO3
1150 CALL A1,NS,256*FR+FC
1160 NEXT
1170 FOR I=FR TO LR STEP 4
1180 M=&H9000+128*(I-FR)
1190 FOR J=FC TO LC STEP 4
1200 CALL A1,NS,256*I+J
1210 CALL A4,M,BP
1220 M=M+4
1230 NEXT:NEXT
1232 INPUT "HISTOGRAM (Y OR N)";R$
1234 IF R$><"Y"THEN 1248
1236 INPUT "NORMALIZATION FACTOR (1-255)";NF
1238 CALL &HF00,NF
1240 INPUT "RENORMALIZE (Y OR N)";R$
1242 IF R$="Y" THEN 1236
1248 INPUT "RETAKE PICTURE (Y OR N)";R$
1250 IF R$="Y" THEN 1130
1260 GOTO170
2000 INPUT "WHICH PIXEL: ROW,COLUMN (0-255,0-255)";FR,FC
2010 INPUT "OPERATING TEMPERATURE";T
2020 N=100
2030 FOR I=0TOC
2040 CALL A1,NS,256*FR+FC
2050 NEXT
2060 FOR I=0TON-1
2070 CALL A1,NS,256*FR+FC
2080 CALL A2,&H9200+40*I
2090 NEXT
2100 INPUT "RETAKE DATA (Y OR N)";R$
2110 IF R$="Y" THEN 2030
2120 GOSUB 4000
2130 INPUT "REPEAT (Y OR N)";R$
2140 IF R$="Y" THEN 2010
2150 GOTO 170
```

ORIGINAL PAGE IS
OF POOR QUALITY

PAGE 30 INTENTIONALLY BLANK

PRECEDING PAGE BLANK NOT FILMED

```
3000 INPUT "FIRST PIXEL: ROW,COLUMN (0-255,0-255)";FR,FC
3010 INPUT "LAST PIXEL";LR,LC
3020 N=(LC-FC+4)*(LR-FR+4)
3030 IF N<4081 THEN 3060
3040 PRINT "TOO MUCH DATA ( >3600 PIXELS )"
3050 GOTO3000
3060 INPUT "OPERATING TEMPERATURE";T
3070 FOR I=0TO3
3080 CALL A1,NS,256*FR+FC
3090 NEXT
3100 M=&H9200
3110 FOR I=FR TO LR STEP 4
3120 FOR J=FC TO LC STEP 4
3130 CALL A1,NS,256*I+J
3140 CALL A2,M
3150 M=M+48
3160 NEXT:NEXT
3170 INPUT "RETAKE DATA (Y OR N)";R$
3180 IF R$="Y" THEN 3070
3190 GOSUB 4000
3200 INPUT "REPEAT (Y OR N)";R$
3210 IF R$="Y" THEN 3060
3220 GOTO170
4000 PRINT
4010 ON WP GOTO 4020,4020,4040
4020 PRINT "TEMPORAL NOISE (T=";T;"C):"
4030 GOTO 4050
4040 PRINT "TOTAL NOISE (T=";T;"C):"
4050 PRINT
4060 M=&H9200
4070 N=100
4080 NN=N-1
4090 NM=NN*48
4100 SC=113.6/NS
4110 PRINT "MEAN (CARRIERS)"
4120 FOR L=0 TO 3
4130 FOR J=0 TO 3
4140 SM=0:SS=0
4150 M1=M+12*J+3*L
4160 M2=M1+NM
4170 FORMM=M1TOM2STEP48
4180 PX=DPEEK(MM)
4190 SM=SM+PX
4200 SS=SS+PX*PX
4210 NEXT
4220 RM(J,L)=SC*SM/N
4230 PRINT RM(J,L),
4240 SD=(SS-SM*SM/N)/NN
4250 RD(J,L)=SC*SQR(ABS(SD))
4260 NEXT:PRINT
4270 NEXT:PRINT
4280 PRINT "RMS NOISE (CARRIERS)"
4290 QM=0:QD=0
4300 FOR L=0 TO 3
4310 FOR J=0 TO 3
4320 QM=QM+RM(J,L)
4330 QD=QD+RD(J,L)
4340 PRINT RD(J,L),
4350 NEXT:PRINT
4360 NEXT:PRINT
```

ORIGINAL PAGE IS
OF POOR QUALITY

```
4370 PRINT "AVG MEAN","AVG NOISE"
4380 PRINT QM/16,QD/16
4390 PRINT
4400 RETURN
5000 A5=A+18
5010 B1=&H9200
5020 B2=&H2BFF
5030 CALL A5,B1,B2
5040 GOTO 190
6000 A6=A+21
6010 B1=&H9200
6020 B2=&H2BFF
6030 CALL A6,B1,B2
6040 GOTO 190
6050 END
OK
```

ORIGINAL PAGE IS
OF POOR QUALITY