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Annual Report

Grant No. NAG-1-349

DIGITAL CONTROL SYSTEM FOR SPACE STRUCTURAL DAMPERS

Submitted to:

National Aeronautics and Space Administration
Langley Research Center
Hampton, Virginia 23665

Attention: Dr. Garnett C. Horner
SDD, MS 230

Submitted by:

J. K. Haviland
Professor

Report No. UVA/528224/MAE85/102

July 1984

DEPARTMENT OF MECHANICAL AND AEROSPACE ENGINEERING

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ABSTRACT

This is an annual progress report on a study of digital control systems for space structural dampers, also referred to as "inertia" or "proof-mass" dampers. Under work performed to date, a recently developed concept for a damper has been improved by adding a small taper to the proof-mass, and using a proximeter to determine position. Also, an experimental damper has been built using a three-inch stroke in place of the standard one-inch stroke. Initially, an analog controller was used to drive the damper, this has now been replaced by an independent digital controller slaved to a TRS-80 Model I computer, which also serves as a highly effective, low-cost development system. Since numerical analyses of the system have indicated a resonance of the proof-mass, leading to "striking" of the stops, provisions have been made for a relative velocity feedback. In one approach, the digital controller has been modified to accept the signal from a linear velocity transducer. In the other, the velocity feedback is included in the digital program. An overall system concept for the use of proof-mass dampers is presented.

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SECTION I

INTRODUCTION

Discussion

The work covered in this report originated with a study of large space structure damping under NASA Grant No. NAG-1-137-1 (1). The work of Auburn and Margulies (2,3) was available at that time, as was the work by Miller (4) on a pivoted proof-mass actuator. The present design grew out of an attempt to design a more weight-effective proof-mass actuator, and much is owed to verbal communications with Dr. Garnett Horner, the NASA project monitor, and with Dr. William Hallauer of VPI&SU.

The present work was started under NASA Grant No. NAG-1-349, following Proposal No. MAE-NASA-2548-83 (5), and was briefly reported in January (6).

Mr. M. Mallette (7), a graduate student, has worked on control laws in parallel with the present work. Some of his results are presented here.

Active Damper Design

The active damper design which is the subject of the present study was originally proposed under NASA Grant No. NAG-1-137-1 (1). During the period of the latter grant, the prototype damper shown in Figure 1 was developed, and development of the analog control system shown in Figure 2 was initiated. Under a further purchase order from NASA, No. L-46164B, the damper was redesigned as in Figures 3 and 4. Twelve of these dampers were delivered to NASA.

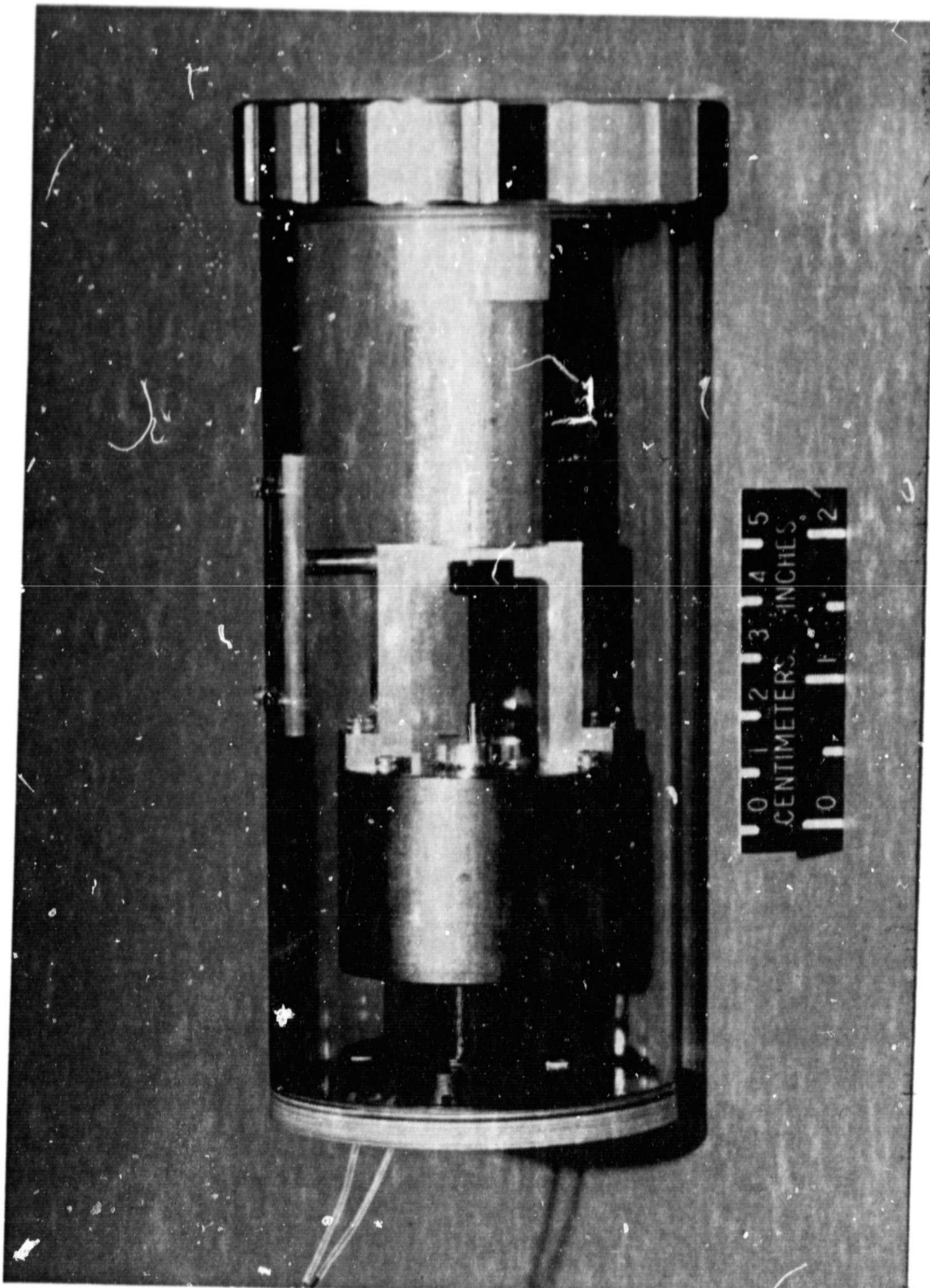


Figure 1. UVA Prototype Inertia Damper

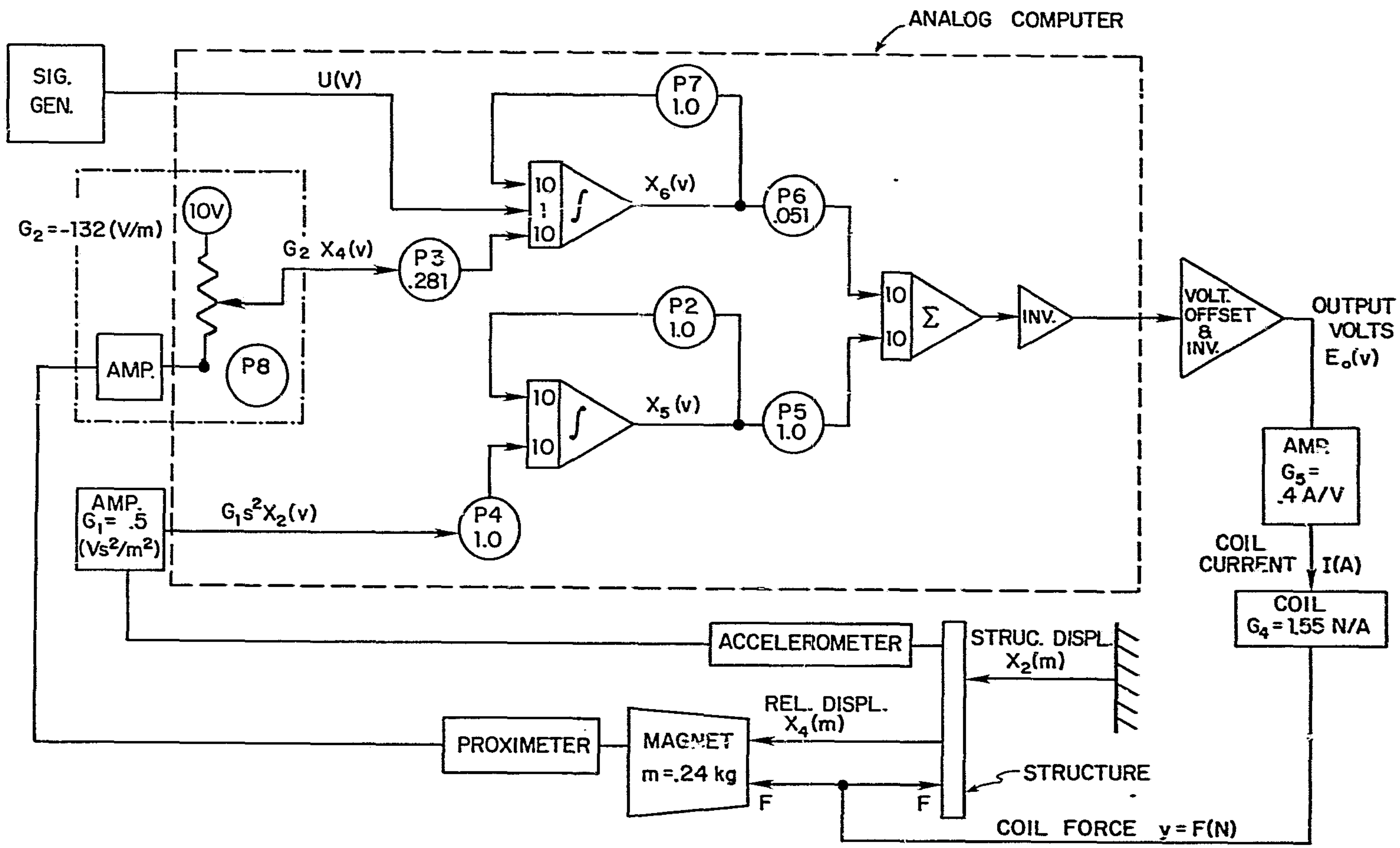
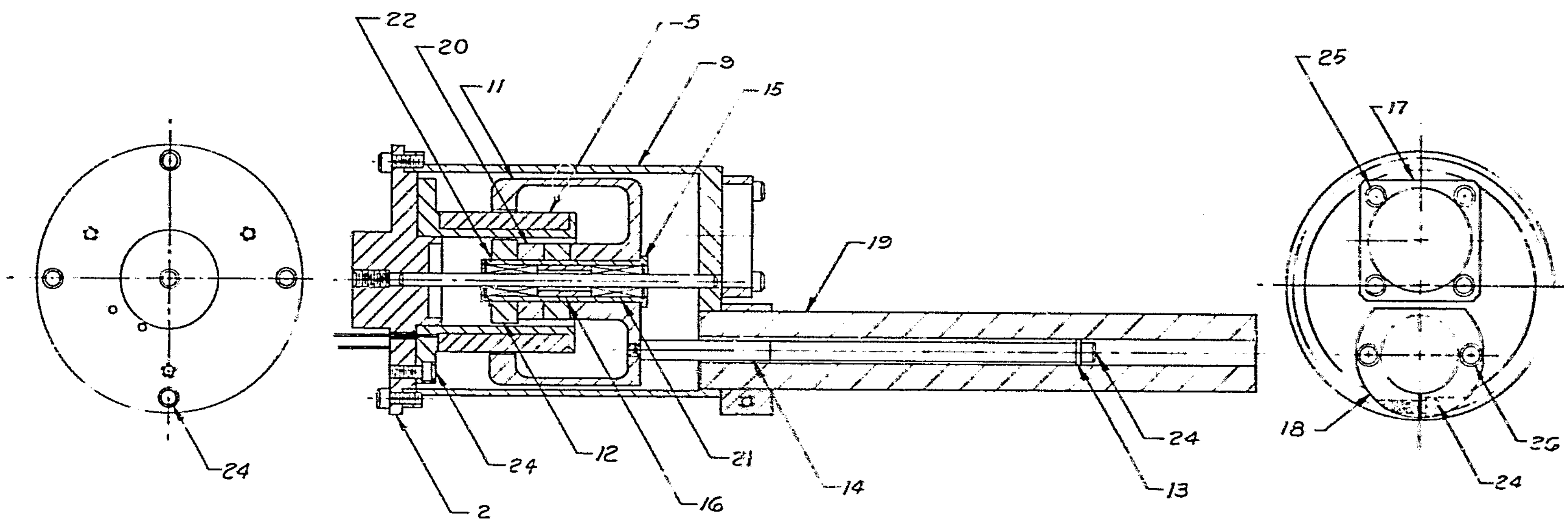


Figure 2. Analog Control System for Inertia Damper



FOR ITEM DESCRIPTION SEE PARTS LIST

ACTIVE DAMPER
ASSEMBLY
12-28-82
J.H.D.

Figure 3. Section of Inertia Damper Supplied to NASA.

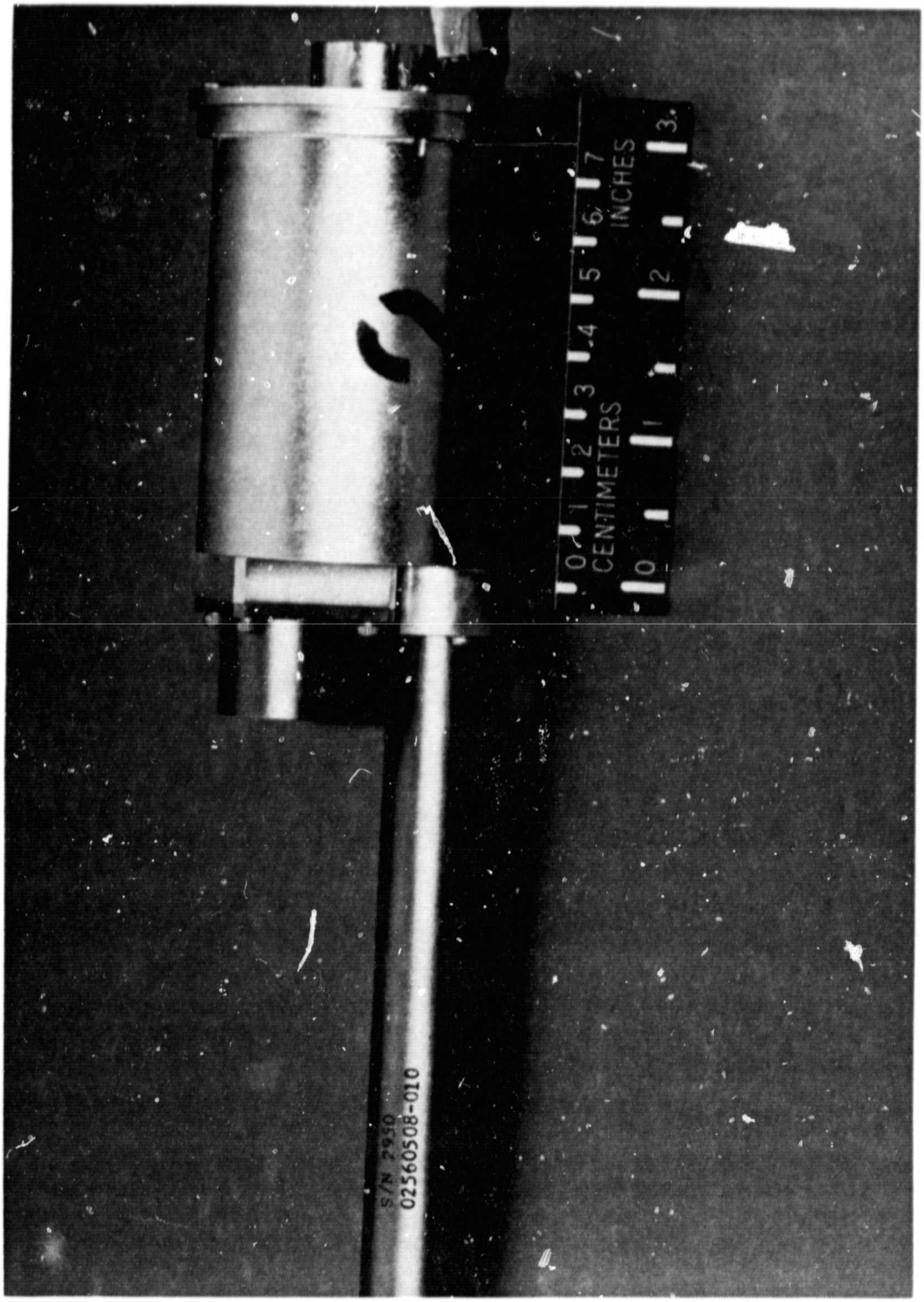


Figure 4. Inertia Damper Supplied to NASA

Under the current grant, NAG-1-349, a prototype digital control system has been developed, and a prototype elongated damper has been built having a three-inch stroke as contrasted with the one-inch stroke of the original. The approach to applications to large space structures is based on the assumption that each damper will have an individual microprocessor-driven control system whose gains can be reset by a central computer. Since it is anticipated that future space structures will experience growth during service, as new sections are added, less emphasis has been placed on optimization. It is now assumed that new dampers will be added as new structural sections are added, that these will be connected by bus to a central computer, and that adaptive control methods will be used in a central computer to change gains, or even control law programs, and to detect failures.

During this period, Mr. M. Mallette, a graduate student, has worked in parallel with the work reported here, under NASA Grant No. NGT-47-005-800.

The time of writing this report has coincided with considerable activity on the project, so that it will be outdated by the time that it is released. An arbitrary cutoff date of June 30, 1984, has been used; changes after this date are not reported.

SECTION II

DAMPER AND ANALOG CIRCUIT

Damper Design

Examples of one-inch and three-inch stroke dampers currently used in the laboratory are shown in Figures 5 and 6. Transparent covers permit their action to be observed at all times. The essential difference between these designs and the design of the dampers delivered to NASA is that the LVDT has been replaced by a proximeter. A small taper has been introduced on the proof-mass body so that its position can be determined by the proximeter.

Analog Control Circuit

The analog control circuit, as finally developed, is shown in Figure 2. Values shown for gains were selected during tests, with the actuator attached to a 15 ft. beam. Equations developed for this circuit are given in the next section; these feature the three transfer functions H_1, H_2 and H_3, which represent coil force due to inputs from the accelerometer, the proximeter, and a signal generator, respectively. The latter is used for testing the system.

A block diagram for the complete system is shown in Figure 7. From this, the equation for the overall closed-loop transfer function was developed. This can be expressed as H_c, the complex damping coefficient, which limits to the design damping coefficient c at high frequencies in most cases.

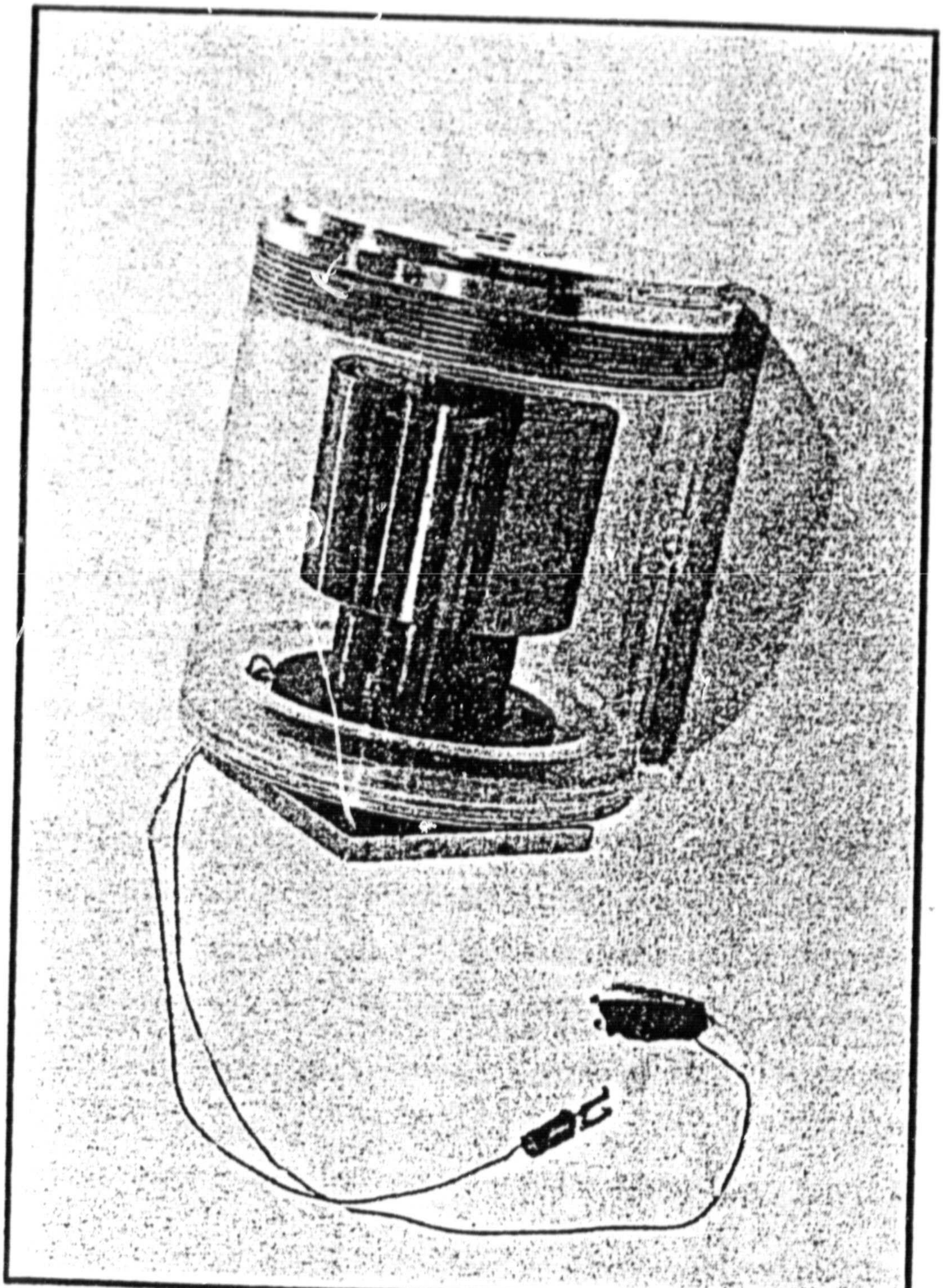


Figure 5. Modified Prototype Damper, One-Inch Stroke

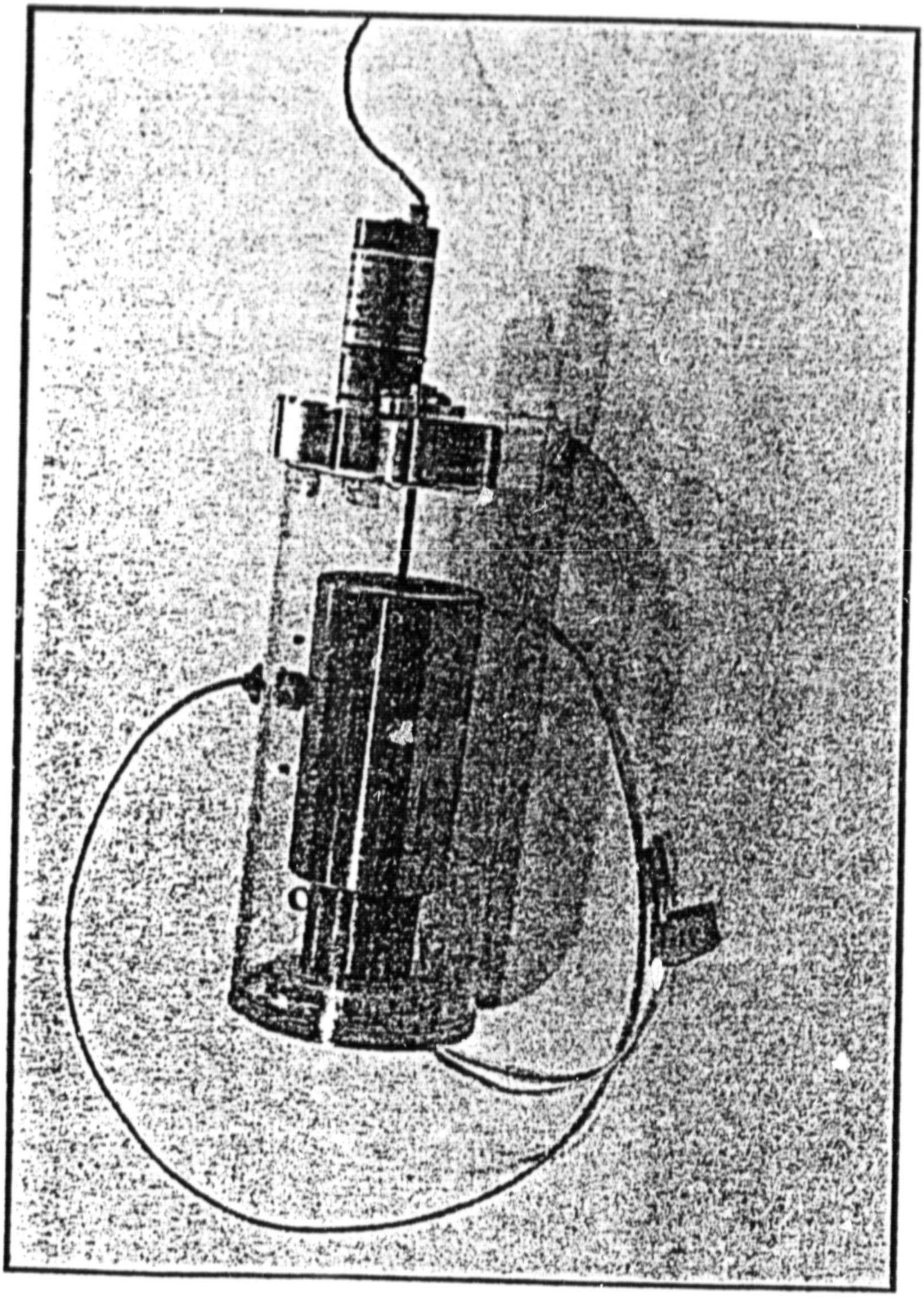


Figure 6. Three-Inch Damper Prototype

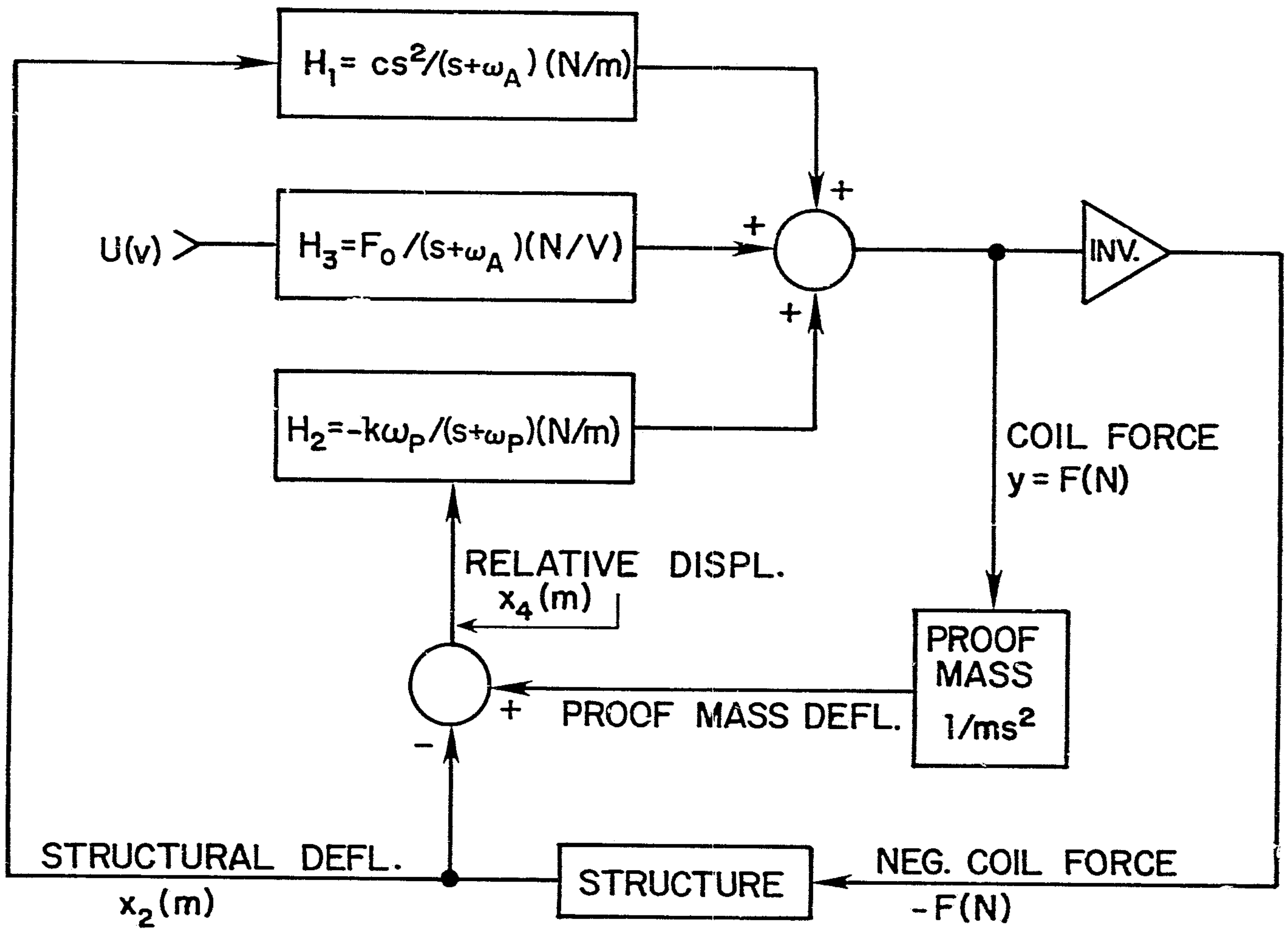


Figure 7. Block Diagram of Analog Circuit.

Analysis of Analog Circuit

Definitions:

x_1 = Structural velocity (m/s)

x_2 = Structural deflection (m)

x_3 = Proof-mass velocity (m/s)

x_4 = Proof-mass relative displacement (m)

x_5 = Integrator output (V)

x_6 = Integrator output (V)

E_o = Output volts (V)

I = Output current (A)

F = y = Coil force (N)

m = Proof mass (m)

G_1 = Gain of accelerometer (Vs^2/m)

G_2 = Gain of proximeter (V/m)

G_4 = Coil force for unit current (N/A)

G_5 = Gain of coil driver (A/V)

u = Input signal (V)

Equations:

$$F = y = H_1 x_2 + H_2 x_4 + H_3 u \qquad \text{(N)}$$

$$F/ms^2 = x_2 + x_4 \qquad \text{(m)}$$

$$H_1 = \frac{100 G_1 G_4 G_5 P_4 P_5 s^2}{s + 10\ P_2} = \frac{cs^2}{s + \omega_A} \qquad \text{(N/m)}$$

c = Design damping coefficient (Ns/m)

ω_A = Roll-off frequency for accelerometer (s^{-1})

$$H_2 = \frac{100G_2G_4G_5P_3P_6}{s + 10\ P_7} = \frac{-k\omega_P}{s + \omega_P} \quad (N/m)$$

k = Design stiffness (N/m)

ω_P = Roll-off frequency for proximeter (s^{-1})

$$H_3 = \frac{10\ G_4G_5P_6}{s + 10\ P_7} = \frac{F_o\omega_P}{s + \omega_P} \quad (N/V)$$

F_o = Coil Force for Unit Signal Generator Voltage (N/V)

Typical Values:

$G_1 = 0.5\ (Vs^2/m)$; $G_2 = -132\ (V/m)$

$G_4 = 0.4\ (V/A)$; $G_5 = 1.55\ (N/A)$

$H_1 = \dfrac{31s^2}{s + 10}\ (N/m)$; $C = 31\ (Ns/M)$

$\omega_A = 10(s^{-1})$

$H_2 = \dfrac{-117}{s + 10}\ (N/m)$; $K = 11.7\ (N/m)$

$\omega_P = 10(s^{-1})$

$H_3 = \dfrac{0.316}{s + 10}\ (N/V)$; $F_o = 0.0316\ (N/V)$

Derivation of H_c:

$$F = H_1x_2 + H_2x_4 + H_3u \quad (N)$$

$$F = ms^2(x_4 + x_2) \quad (N)$$

$$F = \frac{H_1 - H_2}{1-H_2/ms^2}\,x_2 + \frac{H_3}{1-H_2/ms^2}\,u = H_c s x_2 + H_u u \quad (N)$$

$$H_c = \frac{cs^3(s + \omega_P) + k\omega_P s(s + \omega_A)}{s^2(s + \omega_A)(s + \omega_P) + k\omega_P(s + \omega_A)/m} \quad (Ns/m)$$

= True damping coefficient

SECTION III

DIGITAL CONTROL CIRCUIT

Analog Part

The analog part of the digital control circuit is shown in Figure 8. The four input signals are:

1. The signal from a Sundstrand Model 305B servo accelerometer. This will eventually be replaced by a Model QA-900 accelerometer. Output is about 20 mV at one g.
2. The signal from a Hewlett-Packard Model 3311A signal generator. Any signal generator with a voltage offset could be used. This input is used to test the response of the system and to trim it by centering the mass.
3. The signal from a Bently-Nevada 3106-2800-190 amplifier derived from a Model 190 proximeter probe. This signal has a range of approximately -2V to -8V, depending on the probe adjustment. However, with the taper used on the moving mass, the double amplitude of the signal is about one Volt.
4. The signal from a Schaevitz VT-Z series linear velocity transducer. There are no provisions for attaching this to the laboratory damper of Figure 5. However, two of the NASA dampers of Figures 3 and 4 are being modified by adding tapered sleeves to the moving masses, and redesigning the cases to take proximeter probes. This will leave the present LVDT ports free for the attachment of the velocity transducers. Large signals with zero offset can be generated by these devices.

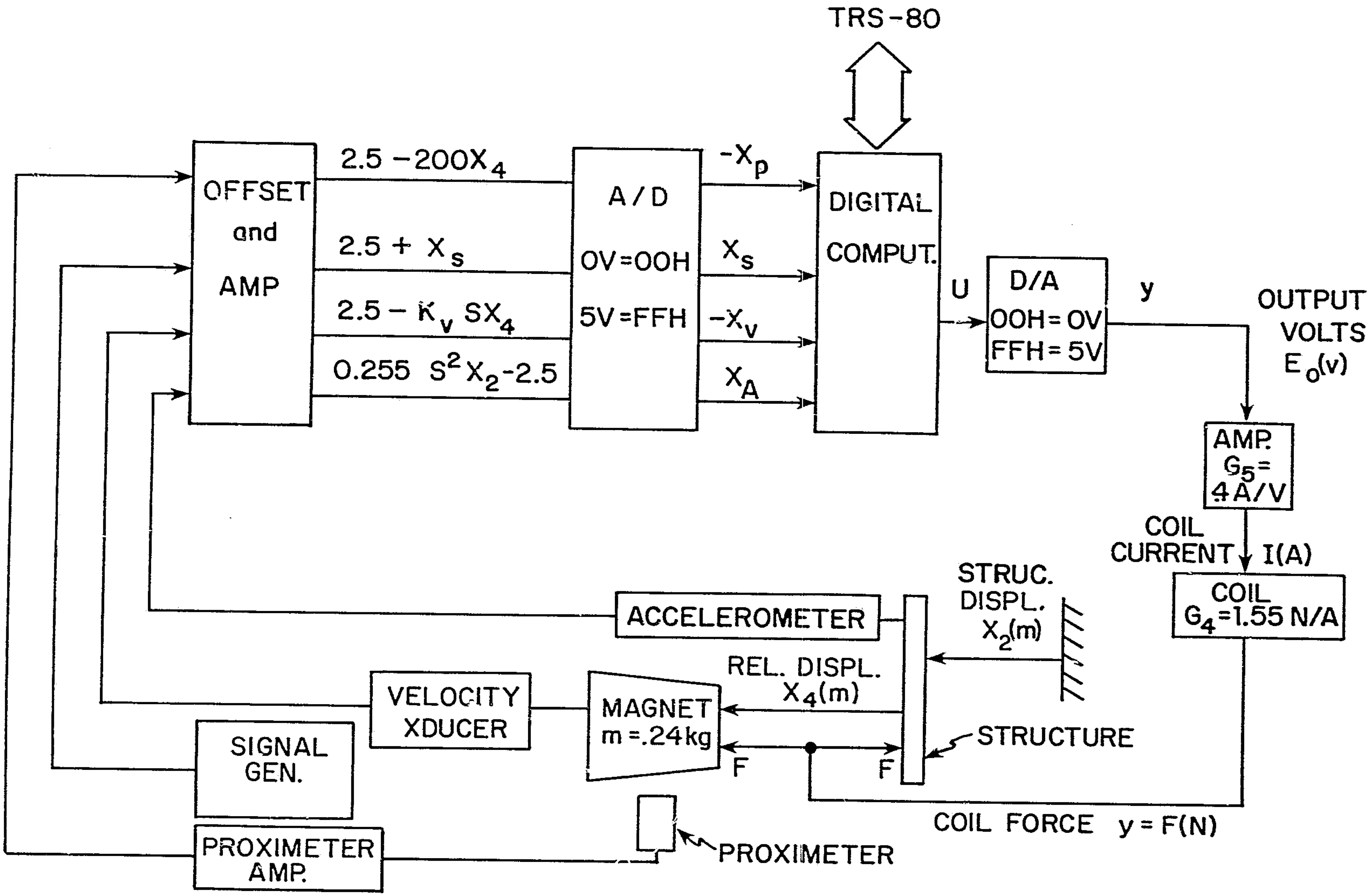


Figure 8. Digital Control System for Inertia Damper.

The offset and amplifier bank shown in Figure 8 consists of voltage followers and operational amplifiers. Output ports from this bank can be sampled with a voltmeter, and potentiometers can then be adjusted so that the full 0 - 5V range can be obtained with -1 to +1 g on the accelerometer, and with the full range of travel of the moving mass on the proximeter. No simple method has been devised for calibrating the velocity pickup, but this will be done when the necessary hardware is available.

The analog-to-digital converter shown in Figure 8 is presently a Datel DAS-952R 16-channel 8-bit monolithic data acquisition system. It has a convergence time of about 60 μsecs when a one MHz clock is used. This is adequate for present requirements, especially if "pipelining" is used in the digital control program.

The digital-to-analog converter system shown in Figure 8 is presently a Datel Model DAC-7523 8-bit monolithic multiplying converter, driven by an 8-bit latch, and in turn driving two operational amplifiers. It's overall range is 0-5 V, this is used to drive a current amplifier supplied by NASA, which delivers -1 to +1 amps to the coil.

The gains of the circuit elements external to the digital computer are shown in Figure 8, note that the D/A and A/D converters cancel each other. A positive input voltage, unless inverted in the digital program, tends to the accelerate the moving mass away from the structure (i.e., positive x_4), whereas the coil reaction acts in the opposite (i.e., negative x_2) direction.

An overall analysis of this system is given in the next section.

Overall Analysis of Analog Components

Assume

$$u = f\ \{x_A, x_P, x_S, x_V\} \qquad (V)$$

then coil force,

$$F = G_4G_5\ f\ \{0.255s_2, 200x_4, x_S, K_V s x_4\} \qquad (N)$$

where

$$G_5 = (2\ \text{Amps}) \div (5\ \text{volts}) = 0.4 \qquad (A/V)$$

and, based on NASA measurements, with a connection for 8 vs. 10 layers of winding:

$$G_4 = (8/10) \times (0.51\ \text{lb}) \times (4.45\ \text{N/lb}) \times (8.5\ \text{ohms}) \div (10V)$$

$$= 1.55 \qquad (N/A)$$

Note that, based on calculations assuming a perfect magnet,

$$G_4 = F/I = n\Phi \qquad (N/A)$$

where I = current, Amperes

n = # turns/meter

Φ = magnetic flux, Maxwells

given

$$\Phi = (0.8\ \text{Tesla}) \div (190 \times 10^{-6}\ m^2)$$

$$= 152 \qquad (\mu M)$$

$$n = (67\ \text{turns}) \times (8\ \text{layers}) \times (39.4\ \text{in/m}) \div (1.25\ \text{in.})$$

$$= 16{,}900 \qquad (m^{-1})$$

$$G_4 = 2.60 \qquad (N/A).$$

Thus, the measured value is about 60% of the ideal. This could possibly be improved with more attention to the design of the magnet. Using the experimental value,

$$F = f\ \{0.158s^2x_2, 124\ x_4, 0.62\ x_S, 0.62\ K_V s x_4\} \qquad (N)$$

Digital Computer

A logic diagram of the digital computer is shown in Figure 9. The Z80 module can be accessed directly from the TRS-80 through the control logic, which causes the responses shown in Table 1.

Table 1. Control Commands

ASSEMBLY LANGUAGE	BASIC LANGUAGE	RESULTS
OUT (40H),A	OUT 64,X[1]	BUSREQ held low (active)
OUT (48H),A	OUT 72,X	BUSREQ held high
OUT (50H),A	OUT 80,X	RESET pulsed low
OUT (58H),A	OUT 88,X	WAIT pulsed low
OUT (60H),A[2]	OUT 96,X[2]	INTERRUPT pulsed low
OUT (68H),A	OUT 104,X	NON-MASKABLE INTERRUPT pulsed low
OUT (70H),A	OUT 112,X	spare
OUT (78H),A	OUT 120,X	spare

Notes: (1) X is any BASIC variable or constant.

(2) Bits D3, D4, and D5 are placed on line when the Z80 responds to the interrupt.

When BUSREQ is held low, the Z80 responds by pulling BUSAK low, this enables the buffers to the TRS-80, and disconnects the Z80. The complete circuit can now be accessed from the TRS-80. When BUSREQ is held high, the Z80 controls the circuit. A RESET command now starts the Z80 from memory location 0, while an interrupt starts the Z80 from locations 0, 8, 10H, 18H, 20H, 28H, 30H, or 38H, according to the values of bits D3, D4, and D5.

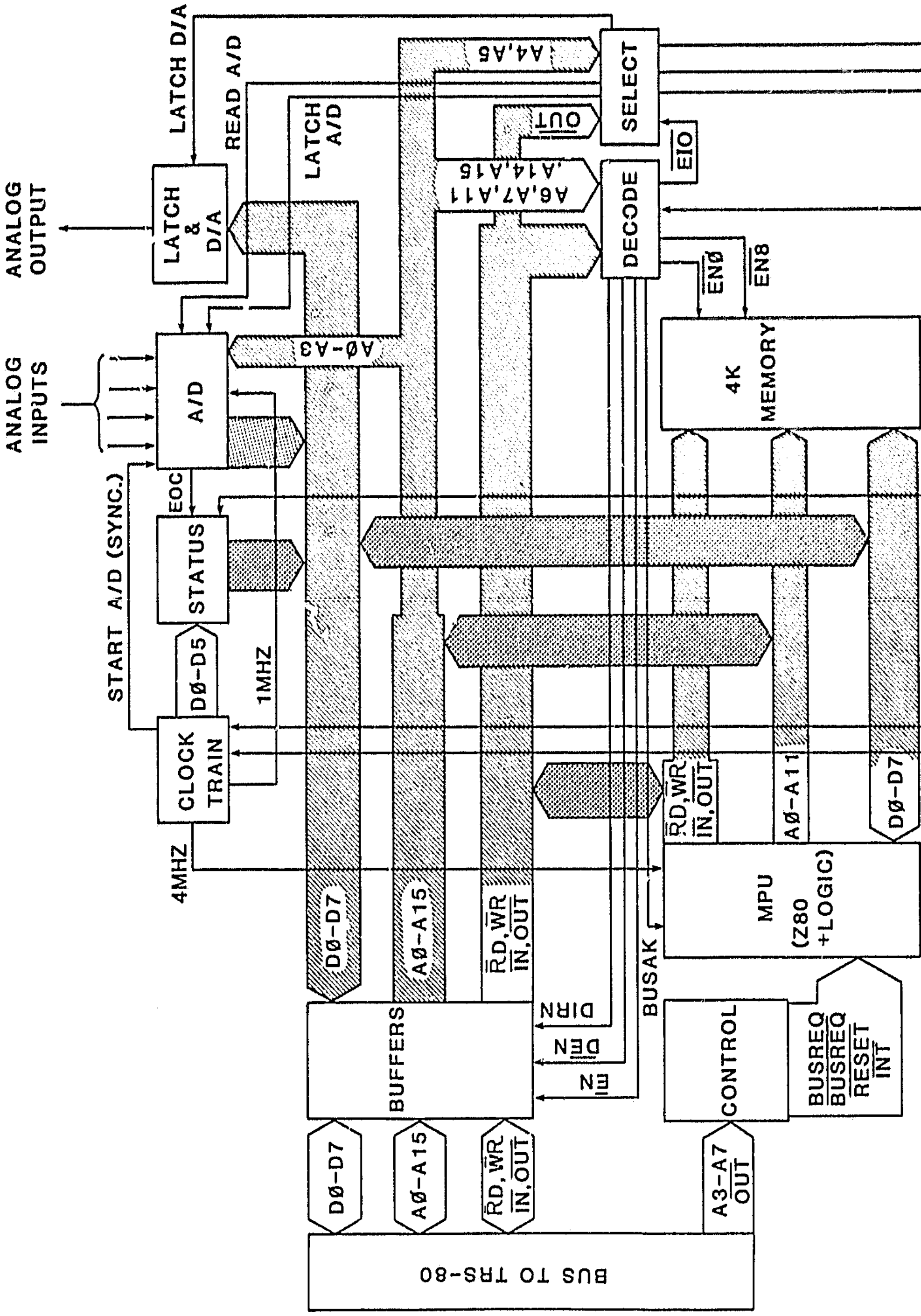


Figure 9. Digital Computer Schematic

Memory can either be 4K RAM or 2K RAM and 2K EPROM. This constitutes the complete memory range of the Z80 as installed, and is mapped fourfold into the TRS-80 from C000H to FFFFH. Foil must be cut in the expansion module of the TRS-80 to make this memory space available without line contention. In addition, 1K of INPUT or OUTPUT is available, both on the control board and in the TRS-80.

The logic module enables the input buffers, the memory, and the select module. The latter responds to INPUT or OUTPUT commands as shown in Table 2.

<u>TABLE 2. Select Commands</u>

ASSEMBLY LANGUAGE	BASIC LANGUAGE	RESULTS
OUT (0),A	-	Spare
OUT (10H),A	OUT 16,X	A (or X) sent to D/A
OUT (20H),A	OUT 32,X	X_A sent to A/D
OUT (21H),A	OUT 33,X	X_P sent to A/D
OUT (22H),A	OUT 34,X	X_S sent to A/D
OUT (23H),A	OUT 35,X	X_V sent to A/D
OUT (30H),A	-	Oscilloscope trigger
IN A,(0)	X = INP (0)	Status sent to A (or X)
IN A,(10H)	X = INP (16)	A/D reading sent to A (or X)
IN A,(20H)	-	Clock reset
IN A,(30H)	-	Spare

The clock is driven by a 4 MHz oscillator, with a divide chain down to 250 Hz, providing a 4 MHz signal to the Z80, a one-only START pulse to the A/D, a one MHz signal to the A/D, and six timing bits to the status module, ranging from 8 kHz to 250 Hz, as bits D0 to D5. It can be reset by IN A,(20H), as shown in Table 2. The EOC (end-of-convergence) signal from the A/D appears as bit D7 in the status module.

The D/A module includes an 8-bit latch enabled by the D/A OUT line, so that the D/A puts out a steady signal except during the 100 ns settling time. As mentioned earlier, the D/A is a Datel model DAC 7523.

Of the 16 input channels available, the Datel model DAS-952R A/D converter uses four in the present application.

SECTION IV

DIGITAL CONTROL PROGRAMS

Development Plan

The digital control program essentially completes the block marked "digital computer" in Figure 8. Since the system is not exactly a control system, with input and output, conventional design practices are not necessarily applicable, causing some difficulty in coming up with a suitable design.

Determination of a suitable control law has been the responsibility of a graduate student, Mr. Mallette. In order to compare results, it has been found convenient to evaluate two functions of frequency, the overall dimensionless damping, $Re\{h_c\}$, and the relative amplitude of the mass and of the structure, $|R_c|$. Further, it has been convenient to define a design damping factor, c, a design stiffness, k, a damping roll-off frequency, w_A (the subscript A is for accelerometer), a stiffness roll-off frequency, w_P (the subscript P is for proximeter), a mass damping, c_P, and a corresponding critical damping ratio ζ_P. All of these terms are discussed in the next section.

It is immediately obvious that the overall damping, h_c, should go to zero at zero frequency to limit the mass travel. Its magnitude at any frequency, together with the damping, c, is a direct measure of the performance of the damper, however, when $|R_c|$ becomes greater than unity, the structural amplitude must be restricted to less than the travel of the proof mass between its stops. It has, in fact, proved difficult to achieve large damping values without large resonances of the proof mass.

The practical result has been that, if the gain controlling damping is set high, the proof-mass strikes the stops when low-frequency or pendulum modes of the structure are excited.

Most of the circuits examined have been designed with a theoretical limit on h_c of unity as frequency goes to infinity. Of course, the digital computer limits the true high frequency response of the system.

<u>Definitions of Control Terms used in Digital Control</u>

Some of these terms are identical to those already defined under the description of the analog control circuit.

With X_4, $X_5 = 0$

Design Damping $= c = \lim_{s\to\infty} \frac{F}{sx_2}$ $\quad(\frac{Ns}{m})$

With X_2, $X_5 = 0$

Design Stiffness $= k = \lim_{s\to\infty} -\frac{F}{x_4}$ $\quad(\frac{N}{m})$

Mass Natural Frequency $= \omega_N = \sqrt{k/m}$ $\quad(s^{-1})$

Mass Damping $= c_p = \lim_{s\to 0} -\frac{F}{sx_4}$ $\quad(\frac{Ns}{m})$

Critical Damping Ratio $= \zeta_p = c_p/2\sqrt{mk}$

With X_4, $X_5 = 0$

Accelerometer Feedthrough $= H_1 = \frac{F}{x_2}$ $\quad(\frac{N}{m})$

With X_2, $X_5 = 0$

Proximeter Feedthrough $= H_2 = \frac{F}{x_4}$ $\quad(\frac{N}{m})$

With X_2, $X_4 = 0$

Signal Generator Feedthrough $= H_3 = \frac{F}{x_S}$ $\quad(\frac{N}{V})$

For overall system:

$$\text{Overall Damping} = H_c = \frac{F}{sx_2} \qquad (\frac{Ns}{m})$$

$$\text{Overall Dimensionless Damping} = h_c = \frac{H_c}{c}$$

$$\text{Relative Amplitude} = R_c = \frac{x_4}{x_2}$$

Note that, from the dynamics of the mass

$$F = ms^2(x_4 + x_2) \qquad (N)$$

hence $$R_c = \frac{H_c}{ms} - 1$$

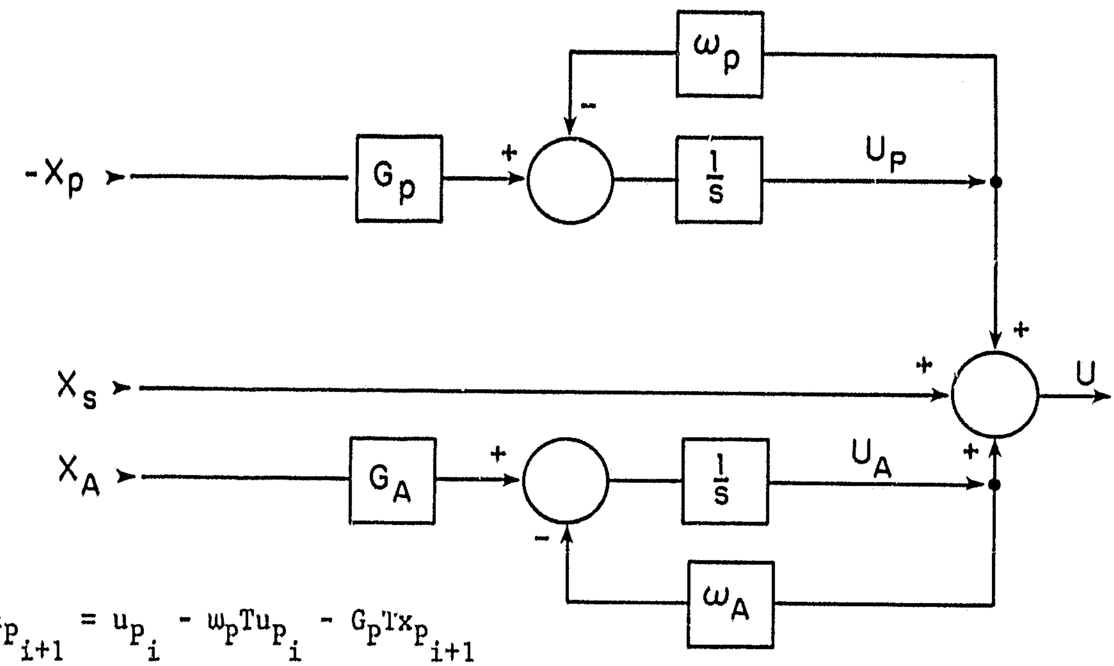
also $$sH_c = \frac{H_1 - H_2}{1 - H_2/ms^2} \qquad (Ns/m)$$

Control Laws

System diagrams for a number of control laws which have been considered are shown in Figures 10 to 17. In all cases, the digital equations, expressions for c, h, etc., and expressions for h_c are given. Z-transform notation has not been used because the sampling period is sufficiently small to permit the use of simple integration. Addition of 80H to input and output is necessary so that signed arithmetic can be used in the CPU. This has been omitted from the figures for clarity.

Evaluation of Control Laws

It will be noted that the P1 parallel realization is the same as the earlier analog control system, provided that corresponding gains are selected. The S1 and S2 series realizations of Figures 13 and 14 represent departures from the parallel to the series realization. Of the two series forms, the overall damping, h_c, for S2 limits to unity as s approaches infinity, as it does for P1, while it limits to zero for S1. Another variant is B1, a parallel system with direct feedback from the proximeter, and no roll-off as s increases.



$$u_{P_{i+1}} = u_{P_i} - \omega_P T u_{P_i} - G_P T x_{P_{i+1}}$$

$$u_{A_{i+1}} = u_{A_i} - \omega_A T u_{A_i} - G_A T x_{A_{i+1}}$$

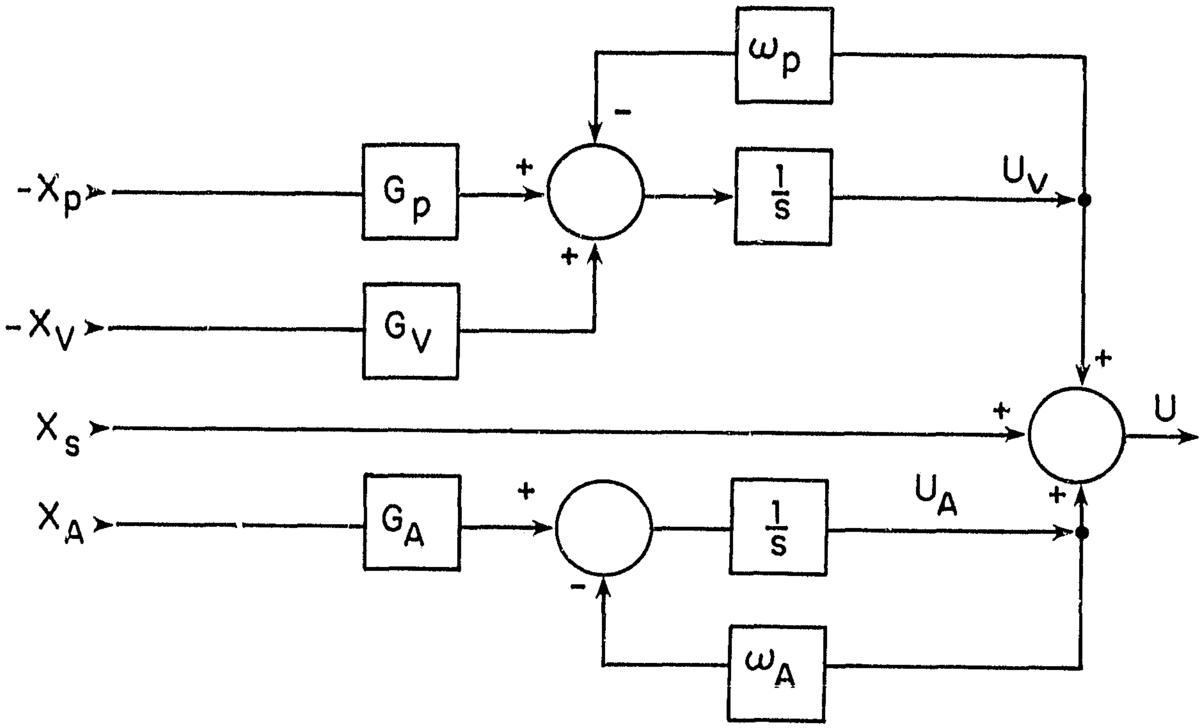
$$u_{i+1} = u_{P_{i+1}} + u_{A_{i+1}} + x_{S_{i+1}}$$

$$c = 0.158\ G_A; \quad k = 124\ \frac{G_P}{\omega_P} \quad ; \quad \omega_N = \sqrt{k/m}$$

$$H_1 = \frac{cs^2}{s + \omega_A}\ ; \quad H_2 = -\ \frac{k\omega_P}{s + \omega_P}$$

$$h_c = \frac{s^3(s + \omega_P) + (k\omega_P/c)\ s(s + \omega_A)}{s^2(s + \omega_A)(s + \omega_P) + (k\omega_P/m)(s + \omega_A)}$$

Figure 10. P1 (Parallel) System Logic.



$$u_{V_{i+1}} = u_{V_i} - \omega_p T u_{V_i} - G_p T x_{P_{i+1}} - G_V T x_{V_{i+1}}$$

$$u_{A_{i+1}} = u_{A_i} - \omega_A T u_{A_{i+1}} + G_A T x_{A_{i+1}}$$

$$u_{i+1} = u_{V_{i+1}} + u_{A_{i+1}} + X_{S_{i+1}}$$

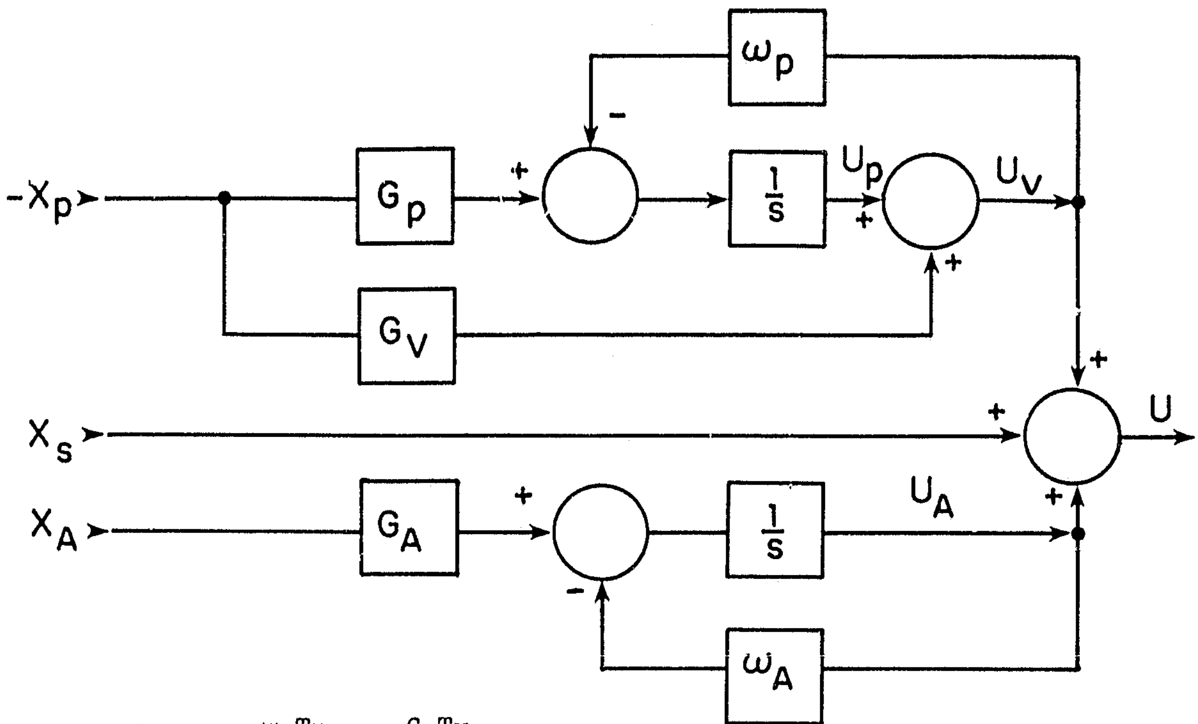
$$c = 0.158\ G_A\ ; \qquad k = 124\ G_P/\omega_P$$

$$c_P = 0.62\ K_V G_V/\omega_P ; \qquad \zeta_P = c_P/2\sqrt{mk}$$

$$H_1 = \frac{cs^2}{s + \omega_A}\ ; \qquad H_2 = -\frac{c_P\omega_P(s + k/c_P)}{s + \omega_P}$$

$$h_c = \frac{s^3(s + \omega_P) + (c_P\omega_P/c)\ s(s + \omega_A)(s + k/c_P)}{s^2(s + \omega_A)(s + \omega_P) + (c_P\omega_P/m)(s + \omega_A)(s + k/c_P)}$$

Figure 11. P1-V (Parallel with Velocity Input) System Logic.



$$u_{P_{i+1}} = u_{P_i} - \omega_P T u_{V_i} - G_P T x_{P_{i+1}}$$

$$u_{V_{i+1}} = u_{P_{i+1}} - G_V x_{P_{i+1}}$$

$$u_{A_{i+1}} = u_{A_i} - \omega_A T u_{A_i} + G_A T x_{A_{i+1}}$$

$$u_{i+1} = u_{V_{i+1}} + u_{A_{i+1}} + x_{S_{i+1}}$$

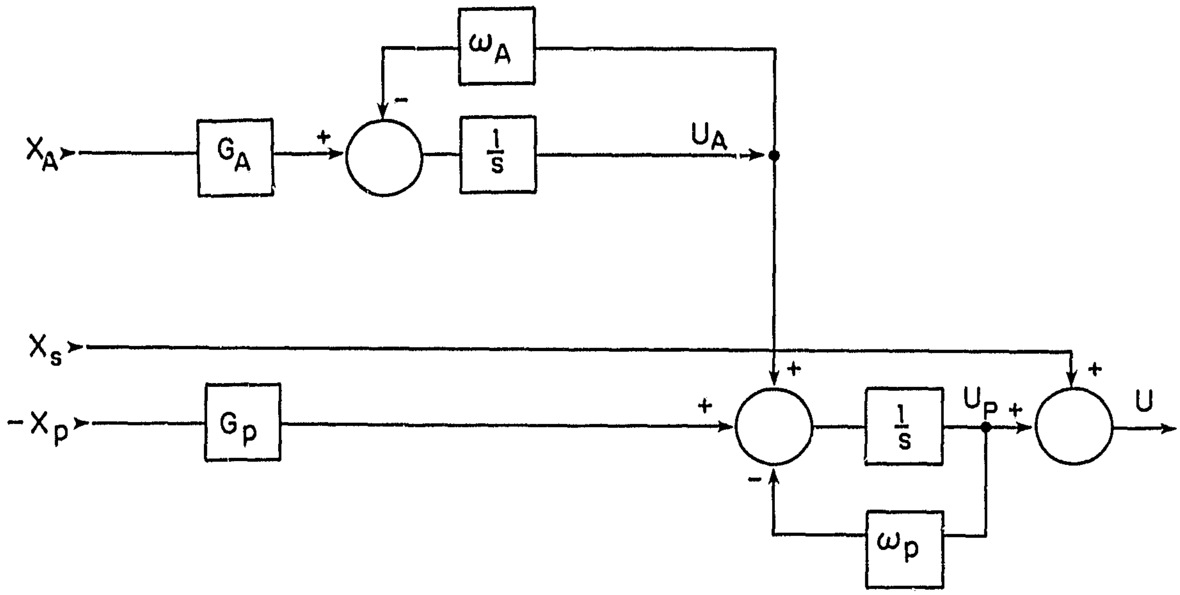
$$c = 0.158\ G_A; \qquad k = 124\ \frac{G_P}{\omega_P}$$

$$c_P = \frac{124\ G_V}{\omega_P}; \qquad \zeta_P = c_P/2\sqrt{mk}$$

$$H_1 = \frac{c\ \text{[illegible]}}{s + \omega_A}; \qquad H_2 = -\ \frac{c_P\omega_P(s + k/c_P)}{s + \omega_P}$$

$$h_c = \frac{s^3(s + \omega_P) + (c_P\omega_P/c)\ s(s + \omega_A)\ (s + k/c_P)}{s^2(s + \omega_A)\ (s + \omega_P) + (c_P\omega_P/m)\ (s + \omega_A)\ (s + k/c_P)}$$

Figure 12. P1-D (Parallel, Damped) System Logic.



$$u_{A_{i+1}} = u_{A_i} - \omega_A T u_{A_i} - G_A T x_{A_{i+1}}$$

$$u_{P_{i+2}} = u_{P_{i+1}} - \omega_P T u_{P_{i+1}} + G_P T x_{P_{i+2}} + T u_{A_{i+1}}$$

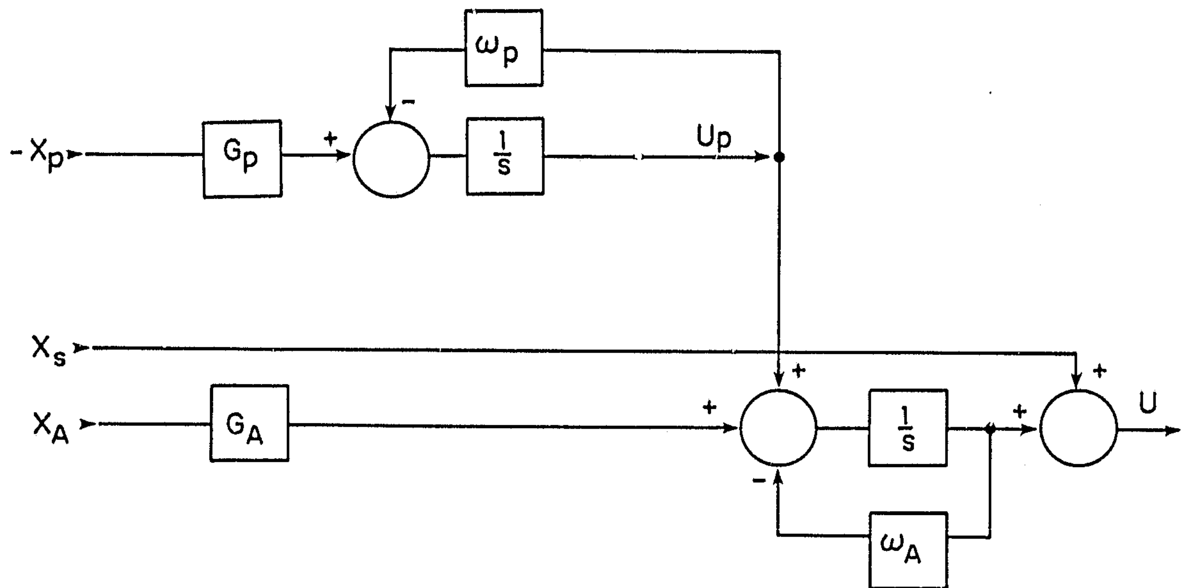
$$u_{i+2} = u_{A_{i+2}} + x_{S_{i+2}}$$

$$c = 0.158\ G_A \quad ; \qquad k = 124\ G_P/\omega_P$$

$$H_1 = \frac{cs^2}{(s + \omega_A)(s + \omega_P)} \; ; \qquad H_2 = - \frac{k\omega_P}{(s + \omega_P)}$$

$$h_c = \frac{s^3 + (k\omega_P/c)\ s(s + \omega_A)}{s^2(s + \omega_A)(s + \omega_P) + (k\omega_P/m)(s + \omega_A)}$$

Figure 13. S1 (Series) System Logic.



$$u_{P_{i+1}} = u_{P_i} - \omega_P T u_{P_i} - G_P T x_{P_{i+1}}$$

$$u_{A_{i+2}} = u_{A_{i+1}} - \omega_A T u_{A_{i+1}} + G_P T x_{A_{i+2}} + T u_{A_{i+1}}$$

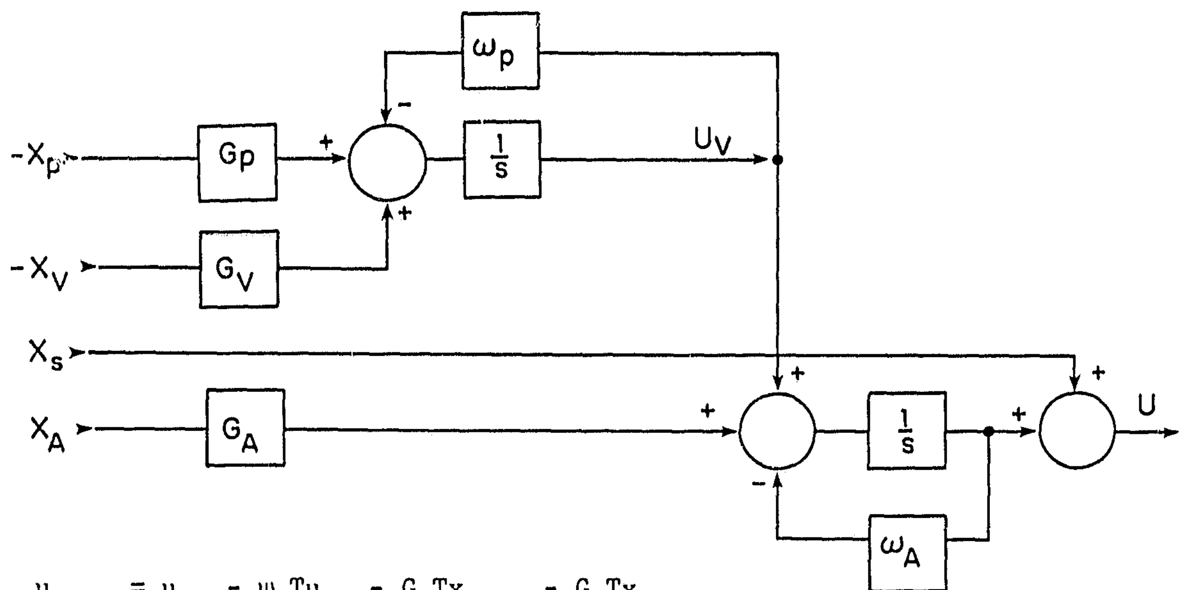
$$u_{i+2} = u_{A_{i+2}} + x_{S_{i+2}}$$

$$c = 0.158\ G_A \quad ; \qquad k = 124\ G_P/\omega_P\omega_A$$

$$H_1 = \frac{cs^2}{s + \omega_A} \quad ; \qquad H_2 = -\frac{k\omega_P\omega_A}{(s + \omega_A)(s + \omega_A)}$$

$$h_c = \frac{s^3(s + \omega_P) + (k\omega_P\omega_A/c)s}{s^2(s + \omega_A)(s + \omega_P) + (k\omega_P\omega_A/m)}$$

Figure 14. S2 (Series) System Logic.



$$u_{V_{i+1}} = u_{V_i} - \omega_P T u_{V_i} - G_P T x_{P_{i+1}} - G_V T x_{V_{i+1}}$$

$$u_{A_{i+2}} = u_{A_{i+1}} - \omega_A T u_{A_{i+1}} + G_P T x_{A_{i+2}} + T u_{V_{i+1}}$$

$$u_{i+2} = u_{A_{i+2}} + x_{S_{i+2}}$$

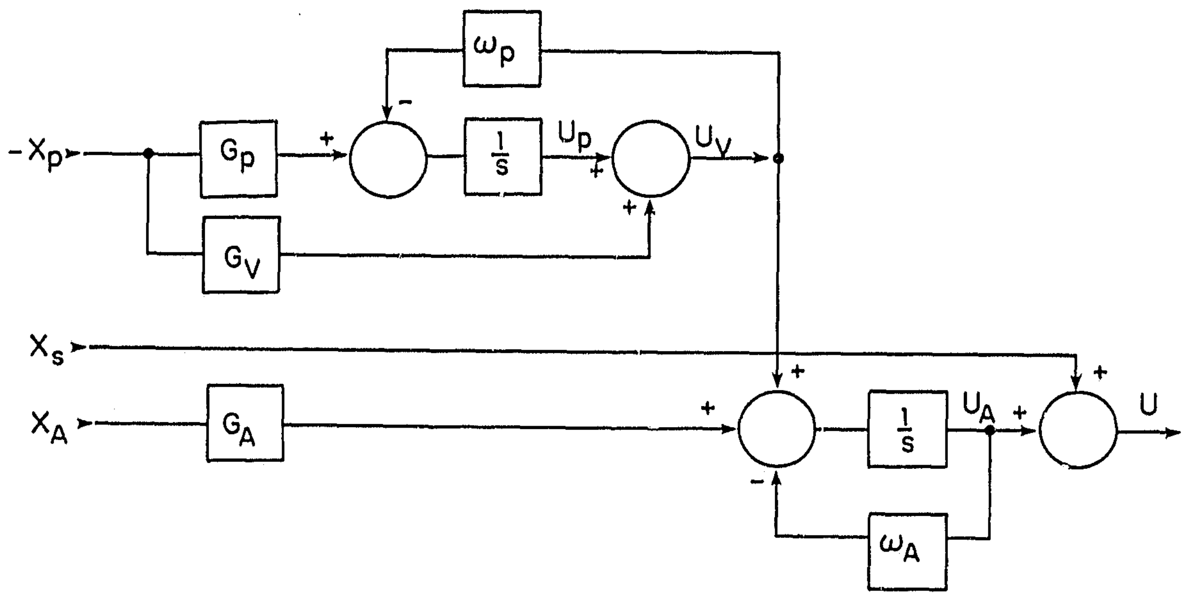
$$c = 0.158\ G_A \ ; \qquad k = 124\ G_P/\omega_P\omega_A$$

$$c_P = 0.62\ K_V G_V/\omega_P\omega_A \ ; \qquad \zeta_P = c_P/2\sqrt{mk}$$

$$H_1 = \frac{cs^2}{s + \omega_A} \ ; \qquad H_2 = -\ \frac{c_P\omega_P\omega_A(s + k/c_P)}{(s + \omega_P)(s + \omega_a)}$$

$$h_c = \frac{s^3(s + \omega_P) + (c_P\omega_P\omega_A/c)\ s(s + k/c_P)}{s^2(s + \omega_A)\ (s + \omega_P) + (c_P\omega_P\omega_A/m)\ (s + k/c_P)}$$

Figure 15. S2-V (Series with Velocity Input) System Logic.



$$u_{P_{i+1}} = u_{P_i} - \omega_P T u_{V_i} - G_P T x_{P_{i+1}}$$

$$u_{V_{i+1}} = u_{P_{i+1}} - G_V x_{P_{i+1}}$$

$$u_{A_{i+2}} = u_{A_{i+1}} - \omega_A T u_{A_{i+1}} + G_P T x_{A_{i+2}} + T u_{V_{i+1}}$$

$$u_{i+2} = u_{A_{i+2}} + x_{S_{i+2}}$$

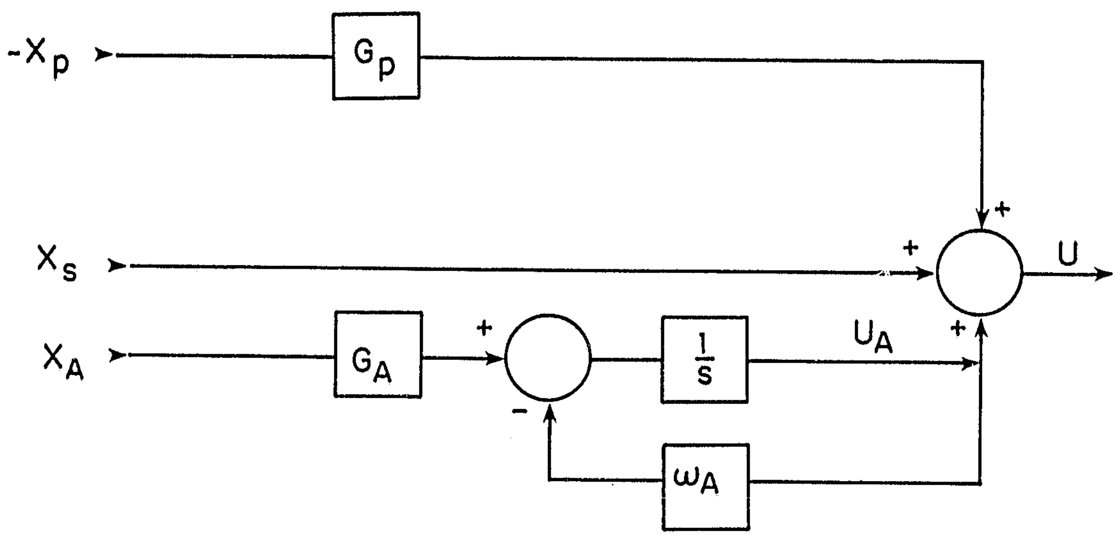
$$c = 0.158\ G_A \quad ; \qquad k = 124\ G_P/\omega_P\omega_A$$

$$c_P = 124\ G_V/\omega_P\omega_A \quad ; \qquad \zeta_P = c_P/2\sqrt{mk}$$

$$H_1 = \frac{cs^2}{s + \omega_A} \quad ; \qquad H_2 = -\frac{c_P\omega_P\omega_A(s + k/c_P)}{(s + \omega_P)(s + \omega_a)}$$

$$h_c = \frac{s^3(s + \omega_P) + (c_P\omega_P\omega_A/c)\ s(s + k/c_P)}{s^2(\ + \omega_A)\ (s + \omega_P) + (c_P\omega_P\omega_A/m)\ (s + k/c_P)}$$

Figure 16. S2-D (Series 2, Damped) System Logic.



$$u_{A_{i+1}} = u_{A_i} - \omega_A T u_{A_{i+1}} + G_A T x_{A_{i+1}}$$

$$u_{i+1} = u_{A_{i+1}} - G_P x_{P_{i+1}} + x_{S_{i+1}}$$

$$c = 0.158\ G_A \quad ; \qquad k = 124\ G_P$$

$$H_1 = \frac{cs^2}{s + \omega_A} \quad ; \qquad H_2 = -k$$

$$h_c = \frac{s^3 + (k/c)\ s(s + \omega_A)}{(s + \omega_A)\ (s^2 + k/m)}$$

Figure 17. B1 (Direct Stiffness) System Logic.

Figures 18 to 21, supplied by Mr. Mallette, show plots of $Re\{h_c\}$ and $|R_c|^2$ against frequency for the P1 and S2 systems with two values for c. For these figures, c has values of 10.11 or 20.22 Ns/m as indicated. Other parameters are ω_A = 16 rps, ω_P = 8 rps, and k = 15.5 N/m. It will be noted that the "resonance" amplitude of the proof-mass, as indicated by $|R_c|^2$ is greater for the P1 system than for the S2 system, and appears to increase more rapidly as c is increased. However, the overall damping $Re\{h_c\}$, is lower for low frequency values for S2, as compared with P1, indicating that this improved behavior may be obtained at the expense of poorer performance.

In an attempt to reduce the apparent resonance of the proof-mass, provisions were made for a velocity feedback in systems P1-V and S2-V of Figures 11 and 15, in anticipation of the availabilility of hardware which would accommodate a velocity transducer. Also, internal velocity feedbacks were introduced into the P1-D and S2-D systems of Figures 12 and 16. The latter two systems are incorporated in the digital program currently under investigation, which are discussed in a later section.

Control Law Design

A justification for the use of velocity feedback can be given as follows. Note first that

$$R_c = H_c/ms - 1$$

and that the limits on R_c for s equal to zero and infinity are zero and unity respectively. Thus, if any "resonance" is to occur, it will be due to the behavior of some H_c at some intermediate frequency.

Now consider the expression for H_c derived earlier

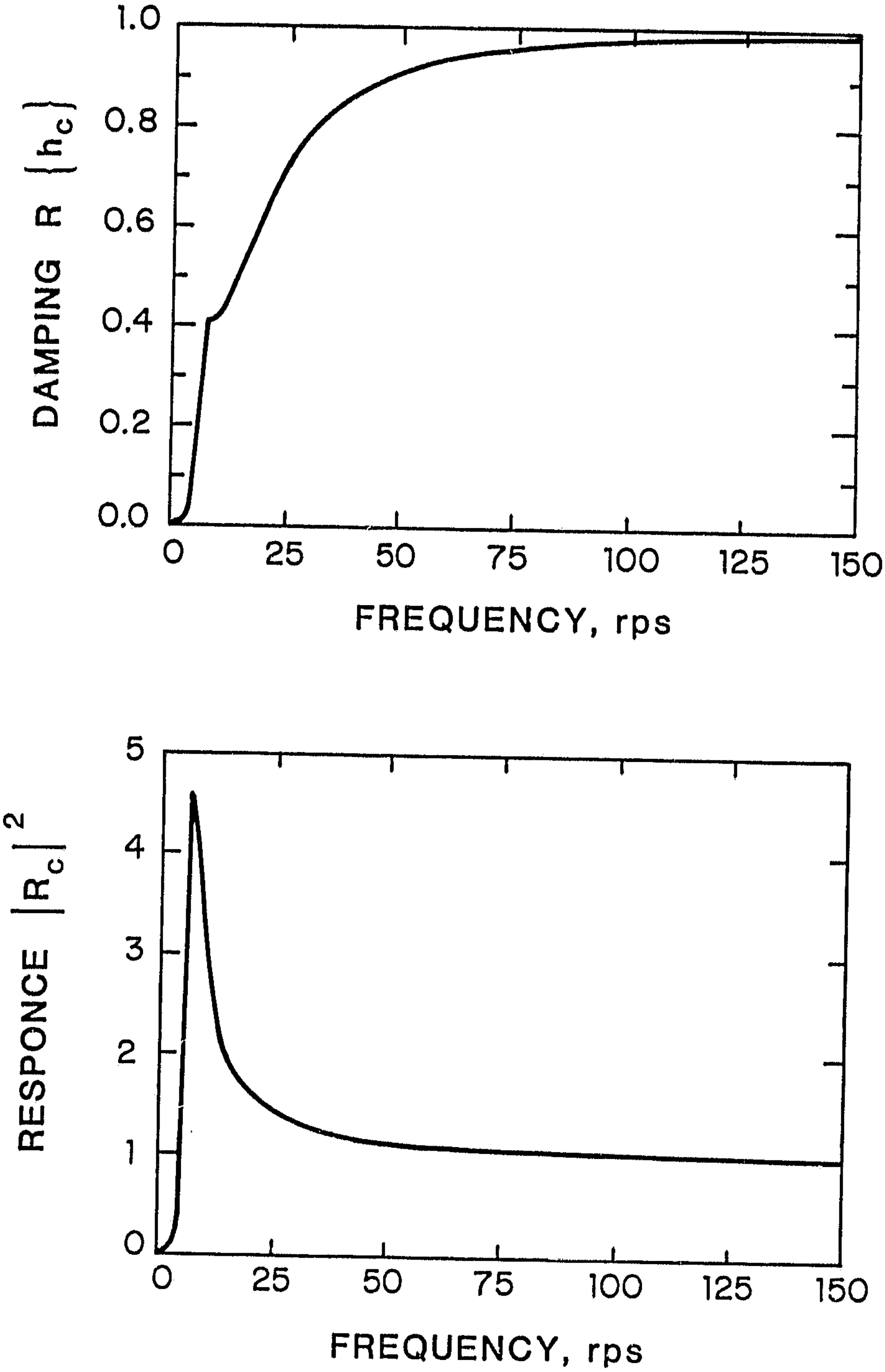


Figure 18. P1 System Damping and Response.
c = 10.11 Ns/m

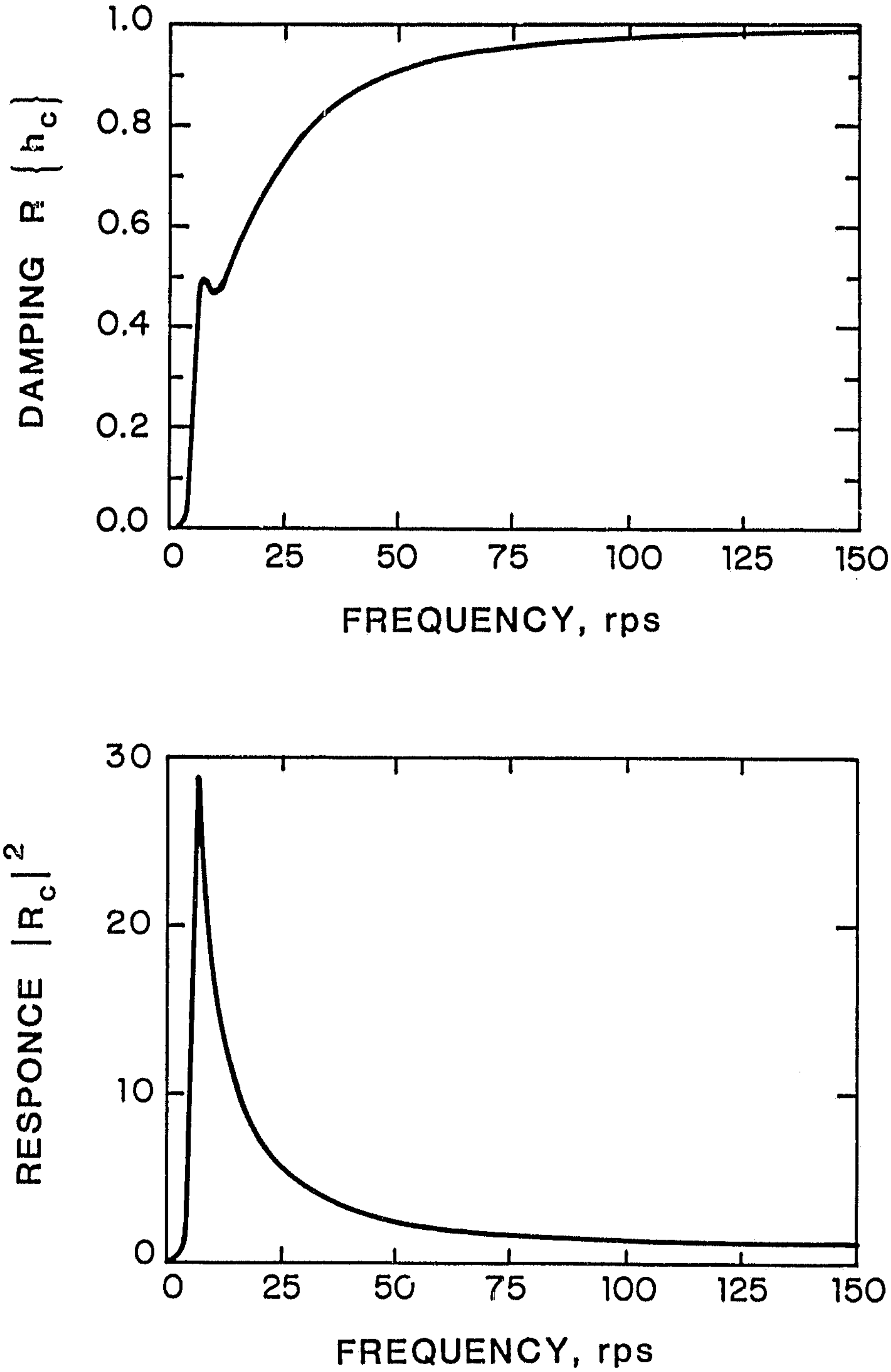


Figure 19. P1 System Damping and Response.
c = 20.22 Ns/m

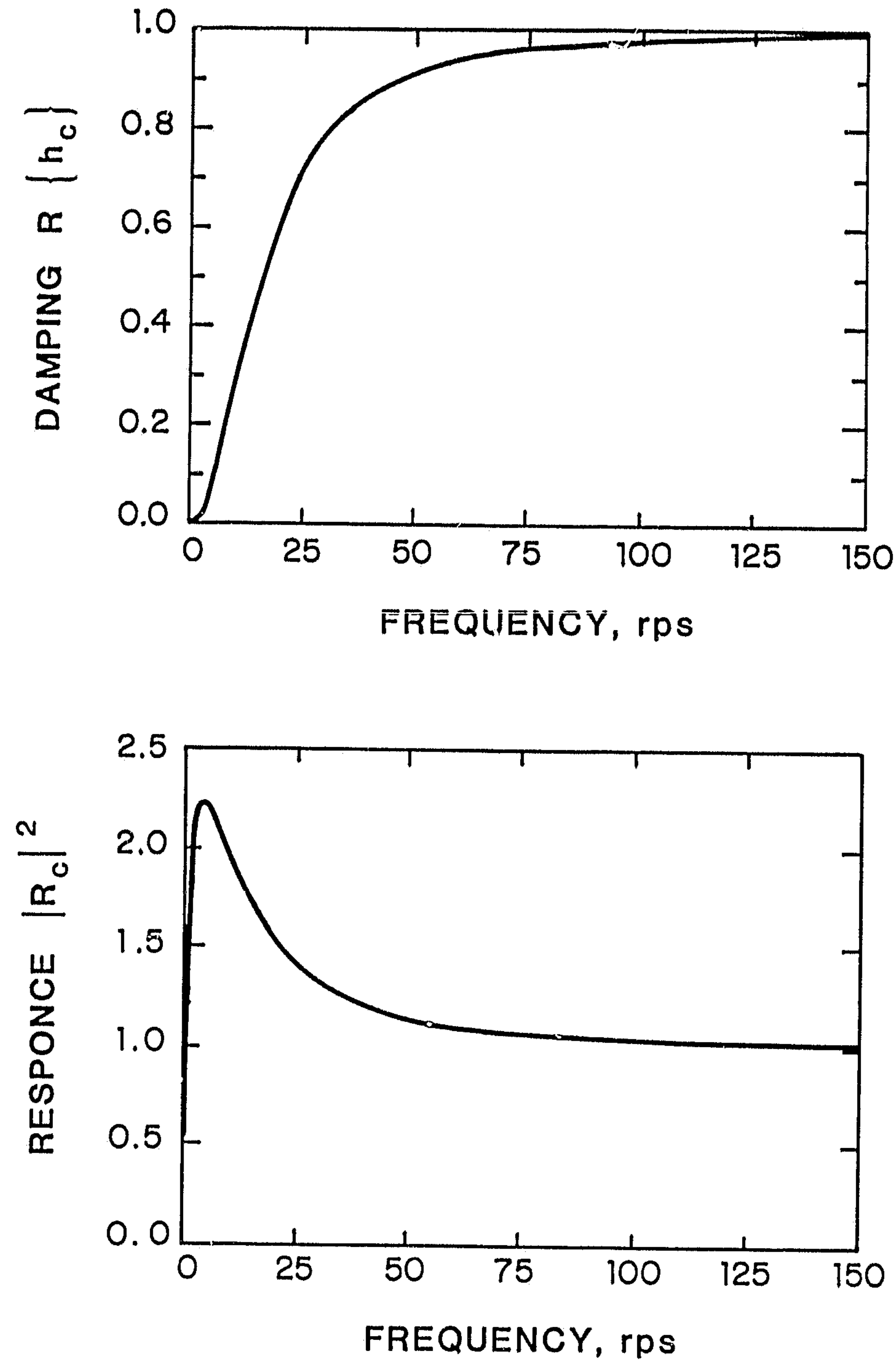


Figure 20. S2 System Damping and Response.
c = 10.11 Ns/m

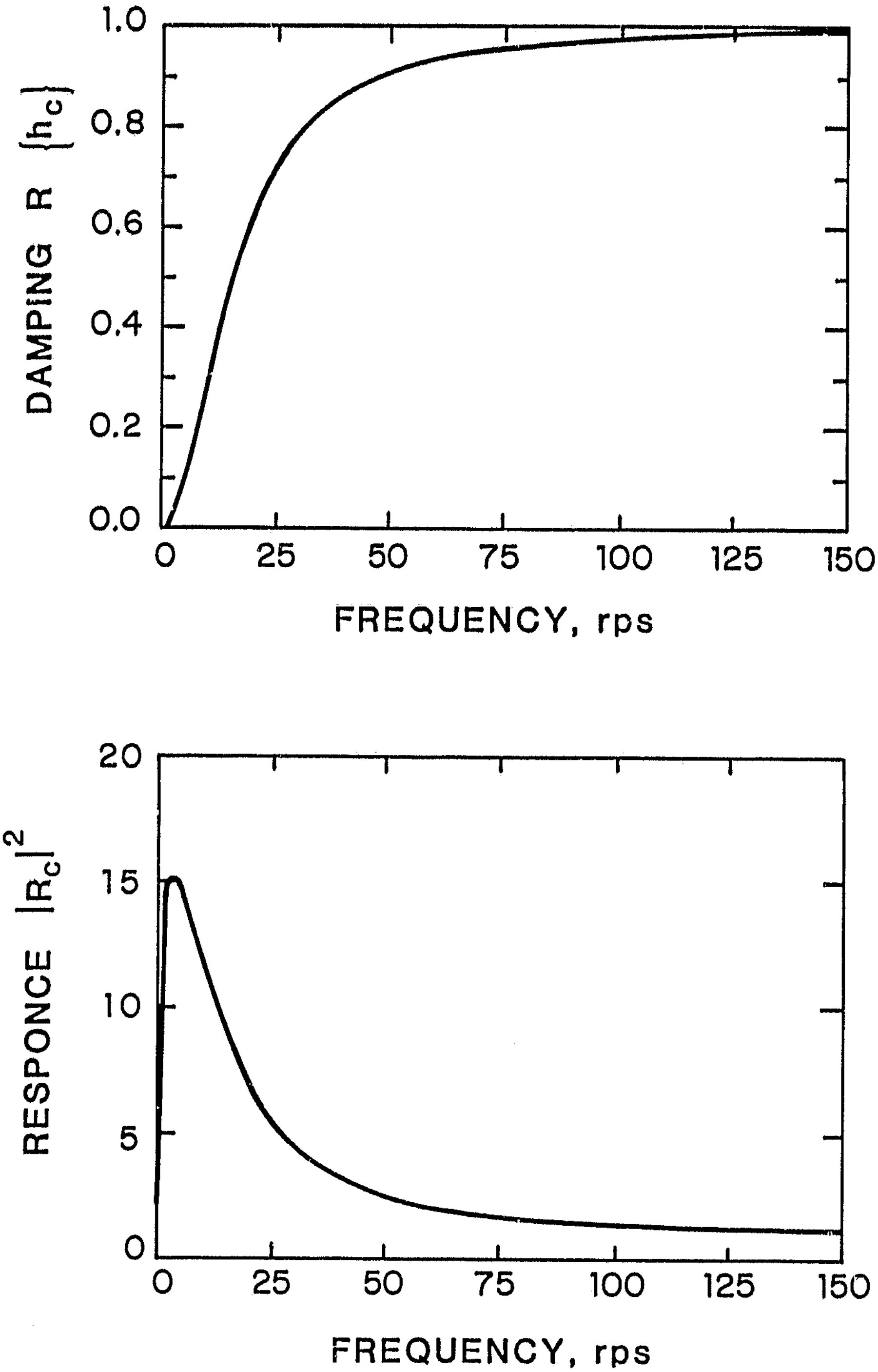


Figure 21. S2 System Damping and Response.
$c = 20.22$ Ns/m

$$sH_c = \frac{H_1 - H_2}{1 - H_2/ms^2}$$

in which H_1 and H_2 are themselves well-behaved. The problem must occur in the denominator of the above equation, which suggests the closed loop transfer function of a control system whose open loop transfer function is $-H_2/ms^2$. These open-loop transfer functions are summarized in Table 4 below for the systems with internal velocity feedback. Three of these systems, S1-V, S1-D and B1-V have not been shown in Figures 10 to 17.

TABLE 4. Open-Loop Transfer Functions

SYSTEM	OPEN-LOOP TRANSFER FUNCTION
P1-V, P1-D S1-V, S1-D	$\frac{(1 + 2\zeta_P\, s/\omega_N)}{(1 + s/\omega_P)(s/\omega_N)^2}$
S2-V, S2-D	$\frac{(1 + 2\zeta_P s/\omega_N)}{(1 + s/\omega_P)(1 + s/\omega_A)(s/\omega_N)^2}$
B1-V	$\frac{(1 + 2\zeta_P s/\omega_N)}{(s/\omega_N)^2}$

The stability criterion is that the phase angle of the open-loop transfer function is equal to $-180 + \phi_m$, where ϕ_m is a suitable phase margin, when the magnitude of the open-loop transfer function is unity. Clearly, a large critical damping ratio is very helpful. On the other hand, a low value for the roll-off frequency ω_P could cause problems with P1-D and S2-D, while a low value for the roll-off frequency ω_A could cause problems with S2-D because a lag-lead system would result. Provided that suitable stability has been provided, as indicated by the open-loop transfer functions in Table 4, the behavior of H_c should be reasonably close to that of H_1/c. The major remaining question is whether to select the S1 type behavior, limiting to zero at high frequency, or the behavior of the other systems shown, limiting to unity.

A further criterion for overall stability is that the damper absorbs energy at all frequencies, i.e.,

$$\frac{1}{T} \int_0^T F\dot{x}_2 dt > 0$$

where $T = 2\pi/\omega$.

If $\quad x_2 = |x_2| \sin \omega t$

$$\dot{x}_2 = \omega |x_2| \cos \omega t$$

$$F = \omega |H_c| |x_2| \cos (\omega t + \phi)$$

Then the above condition becomes

$$\frac{1}{T} \int_0^T \omega^2 |x_2|^2 |H_c| (\cos^2 \omega t \cos \phi - \cos \omega t \sin \omega t \sin \phi)\, dt$$

$$= \frac{1}{2} \omega^2 |x_2|^2 |H_c| \cos \phi > 0$$

This is satisfied so long as

$$|H_c| \cos \phi = \mathrm{Re}\{H_c\} > 0.$$

Thus the damped absorbs energy at all frequencies for which H_c, and therefore h_c, have positive real parts.

Digital Computer Program

The most recent digital computer program is shown in Figure 22. This is written in assembly language for the TRS-80 model 1 using the Editor/Assembler 1.0.

The upper part of the program is run on the TRS-80, whereas the lower half is transferred to addresses starting at C000H, and is therefore loaded into the memory located in the controller when the program

```
7000                      ORG   7000H     ;CTRL60, 11:45A, 7/26/84, BY JKH
7000 CDC901      CTRL60   CALL  01C9H     ;CLEAR AND HOME CURSOR
7003 D340                 OUT   (40H),A  ;OPEN BOX
7005 DD2100C8             LD    IX,0CB00H        ;SET X-INDEX IN TRS-80
7009 3E05                 LD    A,5       ;LOAD
700B DD7700               LD    (IX),A    ;AND
700E C630                 ADD   A,30H     ;DISPLAY
7010 32403C               LD    (3C40H),A         ;WAT
7013 3E06                 LD    A,6
7015 DD7701               LD    (IX+1),A
7018 C630                 ADD   A,30H
701A 32483C               LD    (3C48H),A         ;WPT
701D 3E02                 LD    A,2
701F DD7702               LD    (IX+2),A
7022 C630                 ADD   A,30H
7024 32503C               LD    (3C50H),A         ;GAT
7027 3E09                 LD    A,9
7029 DD7703               LD    (IX+3),A
702C C630                 ADD   A,30H
702E 32583C               LD    (3C58H),A         ;GPT
7031 3E03                 LD    A,3
7033 DD7704               LD    (IX+4),A
7036 C630                 ADD   A,30H
7038 32603C               LD    (3C60H),A
703B 210A71               LD    HL,710AH          ;LOAD
703E 1100C0               LD    DE,0C000H         ;PROGRAM
7041 010008               LD    BC,0800H          ;INTO
7044 EDB0                 LDIR                    ;BOX
7046 D348                 OUT   (48H),A           ;CLOSE BOX
7048 D350                 OUT   (50H),A           ;HARDWARE RESET
704A 3E41                 LD    A,41H             ;DISPLAY
704C 21803C               LD    HL,3C80H          ;CODES
704F 77          DIS      LD    (HL),A            ;FOR
7050 110800               LD    DE,8              ;GAIN
7053 19                   ADD   HL,DE             ;CHANGE
7054 3C                   INC   A
7055 3C                   INC   A
7056 FE48                 CP    48H
7058 C26070               JP    NZ,CON
705B 21C03C               LD    HL,3CC0H
705E 3E42                 LD    A,42H
7060 FE4C        CON      CP    4CH
7062 C24F70               JP    NZ,DIS
7065 3A4038      BREAK    LD    A,(3840H)         ;TEST
7068 FE04                 CP    4                 ;FOR
706A C26E70               JP    NZ,KEY            ;PROGRAM
706D EF                   RST   40                ;BREAK
706E CD2B00      KEY      CALL  2BH               ;SOFTWARE KEYBOARD READ
7071 FE00                 CP    0
7073 CA6570               JP    Z,BREAK
7076 32003C               LD    (3C00H),A
7079 FE20                 CP    20H
707B DA8970               JP    C,NEWP
707E FE28                 CP    28H
7080 D28970               JP    NC,NEWP
7083 CDAB70               CALL  CTRL              ;CONTROL IF SHIFT 0 - 7
7086 C36570               JP    BREAK
7089 FE30        NEWP     CP    30H
708B DA9970               JP    C,NEWG
708E FE38                 CP    38H
7090 D29970               JP    NC,NEWG
7093 CDB770               CALL  NEWPRO            ;NEW PROGRAM IF 0 - 7
7096 C36570               JP    BREAK
```

Figure 22. Control Program (continued on following pages through pg. 45)

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```
7099 E65F       NEWG     AND    5FH
709B FE41                CP     41H
709D DA6570              JP     C,BREAK
70A0 FE4B                CP     4BH
70A2 D26570              JP     NC,BREAK
70A5 CDC970              CALL   NEWGAN          ;NEW GAIN IF A - J
70A8 C36570              JP     BREAK
70AB CB27       CTRL     SLA    A               ;HARD CONTROL INPUT (SHIFT 0 - ")
70AD CB27                SLA    A
70AF CB27                SLA    A
70B1 F640                OR     40H
70B3 4F                  LD     C,A
70B4 ED79                OUT    (C),A
70B6 C9                  RET
70B7 CB27       NEWPRO   SLA    A               ;SELECT NEW PROGAM (0 - 7)
70B9 CB[illegible]       SLA    A
70BB [illegible]         SLA    A
70BD F6[illegible]       OR     199
70BF D340                OUT    (40H),A
70C1 3203C0              LD     (0C003H),A
70C4 D348                OUT    (48H),A
70C6 D350                OUT    (50H),A
70C8 C9                  RET
70C9 E61F       NEWGAN   AND    1FH             ;CHANGE GAIN (A - J)
70CB 3D                  DEC    A
70CC E60F                AND    0FH
70CE 5F                  LD     E,A
70CF CB2B                SRA    E
70D1 1600                LD     D,0
70D3 2100C8              LD     HL,0C800H
70D6 B7                  OR     A
70D7 19                  ADD    HL,DE
70D8 E5                  PUSH   HL
70D9 DDE1                POP    IX
70DB D340                OUT    (40H),A
70DD CB47                BIT    0,A
70DF C2E870              JP     NZ,AB
70E2 CD0271              CALL   ADV
70E5 C3EB70              JP     DISP
70E8 CD0671     AB       CALL   RETRO
70EB CB23       DISP     SLA    E               ;DISPLAY GAIN
70ED CB23                SLA    E
70EF CB23                SLA    E
70F1 21003D              LD     HL,3D00H
70F4 B7                  OR     A
70F5 19                  ADD    HL,DE
70F6 DD7E00              LD     A,(IX)
70F9 B7                  OR     A
70FA C630                ADD    A,30H
70FC 77                  LD     (HL),A
70FD D348                OUT    (48H),A
70FF D350                OUT    (50H),A
7101 C9                  RET
7102 DD3400     ADV      INC    (IX)            ;ADVANCE GAIN INDEX (GAIN REDUCED)
7105 C9                  RET
7106 DD3500     RETRO    DEC    (IX)            ;REDUCE GAIN INDEX (GAIN INCREASED)
7109 C9                  RET
710A 31FFCF              LD     SP,0CFFFH       ;SET SP- START CONTROL PROGRAM
710D C34000              JP     40H      ;JP TO DEMO3. CHANGED TO RST XX BY KEY 0-7
7110 00                  NOP
7111 00                  NOP
7112 C35A00              JP     5AH      ;JP TO DEMO1 BY KEY 1
7115 00                  NOP
```

```
7116 00               NOP
7117 00               NOP
7118 00               NOP
7119 00               NOP
711A C37400           JP     74H       ;JP TO DEMO2 BY KEY 2
711D 00               NOP
711E 00               NOP
711F 00               NOP
7120 00               NOP
7121 00               NOP
7122 C34000           JP     40H       ;JP TO DEMO3 BY KEY 3
7125 00               NOP
7126 00               NOP
7127 00               NOP
7128 00               NOP
7129 00               NOP
712A C38E00           JP     8EH       ;JP TO F1 BY KEY 4
712D 00               NOP
712E 00               NOP
712F 00               NOP
7130 00               NOP
7131 00               NOP
7132 C32201           JP     122H      ;JP TO S2 BY KEY 5
7135 00               NOP
7136 00               NOP
7137 00               NOP
7138 00               NOP
7139 00               NOP
713A C37D01           JP     17DH      ;JP TO DEMO4 BY KEY 6
713D 00               NOP
713E 00               NOP
713F 00               NOP
7140 00               NOP
7141 00               NOP
7142 C34000           JP     40H       ;JP TO DEMO3 BY KEY 7
7145 00               NOP
7146 00               NOP
7147 00               NOP
7148 00               NOP
7149 00               NOP
714A 00         DEMO3 NOP
714B DB00       TIME  IN     A,(0)     ; READ STATUS
714D E620             AND    20H       ; TEST FOR TIME
714F 28FA             JR     Z,TIME    ;LOOP IF LESS
7151 DB20             IN     A,(20H)   ;RESET CLOCK
7153 D322             OUT    (22H),A   ; READ CH#3
7155 00               NOP
7156 00               NOP
7157 00               NOP
7158 DB00       EOC   IN     A,(0)     ;READ STATUS
715A E680             AND    80H       ;CHECK EOC
715C 28FA             JR     Z,EOC     ;LOOP IF EOC LOW
715E DB10             IN     A,(10H)   ;READ A/D
7160 D310             OUT    (10H),A   ;OUTPUT
7162 18E7             JR     TIME      ;RETURN
7164 00         DEMO1 NOP
7165 DB00       TESTA IN     A,(0)     ;READ STATUS
7167 E620             AND    20H       ;TEST FOR TIME
7169 28FA             JR     Z,TESTA   ;RETURN IF LESS
716B DB20             IN     A,(20H)   ;RESET CLOCK
716D D320             OUT    (20H),A   ;READ CH#1
716F 00               NOP              ;WAIT
7170 00               NOP              ;FOR
```

```
7171 00                      NOP                  ;EOC
7172 DB00         AD         IN     A,(0)         ;READ STATUS
7174 E680                    AND    080H          ;CHECK EOC
7176 28FA                    JR     Z,AD          ;RETURN IF EOC LOW
7178 DB10                    IN     A,(10H)       ;READ A/D
717A D310                    OUT    (10H),A       ;OUTPUT
717C 18E7                    JR     TESTA         ;RETURN
717E 00           DEMO2      NOP
717F DB00         TESTB      IN     A,(0)         ;READ STATUS
7181 E620                    AND    20H           ;TEST FOR TIME
7183 28FA                    JR     Z,TESTB       ;RETURN IF LESS
7185 DB20                    IN     A,(20H)       ;RESET CLOCK
7187 D321                    OUT    (21H),A       ;READ CH#2
7189 00                      NOP                  ;WAIT
718A 00                      NOP                  ;FOR
718B 00                      NOP                  ;EOC
718C DB00         AE         IN     A,(0)         ;READ STATUS
718E E680                    AND    080H          ;CHECK EOC
7190 28FA                    JR     Z,AE          ;RETURN IF EOC LOW
7192 DB10                    IN     A,(10H)       ;READ A/D
7194 D310                    OUT    (10H),A       ;OUTPUT
7196 18E7                    JR     TESTB         ;RETURN
7198 DD2100C8     P1         LD     IX,0C800H          ;SET X-INDEX IN BOX
719C DB00         TESTC      IN     A,(0)         ;READ STATUS
719E E620                    AND    20H           ;TEST FOR TIME
71A0 28FA                    JR     Z,TESTC       ;RETURN IF LESS
71A2 D330                    OUT    (30H),A       ;CHECK SIGNAL
71A4 DB20                    IN     A,(20H)       ;RESET A/D CLOCK
71A6 D320                    OUT    (20H),A       ;START XA
71A8 DD4600                  LD     B,(IX)        ;WAT INTO B
71AB CDF500                  CALL   0F5H          ;STEP UA = UA - WAT*UA INTO HL
71AE CDEA00                  CALL   0EAH          ;READ XA
71B1 00                      NOP
71B2 00                      NOP
71B3 DD4602                  LD     B,(IX+2)            ;GAT INTO B
71B6 CD0101                  CALL   101H          ;INTEG UA = UA + GAT*UA
71B9 D9                      EXX                  ;WORK ON UP IN HL',UV IN DE'
71BA D321                    OUT    (21H),A       ;START XP
71BC DD4601                  LD     B,(IX+1)            ;WPT INTO B'
71BF CDF700                  CALL   0F7H          ;STEP2 UP = UP - WPT*UV INTO HL'
71C2 CDEA00                  CALL   0EAH          ;READ -XP
71C5 DD4603                  LD     B,(IX+3)            ;GPT INTO B'
71C8 CD0101                  CALL   101H          ;INTEG UP =UP - GPT*XP INTO HL'
71CB E5                      PUSH   HL            ;SAVE UP
71CC DD4604                  LD     B,(IX+4)            ;GV INTO B'
71CF CD0101                  CALL   101H          ;ADD  UV = UP - GV*XP INTO HL'
71D2 D1                      POP    DE            ;UP INTO DE'
71D3 E5                      PUSH   HL            ;XFER UV
71D4 EB                      EX     DE,HL         ;UP INTO HL', UV INTO DE'
71D5 D322                    OUT    (22H),A       ;START SIG.
71D7 D9                      EXX                  ;WORK ON U
71D8 D1                      POP    DE            ;UV INTO DE
71D9 E5                      PUSH   HL            ;SAVE UA
71DA B7                      OR     A             ;CLC
71DB ED5A                    ADC    HL,DE         ;U = UV + UA
71DD CD1601                  CALL   116H          ;OVER
71E0 CDEA00                  CALL   0EAH          ;READ XS
71E3 57                      LD     D,A           ;XS
71E4 1E00                    LD     E,0           ;INTO DE
71E6 B7                      OR     A             ;CLC
71E7 ED5A                    ADC    HL,DE         ;U = U + XS
71E9 CD1601                  CALL   116H          ;OVER
71EC 7C                      LD     A,H           ;HIGH BYTE OF U
```

```
71ED C680             ADD   A,80H    ;CONV. FOR OUTPUT
71EF D310             OUT   (10H),A  ;OUTPUT U
71F1 E1               POP   HL       ;REPLACE UA
71F2 18AB             JR    TESTC    ;RETURN
71F4 DB00      READ   IN    A,(0)    ;READ STATUS
71F6 E680             AND   80H      ;TEST EOC
71F8 28FA             JR    Z,READ   ;RETURN IF LOW
71FA DB10             IN    A,(10H)  ;READ A/D
71FC C680             ADD   A,80H    ;CONVERT TO SIGNED VALUE
71FE C9               RET
71FF 54        STEP   LD    D,H      ;HL
7200 5D               LD    E,L      ;INTO DE
7201 CD0E01    STEP1  CALL  10EH     ;INIT. SHIFT
7204 B7               OR    A        ;CLC
7205 ED52             SBC   HL,DE    ;SUB HL = HL - B*DE
7207 CD1601           CALL  116H     ;OVER
720A C9               RET
720B 57        INTEG  LD    D,A      ;E
720C 1E00             LD    E,0      ;INTO DE
720E CD0E01    INTEG2 CALL  10EH     ;INIT. SHIFT
7211 B7               OR    A        ;CLC
7212 ED5A             ADC   HL,DE    ;ADD HL =HL + B*DE
7214 CD1601           CALL  116H     ;OVER
7217 C9               RET
7218 CB2A      SHIFTC SRA   D        ;RT. SHIFT D
721A CB1B             RR    E        ;RT. ROT. E
721C 05               DEC   B
721D 20F9             JR    NZ,SHIFTC        ;CONT. UNTIL B CLEARS
721F C9               RET
7220 E0        OVER   RET   PO       ;RETURN IF NO OVERFLOW
7221 3805             JR    C,MINUS  ;JUMP IF NEG OVERFLOW
7223 21FF7F           LD    HL,7FFFH         ;POS RAIL
7226 1803             JR    CONT
7228 210080    MINUS  LD    HL,8000H         ;NEG RAIL
722B C9        CONT   RET
722C DD2100C8  S2     LD    IX,0C800H                ;SET X-INDEX IN BOX
7230 DB00      TESTF  IN    A,(0)            ;READ STATUS
7232 E620             AND   20H      ;TEST FOR TIME
7234 28FA             JR    Z,TESTF  ;RETURN IF LESS
7236 D330             OUT   (30H),A  ;CHECK SIGNAL
7238 DB20             IN    A,(20H)  ;RESET A/D CLOCK
723A D320             OUT   (20H),A  ;START XA
723C DD4600           LD    B,(IX)   ;WAT INTO B
723F CDF500           CALL  0F5H     ;STEP UA = UA - WAT*UA INTO HL
7242 CDEA00           CALL  0EAH     ;READ XA
7245 00               NOP
7246 00               NOP
7247 DD4602           LD    B,(IX+2)         ;GAT INTO B
724A CD0101           CALL  101H     ;INTEG UA = UA + GAT*UA INTO HL
724D D9               EXX            ;WORK ON UP IN HL',UV IN DE'
724E D321             OUT   (21H),A  ;START XP
7250 DD4601           LD    B,(IX+1)         ;WPT INTO B'
7253 CDF700           CALL  0F7H     ;STEP2 UP = UP - WPT*UV INTO HL'
7256 CDEA00           CALL  0EAH     ;READ -XP
7259 DD4603           LD    B,(IX+3)         ;GPT INTO B'
725C CD0101           CALL  101H     ;INTEG UP = UP - GPT*XP INTO HL'
725F E5               PUSH  HL       ;SAVE UP
7260 DD4604           LD    B,(IX+4)         ;GV INTO B'
7263 CD0101           CALL  101H     ;ADD UV = UV - GV*XP INTO HL
7266 D1               POP   DE       ;UP INTO DE'
7267 E5               PUSH  HL       ;XFER UV
7268 EB               EX    DE,HL    ;UP INTO HL', UV INTO DE'
7269 D322             OUT   (22H),A  ;START SIG.
```

ORIGINAL PAGE IS
OF POOR QUALITY

```
726B D9          03250         EXX               ;WORK ON UA
726C D1          03260         POP     DE        ;UV INTO DE
726D 0609        03270         LD      B,9
726F CD0401      03280         CALL    104H      ;INTEG2 UA = UA +T*UV INTO HL
7272 E5          03290         PUSH    HL        ;SAVE UA
7273 CDEA00      03300         CALL    0EAH      ;READ XS
7276 57          03310         LD      D,A       ;XS
7277 1E00        03320         LD      E,0       ;INTO DE
7279 B7          03330         OR      A         ;CLC
727A ED5A        03340         ADC     HL,DE     ;U=UA+XS
727C CD1601      03350         CALL    116H      ;OVER
727F 7C          03360         LD      A,H       ;HIGH BYTE OF U
7280 C680        03370         ADD     A,80H     ;CONV. FOR OUTPUT
7282 D310        03380         OUT     (10H),A ;OUTPUT U
7284 E1          03390         POP     HL        ;REPLACE UA
7285 18A9        03400         JR      TESTF     ;RETURN
7287 00          03410 DEMO4   NOP
7288 DB00        03420 TESTU   IN      A,(0)     ;READ STATUS
728A E620        03430         AND     20H       ;TEST FOR TIME
728C 28FA        03440         JR      Z,TESTU ;RETURN IF LESS
728E DB20        03450         IN      A,(20H) ;RESET CLOCK
7290 D323        03460         OUT     (23H),A ;READ VELOCIMETER
7292 00          03470         NOP
7293 00          03480         NOP
7294 00          03490         NOP
7295 DB00        03500 AK      IN      A,(0)     ;READ STATUS
7297 E680        03510         AND     080H      ;CHECK EOC
7299 28FA        03520         JR      Z,AK      ;RETURN IF EOC LOW
729B DB10        03530         IN      A,(10H) ;READ A/D
729D D310        03540         OUT     (10H),A ;OUTPUT
729F 18E7        03550         JR      TESTU     ;RETURN
7000             03560         END     CTRL60
00000 Total Errors

AK       7295
TESTU    7288
DEMO4    7287
TESTF    7230
S2       722C
CONT     722B
MINUS    7228
OVER     7220
SHIFTC   7218
INTEG2   720E
INTEG    720B
STEP1    7201
STEP     71FF
READ     71F4
TESTC    719C
P1       7198
AE       718C
TESTB    717F
DEMO2    717E
AD       7172
TESTA    7165
DEMO1    7164
EOC      7158
TIME     714B
DEMO3    714A
RETRO    7106
DISP     70EB
ADV      7102
AB       70E8
```

NEWGAN	70C9
NEWPRO	70B7
NEWG	7099
CTRL	70AB
NEWP	7089
KEY	706E
BREAK	7065
CON	7060
DIS	704F
CTRL60	7000

is first run. At the same time, gains are loaded into the memory of the controller, and a display of gain values is shown on the monitor. Finally, BUSAK is brought high, the Z80 is reset, and the controller runs a program called DEMO3.

Meanwhile, the TRS-80 continues to monitor the keyboard, responding to the entries in Table 4.

TABLE 4. TRS-80 Keyboard Instructions

KEY	RESULT
BREAK	TRS-80 returns to DOS
1	DEMO1 runs
2	DEMO2 runs
3	DEMO3 runs
4	P1-D runs
5	S2-D runs
6	DEMO4 runs
7	DEMO3 runs
A	ω_A decreased by 2
B	ω_A increased by 2
C	ω_P decreased by 2
D	ω_P increased by 2
E	G_A decreased by 2
F	G_A increased by 2
G	G_P decreased by 2
H	G_P increased by 2
I	G_V decreased by 2
J	G_V increased by 2
SHIFT 0	BUSREQ held low ("box opened")
SHIFT 1	BUSREG held high ("box closed")
SHIFT 2	RESET pulsed low (restart current program)

The subroutines DEMO1, DEMO2, DEMO3 and DEMO4 read x_A, $-x_P$, x_S, and $-x_V$, respectively, and output them again with zero gain. These programs are useful for system checkout. In the P1-D and S2-D programs, gain changes are always made by shifting, thus only powers of two are possible. Since the clock is reset every 2 ms, the time interval T equals 2^{-9}, so that all of the gains except for G_V can have values from unity to 256, whereas the latter can only have gains of ½ or less. This simple method of multiplication will be replaced when it appears to be justified to do so. The digital program can be modified to accommodate any seven programs.

The program shown does not use the interrupt feature to select subroutines. In its place, software RESET commands are loaded into low memory, so that the required subroutines are accessed when the hardware RESET is pulsed (SHIFT 2 on the keyboard). The effect is much the same, but could not work if an EPROM were used in the controller.

SECTION V

EXPERIMENTAL WORK

Three versions of the damper design have been under test by Mr. Mallette since the inception of this program. Tests have mainly been run on a flexible 15 foot beam, suspended by long cables, with the damper attached horizontally. Some tests have already been run on the "grillage" at NASA Langley.

The normal procedure has been to use the signal generator to excite a vibration mode, then to cut the signal, and to observe the decay rate of the excited vibration.

Typical results from such tests are shown in Figures 23, 24 and 25. However, most runs have been made to characterize the behavior of the control system, without careful recording of the results.

Typically, the achievement of a satisfactory control law has not proved as simple as was first hoped. Certainly, the final chapter has not yet been written on this problem.

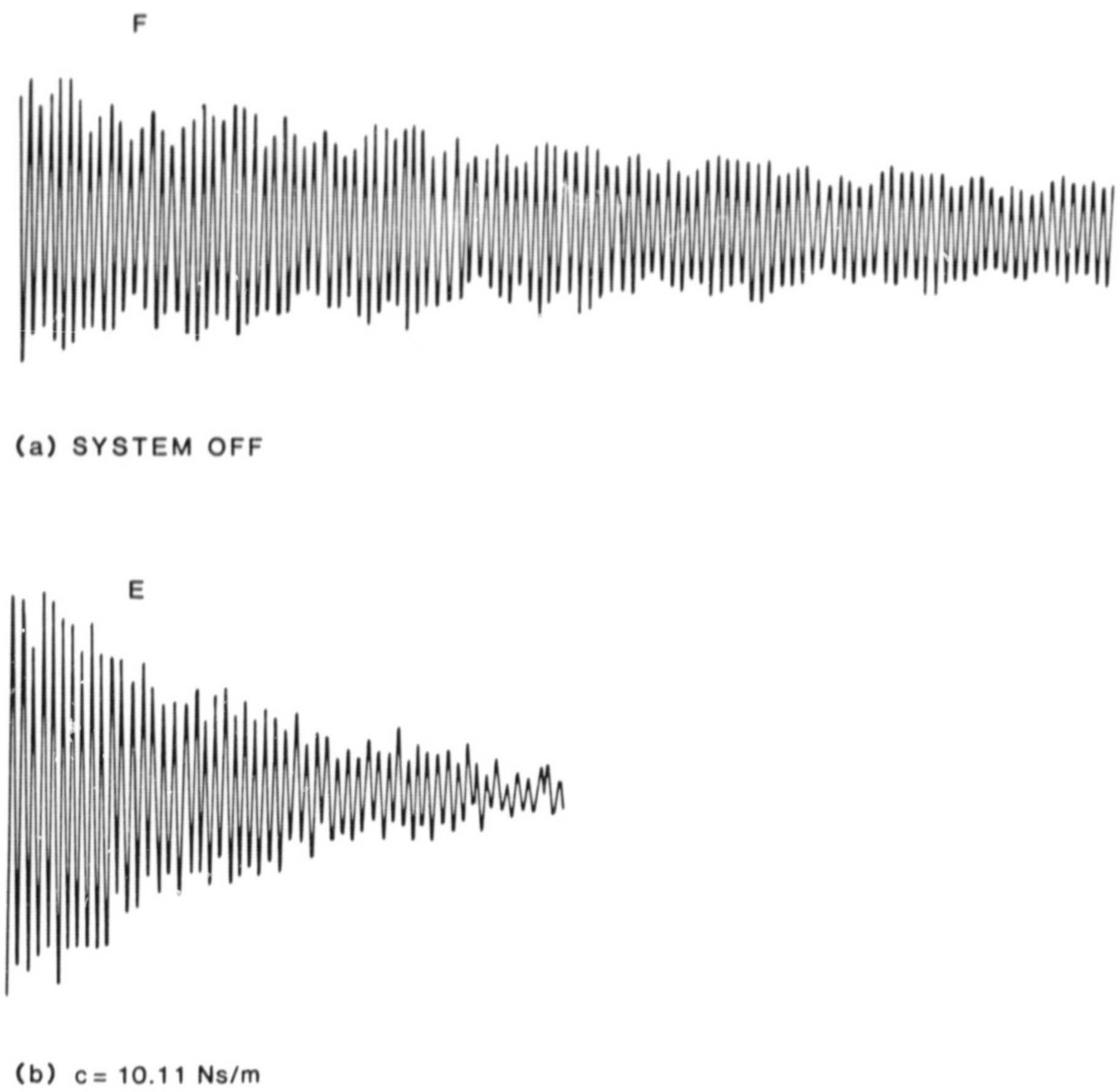
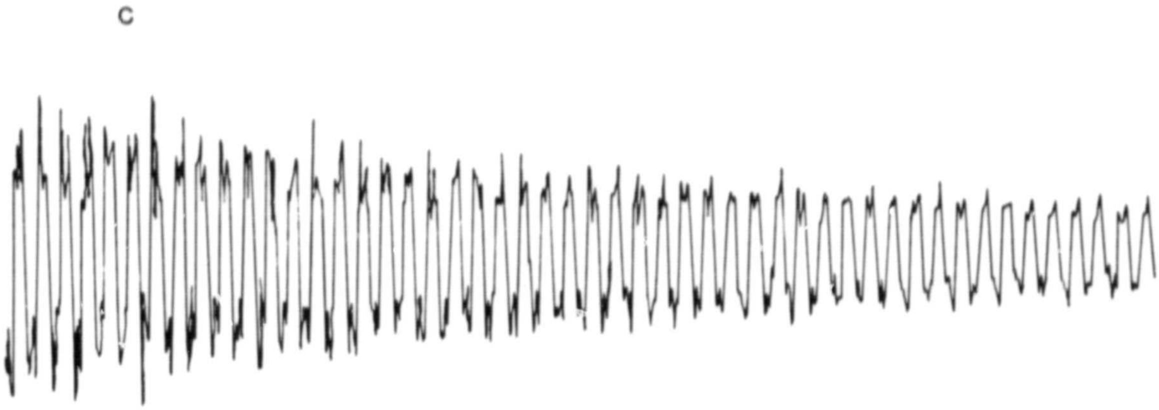
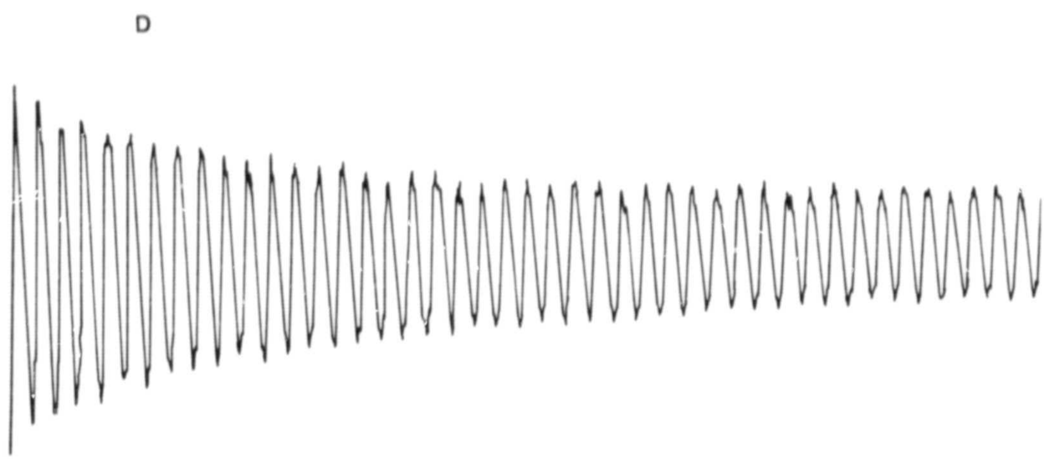


Figure 23. Measured Damping at 5.79 Hz. P1 System

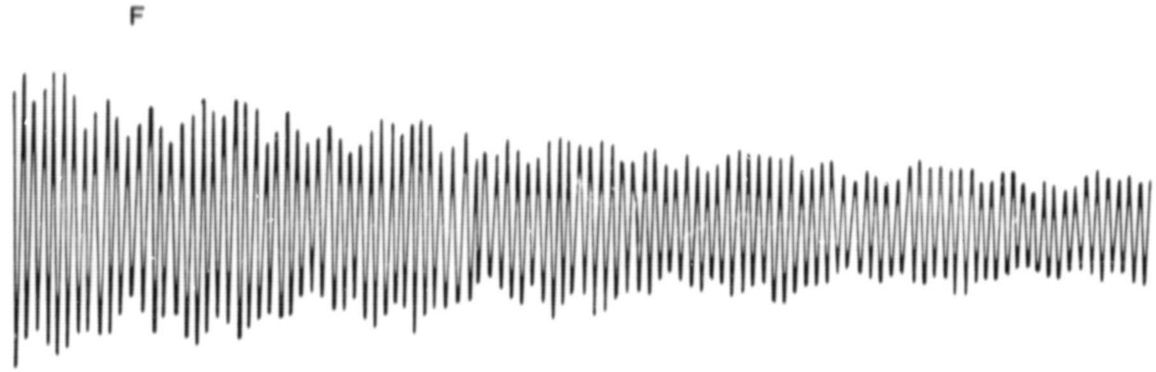


(a) SYSTEM OFF

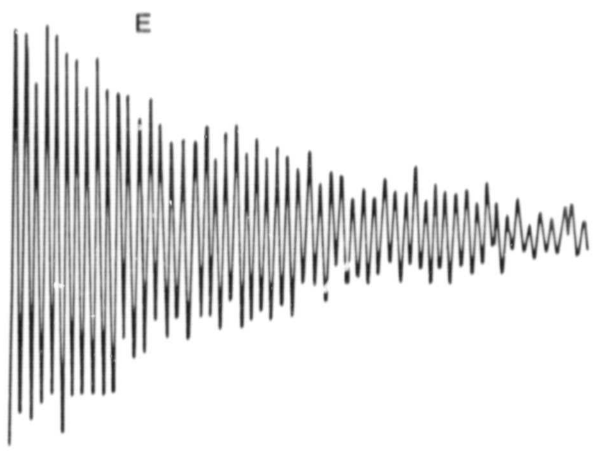


(b) c = 10.11 Ns/m

Figure 24. Measured Damping at 1.95 Hz. P1 System



(a) SYSTEM OFF



(b) c = 20.22 Ns/m

Figure 25. Measured Damping at 4.60 Hz. P1 System

SECTION VI

SYSTEM CONSIDERATIONS

Our original conception was that considerable emphasis must be placed on determining optimum locations for dampers. However, it now seems to be evident that the typical large space structure will undergo considerable modifications and additions during its life, so that optimization of damper locations for any given configuration makes little sense.

Our present concept is that a general purpose damper should be developed, controlled by an individual digital system, whose control law can be dictated by a central computer. Under such a system, the only fixed parameters would be the value of the proof mass and its permissible double amplitude. Given these constraints, the permissible damping factor c can be determined for any given structural amplitude and frequency. Thus assuming a control law which rolls off suitably at low frequencies, the permissible structural amplitude should be only slightly less than the permissible double amplitude of motion of the proof mass.

Following this thinking, we intend to emphasize the development of more sophisticated control laws, paying special attention to the reduction of resonance peaks now present. We also intend to investigate the consequences of "bumping," i.e., of allowing the proof mass to strike the stops. In particular, we want to be sure that no limit cycle motions are possible, in which the proof mass repeatedly strikes the stops.

Figure 26 shows the hypothetical control configuration for a large space structure in which the inertial (or proof-mass) dampers are individually controlled, but are connected to a central computer, so that they can be reprogrammed as required.

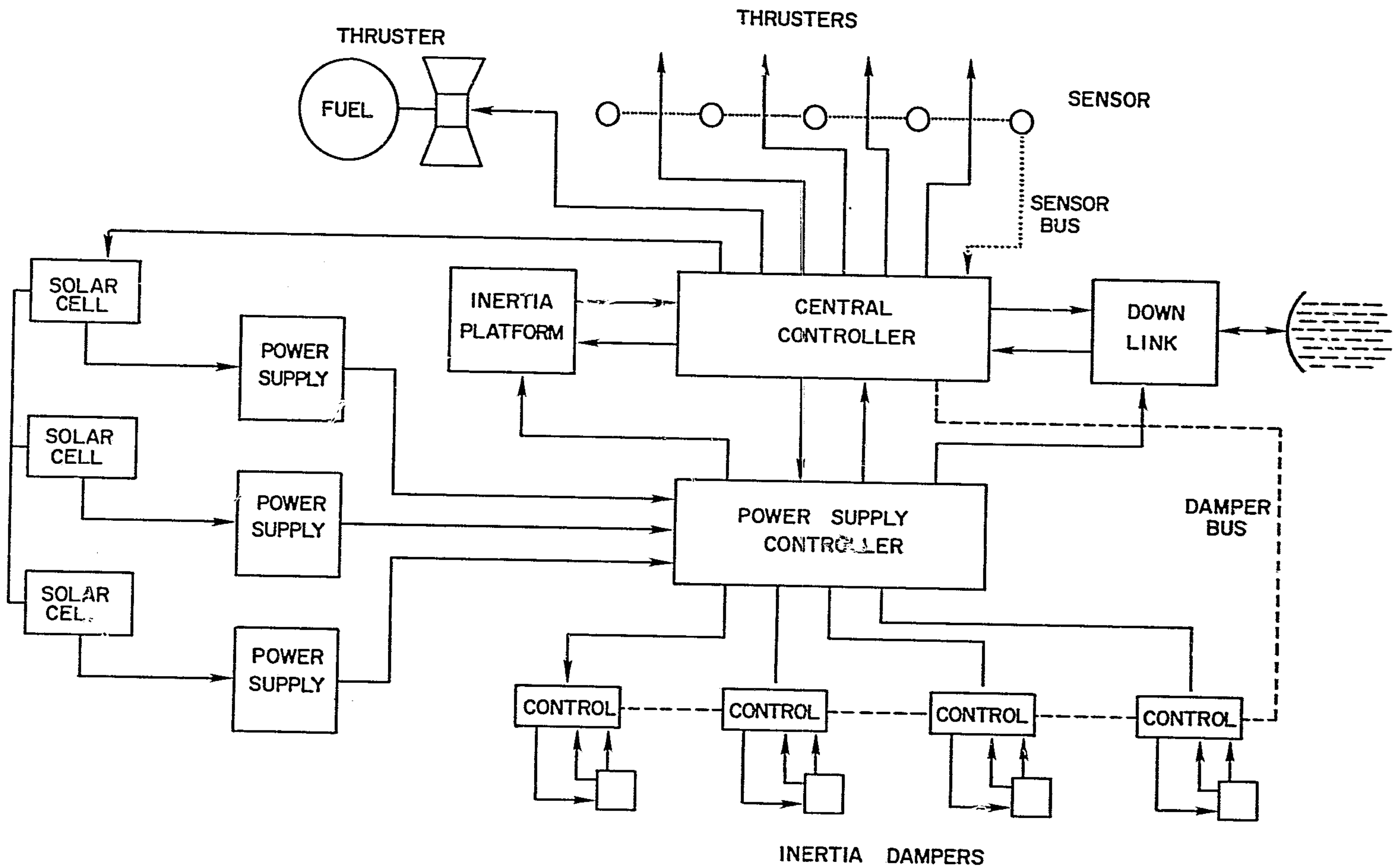


Figure 26. Hypothetical Control Configuration for Large Space Structure with Dampers.

SECTION VII

SUMMARY AND CONCLUSIONS

Summary

In summary, a digital controller has been developed for the linear proof-mass damper, based on a Z80 microcomputer. However, this development is regarded as an interim step, permitting an early look at control law problems, before the final development of a controller based on the INTEL 8051 microcontroller.

Although workable control programs have been developed for the Z80, it has proved difficult to develop a program which employs the full potential of the proof-mass damper.

Typically, the problem has been that there has been a poorly damped resonance of the proof-mass as a result of the virtual centering spring synthesized by the proximeter feedback. Accordingly, much of the recent effort has gone towards damping this mass.

Two approaches are now being tried. In one the signal from a velocity transducer is used as a rate feedback to damp the proof-mass. In the other, a rate feedback is synthesized within the digital program.

Conclusions

(1) The linear proof-mass damper is a feasible concept.

(2) A digital control system can be used for this system.

(3) It may prove desirable to incorporate a velocity feedback into the system.

(4) There is no apparent reason why an 8051 based controller should not be feasible.

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