LinCom

FINAL REPORT

AUTONOMOUS INTEGRATED RECEIVE SYSTEM (AIRS)

REQUIREMENTS DEFINITION

VOLUME IV. FUNCTIONAL SPECIFICATION FOR THE PROTOTYPE AUTOMATED INTEGRATED RECEIVE SYSTEM (AIRS)

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AUGUST, 1984

TR-0884-8211

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1.0 SCOPE

This specification describes the functional requirements for the performance, design, and testing for the prototype Automated Integrated Receive System (AIRS) to be demonstrated for the TDRSS S-Band Single Access Return Link.

2.0 APPLICABLE DOCUMENTS

The following documents form a part of this specification to the extent specified herein. In the event of conflict between the documents referenced herein and the contents of this specification, the contents of this specification shall be considered a superseding requirement.

(a) S-805-1, "Performance Specification for Services Via the Tracking and Data Relay Satellite System," November 1976.

(b) STDN No. 101.2, "Tracking and Data Relay Satellite System (TDRSS) Users' Guide," Rev. 4, January 1980.

(c) HESD 10167, "Prime Item Product Function Specification for S-Band Single Access Return Equipment (SSARE)," Rev. C, February 1978.

(d) STDN No. 108, "PN Codes for Use with the TDRSS," December 1976.

3.0 REQUIREMENTS

3.1 Functional Requirements

The AIRS shall accept the 370 MHz IF output from the NASCOM IF configuration switch, perform data demodulation, provide a reconstructed carrier for Doppler measurement and, for PN spread data, provide PN code epochs for ranging measurements. Figure 3.1-1 illustrates the AIRS functional block diagram. The AIRS shall be able to support the following functions:

a. Acquire and track DG1 PN spread signals as described in Paragraph 3.2.3.2.3.

b. Perform coherent IF combining if required.

c. Acquire and track the suppressed carrier signal.

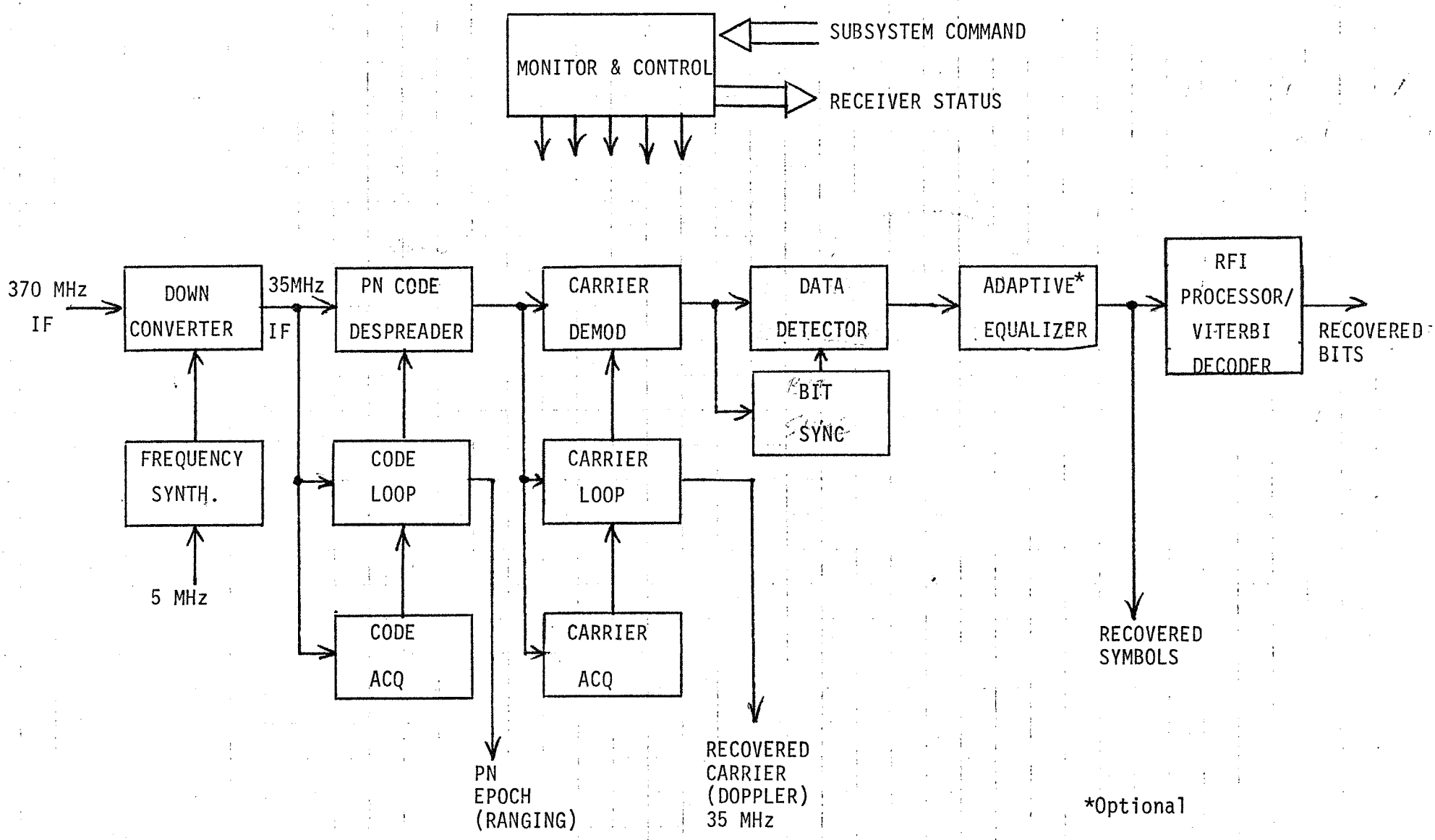

Fig. 3.1-1. AIRS Functional Block Diagram.

d. (Optional) Provide adaptive equalization for data rates > 6 Mbps (I or Q) for NRZ data and 3 Mbps (I or Q) for Bi-ϕ data.

e. Demodulate the data and perform baseband combining if required.

f. Provide RFI mitigation processing for convolutionally encoded data.

3.2 Performance Requirements

The AIRS shall acquire, demodulate, and decode the various signal modulation types defined herein and shall provide the specified output digital data within the bit error rate (BER) limits specified herein. Configuration control will be provided and state vectors or ephemerides data for static and dynamic Doppler correction will be supplied preceding each mission period.

3.2.1 General Requirements

3.2.1.1 Operational Modes

The AIRS shall be implemented to operate in the following operational modes:

a. Signal Acquisition Mode

b. Data Processing Mode

c. RARR Tracking Support Mode

These operational modes will be supported with appropriate static and dynamic setup and parameter commands. Each mode of operation shall conform to the definitions and restrictions in the following paragraphs.

3.2.1.1.1 Signal Acquisition Mode

The AIRS shall acquire the input signals defined in Table 3.2.1.1-1 in compliance with Paragraph 3.2.4 et seq requirements.

3.2.1.1.2 Data Processing Mode

The AIRS shall process the QPSK and BPSK modulated input signals

Table 3.2.1.1-1. AIRS Acquisition Mode Signal Characteristics.

DATA		I/Q POWER RATIO	MODULATION CHARACTERISTICS			C/N_O AND TIME CONSTRAINTS
GROUP	MODE		CW	BIT RATE	MODULATION INITIATED	
1	1 or 2	Any Specified	Never	Any Specified	Always Present	As defined in Para. 3.2.4.1
	3	4:1 to 1:1 1:1 to 1:2*				
	3	1:2*tol:4*	Never	Any for NRZ formats	Always Present	
				Any for Q channel		
				I Channel Biø formats <100Kb/s		
				100Kb/s to 150 Kb/s for I channel, biphase formats. Q Channel off	Q channel after I PN code lock status is sent to ADPE. I channel always present	
2	2 or 3	Any specified	Initially	<10kb/s coded, <20kb/s uncoded	After carrier lock status is sent to ADPE	As defined in Para. 3.2.4.1
			Never	≥10kb/s coded, ≥20kb/s uncoded	Always present	

Acquisition frequency conditions will be as defined in Paragraphs 3.2.3.5.1 and 3.2.3.5.2 (DG-1 only). *Q Channel will have higher C/N_O power.

defined in Paragarph 3.2.3 et seq over any TBD hour mission period in compliance with the following requirements as applicable:

Paragraph 3.2.5	Carrier Tracking
Paragraph 3.2.6	Data Extraction
Paragraph 3.2.7	I/Q Ambiguity Resolution
Paragraph 3.2.8	Data Format Conversion
Paragraph 3.2.10	Monitor and Status Signals

The AIRS shall demodulate data from two input data classes defined as Data Group 1 (DG-1) and Data Group 2 (DG-2). The normal characteristics of these data classes will be as summarized in Table 3.2.1.1-2.

DG-1 signals will be characterized by the use of staggered quadraphase PN (SQPN) spreading of I and Q channel data in Modes 1 and 2. DG-1 Mode 3 QPSK will have the I channel data PN spread and Q channel unspread. DG-1 I and Q channel data may be uncoded or convolutionally coded.

DG-2 signals will be characterized by unspread QPSK modulation in both Modes 2 and 3. DG-2 I and Q channel data may be uncoded or convolutionally coded.

3.2.1.1.3 RARR Tracking Support Mode

The AIRS shall provide a received carrier signal and detected PN epoch period pulse with PN clock to the RARR Equipment over any (3 hour) mission period in compliance with Paragraphs 3.2.5 et seq and 3.2.9 et seq requirements. The received carrier shall be provided from any of the input signals defined in Table 3.2.1.1-2 and the PN epoch and PN clock shall be provided from DG-1 Mode 1, 2 and 3 input signals.

3.2.1.2 Autonomous Operation

The AIRS shall be used primarily as a stand alone receiver during a

Table 3.2.1.1-2. Normal AIRS Input Data Configurations.

DATA GROUP	DATA MODE	RELATIONSHIP	I/Q POWER RATIO	SPREAD	CODED OR UNCODED	SOURCE CONDITIONS
1	1or2	Asynchronous QPSK	**1:4 to 1:1	SQPN	Either	Two Independent Sources
	3	Asynchronous QPSK	**1:4 to 1:1	I Channel only	Either	
2	1	D O E S N O T E X I S T				
	2or3	Asychronous QPSK	1:1 or 4:1*	None	Either	Two Independent Sources
	2or3	BPSK	N/A	None	Either	---

* I Channel will have higher C/N_o power.

** Q Channel will have higher C/N_o power.

user support period. However, it shall be capable of accomodating real time update interrupts regarding system reconfigurations and orbit changes.

3.2.1.2.1 Set-Up Data

The initial set-up data required for autonomous operation during user support period shall include:

(a) Doppler frequency predicts until the AIRS has acquired.

(b) Link Definition. This includes data group, mode, data format, coding/interleaving, data rates, signal level estimates, etc. If transmitted data characteristics are to be switched after link acquisition, this event epoch will be provided.

(c) RFI Scenario. RFI scenario will be provided to aid selecting the mitigation technique.

3.2.1.2.2 Real Time Updates

The AIRS shall be capable of accepting real time updates concerning reconfiguration of the AIRS during a user support period. This includes unscheduled orbit changes for which real time frequency predicts will be provided to AIRS at a rate of 9 samples per second.

3.2.1.2.3. Autonomous Operation

Based on the set-up data, the AIRS shall be capable of automatically configuring the receiver hardware/software to achieve the desired mode of configuration. The AIRS shall, based on (a) initial set-up data and (b) monitor signals during normal data operation, select the following:

(a) IF filter bandwidths

(b) Loop order and bandwidths for PN and carrier tracking, and bit synchronization

Table 3.2.2.3-1. SSARE IF Channel Characteristics.

	PARAMETER	SPECIFICATION
1.	Noise Figure	$\leq$20 dB
2.	Amplitude Response	
	a. Flatness over $\pm$5MHz about F_{IF}*	$\leq \pm$0.45 dB
	b. 3 dB bandwidth	12MHz$\leq$BW$\leq$22 MHz
3.	Phase Nonlinearity over $\pm$3.5 MHz about F_{IF} *	$\leq \pm 2.60^{o}$
4.	Nonlinear Distortion	
	a. AM/AM	$\leq$1.0 dB/dB
	b. AM/PM	$\leq 0.59^{o}$/dB
5.	Signal Gain	
	a. Center Frequency	40 $\pm$1 dB
	b. Short term stability	$\leq \pm$0.05 dB/minute
	c. Long term stability	$\leq \pm$1.0 dB/24 hours
6.	Inband spurious power added relative to maximum output signal level**	
	a. Total power in $\pm$5MHz band about F_{IF}	-30 dBc minimum
	b. Discrete spectral lines	-40 dBc minimum
7.	Out of Band Rejection	
	a. Input image band relative to maximum output signal level	$\geq$40 dBc
	b. 25 dB rejection BW	$\leq$30 MHz centered @F_{IF}
	c. 45 dB rejection BW	$\leq$40 MHz centered @F_{IF}
8.	LO leakage (including harmonics) to Antenna	$\leq$-60 dBm
9.	Phase Noise added to carrier	
	a. 1-10 Hz	$\leq 0.70^{o}$ rms
	b. 10-100 Hz	$\leq 1.20^{o}$ rms
	c. 100-1000 Hz	$\leq 1.00^{o}$ rms
	d. 1 KHz-6 MHz	$\leq 1.20^{o}$ rms
10.	Maximum S + N output level	+6 dBm

* TDRS Equalizer in the bypassed state.

** During maximum SSARE input signal levels.

(c) Acquisition strategy

(d) Tracking configuration

(e) Reacquisition procedure

(f) RFI mitigation technique

(g) Data conditioning

(h) Adaptive equalization

(i) Frequency-aiding

(j) Others

3.2.1.2.4 Configuration Modes

The AIRS shall operate in three distinct configuration modes--the normal mode (NM), the flexible data format mode (FDM) and the test mode (TM).

3.2.1.2.4.1 Normal Mode

In this mode the receiver configures itself automatically and selects the receiver parameters to achieve optimum performance based on preselected user data characteristics.

3.2.1.2.4.2 Flexible Data Format Mode

In this mode the receiver configures itself automatically and selects the receiver parameters to accomodate flexibility in the user data characteristics.

3.2.1.2.4.3 Test Mode

In this mode the receiver configuration and its parameters are selected via external real time serial data interface (e.g. GPIB). In the test mode, the AIRS is then a general purpose dual channel spread spectrum BPSK/QPSK receiver.

3.2.2 IF Channel Characteristics

The IF input shall be the existing SSA Return Equipment (SSARE) IF

Output which will comply with the following requirements. Channel characteristics from user source will be defined in Paragraph 3.2.3.4.

3.2.2.1 TDRS Channel Equalization

3.2.2.1.1 TDRS Distortion Equalizer Performance

Residual distortion level will be $\leq \pm 0.1$dB (over ± 5 MHz about F_c) at the IF Configuration Switch Input. Equivalent residual phase variation level will be $\leq \pm 1.0^o$ (over ± 3.5 MHz about F_c) at the IF Configuration Switch Input.

3.2.2.2 IF Carrier Characteristics

3.2.2.2.1 Center Frequency

The IF Channel carrier center frequency (F_{IF}) will be 370 MHz $\pm$ 530 KHz for the SSA-1 or -2 input frequency uncertainties defined in Paragraph 3.2.3.5.1.

3.2.2.2.2 Phase Noise

The phase noise added to the IF Channel carrier by the SSARE will not exceed the levels defined in item 9 of Table 3.2.2.3-1.

3.2.2.2.3 Incidental AM

The incidental AM added to the IF Channel carrier by the SSARE will not exceed (TBD) %.

3.2.2.3 Channel Characteristics

The IF Channel characteristics will comply with the values listed in Table 3.2.2.3-1.

3.2.3 Input Signal Characteristics

3.2.3.1 Input Data Configurations

The AIRS shall process the input signal configurations listed in Tables 3.2.1.1-2 and 3.2.3.2-1 as defined herein. Normal DG-1 and DG-2 QPSK signals will have independent and asynchronous data from two

Table 3.2.3.2-1. Special AIRS Input Data Configurations (Single Data Source Conditions).

SPEC SUBP	SPECIAL CONFIG.	DATA GROUP	DATA MODE	I, Q DATA RELATIONSHIP	I/Q POWER RATIO	PN SPREAD	CODED OR UNCODED	SOURCE CONDITIONS
(a)	A	1	1 or 2	Synchronous QPSK	Equal	SQPN	Either but I & Q channels identical	Identical data on I&Q channels
(b)	B (NOTE 1)	1	1 or 2	Synchronous QPSK	Unequal	SQPN	Either	Identical data on I&Q channels
(c)	CI	1	1 or 2	I Channel BPSK	N/A	Yes	Either	USC Q Modulator failure
	CQ	1	1 or 2 (Mode 3 Note 2)	Q Channel BPSK	N/A	Yes	Either	USC I Modulator failure
(d)	D	2	2 or 3	Staggered QPSK	Equal	None	Uncoded* I&Q channels	Alternate bits on I&Q channels which are staggered by ½ symbol period
(e)	E	2	2 or 3	Staggered QPSK	Equal	None	Coded I&Q channels	Two concurrent encoder bits on I&Q channels which are staggered by ½ symbol period

Table 3.2.3.2-1. (continued).

SPEC SUBP	SPECIAL CONFIG.	DATA		I,Q DATA RELATIONSHIP	I/Q POWER RATIO	PN SPREAD	CODED OR UNCODED	SOURCE CONDITIONS
		GROUP	MODE					
(f)	FI	1	1 or 2 or 3	QPSK, zero Q data modulation	Any specified*	Yes	Either	PN Spread (except Mode 3) Q channel carrier present
	FQ	1	1 or 2 or 3	QPSK, zero I data modulation	Any specified*	Yes except Mode 3	Either	PN spread I channel carrier present
(g)	GI	2	2 or 3	QPSK, zero Q modulation	Any specified*	None	Either	Q channel carrier present
	GQ	2	2 or 3	QPSK, zero I modulation	Any specified*	None	Either	I channel carrier present

Note 1: Special SSARE Input Data Configuration B above is defined only for the case for which the high powered channel has sufficient EIRP to support the minimum C/N_0 requirements for the channel data rate.

Note 2: Mode 3 with I channel absent looks like DG-2 BPSK.

Table 3.2.3.2-2. Bit Rate and Modulation Characteristics.

	DG-1				DG-2
	MODE 1	MODE 2	MODE 3		Mode 2,3
	I,Q Channel	I,Q Channel	I Channel	Q Channel	I,Q Channel
Data Modulation	MODULO 2 ADDED ASYNCHRONOUSLY TO PN CODE		Same as Mode 1,2	BPSK $\pm\pi/2$	QPSK
Bit Rate: Uncoded NRZ	100b/s to 300Kb/s	1Kb/s to 300Kb/s	100b/s to 300Kb/s	1Kb/s to 6 Mb/s	1Kb/s to 6 Mb/s
Bit Rate: Coded NRZ,(Rate 1/2), Uncoded Biø	100b/s to 150 Kb/s	1Kb/s to 150Kb/s	100b/s to 150Kb/s	1Kb/s to 3 Mb/s	1Kb/s to 3 Mb/s
Bit Rate: Coded Biø,(Rate 1/2)	100b/s to 75Kb/s	1Kb/s to 75Kb/s	100b/s to 75Kb/s	1Kb/s to 1.5Mb/s	1Kb/s to 1.5Mb/s
Bit Rate: Coded NRZ (Rate 1/3)	N/A	N/A	N/A	1Kb/s to 2 Mb/s	1 Kb/s to 2 Mb/s (I only)
Bit Rate: Coded Biø (Rate 1/3)	N/A	N/A	N/A	1 Kb/s to 1 Mb/s	1 Kb/s to 1 Mb/s (I only)

sources on the I and Q channels.

3.2.3.2 Data and PN Code Characteristics

3.2.3.2.1 Bit Rates

The SSA signal modulation and bit rates will conform to Tables 3.2.1.1-2, 3.2.2.1-1, 3.2.3.2-2 and the following conditions:

a. When I and Q channel data sources are independent, the sum of the data rates on the I and Q channels will not exceed 600 Kb/s for DG-1 Modes 1 or 2, 12.3 Mb/s for DG-1 Mode 3 or 24 Mb/s for DG-2 Modes 2 or 3.

b. All bit rates will be defined to ±0.1% accuracy.

3.2.3.2.2 Data Formats and Convolutional Coding

a. DG-1 and DG-2 data when coded will be convolutionally encoded (constraint length 7) at either rate 1/2 or rate 1/3.

b. Uncoded data format will be NRZ-L, M, S or Bi ϕ-L, M, S; convolutionally coded data format will be NRZ-L, M, S. The output of the convolutional encoder may be NRZ to Bi ϕ-L converted.

3.2.3.2.3 PN Coding

The DG-1 QPSK and BPSK signals will be spread with PN codes which conform to the Table 3.2.3.2-3 characteristics and the following conditions:

a. The DG-1 Mode 1 Q channel code will be identical to the Mode 1 I channel code.

b. The DG-1 Mode 2 I and Q channel codes will be different User Code Assignments from STDN 108.

c. The PN chip rate (F_{PN}) will be defined in Pragraph 3.2.3.5.2(a).

Table 3.2.3.2-3. DG-1 PN Coding Characteristics.

PARAMETER	MODE	CHANNEL	CHARACTERISTIC
PN Modulation	1, 2	I, Q	SQPN
	3	I	PSK, $\pm$ 90°
	3	Q	N/A
PN Code Lengths	1	I, Q	$(2^{10}-1)$x256 chips
	3	I	
	2	I, Q	$2^{11}-1$ chips
PN Code Epoch Reference	1, 3	I	All ONES code condition*
	1	Q	All ONES condition delayed by (x+½) chips relative to the I channel epoch. x will be as defined in column 5 of Table 1 of STDN 108.
	2	I	Spacecraft Oscillator
	2	Q	Delayed ½ chip period relative to the I channel code phase.
PN Code Family	1	I, Q	Mode 1 and 3 Return Link Codes as defined in Para. 2.2.3 of STDN 108.
	3	I	
	2	I, Q	Mode 2 Return Link Codes as defined in Para. 2.2.4 of STDN 108.

* The all ONES condition will be synchronized to the all ONES condition of the User S/C received forward link range code.

3.2.3.2.4 Baseband Data

Within any sequence of 512 symbols, the number of transitions will be $\geq$ 64 and the maximum number of consecutive symbols without a transition will be $\leq$ 64.

3.2.3.3 Adaptive Equalizer Mode

When the data rate for DG-1 Mode 3 I or DG-2 I or Q exceed 12 Ms/s (NRZ) or 6 Ms/s (bi-ϕ), adaptive equalization shall be employed with data detection.

3.2.3.4 Channel Characteristics From User Source

The baseband, RF and IF distortions in the SSA-1 or SSA-2 signal channels from the data source on the User Spacecraft to the AIRS input will be the cascade of distortions as defined in the following paragraphs.

3.2.3.4.1 User Baseband Distortion

The user baseband signal distortions will not exceed the values listed in Table 3.2.3.4-1 for the applicable data modes and data configurations.

3.2.3.4.2 TDRS RF Distortion

The TDRS Spacecraft RF signal distortions will not exceed the values listed in Table 3.2.3.4-2 for any data mode or data configuration. The TDRS SSA channel bandwidth will be equivalent to a 5-pole Butterworth filter cascaded with a 3-pole Chebyshev filter with one dB ripple, both with 16.5 MHz 3-dB bandwidth.

3.2.3.4.3 Ground Segment Antenna Distortion

The ground segment Ku-Band Antenna component RF signal distortions will not exceed the values listed in Table 3.2.3.4-3 for any data mode or data configuration.

Table 3.2.3.4-1. User Baseband Signal Distortions.

ITEM	PARAMETER	SSAR PEAK	SSAR RMS	APPLICABLE NORMAL DATA MODES DG-1	APPLICABLE NORMAL DATA MODES DG-2	APPLICABLE SPECIAL DATA CONFIGURATIONS[3]
1.	Data Asymmetry	$\leq \pm 3\%$	$\leq 1.73\%$	1,2,3	2,3	all
2.	Modulator Phase Imbalance (BPSK only)	$\leq \pm 3^{o}$	N/A	None	2,3	C
3.	Modulator Gain Balance	$\leq \pm 0.25$dB	N/A	1,2,3	2,3	all
4.	Relative Phase Between I & Q Channels (Relative to 90^{o})	$\leq \pm 3^{o}$	$\leq 1.73^{o}$	1,2,3	2,3	A,B,D,E
5.	Data Transition Time (90% of initial state to 90% of final state)	$\leq$5% of bit time but not less than 17 ns	$\leq$2.88% of bit time but not less than 17 ns	1,2,3	2,3	all
6.	PN Chip Jitter (Phase)					
	a. To meet tracking rqmts	N/A	$\leq 1^{o}$	1,3I	None	ABC Mode 1
	b. To meet BER rqmts	$\leq \pm 4\%(\pm 14.4^{o})$	$\leq 2.31\%(8.31^{o})$	1,2,3I	None	A,B,C
7.	Noncoherent Mode Frequency					
	a. 1 sec average time	$\leq \pm 3\times10^{-9}$	$\leq 1.73\times10^{-9}$	2	2	All Mode 2
	b. 5 hr average time	$\leq \pm 1\times10^{-7}$	$\leq 5.8\times10^{-8}$	2	2	All Mode 2
	c. 48 hr average time	$\leq \pm 3\times10^{-7}$	$\leq 1.73\times10^{-7}$	2	2	All Mode 2
8.	I/Q Data Skew	$\leq \pm 3\%$	$\leq 1.73\%$	None	None	A,B
9.	I/Q PN Skew (Relative to 0.50 chip)	$\leq$0.01 chip	$\leq$0.006	1,2	None	A,B

Table 3.2.3.4-1. User Baseband Signal Distortions (cont'd).

ITEM	PARAMETER	SSAR PEAK	SSAR RMS	APPLICABLE NORMAL DATA MODES DG-1	APPLICABLE NORMAL DATA MODES DG-2	APPLICABLE SPECIAL DATA CONFIGURATION
10.	PN Asymmetry	≤0.01 chip	≤0.006	1,2,3I	None	A,B,C
11.	PN Chip Rate, Mode 2 (Relative to Absolute Coherence with Carrier Rate)	≤0.01 Hz at PN Rate	≤0.006	2[1]	None	A,B,C Mode 2
12.	Data Bit Jitter[2]					
	a. To meet BER rqmts					
	•Coded biphase data (20Kb/s to 3 Mb/s)	≤ ±0.5%	≤0.29%	1,2,3	2,3	A,B,C,E
	•All Other Data	≤ ±0.1%	≤0.06%	1,2,3	2,3	all
	b. To Meet BSR rqmts Per Para. 3.2.1.6.2					

NOTES:

1. Becomes applicable only if PN code and Carrier Tracking Loops are slaved together.
2. Indicated percentages are the user spacecraft peak clock frequency jitter and peak jitter rate (sinusoidal or 3σ random) as percent of the symbol rate. Bit jitter rates >0.1% peak only apply to biphase data format. Bit jitter refers to symbol jitter when the data is coded. BSR is the bit slippage
3. Special data configurations as defined in paragraph 3.2.3.2.

Table 3.2.3.4-2. TDRS Spacecraft RF Signal Distortions.

ITEM	PARAMETER	S S A R PEAK	S S A R RMS
1.	Composite Phase Noise at TDRS Output[1]		
	a. USC Noncoherent Modes[2]		
	1Hz-10Hz	N/A	$\leq 2.7^{o}$
	10Hz-32Hz	N/A	$\leq 2.7^{o}$
	32Hz-1KHz	N/A	$\leq 2.7^{o}$
	1KHz-6MHz	N/A	$\leq 2.0^{o}$
	b. USC Coherent Modes[2]		
	1Hz-10Hz	N/A	$\leq 2.7^{o}$
	10Hz-1KHz	N/A	$\leq 4.0^{o}$
	1KHz-6MHz	N/A	$\leq 2.0^{o}$
2.	Amplitude Flatness[3]		
	Unequalizable Ripple	$\leq \pm 0.28$ dB	N/A
3.	Phase Linearity[3]		
	Unequalizable Ripple	$\leq \pm 2.8^{o}$	$\leq 1.6^{o}$
4.	AM/PM Distortion	$\leq 3.0^{o}$/dB	N/A
5.	AM/AM Distortion	$\geq$0.9dB/dB	N/A

NOTES:

1 Includes root sum square of USC and TDRS phase noise spectra.

2

	DG-1	DG-2
USC NON COHERENT MODES	2	2
USC COHERENT MODES	1,3	3

3 Includes Ground Segment equalization. Applies over ± 3.5 MHz about center frequency.

Table 3.2.3.4-3. GS Ku-Band Antenna RF Signal Distortions.

ITEM	PARAMETER	SSAR PEAK	SSAR RMS
1.	Phase Noise Added to Carrier		
	1Hz-10Hz	N/A	$\leq 1.10^{o}$
	10Hz-100Hz		$\leq 0.50^{o}$
	100Hz-1KHz		$\leq 0.80^{o}$
	1KHz-6MHz		$\leq 0.90^{o}$
2.	Amplitude Flatness over $\pm$5MHz about Center Frequency	$\leq \pm 0.70$ dB	N/A
3.	Phase Linearity over $\pm$3.5 MHz about Center Frequency	$\leq \pm 1.50^{o}$	$\leq 0.87^{o}$
4.	Total Added Spurious Power in $\pm$10 MHz Band about Center Frequency[1]	$\leq$-41.6 dBc	$\leq$-44.0 dBc
5.	Incidental and Tracking AM (25-400 bps PRN)	$\leq \pm 0.5\%$	$\leq 0.29\%$
6.	Nonlinear Distortion		
	a. AM/PM	$\leq 0.59^{o}$/dB	N/A
	b. AM/AM	T B D dB/dB	N/A

N O T E : [1]Total spurious is relative to total carrier plus modulation power (not carrier alone).

3.2.3.4.4 SSARE RF/IF Distortion

The SSARE RF/IF generated signal distortions will not exceed the values listed in Table 3.2.3.4-4 for any data mode or data configuration.

3.2.3.5 Carrier Frequency and PN Chip Rate Uncertainty

Carrier frequency and PN chip rate residual errors are based on the accuracy of the supplied orbit state vector or ephemerides assuming a ±9 sec time uncertainty. The unstable user spacecraft dynamics are based on a worst case acceleration of 50 m/s^2 with no explicit limit on jerk.

3.2.3.5.1 Frequency Uncertainty - Carrier

a. Tuning Range--The AIRS shall have a tuning range (Δf_c) about the specified F_c. This tuning range shall be ±530 KHz in order to correct for known frequency offsets of ±300 KHz maximum and Doppler offsets as defined below.

b. Doppler Frequency Shifts--The maximum frequency offsets of F_c due to Doppler shifts will not exceed the following values:

COHERENT USER MODES (Two Way Doppler): ±230 KHz

DG-1 Modes 1,3

DG-2 Mode 3

NONCOHERENT USER MODES (One Way Doppler): ±115 KHz

DG-1 Mode 2

DG-2 Mode 2

c. Frequency Rate of Change ($\dot{f}_c$) --The maximum Doppler frequency rate of change of F_c will not exceed the following values:

COHERENT USER MODES (Two Way Doppler):

Acquisition Mode: ±765 Hz/second

RARR Tracking Support Mode: ±1.5 KHz/second

Table 3.2.3.4-4. Ground Segment SSARE RF/IF Signal Distortions.

ITEM	PARAMETER	SSAR PEAK	SSAR RMS
1.	Phase Noise added to Carrier		
	1Hz-10Hz	N/A	$\leq 0.70^{\circ}$
	10Hz-100Hz	N/A	$\leq 1.20^{\circ}$
	100Hz-1KHz	N/A	$\leq 1.00^{\circ}$
	1KHz-6MHz	N/A	$\leq 1.20^{\circ}$
2.	Amplitude Flatness over ± 5 MHz about Center Frequency		
	a. Downconverter Unit	$\leq \pm 0.25$dB	N/A
	b. Conv/Corrector Unit	$\leq \pm 0.10$dB	N/A
	c. TDRS Unequalized Residual	$\leq \pm 0.10$dB	N/A
3.	Phase Linearity over ± 3.5 MHz about Center Frequency		
	a. Downconverter Unit	$\leq \pm 1.80^{\circ}$	$\leq 1.05^{\circ}$
	b. Conv/Corrector Unit	$\leq \pm 0.20^{\circ}$	$\leq 0.12^{\circ}$
	c. TDRS Unequalized Residual	$\leq \pm 1.00^{\circ}$	$\leq 0.58^{\circ}$
4.	Total Added Spurious Power in ± 10 MHz Band about Center Frequency[1]	$\leq$-40.6dBc	$\leq$-43dBc
5.	IF Bandwidth		
	a. 1 dB down	TBD	N/A
	b. 3 dB down	TBD	N/A
	c. 60 dB down	TBD	N/A
	d. Composite Poles	TBD	N/A
6.	Nonlinear Distortion		
	a. AM/PM	$\leq 0.1^{\circ}$/dB	N/A
	b. AM/AM	1.0dB/dB	N/A

N O T E S: [1] Total spurious power is relative to total carrier plus modulation power (not carrier alone).

Data Processing Mode: ±800 Hz/second

NONCOHERENT USER MODES (One Way Doppler)

Acquisition Mode: ±383 Hz/second

RARR Tracking Support Mode: ±750 Hz/second

Data Processing Mode: ±400 Hz/second

d. Frequency Acceleration ($\ddot{f}_c$)

COHERENT USER MODES:

Acquisition Mode: ±30.6 Hz/second^2

Data Processing and RARR Tracking Support Mode:

Stable Orbit: ±30.6 Hz/s^2

Unstable Orbit: $\int_t^{t+9} |\ddot{f}_c| dt < 765$ Hz/s

NONCOHERENT USER MODE:

Acquisition Mode: ±16.6 Hz/s^2

Data Processing and RARR Tracking Support Mode:

Stable Orbit: ±16.6 Hz/s^2

Unstable Orbit: $\int_t^{t+9} |\ddot{f}_c| dt < 383$ Hz/s

e. Residual Frequency Error--The frequency error of the Doppler correction provided to the AIRS will not exceed:

	Doppler Error	Doppler Rate	Doppler Acceleration
Coherent User Modes:	Δf Hz	$\Delta \dot{f}$ Hz/sec	$\Delta \ddot{f}$ Hz/sec^2
Acquisition Mode	±2,200	±2.5	±.002
RARR Tracking & Data Processing Mode			
Stable Orbit	±2,200	±28	±3.1
Unstable Orbit	±10,300	±765	$\int_t^{t+9} \lvert\Delta \ddot{f}\rvert dt < 765$ Hz/s

Noncoherent User Modes:

Acquisition Mode A	1,900*	±8.5	±.001
Acquisition Mode B	4,200**	±8.5	±.001
RARR Tracking and Data Processing Mode			
Stable Orbit	±4,200**	±14	±1.55
Unstable Orbit	±8,800**	±383	$\int_{t}^{t+9} \lvert \Delta\ddot{f} \rvert dt \leq 383$ Hz/s

*User Spacecraft Tuning Error = 700 Hz (Mode 2A)
**User Spacecraft Tuning Error = 3,000 Hz (Mode 2B)

3.2.3.5.2 PN Chip Rate Code Uncertainty

a. Tuning Range--The AIRS shall have a PN code rate tuning range of ±67.9 Kchips/second about the center chip rate of F_{PN} = 3.028 Mchips/second. This tuning range includes ±64.5 Kchips/second variation due to TDRS channelization plus Doppler shifts.

b. Doppler Chip Rate Shift--The Doppler frequency shift of the PN code rate on the received SSAR signals will not exceed the following values:

DG-1 Mode 1 and 3: ±309 chips/second

DG-2 Mode 2: ±154 chips/second

c. PN Rate of Change and Acceleration--The PN code rate of change and acceleration on the received SSAR signals will not exceed the following values:

	$\dot{f}_{PN}$ (chips/s^2)	$\ddot{f}_{PN}$ (chips/s^3)
Stable Orbit:		
DG-1 Mode 1 and 3:	±2	±.04
DG-1 Mode 2:	±1	±.02
For Unstable Orbit:		
DG-1 Mode 1 and 3	±2	$\int_t^{t+9} \lvert \ddot{f}_{PN} \rvert dt < 1.12$ chips/s^2
DG-1 Mode 2	±1	$\int_t^{t+9} \lvert \ddot{f}_{PN} \rvert dt < 0.56$ chips/s^2

d. Residual Chip Rate Error--The chip rate error of the chip rate correction provided to the AIRS will not exceed:

	Chip Rate Error Δf_{PN} chips/sec	Error Rate $\Delta\dot{f}_{PN}$ chips/sec^2	Acceleration $\Delta\ddot{f}_{PN}$ chips/sec^3
Coherent DG-2 Modes 1 and 3:			
Acquisition Mode	±3.0	±.0033	±.26x10^{-5}
RARR Tracking & Data Processing Mode			
Stable Orbit	±3.0	±.0378	±.0042
Unstable Orbit		±13.9	±1.02
$\int_t^{t+9} \lvert \Delta\ddot{f}_{PN} \rvert dt$			< 1.02 chips/sec^2
Noncoherent DG-1 Mode 2:			
Acquisition Mode	±5.7	±.011	±.13x10^{-5}

RARR Tracking & Data Processing Mode			
Stable Orbit	±5.7	±0.0189	±0.0021
Unstable Orbit		±12.6	$\int_{t}^{t\pm951} \lvert \ddot{\Delta f}_{PN} \rvert dt$ < 0.51 chips/sec^2

e. PN Code Epoch Timing Uncertainty--The maximum PN code epoch timing uncertainty between the received PN code state and the Acquisition Mode setup value will not exceed the following values:

DG-1 Modes 1 and 3: ±1900 chips

DG-1 Mode 2: 2047 chips

3.2.3.6 Input Signal Level

TBD based on IF channel interface characteristics.

3.2.3.7 Data Processing C/N_0 Values

The minimum carrier to noise density ratio (C/N_0) of the AIRS input signal for specified BER performance, will be as defined by the following equations as a function of the bit rate (BR). The values apply to the I or Q channels carrier-to-noise ratio and the channel bit rates.

a. UNCODED FORMAT (DG-1,DG-2)	C/N_0 Minimum
NRZ-L, Bi ϕ-L	13.1+10 log(BR)dB-Hz
NRZ-M, Bi ϕ-M,S	13.4+10 log(BR)dB-Hz
b. CODED FORMAT (DG-1, DG-2)	
NRZ-L, Bi ϕ-L	8.1+10 log(BR)dB-Hz
NRZ-M, S	8.2+10 log(BR)dB-Hz

c. DG-1 IDENTICAL I AND Q DATA

For DG-1 Modes 1 and 3 when receiving identical synchronous data on the I and Q channels and for which the I and Q channel power division is balanced (special data configuration A), I and Q channel C/N_0 value will be 3 dB less than defined in (a) and (b) above.

d. C/N_0 VARIATION RATE

The variation rate of C/N_0 will not exceed ±10 dB/second for all data modes.

3.2.3.8 Unbalanced I/Q Power Conditions

The SSARE will receive DG-1 and DG-2 signals having unbalanced I and Q channel powers of up to 4 to 1 ratio as defined in the following paragraphs. The I/Q power ratio will be defined and provided to the AIRS with an accuracy of ±0.4 dB relative to the actual received signal power ratio.

3.2.3.8.1 DG-1 I/Q Power Unbalance

For unbalanced I and Q data rate conditions, the I/Q power ratio will vary as defined in Table 3.2.1.1-2. The minimum C/N_0 of each channel (I or Q) will be consistent with the minimum C/N_0 requirements defined in Paragraph 3.2.3.7 for each channel's data rate.

3.2.3.8.2 DG-2 I/Q Power Unbalance

DG-2 signals will have an I/Q power ratio of either 1:1 or 4:1 consistent with the C/N_0 for the data rate of each channel as defined in 3.2.3.7. The I channel will have the higher power at the 4:1 ratio.

3.2.3.9 RFI Degradation

The AIRS shall incorporate RFI mitigation techniques for coded data. The performance improvement shall be no less than (TBD) dB.

3.2.4 Signal Acquisition

The AIRS shall acquire the SSAR signal under the conditions specified in the following paragraphs within the specified acquisition times with a probability of correct acquisition of 0.9 or greater. For DG-1 modes time to acquire specifications include PN code acquisition.

3.2.4.1 SSAR Return Acquisition

The AIRS shall complete all of the following SSAR acquisition and synchronization activities within the defined time limits for I and Q C/N_0 values defined in Figures 3.2.4-1, 3.2.4-2, and 3.2.4-3.

3.2.4.1.1 PN Code and Carrier

The AIRS shall acquire the I and Q received data channel PN code and carrier signals within the time intervals specified in Table 3.2.4.1-1 and as defined in Figures 3.2.4-1, 3.2.4-2, and 3.2.4-3 after application of the input signal. Probability of acquisition under the specified conditions shall be $\geq$ 90%.

3.2.4.1.2 Bit Sync Acquisition

The AIRS shall achieve Bit Sync Lock within 2,000 symbol periods at 90% probability after application of the input signal for all signal conditions specified herein.

3.2.4.1.3 Decoder Acquisition

The equipment shall obtain branch synchronization in $\leq$ 2000 bit times at a 90% confidence level when convolutionally coded input signals are present. When the encoded symbols are interleaved, the acquisition time shall be $\leq$ 60,000 bit times.

3.2.4.2 False Lock Protection

The following requirements apply for the specified received signal levels:

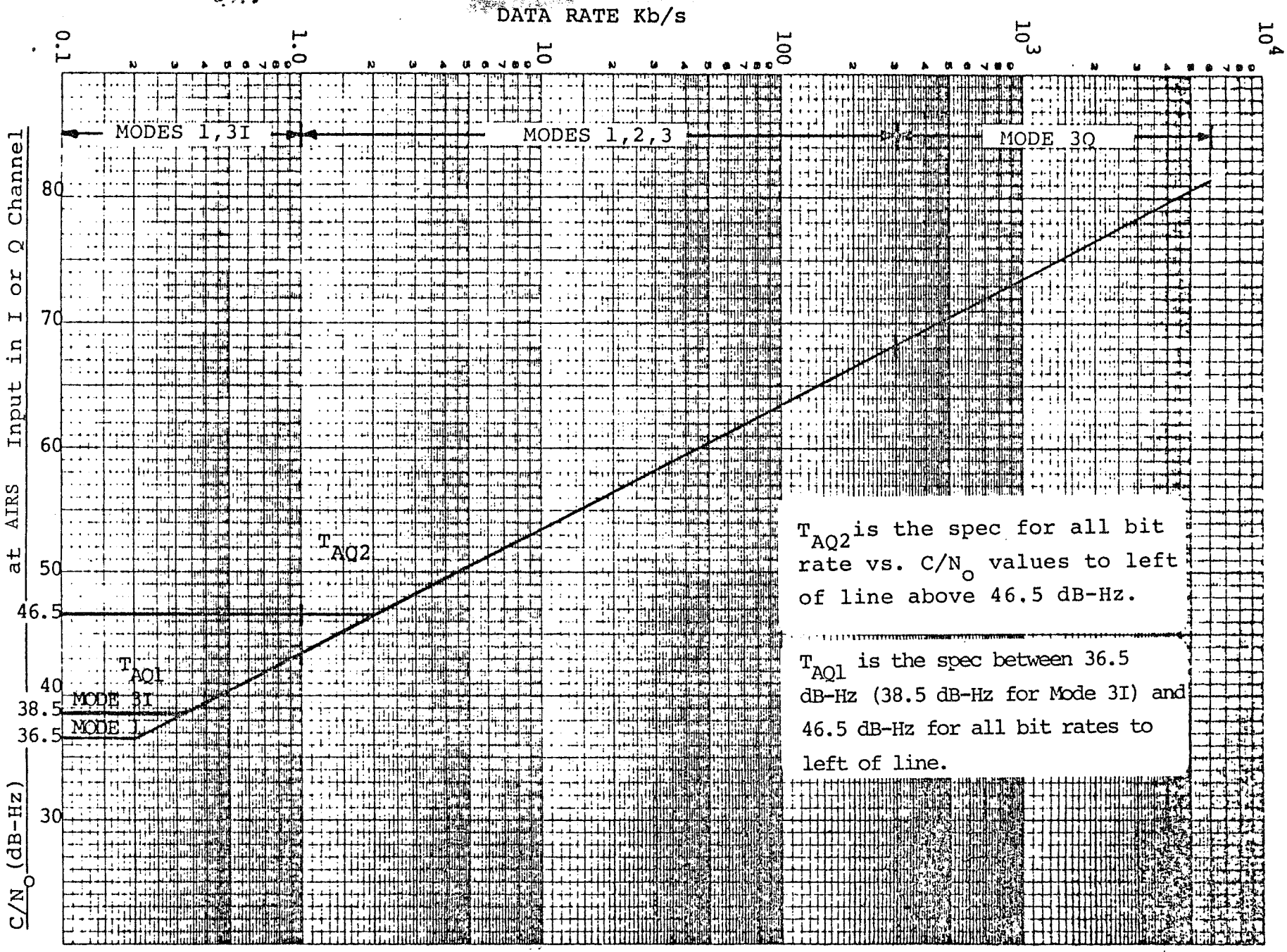

Figure 3.2.4.1-1. DG-1 Uncoded Data Acquisition Spec.

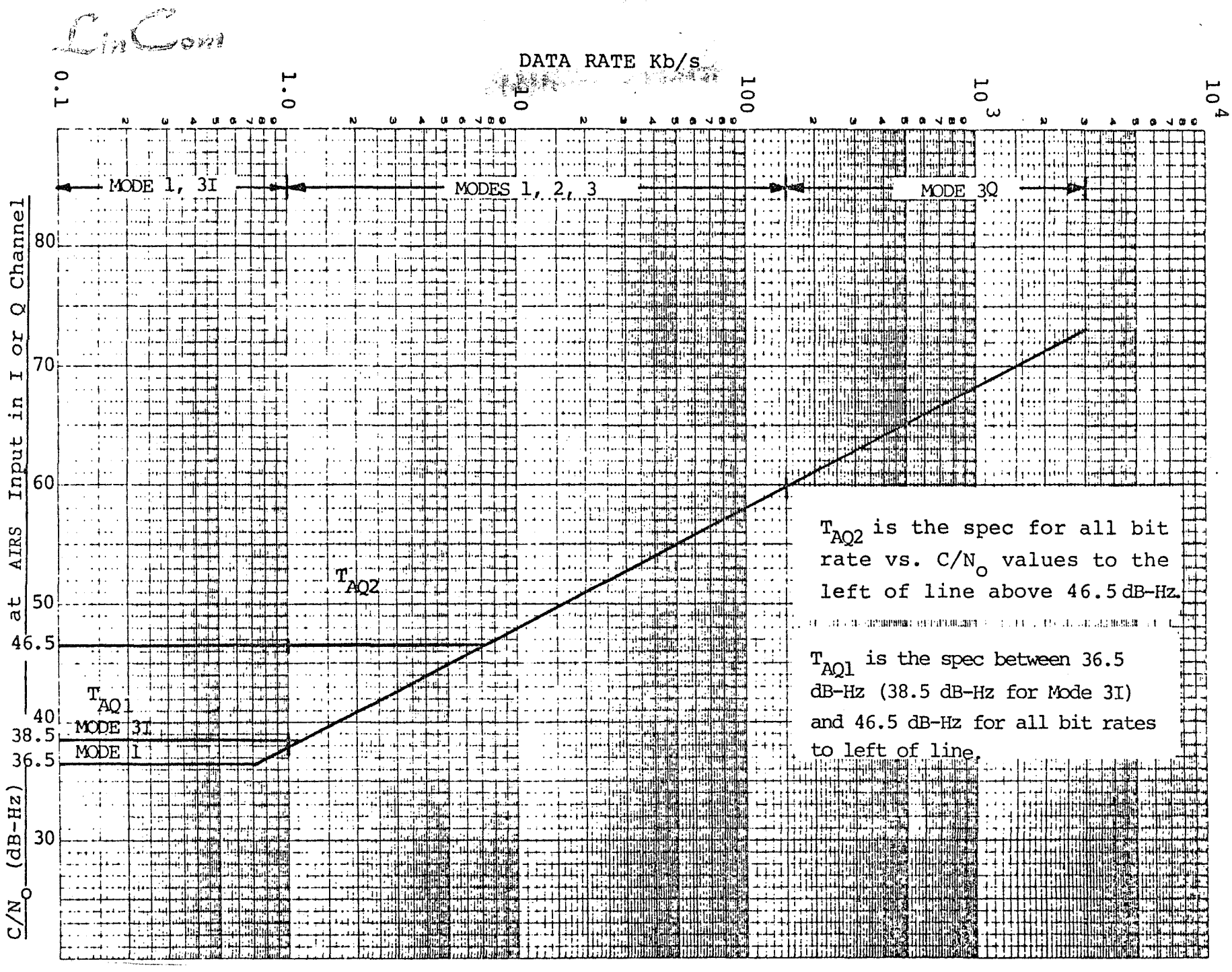

Figure 3.2.4.2-2. DG-1 Coded Data Acquisition Spec.

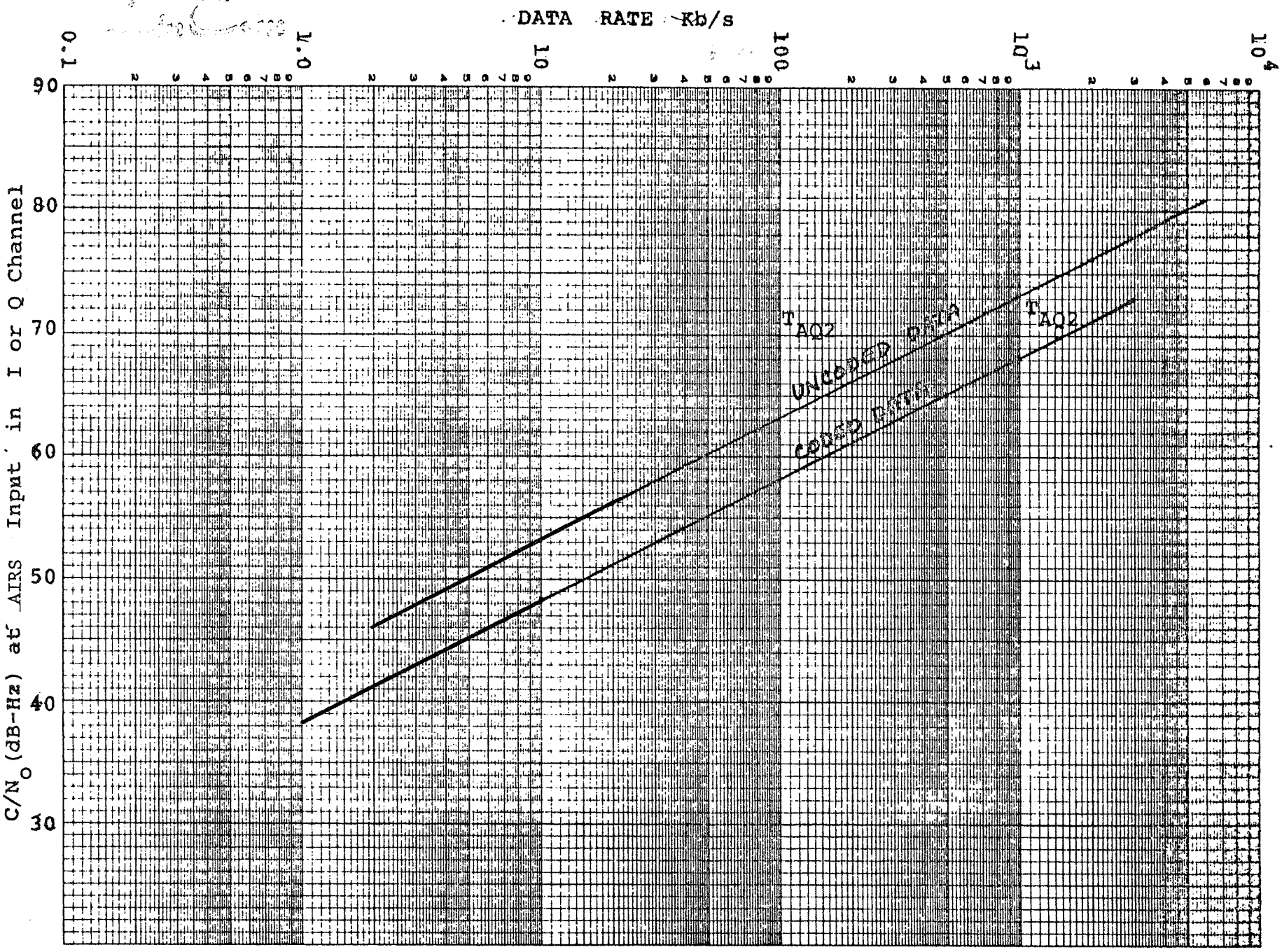

Figure 3.2.4.3-3. DG-2 Data Acquisition Spec.

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Table 3.2.4.1-1. Acquisition Time vs C/N_0 and Mode Requirements

ACQUISITION TIMES			
C/N_0 dB-Hz	1 SECONDS	2 SECONDS	3 SECONDS
39.5	N/A	DG-1 Modes 1,2A,3 DG-2 Modes 2A,3	DG-1 Mode 2B DG-2 Mode 2B
49.5	DG-1 Modes 1, 2A, 3	DG-1 Mode 2B	N/A

a. Multipath - Circuitry shall be provided to prevent acquisition of a DG-1 multipath signal. This protection will be provided for specular reflections whose delay with respect to the direct signal lies within the range 700 ns to 5 ms and whose received signal level is down at least 19 dB with respect to the direct input signal.

b. False Lock - Circuitry shall be provided in the AIRS to protect against false lock in carrier recovery and, during DG-1 signal acquisition, false lock to PN code sidebands.

3.2.4.3 Reacquisition

The AIRS shall employ the pre-drop-lock information to aid reacquisition. Uses of wait state and minisearch schemes shall be employed before reverting to the initial acquisition process. Reacquisition time shall be TBD% faster than the acquisition time for a temporary signal dropout for less than TBD sec.

3.2.5 Carrier Tracking

3.2.5.1 Carrier Cycle Slippage

The AIRS shall comply with the following requirements.

3.2.5.1.1 DG-1 Modes

The demodulator carrier recovery loop mean time to cycle slip for DG-1 Modes 1, 2 or 3 input signals shall not be less than (TBD $\approx$ 1) minutes for C/N_0 values from 28.1 dB-Hz to (TBD $\approx$ 33) dB-Hz and shall not be less than 90 minutes for C/N_0 values greater than (TBD $\approx$ 33) dB-Hz.

3.2.5.1.2 DG-2 Modes

The demodulator carrier recovery loop mean time to cycle slip for DG-2 Modes 2 or 3 input signals shall not be less than 90 minutes.

3.2.5.2 I and Q Channel Interchange

The mean time for random interchange between I and Q channels for all data modes shall exceed 90 minutes. The time to recover, for data configurations for which I and Q channel ambiguity resolution is required, shall not exceed the time to detect, interchange and resynchronize the bit synchronizers and convolutional decoders.

3.2.5.3 Loss of Lock

Carrier and PN loss of lock shall not occur for C/N_0 values 3 dB lower than those defined in Paragraph 3.2.3.7.

3.2.6 Data Extraction

3.2.6.1 Bit Error Rate

In the Data Processing Mode, the AIRS shall provide a bit error rate (BER) of 10^{-5} or better. This applies to both stable and unstable orbits.

3.2.6.2 Bit Slippage Rate Performance

The AIRS data output symbol slippage rate shall not exceed the values specified in Table 3.2.6.2-1. This performance shall be met with the input signal conditions specified herein. Indicated jitter and jitter rate percentages are the user spacecraft peak clock frequency jitter and peak jitter rate (sinusoidal or 3σ random) as percent of the symbol clock rate.

3.2.6.3 Convolutional Decoding

3.2.6.3.1 Rate 1/2 Decoders

The following data coding parameters apply to these return link services: DG-1 modes 1 and 2 for a single data channel; DG-1 modes 1, 2, and 3 for dual data channels; DG-2 for a single data channel (BPSK or SQPSK modulation); and DG-2 for dual data channels (quadriphase

Table 3.2.6.2-1. Symbol Slippage Rate.

AIRS INPUT E_b/N_o	DATA FORMAT	INPUT PEAK CLOCK JITTER	INPUT PEAK JITTER RATE	MAX. SYMBOL SLIPPAGE RATE (BSR)
8.1 dB	NRZ or BiØ	$J \leq .1\%$	$JR \leq .1\%$	10^{-10}
8.1 dB	BiØ	$0.1\% \leq J \leq .5\%$	$0.1\% \leq JR \leq .5\%$	10^{-9}
13.1 dB	BiØ	$0.5\% \leq J \leq 1.0\%$	$0.5\% \leq JR \leq 1.0\%$	10^{-8}*
13.1 dB	BiØ	$1.0\% \leq J \leq 2.0\%$	$1.0\% \leq JR \leq 2.0\%$	10^{-7}*

modulation).

1. Code 1: convolutional, nonsystematic, transparent.

2. Rate: 1/2.

3. Constraint length: K = 7.

4. Generator functions:

   a. G_1 = 1111001.

   b. G_2 = 1011011.

5. Symbols generated from G_1 will precede symbols generated from G_2 relative to the data bit period.

6. Symbols generated from G_2 will be either true or complemented as defined by the service support schedule.

The following data coding parameters will apply to this return link service: DG-2 for a single data channel BPSK modulation.

1. Code 2: convolutional, nonsystematic, transparent.

2. Rate: 1/2.

3. Constraint length: K = 7.

4. Generator functions:

   a. G_1 = 1011011

   b. G_2 = 1111001

5. Symbols generated from G_1 will precede symbols generated from G_2 relative to the data bit period.

6. Symbols generated from G_1 will be complemented.

3.2.6.3.2 Rate 1/3 Decoders

The following data coding parameters apply to these return link sevices: DG-1 mode 3 Q channel (dual data channel configuration), DG-2 for a single data channel (BPSK modulation), and DG-2 for one channel of the dual data channel configuration (quadriphase modulation).

1. Code 3: convolutional, nonsystematic, transparent.

2. Rate: 1/3

3. Constraint length: K = 7.

4. Generator functions:

   a. G_1 = 1111001.

   b. G_2 = 1011011.

   c. G_3 = 1110101.

5. Symbol sequence from the convolutional coding will be generated from G_1, G_2, and G_3 successively relative to the data bit period.

6. Alternate symbols generated from the convolutional coding will be complemented.

3.2.6.3.3 Symbol Interleaving

At symbol rates above 300 Ks/sec, symbol interleaving may be used. The functional description of the periodic convolutional interleaving of either Rate 1/2 or Rate 1/3 convolutional encoder symbols is defined in Appendix J of the TDRSS Users' Guide.

3.2.7 I/Q Channel Ambiguity Resolution

The AIRS shall resolve the DG-1 and DG-2 QPSK I and Q channel output ambiguities for the conditions in the following subparagraphs.

3.2.7.1 DG-1 Data Modes

3.2.7.1.1 Modes 1 and 2

The I and Q channel ambiguity shall be resolved by recognition of different PN codes or delayed codes between I and Q as defined to the AIRS.

3.2.7.1.2 Mode 3

The I channel shall be identified by recognition of the PN code

spreading of the I channel data.

3.2.7.2 DG-2 Data Modes

For DG-2 Modes 2 and 3, the I and Q channel ambiguity shall be resolved for the following conditions.

3.2.7.2.1 Unbalanced (4:1) QPSK Modulation

The AIRS shall detect I/Q power ratio of 4:1 and provide correspondingly correct I and Q channel outputs and lock states.

3.2.7.2.2 Different Channel Data Rates

The AIRS shall automatically resolve any I and Q channel output and lock state ambiguities when the channel data rates differ by 5%.

3.2.7.2.3 Coded/Uncoded Channels

When the I and Q channels have balanced Power, the I and Q data rates differ by less than 5% and one channel is coded but the other is uncoded, channels ambiguity shall be resolved by recognizing the coded channel in conjunction with the decoder. When both the I and Q channels are coded or uncoded, output I and Q channel ambiguity resolution will not be required.

3.2.8 Data Format Conversion

The AIRS shall convert all NRZ and Bi ϕ-M, S data formats to NRZ-L format.

3.2.8.1 Uncoded NRZ-M or S or Bi ϕ-M, S Data Format

The uncoded NRZ-M or S or Bi ϕ-M, S data format shall be converted to NRZ-L by the AIRS to provide negative true data output.

3.2.8.2 Coded NRZ-M, S and Bi ϕ-L Format

a. Bi ϕ-L format whenever used will follow the convolutional encoding. The AIRS shall convert the Bi ϕ-L format to NRZ-L prior to decoding.

b. NRZ-M, S data format whenever selected by the User will be used to format the data prior to convolutional encoding. The AIRS/Decoder Units shall convert from NRZ-M, S to NRZ-L format following Viterbi decoding.

3.2.9 RARR Tracking Support

The AIRS shall provide a reconstructed received carrier and detected PN Epoch period pulse with clock to the RARR Equipment for Tracking Services support. The reconstructed carrier and epoch pulse with clock shall meet the following performance requirements.

3.2.9.1 Reconstructed Carrier

The AIRS shall provide a 17.50 MHz reconstructed carrier signal containing the input signal frequency dynamics. In addition the AIRS shall also provide a time-tagged Doppler estimate to its serial data interface at a TBD update rate.

3.2.9.1.1 Reconstructed Carrier Phase Noise

The AIRS phase noise contribution to the reconstructed carrier signal shall not exceed the following values for the specified C/N_0 values and when integrated over a one second period.

MAX. C/N_0	SYMBOL RATE	MAX. RMS PHASE NOISE JITTER
28 dB-Hz	100 S/s	17.3^o
35 dB-Hz	500 S/s	12^o
38 dB-Hz	1000 S/s	8^o
45 dB-Hz	5000 S/s	4^o

3.2.9.2 PN Epoch and Clock Timing Accuracy

The AIRS shall detect the all ONES state of the received PN code

when operating in DG-1 Modes and provides a PN Epoch pulse with clock to the RARR Equipment.

3.2.9.2.1 PN Clock Time Variation

The PN clock time variation shall meet the following specifications.

a) Initial Fixed AIRS Delays: (Calibrated Delay) $\leq$ 500 nsec

b) Variation on Fixed Delays: (Non-Calibratable Delay) $\leq$ 13 nsec

c) Jitter (rms) at specified minimum C/N_0 values

Below 2KS/s: $\leq$ 14 nsec

Above 2KS/s: $\leq$ 8 nsec

3.2.9.2.2 PN Epoch Time Variation

The PN Epoch pulse shall meet the following specified delay and jitter requirements relative to the PN clock time.

a) Maximum fixed delay from positive going edge of PN Clock: $\leq$ 10% of clock period

b) Variation on fixed delay: $\leq \pm 5$ nsec

c) Jitter (rms): $\leq$ 2 nsec

3.2.10 Self Test and Operational Status Capability

Self-test features of the AIRS when in operational use shall provide an indication of operational readiness, warn of degraded performance, and facilitate maintenance actions. Self-test capability shall be implemented by built-in-test equipment (BITE) or by the inherent capability of the design, or a combination of both.

3.2.10.1 Operation Status

The AIRS self-test capability shall include a determination of the AIRS configuration and the quality of the received signal as follows:

a. AIRS configuration, state and pertinent parameters.

b. Performance indicators such as received signal strength, BER estimate, and phase jitter estimate.

These data shall be assembled in an appropriate serial format and routed to an external interface via GPIB. The time between updates for these data shall be no more than (TBD 1) sec.

3.2.10.1.1 Displayed Monitor and Status Signals

The AIRS shall display the following discrete and analog signals.

3.2.10.1.1.1 Lock Status Signals

The following signals shall be displayed.

a. A Carrier Lock Signal (CLS) shall be provided to indicate received carrier locked/unlocked conditions.

b. A PN Code Lock Signal (PLS) shall be provided to indicate received PN code locked/unlocked conditions.

c. A Received PN Code and Carrier Lock Signal (RLS) shall be provided whenever PLS and CLS are simultaneously obtained.

d. A Bit Sync Lock Signal (BLS) shall be provided to indicate bit sync locked/unlocked conditions.

e. A Decoder Lock Signal (DLS) shall be provided to indicate decoder branch synchronization locked/unlocked conditions.

3.2.10.1.1.2 Analog Signal Monitors

The following signals shall be displayed for operational monitoring purposes.

a. A Signal Strength Signal (SSS) shall be provided.

b. A Signal Quality Signal (SQS) shall be provided.

3.2.10.1.2 Interface Serial Data

The AIRS shall provide monitor signals to the ground segment interface as a part of its serial GPIB data output. The monitor signals are designed to report the status of the receiver and the received signal conditions. The monitor signals shall include:

(a) Lock Indications:

(1) PN despread operational status-searching, tracking, of loss of lock.

(2) Frequency lock loop--off or on (tracking, acquiring).

(3) Carrier lock loop--acquisition, tracking or loss of lock.

(b) AGC. Noncoherent AGC and Coherent AGC Voltages.

(c) Link Performance Indications - symbol error rate, bit error rate and SNR.

(d) Receiver configuration, e.g. PN despread on or off, adaptive equalizer on or off, IF filter bandwidths, etc.

(e) Receiver modes - acquisition, data demodulation, or reacquisition.

3.2.10.2 Set Confidence

The AIRS self-test capability shall include a confidence test which shall indicate whether the AIRS itself and its interfaces with ground station equipments are operating correctly, as follows:

a. The test shall indicate equipment malfunction for at least 90% of all AIRS failure modes, weighted for failure rate.

b. The test shall have a maximum false alarm rate of 5% of the total number of malfunctions indicated.

c. When a malfunction is detected, data concerning the malfunction shall be entered into memory for later review by

maintenance personnel.

This test shall verify that all hardware subsystems are functional, e.g., by injecting an internal CW signal at its input and monitoring voltages at various points of the receiver. It shall also include a test to verify that the receiver software is healthy, e.g. by computing the parity check bits of memory content.

3.2.10.3 Fault Isolation

The AIRS shall include malfunction isolation to the LRU and SRU level.

4.0 TEST REQUIREMENTS

The equipment supplier shall be required to implement a test program that will demonstrate to the purchaser that each of the specified requirements have been met. The test matrix, Table 4-1, provides a list of each of the parameters which must be verified and the method by which the verification shall be performed. The equipment supplier shall submit a test procedure to the purchaser which will provide the detailed test description and the instructions by which the tests will be implemented. The test procedure will be subject to review and approval by the purchaser.

The methods of evaluation prescribed by the test matrix are defined as follows:

a. Functional Demonstration (FD) - Compliance is demonstrated in a non-quantitative manner without the use of external test devices. This is usually a visual observation that the function responded in the sepcified manner when selected.

b. Test (T) - This verification generally requires external test equipment for signal injection and/or signal measurement in

order to demonstrate compliance to a specified parameter value.

4.1 Test Signals

In addition to the normal AIRS outputs, the following test access points shall be available:

a. PN code search flag.

b. Carrier Loop VCO.

APPENDIX

BASELINE RECEIVER

1.0 Introduction

The purpose of this appendix is to describe a baseline receiver design* capable of meeting the AIRS functional requirement specifications. The contractor shall employ the receiver design described below or propose and justify another design. The contractor shall support his proposed design by presenting analytical and/or experimental evidence of its effectiveness in meeting all of the performance requirements given in the specification.

2.0 AIRS Baseline Design Features

Except for the PN acquisition and tracking circuits, the AIRS baseline is a digital receiver controlled by software (numerical algorithms) residing in a numerical processor. All high speed processing is implemented via dedicated high speed logic. The loop control error signals, which are to be filtered with relatively narrowband filters (e.g. carrier loop filter, bit sync loop filter, etc.), will be first pre-processed by these dedicated logic circuits to a speed compatible with the numerical processing. The digital/numerical processor scheme is selected for its versatility in terms of control and parameter selections necessitated by the AIRS requirements.

The specific design approaches are selected to achieve near optimum performance and/or maximum flexibility with minimal impact on the hardware complexity of the receiver. They are outlined in the following sections.

*See also Vols. II and III.

2.1 Dual Channel Acquisition and Tracking

Signals from the I and Q channels are fully utilized in generating the error signals driving the acquisition and tracking circuits. The error signals are weighted according to the specified power split. This approach maximizes the available received power for acquisition and tracking under all user data characteristics.

2.2 PN Acquisition and Tracking

2.2.1 Multichannel PN Acquisition

Coordinated parallel search using sequential detection is employed for PN acquisition*. This will ensure acceptable acquisition time by reducing the uncertainty interval to be searched by each channel. Four channels are used to satisfy the acquisition time requirement and represent efficient use of hardware complexity. Two channels are used for tracking after initial acquisition while the other two will be devoted to verify that the tracking channel is not locking to a code sidelobe or a multipath signal.

2.2.2 PN Sidelobe Lock/False Lock Discrimination

Sidelobe and false lock discrimination are implemented using sequential detection with a higher dismissal rate to look for possible stronger code correlation levels once acquisition is declared.

2.2.3 PN Multipath Lock Discrimination

Multipath lock is prevented by checking code correlation ±2 chips away from declared lock point.

2.2.4 Dual Channel Dithered Early/Late PN Tracking Loop

For DG-1 mode 1 and 2 signals where both channels are spread, PN

*For low data rate, parallel search techniques such as one using CCD matched-filter will be used.

tracking is accomplished using a dithered early/late tracking loop for both the I&Q channels. A 3 dB SNR improvement can be realized for 1:1 power split compared to tracking only one channel.

2.3 Frequency Acquisition and Reacquisition

2.3.1 Frequency Lock Loop

Rapid frequency acquisition is accomplished by employing a frequency lock loop or an alternate and suitable frequency estimation scheme. This approach also avoids false locking to data sidebands--a phenomenon commonly associated with sweep acquisition schemes.

2.3.2 Orbit Uncertainty Estimation

Once the receiver has acquired and tracked the incoming carrier frequency, the estimated Doppler from the carrier loop is used for Doppler correction. The purpose is to reduce the frequency uncertainty for reacquisition during temporary signal loss. It also reduces the frequency dynamics that the receiver carrier tracking loop must handle in the steady state.

2.4 Joint Bit Sync/Carrier Recovery

2.4.1 Data-Aided Carrier Loop

A design based on the data-aided loop is selected for carrier recovery to eliminate crosstalk between the I and Q channels. This alleviates, for example, the tracking problems resulting from 2-phase Costas loop quadrature channel interference associated with the current SSARE DG1-Mode 3 operation.

2.4.2 Joint Carrier/Clock Acquisition

The bit sync and carrier loop function as a single unit and acquire simultaneously. This provides a rapid overall system acquisition.

2.4.3 Digital Implementation

The bit sync and carrier loop are implemented with numerical algorithms. Optimum filter parameters can be selected continuously and instantaneously. Smooth parameter transitions can also be realized easily.

2.4.4 Switchable Second- or Third-Order Loops

A third-order carrier loop is employed as a result of the requirement to track high dynamics for an unstable orbit. A third-order loop also nullifies the static phase error which affects the slip performance of the receiver. However, a second-order loop is used during initial acquisition and subsequent reacquisition to avoid potential stability problems associated with acquiring with a third-order loop.

2.5 Miscellaneous

2.5.1 PN/Carrier Loop Frequency Aiding

After the PN loop has acquired and tracks, the local PN clock, coherently related to the carrier frequency, can be used to aid carrier loop frequency acquisition. The frequency error, due to PN loop tracking jitter, is considerably less than the carrier frequency uncertainty provided by the orbit estimate. Hence the PN clock can be employed to reduce the carrier uncertainty during carrier acquisition. After the carrier loop has acquired and tracks, the carrier frequency can be divided down to aid the PN loop by compensating the Doppler induced PN clock dynamics so that a narrower PN loop bandwidth can be employed.

2.5.2 RFI Mitigation Processing

Provisions for processing demodulated convolutionally encoded symbols corrupted by RFI are incorporated. For the more complicated

nonlinear processing schemes, the processor is implemented using a high-speed ROM (Read Only Memory).

2.5.3 Adaptive Equalizer

Tapped delay line equalizers are included at the output of the data demodulator for high rate data ($\geq$ 6 Mbps per channel). This can increase the SSA data throughput to 12 Mbps per channel.

3.0 DETAILED DESIGN APPROACH

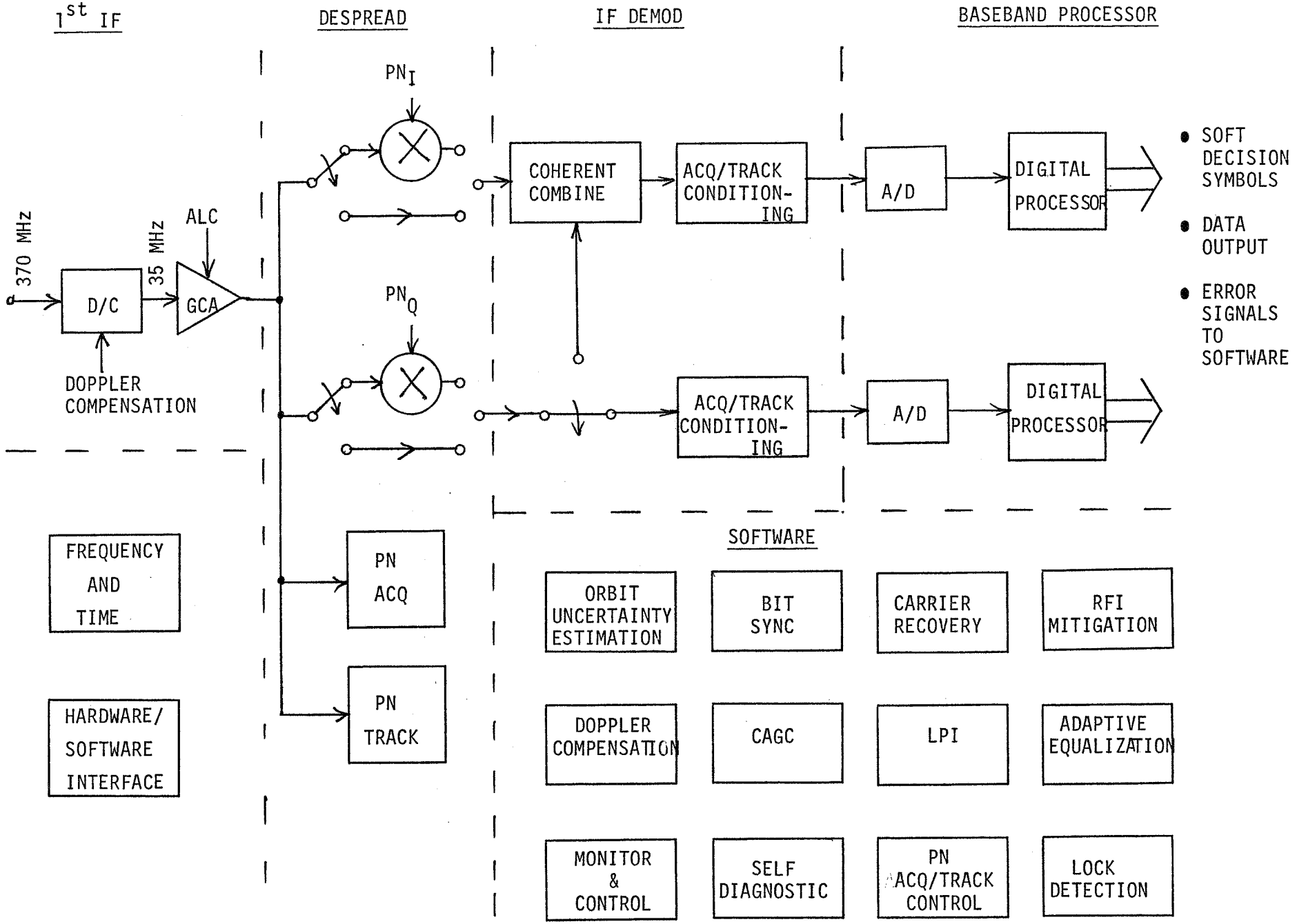
The functional paritions of the AIRS baseline receiver are shown in Fig. 3-1. The receiver consists of a first IF stage where the incoming signal at 370 MHz is down converted and Doppler compensated with available predicts to a 35 MHz second IF. The 35 MHz IF is selected to be compatible with the existing LRD and MRD. The signal is then gain controlled with an automatic level control (ALC) circuit (i.e., noncoherent AGC) before it is fed to the PN despread subsystem.

If the incoming signal is PN spread, it is despread by multiplying off the PN modulation with the local PN code estimate. Despreading is bypassed for the unspread channel. The local PN code estimate is generated by means of the PN acquisition and tracking circuits.

In the IF demodulator section, I and Q channels are combined at IF if they contain identical data. The signals are then demodulated to baseband in the Acq/Track Conditioning block.

After the IF demodulator section, the receiver is implemented digitally. The baseband data is A/D converted and processed by the digital processor. The digital processor consists of high speed logic circuits dedicated to various functions such as filtering and loop error signal generation, etc. The digital processor also outputs the demodulated data.

Fig. 3-1. AIRS Functional Diagram.



All loops (excluding the PN loop and ALC although their parameter selections are under software control) are closed via the software residing in a numerical processor (e.g. a microprocessor with dedicated floating point arithmetic). Additional functions are also shown in the figure.

Other ancillary blocks including frequency and time generation (locked to 5 MHz F&T reference) and hardware/software interface are also required.

In what follows, each functional block indicated in Figure 3.1 will be expounded.

3.1 First IF Section

Refer to Figure 3.1-1. The first IF stage converts the incoming frequency at 370 MHz to an IF of 35 MHz. Its output is then noncoherently gain controlled by the ALC circuit whose response time can be controlled by varying the loop parameters. The bias reference voltage can be varied according to the received data characteristics.

The IF conversion stage also performs Doppler compensation based on the available predicts. In the scheme shown, the Doppler predicts control the frequency output of the synthesizer which operates at a nominal frequency of 55 MHz. The synthesizer is locked to the station Frequency & Time (F&T) reference to provide best achievable frequency stability. The 335 MHz LO frequency is obtained by up converting the synthesizer output by a fixed reference at 280 MHz derived from a 5 MHz F&T reference.

3.2 PN Despread Section

The PN subsystem performs the acquisition, tracking and despreading of PN spread signals. Bypass paths are provided for unspread signals.

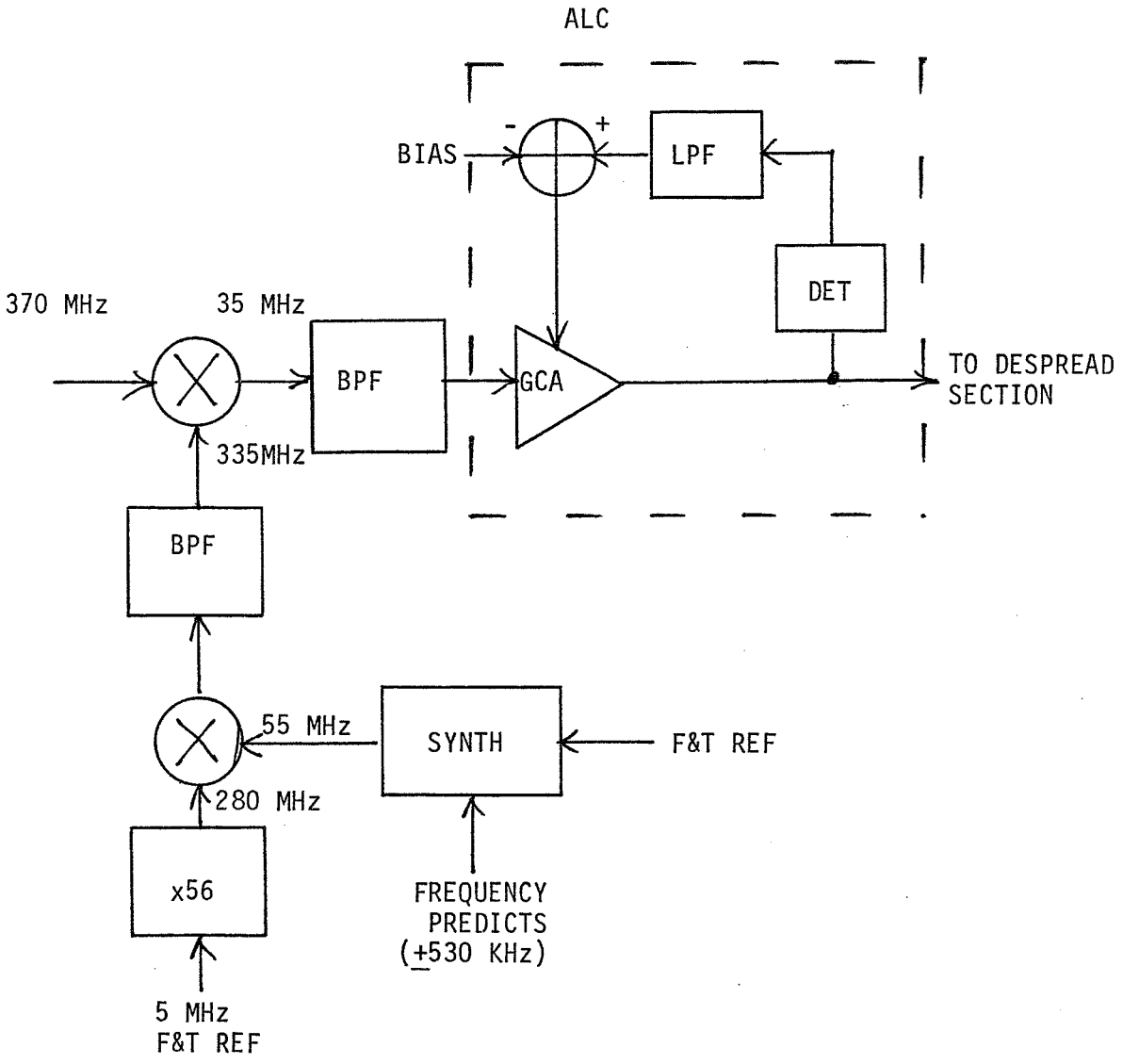


Fig. 3.1-1. First IF Conversion and ALC.

3.2.1 PN Acquisition

Sequential detection is employed for PN acquisition as shown in Figure 3.2-1 to optimize the acquisition performance. The BPF is selected to match the data rate of the incoming signal. In order to satisfy the AIRS acquisition requirement, 4 channels are employed to perform the sequential search in a coordinated manner*. Each channel searches over 1/4 of the total chip uncertainty region thereby increasing the average search rate by a factor of 4. When code sync has been detected, 2 channels will be reconfigured to the tracking configuration. Two remaining PN channels will continue to verify if the tracking channel is locked to a sidelobe by searching for higher code correlation elsewhere. If a sidelobe lock is not detected, they will be used to verify if a multipath lock has been detected by checking the displaced code correlation level (±2 chips relative to the lock point). If a multipath lock is not found, they will then be configured for tracking (DG1 Modes 1 and 2).

3.2.2 PN Tracking

Figure 3.2-2 shows the PN tracking loop. Two dithered early/late gated loops are employed in parallel--one for each data channel (if both I and Q channels are spread). The advantage of the dithered early/late gated loop is its ability to nullify the effects of imbalances between the early and the late channel. The BPF bandwidth is a design parameter and is selected according to the data rate. In the two channel configuration, the I and Q channels are also dithered as well as the early and late channels to nullify imbalances between the I and Q

*See acquisition employing CCD in Vol. III.

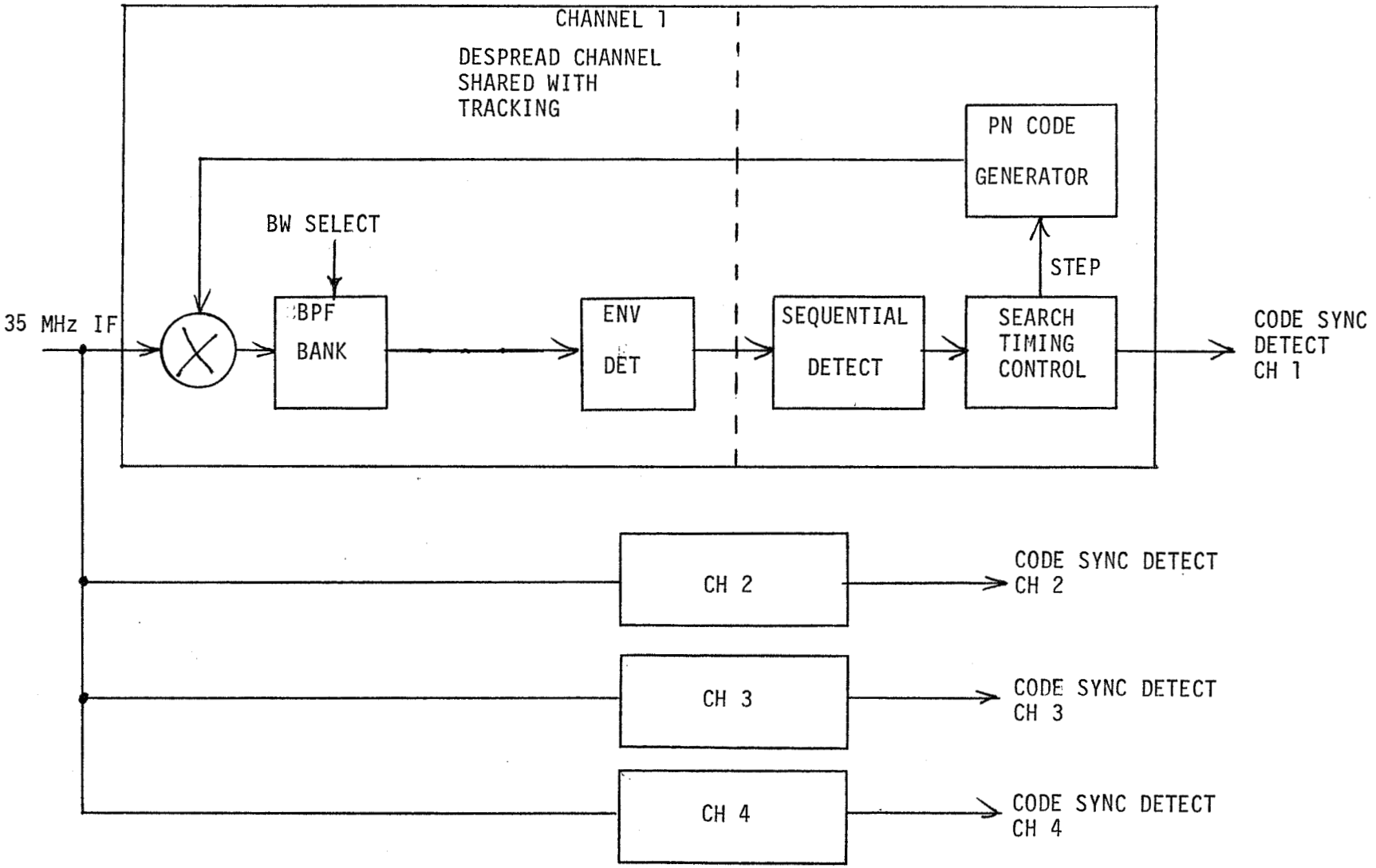


Fig. 3.2-1. Sequential PN Acquisition (4 Channel).

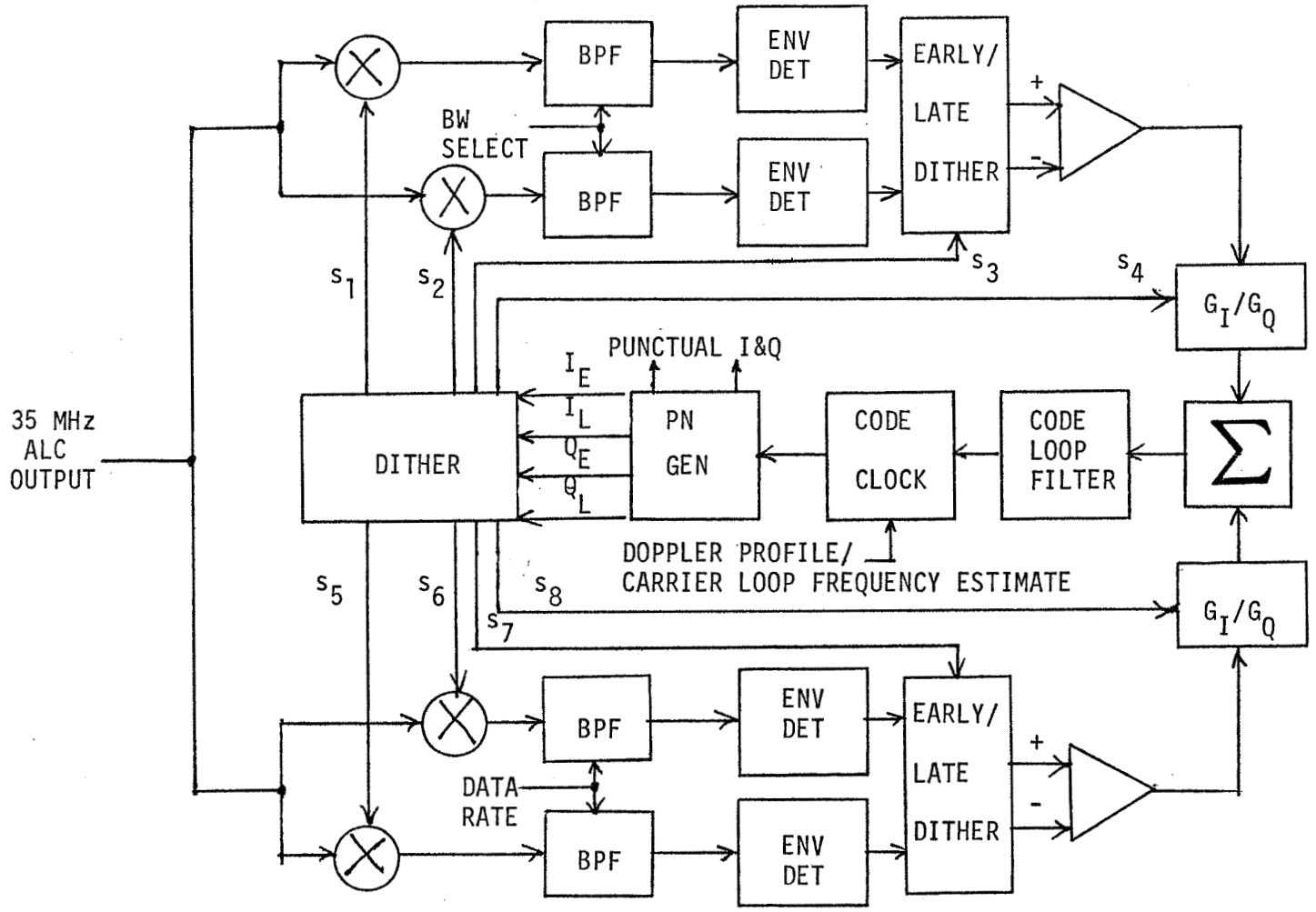


Fig. 3.2-2. 2-Channel Dithered Early/Late PN Tracking Loop.

channels. The timing diagram for the controlling and switching signals (s_1-s_8) are shown in Figure 3.2-3. The gains G_I and G_Q for the PN error signals are selected according to the specified power split. The code clock frequency is aided with Doppler predicts and, after the carrier recovery loop has acquired and tracked, with the carrier loop frequency estimate.

When only one channel is spread, one-half of the tracking loop is used and the configuration reduces to a conventional dithered early/late PN loop.

3.3 IF Demodulator Section

The IF demodulator section consists of the coherent combiner and the signal conditioning block for data wipe-off during carrier frequency acquisition.

3.3.1 Coherent Combiner

When both the despread I and Q channel contain identical data, the two channels are coherently combined at IF using a power combiner and only one channel is used for subsequent processing.

3.3.2 Carrier Acquisition Processing

The carrier acquisition processing subsystem is shown* in Figure 3.3-1. The 35 MHz IF signal has already been down-converted using a frequency synthesizer nominally at 10 MHz. The frequency synthesizer is a numerically controlled oscillator under command of the software residing in the numerical processor. During carrier frequency acquisition, the frequency control is accomplished by means of a frequency lock loop algorithm. During carrier tracking, the frequency

*A simpler scheme is discussed in Vol.III and shall be used.

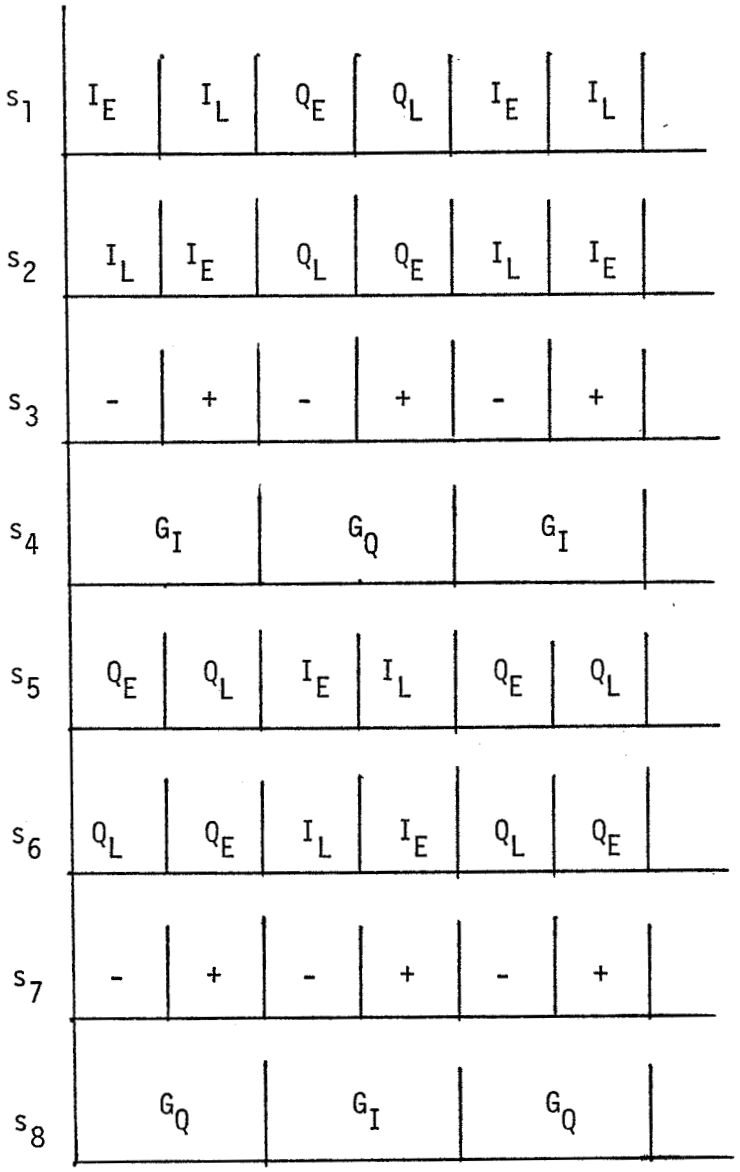
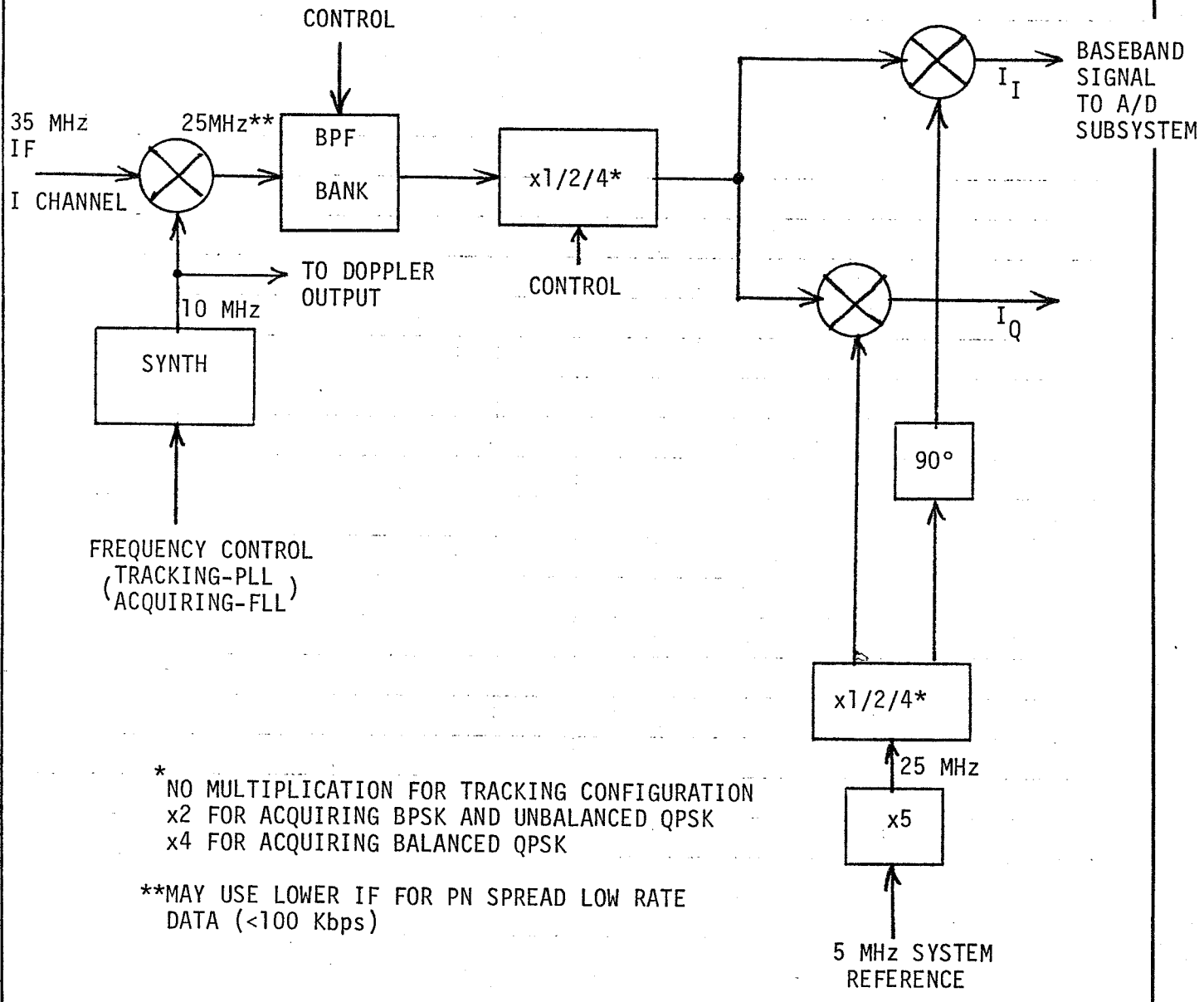


Fig. 3.2-3. Timing Diagram for 2 Channel Tracking



* NO MULTIPLICATION FOR TRACKING CONFIGURATION
x2 FOR ACQUIRING BPSK AND UNBALANCED QPSK
x4 FOR ACQUIRING BALANCED QPSK

**MAY USE LOWER IF FOR PN SPREAD LOW RATE DATA (<100 Kbps)

Fig. 3.3-1. Carrier Acquisition Processing Subsystem (Only I Channel Shown).

control is accomplished by means of a phase-locked loop algorithm. The down-converted signal at 25 MHz is filtered by the BPF whose bandwidth is selected according to the data rate. A 25 MHz IF is chosen to accommodate the higher data rates (12 Mbps/channel). The signal is then complex (I&Q) demodulated by a fixed 25 MHz LO when configured for tracking. For acquiring BPSK and UQPSK (4:1 power split) signals, the signal is doubled and complex demodulated by a 50 MHz LO. For acquiring QPSK signal, the signal is quadrupled and complex demodulated by a 100 MHz LO.

The advantage of this scheme is that switching from acquisition to tracking configuration can be accomplished by simply switching the multipliers.

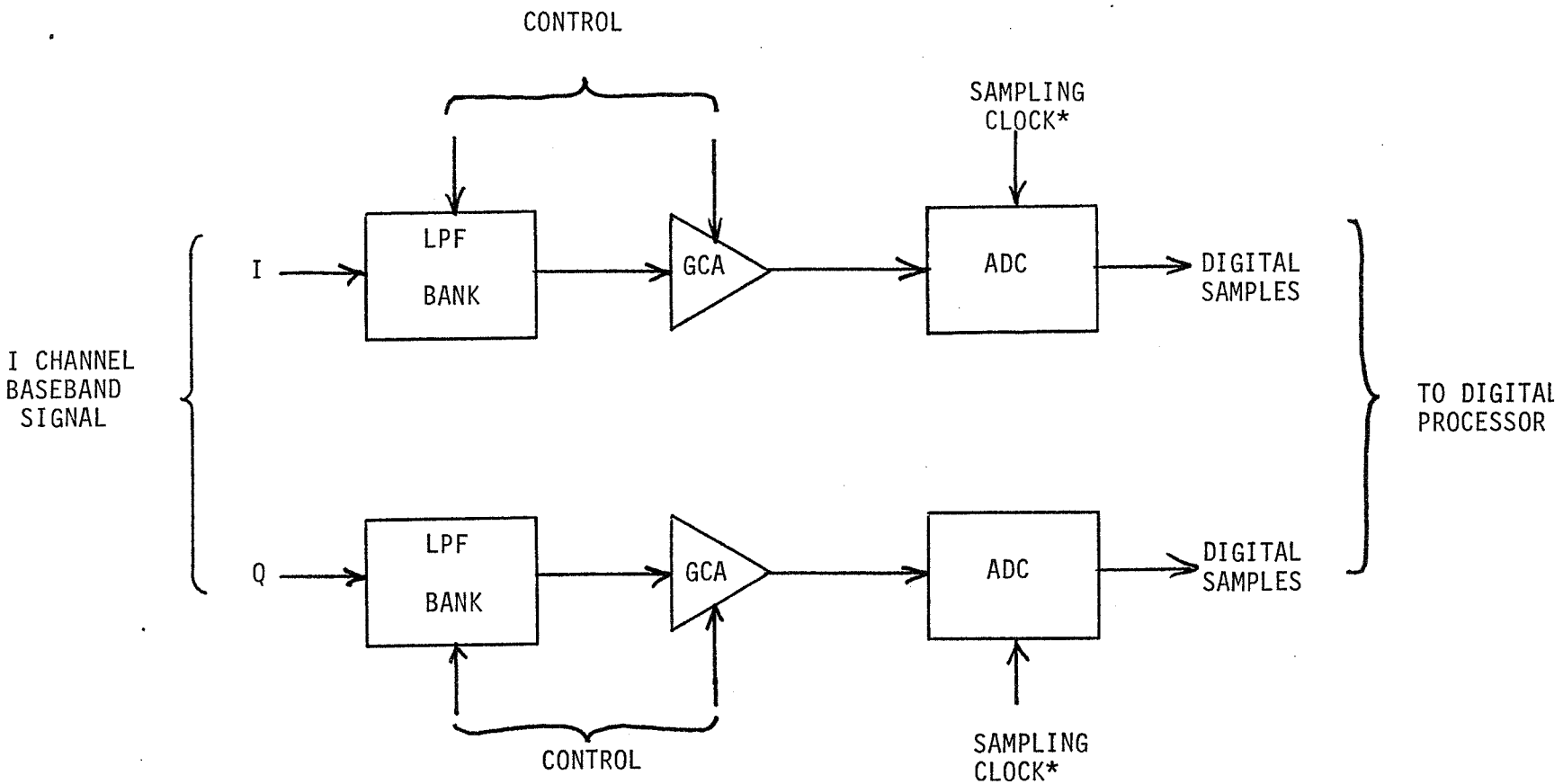
For PN spread low rate data (< 100 Kbps), a 2.5 MHz IF may be considered so that high Q BPFs are not required. In that case the nominal synthesizer output is 37.5 MHz and the 5 MHz system reference is divided by 2 (rather than multiplied by 5) to get 2.5 MHz.

3.4 Baseband Digital Processor Section

The complex demodulated signals (slowly rotating phasors at baseband) are A/D converted, processed and detected by the digital processor. The digital processor has additional functions: (1) it provides error signal samples at a rate compatible with the numerical processor for the tracking and acquisition algorithms, (2) it provides adaptive equalization for high data rates, (3) it provides RFI mitigation processing for convolutionally encoded data, and (4) it provides monitoring signals.

3.4.1 A/D Subsystem

The A/D subsystem is shown in Fig. 3.4-1. The inphase and



*

CONFIGURATION	CLOCK RATE
ACQUISITION	4 x FREQUENCY UNCERTAINTY
NRZ	8-16 x BIT RATE
MANCHESTER	8-32 x BIT RATE

Fig. 3.4-1. A/D Subsystem.

quadrature components of the baseband channel are first filtered by the LPF whose bandwidth is commensurate with the sampling rate. The LPF is used to limit the noise power into the ADC and provide antialiasing filtering for the sampling process. For acquisition the sampling rate is 4 times the frequency uncertainty (4x20 KHz maximum). For tracking NRZ data, the sampling rate is 16 times the bit rate. However, for high data rates (≈10 Mbps) the sampling rate is limited by the processing rate of the digital processor so that 8 times the bit rate is anticipated. For Manchester data the sampling rate is 2 times that of NRZ.

The lowpass filtered signal is then gain controlled to match the dynamic range of the ADC. The GCA setting is preset based on the data rate during initial acquisition. After the receiver has acquired, the GCA is controlled via a coherent AGC loop to optimize performance.

3.4.2 Digital Processor

The digital processor accepts the sampled signals from the A/D subsystem and provides error signals for carrier frequency acquisition, carrier tracking, data clock recovery, coherent AGC and the necessary data for monitoring functions. It groups the samples into demodulated data, provides RFI mitigation processing, and provides adaptive equalization for high rate data.

3.4.2.1 Frequency Acquisition Processing

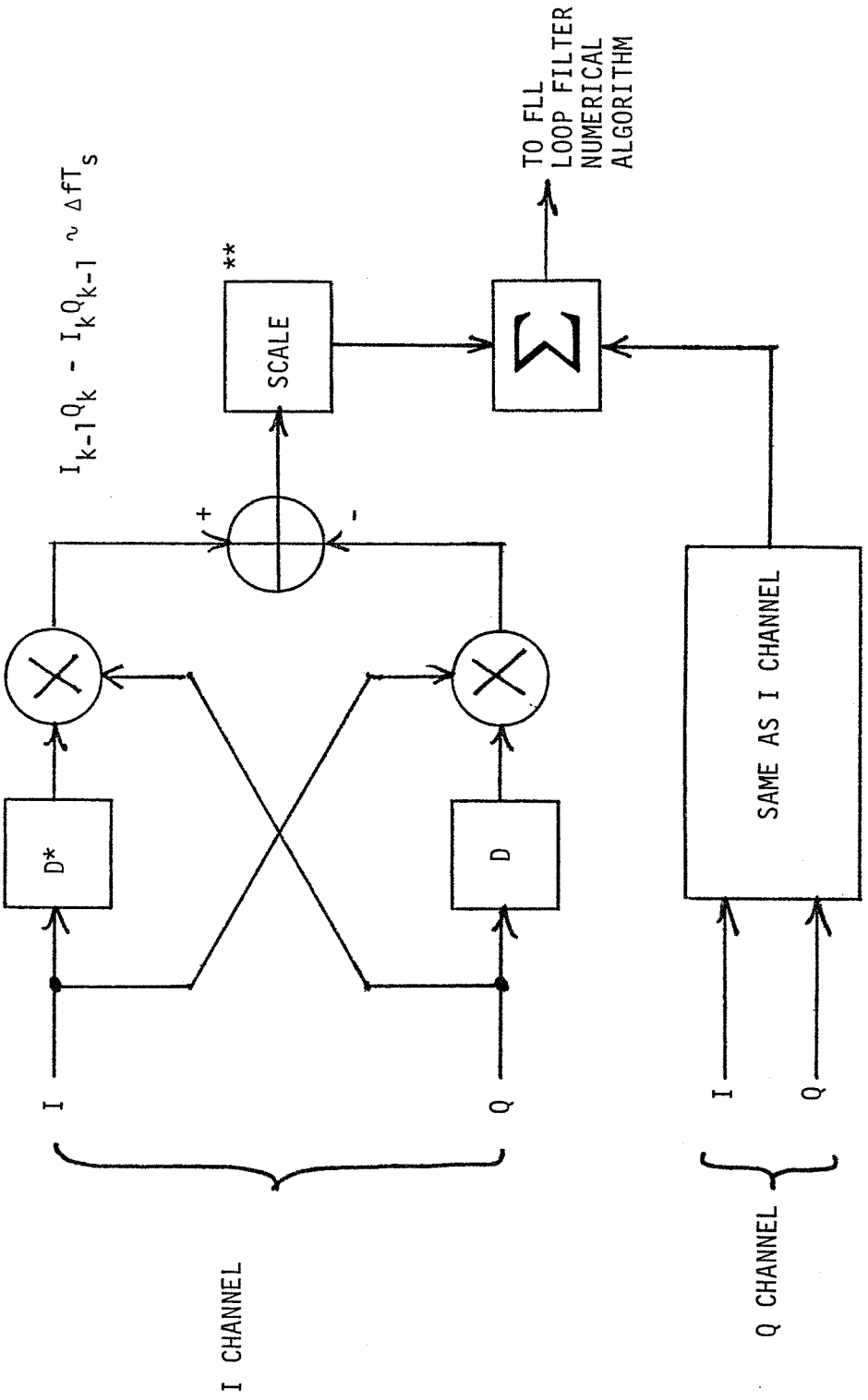
In the carrier frequency acquisition mode, the data in the input signal has been multiplied off so that the input to the ADC is a slowly rotating phasor. Two approaches can be used to estimate the frequency uncertainty; namely, via an open loop estimator and via a closed loop estimator. The open loop estimator in general offers improved

performance at the expense of complexity and will not be addressed presently. Here we consider a frequency lock loop (FLL) mechanization shown in Figure 3.4-2. In this scheme, an estimate of the frequency error is formed from the crossproduct $(I_{k-1}Q_k - I_kQ_{k-1})$ which can be shown to be proportional to the frequency offset Δf and the time between samples. When both I and Q channels contain data and can be separated by the PN despreader, as in a normal DG-1 data configuration, the error signals are weighted with the corresponding power split before feeding to the FLL software. The highest sampling rate is on the order of 80 KHz; therefore, the numerical processor can accomodate the data throughput.

3.4.2.2 Data-Aided Carrier Tracking/Bit Sync

Figure 3.4-3 shows the required data processing for generating carrier and clock loop error signals. Since a data-aided carrier loop is implemented, demodulated data is also available as part of the error generation scheme.

The data-aided loop and the bit sync (a full symbol window DTTL) are basically digital implementation of the equivalent analog loops. The conventional integrate-and-dump circuit is implemented digitally with an accumulator which sums the samples over one symbol duration. To generate the error signal samples for the DTTL bit sync, the I (inphase) component samples are also accumulated over a bit interval centered between two adjacent bits. This gives a measure of the bit sync clock error. However, the error signal is not always of the appropriate sign. Therefore, a transition detector is implemented by examining two adjacent bits and its output is used to correct the sign ambiguity. At the highest data rate ($\approx$10 Mbps) the throughput rate of the error



*ONE SAMPLE DELAY
**SCALE DETERMINED BY POWER SPLIT

Figure 3.4-2. Digital Processing for Carrier Frequency Acquisition.

samples must be reduced in order to be compatible with the speed of the numerical processor. For this purpose, a second fixed length accumulator is used to reduce the data throughput rate. Two DTTLs are implemented for independent I and Q channels.

The error signal samples for the carrier recovery loop based on the MAP theory requires the product Q tanh(I). In that case, the nonlinear element must be implemented with a high speed ROM. However, negligible degradation is anticipated if the tanh(.) function is replaced by a clipper (or more simply, a sign function). The clipping function is easily implemented by a comparison/threshold operation. Error signals from the I and Q channels are weighted and combined according to the power split before feeding to the PLL algorithm software. When the ratio P_I/P_Q is quantized to a power of 2, the (gain) multiplication can be implemented by shifting the position of the bits representing the error signal samples. Again, the fixed length accumulator following the error samples is for the purpose of data throughput reduction.

For Manchester coded data, the accumulator I&D operation must be slightly modified. In this case the accumulator sums the digital samples for the first half bit time and subtracts them for the remaining half. The net effect is identical to first converting the Manchester symbol to NRZ data and then performing the standard operations on the converted NRZ data stream. The above approach is motivated by the MAP estimation.

However, the DTTL can be implemented by tracking half of a Manchester symbol as shown in Figure 3.4-4. In this case the Manchester coded data is treated as NRZ coded data at double the data rate. The advantage of this approach is to have a guaranteed minimum symbol

(phase) transition density of 50% regardless of the source bit transition density. This also eliminates the occurrences of long runs of ones or zeros. The guaranteed transition density greatly improves the acquisition (and tracking) performance of the DTTL. However, means must be provided to resolve the clock phase ambiguity introduced by tracking 2 times the data rate. A standard method is to observe the transitions about the two possible clock phases (from dividing the X2 clock) over a period of time.

Due to its ability to accomodate low bit transition densities, the latter approach or a combination of both (e.g. acquire with the second method and track with the first) are recommended.

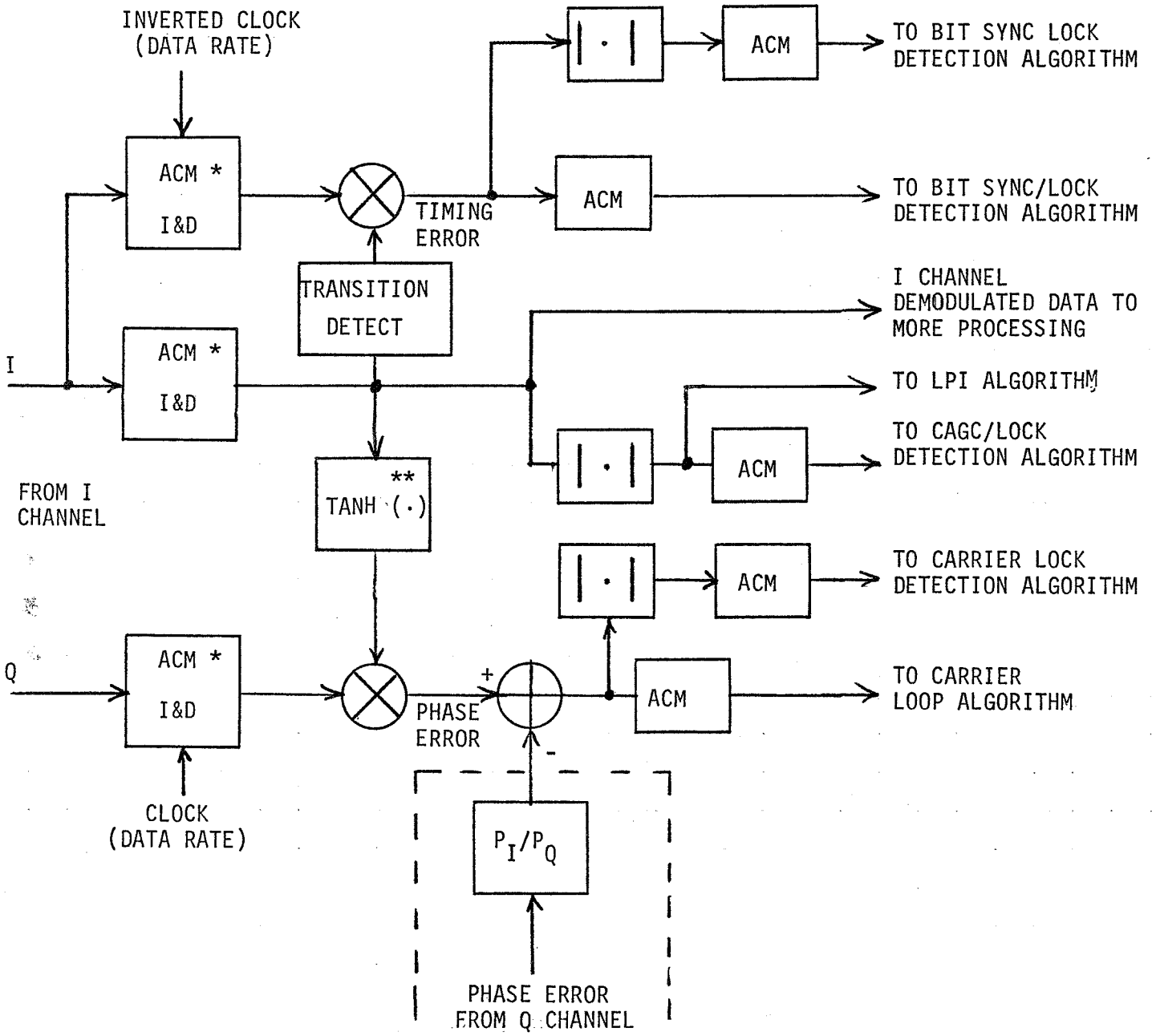
3.4.2.3 Carrier and Bit Sync Lock Detection

Lock detection is accomplished by comparing the power in the demodulated data and the power in the error signal driving the loops (carrier and clock recovery). When the loops are not locked, they are roughly equal. When the loops are in lock the data channel has a much higher power than the error channel. Lock is declared if the power ratio of the data channel to the error channel exceeds a certain threshold. The required signals to be processed by the lock detection software are indicated in Figure 3.4-3.

3.4.2.4 Coherent Automatic Gain Control

The generation of the error signal necessary to drive the coherent AGC software is also indicated in Fig. 3.4-3. The signal is a measure of the energy of the coherently demodulated data. An absolute value function is used to simplify operation. Signal energy estimates from I and Q channels are weighted by the power split and used for AGC control.

3.4.2.5 Adaptive Equalization



*ACM SUMS FULL CLOCK CYCLE FOR NRZ; ACM SUMS FIRST HALF CYCLE AND SUBTRACTS SECOND HALF CYCLE FOR BI-ϕ

**OPTIMAL NONLINEARITY IS TANH FUNCTION. IT CAN BE REPLACED BY A SIGN FUNCTION OR A CLIPPER.

Fig. 3.4-3. Digital Processing for Data Aided Tracking (Only I Channel Shown).

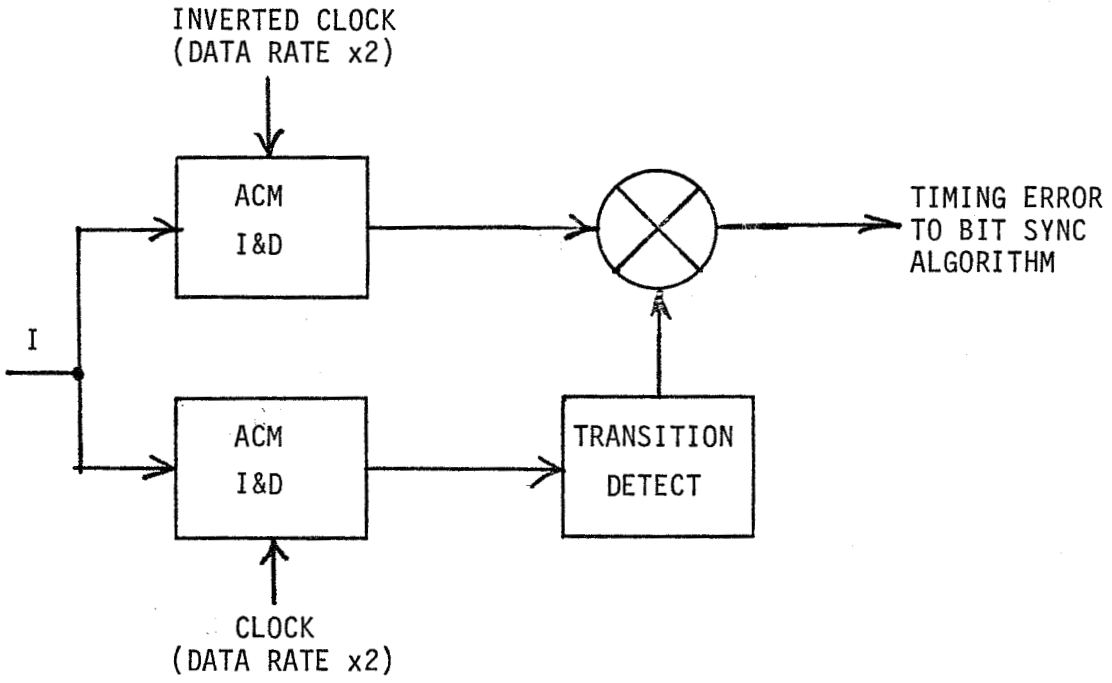


Fig. 3.4-4. Alternate Digital Processing for Tracking Bi-ϕ Signals.

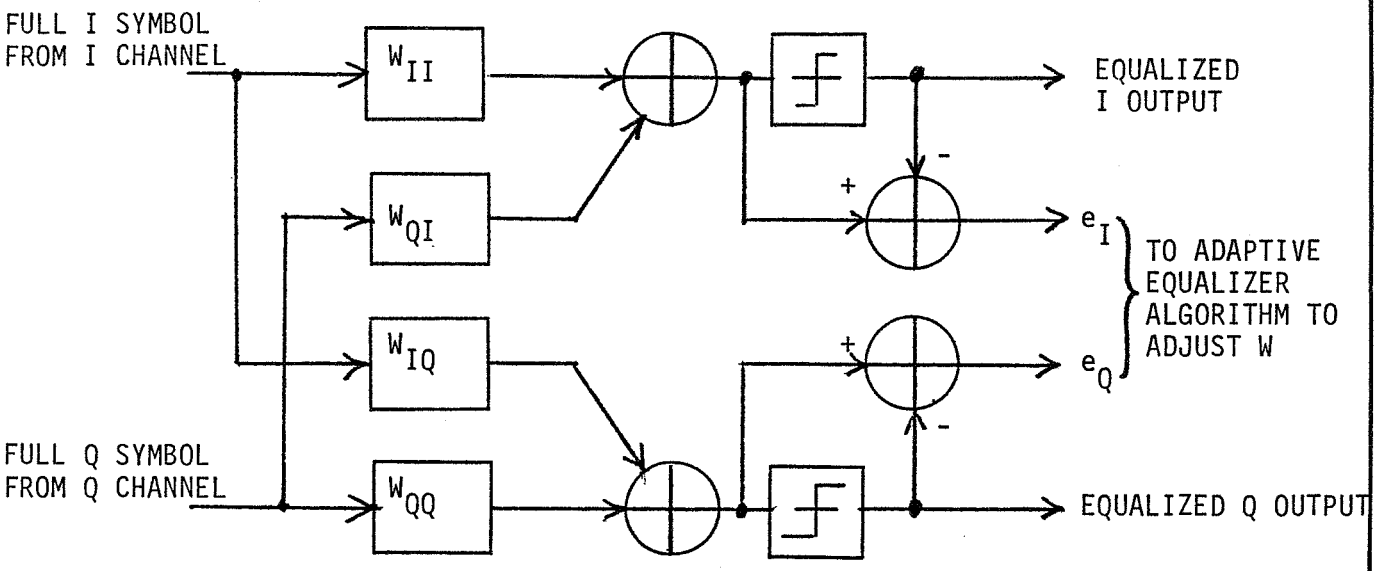
For high rate data ($\geq$ 6 Mbps/channel), adaptive equalization is employed. The technique is shown in Figure 3.4-5. The adaptation algorithm is the method of steepest descent widely described in the literature. The tap weight increments are obtained by correlating the particular tap input with the equalized error defined as the difference between the decision circuit input and output. W represents a transversal filter with settable tap weights. A 3-tap transversal filter is shown in Figure 3.4-5b and should be adequate for our purpose. Again, the error signal samples e_I and e_Q must be accumulated by a fixed length accumulator to slow down the data throughput rate before going to the adaptive equalization software.

3.4.2.6 RFI Mitigation and Viterbi Decoder

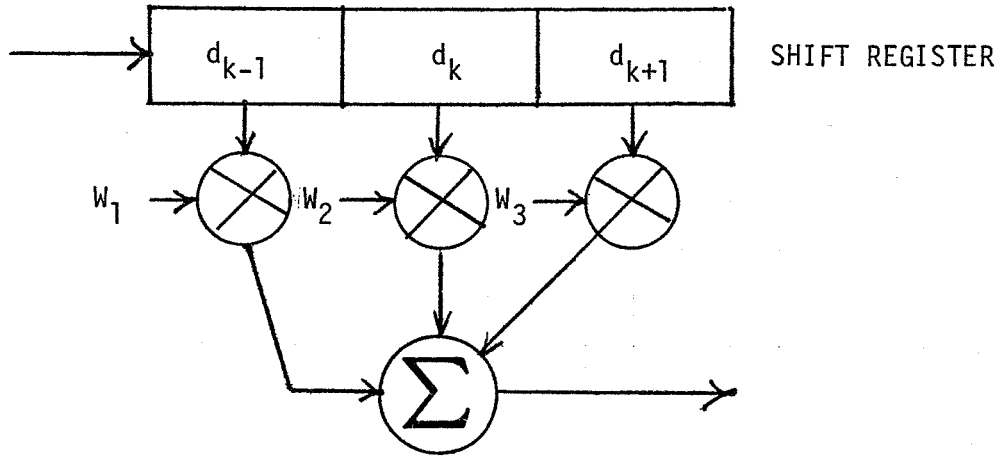
Figure 3.4-6 shows the interface between the AIRS and the existing Viterbi decoder. It is anticipated that the only required signal to integrate the operation of the decoder with AIRS is the code node sync information. Hence, the AIRS can use the existing decoder. Methods of implementing various RFI mitigation schemes in the digital processor are also indicated.

3.4.2.7 Link Performance Indicator

Link performance indication can be obtained by either measuring the SNR of the demodulated data or its pseudo probability of error. In the first method, the sample mean and variance of the absolute value of the demodulated data samples (see Figure 3.4-3) are computed to get an estimate of the SNR. However, since this computation is rather involved, a dedicated arithmetic logic unit (ALU) may be needed. A way of getting around the speed problem is to count every 5 samples or so at the highest data rate. This reduces the speed requirement for the ALU.

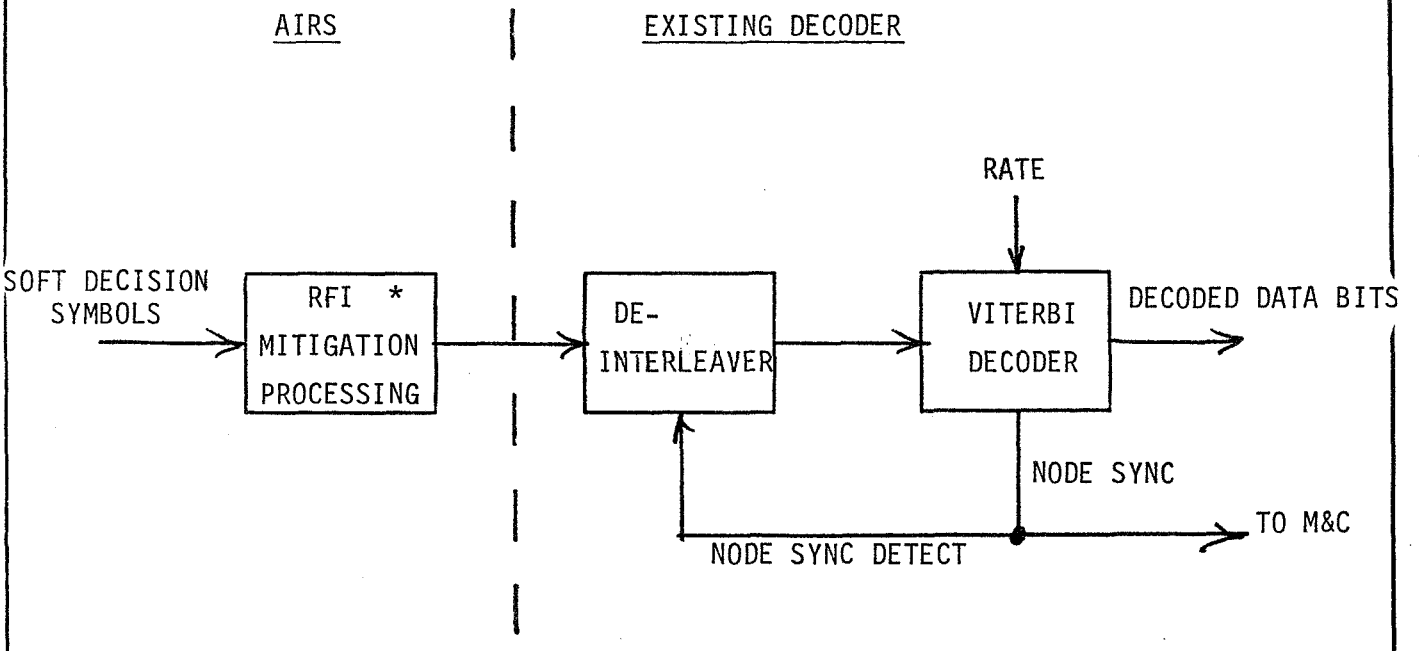


(a) Simplified Adaptive Equalizer



(b) 3-Tap Transversal Filter with Adjustable Tap Weight

Fig. 3.4-5. Digital Processing for Tapped Delay Line Equalizer.



*RFI MITIGATION TECHNIQUES

TECHNIQUE	IMPLEMENTATION
GENERAL NONLINEAR COMPRESSION	ROM; USE INPUT DEMODULATED SYMBOL AS ADDRESS
BLANKING	COMPARE WITH AVERAGE SIGNAL POWER (∿ AGC CONTROL). SET SYMBOL VALUES TO ZERO IF MUCH GREATER THAN AVERAGE
CLIPPING	COMPARE WITH THRESHOLD. FOR EXAMPLE USE 5 BITS OF INPUT SYMBOL REPRESENTATION AND ONLY 3 BITS FOR SOFT-DECISION VITERBI DECODER INPUT

Fig. 3.4-6. RFI Mitigation Processing and Viterbi Decoder.

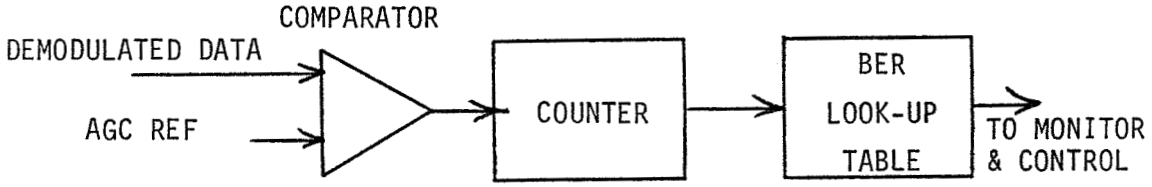


Fig. 3.4-7. Digital Processing for LPI Monitor.

The second approach is shown in Figure 3.4-7. A scaled version of the AGC reference bias is used to set a threshold. The number of signal samples failing to exceed the threshold is counted and the value of the count is related to the BER. This method is considerably simpler to implement.

3.5 Software Section

The various algorithms selected which make up the software section are briefly described in what follows. Further tradeoffs and studies are required to specify the various parameters.

3.5.1 Orbit Uncertainty Estimation

A delay-locked loop is selected. It operates off the difference between the predicted and the measured Doppler to correct for the time uncertainty in the Doppler predicts. Since the uncertainty varies slowly with time (design goal is for reacquisition, not for correcting unstable orbit), a narrow bandwidth first-order loop design suffices.

3.5.2 Doppler Compensation

If only the state vectors or ephemerides are provided to AIRS, AIRS must compute the equivalent Doppler. A design similar to one used in ADPE suffices.

3.5.3 Bit Sync

A full-window DTTL with second-order loop is selected. The bit sync closes the loop by varying the frequency and phase of the clocks controlling the sampling of the ADCs and the clearing and dumping of the accumulators.

3.5.4 CAGC

Coherent AGC off the demodulated data is used. The AGC bandwidth should be roughly 10 times smaller than the carrier loop bandwidth. The

loop is closed by setting the GCA in front of the ADC.

3.5.5 Carrier Recovery

Data-aided loop is selected. A FLL is used to pull in the carrier frequency uncertainty to approximately 25 Hz. Then the carrier loop acquires phase with a second-order loop and tracks with a third-order loop. Upon loss of lock, a second-order loop is again employed for reacquisition. The long loop design closes the loop by changing the frequency and phase of the synthesizer at 10 MHz in Figure 3.3-1.

3.5.6 LPI

Simple computations are involved and depend on the method selected.

3.5.7 RFI Mitigation

Selects nonlinear processing based on RFI model during operation.

3.5.8 Adaptive Equalization

Performs weight updates in the tapped delay lines. Since the channel model does not change rapidly with time, the equalizer is designed to acquire with a larger feedback constant and track with a smaller feedback constant in its steepest descent algorithm.

3.5.9 Lock Detection

Simple filtering and comparison operation is required.

3.5.10 PN Acquisition and Track Control

Controls switching between acquisition and tracking. Switches to a narrower PN loop bandwidth after frequency aiding from carrier recovery is available.

3.5.11 Monitor and Control

The functions are:

- Determine acquisition and tracking sequence.
- Determine optimal reacquisition strategy based on receiver

status.

- Generate monitoring signals.
- Interface with Ground Segment/Operator Control (e.g. ADPE) with serial data.

3.5.12 Self Diagnostics

The AIRS is required to report and isolate faulty subsystems. The extent shall be determined by the contractor.