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DEVELOPMENT AND FABRICATION OF A SOLAR CELL JUNCTION PROCESSING SYSTEM

Final Technical Report
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THE JPL LOW-COST SOLAR ARRAY PROJECT IS SPONSORED BY THE U.S. DEPARTMENT OF ENERGY AND FORMS PART OF THE SOLAR PHOTOVOLTAIC CONVERSION PROGRAM TO INITIATE A MAJOR EFFORT TOWARD THE DEVELOPMENT OF LOW-COST SOLAR ARRAYS. THIS WORK WAS PERFORMED FOR THE JET PROPULSION LABORATORY, CALIFORNIA INSTITUTE OF TECHNOLOGY BY AGREEMENT BETWEEN NASA AND DOE.

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DEVELOPMENT AND FABRICATION OF A SOLAR CELL JUNCTION PROCESSING SYSTEM

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ABSTRACT

A program was undertaken to develop, construct and deliver to JPL a processing system capable of producing solar cell junctions by ion implantation followed by pulsed electron beam annealing. The machine was to be capable of processing 4-inch diameter single-crystal wafers at a rate of 10^7 wafers per year. A microcomputer-controlled pulsed electron beam annealer with a vacuum interlocked wafer transport system was designed, built and demonstrated to produce solar cell junctions on 4-inch wafers with an AM1 efficiency of 12%. Experiments showed that a non-mass-analyzed (NMA) ion beam could implant 10 keV phosphorous dopant to form solar cell junctions which were equivalent to mass-analyzed implants. A NMA ion implanter, compatible with the pulsed electron beam annealer and wafer transport system was designed in detail but was not built because of program termination.

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INTRODUCTION AND SUMMARY

1.1 OBJECTIVE

The overall objective of Spire's effort was to develop, construct and deliver to JPL a processing system capable of producing solar cell junctions by ion implantation followed by pulsed electron beam annealing. The machine was to be capable of processing 4-inch (101.6 mm) diameter single-crystal Czochralski wafers at a rate of 10^7 wafers per year (approximately 1 wafer every 2 seconds). An artist's conception of the junction processor is shown in Figure 1-1.

The wafers were to be P-silicon (boron) with a maximum bulk resistivity of 2 ohm-cm and maximum thickness of 0.010 inches (0.25 mm). The wafers were to be carried by a transport mechanism into and out of the vacuum chambers where the ion implantation and pulsed electron beam annealing processes take place.

Spire was to integrate, test and demonstrate the system prior to delivery; and detailed operating and maintenance manuals were to be prepared for the machine. Based on the manufacturing experience and other inputs, estimates of component lifetimes and costs were to be prepared. This information was to be used for a comprehensive analysis, in accordance with the Solar Array Manufacturing Industry Costing Standards (SAMICS), of the costs associated with the use of the junction processor.

1.2 TASKS

The objectives of the program were to be satisfied by the performance of 5 tasks, each with a detailed set of subtasks.

1.2.1 Task 1 - Development of Pulsed Electron Beam Subsystem

The pulsed electron beam subsystem was to be capable of annealing the damage caused by ion implantation into the crystalline lattice of 4-inch silicon wafers and of electrically activating the implanted dopant material. Before building the subsystem, however, Spire was required to select the optimum method of removing the ion

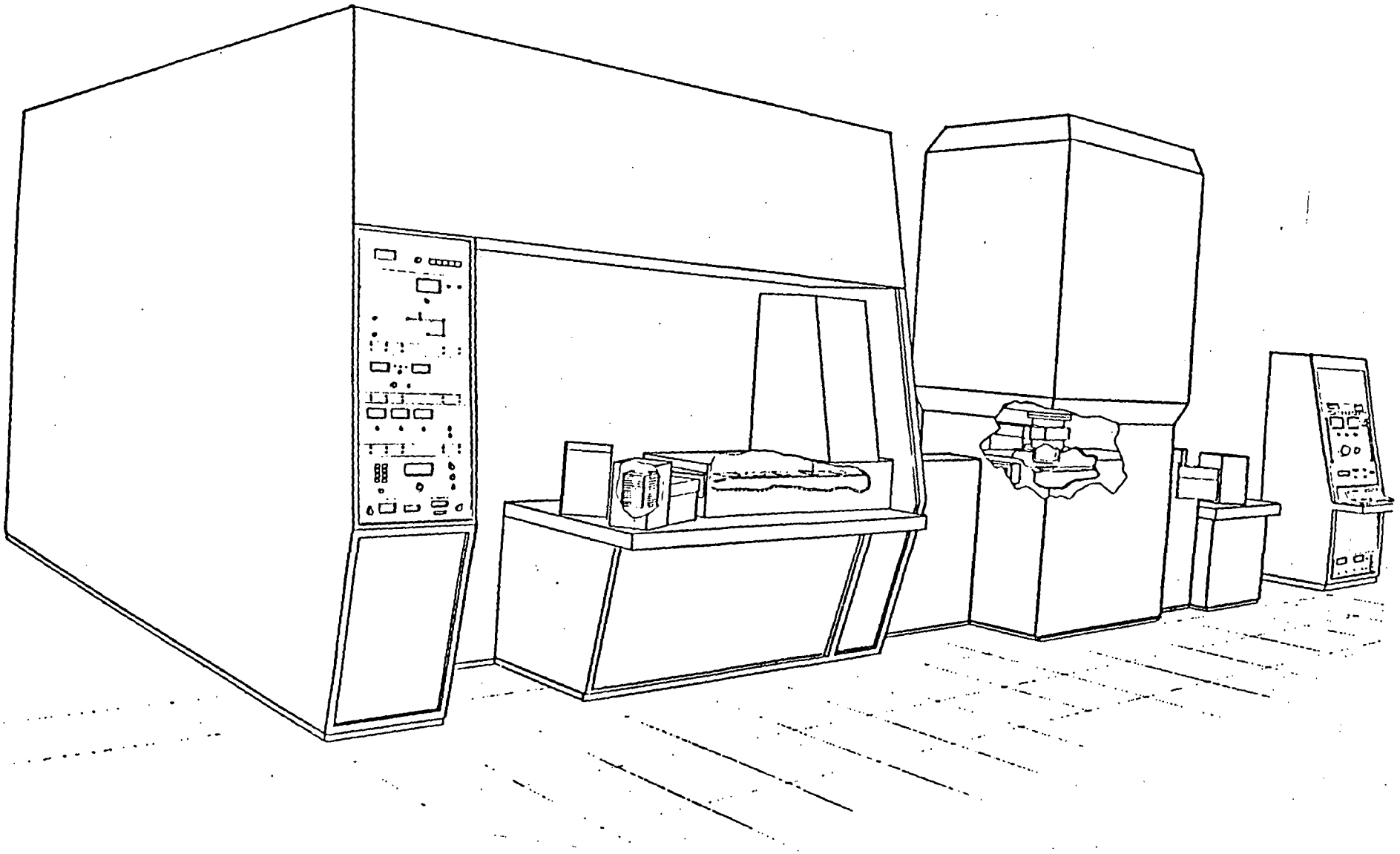

FIGURE 1-1. ARTIST'S CONCEPTION OF SPIRE/JPL JUNCTION PROCESSOR.

implantation damage among four alternatives: (1) single-pulse, full wafer coverage; (2) single-pulse, partial wafer coverage - liquid epitaxy with step-and-repeat to achieve full coverage; (3) multiple-pulse, full wafer coverage - solid epitaxy; and (4) multiple-pulse, partial wafer coverage - solid epitaxy with step-and-repeat to achieve full wafer coverage.

After determining the best pulsed electron beam annealing method, Spire was then to design and fabricate the pulsed annealer to satisfy the requirements presented above. The initial design was to be a "stand-alone" system whose operation could be demonstrated independently.

1.2.2 Task 2 - Wafer Transport Development

Spire was to develop a wafer handling and transport subsystem capable of transporting 4-inch diameter silicon wafers through the junction processor at a rate of 10^7 wafers per year. The option was available for using single or batch (cassette) wafer transfer between the ion implantation and pulsed electron beam subsystems. The wafer transport system also was to include handling mechanisms for correctly orienting the wafers during the ion implantation and pulsed anneal processes as well as interlocked vacuum valves to prevent accidental loss of vacuum in the ion implanter and pulsed annealer subsystem.

1.2.3 Task 3 - Ion Implanter Development

The initial objective of this task was to modify the Government-owned ion implanter, Varian/Extrion Model 200-100, located at Spire to be capable of processing 4-inch diameter silicon wafers at a rate of 10^7 per year. The ion implanter was to provide a fluence of at least 2.5×10^{15} ions/cm^2 of 10 keV phosphorous with a uniformity across the wafer of less than $\pm 10\%$.

Later in the program, it was determined that the best approach to this task was to develop a new ion implanter design utilizing a non-mass-analyzed (NMA) ion accelerator which would satisfy the technical requirements with reduced technical complexity and costs.

1.2.4 Task 4 - Junction Processing System Integration

The pulsed electron beam annealer, wafer transport, and ion implanter subsystems developed in Tasks 1, 2, and 3 were to be integrated, tested and demonstrated by processing wafers at the rated throughput. Selected wafers were to undergo sheet resistivity mapping by Spire and formed into solar cells. The performance of these solar cells were to be evaluated by Spire as a part of this task. Additionally, operating and maintenance manuals of the junction processing equipment were to be written.

1.2.5 Task 5 - Junction Processing System Cost Analyses

Spire was to estimate component lifetimes and failure rates for the junction processing system as part of a cost analysis for the total system. The estimates were to be derived from established data sources and from experience gained during the development, integration and testing phases of the system. This information was to be used in a cost analysis of the junction processor performed in accordance with the Solar Array Manufacturing Industry Costing Standards (SAMIS).

1.3 SUMMARY OF ACTIVITIES

1.3.1 Task 1 - Development of Pulsed Electron Beam Subsystem

A series of annealing experiments showed that the optimum pulsed electron beam annealing technique was single-pulse, liquid epitaxy with full coverage over the 4-inch diameter wafer. The electron beam pulser design was then based on this method of annealing.

A pulsed electron beam annealer, designated SPI-PULSE 7000 was designed, fabricated and successfully tested at a rate of 1 wafer every 2 seconds. Single electron beam pulses were used to anneal 4-inch diameter ion implanted silicon wafers over their entire surface.

Surface resistivity maps were made of several pulse-annealed silicon wafers and solar cells made from the wafers. This information was presented in a report which is included in Appendix 1. The cell characterization indicated that the AM1 efficiency attainable with this technology is approximately 12% over a 4-inch wafer. This average efficiency could be improved by improvements in the metalization on the front of the cell.

1.3.2 Task 2 - Wafer Transport Development

A vacuum-locked walking beam wafer transport was designed and built by a subcontractor to Spire, and the interim system was installed on the SPI-PULSE 7000 electron beam pulser. Spire designed and built cassette elevators and wafer input and output mechanisms for the transport and a wafer lifter device for the pulse annealing station. These systems were demonstrated to operate at a rate of 1 wafer every 2 seconds.

A vacuum-locked walking beam transport system was designed for the ion implanter subsystem which is compatible with the interim transport system of the pulsed annealer. Although detailed design drawings were made, no fabrication was initiated because of the termination of the junction processor development program.

1.3.3 Task 3 - Ion Implanter Development

A series of experiments were conducted using an ion implanter test facility which demonstrated that a non-mass-analyzed (NMA) phosphorous ion implantation gives solar cell performance which is as good, if not better, than conventional, mass-analyzed ion implants. Based on these results, a new NMA ion implanter was designed and some components fabricated.

Beam control experiments were performed in the test facility and ion beam steering and defocusing demonstrated to satisfy the dose uniformity requirements across 4-inch diameter wafers.

Detailed drawings of all components of the ion implanter were made. The program was terminated after the fabrication of a limited number of the components.

1.3.4 Tasks 4 and 5 - System Integration and Cost Analyses

The development program was terminated before the system integration and cost analysis could be performed. An operation and maintenance manual for the pulsed electron beam annealer was written and is included in Appendix 2 of this report.

SECTION 2
TASK 1 - DEVELOPMENT OF PULSED ELECTRON BEAM SUBSYSTEM

2.1 GENERAL

The development of the pulsed electron beam subsystem consisted of three subtasks. First, developmental testing to determine the best approach for annealing 100-mm diameter silicon wafers, electron beam control experiments, and wafer preheat experiments. Second, design and fabrication of the electron beam pulser. Third, testing and evaluation of the pulsed annealer subsystem, including large area annealing experiments, testing of pulser lifetime and reliability, and cell processing. Each of these subtasks was performed successfully.

2.2 DEVELOPMENTAL TESTING

2.2.1 Solid Phase Annealing Experiments

Experiments were carried out to determine the feasibility of pulse-annealing ion implantation damage by a series of low-fluence pulses from a large-area electron beam. This method of annealing would have the advantage of requiring a smaller beam energy per pulse than single-step, liquid-phase regrowth of the amorphous layer formed by ion implantation.

Using Spire's SPI-PULSE 5000 accelerator, it was found experimentally that multiple pulses by an electron beam with a fluence less than about 0.5 J-cm^{-2} produced polycrystalline regrowth of the amorphous layer if the wafer was allowed to cool between pulses. Increasing the total fluence by using a pulse duration greater than 100 ns (up to 1 microsecond) resulted in damage to the wafer by surface cracking. This effect could be avoided only by heating the wafer to 300°C or greater during the pulse annealing process.

Based on these experiments, it was concluded that solid-phase annealing by a series of short, low-fluence pulses or by single, low-power pulses of microsecond duration is not practical for the pulsed electron beam processor. Liquid-phase annealing, on the other hand, has been demonstrated conclusively to form solar cell junctions which are of nearly equal performance to those formed by furnace annealing.

2.2.2 Overlapping of Pulse-Annealed Regions

An experiment was conducted to evaluate the effect of overlapping high-fluence pulses of electrons on ion-implanted silicon solar cell junctions. The experiment simulated the conditions which would be encountered in the fabrication of solar cells which were annealed by multiple pulses of overlapping electron beams. Wafers of 10-ohm-cm, p-type silicon were implanted with 2.5×10^{15} cm^{-2} of 10-keV $^{31}P^{+}$ ions and pulse annealed at a fluence of 1 $J\text{-}cm^{-2}$. Half the wafers were subjected to a second pulse of the same fluence. The annealed regions of the wafers were then formed into 2 x 2-cm solar cells and the voltage-current characteristics of the cells were measured under AM0 illumination. For test purposes, these cells were not constructed with an antireflection coating or a back-surface-field structure. The efficiency of the single- and double-pulsed cells was as follows:

Single-Pulsed Cells

Cell No.	Efficiency (%)
1	8.1
2	8.3
3	8.2

Double-Pulsed Cells

4	6.7
5	6.7
6	6.3

The voltage-current characteristics of cells No. 3 and No. 4 are shown in Figure 2-1. The efficiency of the single-pulsed cells, although low because the cell formation process was not optimized, is clearly greater than the efficiency of the double-pulsed cells. The loss of efficiency is attributed to increased junction depths and damage from thermal stresses caused by the second pulse onto the already annealed structure of the cell. It seems clear from these and earlier experiments at Spire that solar cells with large overlapping areas of pulsed electron beam annealing would be inferior to single-pulsed cells.

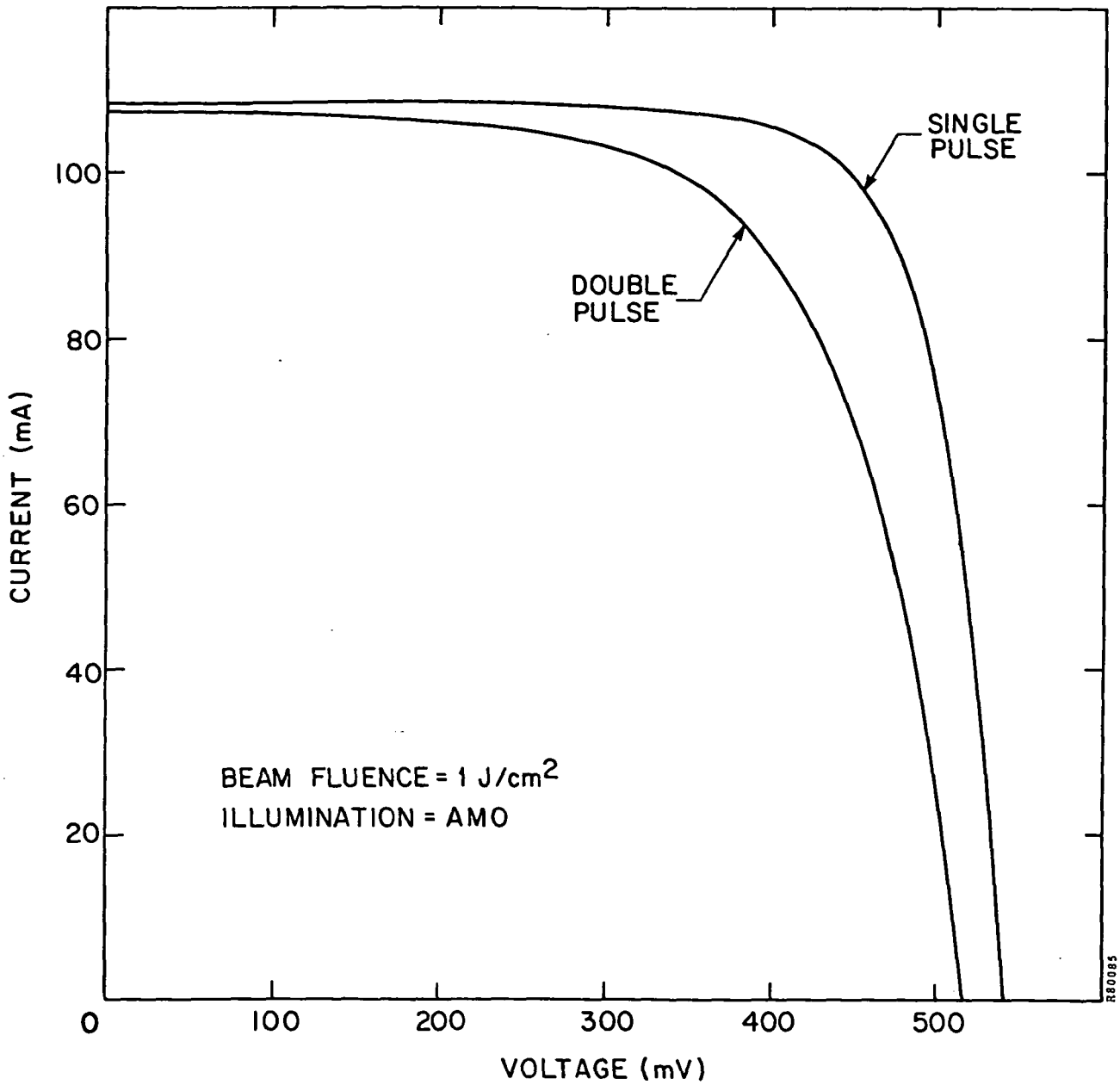

FIGURE 2-1. VOLTAGE-CURRENT CHARACTERISTICS OF SINGLE- AND DOUBLE-PULSE ANNEALED SOLAR CELLS.

We have also observed that implanted wafers annealed by several abutting, nonoverlapping pulses have a high risk of shorting the photovoltaic junction. The shorting occurs along grain boundaries of the polycrystalline region which is formed at the low-fluence edge of the pulsed electron beam. Complete regrowth of the polycrystalline region between the abutting areas would require special processing which would greatly increase the cost and complexity of the annealer.

We concluded from these tests that the use of a single pulse of electrons to cover the entire surface of the wafer is the preferable technique for pulse annealing in the junction processor. On this basis, we made the decision to develop a pulsed electron beam subsystem which is capable of annealing 10-cm-diameter wafers in a single pulse.

2.2.3 Beam Control Experiments

With pulsed electron beam currents approaching 50 kA in the annealer, the conduction of this current away from the wafers during the annealing step is an important design consideration. If the electron beam could propagate in a low-density plasma, partial space charge and current neutralization of the beam would be provided by the low-energy ions and electrons in the plasma. Thus a lower net current would be carried to the surface of the wafer.

A series of experiments was performed on the SPI-PULSE 5000 in which argon gas was introduced into the diode region of the pulser. Modifications to the standard carousel vacuum-process chamber met the experimental requirement of maintaining a controlled and measured gas pressure in the diode region.

The argon was leaked into the back of the chamber through an ultrafine needle valve. The diffusion pumps were throttled down to maintain steady pressure values from 0.1 to 40 microns. The pressure was measured using a McLeod gauge for the higher pressure values and a calibrated thermocouple gauge for values below 10 mTorr.

Before conducting experiments, the effect of the gas pressure on the beam was measured. Diode voltage and current monitor traces were used to determine the peak voltage, current and voltage pulse width, as shown in Figure 2-2. A carbon calorimeter

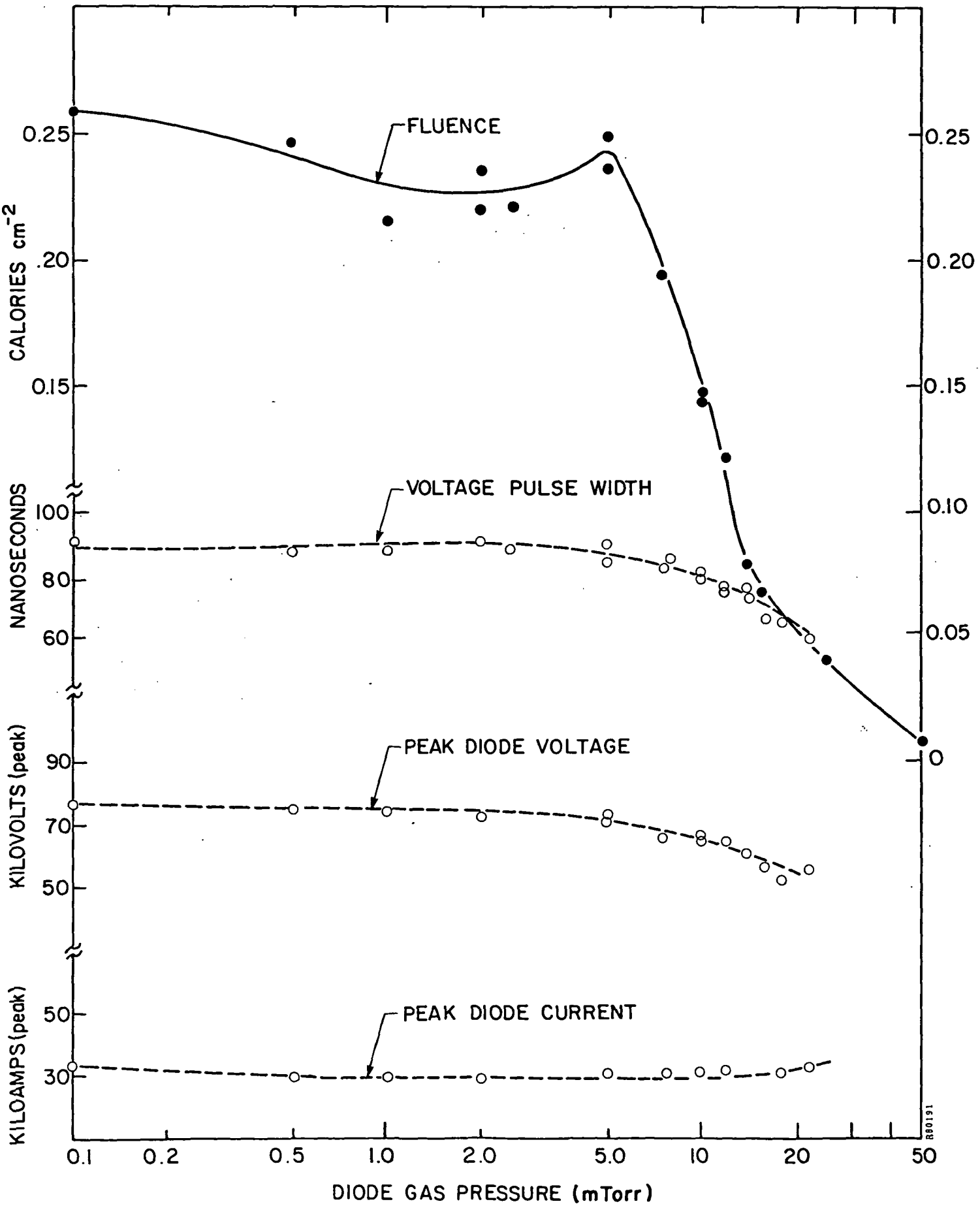

FIGURE 2-2. BEAM PARAMETERS VERSUS GAS PRESSURE.

was used to measure the fluence on the beam axis, and ion-implanted test wafers were used as witness plates to determine the beam profile. At a "maximum" pressure the charging voltage and magnetic field were varied to obtain a uniform anneal for constant fluence experiments.

Experiments were first performed using a standard 2-inch-beam setup with a 90 mil anode-to-cathode gap and a sample spacing of 5 mm. Calorimetry data was taken for pressures from 0.5 to 14 mTorr at a 150 kV charging voltage. The uppermost curve in Figure 2-2 presents the results of this data. Test wafers were shot at high vacuum, then at argon pressures from 6 to 22 mTorr. The high-vacuum anneal showed some weak spots. At 6 mTorr a weak center surrounded by an annular annealed region appeared and grew until fluence was almost totally lost at 22 mTorr. The outline of the anneal became more circular at 8 mTorr and remained so for higher pressures. These experiments showed that with an argon background gas, process chamber pressures higher than 14 mTorr would result in loss of useful beam fluence. Even though these experiments did not show a significant improvement in beam uniformity with increased diode gas pressure, another variable for beam control was identified to match the pulse generator load for large diode gaps.

2.2.4 Wafer Preheat Experiments

During ion implantation in a large-volume production line, the wafers would be heated to temperatures close to 100°C by the ion beam. Since this heating could influence the pulse annealing process, a number of experiments using a specially designed infrared wafer heater were conducted. The SPI-PULSE 5000 accelerator was used to carry out these tests. The infrared substrate heater allowed the test wafers to be heated in vacuum to temperatures through 400°C with only a 1°C per second temperature drop after heater turnoff. Early tests indicated that preheating followed by a cooldown period before pulsed electron beam annealing does not offer any advantage. However, wafers directly annealed by a pulsed electron beam while hot showed a somewhat more uniform anneal. Finished cell characteristics were identical for wafers pulsed cold or heated, if followed by a 400°C contact sinter. Further preheat testing is necessary to determine whether preheat may raise the damage threshold level. As a result of these experiments, no specific provisions for wafer preheating were included in the design of the pulsed electron beam annealer.

2.3 PULSER DESIGN AND FABRICATION

Based on the results of the developmental experiments, the pulsed electron beam subsystem, designated SPI-PULSE 7000, was designed and fabricated. The pulser includes an electron accelerator which can be discharged once every 2 seconds for single-pulse annealing of 10-cm-diameter silicon wafers. An interim wafer handling system was also designed and built (see Section 3) to move wafers into and out of the vacuum chamber which houses the electron accelerator and beam control apparatus.

2.3.1 Design Calculations

The electrical parameters of the pulsed annealer were investigated using a simple computer model which has been shown to predict the operation of existing accelerators at Spire rather closely. Lumped circuit parameters were used to model the pulser system, and the electron beam accelerator was represented as a space-charge-limited diode with an anode-cathode gap which closes at constant speed. The circuit model used in the calculations is shown in Figure 2-3, where R, L, C and V_o are, respectively, the series resistance, inductance, capacitance and initial charging voltage of the capacitor. The field-emission diode has a radius, a, a gap, g, and an expansion velocity of the cathode plasma, v.

Results of calculations of the energy fluence at the surface of a 10-cm-diameter wafer as a function of store capacitance (inductance held fixed) and series inductance (capacitance held fixed) is shown in Figure 2-4. The crossover point at a fluence of 1.8 J-cm^{-2} is the design-point chosen for the SPI-PULSE 7000. The computer model indicates that the average energy of the electrons is 18.6 keV under these conditions.

On the basis of the computer calculations and the past experience at Spire in annealing smaller diameter wafers, the electrical parameters chosen for the SPI-PULSE 7000 are as follows:

Total Capacitance:	40 nF
Front-End Inductance:	100 nH (approx.)
Maximum Charging Voltage:	300 kV

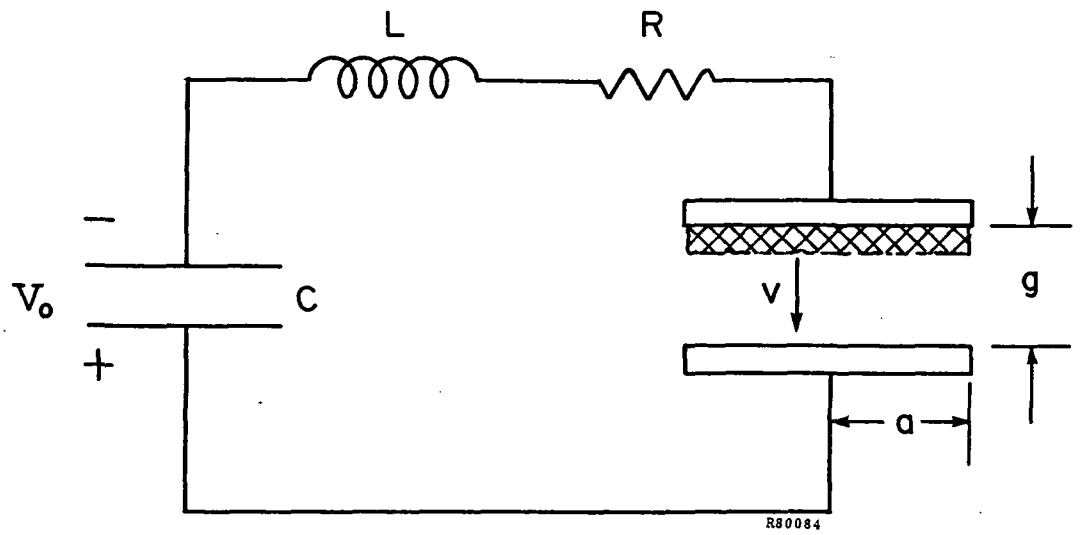

FIGURE 2-3. LIMITED PARAMETER CIRCUIT MODEL OF PULSED ELECTRON BEAM ANNEALER.

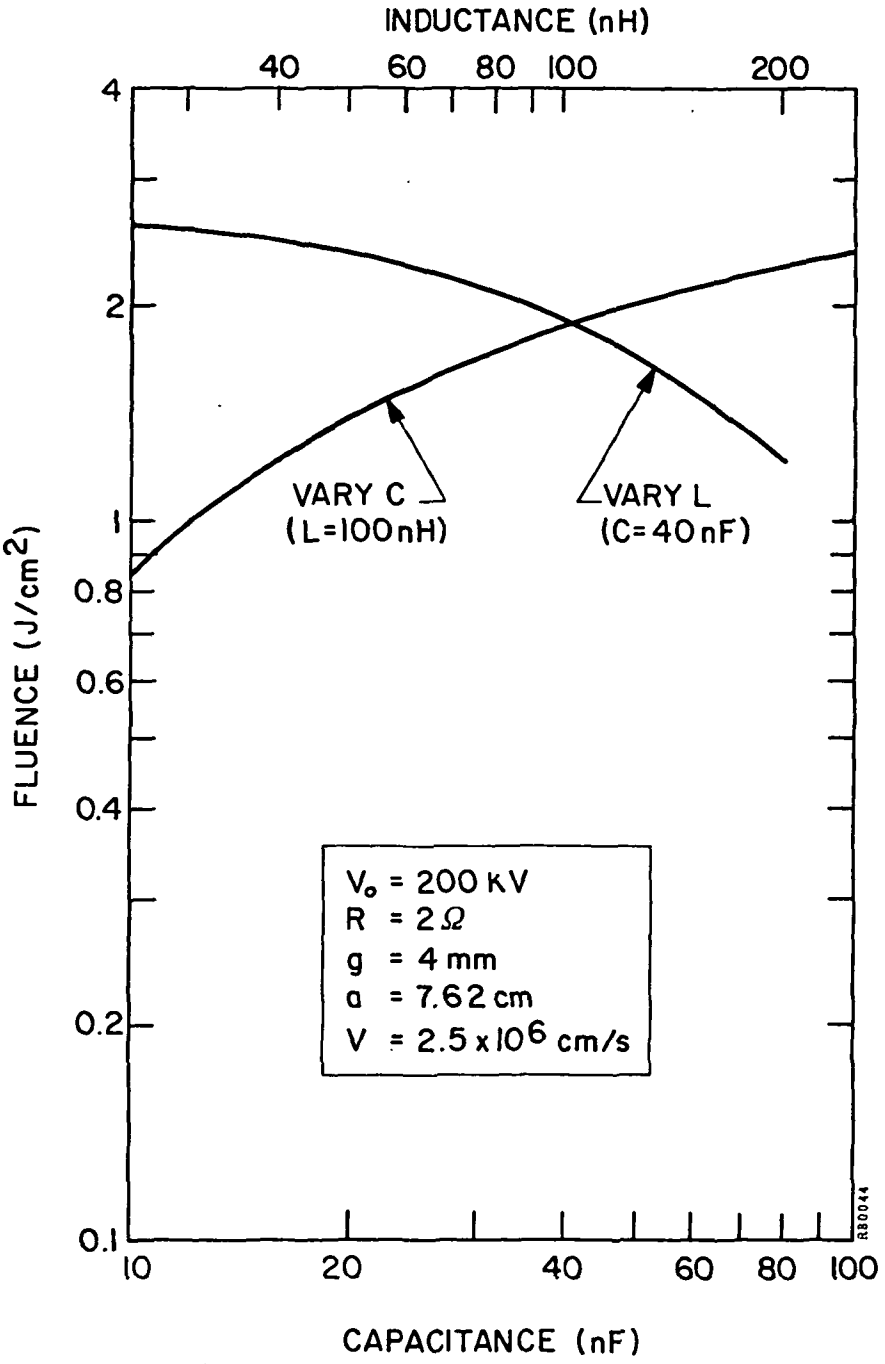

FIGURE 2-4. RESULTS OF ELECTRICAL MODELING OF PULSED ELECTRON BEAM ANNEALER.

Operating Charging Voltage:	200 kV
Maximum Charging Current:	15 mA
Pulse Repetition Rate:	0.5 to 1 s^{-1}

2.3.2 Design of Energy Store

Because of the high charging voltages and the low circuit inductance required in the pulser, we decided to break down the energy store into several separate capacitors charged and discharged in parallel. A schematic diagram of this arrangement is shown in Figure 2-5. The modular nature of the energy store gives the possibility of varying circuit parameters and eases the problems of mechanical assembly and disassembly.

The capacitive energy store consists of as many as 19 parallel-charged transmission lines. The characteristics of the individual lines are as follows:

Capacitance:	2.9 nF
Inductance:	14.2 nH
Electrical Length:	104 cm
Overall Length:	135 cm
Diameter:	24.1 cm
Dielectric Thickness:	0.79 cm

The dielectric material of the line is a high-strength epoxy which is cast around an aluminum cylinder, the central electrode of the coaxial line. The outer conductor is a conductive coating placed on the dielectric after casting.

The lines are placed vertically in a hexagonal arrangement in a vessel which is pressurized with dielectric gas. The capacitor array is charged by a high-voltage electronic power supply and discharged into the accelerator by a mechanically actuated switch as shown in Figure 2-5.

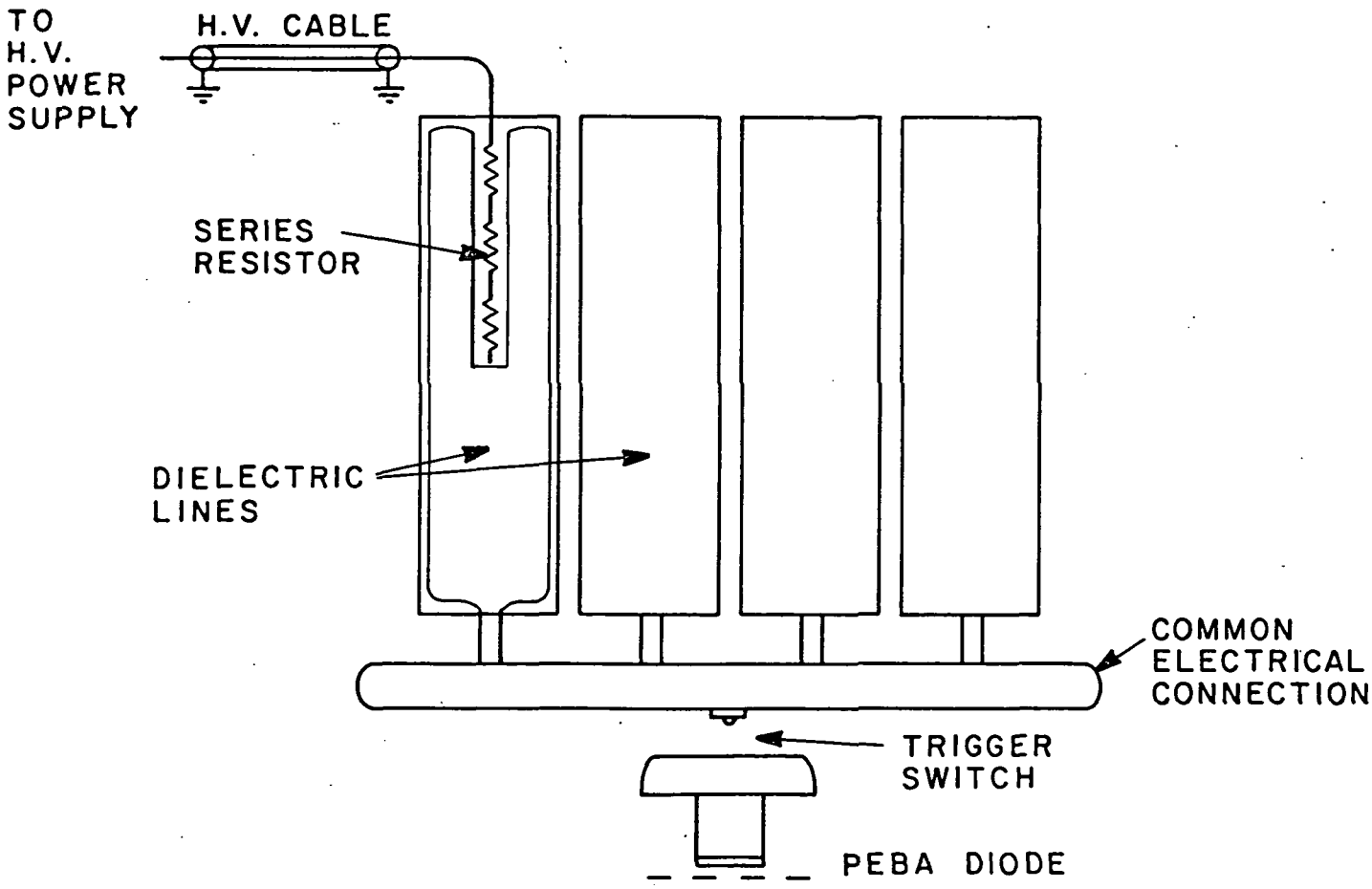

FIGURE 2-5. SCHEMATIC OF MULTIPLE-LINE ENERGY STORE AND PARALLEL CHARGING AND DISCHARGING SYSTEMS.

2.3.3 Pulser Subsystem Design

The major elements of the pulsed electron beam subsystem are shown schematically in Figure 2-6. The pressure vessel contains the capacitative energy store discussed in Section 2.3.2; the vacuum process chamber contains the electron beam diode, the magnetic beam guiding structure, and the wafer handling and transport mechanism. Figure 2-7 is a functional block diagram of the elements of the subsystem; all of these elements were designed to be controlled by a microprocessor controller.

2.3.4 Pulser Subsystem Fabrication and Assembly

Following the design computations and a number of experimental verifications of design principles, the pulsed electron beam subsystem and an interim wafer transport system were designed and fabricated. The transport systm is described in Section 3. Figure 2-8 shows the pulser subsystem after all components were fabricated and assembled. An interior view of the processing chamber, Figure 2-9, shows one of the pole pieces of the beam guiding field electromagnet (center), a part of the wafer transport track (sides), lifter mechanism (center), and the anode structure (above) of the electron beam accelerator diode. Figure 2-10 shows the guiding field electromagnet coil and yoke before assembly on the pulser. The electromagnet is located behind the vacuum chamber and is not visible in Figure 2-8.

2.3.5 Pulser Subsystem Testing

The pulsed electron beam annealer is comprised of seven separate subsystems. These are the vacuum system, wafer transport, insulating gas supply for the high voltage tank, magnet and its power supply, high voltage power supply, diagnostic equipment and electronic controls. Each subsystem was tested both separately and under coordinated operation. The microprocessor control system was used for all tests. It was not adversely affected by triggering of the pulse generator or operation of any other part of the pulser system.

Vacuum System

Full operation of the cryopumped vacuum system was accomplished with an average indicated pressure in the process chamber at 2×10^{-6} torr. Pressures in the 10^{-7} torr range were commonly measured after a few hours of pumping.

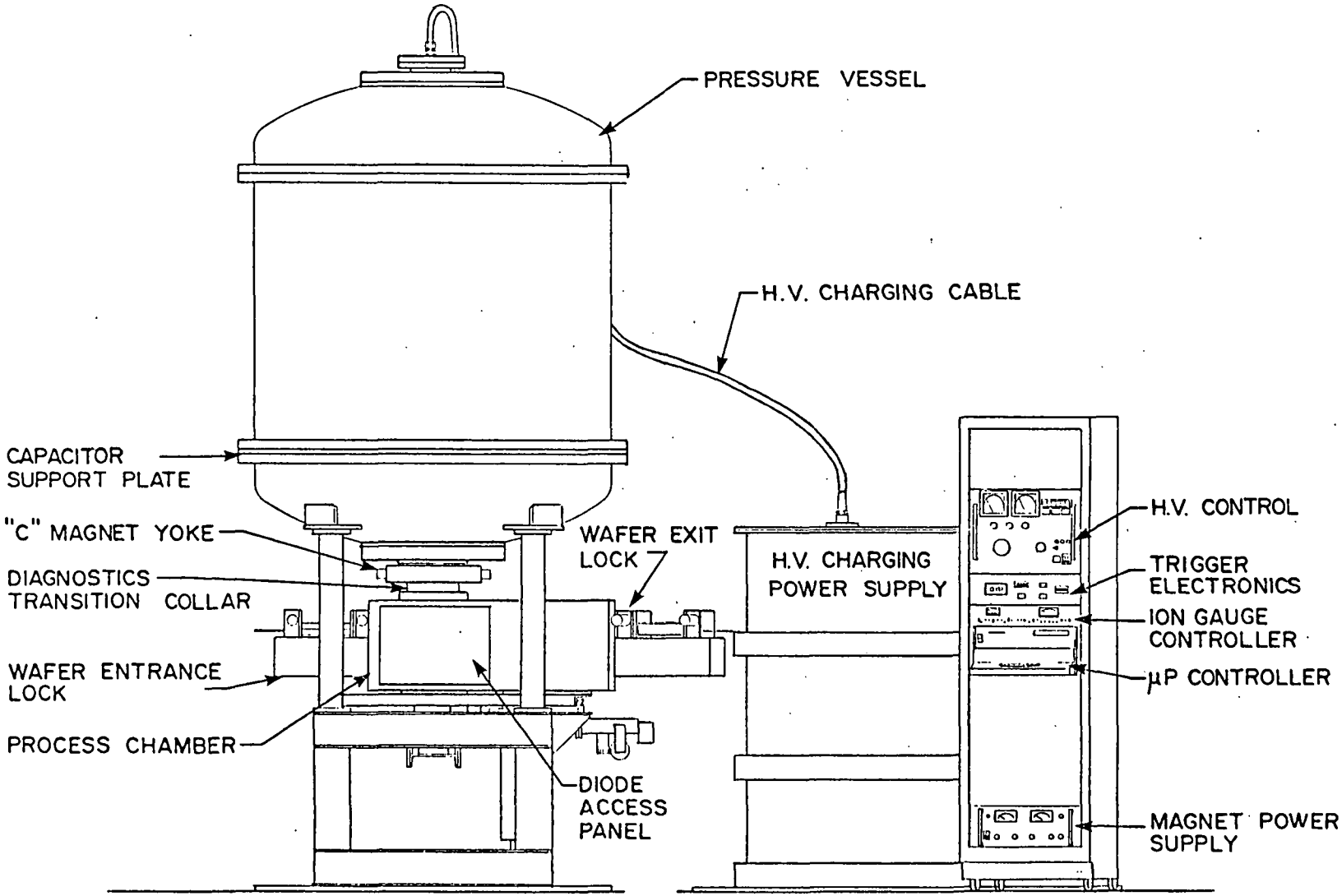

FIGURE 2-6. SPI-PULSE 7000 SCHEMATIC DIAGRAM.

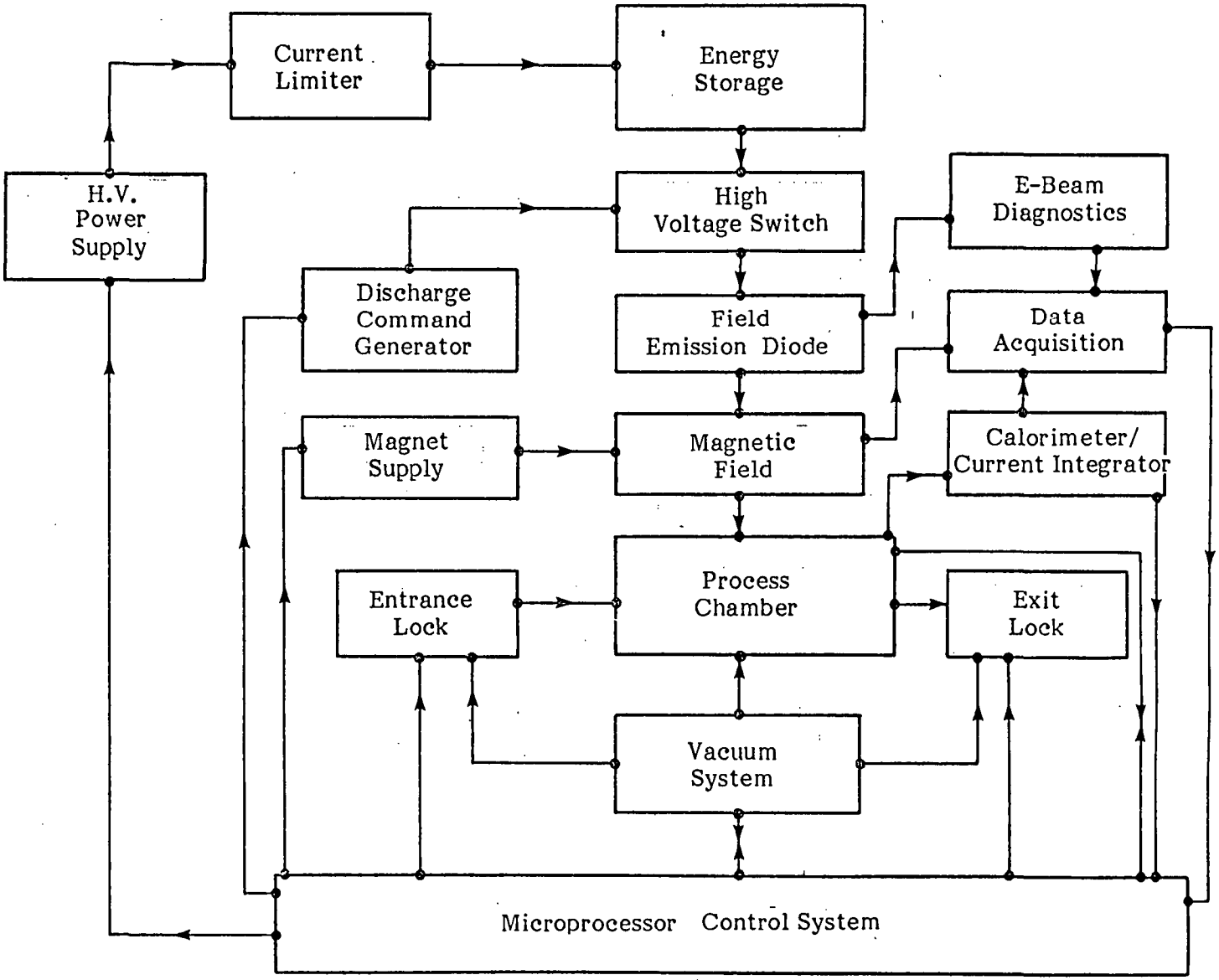

FIGURE 2-7. SPI-PULSE 7000 FUNCTIONAL BLOCK DIAGRAM.

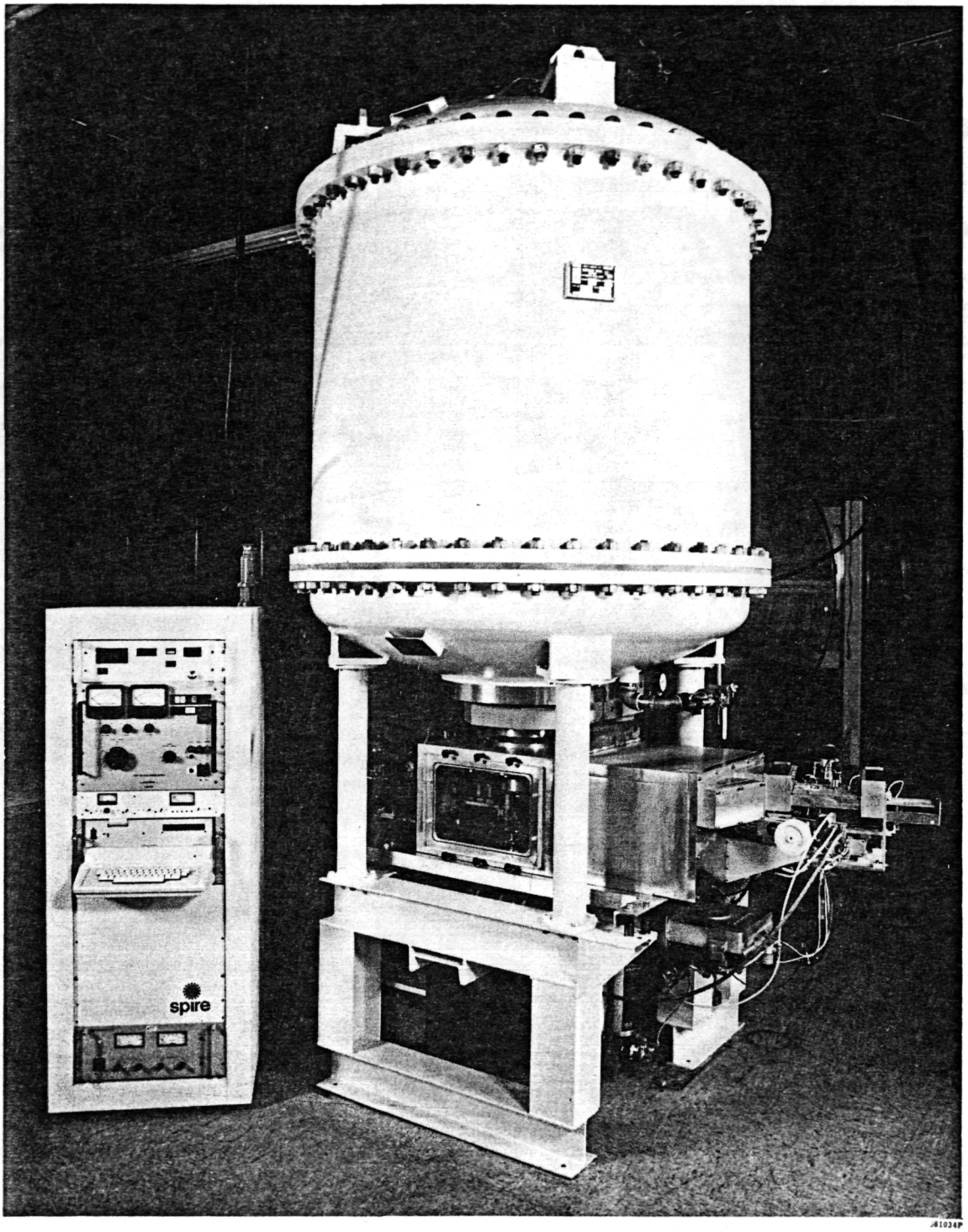

FIGURE 2-8. PHOTOGRAPH OF SPI-PULSE 7000 PULSED ELECTRON BEAM SUBSYSTEM.

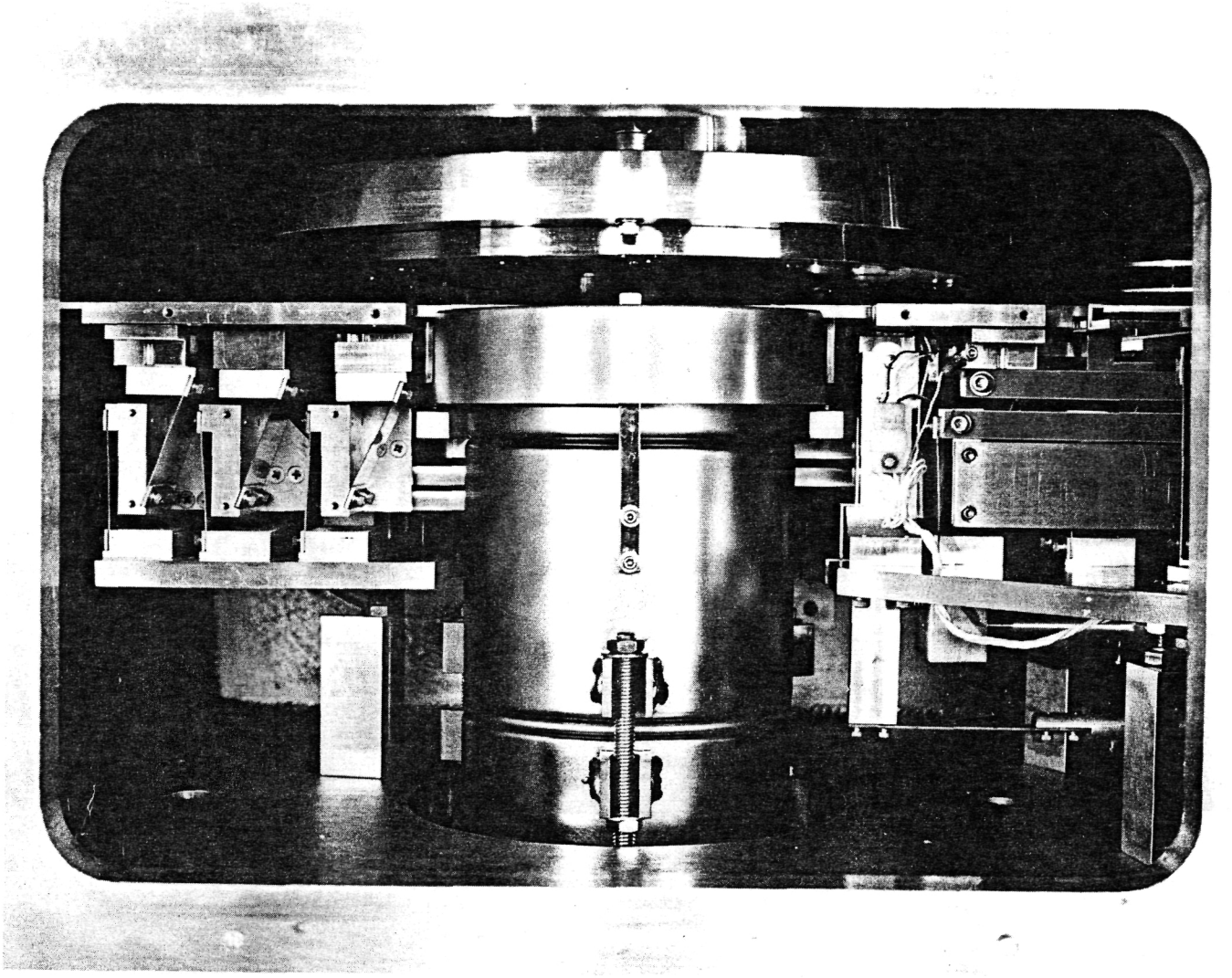

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FIGURE 2-9. VIEW THROUGH FRONT PORT OF WAFER PROCESSING CHAMBER.

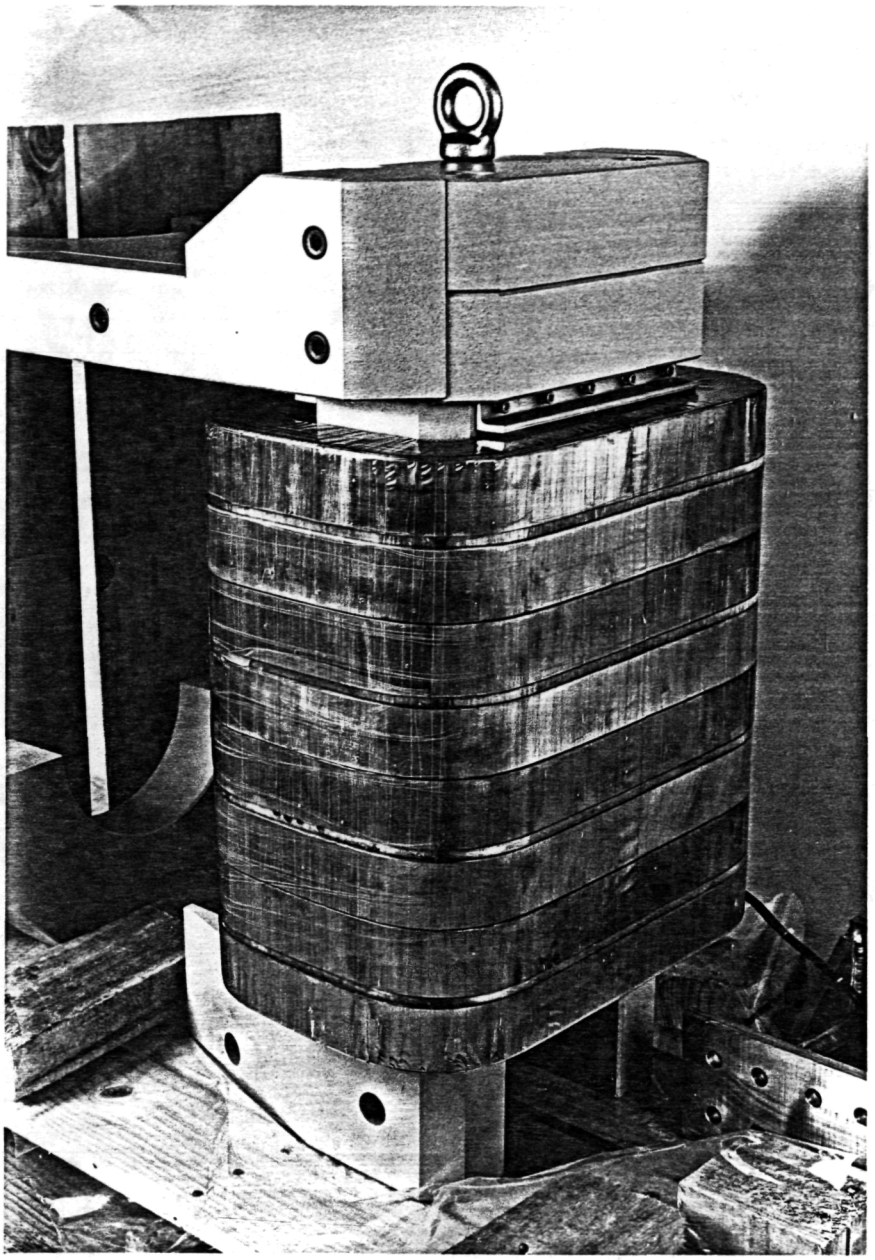


FIGURE 2-10. BEAM GUIDING FIELD COIL AND YOKE BEFORE ASSEMBLY OF PULSER SUBSYSTEM.

Interim Wafer Transport

The interim wafer transport, described further in Section 3, and the mechanism to lift the wafers into place for pulsed annealing were demonstrated to operate at a rate of one wafer every 3 seconds. The magnetic field in the region of the lifter causes no adverse effects on the operation of the transport.

Insulating Gas System

The energy store and high-voltage switch were designed to operate with 100 psi of insulating gas. A mixture of nitrogen and carbon dioxide was found to give satisfactory charging and switching at voltages up to 180 keV. The addition of a few percent of SF_6 was required to prevent arcing at voltages above 180 kV.

Magnetic Field System

The magnet was tested for power consumption, cooling and field strength. This system is required for uniform electron beam irradiation of the samples. The maximum field is limited by saturation effects, particularly above 2.5 kG. However, annealing experiments have shown that the optimal field is below 2 kG. At this 2 kG level the magnet draws only 130 watts, significantly below the 3 kW first estimated for this subsystem in an early SAMICS analysis of the pulsed electron beam annealer. This represents a significant savings in total power and cooling requirements.

High-Voltage Power Supply

The first high-voltage power supply for the pulser was tested up to its maximum, no-load voltage rating of 180 kV. At 160 kV, this power supply had a demonstrated output of 5 mA. Later in the program, this power supply was replaced by a 300 kV, 17 mA unit so that tests at higher charging voltages could be performed. The new supply performed satisfactorily over all of its voltage and current range.

Beam Diagnostics

Diagnostic equipment for the electron beam pulser includes diode voltage and current monitors and an electron beam calorimeter. The diode voltage monitor, a capacitive voltage divider measured directly on the diode "shank", was calibrated using a

low-voltage pulser and found to have a calibration factor of 1710 volts per signal volt output. The current monitor, which uses a chain of shunt resistors in the diode current path, was measured to have a calibration factor of 73 amperes per signal volt.

The calorimeter consists of 29 disks arranged in the pattern shown in Figure 2-11. When irradiated by the electron beam, the disk rises in temperature about 4-6°C and cools slowly with typical time constants exceeding 8 seconds. The disks are within $\pm$5% of the average calibration which is corrected for energy radiated away when the surface temperature is high, immediately after the pulse. Carbon is the only material which can be used which will not melt or spall from this radiation.

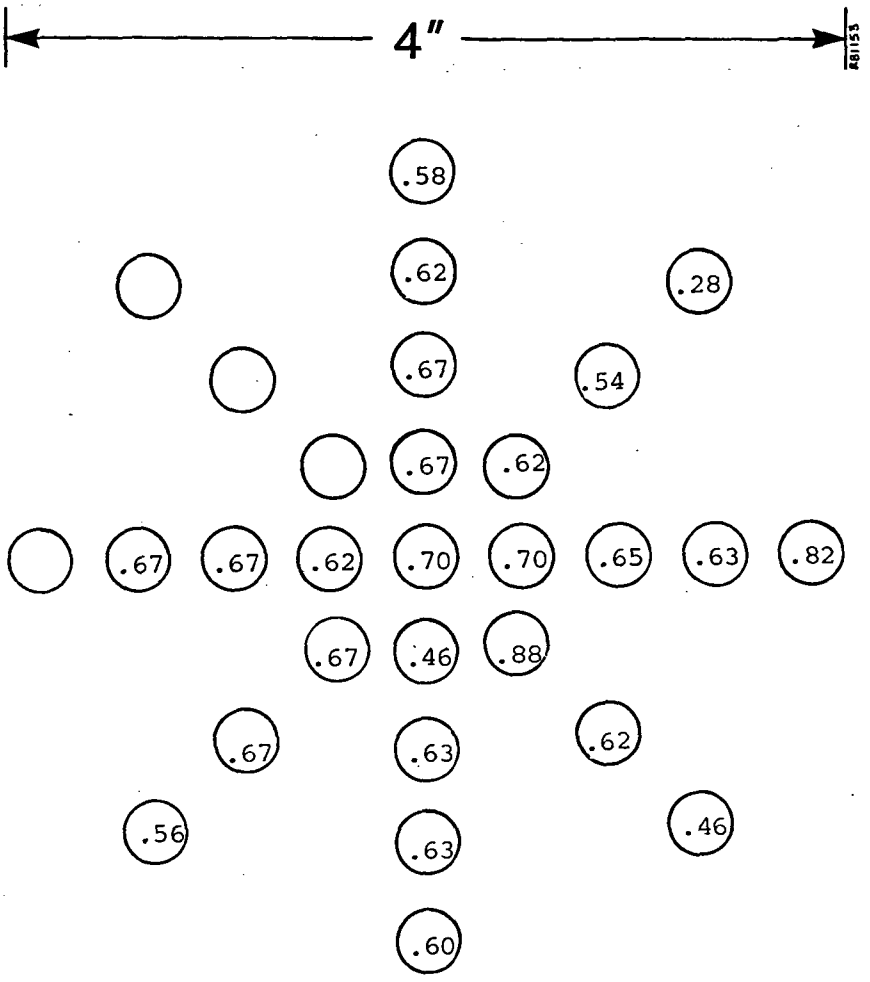
The calorimeter has an electronics package which multiplexes the readout from 25 probes for digitization every 0.5 seconds. The signal from the probes is grounded on one side in three places and filtered to remove RF noise. The digitized signals are analyzed by a microcomputer which extrapolates the temperature profiles to time zero, accounting for average initial readings and the varying delay in the multiplexer. A sample of the corrected data from the computer is shown in Figure 2-11.

2.3.6 Pulse Generator Tests

Tests of the electrical characteristics of the pulse generator were conducted by shorting the electron beam diode through a plate with minimal inductance. Figure 2-12(a) shows a typical signal on the diode current monitor under this condition. This trace can be used to define the equivalent electrical parameters of the pulse generator, using the LRC circuit model shown in Figure 2-12(b). The current follows an equation of the form:

$$I = I_o \exp [- (R/2L)t] \sin [(LC)^{1/2} t]$$

where the exact solution to the circuit model was simplified, since $(L/R)^2 >> LC$. Here L is the total inductance of the pulse generator with the largest contribution from the switch and collector plate. The total capacitance C is that of the energy store plus stray contributions. The total resistance R is believed to be mostly from the arc in the switch.



AVERAGE READING ON ALL POINTS

.64±.09 J/cm²

FIGURE 2-11. CALORIMETER ARRAY AND READOUT.

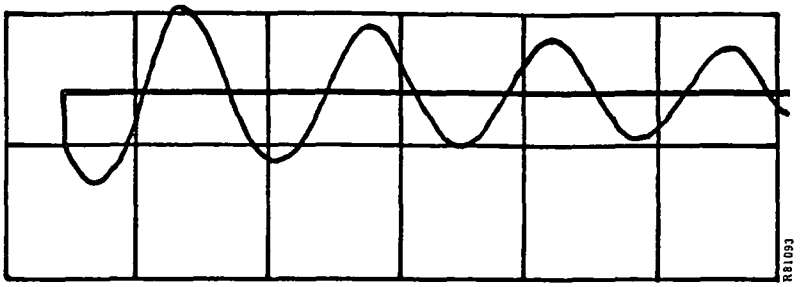
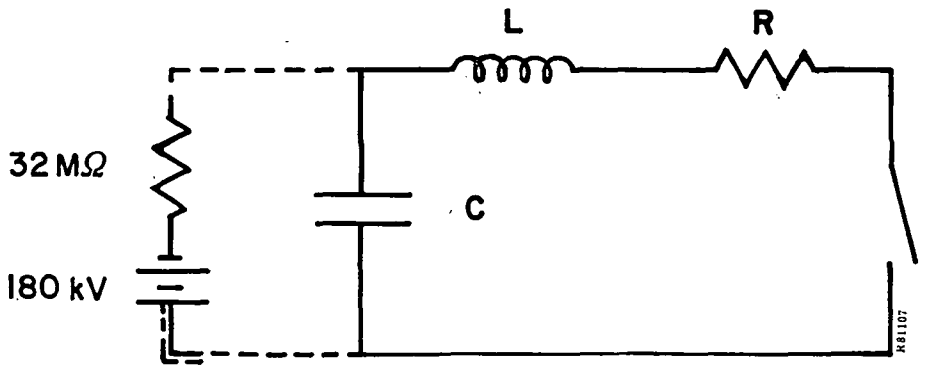


FIGURE 2-12(a). CURRENT SIGNAL FROM PULSE GENERATOR WITH THE DIODE SHORTED; 50 kV CHARGE, 34.5 kA/div, 50 ns/div.



MEASURED	DESIGN
L 86 nH	100 nH
R .14 ohms	—
C 23 nF	24 nF

FIGURE 2-12(b). EQUIVALENT CIRCUIT MODEL FOR PULSE GENERATOR WITH MEASURED PARAMETERS FROM (a).

The parameters R, L and C were determined from Figure 2-12(a), giving the total charge initially in the energy store (corrected for experimental decay) and the value of C = 23nF (±5%). The period of the oscillation is 280 ns (±5%), which is equal to 2 $(LC)^{1/2}$, or L = 86 nF (±10%). The total resistance was determined from measurement of successive peaks on the curve, and R = 0.14 ohms (±10%). These values are close to the design parameters of 24 nF (8 storage lines) and 100 nH.

2.3.7 Electron Beam Diode Tests

The first setup used for diode tests was determined by the original design model (see Section 2.3.1). Diode parameters were then varied in a stepwise approach to the optimum electron beam required for annealing.

The variable parameters are cathode radius, cathode-anode gap, sample-anode gap, applied magnetic field and charging voltage on the energy store. Table 2-1 lists the variations of these parameters during the test of the diode.

TABLE 2-1. PARAMETRIC MATRIX FOR DIODE TESTS

Exp't	Cathode radius (in.)	Cathode-anode gap (in.)	Sample anode gap (in.)	Magnet field (kG)	Charging voltage (kV)
1	6	0.098 0.197	0.092 0.215	0 2.0	25, 50, 100, 125
2	4	0.116	0.188	0, 1.6	25, 50, 100, 125
3	4	0.092, 0.110 0.135	No anode	0, 2.0	140
4	4	0.098	0.212 0.171	0, 0.18, 0.36, 0.72 1.0, 2.0	140, 150 160
5	4.5	0.108	0.171	0.7, 1.0	150, 160 170, 180

An example of the beam voltage and current traces and the electron beam energy spectrum determined from them (corrected for inductive effects) is shown in Figure 2-13. The average energy of the electrons is about 13 keV.

Correct functioning of the diode was verified by measurements of beam perveance. The perveance is defined as $I/V^{3/2}$, and is a geometrically determined quantity for planar, nonrelativistic, space-charge-limited electron beam diodes. For MKS units (amperes, volts, meters) its value is given by:

$$I/V^{2/3} = 2.33 \times 10^{-6} \pi \, r^2/d^2$$

where I and V are the diode current and voltage, respectively, r is the cathode radius, and d is the cathode-anode gap. As shown in Figure 2-14, the perveance is a time-dependent function. This arises from the plasma which forms at the cathode at the start of the pulse and drifts to the anode at nearly constant velocity. In higher power diodes a plasma may also form at the anode and drift in the opposite direction. Thus the value of the cathode-anode gap should be written as:

$$d = d_o - vt$$

where d_o is the initial gap, v is the closure velocity due to plasma drift and t is time. The value of v is approximately 2.5×10^4 m/s, and the theoretical curve is plotted in Figure 2-14 using this value. Agreement between the curves indicates that the diode is operating as expected.

The successful demonstrations of the operation of the electron beam pulse subsystem allowed the commencement of silicon wafer annealing experiments discussed in Section 2.4.

2.4 ANNEALING EXPERIMENTS

As soon as the pulser was capable of forming an electron beam, experiments on annealing ion implantation damage in silicon wafers were initiated. Two general types of experiments were conducted, "qualitative" and "quantitative". The qualitative tests involved literally hundreds of electron beam pulses onto ion implanted silicon wafers for approximate optimization of the accelerator parameters. The change of the shiny

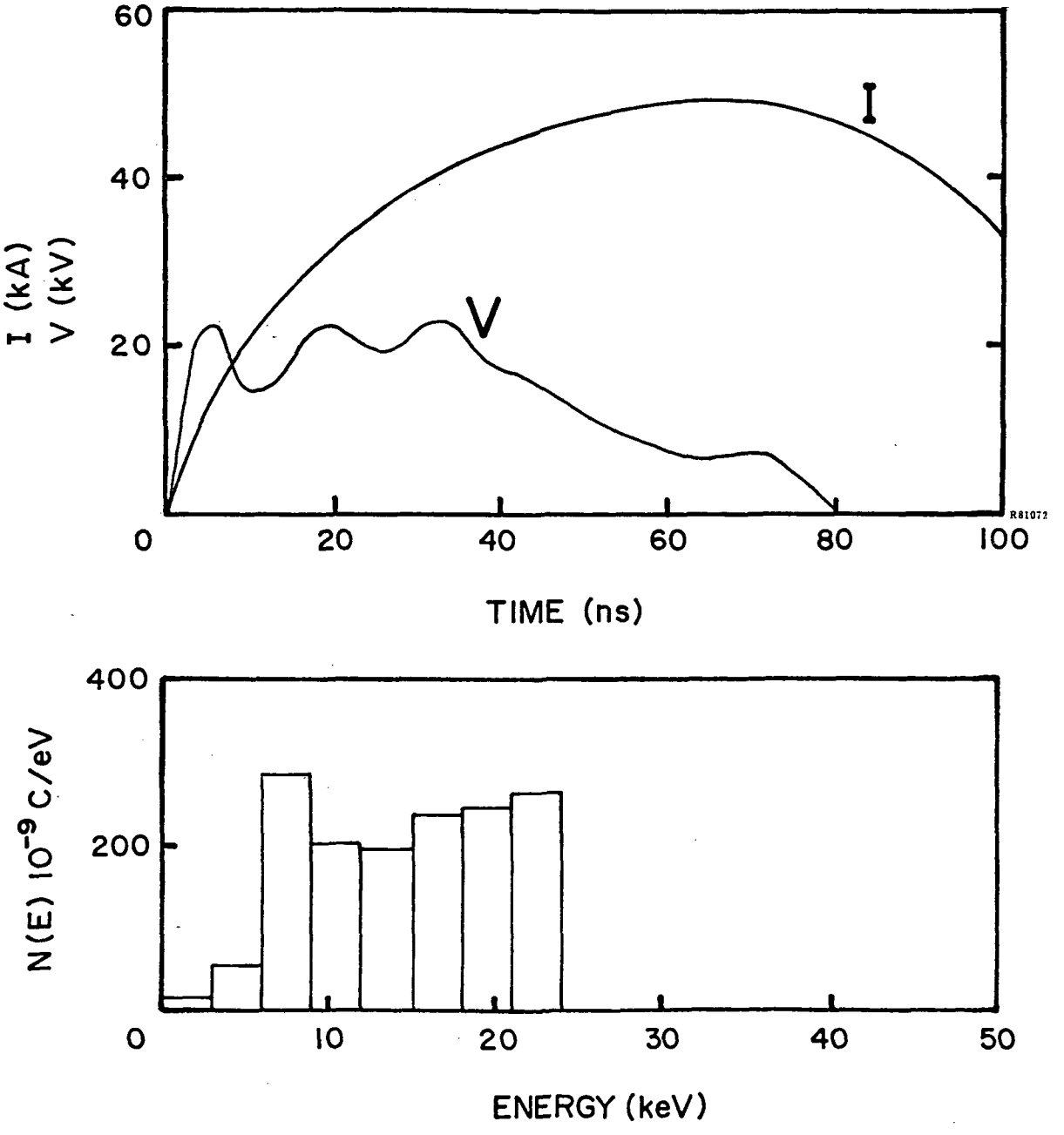


FIGURE 2-13. TYPICAL CORRECTED DIODE VOLTAGE, CURRENT AND ELECTRON ENERGY SPECTRA FROM COMPUTER CODE EBSPEC.

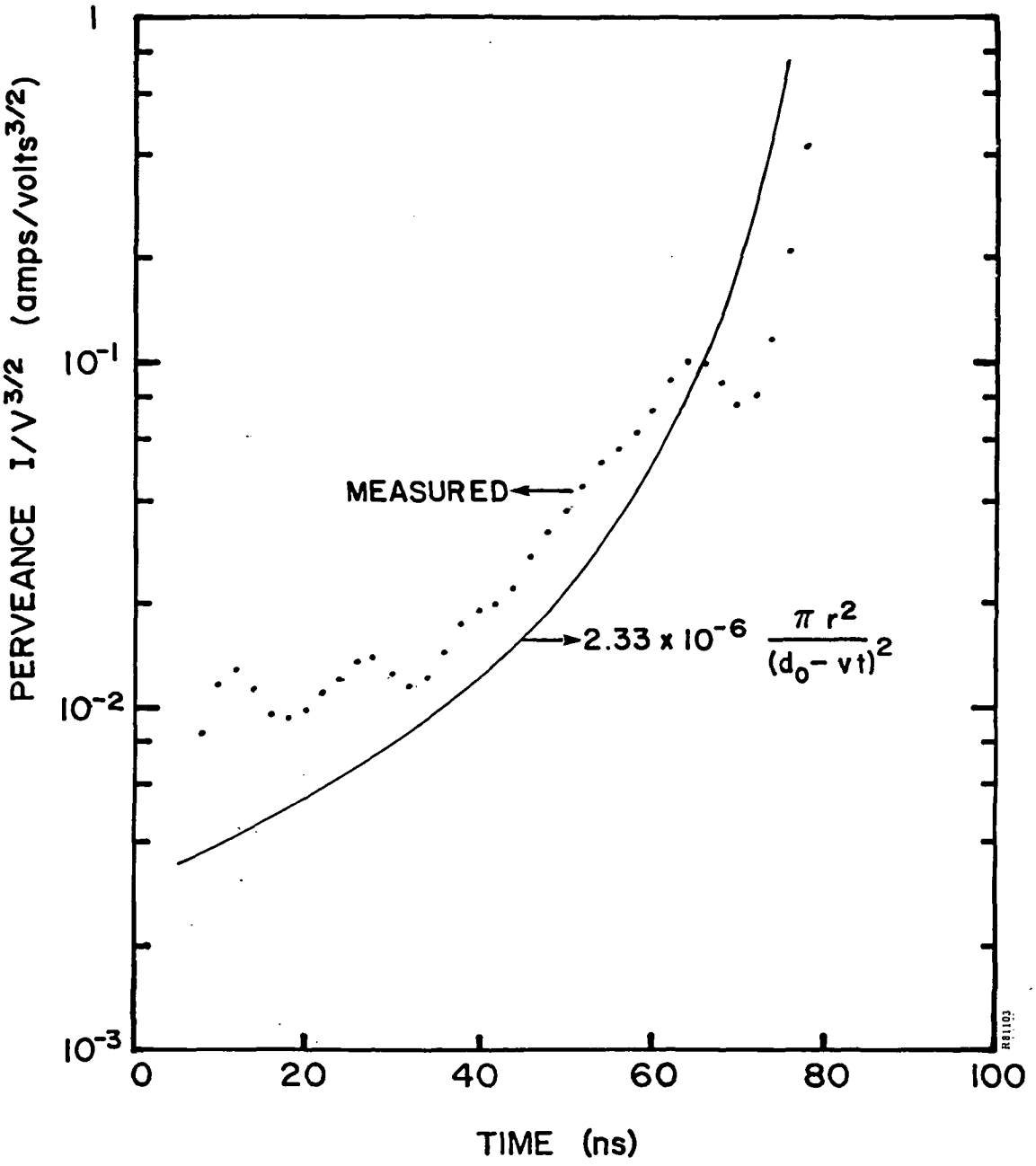


FIGURE 2-14. MEASURED AND MODELED DIODE PERVEANCE FOR PULSE SHOWN IN FIGURE 2-13.

amorphous surface to the characteristic blue-gray color of crystalline silicon gave a good qualitative indication of the size and uniformity of the beam. Visually apparent surface damage on the wafer indicated "hot spots" in the electron current density.

Quantitative tests involved mapping of the surface resistivity of the annealed wafer and, in many cases, the actual formation and characterization of solar cells. The quantitative tests were performed only after the electron beam parameters appeared to be optimized qualitatively. For brevity, only the quantitative tests will be discussed here.

2.4.1 Preliminary Experiments

Samples for the initial annealing tests were 100 mm diameter silicon wafers with a polished surface and as-cut backs, 0.020 inch thick. They were cleaned, implanted with 2.5×10^{15} ions/cm^2 of 10 keV phosphorus, cleaned a second time and delivered to the junction processor test station. Typical wafer resistivity was 10 ohm-cm. Some samples with etched surfaces, 0.013 inch thick and 1 ohm-cm were tested to see the effects of different wafer parameters.

These samples showed small-scale non-uniformities (typical spatial variation approximately 1 mm) which would not show on calorimeter tests. The entire surface of a wafer pulsed at a magnetic field of 1.2 kilogauss was annealed, however, there was some surface damage, believed to be slip in the worst case, in the center of the wafer. At a magnetic field of 2.6 kilogauss, the surface was uniformly spotted with small areas of damage adjacent to small areas (approximately 1 mm o.d.) of unannealed material. The fine scale variations in the beam fluence were caused largely by shaddowing by the wire structure of the anode mesh. There were no apparent differences in the results for the wafers with other surface, thickness or resistivity parameters.

The best annealing results were achieved with a 4.5-inch cathode. The optimum anode-cathode gap was found to be 2.5 mm with a subsequent beam drift distance of 7.8 mm. The most uniform spot was at a charging voltage of 185 kV with an impressed axial magnetic field produced by 9 Amps through the coil, corresponding to a magnetic field of 1.5 kilogauss. It was found that beam uniformity and elimination of anode mesh

shadowing required that the zone beyond the natural pinch of the electron beam be used. The pinching of the electron beam by the beam's self-induced magnetic field dictated the 7.8 mm drift distance between the anode mesh and the silicon wafer.

The beam produced by this technique is sufficiently uniform to require visual examination of wafers to observe deficiencies that may be finer than the multi-point calorimeter is capable of detecting. A large number of wafers were implanted and pulsed to perform the final fine adjustments of geometrical parameters.

The best appearing wafers were made into solar cells at several stages in the electron beam studies. Table 2-2 lists the results of the best cells from wafers processed one month before the improved group shown in Table 2-3. In each case the "best" cells are shown. Although there has been little change in overall efficiency, the cells of Table 2-2 are individually good cells selected from 8 per wafer. There was poor uniformity of performance on each 4-inch wafer. In the later Table 2-3 lot, all of the cells that survived fabrication losses are shown for two wafers, demonstrating that a far more uniform anneal was created. However, some wafer-to-wafer variability remained, even though the performance tends to be uniform for all the cells made from a given wafer.

A test to correlate final cell performance with sheet resistance was performed. A wide range of sheet resistance for visually annealed 4-inch wafers was available. Figures 2-15 and 2-16 show cell performance for two of these wafers together with the location and efficiencies of 2 x 2 cm cells made from the 4-inch wafers. The higher sheet resistance appears to have marginally better performance. Microscopic surface examination of the cells of Figure 2-15 indicated the presence of damage zones not apparent to the eye which are not present on the cells of Figure 2-16. It is thus believed that some improvement in beam uniformity still remains to be accomplished.

2.4.2 Detailed Annealing Experiments

A total of 240 mesa cells were made on four 4-inch diameter silicon wafers to study the uniformity and quality of the pulsed electron beam annealing. Sheet resistance and conversion efficiency were mapped over the 81 cm^2 area of the wafers. Failing

TABLE 2-2. EARLY PEBA CELLS

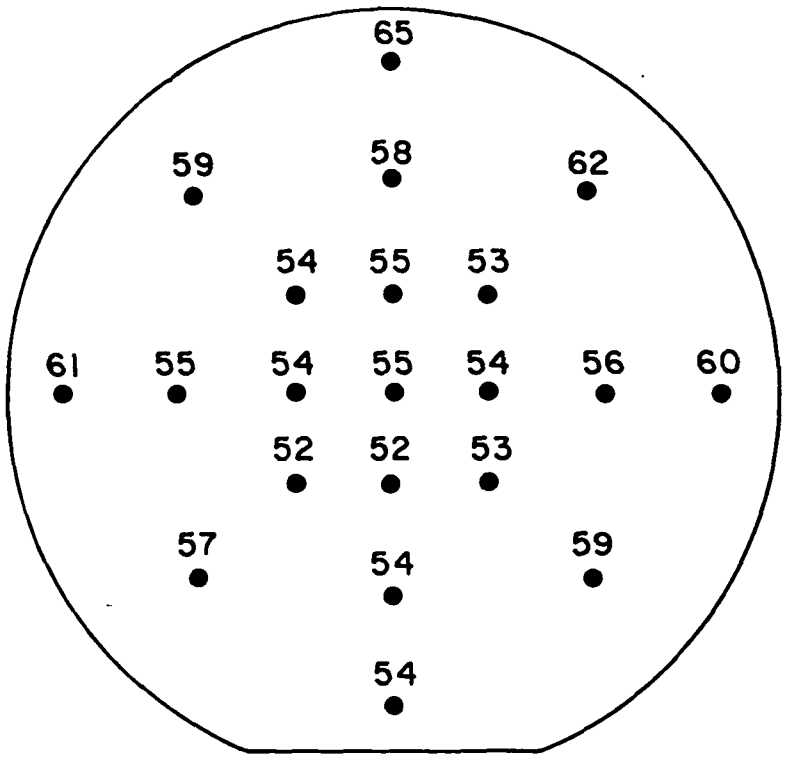
Cell	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF %	Eff (AM0) %
7-1	544	24.2	69.2	6.74
10-1	559	26.1	72	7.78
16-2	553	27.3	70.7	7.88
17-3	558	27.4	70.4	7.96
Control	563	28.1	76.2	8.90

No antireflection coating or back surface field

TABLE 2-3. JUNCTION PROCESSOR/PEBA CELLS

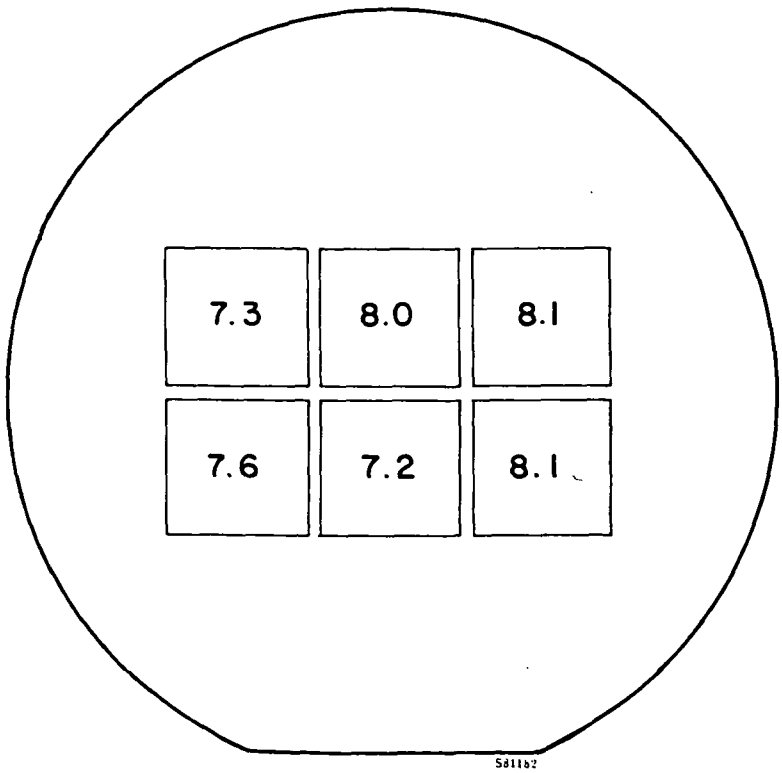
Lot Number:	4031	Resistivity:	10.0 ohm-cm
Surface:	Pol	AR Coating:	None
Comment:	PEBA	Material:	CZ
Cell Area:	4.0 cm^2	Thickness:	18 mils
Illumination:	AM0	Temperature:	25°C

Cell	V_{oc} (V)	J_{sc} (mA/cm^2)	FF %	Eff (AM0) %
71	0.540	29.4	71.9	8.45
72	0.540	29.3	69.8	8.15
73	0.535	29.0	71.6	8.20
74	0.540	29.1	68.9	8.01
75	0.540	29.1	69.3	8.05
76	0.543	29.1	72.8	8.50
91	0.545	28.5	71.9	8.25
94	0.553	28.2	73.8	8.50
Ave.	0.552	29.1	71.3	8.26
Sdv.	0.005	0.3	1.7	0.20



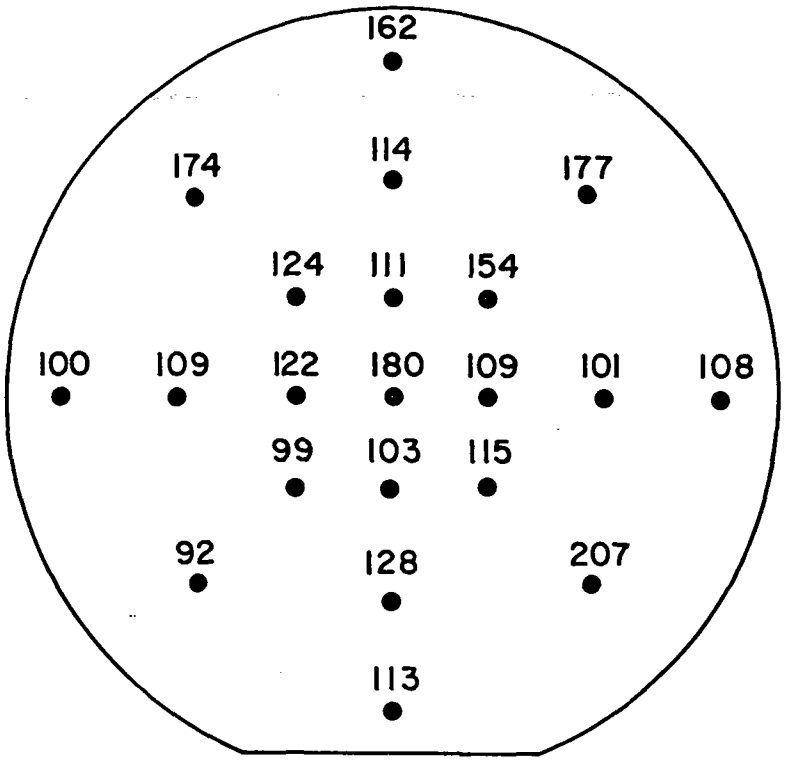
SHEET RESISTANCE
(Ω/□)

WAFER No. 10



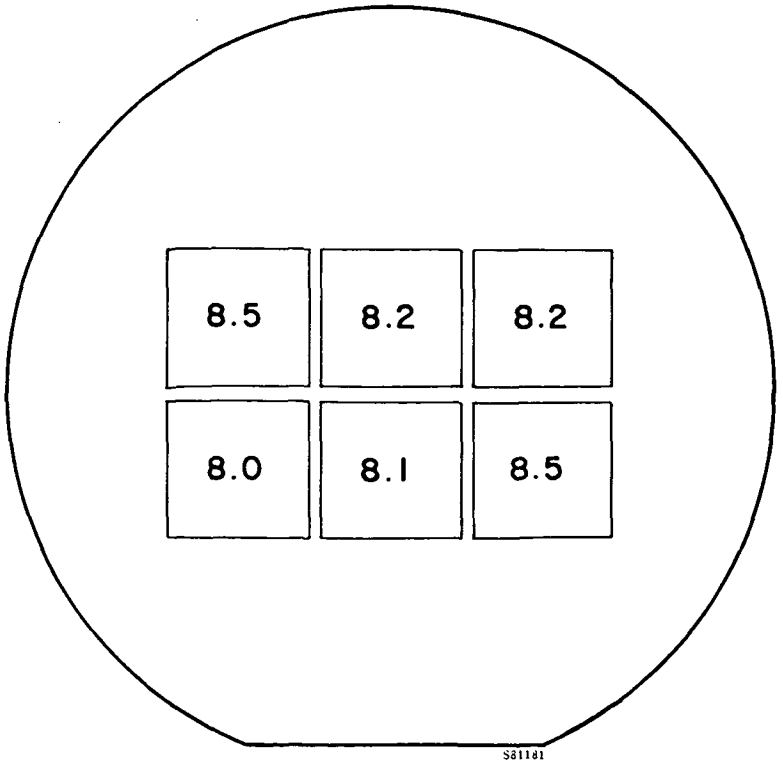
AMO EFF. (%)

FIGURE 2-15. CELL EFFICIENCY VERSUS SHEET RESISTANCE - LOW VALUES.



SHEET RESISTANCE
(Ω/□)

WAFER No. 7



AMO EFF. (%)

FIGURE 2-16. CELL EFFICIENCY VERSUS SHEET RESISTANCE - HIGH VALUES.

metallization reduced the FF on some of the cells, thus lowering the average efficiency on each wafer. The results of this study are given in Appendix 1, which is a copy of Spire's Report DP-10073-01 (October 1982). We achieved an average AM0 efficiency of 7.56% for 60 mesas formed on a 4-inch wafer. No AR coating or BSF was used. If an AR coating were applied, the efficiency would be increased by about 40%, yielding AM0 efficiency of 10.6%. Our experience indicates that the AM1 efficiency would be 18% higher, or about 12.5%.

In summary, the results of the characterization of ion implanted pulsed electron beam annealed solar cells indicate that the efficiency attainable with this technology is approximately 10.6% (AM0) and 12.5% (AM1) over a 4-inch wafer. The uniformity is satisfactory, yielding cells with a standard deviation of 5% over the surface. The metallization and the absence of a BSF on the cells appears to limit the efficiency.

SECTION 3
TASK 2 - WAFER TRANSPORT SYSTEM DEVELOPMENT

3.1 GENERAL

In principle, the completed wafer transport system would be required to transfer 4-inch diameter silicon wafers in and out of the vacuum chambers where ion implantation and pulsed electron beam annealing takes place. The system would include wafer loading and unloading stations, vacuum locks between regions of different pressure, a transport mechanism to carry the wafers between process steps, and wafer-handling devices at both the ion implantation and pulsed annealing stations of the junction processor. The entire system should be operated by an automatic control system with built-in operational monitors and safety interlocks. The wafer transport control system should communicate with the controllers and operational monitors of the ion implanter and pulsed annealer.

Because the program was not taken to completion, and the ion implanter and pulsed annealer were not integrated into a complete junction processor system, a full wafer transport subsystem was not designed and built. However, an interim wafer transport and handling system was designed, built and demonstrated for the SPI-PULSE 7000 pulsed electron beam annealer. This interim transport mechanism could be expanded to include the ion implanter to form a fully operational junction processing system. The following sections of this report describe the interim wafer handling system.

3.2 INTERIM WAFER HANDLING SYSTEM

3.2.1 Design

The interim wafer handling system was initially designed to allow a single wafer to pass a vacuum lock into the diode region of the process chamber and then out through an exit lock. The design and fabrication to Spire's specifications was undertaken by Brooks Associates, Inc., North Billerica, Massachusetts. Each 6-inch entrance and exit lock was designed to accommodate a wafer platen, if required, with dimensions of 5 inches square by 0.150 inch thick. A lock consists of two pass-through port valves, vestibule, transfer track and drive, pump port and vent valves, position sensor and porch track section.

Later, Spire designed cassette elevators and wafer input and output mechanisms to provide automated pulsed annealing of sample lots up to 50 wafers without removing the cassettes. A diagram of the wafer handling system is shown in Figure 3-1. Not shown is the mechanism to lift the wafer (and its carrier platen) to the position for annealing by the beam of the electron accelerator. This lifter physically removes the wafer from the transport track and then replaces it on the track after annealing.

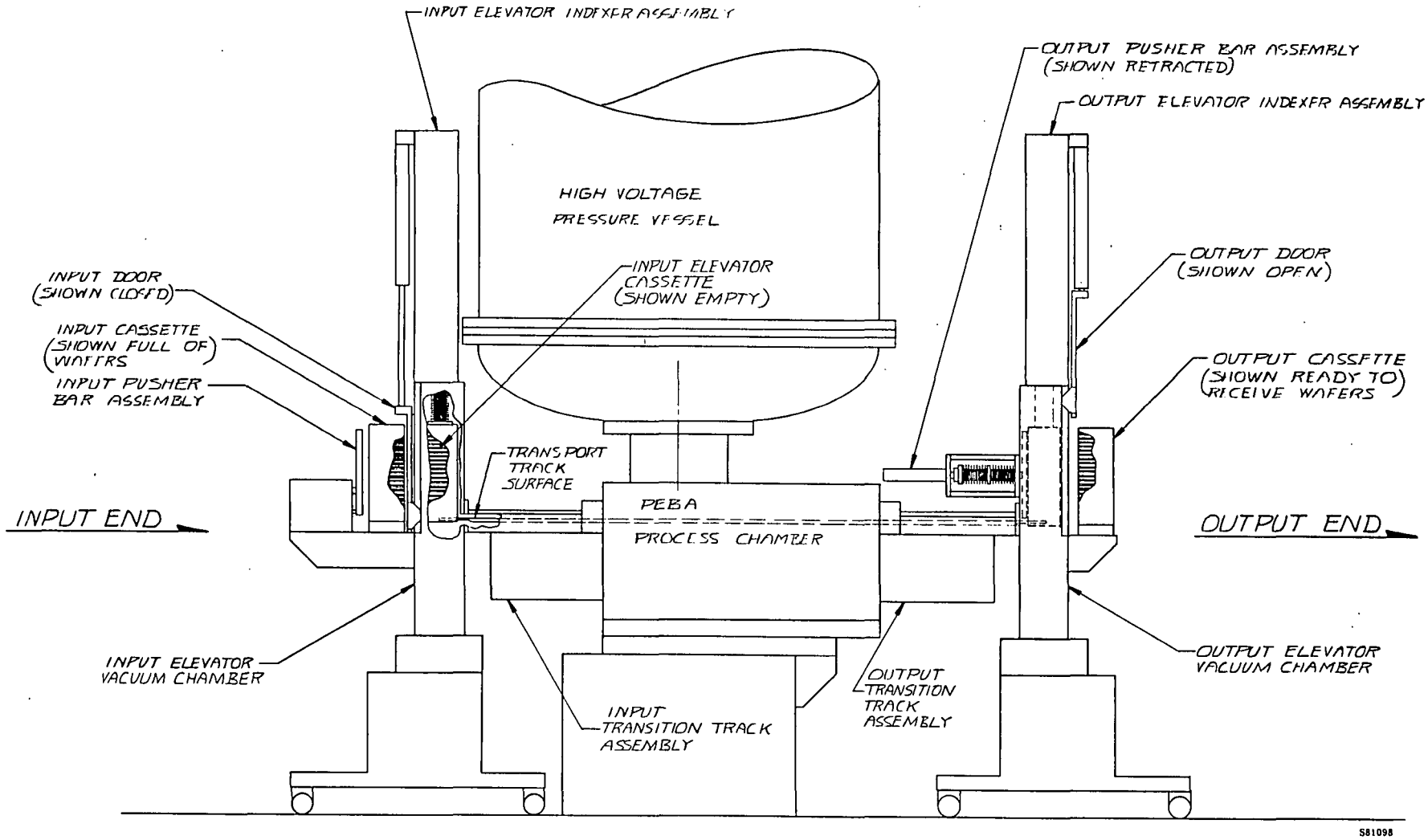
The wafer transport designed by Brooks Associates, Inc., consists of two (or more) vacuum locks and an Orbitrac™ walking-beam transport mechanism. Comprised of three rails that describe oscillatory motion, the walking beam transport moves wafers by an alternating movement of the center and side rails. The motion describes a series of arcs which carry the wafer forward along the walking beam. This system is shown schematically in Figure 3-2. The transport track was designed with two output branches by way of a "Y" switching device. This feature was included to provide the eventual capability of increasing the throughput of the junction processor. The "Y" switching design would allow unloading a filled cassette from the machine while a second, active cassette was being filled from the other output branch.

3.2.2 Fabrication

The Orbitrac™ transport and vacuum locks were fabricated by Brooks Associates, Inc., and the cassette elevators, loading and unloading stages, and the wafer lifter were built by Spire. A photograph of the "Y" track section is in Figure 3-3 which also shows portions of the output vacuum lock and the track drive assembly. Photographs of the completed pulsed annealer and parts of the interim wafer handling system are shown in Figures 2-8 and 2-9.

3.2.3 Operation

The interim wafer handling and transport system was assembled, tested and demonstrated to operate at a rate of one wafer every 2 seconds. Some problems were observed with the mechanical components of the input and output loading and unloading mechanisms which could be corrected by redesigns of a few parts.



ELEVATOR/CHAMBER INTEGRATION

FIGURE 3-1. PULSED ELECTRON BEAM ANNEALER (PEBA) AND INTERIM WAFER HANDLING SYSTEM.

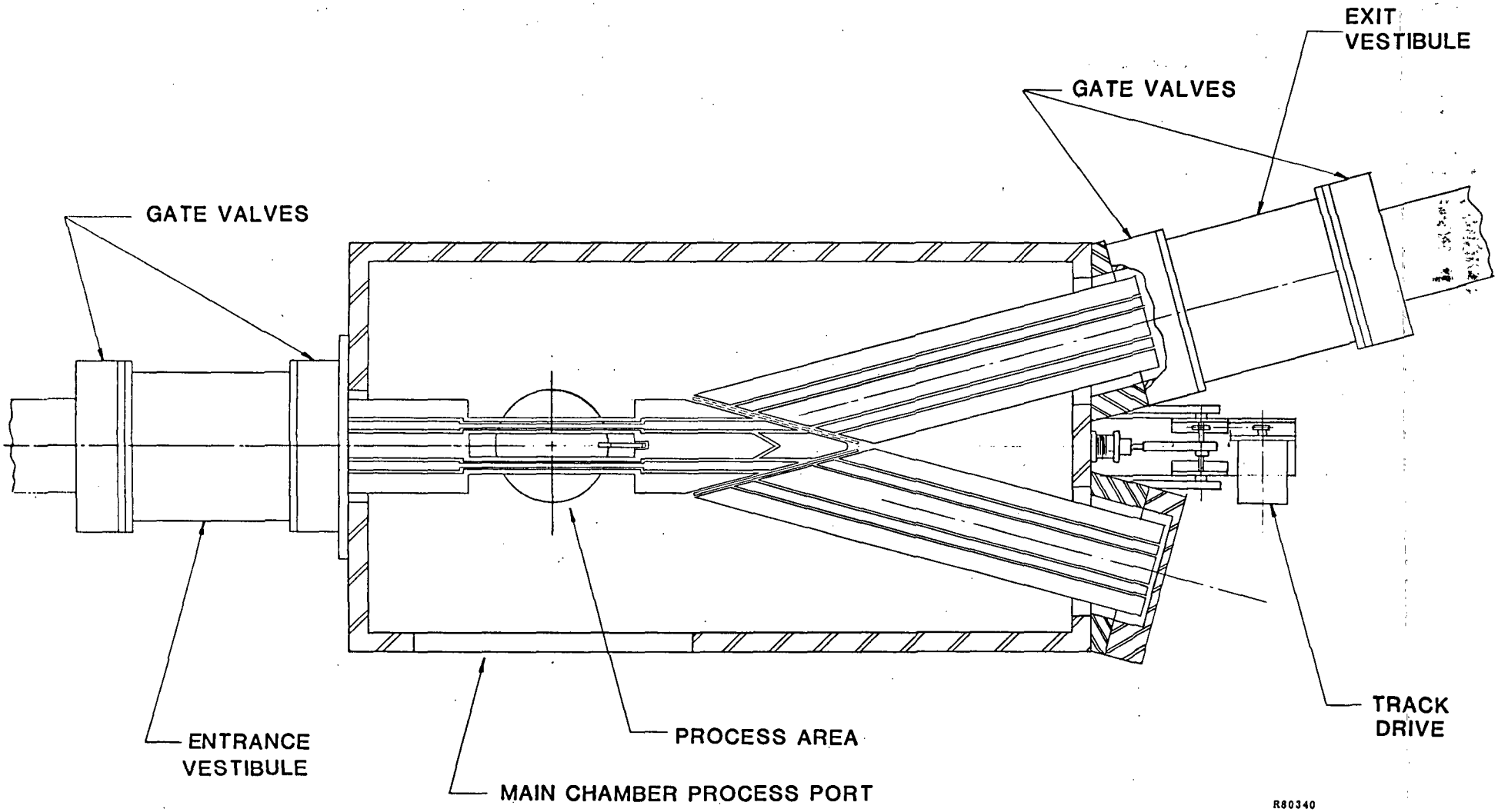


FIGURE 3-2. PLAN VIEW OF PROCESS CHAMBER AND INTERIM TRANSPORT SYSTEM.

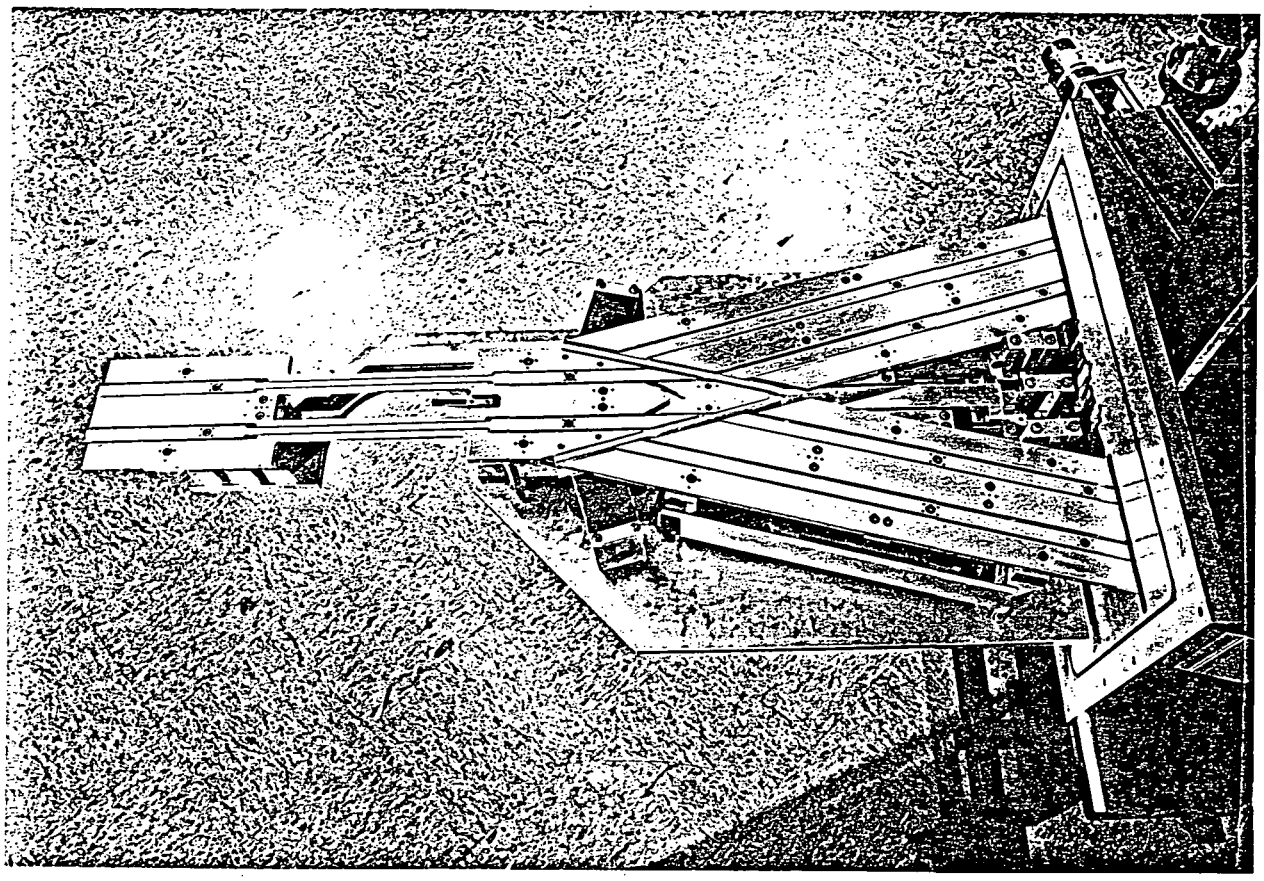


FIGURE 3-3. INTERIM WAFER TRANSPORT "Y" TRACK SECTION.

The major problem encountered with the present method of advancing the cassettes in the locks is caused by the lack of long term stopping reproducibility of the hydraulic switches that sense cassette position. Small variations in the reaction time of these switches alter the location of the slot relative to the walking beam track and produce loading and unloading malfunctions.

It is suggested that a positioner based on a single turn of a lead screw be used instead of the existing mechanism. Conventional optical edge detectors or a cam would be used to sense the end of the turn and a commercial stepping motor could supply the drive power.

The automatic process control system was demonstrated to operate reliably over long periods of time without intervention by the machine operator.

Appendix 2 is an instruction manual for the pulsed electron beam annealer and interim wafer handling system and contains complete information on the detailed operation of these subsystems.

SECTION 4
TASK 3 - ION IMPLANTER DEVELOPMENT

4.1 GENERAL

The original plan of the program was to modify an existing JPL-supplied Model 200-1000 ion implanter built by Varian/Extrion for the junction processor system. It was later agreed that this approach would have required too extensive and costly modifications to be practical. Some of the considerations which led to changing the original plan were that the wafer transport system would have been very difficult to install into the Varian/Extrion ion implanter configuration, major rebuilding would be required to increase the ion beam current, and a much larger electromagnet structure would have been required for mass analysis of the physically larger, higher current ion beam.

For these and other technical reasons it was mutually agreed that a new ion implanter should be designed for the junction processor system. This ion implanter should be easily integrated with the wafer handling and transport system used with the pulsed annealer and, if possible, be less complicated and costly than conventional general-purpose ion implanter systems.

The approach adopted was to design and build a non-mass-analyzed (NMA) ion implanter in which all charged species formed in the ion source are accelerated and implanted into the silicon wafer. This requires the ionization of pure dopant material (phosphorous) in the ion source, but substantially reduces the geometrical, mechanical and electrical complexity of the implanter subsystem by eliminating the mass analyzing electromagnet and reducing the length of the beam line. Before embarking on the design of the NMA ion implanter, a testing facility was set up in the laboratory and experiments were conducted to explore ion beam dynamics and to assure that the solar cell junctions formed with the multi-species ion beam were equivalent to those formed with a mass-analyzed beam.

4.2 DESIGN CONCEPT

The design concept for the NMA ion implanter is shown in Figure 4-1, together with the walking beam wafer transport mechanism. The ion beam is extracted from a high-current ion source which is mounted in its own pumping system above the wafer transport.

The downstream zone above the wafer and track contains an electrostatic beam expander and steering structure and a Faraday cup arrangement for measuring the beam current. Monitors below the track are used for sampling the beam during wafer processing. Beam centering is performed by a combination of steering potential and geometry. Information feedback on centering is available from below-track monitors and visually through appropriately placed ports on the vacuum chamber. The latter is possible because residual gas in the chamber glows with a characteristic wavelength when the ion beam impacts the atoms.

The ion source shown in Figure 4-1 is a modified Freeman type. The principal modifications from a standard commercial design are to increase the ion current output capabilities and to extend the lifetime of the solid charges in the ion source boiler. Figure 4-2 is a design layout of a modified Freeman ion source for the NMA ion implanter.

4.3 NMA ION IMPLANTER TEST FACILITY

4.3.1 Beam Steering and Defocusing Tests

It is very difficult to predict numerically certain aspects of the beam transport at the high currents intended for the NMA implants. Of special importance is the degree of defocusing provided by the space charge expansion in the beam bender. This will vary with the electric field used, beam current, beam shape, and geometry, but this dependence cannot be reliably predicted on the basis of theory. Therefore, it was decided to assemble a test setup based on commercial hardware that could serve to perform beam studies as well as implant some wafers to a rough degree of uniformity. Figure 4-3 shows a diagram of the facility.

The ion source was a commercial unit built by Varian/Extrion. The extraction geometry was modified to permit operation with a well-focused beam at 10 keV as well as other energies.

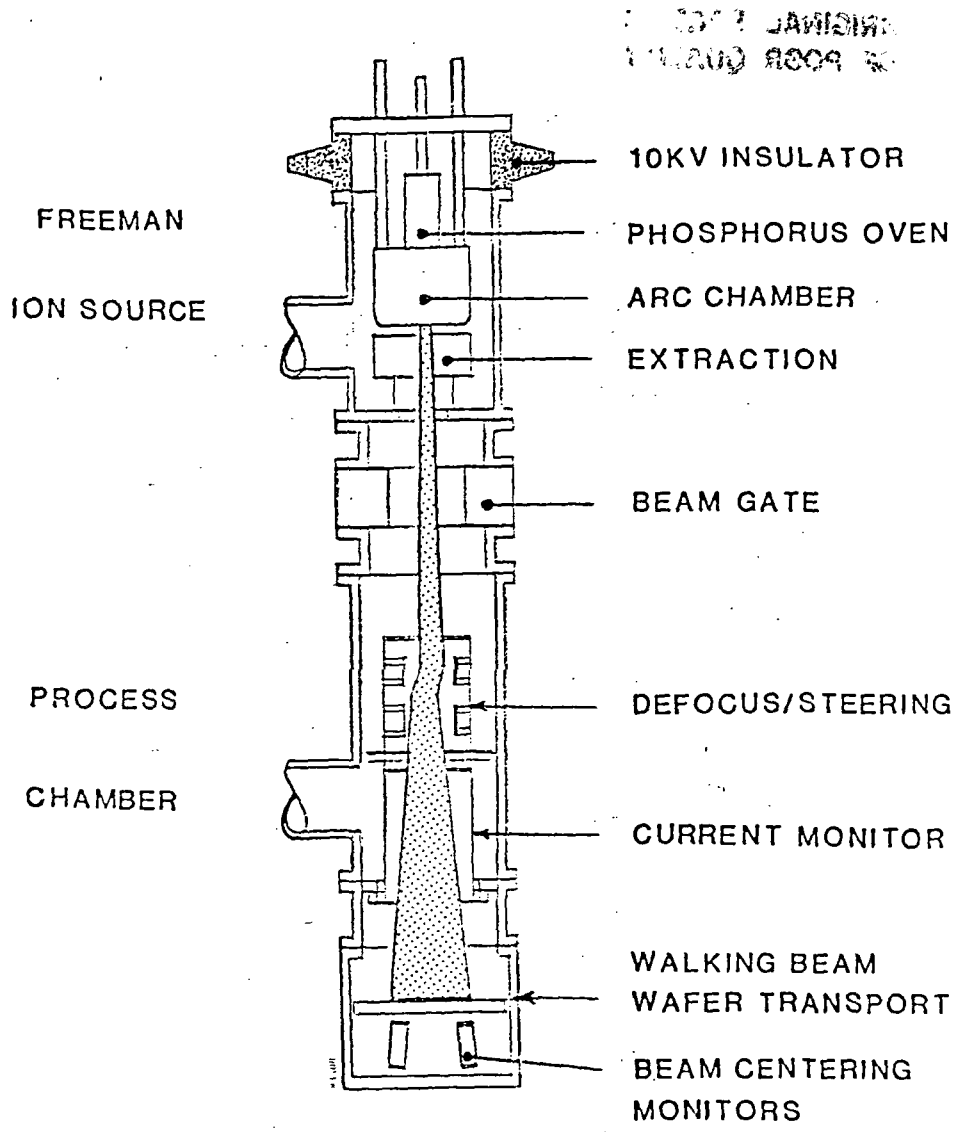


FIGURE 4-1. CONCEPTUAL DESIGN OF NON-MASS-ANALYZED ION IMPLANTER.

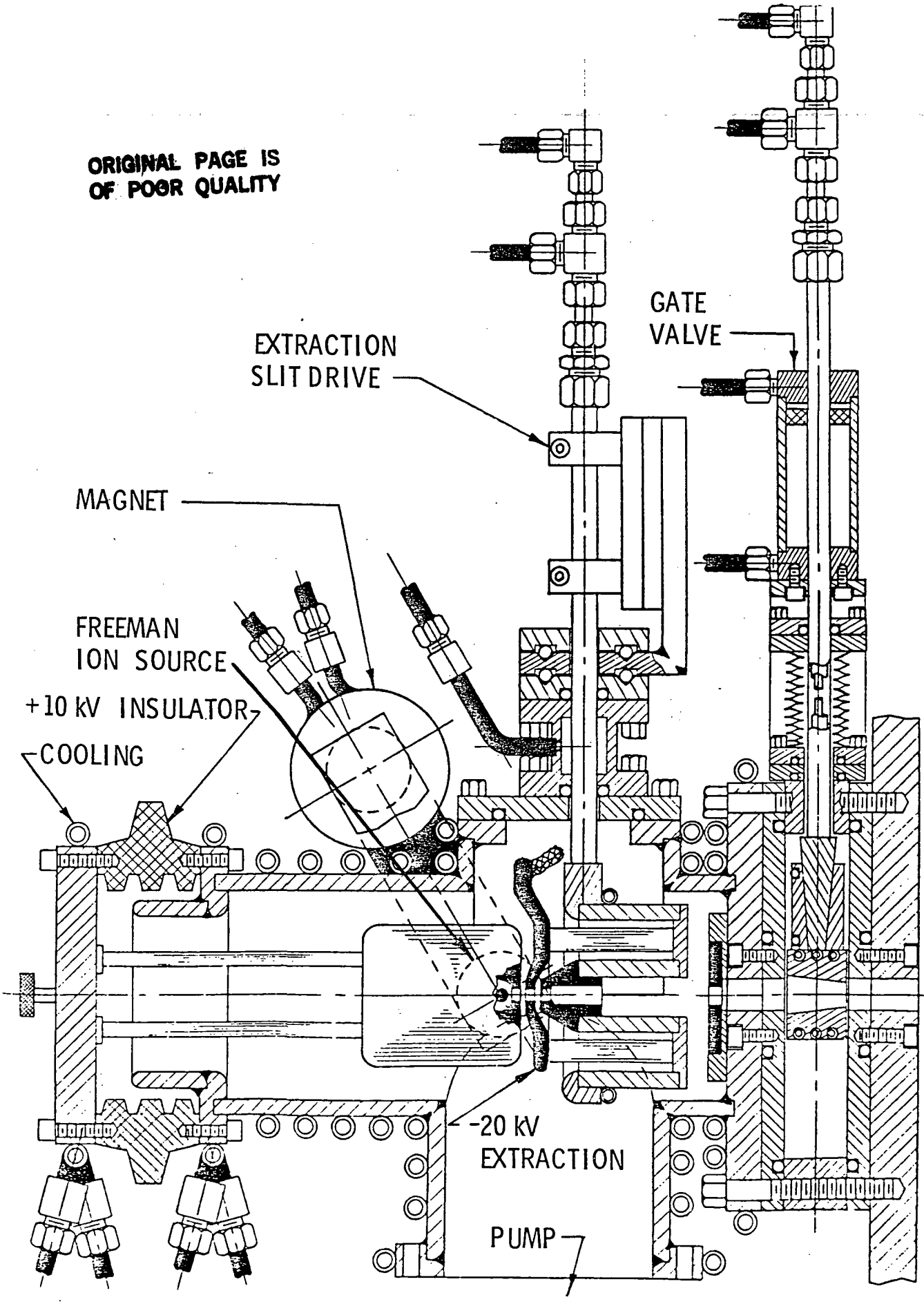


FIGURE 4-2. DESIGN LAYOUT OF NMA ION SOURCE.

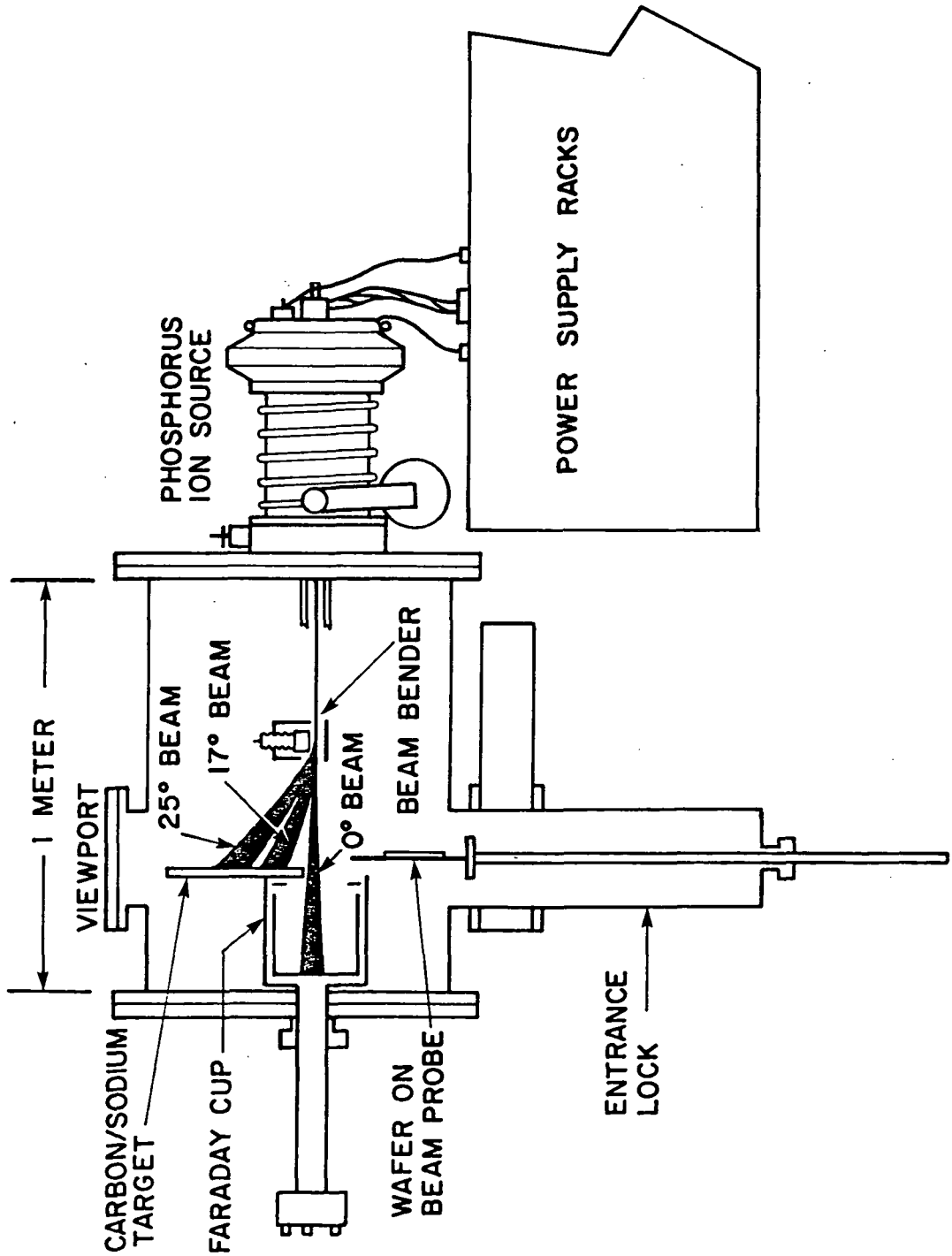


FIGURE 4-3. NMA ION IMPLANTER TEST CHAMBER.

The beam steering test device was of a form shown in Figure 4-4. The plate separation of the test fixture was 1.5 inches in this design. Although experiments have been performed on other shaped electrodes, simple parallel plates produced the best beam steering results. Voltages up to -12 kV were used successfully in this test.

The Faraday cup shown in Figure 4-3 was a large area unit with electron suppression. The carbon target mounted on the cup was used to display the beam spot produced by the bend. The target was scored with a ruled pattern to permit measurements of the spot dimensions. Additionally, the target was impregnated with sodium to produce a distinct orange glow in zones where the beam struck.

The beam probe served two purposes. It could be used as an occulting mask to measure the dimensions of the unbent beam and also served as the wafer carrier during the NMA implant, since it could conveniently be removed through an entrance lock without venting the system. The probe could be rotated on axis to avoid normal incidence implants, if desired. However, for the 17° and 25° bend beams, implantation far from normal incidence was inevitable. Because of the fan in beam angles, a wide range of implant angles per wafer was produced.

Several tests to analyze the beam from the ion source were completed. A phosphorus beam was analyzed using a commercial ion implanter as a mass spectrometer. Figure 4-5 shows a log plot of the major species created. The main contaminant was oxygen since some of the phosphorus has a surface oxide growth. There are several species of phosphorus, since the normal gaseous form at moderate temperatures is P_4. The heat of the ion source breaks up the P_4 molecule into lower forms, as can be seen in the figure.

The beam bender was tested to determine the degree to which simple theory failed to account for space charge polarization effects. Figure 4-6 shows that significant deviation begins to occur when the bender voltage is 50 percent of the ion beam voltage. These data correspond to the highest current, 6 milliamperes, available with the unmodified commercial ion source.

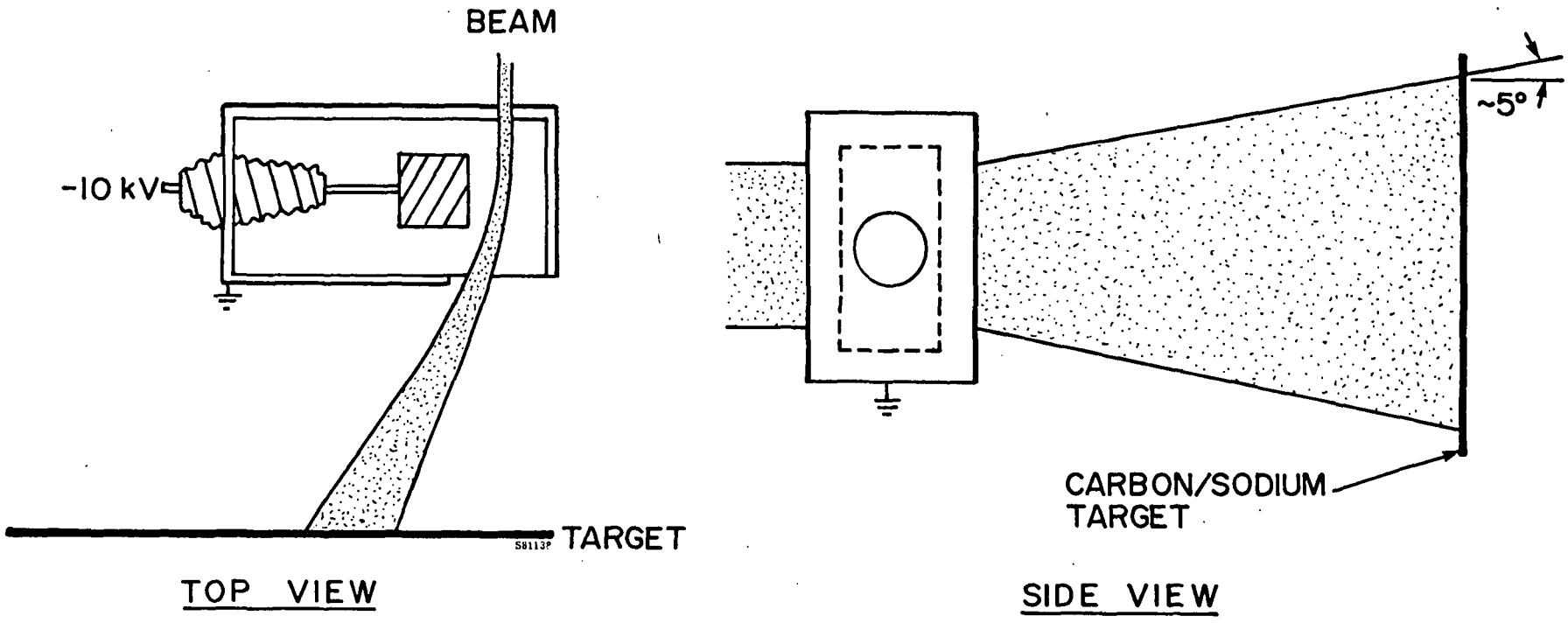


FIGURE 4-4. TEST MODEL BEAM STEERING DEVICE.

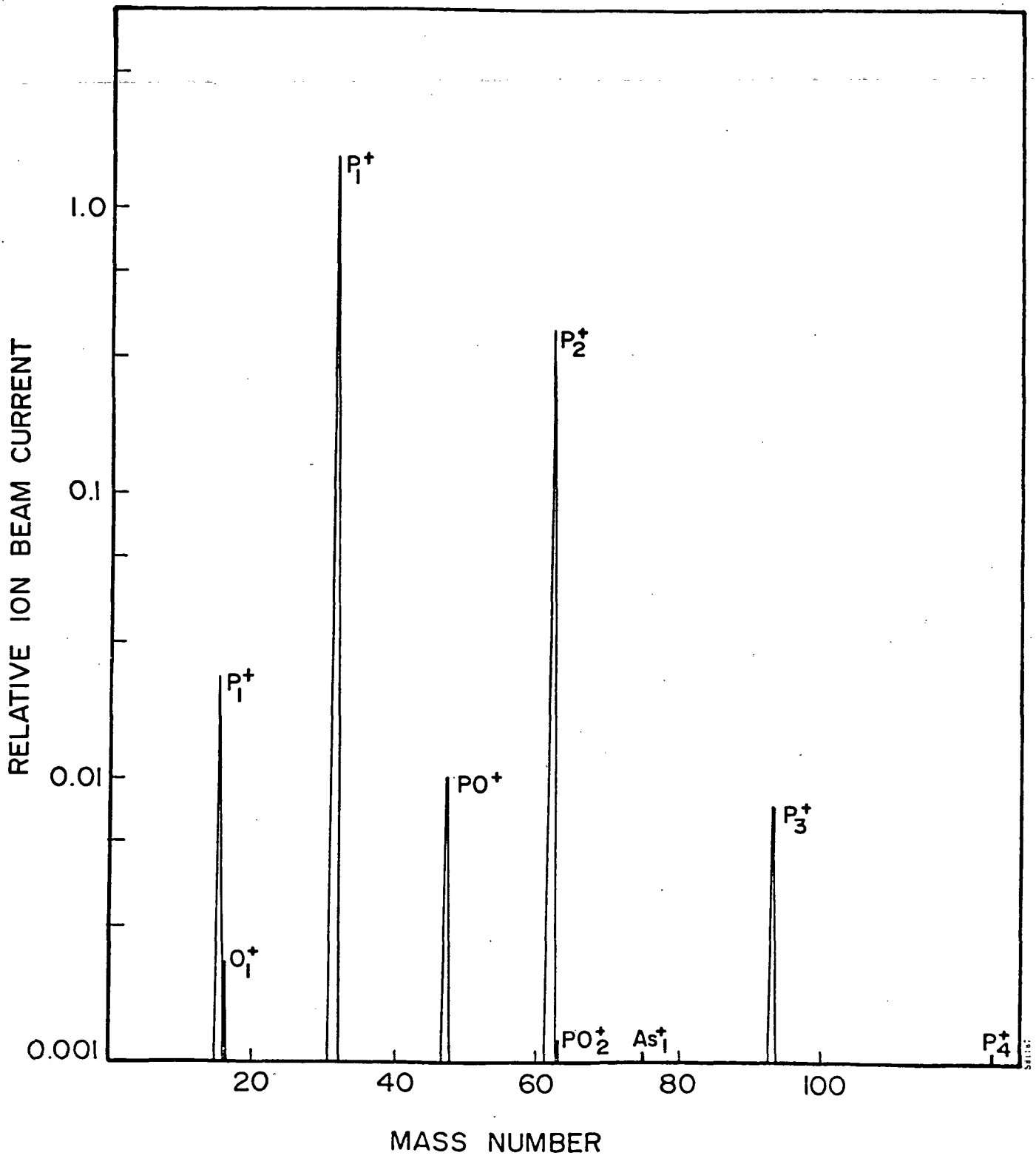


FIGURE 4-5. IONS PRODUCED BY COMMERCIAL GRADE SOLID PHOSPHORUS.

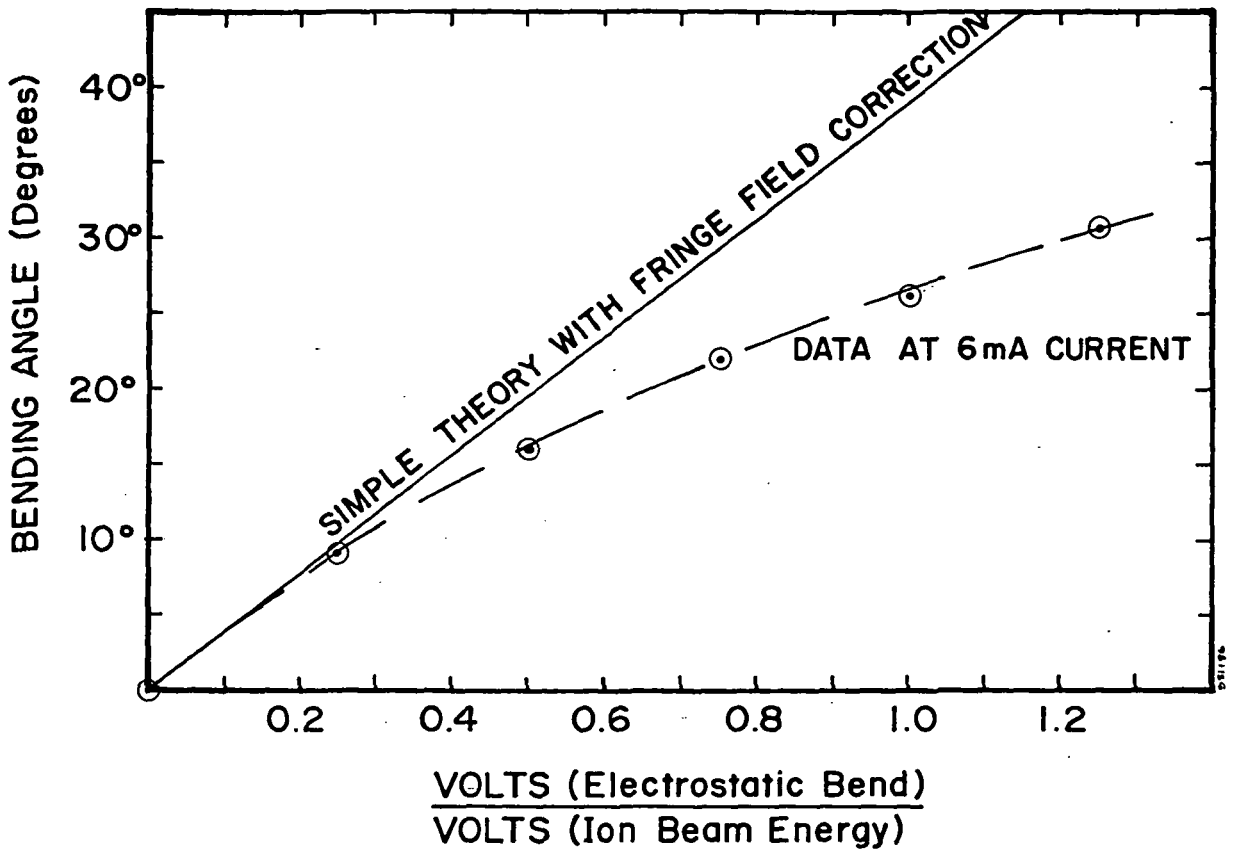


FIGURE 4-6. ELECTROSTATIC BEAM BENDING AT HIGH CURRENT.

Figure 4-7 shows the horizontal (narrow beam axis) defocusing as a function of ion current. An initial rapid rise in divergence was observed as all of the neutralizing electrons were swept clear and the current was increased to the level where space charge became important. A second, relatively shallow slope then appeared at higher current.

A second approach to the beam steering design was investigated and eventually adopted for the NMA ion implanter. Instead of a single transverse electric field region, two zones with fields in opposite directions were adopted for beam bending and defocusing, as shown schematically in Figure 4-8.

The configuration shown in Figure 4-8 results in an "offset" beam in that it is first deflected right and then symmetrically left to cancel out the bend. Large volumes without space charge neutralization can be created with this configuration, and beam steering can be readily introduced to cancel the offset that is created. In addition, beam spot irregularities can be corrected to some extent by modifying the defocus plate geometry. Unlike the initial beam deflector design which required voltages up to -12 kV, this large volume offset deflector needs only about -1 kV to operate with a 10 keV beam energy.

A preliminary measurement of the beam uniformity was made with the new deflector. These data were not taken with the final high-current ion source configuration and were intended only to demonstrate the value of defocusing by this offset method. Figure 4-9 shows the data expressed in terms of the beam divergence angle. The data are plotted as the deviation from the mean ion current as seen through a 19 mm diameter occulting mask. The non-defocused beam has a much smaller divergence angle and typically exhibits a two- or three-peaked structure. The defocused beam spreads over a wide angular range consistent with the larger beam spot and the variations are far less pronounced.

4.3.2 Tests of High-Current Modifications for Ion Source

The design goal was to provide up to 10 milliamperes of phosphorus atoms into a rectangular spot. There exists a 20% difference between the atom current of phosphorus and the ion current because of species such as P_2^+. Thus, in principle, only

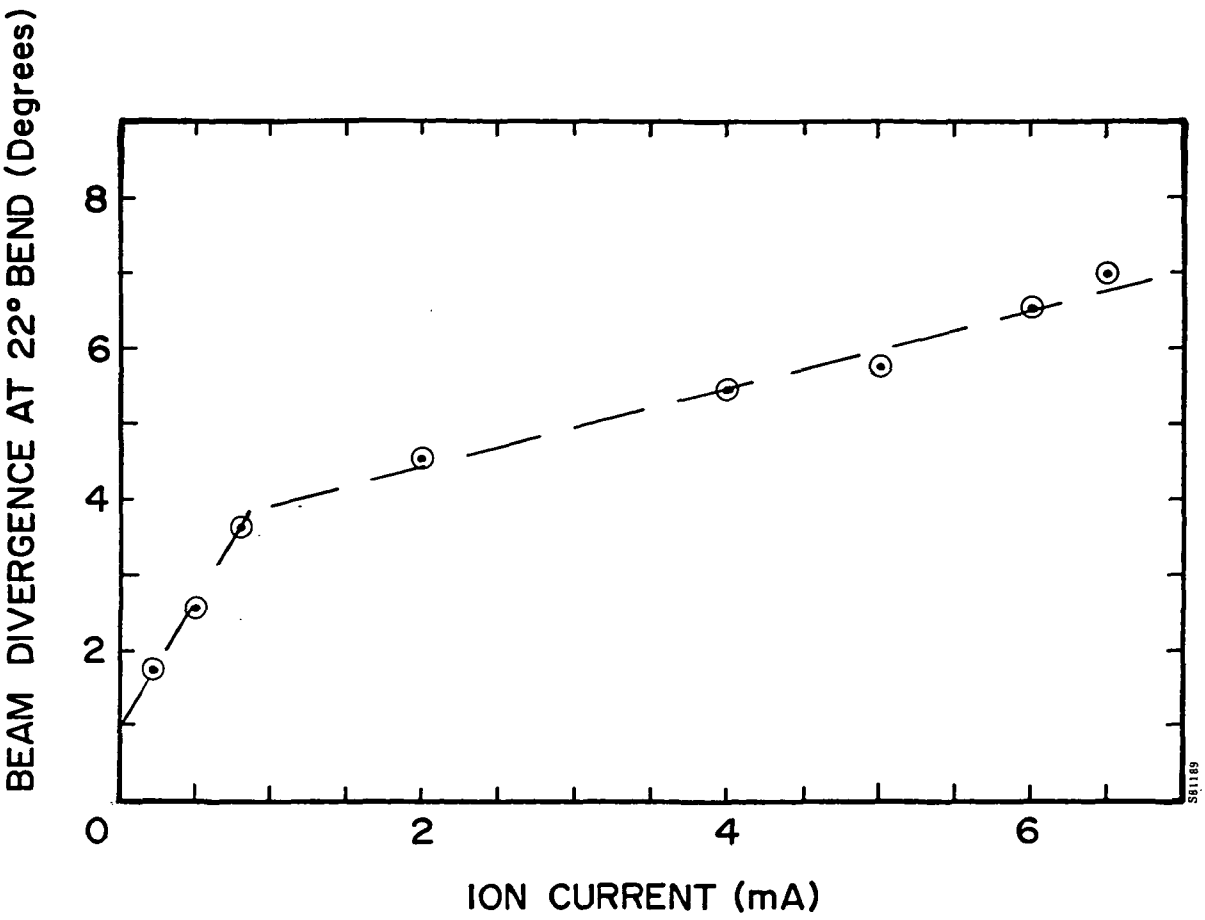


FIGURE 4-7. ION IMPLANTER BEAM SPREAD AFTER BEND/DEFOCUS.

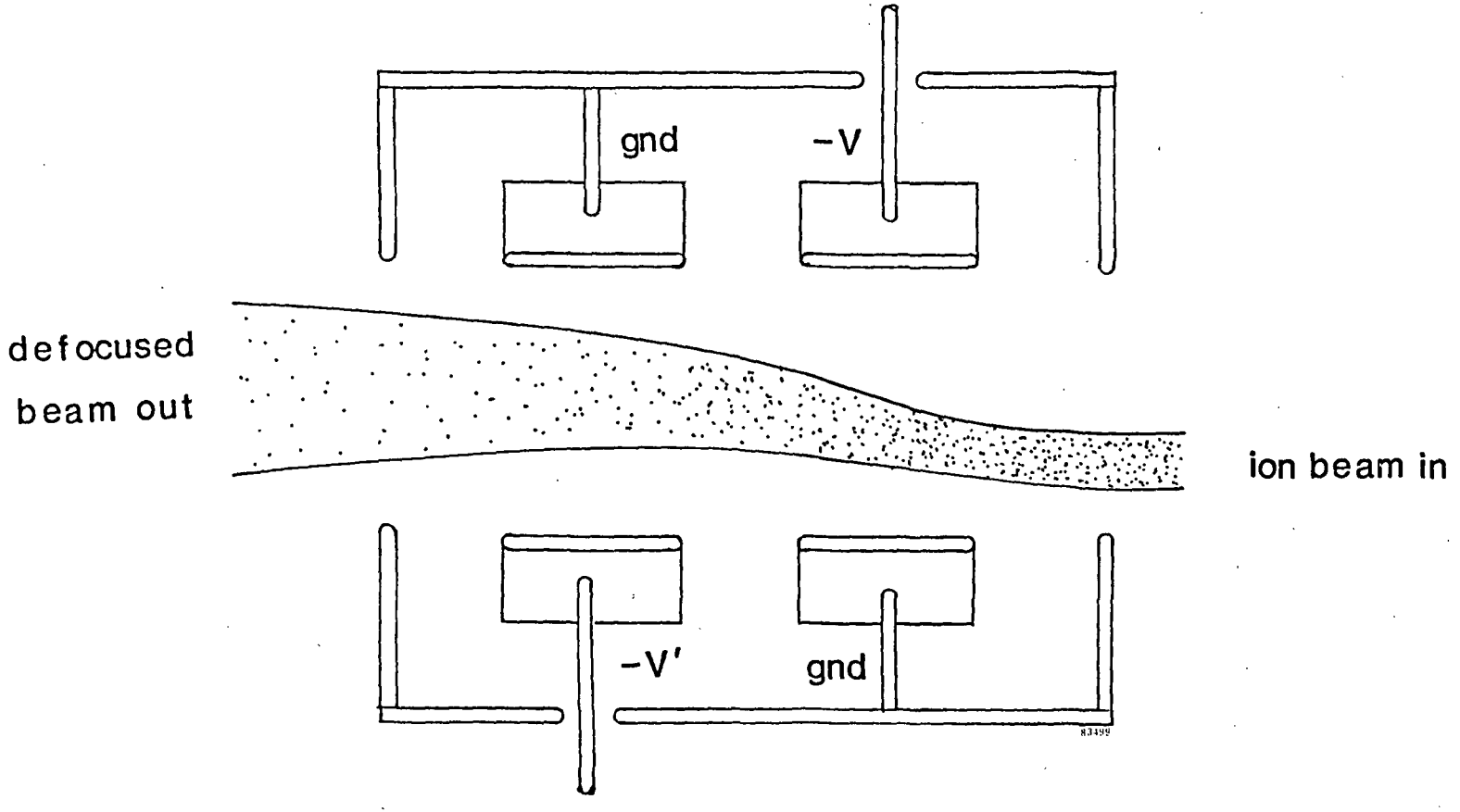


FIGURE 4-8. DESIGN ADOPTED FOR ELECTROSTATIC BEAM BENDING AND DEFOCUSING.

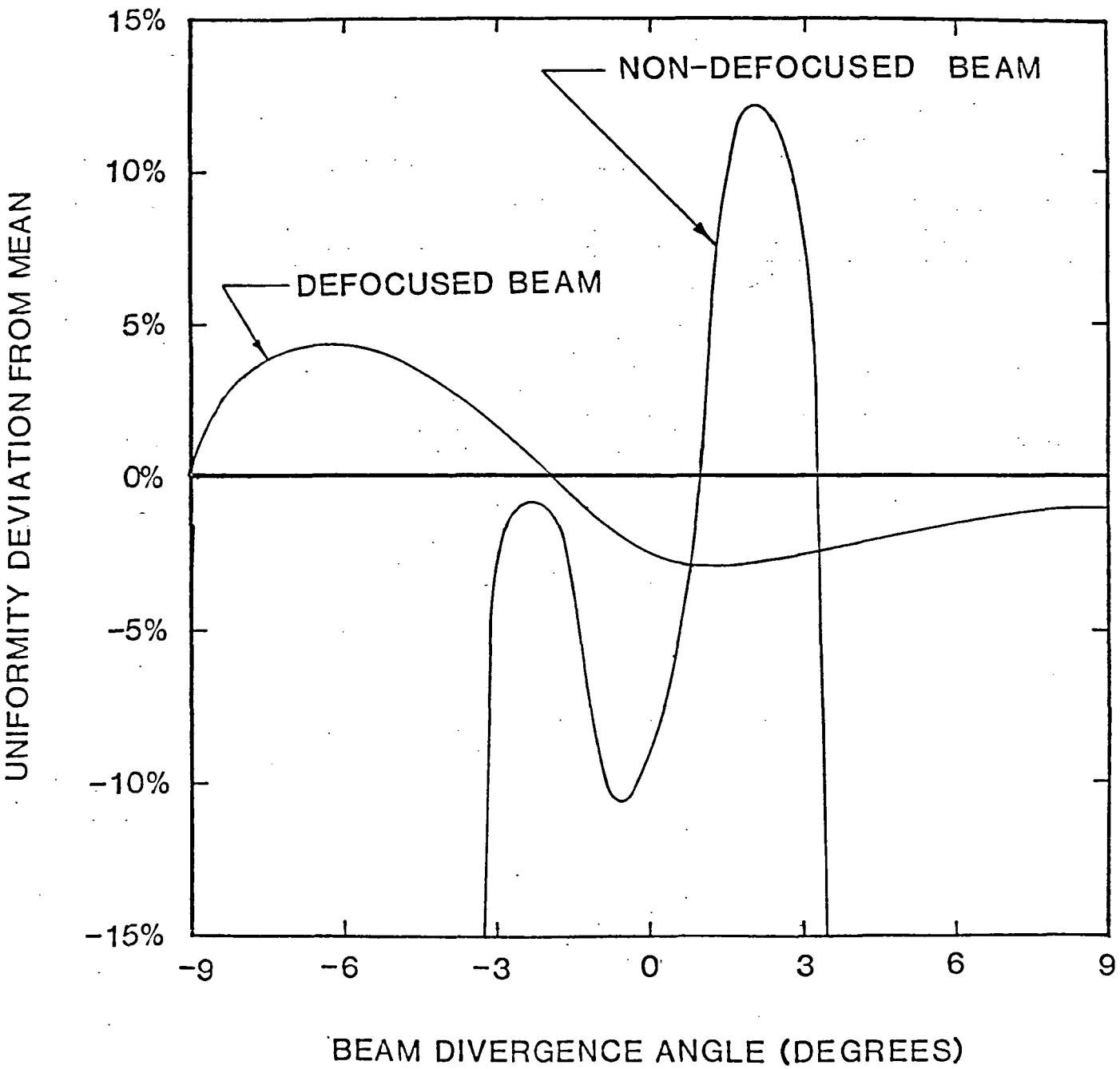


FIGURE 4-9. UNIFORMITY IMPROVEMENT WITH DEFOCUS.

8.3 milliamperes of charged particles would be needed. However, if the worst case of an elliptical beam spot were assumed, at least one third of the current would be lost in forming a rectangular spot, and the total beam needed is 12.5 milliamperes. A real goal of 15 milliamperes was set to guarantee excess margin.

Figure 4-10 shows the results of an early test to increase the phosphorus ion current drawn from the commercial ion source by simply increasing the extraction voltage at the exit slit. This and subsequent tests indicate that simple geometrical changes in the extraction region should be sufficient to effect the high current modification consistent with a beam divergence which is compatible with the downstream beam optics.

4.3.3 Tests of Solar Cells Implanted with NMA Ion Beams

Phosphorus implants in silicon wafers were made using the NMA test facility described above. In the initial tests, the effects of bending the NMA beam on cell efficiency were studied and the results compared with a control implanted by the commercial mass-analyzed ion implanter.

The performance of the test cells, implanted with 10 keV phosphorus doses between 5×10^{14} and 1×10^{16} ions/cm^2 and at three different beam bending angles, are shown in Table 4-1. Data on a control wafer implanted with 10 keV phosphorus in the commercial mass-analyzed implanter with a dose of 2.5×10^{15} ions/cm^2 are also shown. All wafers had a boron implanted back-surface-field and all were co-processed except for the implant.

The most obvious statement about these data is that there is very little difference between any of the cells, despite the wide variation in implant conditions. There is no observable dose effect. The implants at 25° may have a marginally higher efficiency, especially compared to the 0° data. However, it is not obvious whether this subtle difference is due to bending from neutral gas, a neutral beam effect, or the shallower implant. The latter is a result of the steeper implant angle relative to the wafer surface. At 25°, this corresponds to an effective energy of 9.06 keV if the implants were at normal incidence.

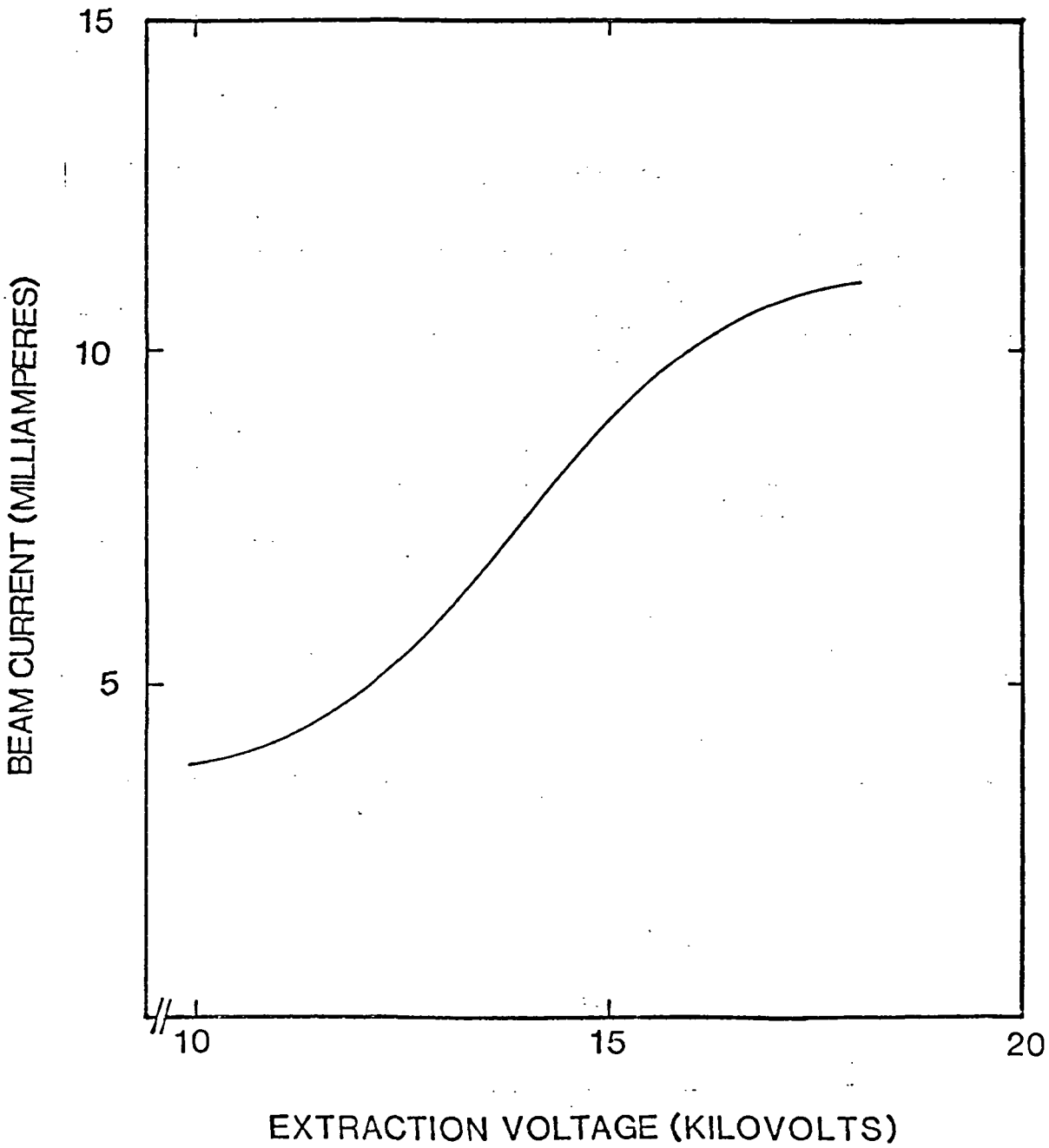


FIGURE 4-10. PHOSPHORUS ION CURRENT AS A FUNCTION OF EXTRACTION VOLTAGE.

TABLE 4-1. NMA IMPLANTED CELL RESULTS

Beam deflection angle	V_{oc} (mV)	J_{sc} mA/cm^2	FF %	(AM0)* %	(AM1)** %
0° (dose = 1)	580±1	28.8±0.21	74.8±0.9	9.22±0.9	15.2±0.1
0° (dose = 2)	579±1	29.0±0.18	75.1±0.5	9.30±0.03	15.4±0.1
0° (dose = 4)	579±2	28.8±0.27	75.3±0.8	9.26±0.10	15.3±0.2
17° (dose = 2)	580±1	29.0±0.18	75.3±0.4	9.36±0.06	15.5±0.1
17° (dose = 4)	579±1	28.7±0.18	75.7±0.4	9.29±0.04	15.3±0.1
25° (dose = 1)	579±2	29.2±0.19	74.9±0.5	9.36±0.06	15.5±0.1
25° (dose = 1)	579±1	29.0±0.19	75.5±0.5	9.35±0.03	15.4±0.1
25° (dose = 4)	580±1	28.8±0.22	75.6±0.7	9.34±0.03	15.4±0.1
Control	577±1	28.8±0.12	75.4±0.4	9.27±0.06	15.3±0.1

*No AR Coating.
**times 1.4 for AR coat and times 1.18 for AM1.

Figure 4-11 compares the quantum efficiency of a typical NMA implant with a control. It can be seen that there is a distinct loss only in the blue performance, consistent with the deep implant expected of a 30 keV neutral beam component present in the 10 keV ion beam of the commercial implanter. The very close match in quantum efficiency above 700 nanometers between these two widely differing implant techniques indicates that a solid phosphorus source gives an NMA implant equivalent to mass analyzed techniques.

Based on these data, it was decided that beam deflection through a large angle to remove neutral components was not required in the design of the NMA ion implanter. This was a major simplification which reduced the complexity of the beam steering and expander control circuitry.

4.4 DESIGN OF NMA ION IMPLANTER

A design layout of the NMA ion implanter is shown in Figure 4-12 with the location of the control electronics and principal components defined. The unit measures about 2.5 feet deep, 6 feet wide by about 6.5 feet high. A cassette wafer loader and unloader is shown in this diagram, although the wafer transport system has been designed to be easily

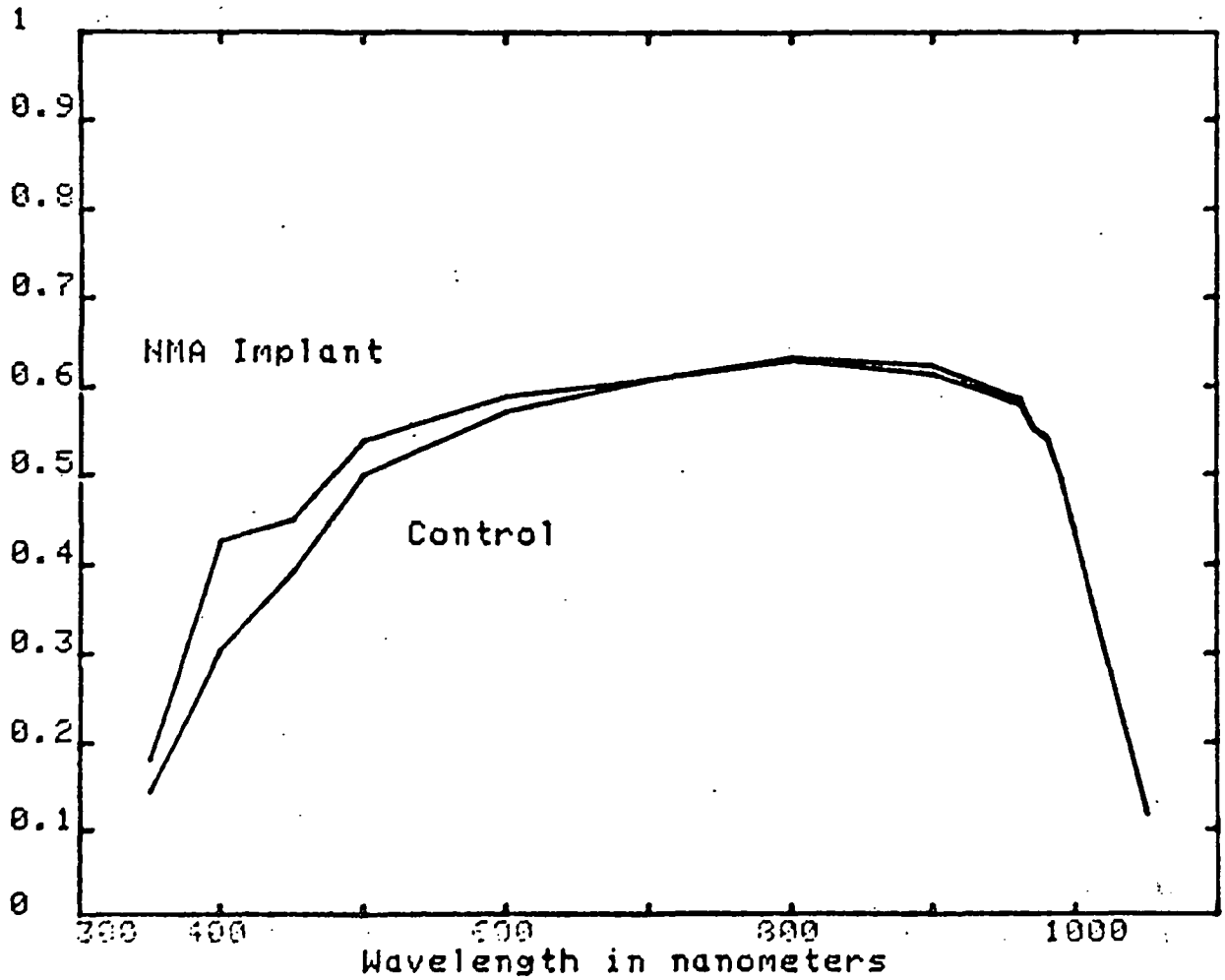
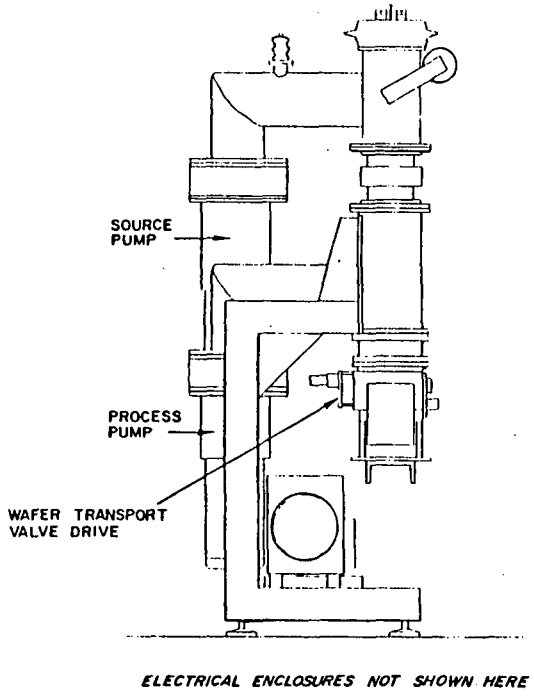


FIGURE 4-11. COMPARISON OF QUANTUM EFFICIENCY FOR NMA IMPLANT AND CONTROL.



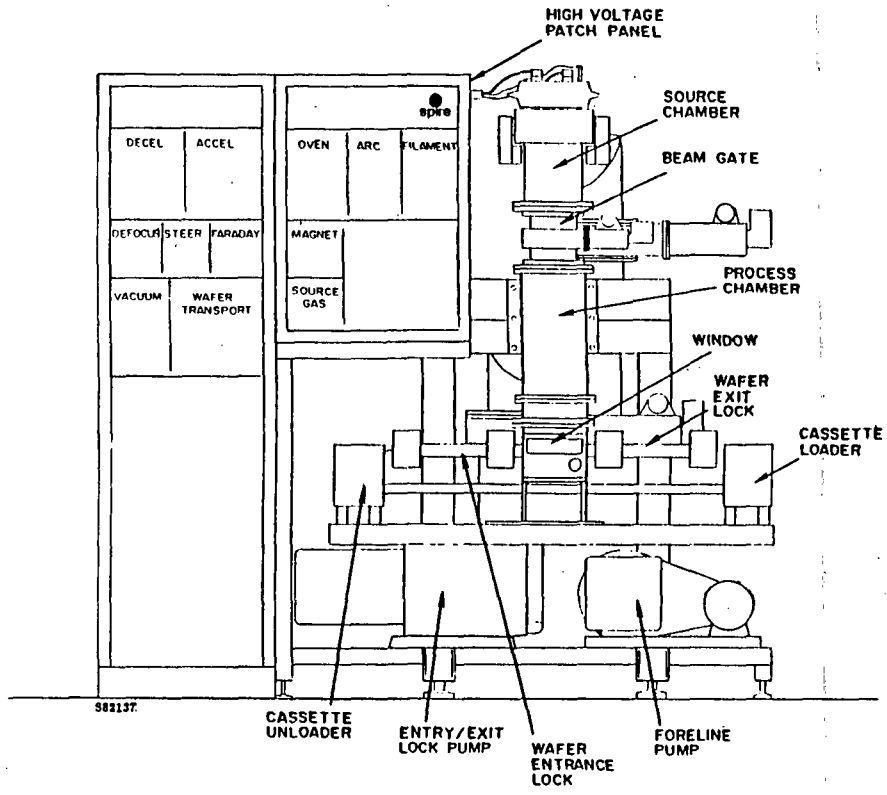


FIGURE 4-12. DESIGN LAYOUT OF NMA ION IMPLANTER.

integrated with the pulsed electron beam annealer. When integrated, the implanted solar cells could be transported directly to the annealer without breaking vacuum. A continuous feed walking beam track moves the wafers under the ion beam which is operated continuously.

The ion beam has two principal axes, parallel and perpendicular to the track motion. Beam uniformity requirements are quite different on these axes, as shown in Figure 4-13. The motion of the wafer will result in an averaging of the implanted dose along the path of the track, and no attempt is needed to generate beam uniformity on that axis. Perpendicular to the track, there is no wafer motion and any irregularities in the beam profile would result in stripes of variable ion dose on the wafer. It is this axis that is important and beam uniformity control is quite critical.

4.5 FABRICATION AND TESTING

4.5.1 Fabrication

The following components of the NMA ion implanter were fabricated in the Spire shop or at outside machine shops:

- Ion source body
- Parts of phosphorus oven
- Beam extraction system
- Beam deflection and defocusing system
- Beam gate
- Faraday cups

Although detailed engineering drawings of all other components of the ion implanter were made, termination of the development program precluded the fabrication of these parts. Layout drawings of the principal parts of the ion implanter are in Appendix 3.

4.5.2 Testing

No testing of the fabricated ion implanter components was performed during the contract period because of the termination of the program. Subsequent tests of the ion source indicated that beam currents greater than 12 mA could be extracted with good uniformity over the long axis of the beam spot.

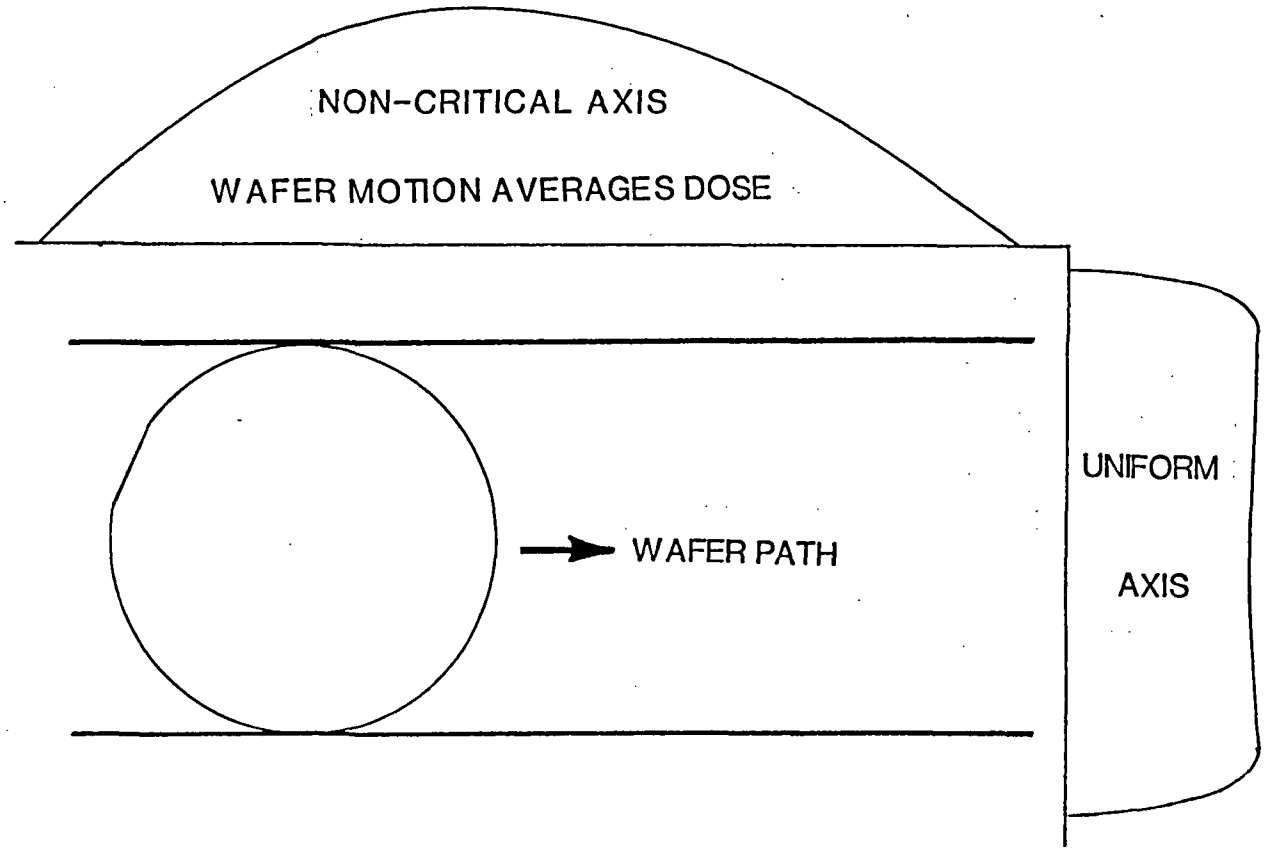


FIGURE 4-13. UNIFORMITY REQUIREMENTS WITH WALKING BEAM TRACK.

SECTION 5
TASKS 4 AND 5 - JUNCTION PROCESSOR SYSTEM INTEGRATION AND COST ANALYSES

5.1 SYSTEM INTEGRATION

The ion implanter, wafer handling and transport system, and pulsed electron beam annealer were to be integrated into a complete operating system and demonstrated prior to delivery to JPL. Operating and maintenance manuals for the overall system and its subsystems were to be delivered along with the equipment.

No system integration was undertaken because of the termination of the development program. An instruction manual for the pulsed electron beam annealer was completed and is included in Appendix II of this report.

5.2 COST ANALYSIS

Based on established data sources and Spire's experience, component lifetimes for critical parts of the junction processor, maintenance schedules, and direct and indirect costs were to be used as input to the Solar Array Manufacturing Industry Costing Standards (SAMICS) computer model for solar cell production cost analyses.

No cost analyses were actually performed because of the termination of the junction processor development program.

SECTION 6
CONCLUSIONS

The development of a processor system for forming solar cell junctions by ion implantation followed by pulsed electron beam annealing, although terminated before its completion, had several positive results. First, the electron beam pulser was successfully demonstrated to anneal the entire surface of 4-inch diameter wafers at a rate corresponding to 10^7 wafers per year. The annealing quality was equivalent to that of standard furnace anneals. Second, the wafer transport system was demonstrated to input wafers from a cassette into the vacuum interlocked processing chamber of the electron beam annealer, place the wafers in position during pulsing, and remove them from the vacuum chamber into an output cassette. Designs for an equivalent, compatible wafer transport for the ion implanter were also made.

A third encouraging result was the demonstration that a non-mass-analyzed (NMA) ion implanter could produce solar cell junctions that are as good as those formed by conventional mass-analyzed ion beams. The NMA beam from a modified Freeman ion source was shown to have adequate uniformity and could be electrostatically steered so that the designs of a complete NMA ion implanter system could be completed with considerable confidence in its performance upon fabrication.

Finally, a series of 4-inch diameter solar cells formed by ion implantation and pulsed electron beam annealing were evaluated and shown to have approximately 12% AM1 efficiency after metalization. In fact, the metalization appeared to set the efficiency limit for these cells.

APPENDIX I

SUMMARY OF SHEET RESISTIVITY MAPPING OF PULSE ELECTRON BEAM ANNEALED WAFERS AND PERFORMANCE EVALUATION OF SOLAR CELLS

October 1982

Submitted to:
JET PROPULSION LABORATORY
4800 Oak Grove Road
Pasadena, CA

Submitted by:
SPIRE CORPORATION
Patriots Park
Bedford, MA 01730

SUMMARY OF SHEET RESISTIVITY MAPPING OF PULSE ELECTRON BEAM ANNEALED WAFERS AND PERFORMANCE EVALUATION OF SOLAR CELLS

The uniformity and quality of the four-inch pulsed electron beam anneal has been measured by combining sheet resistance mapping with conversion efficiency mapping. The cell conversion efficiency (without antireflection coating) is found to be 7.5% (AM0) with a five percent variation across the wafer. With an antireflection coating the AM1 efficiency would be approximately 12%.

Starting material for the experiments to the described consisted of four-inch 10 ohm-cm (100) Si wafers. Each wafer was provided like a back surface field and was then implanted with phosphorus at 10 keV to a dose of 2.5×10^{15} ions/cm^2. This implantation was annealed with a single submicrosecond burst of electrons which deposited approximately 1 joule/cm^2. One burst annealed the entire wafer.

Numerous sheet resistance maps were constructed in order to test the dependence of uniformity on beam parameters. Figure 1 shows the result of studies of the effect of charging voltage on sheet resistance. The set of data denoted as "center" show the four-point probe values of sheet resistance at the center of each wafer (6 wafers). The data denoted by R ~ 1" indicate the average of eight measurements taken on a circle of radius = 1". The error bars indicate one standard deviation of the average. Similarly, the data set denoted R ~ 2" shows the sheet resistance averaged over eight measurements taken near the edge of the wafer. In this way, the overall uniformity, as a function of beam charging voltage, was measured and judged. The range between 165 kV and 185 kV is seen to offer best uniformity.

On the basis of the above experiment, 165 kV was selected for the charging voltage. The dependence of the uniformity of the anneal on magnetic field was also examined, by using magnet current as the parameter. Figure 2 shows the result of this analysis. The best anneals are achieved with magnet current in the range of 8.5A to 10A.

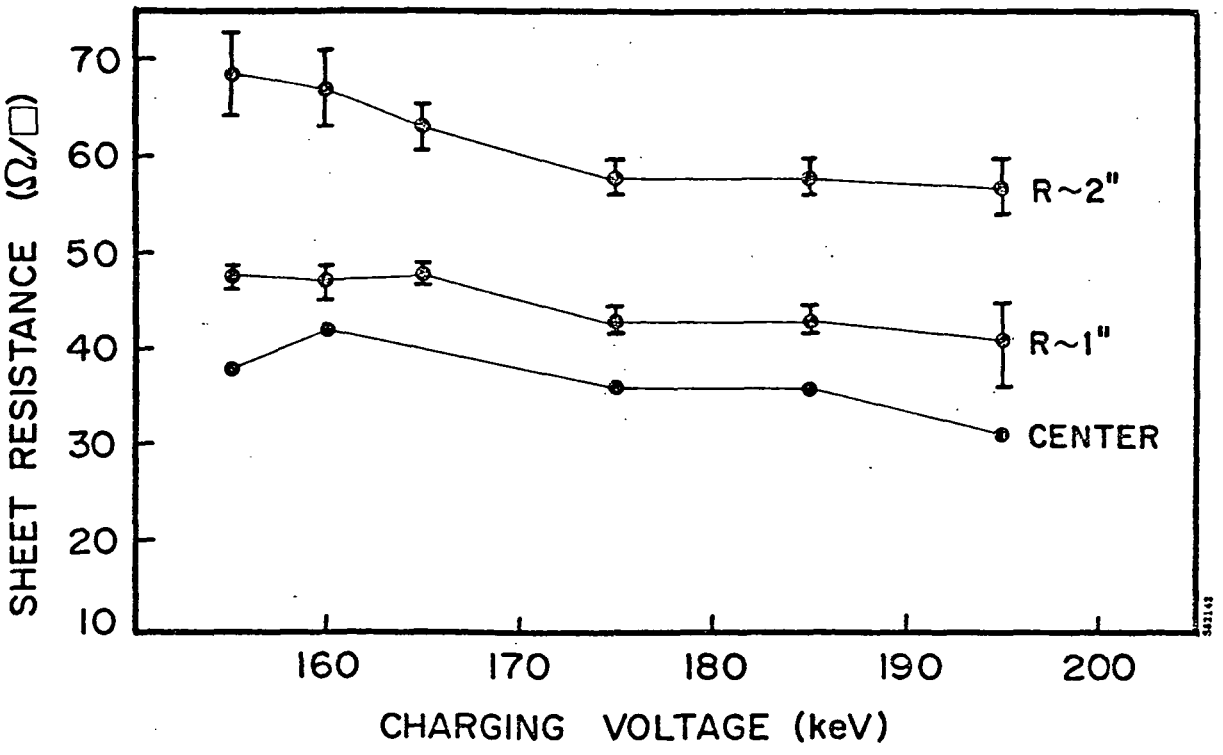


FIGURE 1. SHEET RESISTANCE UNIFORMITY AS A FUNCTION OF CHARGING VOLTAGE.

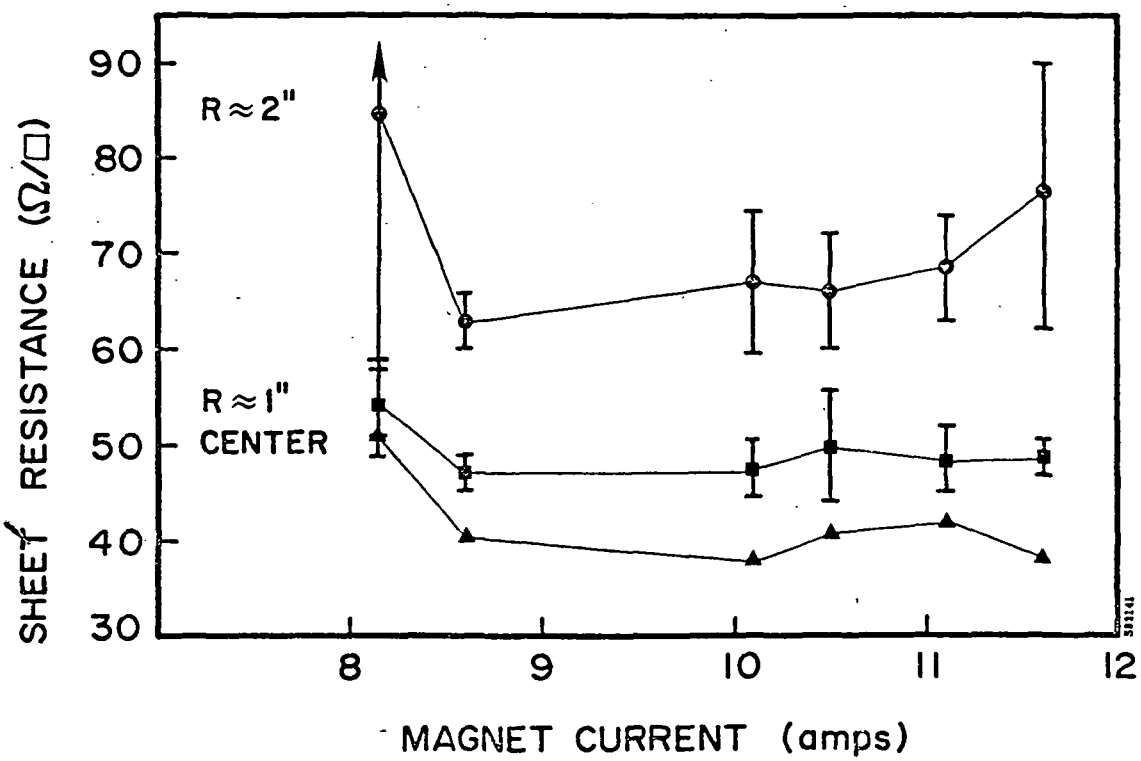


FIGURE 2. SHEET RESISTANCE UNIFORMITY AS A FUNCTION OF MAGNETIC FIELD, IN UNITS OF MAGNET CURRENT. (Magnetic field in this current range is 0.16 kilogauss per ampere.)

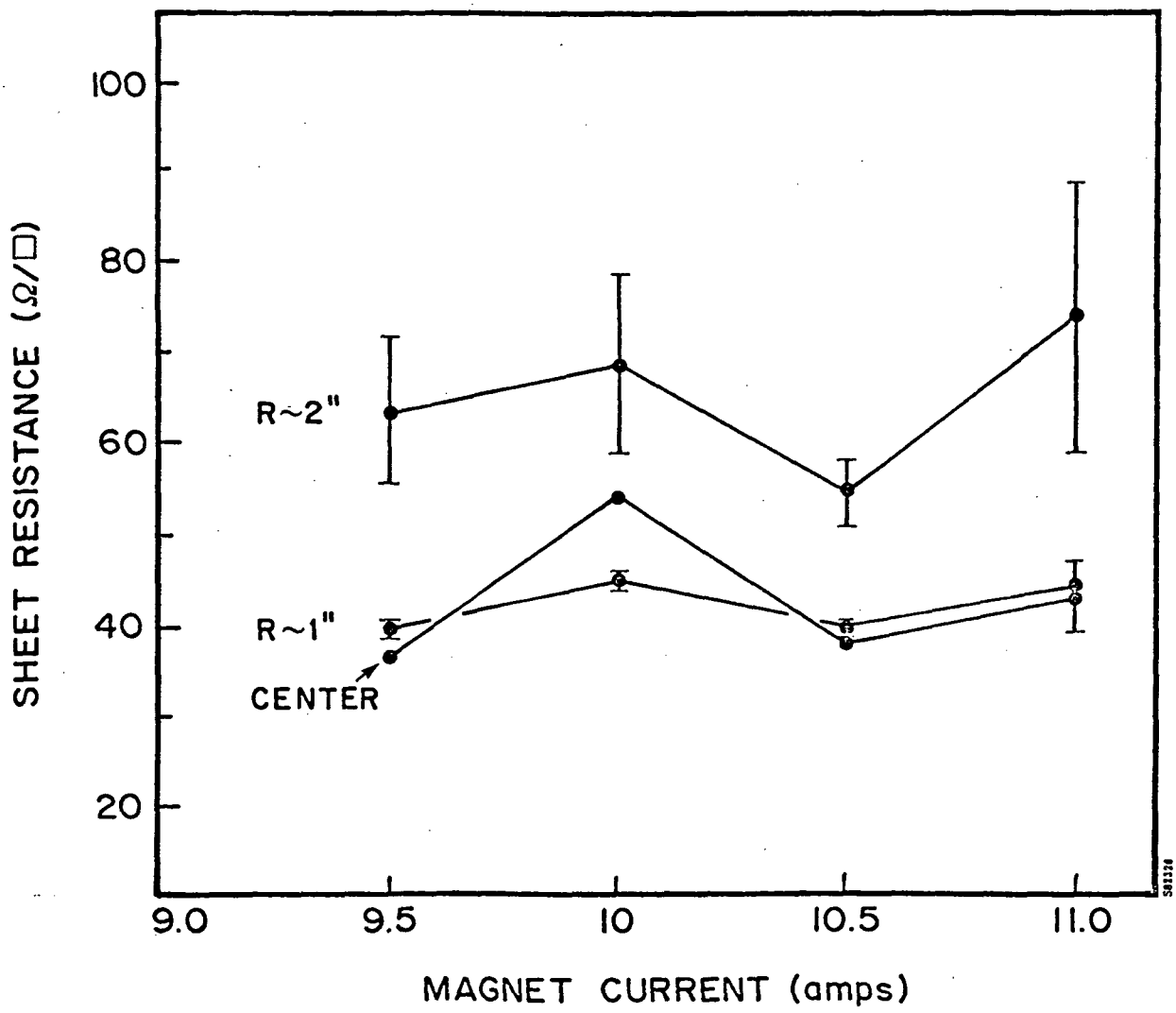


FIGURE 3. SHEET RESISTANCE UNIFORMITY AS A FUNCTION OF MAGNETIC CURRENT AFTER MACHINE MAINTENANCE. (Magnetic field in this current range is 0.16 kilogauss per ampere.)

The effect of magnet current on sheet resistance uniformity was re-examined after maintenance to the storage capacitors. Figure 3 shows the result. Based on this data, a beam charging voltage of 170 keV and magnet current of 10.5A were chosen for pulsing.

In a second set of experiments, a pattern of 60 1cm x 1cm squares was used to define the measurement configuration. For the purposes of sheet resistance mapping, 60 mesas were formed by using a wafer dicing saw which cut grooves of depth ~1 mil between the mesas. In this way, the junction on each mesa was separated from the other junctions. For solar cell measurements a metal grid pattern was first deposited by using photolithography and electron beam evaporation of Ti-Pd-Ag. The metal pattern consisted of 60 1cm x 1cm solar cell grids which were not interconnected. The wafer dicing saw was used to isolate the junctions of the 60 cells.

Figure 4 shows a detailed sheet resistance map obtained by four-point probe measurement on 60 mesas. The average sheet resistance is 36.2 Ω/□ with a standard deviation of 7.2 Ω/□. Although this is a 20% variation, the cell performance to be described below showed much less variation.

Figures 5-8 show maps of the open circuit voltage (V_{oc}), short circuit current (J_{sc}), fill factor (FF) and efficiency (Eff) for solar cells formed on 60 individual mesas. The insolation spectrum was AM0, 135 mW/cm^2. Cell temperature was maintained at 25°C by a water-cooled block. The average AM0 efficiency is 7.56% with a standard deviation of 0.4. The percent standard deviation is better than 5%, indicating excellent uniformity. Were this wafer to be made into a four-inch cell with AR coating, it would have an efficiency of approximately 12%.

Examination of the fill factor map indicates that some diodes have fill factor of less than 70%. This is attributable to the metallization which partially failed in some regions. Thus, the junction fill factor resulting from the pulsed electron beam anneal is in the 70% to 80% range.

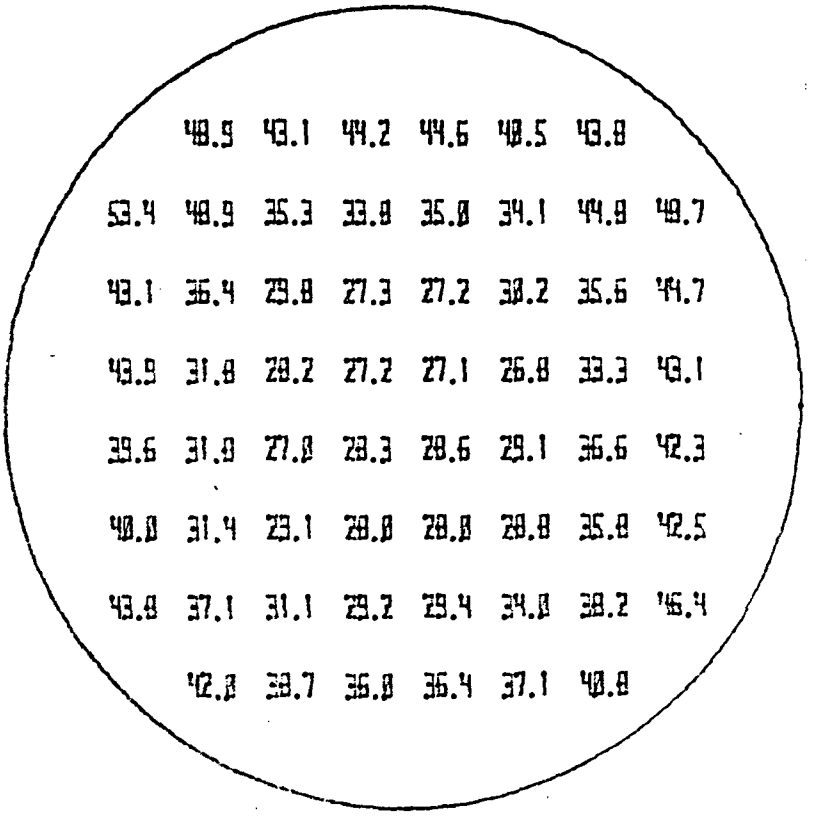


FIGURE 4. SHEET RESISTANCE MAP OF 60 INDIVIDUAL MESAS (ohms per square).

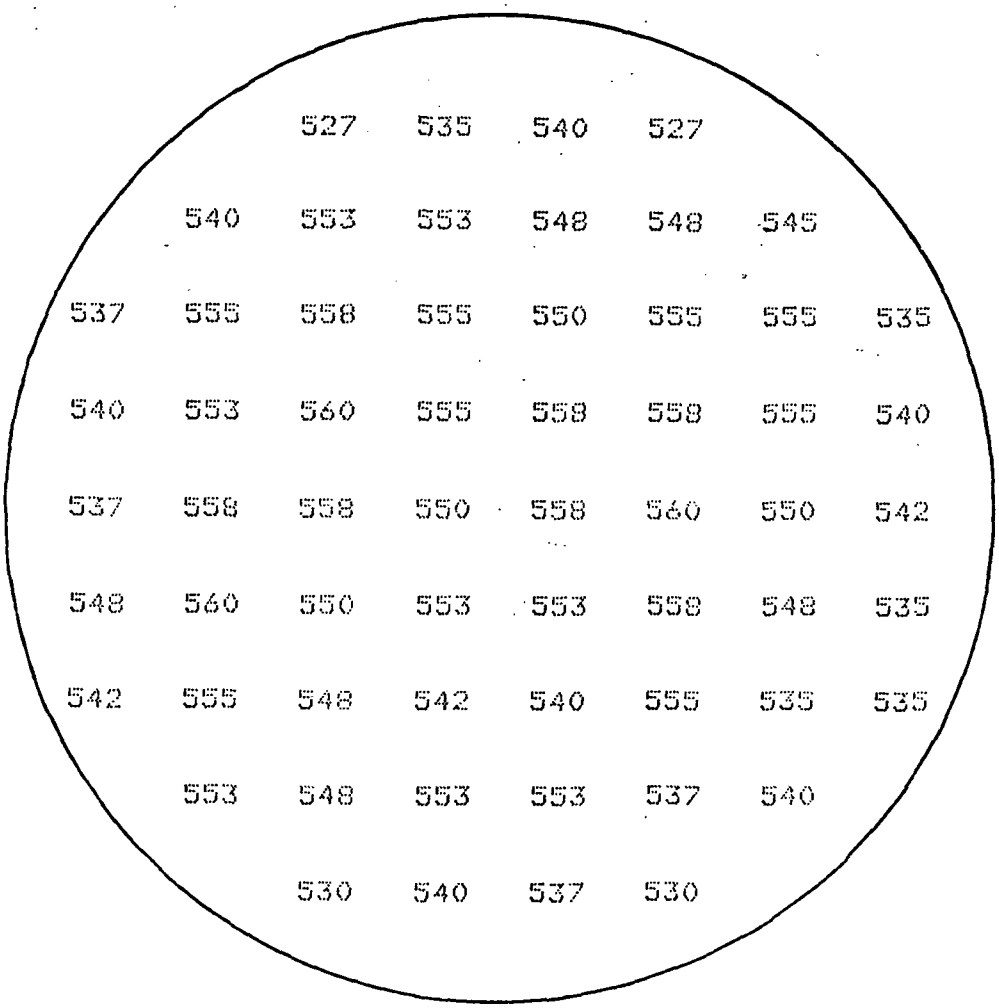


FIGURE 5. V_{OC} MAP OF 60 MESA CELLS.

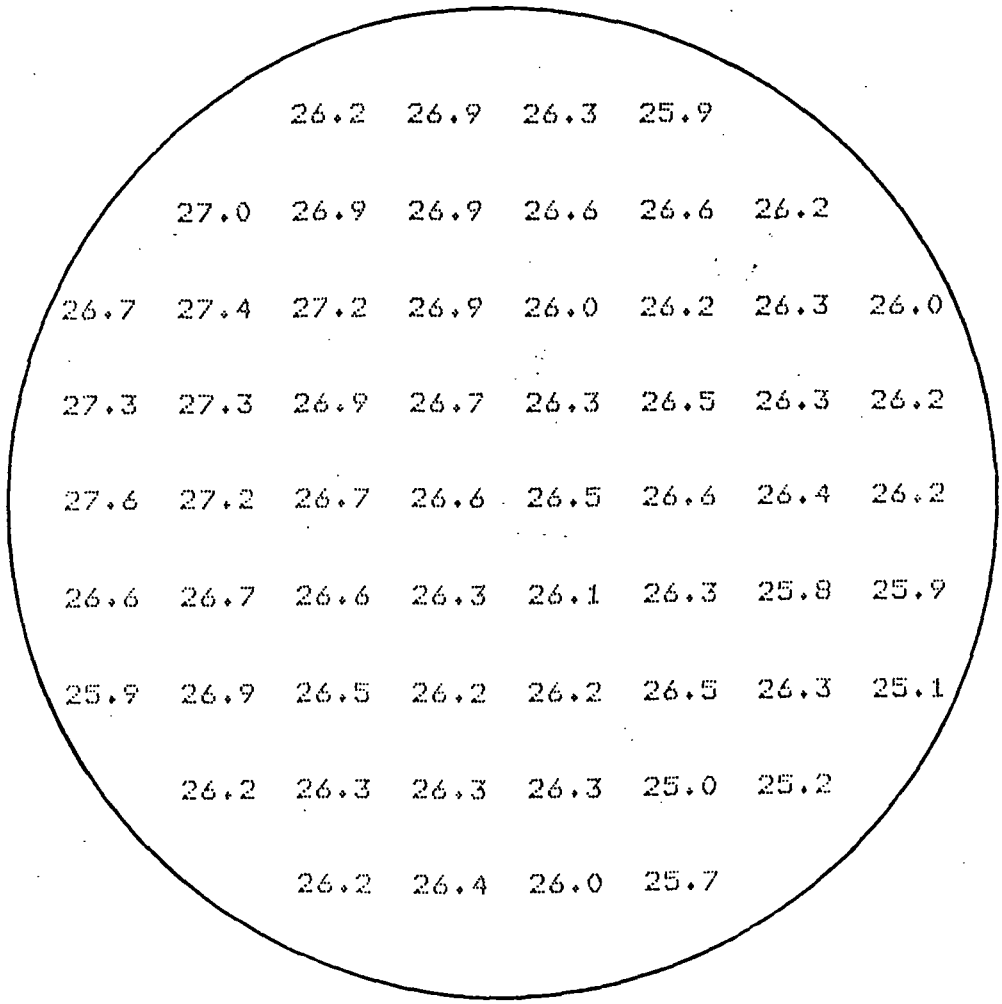


FIGURE 6. J_{SC} MAP OF 60 MESA CELLS.

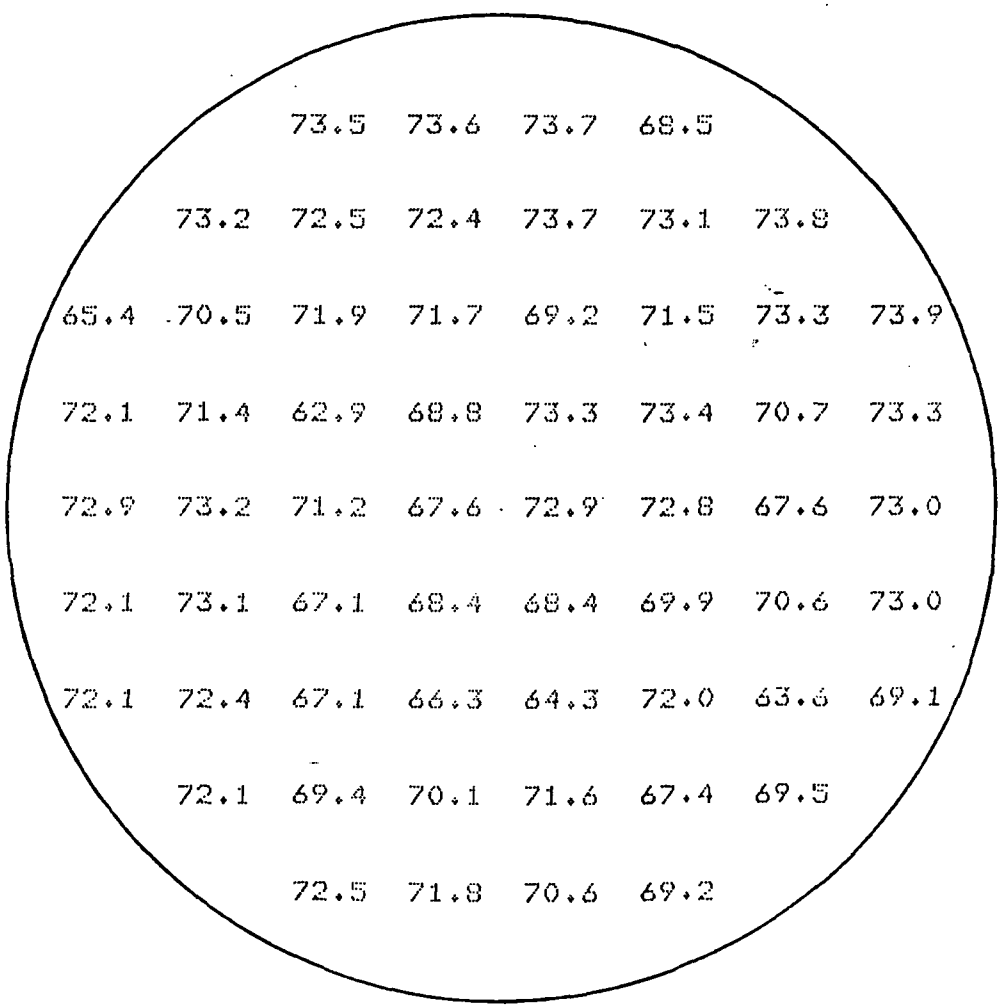


FIGURE 7. FILL FACTOR MAP OF 60 MESA CELLS.

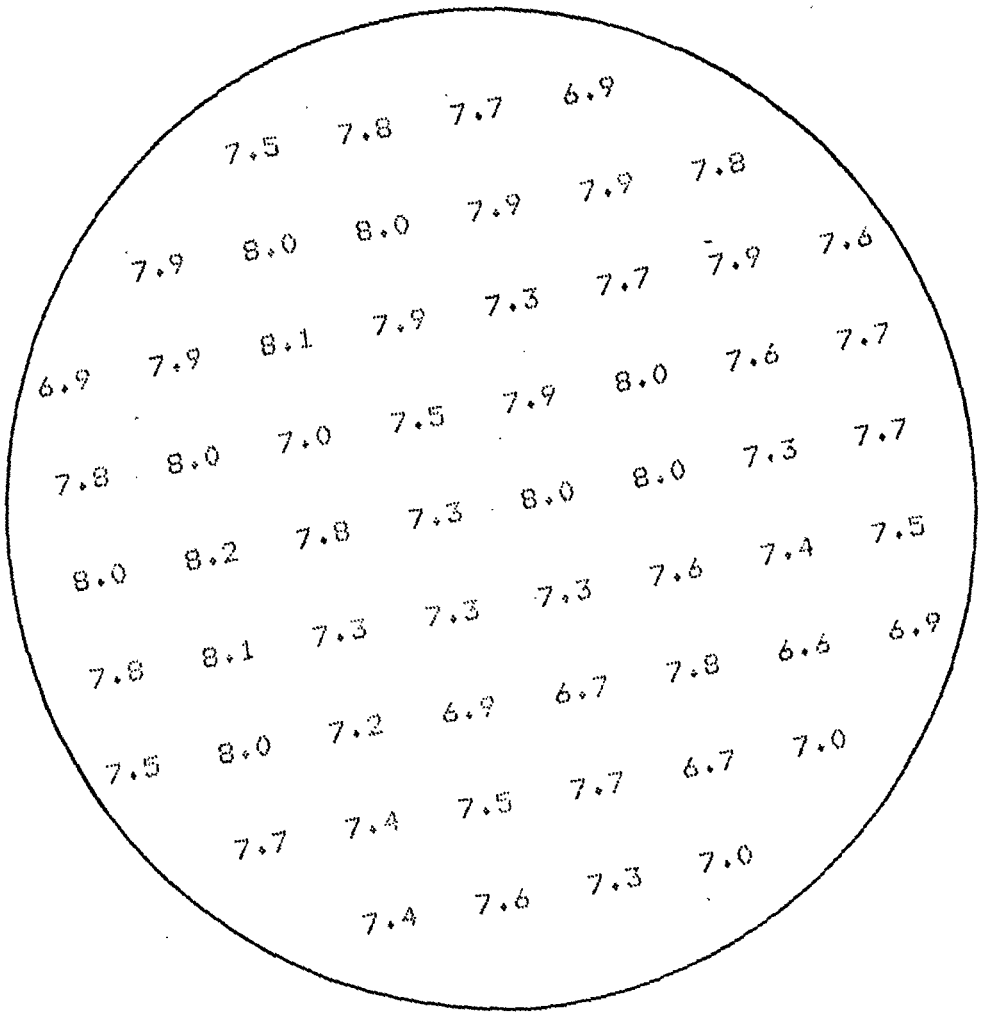


FIGURE 8. EFFICIENCY MAP OF 60 MESA CELLS.

Table I shows a summary of the above wafer and three other wafers. A total of 240 cells were formed in this way, and the complete maps can be found in the appended data tabulation. The results indicate that satisfactory annealing has been achieved over an area of 81 cm^2.

SUMMARY

The results of characterization of ion implanted pulsed electron beam annealed solar cells indicate that efficiency attainable with this technology is 12% over a four-inch wafer. The uniformity is satisfactory, yielding cells, (distributed over a four-inch wafer) with a standard deviation of 5%. The metallization appears to be limiting the efficiency.

TABLE 1. SUMMARY OF SOLAR CELL PERFORMANCE MAPPING

WAFER ID	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	Eff (%)
4205-1	543	25.9	70.0	7.29
	(13)	(0.7)	(6.3)	(0.78)
4205-2	543	25.9	72.1	7.49
	(14)	(0.7)	(1.4)	(0.35)
4205-3	530	25.3	70.0	6.92
	(11)	(0.4)	(2.5)	(0.41)
4205-4	547	26.4	70.8	7.56
	(9)	(0.5)	(2.7)	(0.40)

NOTES: Insolation Spectrum is AM0, 135 mW cm^{-2}, T = 25°C, No antireflection coatings were employed. Each entry in the table represents an average of 60 cells on the wafer; the standard deviation is shown in parenthesis.

TABULATION
OF DATA

4205-1 Voc MAP

$\bar{V}_{oc}$ = 542.5 mV

σ = 13.4 mV

		527	540	527	529		
	522	517	545	547	542	524	
527	524	547	553	555	558	542	519
524	532	555	555	545	555	553	529
527	535	547	550	555	555	553	529
535	555	560	558	558	563	558	514
537	550	555	560	560	553	555	527
	542	550	547	542	550	550	
		527	537	537	527		

4205-1 Jsc MAP

$\bar{J}_{sc}$ = 25.92 mA/cm²

σ = 0.71 mA/cm²

		26.4	26.4	26.3	25.4		
	26.6	22.3	26.5	26.4	25.9	26.1	
26.6	26.7	26.2	26.1	25.9	25.7	26.1	25.5
27.0	26.8	26.2	26.1	26.3	26.0	25.7	25.8
27.1	26.3	26.3	25.6	25.7	26.0	26.0	25.9
26.7	26.3	26.0	25.6	25.7	25.7	25.8	25.6
25.8	26.3	26.2	25.8	26.1	26.0	25.7	25.1
	26.3	25.9	26.0	26.5	26.0	24.8	
		25.4	25.1	24.5	24.3		

4205-1 Efficiency MAP

$\bar{h}$ = 7.29 %

σ = 0.78

		5.6	7.6	6.4	7.2		
	5.9	2.9	7.5	7.6	7.5	7.0	
7.4	7.3	7.8	7.7	7.8	7.8	7.5	7.0
7.5	7.3	7.7	7.7	6.9	7.7	7.6	7.4
7.6	6.0	7.6	7.5	7.6	7.6	7.7	7.1
7.7	7.9	7.8	7.6	7.6	7.8	7.7	5.5
7.5	7.7	7.6	7.8	7.9	7.6	7.6	7.1
	7.7	7.6	7.4	7.2	7.7	7.2	
		7.0	7.3	7.1	6.7		

4205-1 Fill Factor MAP

$\overline{FF} = 69.96\%$

$\sigma = 6.31$

		54.8	72.2	62.4	72.9		
	57.6	34.2	70.4	71.0	72.0	69.7	
71.1	70.7	73.3	72.4	73.2	73.3	71.9	71.5
72.2	68.9	71.3	72.1	65.2	72.4	72.0	72.9
72.5	57.3	71.8	71.7	71.8	71.6	72.5	70.2
72.9	73.1	72.8	71.9	71.9	73.2	72.3	56.5
73.5	71.8	71.0	72.6	72.8	71.4	71.8	72.5
	72.7	72.5	70.5	67.6	72.7	70.9	
		70.5	73.3	72.6	71.1		

4205-2 Voc MAP

$\overline{V_{oc}} = 542.8$ mV

$\sigma = 14.1$ mV

		519	527	529	519		
	517	540	545	550	545	522	
519	540	545	555	555	550	540	511
524	545	555	555	550	555	542	527
527	545	555	547	555	560	553	529
527	553	560	560	558	553	553	537
522	560	555	560	558	558	547	529
	545	560	558	555	547	545	
		524	529	532	529		

4205-2 Jsc MAP

$\bar{J}_{sc} = 25.89$ mA/cm²
$\sigma = 0.68$ mA/cm²

		25.3	26.2	25.8	25.3		
	26.6	26.7	26.3	26.0	25.8	25.9	
26.2	26.8	26.6	25.8	25.6	25.9	25.7	25.4
26.7	26.3	26.3	26.1	26.0	26.0	26.0	25.9
26.9	26.7	26.4	26.2	26.1	26.0	25.9	25.9
26.9	26.8	26.4	26.2	26.0	25.5	25.3	25.3
25.6	26.5	26.7	26.2	26.1	25.8	25.2	24.6
	25.4	26.4	25.8	25.7	25.7	24.3	
		24.1	24.9	24.8	23.6		

4205-2 Efficiency MAP

$\bar{\eta} = 7.49\ \%$

$\sigma = 0.35$

		6.9	7.5	7.5	6.9		
	6.9	7.9	7.9	7.7	7.6	7.2	
7.3	7.8	7.2	7.8	7.7	7.4	7.5	6.9
7.5	7.7	7.9	7.7	7.6	7.7	7.5	7.3
7.6	7.9	7.9	7.6	7.7	7.8	7.6	7.4
7.7	8.0	7.8	7.7	7.5	7.2	7.4	7.0
7.0	8.1	7.9	7.7	7.6	7.6	7.4	6.9
	7.5	8.0	7.7	7.6	7.6	6.8	
		6.8	7.0	7.1	6.7		

4205-2 Fill Factor MAP

$\overline{FF}$ = 72.09 %
σ = 1.44

		71.4	73.2	74.1	71.3		
	67.8	73.8	74.2	73.3	73.0	72.6	
72.5	72.8	67.1	73.3	73.5	70.0	72.9	72.3
72.6	73.2	73.6	71.9	72.4	72.7	72.2	72.5
72.6	73.5	72.8	71.9	71.7	71.9	71.7	72.7
73.2	73.3	71.5	70.7	69.7	68.7	71.7	69.7
71.0	74.0	72.1	71.0	71.0	71.6	72.6	71.4
	73.2	73.0	72.3	71.9	73.0	69.7	
		72.4	72.3	72.7	72.9		

4205-3 Voc MAP

$\overline{V_{oc}} = 529.5$ mV

$\sigma = 10.6$ mV

		537	537	531	521		
	534	537	531	537	534	524	
539	537	521	534	529	526	524	519
539	534	521	529	531	496	516	534
534	521	531	537	521	485	514	537
529	531	529	534	521	524	514	534
524	529	537	534	524	516	539	534
	531	544	534	534	539	539	
		539	542	547	537		

4205-3 Jsc MAP $\bar{J}_{sc} = 25.27\ mA/cm^2$
$\sigma = 0.43\ mA/cm^2$

		25.0	25.1	25.5	25.3		
	25.3	25.1	25.2	24.7	24.8	25.3	
25.5	25.4	25.3	24.8	24.6	24.6	25.2	24.7
25.8	25.4	25.4	25.1	24.7	25.4	25.0	24.6
25.9	25.8	25.3	25.5	25.0	25.7	25.2	24.7
25.3	25.6	25.7	25.2	25.0	25.1	24.7	24.7
25.9	26.1	26.0	26.2	25.2	25.2	25.0	24.5
	25.8	26.1	25.3	25.3	25.1	24.8	
		25.8	25.5	25.6	25.4		

4205-3 Efficiency MAP

$\bar{\eta} = 6.92\ \%$

$\sigma = 0.41$

		7.2	7.2	7.2	6.7		
	7.1	7.2	7.1	7.0	7.1	6.9	
7.5	7.2	6.6	6.9	6.5	6.5	6.9	6.3
7.5	7.3	6.7	6.7	6.8	6.0	6.3	6.9
7.4	6.7	6.9	7.0	6.5	5.8	6.1	6.9
7.2	7.1	6.9	7.0	6.4	6.6	6.2	6.8
7.3	7.5	7.3	7.2	6.7	6.2	7.0	6.9
	7.4	7.6	7.0	7.0	7.1	7.0	
		7.4	7.3	7.5	7.2		

4205-3 Fill Factor MAP

$\overline{FF}$ = 69.99 %

σ = 2.48

		72.2	72.0	72.4	69.2		
	71.4	72.1	71.5	71.7	72.3	70.9	
73.9	71.3	68.1	70.7	68.1	68.2	71.2	66.6
72.7	72.5	67.9	68.1	69.9	64.2	66.6	71.0
72.9	67.6	70.0	69.2	67.3	63.5	64.2	70.3
72.8	70.0	68.4	70.0	66.6	67.7	66.5	69.6
72.8	73.0	71.2	70.1	68.3	64.5	70.0	71.1
	72.8	72.5	70.4	70.0	71.3	70.5	
		71.7	71.7	72.3	71.7		

C-2

APPENDIX 2

PULSED ELECTRON BEAM/WAFER TRANSPORT SYSTEMS OPERATIONS AND MAINTENANCE

December 1982

Submitted to:
JET PROPULSION LABORATORY
4800 Oak Grove Road
Pasadena, CA

Submitted by:
SPIRE CORPORATION
Patriots Park
Bedford, MA 01730

I. INTRODUCTION

This manual is intended to provide the reader with a working knowledge of the SPI-PULSE™ 7000 electron beam processor shown in Figure 1-1. The major components of the equipment - the pulser, wafer handling system, and microprocessor - are described. Figure 1-2 shows the overall system. Sufficient theory is presented to acquaint the reader with the transmission line properties and field emission behavior of the processor. Operating instructions and maintenance and troubleshooting procedures are also provided.

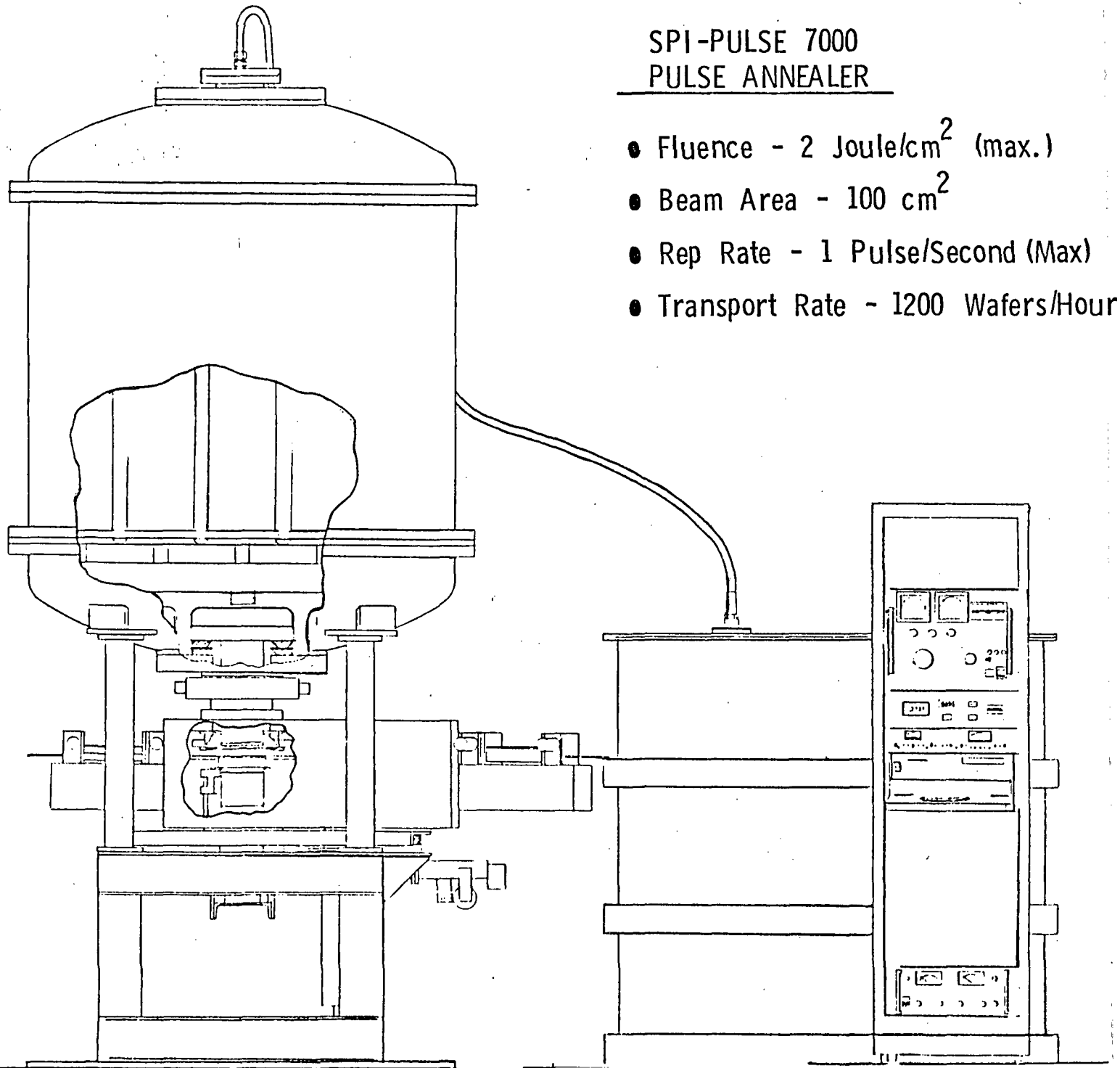
The SPI-PULSE 7000 is designed to irradiate samples with a high power electron beam. The electron energy is kept low to minimize radiation damage to crystals, to minimize brehmsstrahlung radiation produced, and to maximize the energy dose on the surface of the sample. For a typical application, annealing ion-implantation radiation damage in crystals, the electron beam current density is very high, and self-electric and self-magnetic fields dominate beam propagation.

The SPI-PULSE 7000 is also designed to irradiate the surface of a sample in a short pulse. The objective is to heat the surface to a high temperature, possibly melting a thin layer, without heating the bulk of the material. Rapid cooling of the surface - quenching - by thermal conduction to the bulk of the sample material will occur. The principal effect sought is thermal, but the user should be aware of the electrical effects and x-rays produced.

WARNING: High voltage (up to 300 kV) is present in the charging circuit of the SPI-PULSE 7000. Accidental contact by personnel with this high voltage can be fatal. Maintenance of the high-voltage charging system should only be performed by trained personnel familiar with the hazards involved. Spire Corporation assumes no liability for any injury incurred through negligence.

SPI-PULSE 7000
PULSE ANNEALER

- Fluence - 2 Joule/cm^2 (max.)
- Beam Area - 100 cm^2
- Rep Rate - 1 Pulse/Second (Max)
- Transport Rate - 1200 Wafers/Hour



spire

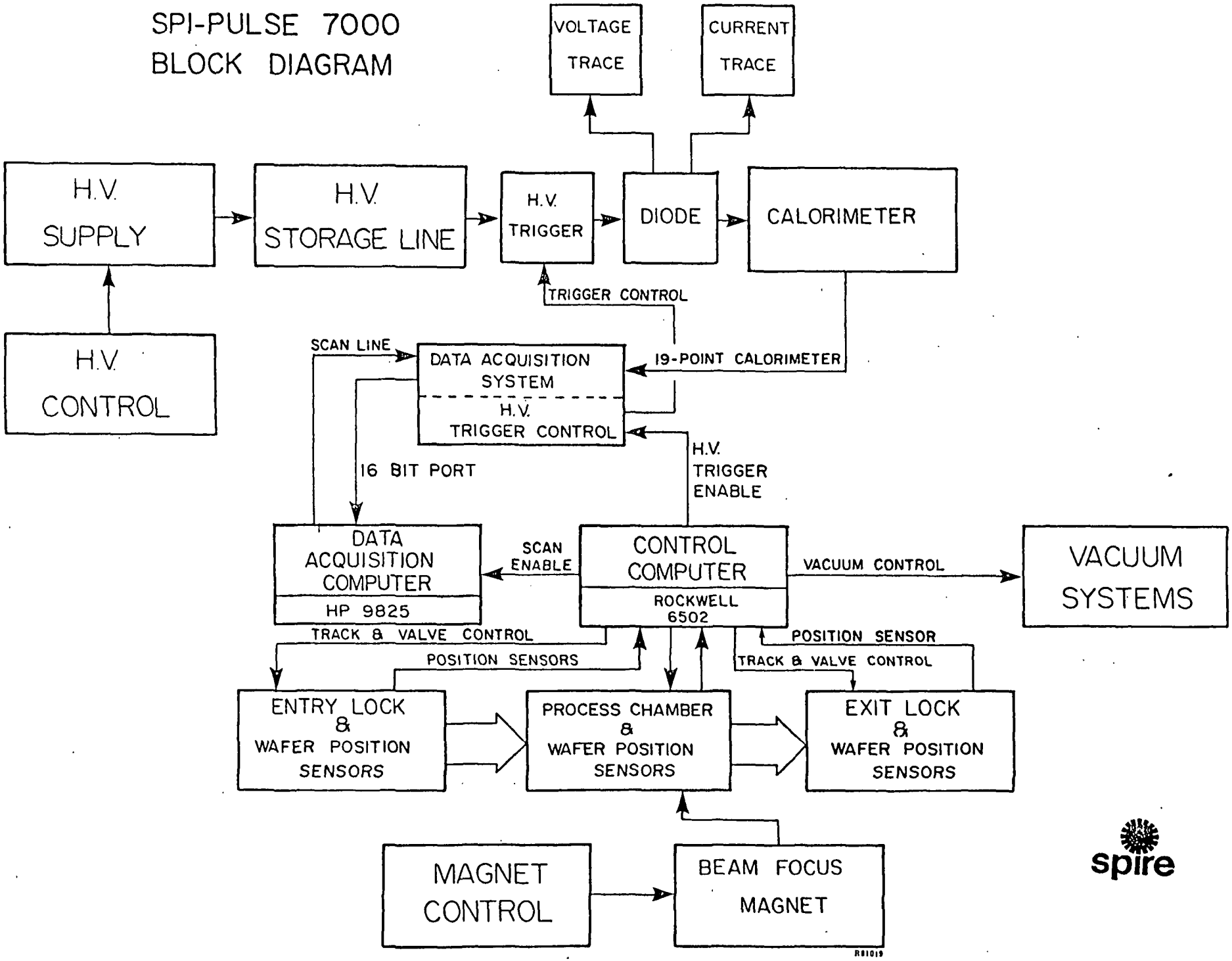


FIGURE - 1-2 SPI-PULSE 7000 BLOCK DIAGRAM

II. THEORY OF OPERATION

A. Computer Control of Components

The microprocessor subsystem controls all system functions in accordance with the software program which is currently resident in RAM, having been loaded from tape or entered from the keyboard.

Control is implemented through memory mapped I/O. In a memory mapped I/O system each output which must be turned on and each input which must be sensed is connected to a line which corresponds to one of eight bits of a register. These registers are addressed by the microprocessor as though they were locations in memory, thus turning on or off or sensing the state of any line is accomplished by writing a bit pattern into, or reading a pattern from the appropriate memory location.

In order to provide a high degree of noise immunity, the Orbitrac and End Station Control Systems optically isolate every input and output from the microprocessor to the system, except for operator interface elements.

The circuits used consist of three types; optically coupled outputs for low current DC use; optically coupled inputs for sensing limit switches, etc.; and doublely optically isolated AC outputs for 110 volt devices. Certain inputs and outputs require additional conditioning, and several motor drive boards and a sensor pre amp board are included in the I/O circuitry.

The valve motor output provides the 1 amp at 24 volts required to open and close the locks; regulate the voltage to these motors for consistent cycle times; and sense the limit switches in order to automatically turn off a motor when the valve reaches the position required.

The sensor pre amp circuitry provides buffering and boosts the signal to noise ratio of the outputs of the optical wafer sensors before sending the signal to the microprocessor.

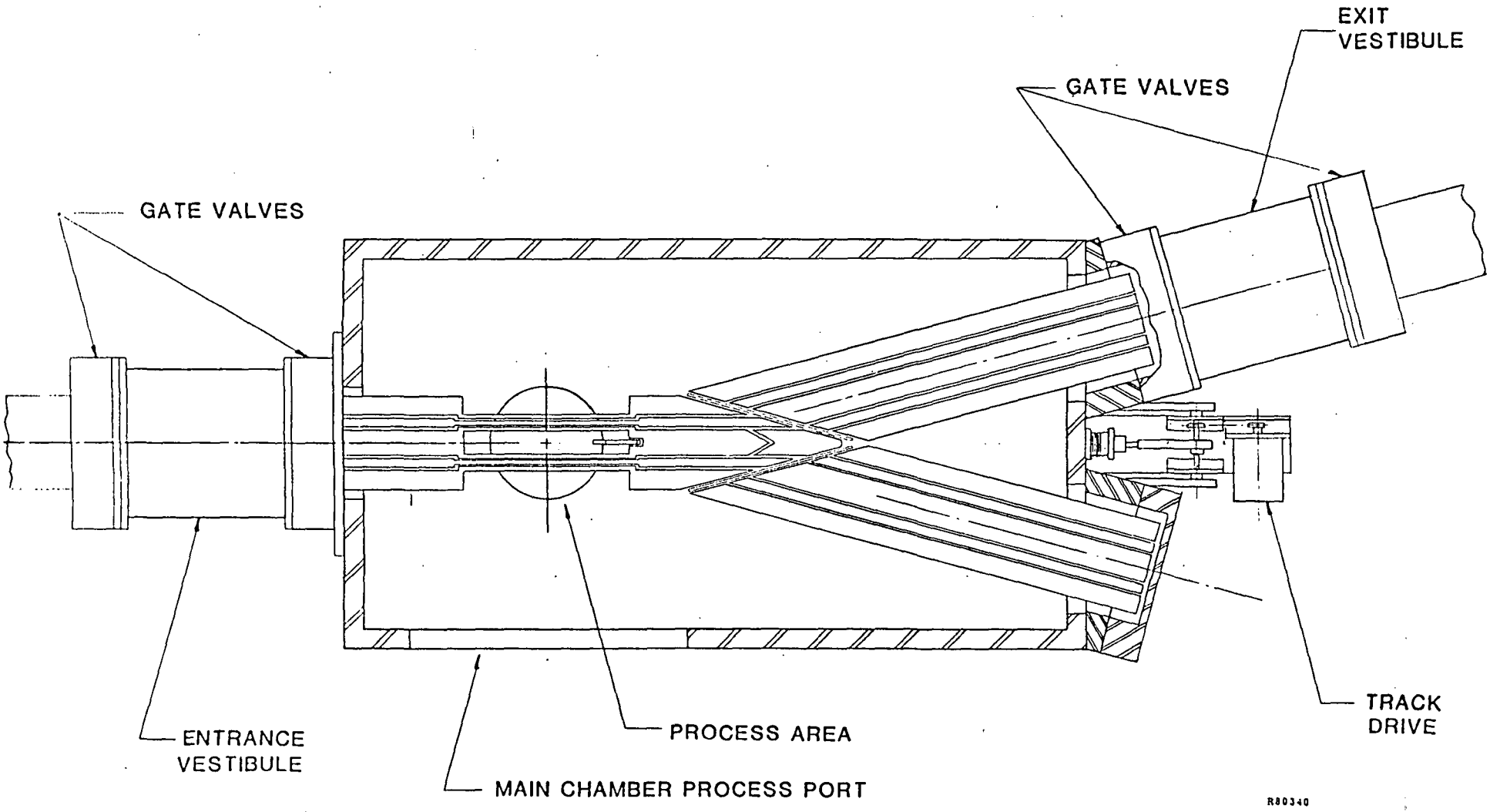
The stop, lifter, and trigger mechanisms are direct electrical feeds to the microprocessor. In the automatic mode, lifter operation is dependent on the activation of the stop mechanism, and the trigger is dependent on the lifter operation.

B. Function of High Voltage, Liners, Triggers and Diode Components

1. High Voltage
   a. Ion Implantation damages the crystal structure creating an amorphous surface. Through the use of high voltage sub-microsecond discharge, it is possible to melt the surface of the wafer to a depth of approximately 0.5 microns. This melted region quickly recrystallizes using its unmelted base as a region to initiate crystal growth.
   b. The high voltage power supply is a two section, 300 kilovolt oil insulated DC unit rated at 17 milliamps, continuous load current.

2. Liners (Capacitor Stack)
   a. The energy store is a coaxially configured group of high-voltage capacitors which serve as a transmission line during discharge to the field emission diode. The 13 capacitors are charged in parallel through a high voltage resistor which isolates and protects the power supply from surges. The high voltage power supply is connected to the resistor through a power cable.

3. Trigger Mechanism
   a. The trigger cup is connected to and mounted below the common collector plate at the lower end of the capacitor stack. It extends across the gap between the capacitor stack and the dome cap of the field emission diode. The electropneumatically actuated trigger, when actuated, initiates the discharge of the energy stored in the capacitor stack unit into the diode.



PROCESS CHAMBER OF SPI-PULSE 7000 - Top View

spire

4. Diode Components

   a. The field emission diode is mounted on the lower cover of the pressure vessel and is composed of the dome cap, insulator rings, cathode shank, cathode and anode assembly. The upper insulator isolates the dome cap and cathode shank from ground and also is the pressure interface between the pressurized capacitor stack and the evacuated chamber housing the diode. The lower section of the diode is an integral assembly easily detached from the upper section of the diode and removed from the process chamber for servicing or adjustment. Cathode-to-Anode "gap" is adjustable by inserting spacers of various thicknesses which standoff the anode assembly. In a similar manner, spacers are used to adjust the sample-to-anode distance.

C. Orbitrac Theory

The basic kinematic theory of ORBITRAC is outlined here to provide the user with a general understanding of its operation.

The function of the ORBITRAC System is to transport wafers from the end station to the Process Chamber. This is accomplished using a "walking beam" which is really a misnomer because it is not the beam (i.e. track surface) but the object being transported that "walks" along the length of the beam. This "walking beam" effect is a cyclical operation; the object being transported is actually carried along an incremental amount during each cycle of operation. See Figure 2-1 for a top view of a Y-track section.

"Walking Beam" Motion"

To understand the wafer's motion along the beam or (track surface) it is important to understand the kinematics (i.e. movement without regard to forces) of the beam itself which carries the wafer. Figure 2-2 shows an elliptical orbit that rotates in a clockwise direction. Starting at Point A the orbit moves upwards and to the right passing through Point B and then descending,

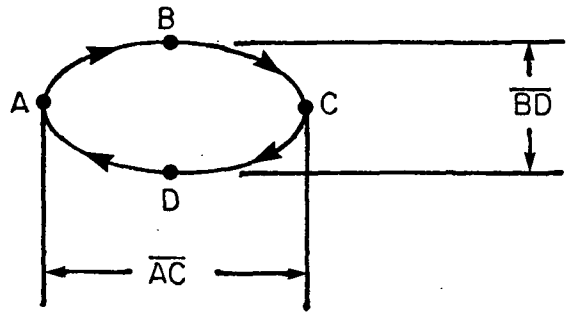


FIGURE 2-2 - ELLIPTICAL ORBIT

still to the right, to Point C; at Point C the orbit changes horizontal direction and, still descending begins to move to the left; as the orbit passes through Point D it begins to rise, still moving left until it reaches Point A. A "walking beam" follows precisely the same motion, going back and forth through Points A & C continuously, following the orbital path just described. This is the only motion of the walking beam.

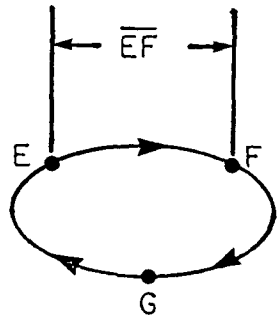


FIGURE 2-3 - BEAM ORBIT

3-Phase ORBITRAC System

A 3-phase ORBITRAC System consists of three walking beams operating at 120 degrees Phase difference to one another. Figure 2-3 shows the shape of the orbit (same as Figure 2-2) that each beam is following. As the first beam (Phase I) travels in its orbit from Point E to Point F the second beam (Phase II) is traveling from Point G to Point E and the third beam (Phase III) is traveling from Point F to Point G. This describes the relative motion of each walking beam during the first 1/3 of a full cycle. During the second 1/3 of the cycle Phase I is traveling from F to G and during the last 1/3 of the cycle Phase I is traveling from G to E, thus completing one full cycle of operation. And similarly the other two beams (Phase II & Phase III) would be completing their respective orbital paths.

The actual motion of the wafer occurs between Points E and F of each beam's orbit. During one complete cycle the wafer travels 3 EF.

Figure 2-4 shows a profile of one complete cycle in a 3-Phase System when the start of the cycle is orbitrarily chosen to begin when the Phase I beam is at Point E (See Figure 2-3) in its orbit.

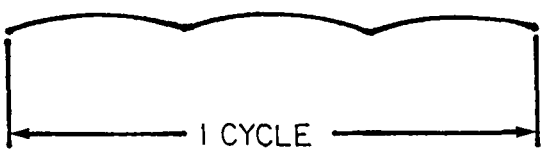


FIGURE 2-4 - PROFILE OF ONE CYCLE

Creating the ORBIT

The orbital motion of the walking beam is generated by a Module (see Figure 2-5). The Module is really the heart of the ORBITRAC System and an understanding of its kinematics is fundamental in obtaining an orbit that will optimize smooth and consistent wafer motion.

There are five basic components in a Module - a base, a center block, a top block and two flexures. The base is fixed to a mounting plate, the center block is supported thru a vertical flexure to the base, and the top block is supported thru an angled flexure to the center block.

To create the orbital motion of one walking beam a minimum of two Modules, mounted in a line on a baseplate, must be connected rigidly together in the following manner. The center blocks of each module are connected with a rigid beam called a Beam Connector; the top blocks of each Module are connected with a rigid link called a Top Connector (see Figure 2-6). Then, when any point on the center blocks or on the Beam Connector is driven by a horizontal force (ref. Figure 2-6) they will move as one unit and similarly for the top blocks and their Top Connectors.

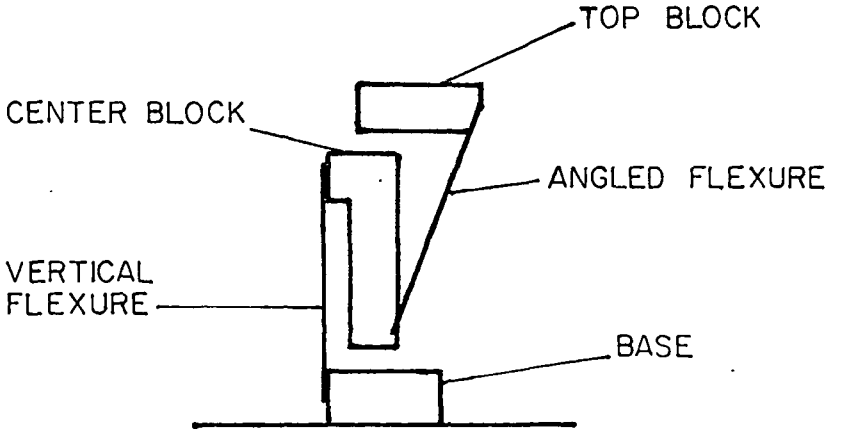


FIGURE 2-5 - MODULE - SIDE VIEW

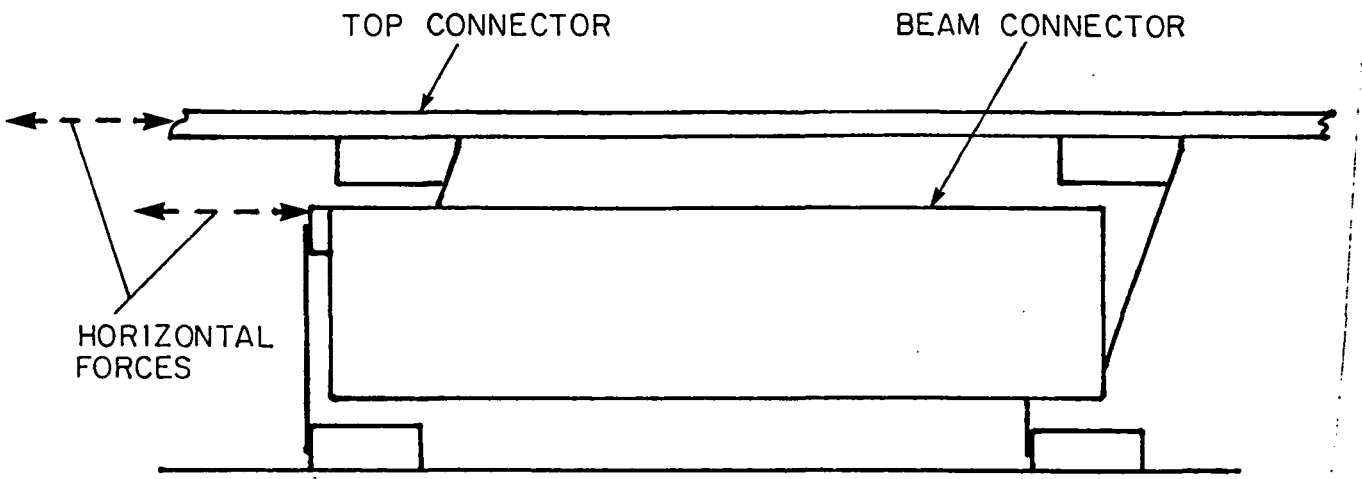


FIGURE 2-6 - MODULE CONNECTIONS

When the Modules are correctly assembled and driven horizontally back and forth with a suitable drive mechanism, the profile of the motion of each connected unit is an arc. Figure 6 shows the motion profile of a vertical flexure to which the beam (center blocks & Beam Connector) is attached. Because the Beam is supported at each end by a vertical flexure Figure 6 is also a motion profile of the entire Beam (i.e. every point on the Beam).

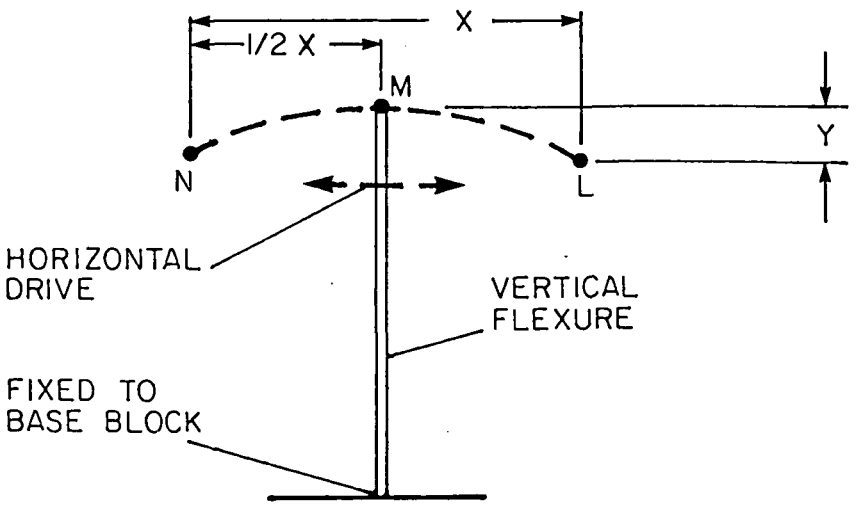


FIGURE 2-7 - BEAM MOTION RELATIVE TO BASEPLATE

Note that the vertical flexure is "flexed" an equal amount 1/2 x right and left of its unstressed (i.e. vertical) position.

This motion is a cyclical motion, i.e. the flexure is driven from Point M to Point L, back thru Point M to Point N, back thru Point M to Point L, etc. This is the only motion of the Beam (i.e. center blocks and Beam Connector).

Figure 2-8 shows the motion profile of the Track (top blocks and Top Connector) relative to its "fixed" base (the center blocks):

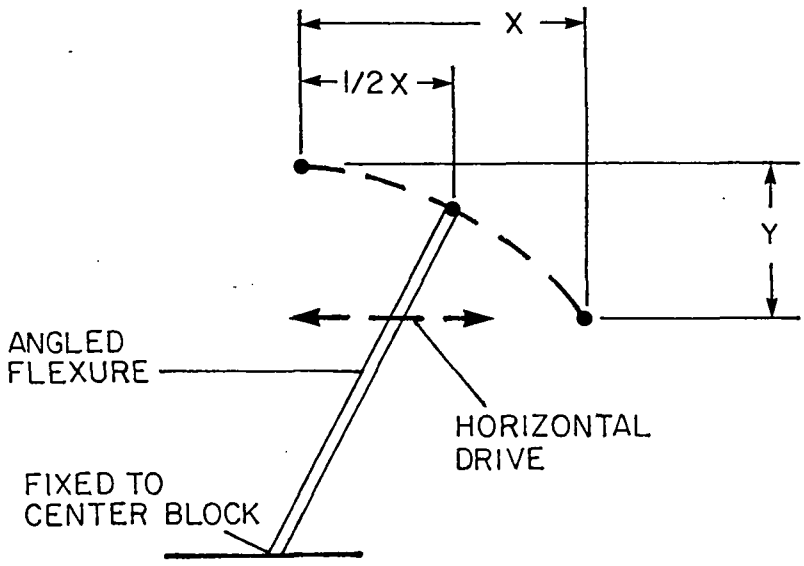


FIGURE 2-8 - TRACK MOTION RELATIVE TO CENTER BLOCK

This motion is also cyclical, similar to the Beam motion. However, it will never be observed as such because the Track motion shown in Figure 2-8 is relative to the Beam, which is also moving.

It is these two simple motions, the Beam and the Track relative to the Beam, that produce the elliptical orbit described in Figure 2-2. When the Beam and the Track are driven such that there is a Phase difference between their respective drives, the Track motion relative to the Base (on which the Modules are mounted) is an elliptical orbit whose major axis (AC in Figure 2-2) is large compared to its minor axis (BD in Figure 2-2).

Once this "walking beam" of the Track (i.e. Top Connector) has been created it can be used to transport objects without any other hardware.

III. OPERATING INSTRUCTIONS

A. Startup Procedures

1. High Voltage
   - A. Assure all controls are OFF, and high voltage assembly is grounded.
   - B. Turn on "Main Power" circuit breaker (white light comes on).
   - C. Turn on "Overload" circuit breaker.
   - D. Depress HV "ON" (red light comes on) Note: Transformer charging current may occasionally trip the main circuit breaker. This is not a fault.
   - E. Rotate "Maximum Output Voltage" control clockwise until desired voltage is reached.
   - F. At completion of test or operation, depress the HV "OFF" pushbutton. The internal output discharge assembly will rapidly drop the output to less than approximately 10kv. Being a multigap assembly, oil film gaps will not totally discharge the unit. If output control is returned to zero, and the HV "ON" and "OFF" operations are performed a few times, contact bounce will complete the discharge.
   - G. The "NO-LOAD" output voltage of this unit is capable of exceeding the safe limit. For extended life - DO NOT permit output to exceed 300kV.

2. Magnet - Hewlett Packard Power Supply.
   - A. Assure all controls are OFF, and power supply is grounded.
   - B. Turn on "Line" circuit breaker (light comes on).
   - C. Using Table 3.1 as a guide, adjust "Current" with course knob to slightly exceed your desired value.
   - D. Adjust "Voltage" with coarse knob to slightly below desired value.
   - E. Adjust with "Fine" knob to achieve desired value.

Note: A digital volt meter, when connected directly to magnet terminals, allows for very accurate adjustment.

F. Figure 3-1 maps the fringing field in the diode region.

TABLE 3.1 MAGNET CALIBRATION

V (Volts)	A (Amps)
1.28	2.0
2.56	4.0
3.86	6.0
5.22	8.0
5.52	8.5
5.85	9.0
6.17	9.5
6.47	10.0
6.79	10.5
7.12	11.0
7.44	11.5
7.76	12.0
9.03	14.0
10.30	16.0
11.63	18.0
12.90	20.0

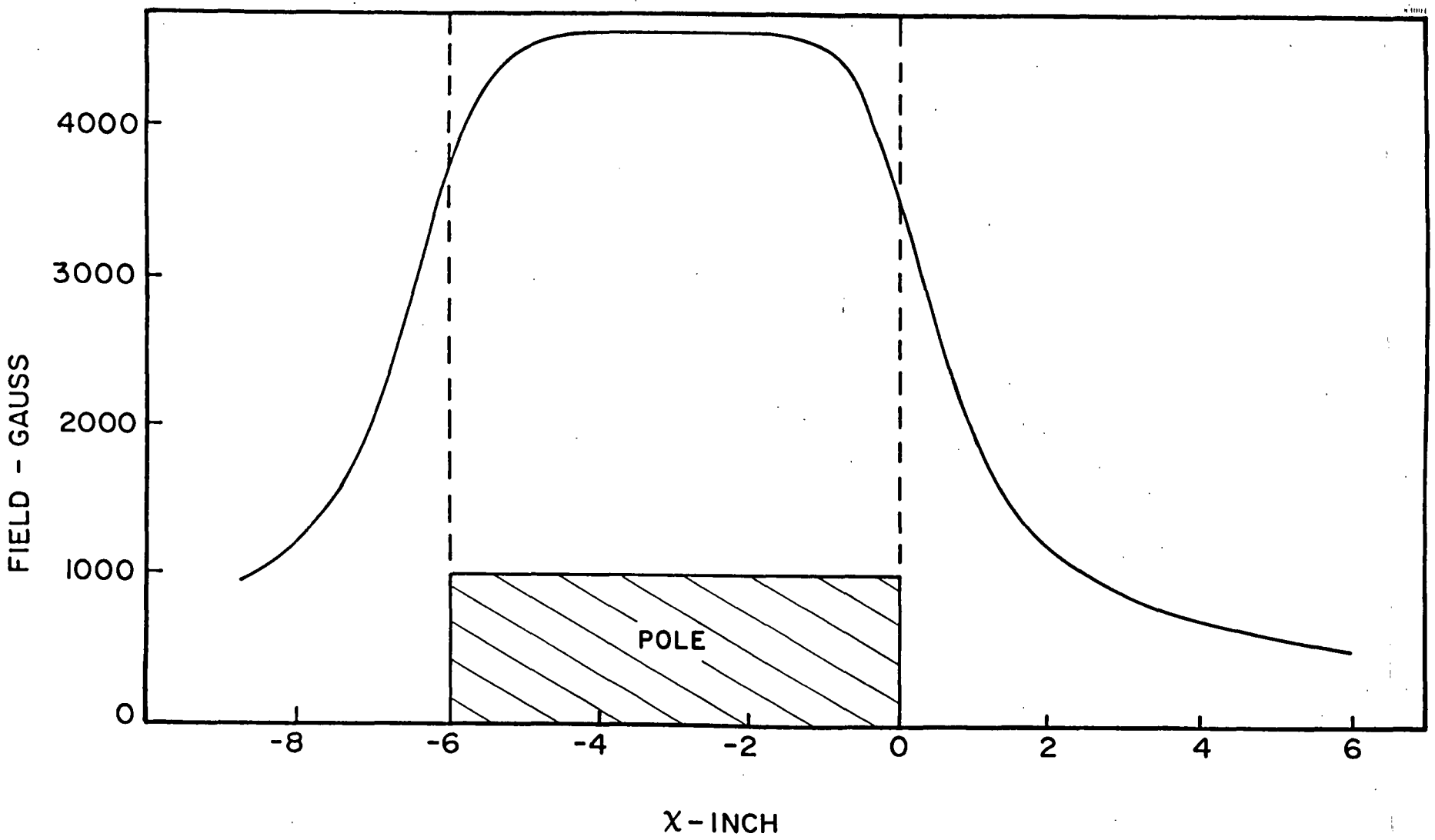


FIGURE 3.1 MAGNET FRINGING FIELD

3. Setting up Diode

I. Cathode Installaiton

a. The 4 1/2 inch round cathode is mounted with a center stud and is screwed in hand tight.

Note: Use of plastic gloves is recommended to avoid finger contact.

II. Cathode to Anode Adjustment (Gap)

a. The gap is adjustable by inserting sets of C-spacers (supplied) between the planarity adjuster and the receiver ring and tightening the receiver ring retaining screws. (See Drawing #214-0005 Section A-A)

b. The matched sets, when used with the 4 1/2 inch cathode (.375 inches thick), will provide a gap equal to the C-spacers thickness.

III. Anode Installation

a. Anode material should be cut into a 10 inch circle.

Note: material should be non-magnetic.

b. Secure the anode screen between the anode rings with the supplied screws, alternating short and long.

c. Place anode and ring unit into bayonet ring and secure with supplied hex nuts.

IV. Anode to Sample Adjustment (Distance).

a. Matching sets of copper spacers (supplied) may be attached to the bottom side of the anode bayonet ring to adjust distance.

b. Spacer thickness and resulting distance are as follows:

.022"	.014"
.040"	.032"
.080"	.072"
.118"	.110"
.156"	.148"

Note: Resulting distance assumes using a .012" thick sample.

V. Anode Assembly Installation

a. The entire anode and bayonet ring assembly is now attached to the receiver ring using the bayonet mounting screws.

b. The anode and bayonet ring assembly can be removed by rotating due to the action of the bayonet ring mounting screws.

Note: Removal of the Bayonet ring mounting screws is not recommended.

B. System Software

1. Software Modules - The Spire 7000 Control Software consists of the following elements:

a. A RAM based program written in "Basic".

b. Rockwell "Basic" interpretor contained in two ROMS located at Hex B000 to CFFF.

c. Rockwell Aim 65 Monitor contained in two ROMS located at Hex E000 to FFFF.

2. System I/O

a. The system software comunicates with hardware through memory mapped I/O, therefore individual elements (motors, solenoids, etc.) are controlled by setting (turning on) or clearing (turning off) binary bits in a register addressed as a memory location. Similarly, inputs to the system appear as binary bits ON (high) or OFF (low), when the appropriate memory addresses are read.

b. Whenever possible, 'Cause-Effect' functions have been located at the same bit position in the corresponding input and output register; for example, bit position 1 of register N (output) may open a solenoid valve and bit position 1 of register N + 1 (input) would be the set point of the gauge monitoring the pressure associated with those solenoids. Note, also that the hardware addresses output registers as 'Base Address' and the corresponding input register as 'Base + 1'.

3. Operating Procedure - The following describes the procedure for general operation of system software.

   a. Upon power up or reset, the monitor program clears all registers and utilizes the CPU I/O ports for keyboard/display operation. In this mode, the assembly language programming and memory content manipulation are available.

   b. The applications program is loaded as follows: Activate the basic interpretor by depressing "5" on the keyboard. Respond to all prompts by depressing "Return" key (CR). This initializes memory locations and pointers.

      The "Basic" load instruction can now be executed by typing "LOAD" (CR) and using the file name "SPIRE". The sequence is as follows; system prompts are shown and user responsibilities are underlined.

      AIM 65 BASIC VI.O*
      (CONTROL/PRINT)
      OFF (LOAD (CR)
      In = T F = SPIRE T = 1

      * Important: Depress "CONTROL" and "PRINT" keys simultaneously to turn off printer before loading program.

      When the tape is loaded, the system will respond with " ". The applications program can now be run.

      When running the applications program, note that the program must be run at least once to initialize certain hardware functions before the "BASIC" immediate mode can be used. The command mode may be entered at any time by depressing (CR) without enterdata or depressing the (F1) key. To initiate program execution, type in the following dialogue:

RUN (CR)
CHANGE VARIABLES? N(CR)
RUN OR TEST? R(CR)

The program will now take over and automatically check end station vacuum. When vacuum setpoints are satisfied, microprocessor will prompt as follows:

"HOW MANY WAFERS"?

Any integer responce will satisfy this prompt which is followed by:

"READY TO TRANSFER"?

A "Y" (CR) response will initiate wafer processing.
Note: To run wafers in this automatic mode without the stop, lifter or pulser operational, type T(CR) when computer asks "READY TO TRANSFER"?

C. Cassette Loading/Unloading

1. Wafer Loading
   a. Wafers are to be loaded onto the carbon/aluminum wafer carriers using proper wafer handling techniques.

2. Cassette Loading
   a. Loaded wafer carriers should be placed in "input" cassette from top to bottom.
   b. Place loaded input cassette on input end station and secure with cam-lock lever.
   c. This will activate a computer read switch which initiates wafer processing.

3. Wafer Processing (Automated)
   a. End station pusher bar will batch transfer wafers from external input cassette to internal input cassette.
   b. Vacuum sealing door closes activating switch.

c. Pumpdown begins.
d. Cassette indexing (vertical motion) is monitored by infrared sensors with a comb structure.
e. Cassette indexing is driven by hydraulic action.

4. Cassette Unloading
a. Unloading procedures begin after run is complete.
b. Output end station sealing door opens.
c. Internal wafer pusher bar batch transfers wafers from internal cassette to external cassette.
d. Cam-lock lever is released and external cassette is removed.
e. Wafer carriers are removed from cassette.
f. Wafers are removed from carriers using proper wafer handling techniques.

D. Trigger and Vacuum Controls

1. Trigger Panel
a. Turn unit on.
b. Charging voltgage is displayed by digital readout.
c. For automatic operation, auto trigger thumbwheel is set at desired voltage.
d. For manual operation, auto trigger thumbwheel is not operational.
e. Auto/manual button must be set for appropriate operation (light will designate mode).
f. Trigger button operates only under manual conditions.
g. Cumulative shot number is displayed at anneal cycle readout.

2. Vacuum Gauge Controller (see Granville - Phillips Instruction manual #270013)
a. Turn power on.
b. Unit is computer controlled for automatic wafer processing.
c. Following description included for manual operation only:

TC#1 SET - recessed pot for adjusting the set point where the TC#1 process relay energizes.
TC#1 ZERO - recessed pot for adjusting the TC#1 zero
TC Select Switch - selects which TC output is displayed on the meter.

Degas Switch - switches the degas power to the gauge tube grid.
PC Set - recessed pot for adjusting the set point corresponding to decade and meter reading where the IG process relay energizes.

Filament Switch - Three position switch that controls filoment status:

1. Auto on (down) control of the filament is by use of the TC#2 process set point.
2. Center - Intermediate position.
3. On/Off (up)- spring loaded position which reverses filament state each time toggled.

Emission Switch - Spring loaded switch that, in the adjust position, displays a reading corresponding to the emission current on the ion gauge meter.
Emission Adjust - recessed pot used to adjust the emission current to the recommended value depending upon gauge tube sensitivity.
Decade Lights - indicates pressure decade.
Range Switch - Selects pressure decade during manual operation.
Autorange Switch - selects mode of operation of autoranging circuit.

3. End Station Reset Panel (Below Microprocessor Keyboard)
   a. Reset switch allows end stations to be cleared (down) and reset (up) if processing run involves fewer than 50 wafers.
   b. Automatic operation will resume after "Reset", with venting and pusher bar action transferring wafers to external cassette for removal.

E. Manual Computer Commands

1. Operating in the "Test" or "Manual" Mode -
   a. Note, that typing "E" for exit in response to any prompt will return the program to the previous level and prompt.
   b. Test function codes are as follows: (codes may be added to select several functions simultaneously).

Test 1.

Valve No.	Open	Close
V1 (input)	1	2
V2 (output)	16	32
ALL	17	34

Test 2.

	UP	DOWN
Lift 1	1	2
Stop 2	1	2
Gate 3	1(left)	2(right)

Test 3.

Main Track	4
Entry Track	16
Exit Track	128

Test 4.

Solenoid	Pump	Vent
Chamber (rough)	4	32
High Vacuum	253(open)	221(close)

Test 6 - To enable the end stations for manual operation, type "9" CR followed by "51" CR.

2. Reset Switch (Red Button)
   a. Depressing at any time will stop all operations and bring machine to a "safe" state (valves closed).

F. Verification of Proper Operation

1. Indexing of End Stations
   a. Computer controlled indexing of the input end station, will deposit wafers to the Orbitrack Transport System. Wafers are removed from the internal input cassette starting at the bottom and continuing for 50 indexing cycles. Failure of the indexing system will terminate vertical motion and therefore prevent further processing of wafers.

   b. The Internal Output cassette starts filling from the top and continues for 50 wafer output cycles. Failure to properly index (accept wafer), will result in a wafer "log-jam" on the transport system. Should this happen, the processing run should be immediately terminated by depressing the red "Program Escape" button on the microprocessor keyboard. Wafers should then be removed manually (at air), and the end station indexing system alignment should be checked. (see section 4.).

2. Transport System
   a. The drive assembly provides all forces and motion required to produce the orbital motion of the 3-phase track. It consists of a 24 VDC motor, belt-driven keyed shaft (for 120° phasing of three phases), three eccentrically mounted ball bearings, and three bellows assemblies to transfer motion from atmosphere into vacuum.
   b. Track motion and BAI valve operation is simultaneously initiated by microprocessor command. This occurs after both end stations are pumped down to specified set points.

c. End station indexing will "deposit" a wafer onto the track system.

d. A fiber optic sensor located at the end station allows the computer to see that the "deposited" wafer is now cleared, and another indexing cycle begins.

e. The "output" end station also has a fiber optic sensor which allows indexing only when wafers are safely cleared (in the cassette).

3. Stop and Lifter Mechanisms

a. The stop mechanism is a simple pivoting device, air driven externally through a bellows to produce an approximate .090" movement up and down, and is electrically isolated to act as a switch closure when "bumped" by a moving wafer (carrier). In its "up" position the stop is elevated .060" above the plane of the Y-Track and prevents passage of a wafer beyond the stop until it is lowered and out of the way. In its "down" position, the stop is .030" below the plane of wafer motion and provides no obstruction to passage of the wafer.

b. The lifter mechanism is activated by the microprocessor which receives a signal from the stop. The air driven lifter raises the wafer to the "firing" position by contacting the copper spacers of the anode bayonet ring. (These spacers are used to adjust Anode to sample distance as discussed in section 3.3.IV).

Note: To run wafers in automatic mode without stop or lifter operational, type T(CR) when computer asks "READY TO TRANSFER".

G. Beam Diagnostics

A. The parameters required to achieve the best anneal of a 4 inch wafer are:

CATH. = 4 1/2 In.

Anode = 8"w-30 In. (w for tungsten)

Gap = .098 In.

Dist. = .306 In.

Pres. = 2×10^{-5} Torr

I_{mag} = 8.0 amps.

V_o(cond) = 100 kV

V_o (sample) = 170 kV

Explanation: Cathode - 4 1/2 Inch diameter X .375 inches thick made of POCO Graphite.

Anode - 10 inch diameter tungsten mesh (99.95% pure) 30 wires per inch of .004" diameter.

Gap - achieved by using the .039" and .059" C-Spacers together.

Distance - achieved by using the .156", .118" and .040" copper spacers together. Note: geometrical correction factor of (-.008") must be added to the spacers to achieve the correct distance. (Example: .156 + .040 - .008 = .306").

Pressure - Processing chamber pressure of 2×10^{-5} Torr or better is required to initiate wafer processing.

I_{mag} - The current through the magnet = 8.0 amps.

V_o (cond.) - Conditioning shots on empty wafer carriers are required after the process chamber is pumped down. This "conditioning" process will pulse clean the cathode by removing any contaminants (water vapor, etc.), which are introduced by opening the process chamber to atmosphere. Conditioning shots are done at 100 kV (all other parameters as noted) and are repeated at least 6 times.

V_o (sample) - The voltage required for a proper anneal of a 4-inch Silicon wafer when the other parameters are followed.

NOTE: Refer to report - DP-10073-01 (Summary of Sheet Resistivity Mapping of Pulse Electron Beam Annealed Wafers and performance Evaluation of Solar Cells).

H. Wafer Appearance After Anneal

1. Visual Uniformity.
   a. Since annealing is employed to repair the crystal structure damage caused by Ion Implantation, the different reflective characteristics of an amorphous (implanted) surface vs. an annealed (repaired crystal structure) is used to visually see if uniformity exists.
   b. The color of an annealed wafer should be highly uniform. Spotty regions indicate "under-anneal", and pin-point marks or a hazy appearance are signs of an "over-anneal".

IV MAINTENANCE

A. Assembly/Disassembly (See Drawing #214-0002)

1. Energy Store Tank
   a. The tank is pressurized/depressurized through the manifold assembly.
   b. Gas pressure for proper operation is 100 psi, (60% N_2 and 40% CO_2).
   c. Tank pumpdown is achieved by opening the manifold valve and allowing gas to escape. NOTE: It is recommended that an externally vented exhaust line be attached to the manifold.
   d. The tank may be opened by removing the 48 bolts on the lower flange. The upper flange is not loosened.
   e. There is a woven mesh that is placed between the flanges; this must be replaced during reassembly to achieve a properly grounded system.

2. High-Voltage Cable Feedthrough
   a. Assure that High-Voltage Power Supply is turned off.
   b. Cable is unbolted from top of energy store tank and removed.
   c. A properly grounded strap should now be used to "short" any residual charge still on the lines. This is achieved by dropping the strap through the H.V. cable opening.
   d. A short (13") extension cable is used to connect the High Voltage cable to the liners. (actually, it is connected to a high voltage resistor which is in turn connected to the liner network). This cable can now be removed.

3. Trigger Mechanism
   a. Trigger action is electropneumatically controlled and air driven. (An external source of N_2 gas at 110 psi is used).
   b. The N_2 supply should be removed.
   c. Remove the 12" diameter blank-off plate on top of the energy store tank.
   d. The Trigger N_2 source/exhaust line feedthrough, is loosened and dropped into the store tank unit.

4. Tank Removal - With the completion of steps 1-2 we can now completely remove the energy store tank from the machine.
   a. Anchor the 4 I-Beam legs to the floor.
   b. Attach the overhead crane to the four U-bolts on top of the tank.
   c. Tank can now be raised and set on the anchored legs.

5. Capacitor Stack Assembly Removal
   a. Remove the 8 recessed socket head bolts from the lower tank flange. This releases the capacitor stack assembly from the tank unit. NOTE: There is a woven mesh between the tank flange and the capacitor support plate which is used for grounding purposes.
   b. The tank unit can be carefully raised with the crane and placed back on the main machine for safe storage.

6. Liner Removal
    a. Remove the terminal assembly cover.
    b. Remove the six screws of the trigger retaining ring (copper).
    c. Remove the end plate for the liner you wish to remove.
    d. The storage line socket ring should be carefully removed. NOTE: finger stock might "spring" out. (See Drawing #214-0002 Detail A).
    e. The Hex-Ring which holds the liner in place at the top of the "stack" should now be removed.
    f. The liner can now be removed with use of the overhead crane. (See Drawing #214-7130). NOTE: Exercise extreme caution so not to mark sides of liner.

7. Load Resistor Removal (See Drawing #214-0011)
    a. Unscrew the 4 Oval-Head screws being careful not to drop them inside liner.
    b. Resistor can then be lifted out by either crane or by hand.

8. Reassembly/Pumpdown
    a. This is best achieved by assembling in the reverse order of disassembly, using the previous steps as your guide.
    b. Pumpdown is started after all systems are reassembled.
    c. NOTE: It is a good check of the electrical system to now charge the system to 40kv. If no discharge occurs, system is OK.
    d. Turn voltage off.
    e. Check that vacuum in the process chamber is on the Hi-Vac scale. CAUTION: Failure to have vacuum in the process chamber could result in fracture of the diode insulating rings.
    f. Attach a roughing pump using flexible rubber tubing to the manifold and initiate pumping.
    g. A 24-hour pumping period is recommended and a vacuum of less than 100 microns should be achieved.
    h. Poor vacuum could be corrected by cleaning and regreasing O-Rings and gaskets.
    i. After proper vacuum is achieved, backfill tank to 100 psi with 60% N_2 and 40% CO_2 and allow system to stabilize.

9. Diode System (See Drawing #214-0005, Section A-A)
    a. Can be removed as discussed in section 3.3.

10. Transport System
    a. Removal of the process chamber transport system is achieved by:
        1. Removing Output end station.
        2. Removing screws on the "output" side of the process chamber end plate.
        3. Removing the three bolts that hold the lower magnet pole in place (inside process chamber).
        4. Removing transport system while someone "jockeys" magnet pole out of position. NOTE: Removal of diode assembly might aid in in transport system removal.
    b. Any adjustments or operational information can be found in Section 4 of the Spire Y-Track Operator/Maintenance Manual.

11. Vacuum System - See Appropriate Manufacturer's Manual
    a. Roughing Pumps - Oil should be changed as recommended by pump manufacturer.
    b. Cryopump - Absorber unit must be replaced at 10,000 hrs. as recommended in the CTI-Cryogenics Manual.
    c. Cryopump Gate Valve - maintenance as required in manufacturer's Instruction Manual.
    d. BAI-Valves - O ring seals can be cleaned with a cotton swab.

12. End Station Alignment
    a. Proper alignment will have a "downward cascade" effect at points of transfer.
    b. Input End Station is aligned by first checking the internal cassette to track transfer action. Internal cassette height adjustments can be made by inserting shims between top of cassette and the bellows flange.
    c. External to internal cassette adjustment is achieved by "shiming" the 4 rectangular "legs" of the external cassette platform.

d. Output End Station is adjusted using Input End procedures. NOTE: actual use of a wafer carrier to check adjustments is recommended.

e. If the transport system cannot "pickup" or "deposit" a wafer at the end stations, an alignment is needed.

APPENDIX 3
LAYOUT DRAWINGS OF ION IMPLANTER

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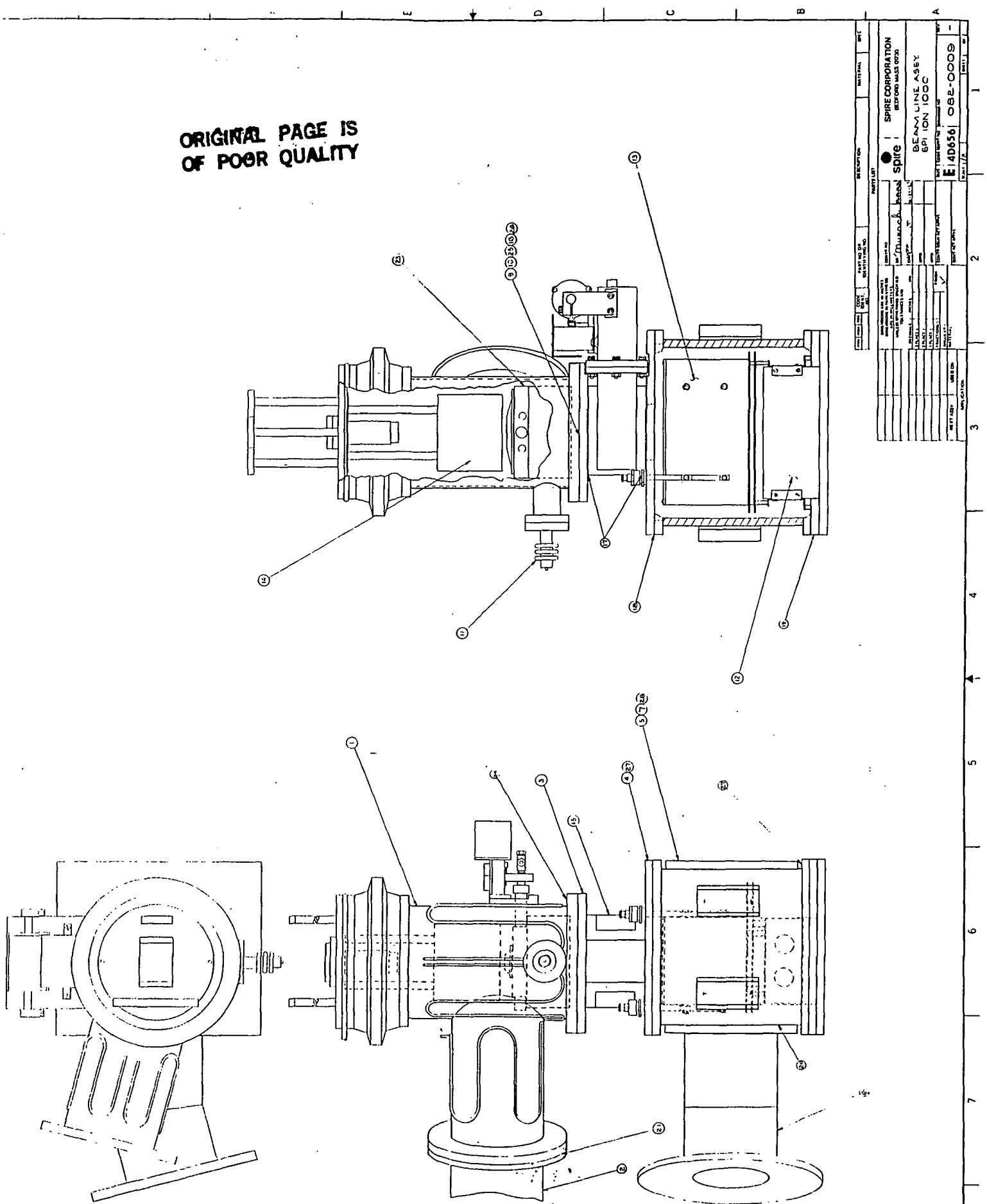

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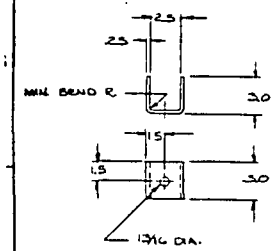

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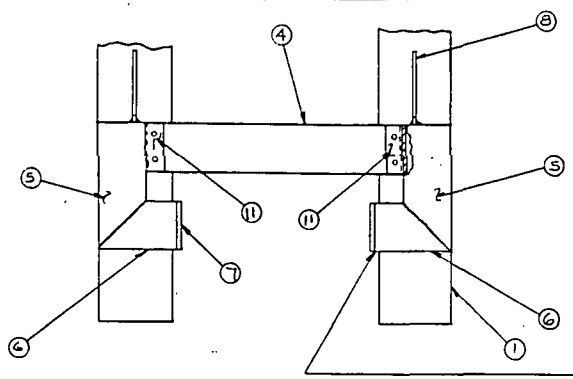

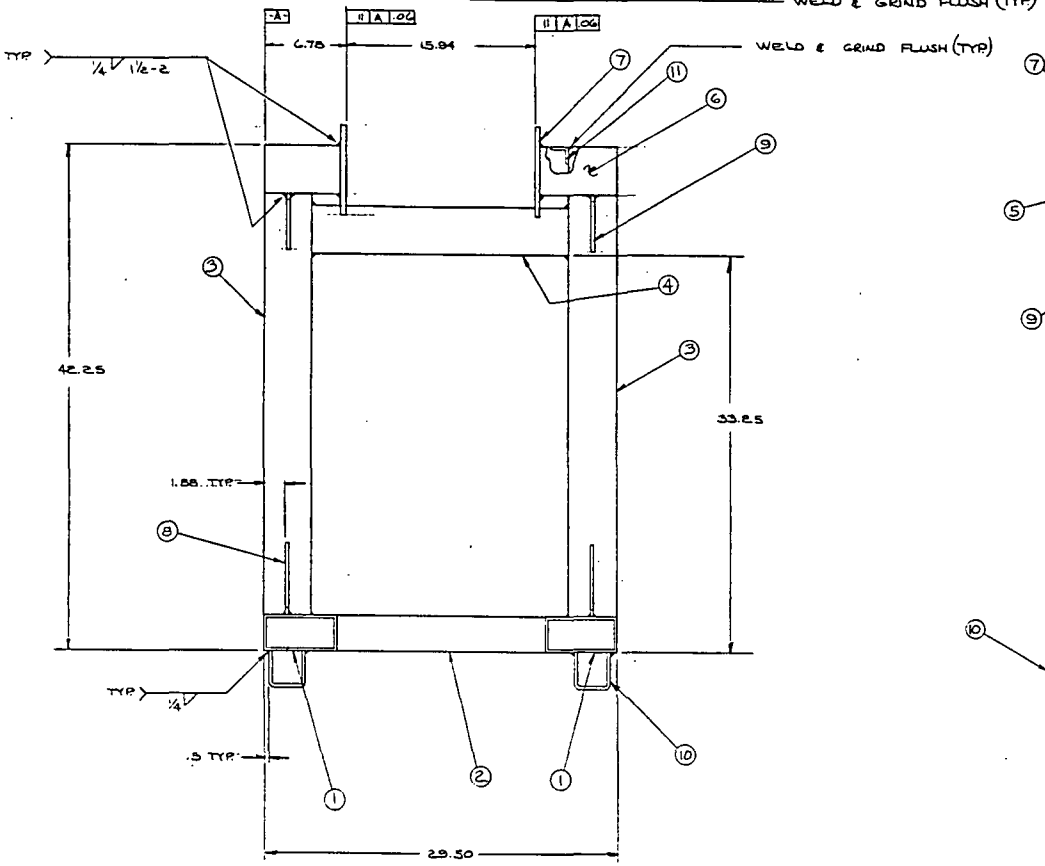

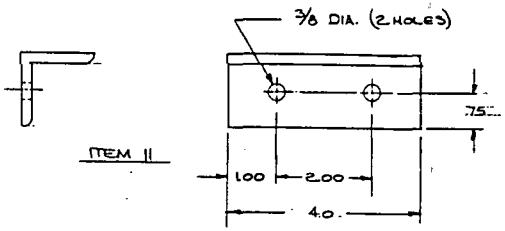

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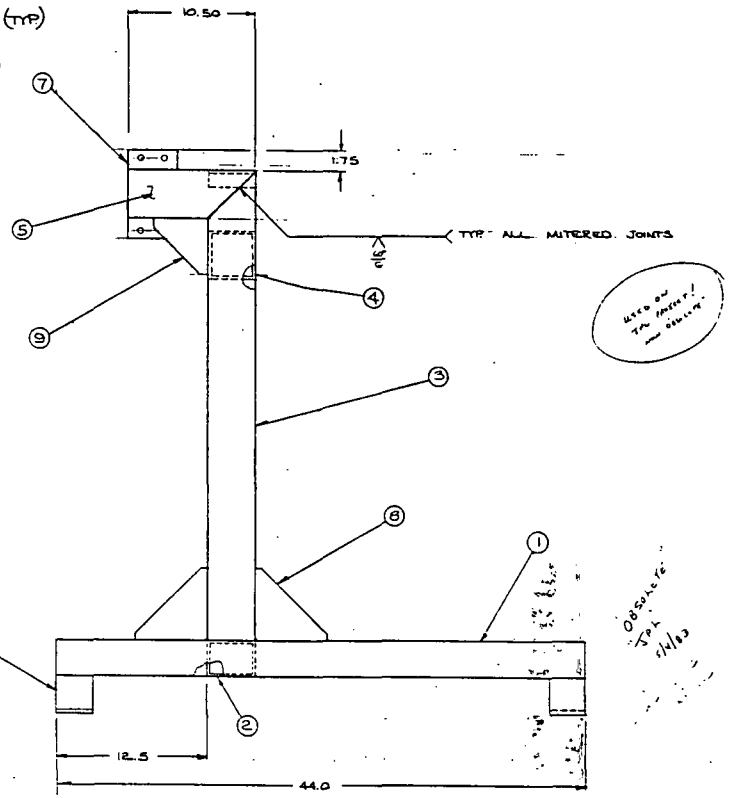

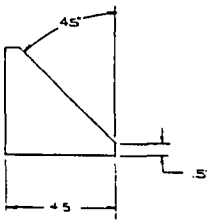

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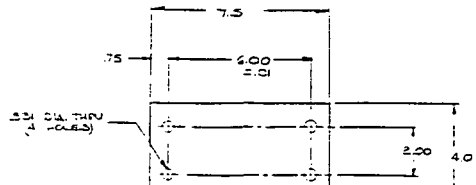

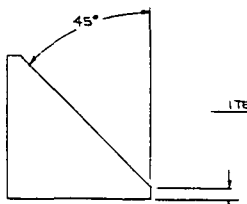

ITEM 8

11	2	1½ x 1½ x 3/16 ANGLE HRS	
10	4	¼ THK HRS A36 AS REQ'D	
9	2	5.0 X 5.0 X .25 THK HRS	PLATE A36
8	4	6.5 X 6.5 X .25 THK HRS	PLATE A36
7	2	7.5 X 4.00 X .50 THK HRS	PLATE A36
6	2	4 X 4 X .188 WALL X 6.28 LG HRS	SQ. STRUCT. TUBING ASTM-A500
5	2	4 X 4 X .188 WALL X 10.50 LG HRS	SQ. STRUCT. TUBING ASTM-A500
4	1	4 X 4 X .188 WALL X 21.50 LG HRS	SQ. STRUCT. TUBING ASTM-A500
3	2	4 X 4 X .188 WALL X 39.25 LG HRS	SQ. STRUCT. TUBING ASTM-A500
2	1	6 X 3 X .188 WALL X 17.50 LG HRS	RECT. STRUCT. TUBING ASTM-A500
1	2	6 X 3 X .188 WALL X 44 LG HRS	RECT. STRUCT. TUBING ASTM-A500

ITEM NO.	QUANT.	PART NO OR IDENTIFYING NO	DESCRIPTION	MATERIAL	SPEC

PARTS LIST

SPIRE CORPORATION
BEDFORD MASS 01730

ION IMPLANTER FRAME

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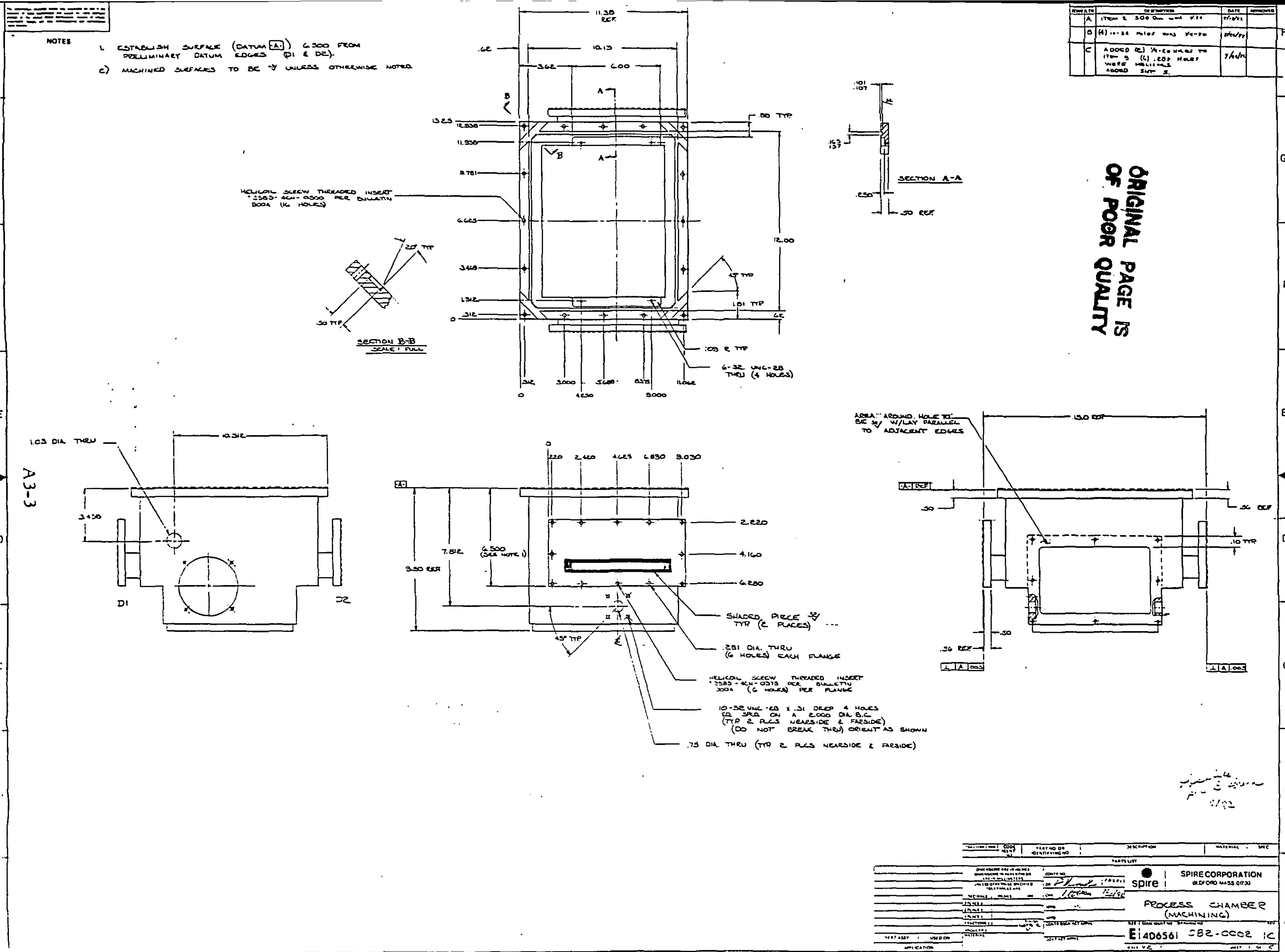

NOTES
1. ESTABLISH SURFACE (DATUM -A-) 6.300 FROM PRELIMINARY DATUM EDGES (D1 & D2).
2) MACHINED SURFACES TO BE 32/ UNLESS OTHERWISE NOTED.
A ITEM 2 .500 ...
B (4) 10-32 HOLES WAS 1/4-20
C ADDED (2) 1/4-20 HOLES TO ITEM 5 (4) .203 HOLES WERE HELICOILS ADDED SHT 3.
11.38 REF
10.13
3.62
6.00
.62
.80 TYP
12.00
45° TYP
1.81 TYP
.03 R TYP
6-32 UNC-2B THRU (4 HOLES)
HELICOIL SCREW THREADED INSERT *3585-4CN-0500 PER BULLETIN 300A (16 HOLES)
20° TYP
.30 TYP
SECTION B-B
SCALE: FULL
SECTION A-A
.50 REF
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1.03 DIA. THRU
10.312
3.430
D1
D2
7.812
6.500 (SEE NOTE 1)
9.30 REF
45° TYP
SHADED PIECE 32/ TYP (2 PLACES)
.281 DIA. THRU (6 HOLES) EACH FLANGE
HELICOIL SCREW THREADED INSERT *3585-4CN-0375 PER BULLETIN 300A (6 HOLES) PER FLANGE
10-32 UNC-2B X .31 DEEP 4 HOLES EQ. SPA. ON A 2.000 DIA. B.C. (TYP 2 PLCS NEARSIDE & FARSIDE) (DO NOT BREAK THRU) ORIENT AS SHOWN
.75 DIA. THRU (TYP 2 PLCS NEARSIDE & FARSIDE)
AREA AROUND HOLE TO BE 32/ W/LAY PARALLEL TO ADJACENT EDGES
15.0 REF
.56 REF
.10 TYP
SPIRE CORPORATION
BEDFORD MASS 01730
PROCESS CHAMBER (MACHINING)
E 4D6561 382-0002 1C

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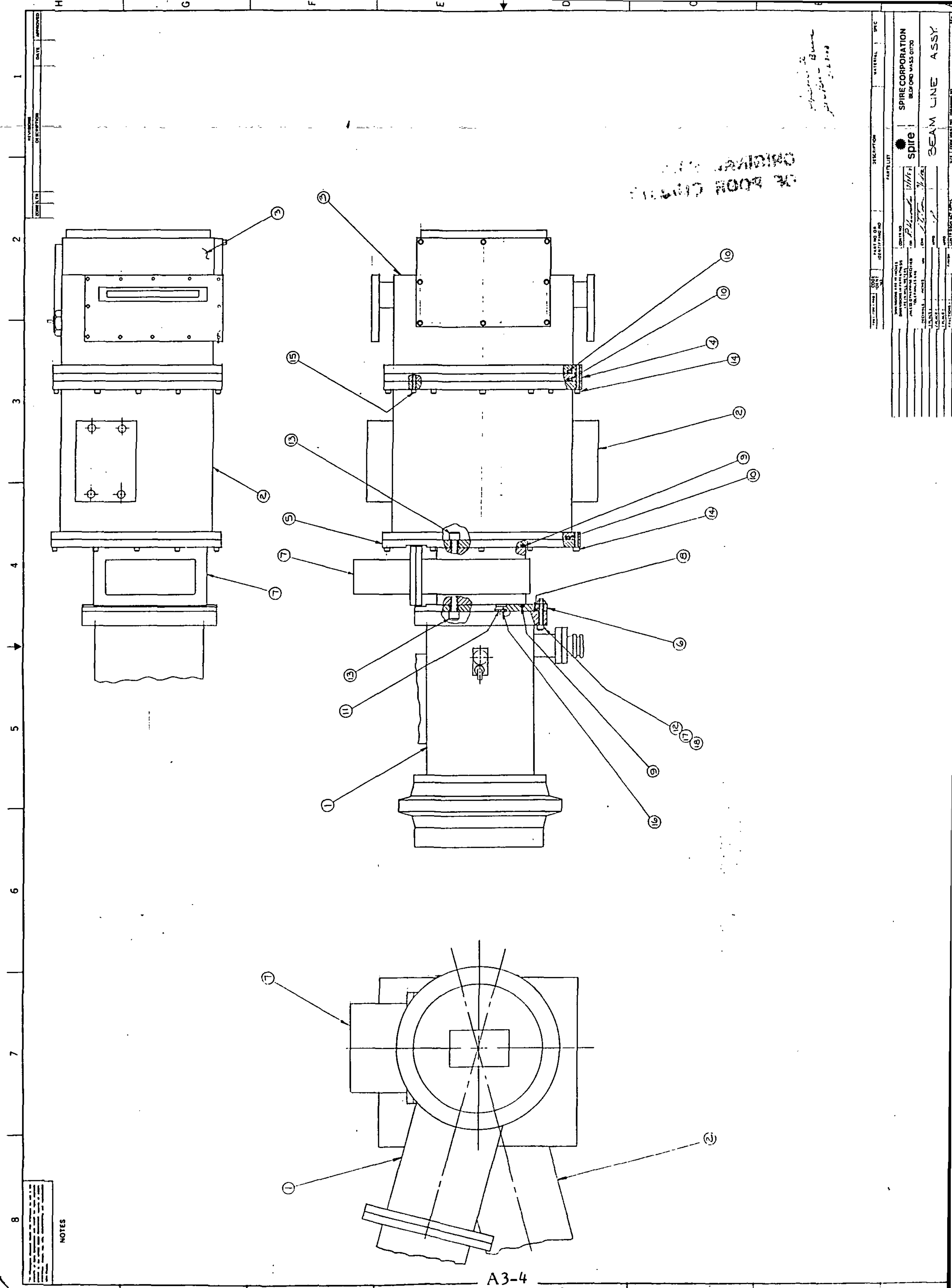
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BEAM LINE ASSY
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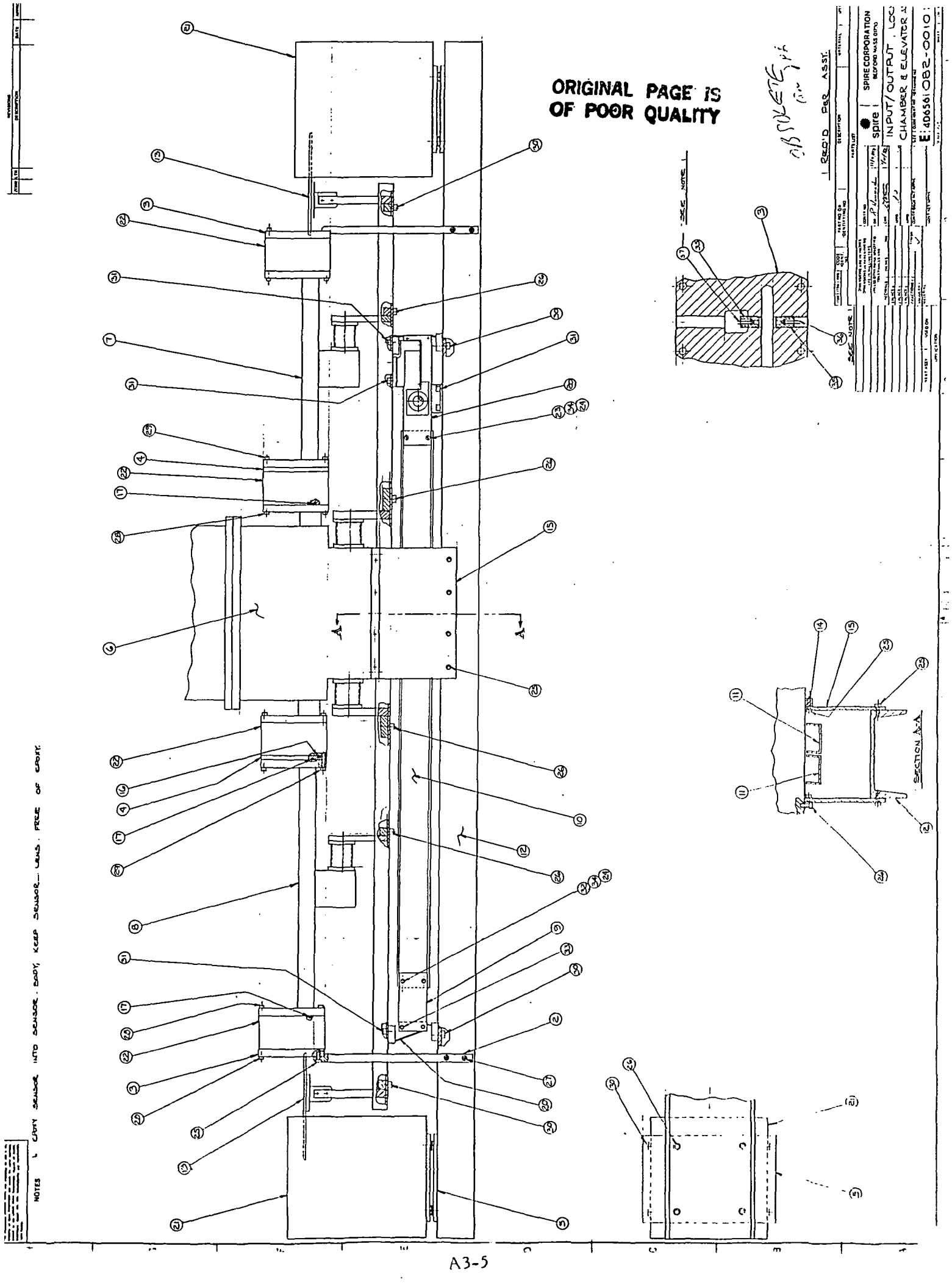
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CHAMBER & ELEVATOR
SECTION A-A
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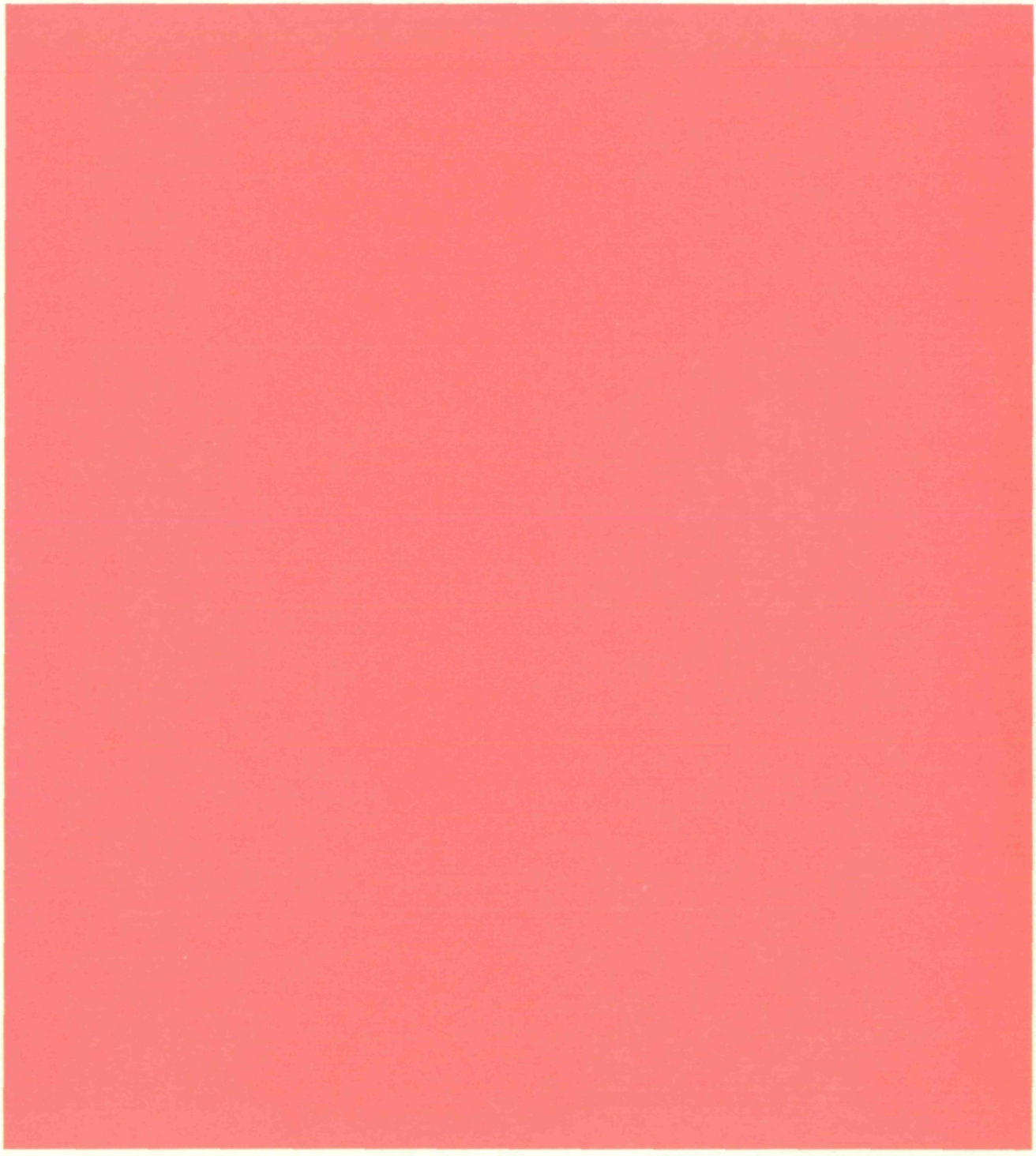

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