TDRSS S-SHUTTLE UNIQUE RECEIVER EQUIPMENT

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ABSTRACT

Beginning with STS-9, the Tracking and Data Relay Satellite System (TDRSS) will start providing S- and Ku-band communications and tracking support to the Space Shuttle and its payloads. The most significant element of this support takes place at the TDRSS White Sands Ground Terminal, which processes the Shuttle return link S- and Ku-band signals. While Ku-band hardware available to other TDRSS users is also applied to Ku-Shuttle, stringent S-Shuttle link margins have precluded the application of the standard TDRSS S-band processing equipment to S-Shuttle. It was therefore found necessary to develop a unique S-Shuttle Receiver that embodies state-of-the-art digital technology and processing techniques. This receiver, developed by Motorola, Inc., enhances link margins by 1.5 dB relative to the standard S-band equipment and its bit error rate performance is within a few tenths of a dB of theory. The goal of this paper is to provide an overview description of the SSRE, which includes the presentation of block diagrams and salient design features. Selected, measured performance results are also presented.

1. INTRODUCTION

Beginning with STS-9 the Tracking and Data Relay Satellite System (TDRSS) will start providing communications and tracking support to the Space Shuttle and its payloads under a broad range of operating conditions and data throughput requirements. Such support will take place at both S- and Ku-band frequencies, under forward (JSC-to-Shuttle) and return (Shuttle-to-JSC) link conditions, during launch (S-band only) and, of course, during in-orbit operation.

To support forward link operation the TDRSS ground terminal at White Sands, New Mexico (WSGT) will act as a ground relay between JSC and the TDRS-Shuttle link. At WSGT, necessary processing such as PN spreading, data format conversion, doppler compensation, and baseband-to-RF conversion is performed. No other data-related processing is performed at WSGT and the TDRS satellite further acts as a bent pipe repeater between WSGT and Shuttle. Figure 1 highlights salient interfaces between JSC, Shuttle and the TDRSS, while Figure 2 amplifies on TDRSS Ground Network support to Shuttle operations.

The most significant communications and tracking support provided by the TDRSS to Shuttle takes place at WSGT in the processing of return link S- and Ku-band signals. Here, WSGT receiver hardware performs demodulation, symbol synchronization and data detection (coded and uncoded), and relays the detected data via NASCOM to JSC. Additional return link processing at WSGT involves doppler tracking, phase ambiguity resolution and closed-loop autotracking of the TDRS Ku-band antenna in the direction of Shuttle.

To support Ku-Shuttle return link operation, WSGT receiver hardware that is available to other TDRSS Ku-band Single Access (KSA) users is uniquely configured to handle the Shuttle 3-channel modulation schemes. This involves appropriate application of the KSA High and Medium Rate Demodulators and Symbol Synchronizers, and a multiplexed set of Viterbi decoders to handle coded data rates up to 50 Mbps.

For S-Shuttle return link operation the originally planned TDRSS support also called for the application of WSGT receiver hardware available to other TDRSS S-band Single Access (SSA) users. Due to stringent Shuttle link budget considerations, however, the link margins available via the standard SSA equipment were found to be insufficient, and it was found necessary to develop a unique S-Shuttle receiver that embodies state-of-the-art digital technology and processing techniques. The uniqueness of this S-Shuttle Receiver Equipment (SSRE), developed by Motorola, Inc., may be highlighted by several significant features:

- all-digital processing after IF-to-baseband conversion
- integrated carrier loop/symbol sync design
- link margin enhanced by 1.5 dB relative to existing SSA equipment
- bit error rate performance within a few tenths of a dB of theory

The SSRE represents an important achievement in the development of state-of-the-art digital hardware that implements near-optimal communication signal processors. It also serves as a benchmark for future hardware research and development to be undertaken by NASA in support of TDRSS operations over the next decade, and for on-going support during the post-TDRSS era.

The goal of this paper is to provide an overview description of the SSRE, involving the presentation of block diagrams and salient design features. Selected, measured performance results are also presented. Toward this end Section 2 begins with a summary of S-Shuttle signal characteristics that must be supported by the SSRE and is followed in Section 3 by an overview of the SSRE and associated interfaces. Section 4 proceeds to focus on several of the SSRE components, highlighting their specific functions and significant features. Selected results are presented in Section 5 and conclusions are contained in

2. TDRSS/S-SHUTTLE RETURN LINK SIGNAL CHARACTERISTICS AND OPERATIONS CONSIDERATIONS

Salient S-Shuttle return link signal characteristics are as follows:

- BPSK modulation
- Data Rate
  - Mode 1: 96 KBPS
  - Mode 2: 192 KBPS
  - Mode 3: Unmodulated Carrier
- Coding
  - Convolutional
  - Rate 1/3, constraint length 7
  - Non-transparent
- Signal Format
  - Bi-ϕ (Manchester)

From an operational viewpoint three additional aspects that warrant mentioning in this context are:

- signal dynamics
- antenna switching transients
- degraded signal level

Under normal conditions, S-Shuttle will operate in a coherent turnaround mode, which implies that the uncompensated doppler at the SSRE input can exceed 130 KHz; typically, however, doppler compensation will reduce residual doppler to well below this value. This doppler value may be significant during signal acquisition, since under certain conditions a large doppler offset may lead to false carrier lock.

Antenna switching transients must also be contended with. In particular, S-Shuttle employs one of four quad antennas at a time, and when switching from one antenna to the next takes place, a brief signal drooout occurs (e.g., $\leq$ 50 ms). While data bits will, of course, be lost during the antenna switch, it is imperative that the SSRE demodulator stay in lock or recover quickly after the antenna switching process is complete.

A third operational aspect of importance involves S-Shuttle operation under degraded EIRP conditions. To compensate for this contingency both of the TDRS SSA antennas may be used simultaneously to relay Shuttle signals to WSGT, where they may be appropriately combined to provide up to 2.5 dB SNR enhancement.

It is clear from the above discussion that the SSRE must handle three distinct data modulation modes and simultaneously contend with a variety of other signal and channel conditions. SSRE design features and selected performance results, and how they relate to the above discussion, are treated in the sections that follow.

3. SSRE OVERVIEW

The WSGT contains two SSRE components. Under normal operating conditions only one will be necessary, but a second is available to support the SSA antenna combining operation briefly discussed in Section 2.

A simplified block diagram overview of the SSRE, and associated interfaces, is presented in Figure 3. A preliminary discussion of the SSRE components shown is presented here with more detailed discussion to follow in Section 4. The information here is primarily based on [1, 2].

ANALOG/DIGITAL INTERFACE

The incoming 35 MHz IF signal is first processed by a wideband ($\sim$ 10 MHz) noncoherent AGC to control the dynamic range of the composite signal + noise into the coherent AGC and the remainder of the receiver. As seen in Figure 3, the coherent AGC output is then processed by an analog voltage controlled amplifier (VCA), in-phase and quadrature mixed to baseband, and each low pass filtered in an analog fashion. It is at this point that digitation takes place, via 8 bit A/D conversion, and all remaining processing through NCO carrier reconstruction is then performed digitally.

The analog/digital interface is clearly identified in Figure 3. The treatments of the coherent AGC and the NCO are to be noted. Specifically, both are treated as lying directly on the interface since they both accept digital inputs while producing analog outputs.

Also noteworthy are the analog in-phase and quadrature low pass filters. The one-sided 3 dB bandwidth of each filter may take on one of three values, depending on the Shuttle mode of operation. The bandwidths are as follows:

- Mode 1 (288 KSPS): 1.75 MHz
- Mode 2 (576 KSPS): 3.5 MHz
- Mode 3 (unmodulated): 54 KHz

The significance of Mode 1 and 2 low pass filter bandwidths, as they relate to subsequent processing, is discussed in Section 4.

CARRIER LOOP/SYMBOL SYNCHRONIZER

Probably the heart of the SSRE is the "integrated" carrier tracking loop/symbol synchronizer. The term "integrated" is employed here since, contrary to conventional receivers which first perform carrier tracking and demodulation followed by symbol synchronization, the SSRE performs both operations simultaneously. Implementation of this design feature involves the use of digital, integrate-and-dump (I-D) arm filters in both the carrier loop and symbol synchronizer. Application of I-D arm filtering leads to a design which is near-optimum in nature and is therefore a very significant aspect of the SSRE in maximizing the efficient use of available carrier-to-noise ratio. A more detailed discussion of this portion of the SSRE will be presented in Section 4.

AMBIGUITY RESOLVER

Because the signal format of S-Shuttle data is Bi-Φ in nature, timing ambiguity associated with the mid-symbol and end-symbol instants, may exist. Resolution of this potential ambiguity is straightforwardly accomplished by this component of the SSRE.

LOCK DETECTOR

The lock detector implements the post-detection accumulated $\{|I|-|Q|\}$ characteristic which is used to ascertain when the carrier loop is in lock; the algorithm employed also prevents false carrier lock from occurring. Noteworthy here, once again, is an interesting departure from conventional receivers. While the typical receiver employs two separate lock detection circuits to monitor lock-up of the carrier loop and symbol sync, the present "integrated" design requires only once such circuit. The Lock Detector component is also expanded upon in Section 4.

SSRE OUTPUT INTERFACES

As seen in Figure 2 the SSRE provides several distinct outputs:

- recovered carrier
- recovered symbol clock
- 8 bit soft decision data
- lock status

The recovered carrier is externally used for doppler extraction and is further available as an output to be used in conducting laboratory measurements (e.g., for cycle slipping measurements). The recovered clock drives the external Viterbi decoder and also serves as an output for laboratory measurements (e.g., for data bit jitter measurements). The 8 bit soft decision data outputted by each SSRE may be combined as shown to enhance the effective output signal-to-noise ratio by approximately 2.5 dB. Whether or not combining is employed, the 3 most significant bits per detected information are then used as inputs to the Viterbi decoder. Finally, lock status output data is used both by WSGT and JSC for real-time performance monitoring.

The next section proceeds to provide some more detailed design information on selected portions of the SSRE.

4. SSRE DESIGN DETAILS

4.1 INTRODUCTION

Of the SSRE components identified in Figure 3, the following are treated in more detail in this section:

- Integrated Carrier Loop/Symbol Synchronizer
- NCO
- Lock Detector
- Coherent AGC

Each is individually considered in the subsections that follow, with the major consideration being the first item.

4.2 INTEGRATED CARRIER LOOP/SYMBOL SYNC

4.2.1 Overview

Figure 4 provides a simplified description of the carrier loop/symbol sync integrated structure, which motivates the subsequent more detailed discussion. The I and Q A/D converter outputs of Figure 3 are fed into the carrier loop portion of the SSRE, with the I component simultaneously employed by the symbol sync. The carrier loop accumulates I and Q samples, with each accumulator dumped once per symbol time, under the control of the clock shown. Of special significance here is the fact that each of the I and Q accumulators implements a digital, integrate and dump (I-D) filter and therefore each also requires an appropriate Bi-ϕ inversion operation to be performed on each of the samples accumulated during the second half of the accumulating period. The I-accumlator output represents desired soft decision data for external combining and Viterbi decoding. This output is also sign detected to yield a hard decision estimate of the data, denoted by $\hat{d}$, which is used to implement a decision directed carrier tracking loop. The I/Q multiplier output is then digitally filtered to yield the error signal for carrier reconstruction via the NCO.

The I input samples are simultaneously applied to symbol synchronization. As seen, mid-symbol and end-symbol accumulations are performed, dumped by the clock at appropriate intervals and processed by a Data Transition Tracking Loop (DTTL)-type of algorithm that is optimized for the Bi-ϕ signal format. Specifically, a mid-symbol polarity transition always occurs in each and every Bi-ϕ symbol, while end symbol transitions occur at an average rate equal to one minus the symbol transition density. The manner in which the symbol sync algorithm takes advantage of this will be clarified shortly. Note also from Figure 4 that the hard decision estimate, $\hat{d}$, is simultaneously employed by the carrier loop and symbol sync portions.

The integrated nature of the carrier loop/symbol sync structure is apparent from Figure 4 and the above discussion. Clearly, satisfactory operation of one portion is intimately dependent on satisfactory operation of its counterpart. This complicates the signal acquisition procedure, but once acquisition is complete and tracking takes over, the benefit of enhanced SNR operation, via the carrier loop I and Q I-D matched filters, readily presents itself. This benefit is, of course, coupled with the important advantage all digital processing provides in minimizing implementation losses.

4.2.2 Carrier Loop Details

A more detailed block diagram characterization of the carrier loop component is shown in Figure 5.

As seen, 16 samples per symbol are accumulated in each of the I and Q arms, independent of mode of operation; this independence makes the SSRE digital processing essentially transparent to the underlying nature of the analog input to WSGT. What is necessary, however, is that the sample clock rate be adapted appropriately. This is accomplished as follows.

The SSRE employs an underlying clock reference of 27.648 MHz, which is used to generate a sample clock rate matched to the mode of operation. In addition, the 3 dB bandwidth of each of the I and Q analog arm filters in Figure 3 is chosen for compatibility with sampling rate. Specifically, from Section 2, the one-sided 3 dB bandwidth for Mode 1 is 1.75 MHz, which implies a somewhat greater effective noise bandwidth. From a system theoretic viewpoint, noise samples taken at the Nyquist rate (based on the noise bandwidth) are statistically independent. Accordingly, the 1.75 MHz 3-dB bandwidth implies that more than 12 independent samples may be accumulated over the Mode 1 symbol duration.* This is

* I.e., 2 x (one-sided noise bandwidth)/symbol rate = 2 x $1.75 \times 10^6 / 2.88 \times 10^5 > 12$.

the basis for the 16 sample accumulation per symbol employed by the SSRE. Note that the associated nominal sampling rate is 4.608 MHz, which represents 6 cycles of the 27.648 MHz clock reference. Similarly, for Mode 2 the nominal sampling rate is 9.216 MHz and the associated low pass arm filter 3dB bandwidth is 3.5 MHz. As discussed below, these nominal sampling rates may be adjusted by the symbol sync component.

The number of quantized bits available at the input to each subcomponent is also indicated in Figure 4. The quantization scaling inherent in the 8 bit input to the I and Q accumulators is derived from the coherent AGC; the scaling reflects a dynamic range of ± 8|m| and a quantization stepsize of |m|/16, where |m| is the estimated signal mean absolute amplitude. It is apparent that negligible amplitude information is lost via the SSRE quantization scheme.

The I/Q multiplier output is further accumulated over 16 symbol intervals to enhance SNR and is fed into the phase and frequency components of the digital loop filter; this implementation leads to a second order carrier loop with a nominal damping factor of 0.707. Several additional aspects of the loop filtering should also be noted:

- the symbol accumulator is an integral part of the overall loop filter and, it, coupled with the other filter components shown, specifies the carrier loop bandwidth.
- frequency and phase scaling are also necessary for loop bandwidth specification and must reflect the symbol accumulation rate.
- phase and frequency clipping are employed to prevent overflow, but the probability of an overflow occurrence is very low.
- for carrier acquisition frequency sweeping is implemented by adding an appropriate digital word as shown in Figure 5; the frequency sweep limits are ± 70 kHz.

Also of importance with regard to frequency sweeping is the issue of false lock, under Mode 1 and 2 conditions. Because of the decision-directed nature of the loop, and the fact that it employes digital I-D arm filters, the potential for false lock presents itself at frequency offsets which are rational multiples of half the symbol rate [3]. The greatest possibility occurs at a frequency offset equal to half the symbol rate which is 144 kHz for Mode 1 and 288 kHz for Mode 2. For anticipated doppler offsets, however, these components do not occur, and other potential false lock states are automatically bypassed via the SSRE lock detector circuitry.

To complete the discussion on the carrier loop we include Figure 6 which describes the NCO. As seen, a 10 bit word is provided to the Sine Generator ROM which, in turn, generates an 8 bit word for D/A conversion to yield the desired updated carrier reference. The associated reference frequency varies over the range 500 kHz ± 50 kHz. Note that this reference is mixed with a fixed 34.5 MHz IF, the output of which yields the recovered carrier — nominally equal to 35 MHz — and is also an externally available output of the SSRE.

A summary of salient carrier loop parameters is presented in Table 1.

4.2.3 Symbol Sync Details

A more detailed block diagram characterization of the symbol sync component is shown in Figure 7. The symbol sync error signal is generated by using a DTTL-type of algorithm that is matched to the Bi-ϕ symbol format employed by Shuttle. Specifically, as seen, both "end-symbol" and "mid-symbol" accumulations are performed, with each involving 8 samples - i.e., a time interval equal to half a symbol duration. The mid-symbol accumulator sums up to the 5th thru 12th samples of the 16 samples encompassing the assumed symbol period. Under tracking conditions, the timing error will be a small fraction of a symbol and, by virtue of the Bi-ϕ format, a polarity transition will always occur during the mid-symbol accumulation interval; accordingly, a measure of the timing error is always available from the mid-symbol accumulator. The output of this accumulator is multiplied by the estimate of the given symbol's polarity, which is derived from the I accumulator output as shown; this multiplication is necessary for appropriate error signal generation, since it provides the direction of the timing error.

Under tracking conditions, when the timing error is sufficiently small (less than a quarter of a symbol period) the end-symbol accumulator straddles two adjacent symbols. For the end symbol, a polarity transition will only occur when the adjacent symbols are equal in polarity — this occurs at an average rate equal to one minus the symbol transition density. Note that the multiplication

by $(\hat{d}_n+\hat{d}_{n-1})/2$ generates the proper sense, or direction, of the timing error when a symbol transition does not occur and equals zero, otherwise. The fact that both end-symbols and mid-symbol transitions can be taken advantage of is a benefit of using the Bi-ϕ format, relative to NRZ.

The end-symbol and mid-symbol error signals are differenced to yield the composite error signal for processing by a second order loop filter. This loop filter consists of an N symbol accumulator followed by appropriate phase and frequency scaling and processing. The accumulation interval N is given by:

- N = 16 for wideband loop (acquisition)
- N = 128 for narrowband loop (tracking)

The composite effect of the N symbol accumulation and phase and frequency scaling specifies the loop bandwidth. Also of interest is the manner in which the sample clock rate is updated. The phase scale output is clipped to 4 bits for both Modes 1 and 2. This provides a capability for changing the clock phase as follows:

- Mode 1: up to 2 sample intervals in 1/6 sample ($\sim$.04μs) increments
- Mode 2: up to 4 sample intervals in 1/3 sample ($\sim$.04μs) increments

The frequency scale output is also clipped and the output is used to either stuff or delete clock pulses so that the effective clock rate may be effectively increased or decreased, respectively. The stuffing or deletion is uniformly spread over the N symbol accumulation interval prior to scaling. This frequency correction capability of the SSRE is useful in compensating for data bit jitter that may be present in the incoming signal.

Salient parameters of the symbol sync are summarized in Table 2.

4.3 LOCK DETECTOR

The Lock Detector circuit is shown in Figure 8. It provides lock status information to the SSRE output, to reflect lock of the integrated carrier loop/bit sync, and further initiates loop bandwidth adjustments to reflect switchover from acquisition-to-tracking and vice versa, if loss of lock occurs. The algorithm displayed by the figure is self-explanatory and need not be expanded upon. As a companion to Figure 8, Figure 9 displays the SSRE state diagram which describes the flow of the acquisition/tracking/reacquisition procedures performed by the SSRE.

4.4 COHERENT AGC

Figure 10 describes the coherent AGC circuit. The I accumulator output, under lock conditions, will typically exceed the noise level substantially. Thus, the 256 symbol accumulator output represents a close estimate of the signal amplitude under lock conditions. This then serves as a reference for gain control in a typical fashion. Note that the Coherent AGC represents one of the digital/analog interfaces of the SSRE.

5. SSRE PERFORMANCE

Selected SSRE performance results are presented in this section to reflect both demodulator and symbol error rate (SER) performances. These results reflect tests performed both by Motorola, Inc. and by the Electronic Systems Test Laboratory (ESTL) at JSC.

Figures 11 and 12 display results generated on SER performance and reflect SER results for both Modes 1 and 2, respectively. As seen, both modes behave in essentially identical fashions, with measured results extremely close to theoretical predictions — i.e., discrepancies <0.5 dB for SER values from 10^{-1} to 10^{-5}. Note that the Mode 1 $E_S/N_O \sim 2.8$ dB is the worst case Shuttle operating value. For Mode 2 the worst case E_S/N_O is approximately -0.2 dB.

Figure 13 illustrates carrier tracking loop performance, wherein rms phase jitter is plotted vs E_S/N_O. As seen, both Mode 1 and Mode 2 performances are substantially better than spec requirements. Furthermore, Mode 3 results (not shown here) display phase jitter performance very similar to that of Fig. 13.

Numerous additional tests were run at ESTL [4] to assess in-depth SSRE performance under both acquisition and tracking conditions. A brief summary of several of these results, together with pertinent observations now follow.

- For anticipated doppler uncertainties during acquisition Mode 2 never experienced false lock.

- For Mode 1 and under sufficiently strong signal conditions, temporary false lock occurrences were observed at frequency offsets of ± 36 kHz, ± 48 kHz, and ± 72 kHz, but the SSRE prevented a false lock from taking hold; these temporary false locks are consistent with the alias lock predictions of [3] and reflect the active arm filters employed by the SSRE. Furthermore, at an offset of ± 144 kHz a solid false lock did occur, but offsets of this magnitude are not anticipated during normal operation. Again, theory predicts the dominance of this 144 kHz component and its potential for yielding a false lock; specifically the dominance of this component is based on the decision — directed implementation of the carrier tracking loop.

Acquisition Time

- At expected C/N_0 levels ($\sim$ 62.8 db-Hz), the SSRE mean acquisition time never exceeded 0.5 seconds for both Modes 1 and 2.

- In the absence of doppler compensation mean acquisition time never exceeded 1 second.

Acquisition Threshold

- Thresholds and margins are summarized in Table 3. Note the much lower Mode 3 threshold which is based on the use of a much narrower acquisition loop bandwidth (See Table 1).

Cycle Slipping

- Under typical operating conditions, wherein the return link C/N_0 exceeds its forward link couterpart by 7.9 dB, and coherent turnaround tracking operation is in progress, the cycle slip thresholds are:

  Mode 1: 55.9 dB—Hz

  Mode 2: 57.4 dB—Hz

This compares to a nominally expected C/N_0 level of 62.8 dB—Hz.

Antenna Switching

- The switching from one Shuttle quad antenna to another requires a break-before-make operation — which, in turn leads to a signal dropout interval. At nominal C/N_0 values ($\sim$ 62.8 dB—Hz) and break intervals less than 25 ms, carrier loop lock was found to be lost with a 45% probability and $\leq$ 1600 symbol errors were made. Note that recovery from an antenna switch requires relocking of both the carrier and symbol sync loops. The rapid recovery of the SSRE once again displays its excellent performance.

6. CONCLUSIONS

The Tracking and Data Relay Satellite Systems, once operational, will significantly enhance the communication capabilities of Shuttle at both S- and Ku-band frequencies. Because of the unique nature of the Shuttle mission and its associated communication requirements, specialized supporting hardware and ground station configurations had to be developed. This paper focussed on the Shuttle S-band component and described in detail the unique S-Shuttle Receiving Equipment (SSRE) developed for incorporation into the TDRSS White Sands Ground Terminal.

To support S-Shuttle stringent link budget requirements, a state-of-the-art all digital SSRE design was pursued by its developer, Motorola, Inc. This paper described several of its significant features, including its integrated carrier-loop/sync sync component and its use of near-optimum digital-integrate-and-dump arm filters in the carrier loop. Selected performance results were also presented and the closeness (<.5 dB) of its error rate performance to theory was highlighted.

The SSRE represents an achievement that should serve as a basis for future state-of-the-art developments to be supported by NASA. One such TDRSS project is already under way. It involves the development, by Harris Corporation, of an all digital demodulator that performs A/D conversion at IF and implements third order carrier tracking loops to significantly enhance tracking performance under high dynamics conditions — such as occur during spacecraft unstable orbit conditions. An integrated carrier loop/symbol sync feature is also included. This new demodulator should be incorporated into the White Sands receiver, and become operational by 1985, at which time it will begin supporting S-band TDRSS users with data rates up to 300 kbps.

REFERENCES

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2. Motorola, Inc., Government Electronics Division, Operation & Maintenance Instructions: S-Band Shuttle Return Equipment for TDRSS Tracking, Return and Modulation Equipment (TRAM), Document No. 68-P09801M.
3. Marvin K. Simon and Kai T. Woo, "Alias Lock Behavior of Sampled-Data Costas Loops," IEEE Trans. Comms., Vol. COM-28, No. 8, August 1980, pp. 1315-1325.
4. Electronic Systems Test Laboratory, TDRS/Orbiter SSA Return and Two-Way RF Acquisition Test Report, JSC 18723, January 1983.

TABLE 1

CARRIER LOOP PARAMETERS

- INPUT IF: 35 MHZ
- DECISION-DIRECTED LOOP
  - DIGITAL INTEGRATE-AND-DUMP ARM FILTERS
  - 16 SAMPLES/SYMBOL
- SECOND ORDER LOOP
- 0.707 DAMPING FACTOR
- ACQUISITION SWEEP RANGE: ± 70 KHZ

CARRIER LOOP BANDWIDTHS (ONE-SIDED)

	ACQUISITION	TRACKING
MODE 1	1500 HZ	290 HZ
MODE 2	2400 HZ	510 HZ
MODE 3	250 HZ	24 HZ

- NCO FREQUENCY RANGE: 500 KHZ ± 50 KHZ

TABLE 2

SYMBOL SYNC PARAMETERS

- DATA TRANSITION-TRACKING-LOOP TAILORED TO BI-PHASE SYMBOL FORMAT
  - MID-SYMBOL AND END-SYMBOL ACCUMULATORS
  - HALF-SYMBOL ACCUMULATION WINDOWS
- SECOND ORDER LOOP

SYMBOL SYNC LOOP BANDWIDTHS (ONE-SIDED)

	ACQUISITION	TRACKING
MODE 1	2.88 KHZ	360 HZ
MODE 2	5.76 KHZ	720 HZ
MODE 3	N/A	N/A

- TIMING (PHASE) ADJUSTMENT CAPABILITIES
  - MODE 1: UP TO 2 SAMPLE INTERVALS IN ¼ SAMPLE INCREMENTS
  - MODE 2: UP TO 4 SAMPLE INTERVALS IN ¼ SAMPLE INCREMENTS
- FREQUENCY ADJUSTMENT CAPABILITIES
  - MODE 1: UP TO 1.0% CHANGE IN ~ .008 INCREMENTS
  - MODE 2: UP TO 2.0% CHANGE IN ~ .016 INCREMENTS

TABLE 3

SSRE ACQUISITION THRESHOLDS AND MARGINS

MODE	THRESHOLD C/N_0 (DBHZ)	REQUIRED C/N_0	MARGIN (DB)
1	51.2	60.2	9.0
2	48.9	57.2	8.3
3	29.3	N/A	N/A

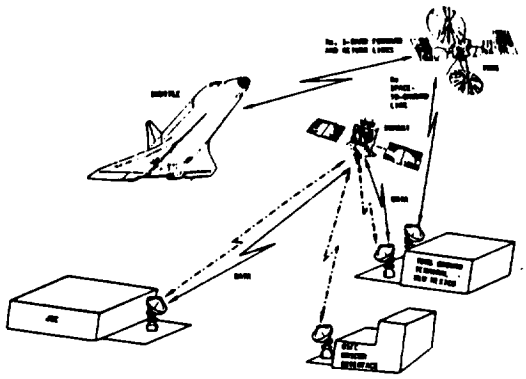

FIGURE 1: JSC, SHUTTLE AND TDRSS INTERFACES

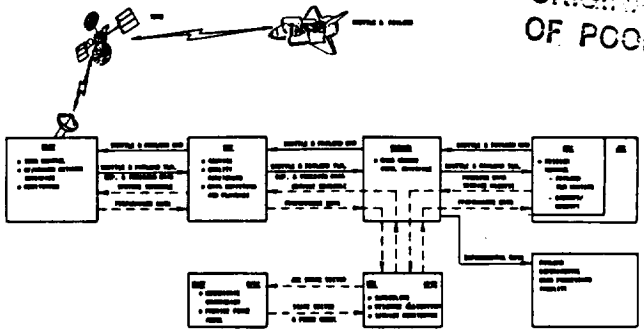

FIGURE 2: TDRSS NETWORK SUPPORT TO STS MISSION - AN OVERVIEW

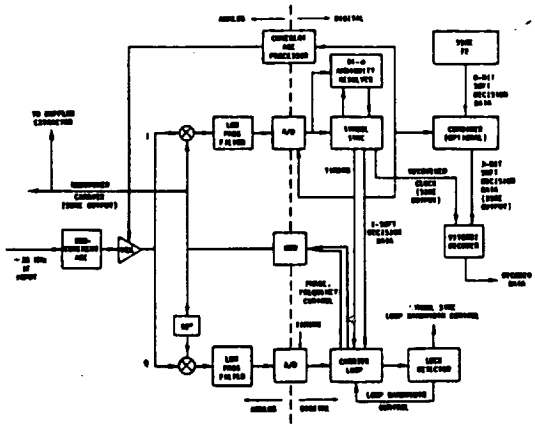

FIGURE 3: SSNE OVERVIEW AND ITS INTERFACES

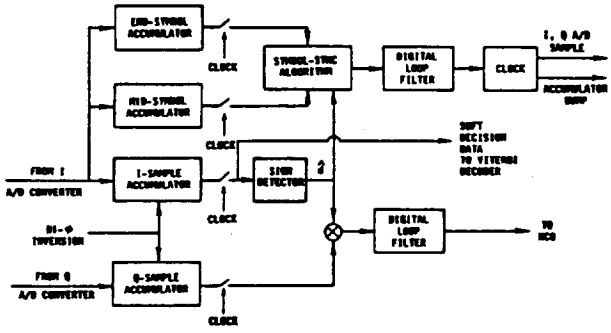

FIGURE 4: OVERVIEW OF SSNE, INTEGRATED CARRIER LOOP/SYMBOL SYNC

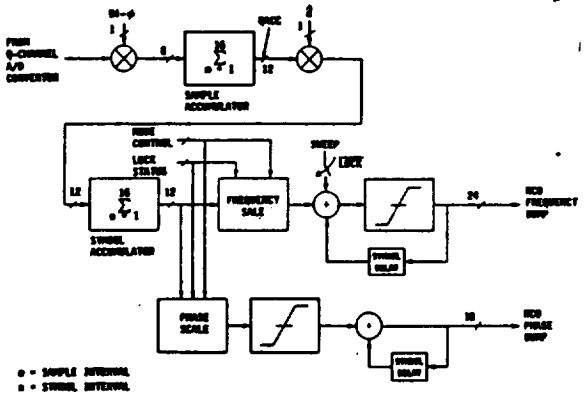

FIGURE 5: CARRIER TRACKING LOOP

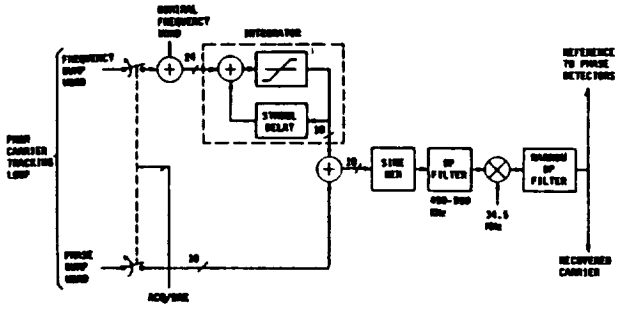

FIGURE 6: NUMERICALLY CONTROLLED OSCILLATOR (NCO)

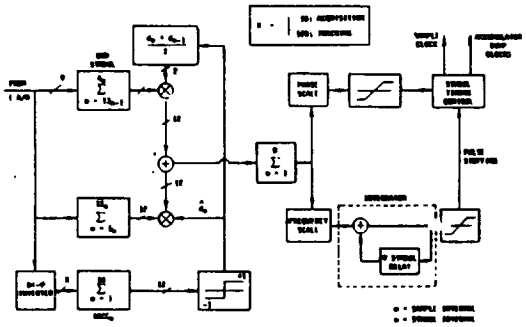

FIGURE 7: SYMBOL SYNCHRONIZER

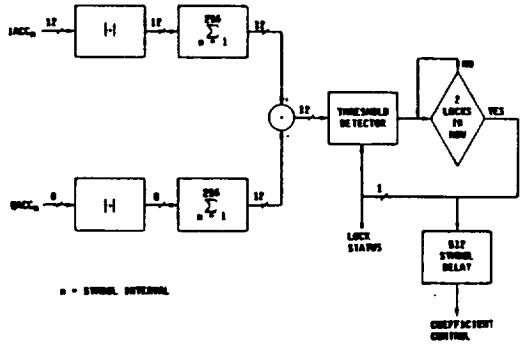

FIGURE 8: LOCK DETECTOR

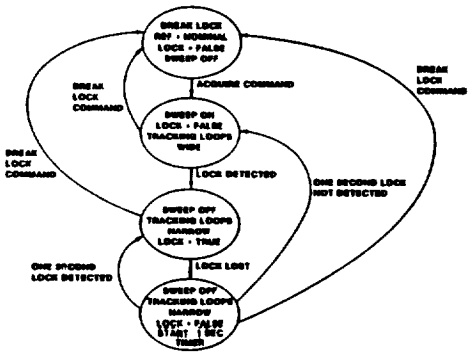

FIGURE 9: SSNE STATE DIAGRAM

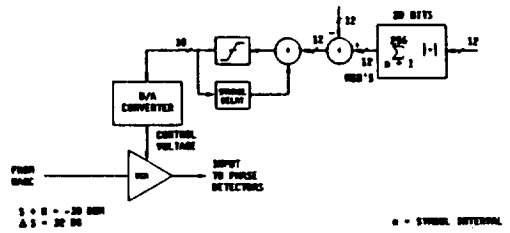

FIGURE 10: COHERENT AGC

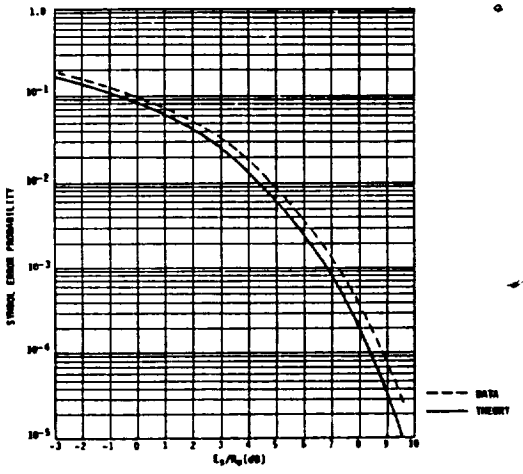

FIGURE 11: PROBABILITY OF ERROR FOR PSK DATA - MODE 1

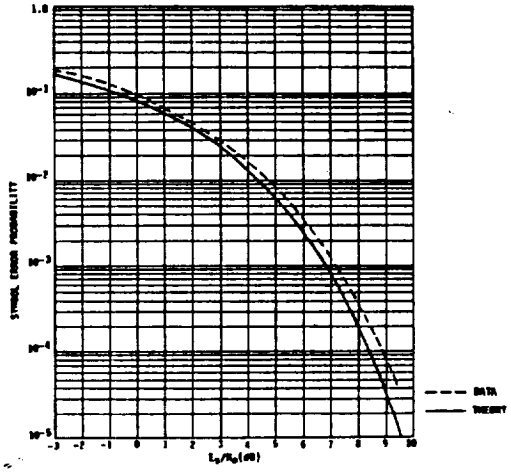

FIGURE 12: PROBABILITY OF ERROR FOR PSK DATA - MODE 2

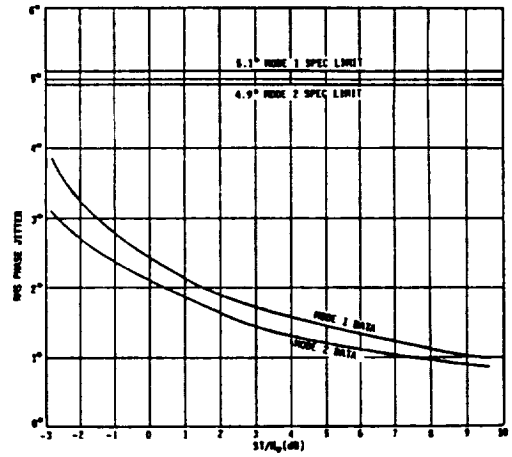

FIGURE 13: MODES 1 AND 2: DEGREES OF PHASE JITTER