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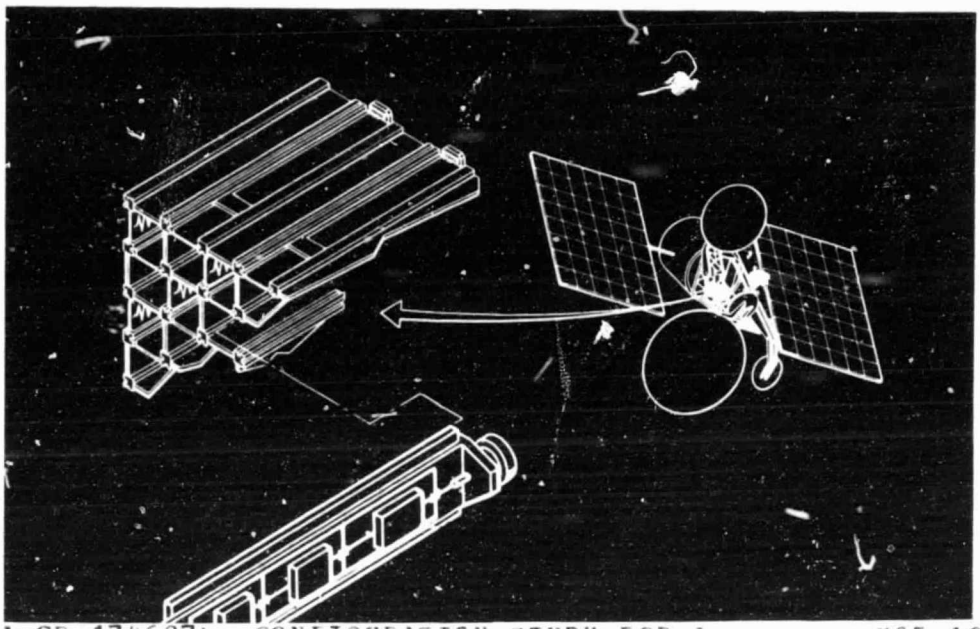
Configuration Study for a 30 GHz Monolithic Receive Array

TECHNOLOGY ASSESSMENT



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16. Abstract

This report summarizes the results of configuration and design studies for 30 GHz receive antennas on a communications satellite. The antennas use reflector focusing systems with phased array feeds for beampointing, aberration correction, and interference suppression. The phased array feed designs are based on MMIC module technology. The antennas form simultaneous multiple beams in both scanning beam and fixed beam designs. Polarization diversity is used for beam isolation.

The initial configuration study and parametric design analyses encompassed Gregorian, Cassegrain, and single reflector systems. Parametric design and performance curves were generated. A preliminary design of each reflector/feed system was derived including radiating elements, beam-former network, beamsteering system, and MMIC module architecture. Performance estimates and component requirements were developed for each design. A recommended design was selected for both the scanning beam and the fixed beam case.

Detailed design and performance analysis results are presented for the selected Cassegrain configurations. The final design point is characterized in detail and performance measures evaluated in terms of gain, sidelobe level, noise figure, carrier-to-interference ratio, prime power, and beamsteering. The effects of mutual coupling and excitation errors (including phase and amplitude quantization errors) are evaluated. Mechanical assembly drawings are given for the final design point. Thermal design requirments are addressed in the mechanical design.

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TABLE OF CONTENTS

1 MONOLITHIC RECEIVING ARRAY TECHNOLOGY

In this section we cover the status of the use of monolithic microwave integrated circuits (MMICs) in phased array feeds. This discussion is in two main parts; the current status of MMIC technology and the technologies associated with the integration of MMICs into phased feeds.

The current status of MMIC technology section will cover the areas of cost performance, reliability and design considerations. An assessment of these areas while primarily circuit and processing oriented have important ramifications to the use of MMICs in arrays.

The section on integration of MMICs into phased array feeds will address transitions to the MMICs, compatible antenna radiating elements and reliability considerations.

1.1 STATE OF THE ART OF MONOLITHIC MICROWAVE INTEGRATED CIRCUITS

1.1.1 Overview - Advantages and Disadvantages

Monolithic microwave integrated circuits (MMICs) have been a fast growing field in the last five years. This section will cover some of the important advantages of MMICs that have led to this interest; it will also cover some of the disadvantages of using a monolithic approach.

Monolithic means all active and passive circuit elements and interconnections are formed on the surface of a semi-insulating substrate. There are several attributes of monolithic circuits:

1) low cost

2) small size

3) improved reliability

4) highly reproducible

5) multifunction circuits

6) better performance.

The low cost derives from the reduction in required assembly.

Individual, non-monolithic circuits must be packaged, assembled, and wire bonded; a very labor intensive procedure. By placing all the circuits on a single chip this handling is greatly reduced and the total cost is more a function of material and processing costs.

The small size of the monolithic circuits allows a large number of the circuits to be processed on a single wafer, the greater the number of circuits that can be processed at one time the lower the cost per circuit. Figure 1 shows projected cost of an MMIC module through 1987. Each module consists of a radiating element, a low noise amplifier, a phase shifter and some logic elements. As can be seen, by 1987 the cost is expected to be reduced by a factor of 10.

This cost estimate is based on material costs, processing costs, fully loaded labor costs and RF and DC circuit testing. The material cost includes substrate qualification, epitaxial growth, (and/or ion implantation) and profile evaluation. The processing costs include assumptions of the development of a 50% yield capability and the use of electron beam lithography techniques. The electron beam lithography is needed to achieve the sub-micron gate geometries required at millimeter wave frequencies. If new processing technologies are developed that allow the use of electron beam lithography for the fine features and the higher throughput photolithography for the circuit elements a reduction of processing costs is possible.

Testing costs include both RF and DC testing. Wafers are DC probed before dicing to identify function circuits. Each function circuit must then be RF tested. These procedures can be made fairly automated under production conditions. For example GE recently had a production contract to produce 500 S-band, monolithic phase shifters. During the 4-month effort the mean time required to DC and RF test a single phase shifter chip was reduced from 45 minutes to under 15 minutes. This included taking a diced chip, cleaning it, mounting it in the test package, verifying the DC characteristics, and RF testing each phase state at 15 frequencies in the band of interest. Some of the innovations made possible by the large number of chips to be tested included elimination of wirebonds by using specially designed RF and DC probes, elimination of conductive epoxy by using a special mechanical housing and computer control of phase state and RF testing.

Not included in the above cost estimates are any nonrecurring costs such as capital investment, engineering, mask generation, and process development. These costs are quite high but become relatively less important in long term production runs.

The MMIC advantages of improved reliability, highly reproducible and better performance are related to placing all the circuits on a single chip. The elimination of wire bonds and the need for external matching circuits removes many of the undesirable parisitics which affect performance and cause circuit to circuit variation. Monolithic approaches also allow the designer to take previously unused approaches. For example, distributing amplifier stages to enhance performance; this is usually avoided in discrete amplifiers because of the cost penalty.

The small size of monolithic circuits allows a high level of circuit integration on a chip including placing phase shifters, mixers, amplifiers and switches on the same substrate. This leads to devices whose performance more closely tracks with temperature variations.

There are also disadvantages to monolithic circuits some of which are:

1) poor device to chip area ratios,

2) circuit tuning,

3) circuit RF coupling.

4) thermal dissipation.

The active devices used in monolithic circuits occupy a relatively small percentage of the chip area. This results in inefficient use of substrate material by putting circuits on it. From a material cost standpoint monolithic approaches are uneconomical.

Circuit tuning of monolithic circuits is difficult. It can be achieved by using circuit elements that can be laser trimmed or mechanically removed but this violates one of the perceived advantages of monolithics viz. minimizing assembly labor. Another solution is to use designs that are insensitive to process variations.

The problem of circuit RF coupling is a result of the small chip sizes involved. Figure 2 shows the coupling between two parallel microstrip lines on a GaAs substrate; the coupling is calculated as a function of line length and line spacing. It can be seen that coupling becomes quite unacceptable for long lines and may be too high for lines under a quarter-wavelength long. This causes circuit sizes to grow thus compounding our first disadvantages.

Thermal dissipation results in power devices where the rest can not be removed through the chip. One solution to this is to make the chip very thin making heat transfer easier but the chips become more difficult to handle.

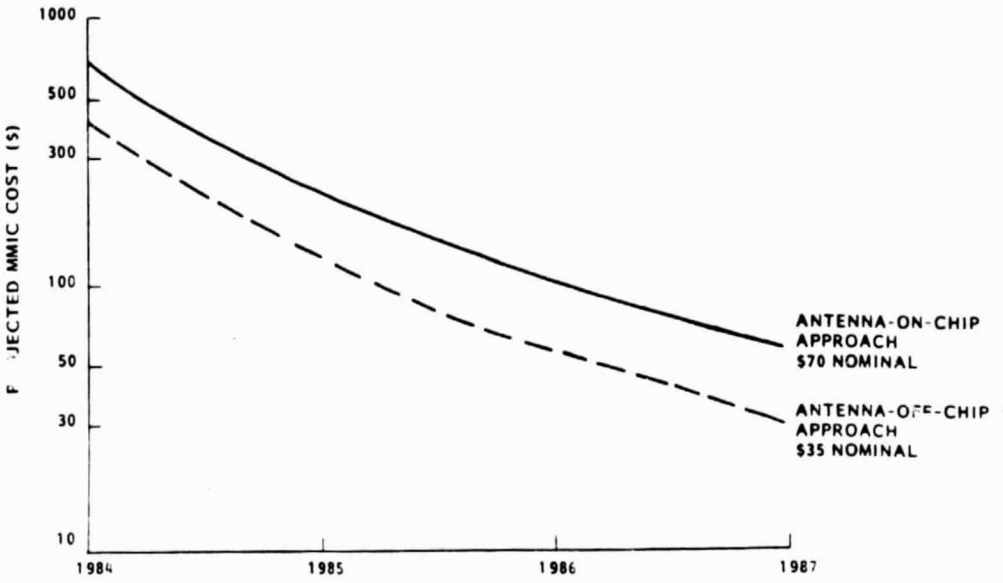

Figure 1. Projected MMIC Processing Costs Through 1987

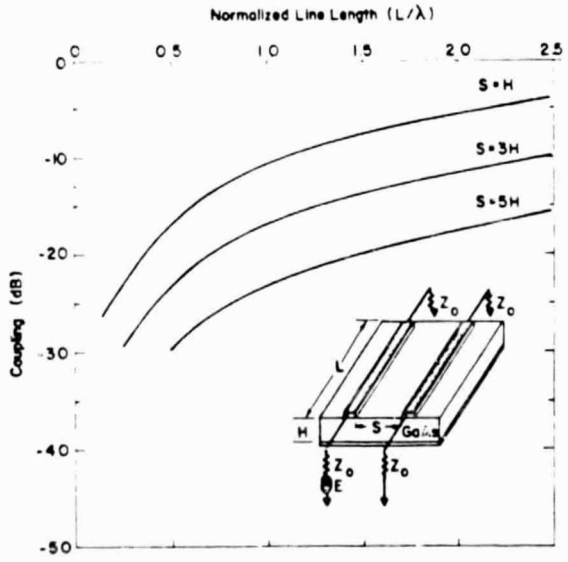

Figure 2. Calculated Coupling Between Adjacent Parallel Microstrip Lines as a Function of Spacing and Frequency

1.1.2 Fabrication Technology

1.1.2.1 Materials and Devices

A broad array of III-V semiconductor alloys and devices is currently being investigated for higher frequency applications. Among the technologies under development, GaAs technology is by far the most mature. Discrete sub-micron gate-length MESFETs have demonstrated useful gain to 40 GHz. Two physical factors that determine the suitability of a III-V alloy for microwave application are its low field electron mobility and high field saturation velocity, which determine the electron source-to-drain transit time in a MESFET.

Another III-V compound material that has an electron saturation velocity that is approximately 25% higher than GaAs (i.e. 2.3×10^7 cm-sec^{-1} as opposed to 1.8×10^7 cm-sec^{-1} for GaAs) is InP. However, the present state of InP material quality and device processing has not yet resulted in a device that is conclusively superior to comparable geometry devices fabricated on GaAs.

Other III-V alloys, such as InGaAs, that have significantly higher low field electron mobility (11,000 cm$^2 \cdot$V^{-1} sec^{-1} for InGaAs as opposed to 4400 cm$^2 \cdot$V^{-1} sec^{-1} for GaAs) and higher peak velocity (2.4×10^7 cm/sec) have not shown significant microwave performance due to the lack of a suitable metal-semiconductor (Schottky) gate. For instance, the barrier height of a Au-InGaAs Schottky junction is only .2V, which makes the junction contact too leaky to be useful.

Alternatives to the GaAs MESFET that offer the potential of better transistor performance are unattractive for this application because of the present state of their development and added fabrication complexity. Devices such as the HEMT (High Electron Mobility Transistor), PBT (Permeable Base Transistor), and Vertical Geometry FET require considerable further development before these devices can be integrated into MMICs.

The GaAs MESFET is the most important circuit element in the fabrication of MMICs, since its design and construction will determine the MMICs performane, producibility, and reproducibility.

The performance and reproducibility of a GaAs MESFET are both material and device-geometry related. The predominant factors in the GaAs MESFET structure that determine its performance and reproducibility are the substrate-active-layer interface, the gate length, and the gate and source resistances. The effect of these variables on device performance is well understood, and the control of these variables is well within present processing capability for devices.

The physical features of a completed GaAs FET that we are presently using are shown in Figures 3, 4, and 5. The FET uses a recessed-gate (etched-channel) structure and multiple gate feeds and is presently considered to be the optimum structure for a low noise FET.

Shown in Figure 3 is a top view of the MESFET. The device has a total gate width of 100 microns and is fed at three points to reduce the gate resistance and minimize the phase delay of the incoming RF signal along the width of the gate stripe (i.e. the maximum gate distance from a feed point is 16.6 microns). To allow the gate to be fed at multiple points, the MESFET source is segmented into four sections. These sections are connected with air-gap crossovers. A gold multi-level metallization system, which is also visible in Figure 3, is used to fabricate the crossover network. The gate recess, which is used to reduce source resistance, is precisely controlled by the monitorings of the full channel current (I_f).

The gate resistance R_g is a noise source itself, and it deteriorates the gate noise correlation with channel noise. In the MESFET, the gate resistance is minimized by the gate feed network, the gate metallization system (Ti/Pt/Au), and the gate metallization thickness.

Another circuit element that will deleteriously effect MESFET performance is R_c, the source and drain contact and spreading resistance. Not only does poor ohmic contact degrade noise figure, but its distributed nature makes the MESFET performance more sensitive to source-drain spacing variation. A N^+-Ge/Ni/Au metallization system results in a contact resistance of less than 10^{-6} Ω-cm^2, which is sufficiently small to make the contact resistance substantially smaller than R_{S2} and R_{S3}.

As shown in Figure 6, a MESFET's structure consists of three layers, which are grown on bulk GaAs and then successively etched backed. Since for low noise operation, I_{DS} is biased to approximately 15% I_{DSS}, the source-drain conduction will be near the buffer-active-(channel) layer interface. Thus the quality of the buffer and active layers is very important at this interface, since lower electron mobility will result in transconductance compression.

1.1.2.2 MMIC Processing

As is described in Section 1.1.2.1, a recessed gate MESFET with .3 μm gate length can be designed to be minimally affected by processing variations while providing the necessary performance for 30 GHz operation. This describes GE's present MMIC processing sequence which contains all the essential elements of the above discussion.

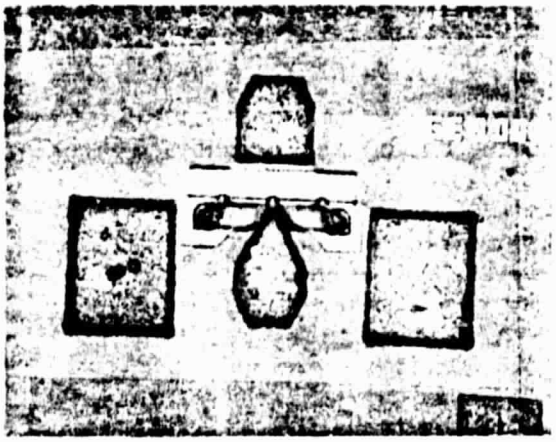

Figure 3. Top View of a GaAs MESFET

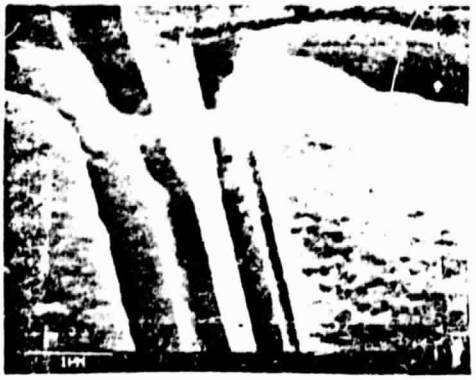

Figure 4. SEM Microphotograph of 0.3um Gate in Recessed Channel Showing Gate and Gate Feed

Figure 5. SEM Microphotograph of GaAs MESFET Mesh with 0.3um Gate Metallization Over Mesh Edge to Buffer Layer

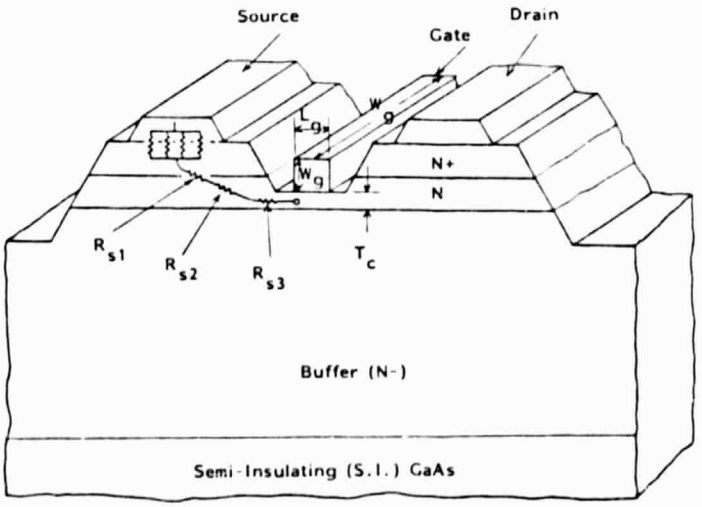

Figure 6. Cross-Section Drawing of Recessed Gate Structure with the MESFET Equivalent Circuit Source Elements

As described in the previous section, the etched-channel or recessed-gate MESFET structure is presently considered to be the optimum device design for low noise amplification. GE's approach for fabricating this structure basically consists of a series of selective etch back steps of vapor phase epitaxy (VPE) layers that have been grown with the desired doping profile. Isolated MESFETs are fabricated in GaAs mesa islands on semi-insulating GaAs wafers. The starting GaAs substrate material that forms the basis for the construction of the MMIC consists of three layers grown by VPE on semi-insulating GaAs. From these three layers are etched the source and drain contacts, the recessed channel, and the MESFET isolation mesas. The doping profile for the layers is shown in Figure 7.

The N^+ (heavily doped) ohmic contact layer is 0.25 μm micron thick. Its purpose is to provide electrical contact to the active layer and to minimize the parasitic source and drain resistances. As shown in Figure 8, the use of the N^+ contact reduces the effect of source-drain separation processing variation on device noise figure. The active layer (designated as n to indicate moderate doping) forms the MESFET channel and resistors in the MMIC structure. The undoped n- buffer layer provides electrical isolation under the channel and prevents migration of impurities and defects from the semi-insulating substrate into the MESFET area, and, therefore, improves the electron mobility near the active layer interface.

The sequence of process steps we perform on the VPE grown layers and the MMIC circuit elements that result at each step are shown in Figure 9. MESFETs are fabricated in Steps 1, 2, and 5 on isolated mesas or islands of epitaxial material. The n^+ and n semiconductor layers are etched to form ohmic contacts for the source and drain and recessed channel region of a Schottky gate, as is shown in Figures 10 through 13. Resistors are also formed by etching the mesa structure and thinning the n region to achieve the desired resistance, as is shown in Figure 14. The remaining passive circuit elements are fabricated off the mesa in Steps 5 through 9 on the insulating buffer layer. Figures 15 through 18 follow the development of two of these passive elements, the metal-insulator-metal (MIM) capacitor and the air bridge.

The channel thinning procedure shown in Step 1 of Figure 11 etches the MESFET and resistor channels to a predetermined thickness. A chemical etch rapidly removes the bulk of the n^+ layer. The channel layer now has a more uniform doping-thickness product than the originally grown layer. Adjustment of the device's pinch-off voltage and saturation current is made by a series of slow etches followed by electrical measurement.

The mesa etch (Step 1, Figure 11) removes the channel and active layers except in those areas where FETs and resistors are to be formed. The resulting mesas are isolated from each other, and the rest of the substrate is stripped to the semi-insulating buffer layer on which the remaining passive elements will be formed. To ensure good isolation, etching into the buffer layer is continued until a breakdown voltage of 500 V is achieved.

Ohmic contacts are formed in Step 2, Figure 12, where it is crucial to obtain the low contact resistance necessary for low-noise and high-power FETs. Ohmic contacts for FETs and resistors are using E-beam lithography, and a weak etch is used to clean the n^+ contact surface. The following metals are sputtered in succession:

- Ni 50 Å wetting agent
- Ge 300 Å to form Au/Ge alloy
- Au 600 Å
- Ni 200 Å wetting agent to prevent balling up of gold
- Au 1,600 Å to cap contact

A lift-off process is used, leaving the metal only on the contact areas. Alloying of the contacts is then achieved by placing the wafers in a 450-degree furnace and allowing them to remain there three minutes after their temperature reaches 440 degrees C. Resulting sheet resistances of the ohmic contact areas are less than 1×10^{-6} ohms-cm^2. The formation of resistors continues next with another masking step and the removal of the n^+ layer. The resistance values are brought into specification by further etching into the n region, as is shown in Figure 14.

The GaAs MESFET structure is completed with Step 5 (Figure 13), in which the Schottky gate is formed. The gate structure is defined by E-beam lithography because of the .3 µm geometry required. E-beam resist (PMMA) is first deposited over the wafer. The gate area is then opened using E-beam lithography. The channel is then recessed and then the gate metallization deposited.

E-beam lithography allows the channel recess to be aligned to the source within .1 micron. This is the most critical step in the MMIC process, requiring (1) gate lithography, (2) critical alignment to the channel opening, (3) low-leakage Schottky barrier formation, and (4) clean lift-off of the metal. Reference to Figure 19 shows that the gate metal is also used for air bridge underpasses and the bottom metal periphery of interdigitated capacitors. As a processing option, it may also be used to form metal-insulator-metal (MIM) capacitor bottom electrodes, eliminating the need for Step 4. The gate metal must be evaporated because damage is induced on the GaAs surface if sputtering is used. The following metals are evaporated:

- Ti 500 Å Schottky Barrier Metal
- Pt 500 Å Barrier metal (to prevent diffusion of gold into Ti)
- Au 4,000 Å Conducting layer.

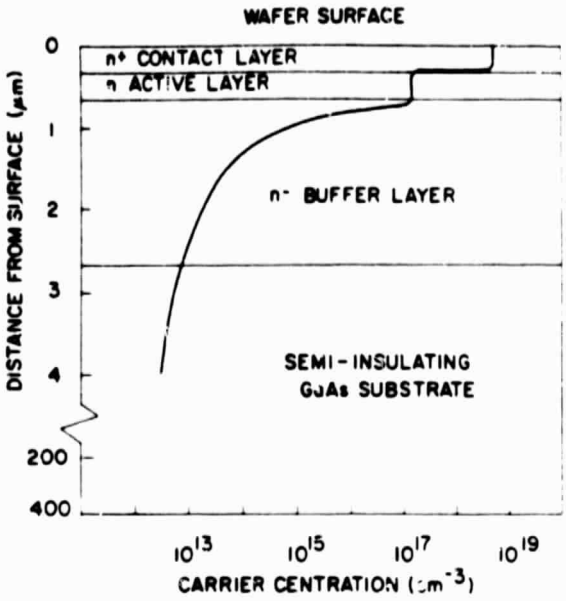

Figure 7. GaAs MMIC Epitaxial Structure

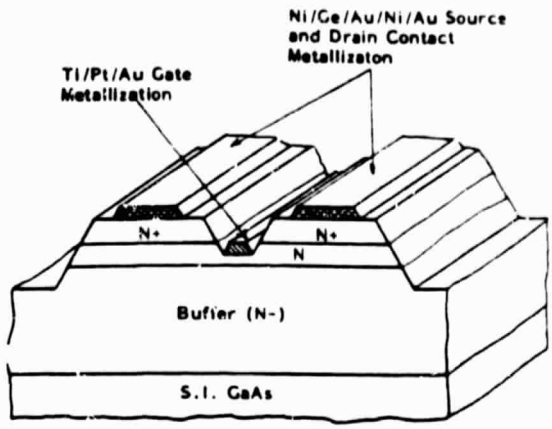

Figure 8. GaAs Recessed Gate MESFET Cross-section with Source, Drain and Gate Metallization

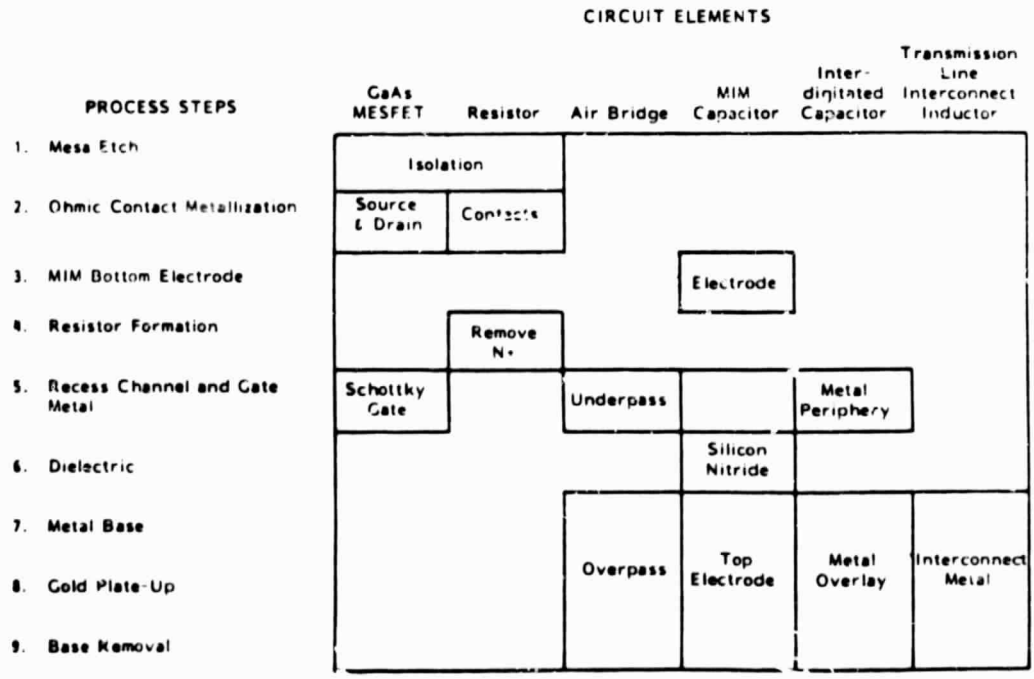

Figure 9. Formation of Circuit Elements in the GaAs MMIC Process

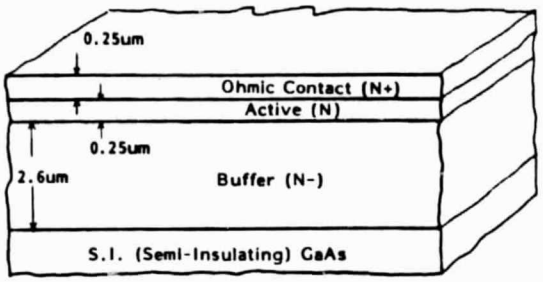

Figure 10. GaAs Wafer Material Cross-section Showing Buffer (n-), Active (n) and Ohmic Contact (n+)

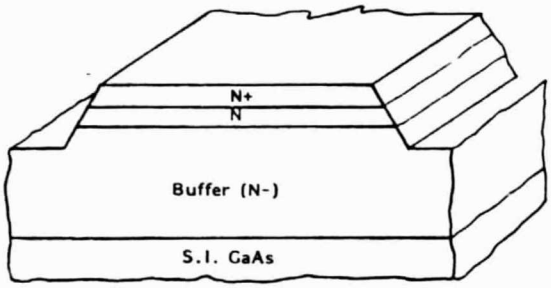

Figure 11. (Step 1) GaAs Wafer Cross-section After MESA Etch

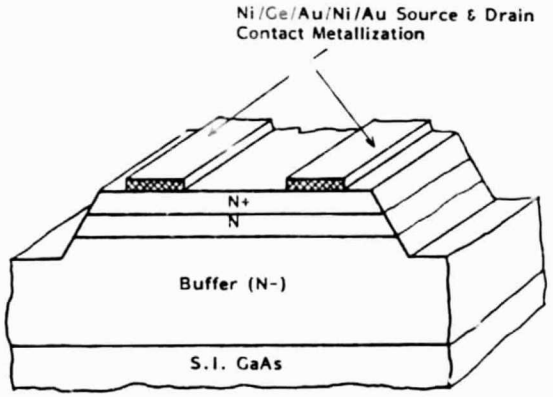

Figure 12. (Step 2) GaAs Wafer Cross-section After Source Drain Ohmic Contact Metallization

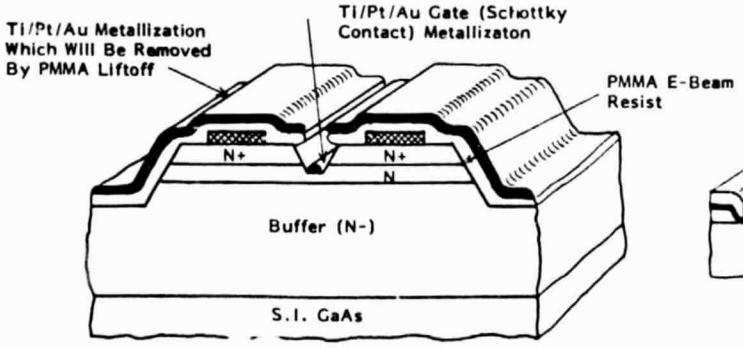

Figure 13. (Step 5) GaAs MESFET Cross-section Showing Recessed (Etched Channel) Gate and Gate Metallization Prior to Photoresist Lift-Off

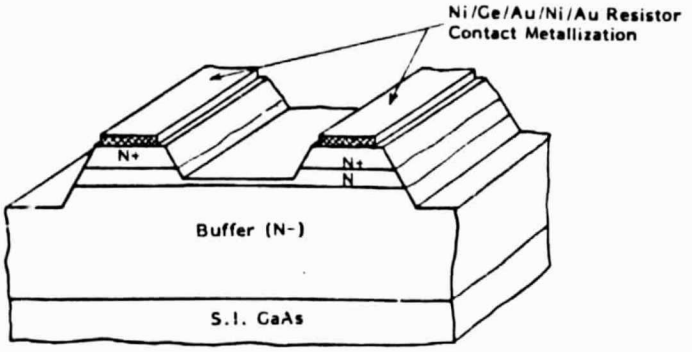

Figure 14. (Step 4) Cross-section of Resistor Form-by n-Channel Thinning

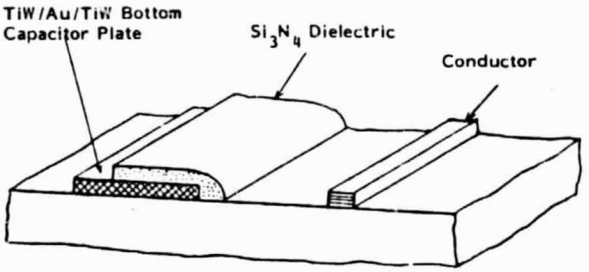

Figure 15. Air Gap Crossover and Metal-Insulator-Metal (MIM) Capacitor Formation Showing Bottom Plate and Dielectric Depositions

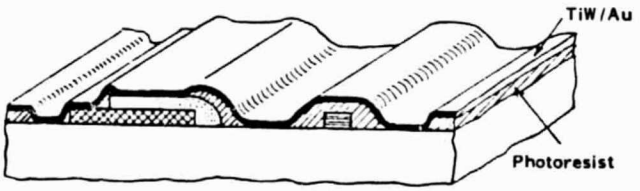

Figure 16. Air-Gap Crossover and MIM Capacitor Formation Showing Top Metallization

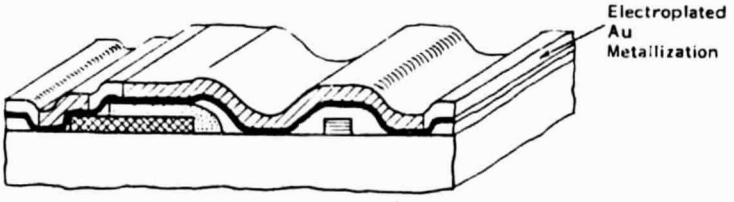

Figure 17. Air-Gap Crossover and MIM Capacitor Formation Showing Top Metallization After Electroplating

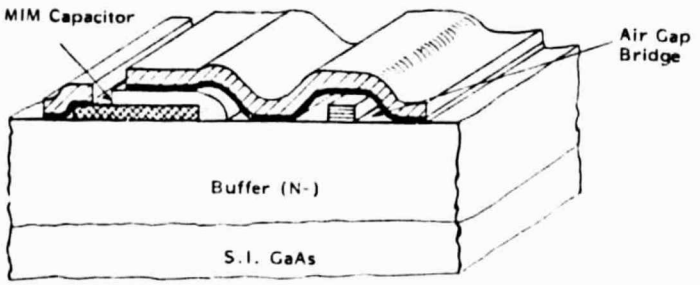

Figure 18. Completed Air-Gap Crossover and MIM Capacitor Formation After Photoresist Removal

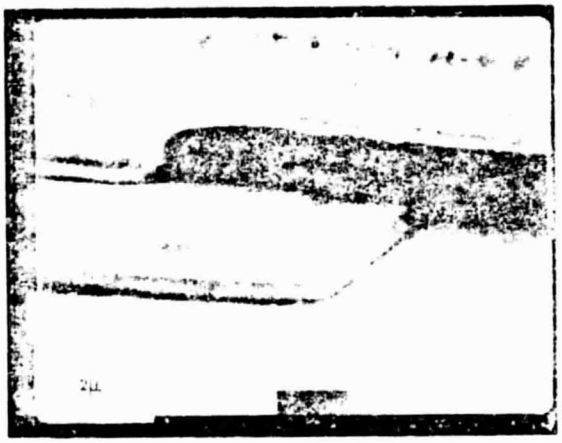

Figure 19. Air Bridge Underpass

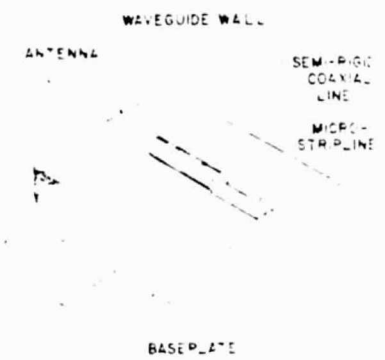

Figure 20. Antenna Coaxial Transducer

After lift-off of the gate metallization, the transistors are complete, and a DC test is performed. The saturation current, I_{dss}, pinch off voltage, V, and current-voltage relationships of the tested devices are recorded.

The resistors and MESFETs have now been fabricated on the mesas.

- TiW 500 Å Adhesion to GaAs
- Au 4,000 Å To form conducting path
- TiW 500 Å Adhesion to silicon nitride

Sputtering is used for this process because its adhesion has proven superior to that of evaporated metal and its surface smoothness results in fewer shorts. However, Step 4 can be consolidated on the same mask as Step 5 by eliminating the sputtering, and for the purposes of th following discussion the two metallizations may be considered identical.

In Step 6, silicon nitride (Si_3N_4) forms the dielectric for MIM capacitors. A plasma is used to deposit the nitride on the entire GaAs wafer, after which photoresist is applied to protect the capacitor areas where dielectric will remain. Hydrofluoric acid etches away the unwanted nitride. The dielectric constant of the nitride layer is 6.5, resulting in a capacitance per unit area of 0.2 pF mil^{-2} for a thickness of 0.186 microns. To attain the desired capacitance, a monitor wafer is measured with an ellipsometer to determine the thickness and refractive index of the nitride layer.

In step 7, a metal base of titanium-tungsten and gold is sputtered:

- TiW 500 Å Adhesion to GaAs substrate
- Au 1,000 Å Conducting surface for plate-up.

Following top-side (circuit-side) processing, the wafer is mounted face down to a flat quartz plate and mechanically thinned to 4 mils thickness. While still mounted, the back (ground plane) side of the wafer is processed. A via hole mask is aligned with the circuit side pattern using an infrared aligner (i.e. GaAs is transparent to infrared), via holes are then etched. The ground plane is then metallized using thin film evaporation and ground contacts to the circuit are made.

1.2.1 Transitions

The use of monolithic circuitry allows the receiver front end to bcome an integral part of the antenna feed and beamforming network. The low noise amplifier, phase shifter, weighting amplifier, and mixer submodules become distributed throughout the feed array, thereby making it possible to achieve a minimum system noise figure. In order to take maximum advantage of this potential, low loss, well matched transitions from the modules to the beam combining network must be used. These transitions will be covered in this section.

If the beam combining network is realized in microstrip or stripline the transition is relatively easy to achieve. For microstrip a wire is bonded from one transmission line to the next; the ground planes of both must also be electrically continuous. This type of transition is routinely made with MMICs.

A transition from stripline to the module is only somewhat more difficult as both structures are TEM. Again a wire or ribbon is bonded from one transmission line to the next transmission line. A degree of compensation must be incorporated to account for the discontinuity of removing one-half of the dielectric and one ground plane.

A transition from waveguide to microstrip is more difficult to achieve. There are four transitions that are commonly used:

1) antenna coaxial transducers

2) antenna feedthrough transducers

3) ridged waveguide transducers

4) printed circuit transducers.

The antenna coaxial transducer consists of an antenna formed by the center conductor of a coaxial line, which protrudes through the broadwall of the waveguide. The waveguide is terminated in a short circuit. The other end of the coaxial line is connected to the microstrip circuit as shown in Figure 20. There is an optimum position for the antenna in waveguide in which the impedance of the probe/shorting wall combination is matched to the coaxial line impedance. This position is typically .23 to .218 λg.

The antenna feedthrough transducer consists of a 1- or 2-mil diameter gold wire antenna protruding through the broadwall of the waveguide at the optimum position, as above. The other end of the wire is bonded directly to the circuit. The short distance through the waveguide wall forms a coaxial line with air dielectric. Again the waveguide is terminated in a short circuit.

A ridged waveguide transducer consists of a set of quarter wave, stepped, ridged waveguide sections that transform the input waveguide impedance to that of the microstrip (Figure 21). The final step of the ridged waveguide transformer is connected to the microstrip line via pressure contact. The number of quarterwave sections can be chosen to achieve the bandwidth required. The insertion loss for a single transition is typical under .4 dB with an associated VSWR of 1.15:1. Certain problems arise in the use of the ridged waveguide transition. One is direct leakage of power from the open end of the waveguide. Another is the difficulty of achieving good electrical contact between the ridge and the microstrip line.

The printed circuit transducer consists of a dielectric substrate with a circuit pattern printed on each side, inserted into the waveguide. The pattern consists of gradually tapered ridges on opposite sides of the dielectric, concentrating and rotating the electrical field into a parallel line. This symmetrical line is matched to the asymmetrical microstrip with a balun. Figure 22 shows the substrate inserted into the waveguide.

The ridges and the ground plane of the microstrip must make electrical contact with the wall of the waveguide. The balun section is obtained by slots in the ground plane and a reduction of the upper line width. Propagation through the waveguide is prevented by the ground plane dividing the guide into two parallel guides with a cutoff frequency for above the waveguide band.

Measured results of this transition show insertion loss less than .25 dB over a 25% band with a VSWR of 1.5:1 or better. The transition can be optimized for narrower band operation (10%) with less than .1 dB insertion loss with a VSWR of 1.2:1 or better.

1.2.2 Monolithic Circuits for Phased Array Applications

A variety of amplifier circuits including low noise, variable gain, and power amplifiers have been fabricated in monolithic form[1]. Circuits with usable gain up through K-band have been reported[2]. Figure 23 shows a two-stage low noise GaAs amplifier for receive applications designed at the General Electric Electronics Laboratory. The amplifier is complete in that it includes the input, output, and interstage matching circuitry as well as the DC bias networks. The chip size is only 0.89 by 2.29 mm and has a thickness of 0.10 mm. This extremely small size is made possible by the use of lumped elements in the impedance matching networks. The spiral inductors and interdigitated capacitors of these networks can be seen in the photograph. Two versions of this low noise amplifier circuit have been fabricated, one for S-band and the other for C-band. Both deliver a gain of approximately 18 dB over a 20 percent bandwidth.

Figures 24 and 25 show typical monolithic power amplifiers fabricated on GaAs for transmit applications. Both amplifiers employ distriutd element impedance matching circuitry and include on chip DC bias networks. These circuits have been thinned to 0.10 mm thickness to lower the thermal resistance between the MESFETs and the chip carrier. Via or plated through holes are also used to realize low inductance contacts to ground. The three-stage amplifier of Figure 24 has demonstrated 20 dB of gain between 5.2 and 6.0 GHz and a power output of 400 mW. The chip size measures 1.91 by 4.70 mm. Similar designs have also been fabricated for S- and X-band operation. The two-stage power amplifier of Figure 25 delivers 1.5 watts of output power at C-Band with a gain of better than 16 dB. The chip size measures 2.16 by 4.83 mm.

Variable gain amplifiers allow for adaptive amplitude weighting in phased array systems. Amplifiers having a gain continuously variable from -15 to +5 dB have been fabricated in monolithic form by using dual gate MESFETs as the gain controlling element[3]. A variable DC bias voltage is applied to one gate while the second gate is terminated in a specific impedance so as to make the amplifier's phase shift relatively unchanged with gain setting.

Phase shifters and transmit/receive switches have been successfully fabricated in monolithic form by utilizing resonated MESFETs as switching elements. Figure 26 shows a complete four-bit GaAs phase shifter with integral T/R switch. The circuit uses series loaded lines for the 22.5 and 45 degree bits, and a switched line configuration for the 90 and 180 degree bits. The relative phase shift over the frequency range of 5.3 to 5.9 GHz is shown in Figure 27 for each of the sixteen phase states. The RMS phase error from ideal over the above band and over all phase states is only 11.1 degrees. The phase shifter has a mean measured insertion loss of 7.5 dB with a deviation of less than ± 1.0 dB for any phase state. The complete circuit measures 8.00 by 8.26 mm with a thickness of 0.10 mm.

A monolithic high power transmit/receive switch is shown in the photograph of Figure 28. The single-pole, double-throw switch consists of a series FET in the transmitter branch and a shunt FET located a quarter wavelength away from the output junction in the receiver branch. The application of a sufficient negative gte bias to the FETs switches the transistors "off" and the T/R switch into the receive mode. Removal of the gate bias places the T/R switch into the transmit mode. The high power T/R switch has a measured insertion loss of less than 1.2 dB when in either the transmit or receive mode and provides 22 dB of receiver isolation during transmitting. The switch has been tested at power levels of up to 10 watts with no performance degradation. The circuit is 4.62 by 1.75 mm and is also 0.10 mm in thickness.

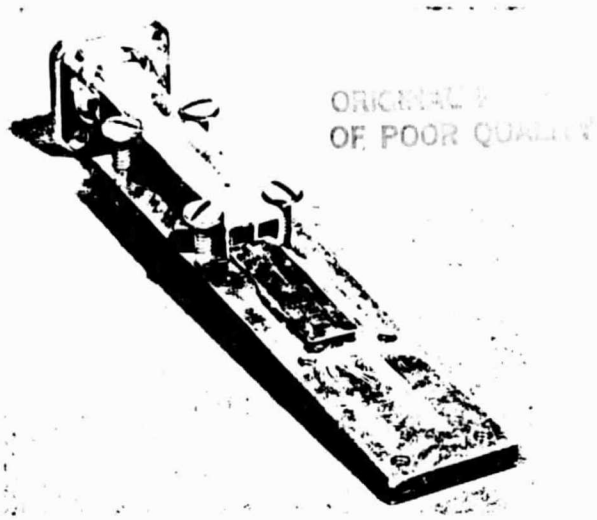

Figure 21. Ridged Waveguide to Microstrip Transistion

Figure 22. Printed Waveguide to Microstrip Transistion

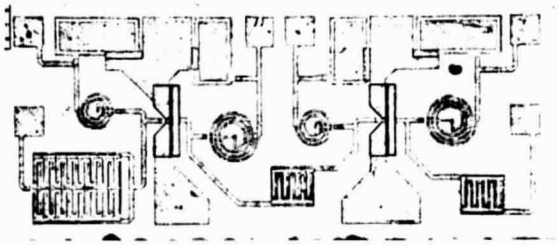

Figure 23. Two-Stage C-Band Low Noise Monolithic Amplifier
Chip Size: 0.89 x 2.29 mm

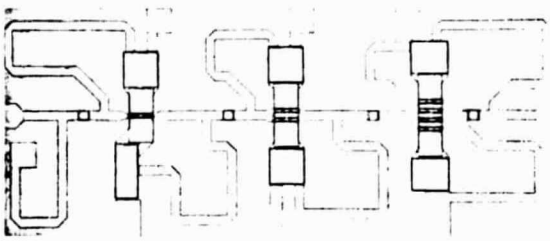

Figure 24. Three-Stage C-Band Driver Amplifier
Chip Size: 1.91 x 4.70 mm

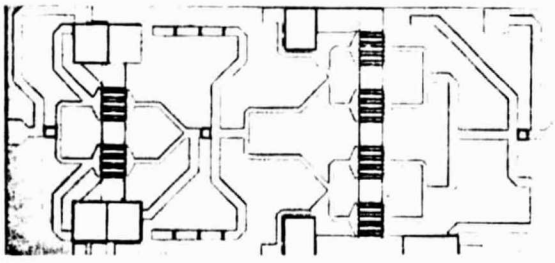

Figure 25. Two-Stage C-Band Power Amplifier
Chip Size: 2.16 x 4.83 mm

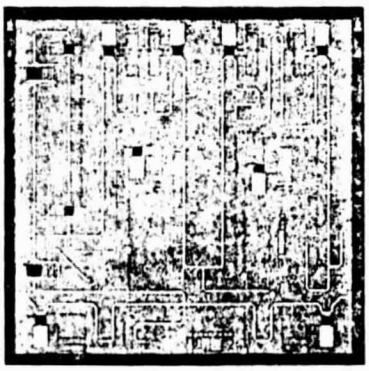

Figure 26. Four-Bit GaAs Phase Shifter with Integral T/R Switch
Chip Size: 8.00 x 8.26 mm

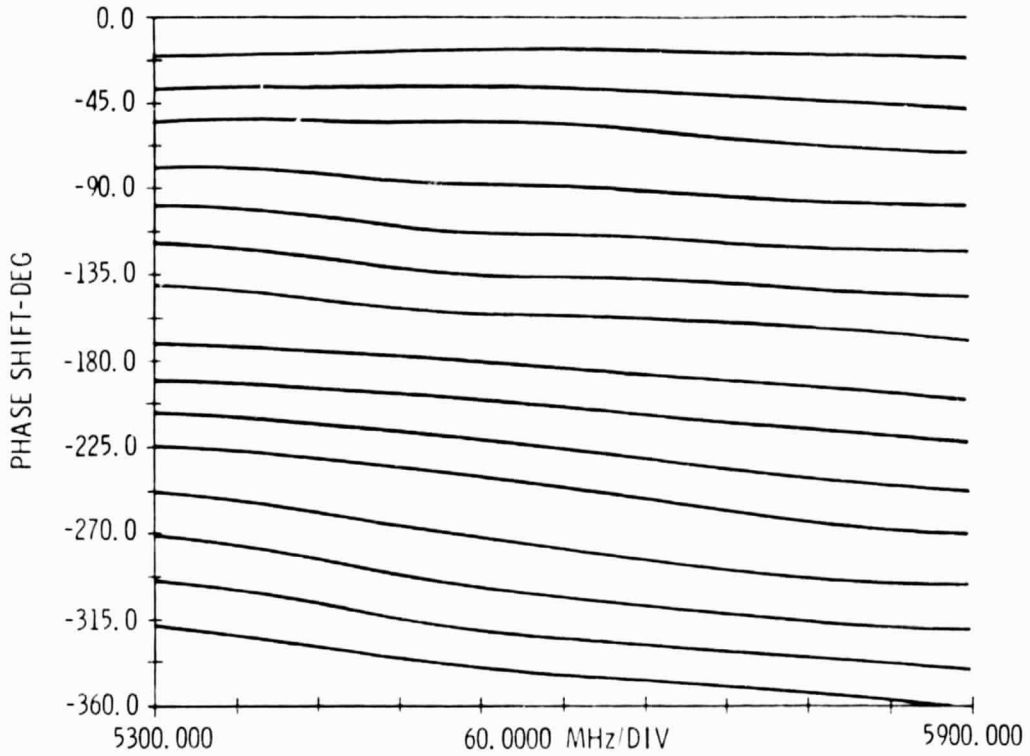

Figure 27. Relative Phase Shift as a Function of Frequency for the C-Band Monolithic Phase Shifter

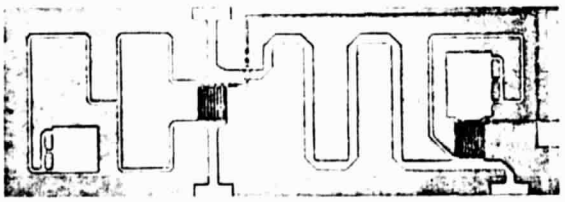

Figure 28. High Power Monolithic Transmit/Receive Switch
Chip Size: 4.62 x 1.75 mm

The degree of integration for monolithic microwave circuitry has been limited primarily by yield considerations[4]. Circuits with large areas have a proportionately higher probability of defects. Therefore, circuits such as amplifiers have been limited to a maximum of three and four stages. Indeed the most complex MMIC discussed above is the four-bit phase shifter with integral low power T/R switch. As processing techniques improve and material fabrication matures, the degree of circuit integration will increase. A suggestion pertaining to the possible integration of circuit functions would be the combination of the first stages of receiver low noise amplification with the high power T/R switch onto a single chip. One might also consider the inclusion of digital logic onto the phase shifter chip. Ultimately, a complete transmit/receive module will be fabricated on a single monolithic chip.

1.2.3 Packaging and Testing of Monolithic Circuits

A MMIC package or carrier should provide mechanical support for the fragile circuit as well as affording connecting terminals to the circuit's RF ports and DC/control lines. The carrier design should allow for testing of the MMIC before it is placed into the transmit/receive module, and once in the module housing the carrier should interface to other circuit carriers with minimal parasitics. Additionally, a method of fastening the carrier to the module housing must be provided. It is also desirable that the carrier design be universal in that a single design is amenable to a wide variety of monolithic circuits.

Many of the carriers reported upon for the mounting of MMICs resemble the packages used for power transistors. The circuit is bonded to a flange style base with alumina substrate microstrip lines providing connections for the RF ports and separate pads for the connection of the required DC voltages. The disadvantage of this style of carrier is that the flange mounting scheme results in the overall carrier size being substantially larger than the MMIC. Also the method for DC connections may not be optimum for application of the circuit in a T/R module.

A MMIC carrier in use at General Electric is shown in the photograph of Figure 29. The carrier base is machined from brass and is gold plated. On the top surface of the carrier a slot is machined with length and width corresponding to that of the MMIC chip. The slot depth is selected so as to make the chip top surface coplanar with the carrier and the alumina RF interconnecting boards. This feature facilitates making short wire bond connections from the circuit's RF ports to the interconnecting boards and if required, from the circuit's ground points to the metal carrier.

The alumina RF interconnecting boards have a 50Ω microstrip transmission line with a large bonding pad at the end. The large pad allows for the use of a greater number of wire bonds when interconnecting to other circuit carriers and helps compensate for the discontinuity at the carrier to carrier interface. Both the interconnecting boards and the MMIC chip are fastened to the metal carrier base with silver loaded epoxy. When maximum thermal conductivity between the circuit and the carrier is required, the chip should be soldered in place.

Connection to the circuit's DC power and control points are made via miniature feed-through pins which are soldered into the carrier base. These pins consist of a 0.46 mm diameter gold plated Kovar wire glass fitted into a 1.57 mm diameter gold plated Kovar eyelet. Wire bonds make the connection from the top of the feed-through pins to the MMIC. The circuit carriers are held into module housings by an 0-80 screw. A tapped blind hole is located in the bottom of the carrier for this purpose.

A hermetically sealed refinement of this circuit carrier, which is presently under development, is illustrated in Figure 30. The carrier base is gold plated Kovar which is flat on both the top and bottom surfaces. The Kovar material has a thermal coefficient of expansion which is well matched to that of alumina and GaAs. Feed-through pins for DC power and control line connections are fitted directly into the carrier base thereby eliminating the pin soldering operation. A one piece alumina interconnect board bonded to the carrier base is printed with microstrip lines for the RF interconnects. The size of the cut-out in this interconnect board can be varied so as to accommodate different circuit sizes with a single carrier design. The alumina has a thickness of 0.13 mm which is well matched to that of our GaAs circuits. A ceramic cover seals to all four sides of the interconnect board to complete the hermetic package.

An 0-80 mounting stud welded to the carrier base provides a means of fastening the circuit carrier to the module housing. With this arrangement, the MMIC carrier may be made much thinner than the present design which has a tapped hole for mounting. Therefore, not only is the weight of the carrier reduced, but the carrier to carrier interfaces are improved making the design usable up to higher frequencies.

A number of interesting circuit carriers are presently being developed for high speed digital integrated circuits[5]. Research is being devoted to improved substrate materials[6], chip bonding methods, and carrier hermetic sealing techniques. A number of the developments will be directly applicable to the packaging of monolithic microwave integrated circuits.

Monolithic circuits are characterized with respect to their RF performance before they are committed to a module. A simple, low cost test fixture for performing this function is shown in Figure 31. The MMIC carrier is held to the test fixture base with a single screw. SMA series connectors are mounted on end plates which attach to the test fixture base. The center pins of the SMA connectors make pressure contact on the RF microstrip lines and DC power is applied from the underside via the feed-through pins. The connectors shown have been found to have good performance and yield reproducible data at frequencies up through 16 GHz.

It is often desirable to test MMIC chips for their RF performance before they are mounted onto a carrier. Figure 32 shows a test fixture for this purpose which has been used for the evaluation of silicon-on-sapphire phase shifter bits. The test fixture consists of an upper and lower half. The MMIC to be tested is held into position in the lower half of the fixture by pressure on the chip's edges. The top portion of the fixture aligns with dowel pins to the lower half. Short probes soldered to the fixture's microstrip lines make contact to the MMIC's FF and DC pads. A set of these fixtures has been used to test over 5,000 circuits during a 3-month period.

For large scale production of MMICs it will be necessary to RF probe test circuits at the wafer level, i.e., before the wafer is separated into individual chips[7]. This technique has the advantage that bad circuits may be identified and dismissed before further handling.

1.2.4 Assembling MMICs into Transmit/Receive Modules

The extremely small size of monolithic microwave integrated circuitry makes possible the assembly of transmit/receive modules which may be located at each element of a phased array system. A block diagram of a typical module developed at General Electric for a C-Band Advanced Tactical Radar is shown in Figure 33. Functions within a dotted box represent those contained on a single monolithic chip. A four-bit bi-directional phase shifter provides element phase weighting during both transmit and receive modes. Transmit gain is achieved with a 3-stage driver amplifier cascaded with the parallel combination of four 2-stage power amplifiers. Pairs of power amplifiers are driven in quadrature to eliminate even mode reflections from their input and certain intermodulation products at their output. Each power amplifier is designed to deliver 2 watts of power output so that after combination and the insertion losses associated with the module front end, the net RF output power will be a minimum of 5 watts. Receive gain is provided by two cascaded 2-stage low noise amplifiers. The high power T/R switch provides 22 dB of isolation between the transmitter output and the receiver first low noise amplifier stage. During operation the receive stages are biased "off" when in the transmit mode and the transmit stages are biased "off" when in the receive mode.

The breadboard version of the C-Band module is shown in the photograph of Figure 34. The module assembly consists of the circuit carriers (described in Section 1.2.3) mounted into an aluminum housing. The DC power and control signal feed-through pins plug into a printed wiring board which is located on the underside of the module housing. The power/control lines are routed to a single multi-pin connector located on the housing end. Four-way Wilkinson dividers for transmitter RF power division and combination are evident in the photograph. These circuits are fabricated using a monolithic process on silicon-on-sapphire substrates.

Circuit carriers are butted directly together with the RF microstrip interconnects being made with multiple wire bonds. The use of multiple wire bonds reduces the equivalent series inductance of the interconnect thereby improving the electrical performance of the carrier to carrier interface[8]. An interconnect made with multiple bond wires will actually have less inductance and be mechanically stronger than one made with an equivalent ribbon.

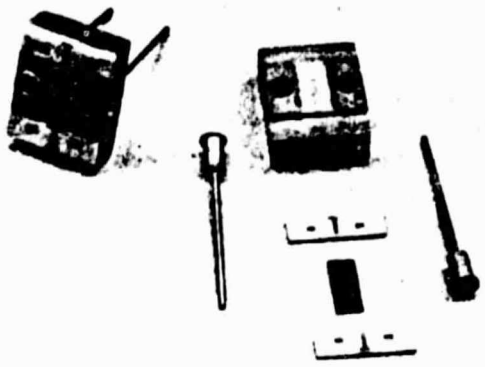

Figure 29. MMIC Carrier for Module Applications

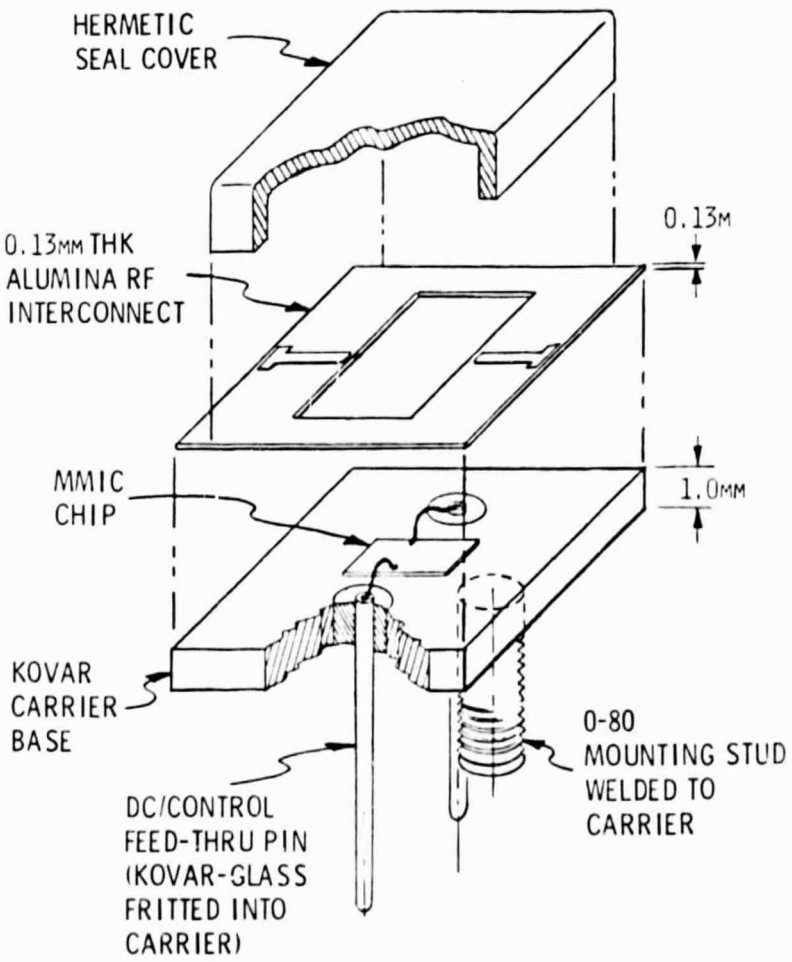

Figure 30. Hermetically Sealed MMIC Carrier

Figure 31. Low Cost Fixture for RF Testing Packaged MMICs. Usable Up Through 16 GHz.

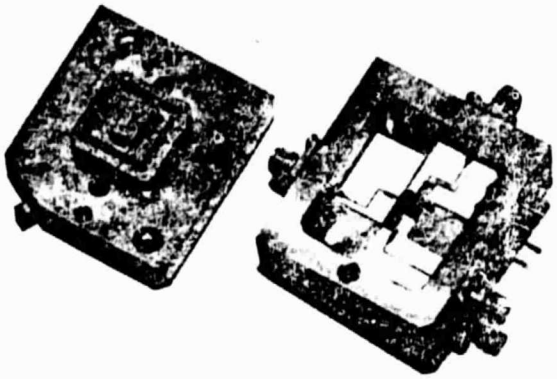

Figure 32. Fixture for RF Testing Unpackaged MMIC Chips

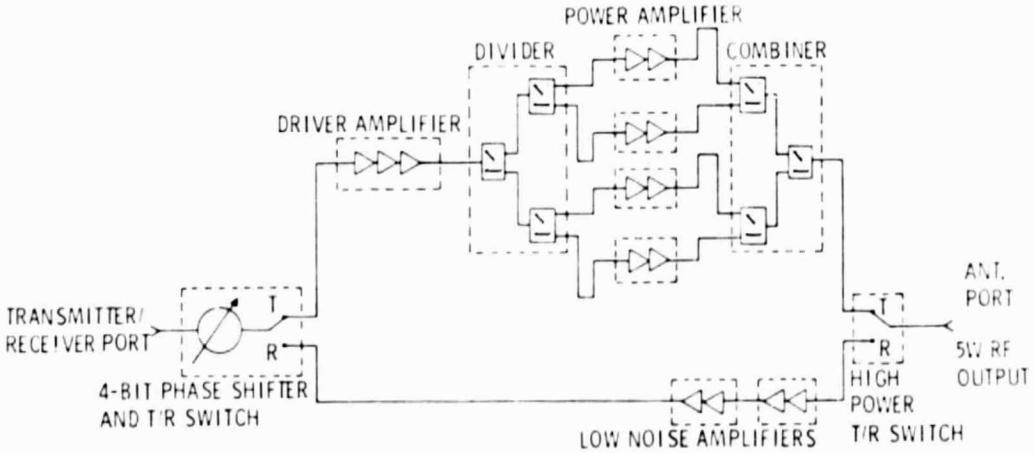

Figure 33. Transmit/Receive Module for an Advanced Tactical Radar

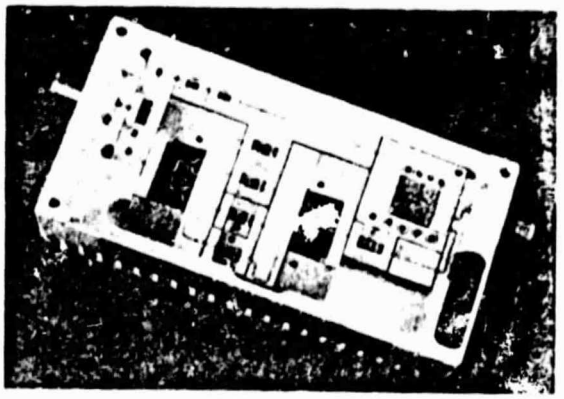

Figure 34. C-Band MMIC Transmit/Receive Module

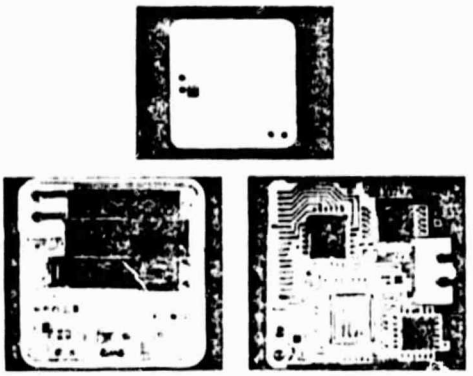

Figure 35. Phase Shift Module with Integral Controller for a Phased Array Lens Antenna

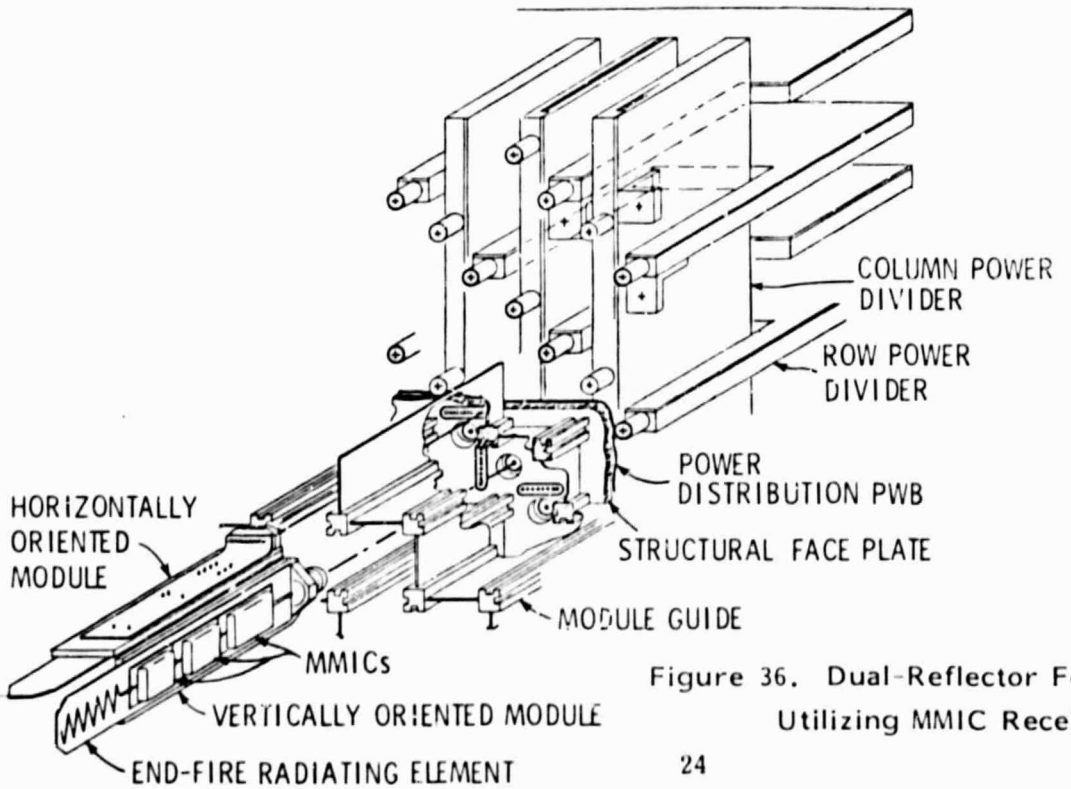

Figure 36. Dual-Reflector Feed Array Assembly Utilizing MMIC Receive Modules

To prevent low frequency amplifier oscillations, a large parallel plate chip capacitor is bonded to the amplifier carrier's top surface and wired in shunt with the amplifier's drain bias line. This capacitor is evident in the photograph of Figure 23. For maximum effectiveness the capacitor should be located as close as possible to the amplifier chip. Low frequency oscillations can be particularly detrimental in a T/R module since they may mix with the desired signal rendering in-band spurious signals.

The internal dimensions of the C-Band module housing were carefully selected so as to avoid in-band cavity resonances. For this particular module, the operating band is between the calculated first and second resonant modes. If any in-band resonances do occur, they can usually be eliminated by bonding a magnetically lossy material to the housing cover to suppress surface currents. The overall module size (83 × 41 × 25 mm) was selected so that unit would fit into the phased array element grid pattern. A thermal analysis was performed on the module housing to ensure that there existed adequate heat sinking for the power amplifier circuits.

The C-Band breadboard module has a measured net gain of 27 dB in the receive mode and 20 dB in the transmit mode. A prototype module now under development will integrate more circuit functions per GaAs chip thereby reducing the module part count and size. It will also include provisions for an integral module controller.

A transmit/receive module developed by General Electric for operation at S-band is shown in Figure 35. The module is comprised of a 4-bit phase shifter, two T/R switches, two stages of receive amplification, and three stages of transmit amplification. In this module package, DC power and control signals are routed in the same plane with the monolithic circuitry. The complete transceiver is approximately 13 × 13 × 25 mm in size.

A MMIC module for controlling the element phase in a space based phased array lens antenna is shown in Figure 36. The RF monolithic circuitry which is mounted onto one side of an alumina supporting substrate consists of a 4-bit phase shifter and two baluns for transitioning to the lens dipole radiating elements. An 8-bit microprocessor based controller system is located on the opposite side of the alumina substrate. The controller calculates the proper phase shifter state based on the element position, compensating for the spherical phase front incident upon the lens. The beam steering information is encoded in the RF signal sent by the main feed and is decoded by the controller. Plated through holes in the alumina substrate provide interconnection for the controller and RF circuitry. The entire module is only 25 × 25 × 3.6 mm in size.

1.2.5 Integration of Modules into Phased Arrays

The form in which transmit/receive modules using MMICs are integrated into a phased array will be dictated by the application and performance requirements for the phased array system. Some aspects of the array design that will be impacted by the use of MMIC modules and must be considered by the array designer include the type and media for the RF feed network, a technique for the distribution of DC power and control signals, a means by which the modules may be fastened into the array and be accessible for easy replacement, as well as a method for the removal of excess heat generated by the active circuitry.

A concept for the assembly of a 30 GHz active receive array to be used as the primary feed in a dual reflector satellite antenna is shown in Figure 36. Because of the high frequency of operation, the spacing between array elements is extremely limited. By orientating the modules in a longitudinal fashion as shown in the figure, it is possible to locate the active circuitry with each radiating element.

The array concept shown is actually two interleaved independent arrays, one horizontally polarized and the other vertically polarized. Grooved guide posts attached to a structural face plate are arranged in a pattern dictated by the element grid. The active module which consists of a low noise amplifier, variable gain amplifier, and phase shifter integrated with a printed end-fire radiating element is inserted between the guide posts in the appropriate vertical or horizontal orientation. The RF signal connection to the beam combining network is made with a plunge style connector having one part secured to the module and the mating part secured to the structurel face plate. The DC power and control signal connections are made via a multi-pin miniature connector secured in the same fashion as the RF connector. The vertical and horizontal beam combining networks are stripline dividers. Stripline circuitry has been selected because its self-shielding property will minimize the detrimental effects of transmission line radiation and coupling, and because of its wide flexibility with respect to combiner/divider design and line impedances. A printed wiring harness for the DC power and control lines is laminated to the back side of the structural face plate. A one piece protective cover fits over the array face.

Excess heat generated by the active circuitry is transferred by conduction from the module housing to the structural face plate. Heat pipes may be integrated into the face plate to efficiently conduct heat from the array to an external radiator[9].

An ECM phased array also assembled from modules orientated in a longitudinal fashion is shown in Figure 37. The array is comprised of eight row subarrays each consisting of eight elements. A subarray assembly contains two 4-way power dividers, eight wideband 2-bit phase shifters, and two beam steering computers. The beam steering computers are located on the bottom side of the subarray housing and are interconnected to the phase shifters via a multi-layer printed wiring board. A subssembly of eight end-fire radiating elements plugs into the row subarray with plunge style RF connectors. The row boards mate with column power dividers also through plunge connectors. The next iteration in the development of this array will include both a monolithic transmit and receive amplifier for each radiating element.

When a phased array system must be conformal, such as in airborne installations where the array must not alter the aerodynamic contour of the aircraft or intrude significantly into the aircraft structure, it is necessary to configure the transmit/receive circuitry along with the radiating element in a transverse fashion. To minimize the array depth, the radiating element, active RF circuitry, beam combining network, and logic control circuitry may all be located in a single plane or may be subdivided into multiple planes with the electrical interconnections between them. The feasibility of locating all the circuitry in a single plane which will result in the thinnest possible array, is dependent upon the element spacing, the size of the radiating element and active circuitry, and the type of beam combining network selected.

A 20 GHz conformal receive array presently under development is shown in Figure 38. A circularly polarized radiating element, low noise amplifier, and three-bit phase shifter are fabricated on a single GaAs substrate. This implementation reduces the number of RF wire bond interconnects that would be required with separate chips. Sixteen active elements are bonded to a thin alumina supporting substrate to form a four by four element subarray. This supporting substrate is suspended approximately $\lambda_0/10$ above a ground plane that serves as a reflecting surface for the radiating element. A series coupler beam combining network is located in the space between rows of radiating elements. The couplers' isolated port terminating resistors are implanted into the GaAs substrates and grounded with via holes. Multiple wire bonds interconnect the couplers and GaAs circuitry. DC power and data bus lines are printed onto the bottom side of the alumina supporting substrate. Interconnects to the GaAs circuitry are made via plated through holes.

It is also possible to update current phased array systems with monolithic circuitry for improved performance. Figure 39 shows an example of this concept where the horn elements of a waveguide fed 20 GHz transmit array have been replaced by active modules. Each module consists of a multi-stage 0.5 watt amplifier, a 5-bit phase shifte and a subarray of circularly polarized patch radiating elements. A microstrip to waveguide transition allows interconnecting the GaAs circuitry with the waveguide feed.

1.2.6 Radiating Elements for Integration with MMICs

A number of radiating elements including some novel implementations of classic radiators have been developed recently which are ideally suited for integration with monolithic transmit/receive modules. One type of element which has received much attention lately, particularly for application in conformal arrays, is the microstrip path[10].

Patch radiators are printed onto one surface of a dielectric substrate, while the other side is completely metallized to form a ground plane. The patch may take on various geometric shapes with rectanguar and circular being the most common. The radiator may be fed from the backside of the substrate by a coaxial line, by a microstrip line located on the same surface of the substrate as the patch, or excited as a parasitic element by a secondary radiator.

The half-power beamwidth and operating bandwidth of a patch element is a function of the dielectric constant of the substrate onto which the element is printed. For low dielectric constant substrates, the half-power beamwidths are in the neighborhood of 90°. The 2:1 VSWR bandwidth may range between 1 and 10% depending upon the substrate thickness. To increase the half-power beamwidth the physical size of the patch must be decreased by printing it onto a high dielectric constant substrate. This implementation, however, has an adverse effect on the element's operating bandwidth ranges from only 0.1 to 0.5%.

Basic patch elements produce a linearly polarized field pattern. Circular polarization may be obtained from a single-feed-point patch element by either slightly altering the shape of the radiator or by including capacitive or inductive elements in the structure so as to excite two orthogonal modes. The disadvantage of this technique is that the excitation of the two modes varies as a function of frequency. Therefore, the ellipticity of the polarization degrades rapidly off the element's center frequency. A 30 GHz single feed circularly polarized patch element fabricated at General Electric is shown in the photograph of Figure 40. This element is printed on a 0.43 mm thick GaAs substrate.

Circular polarization may also be obtained from a patch element by feeding it orthogonally with two lines from an external quadrature divider. If an isolated type of divider is employed, the element's bandwidth with respect to VSWR and pattern ellipticity may be increased. Signals reflected at the element feed points are dissipated in the quadrature divider's isolating load as opposed to being re-radiated at the opposite feed point. As a result, the input VSWR and polarization purity for the dual-feed circularly-polarized patch element can potentially be less frequency dependent than a comparable single-feed circularly-polarized patch. The disavantage of the dual-feed element is the additional area required for the external divider.

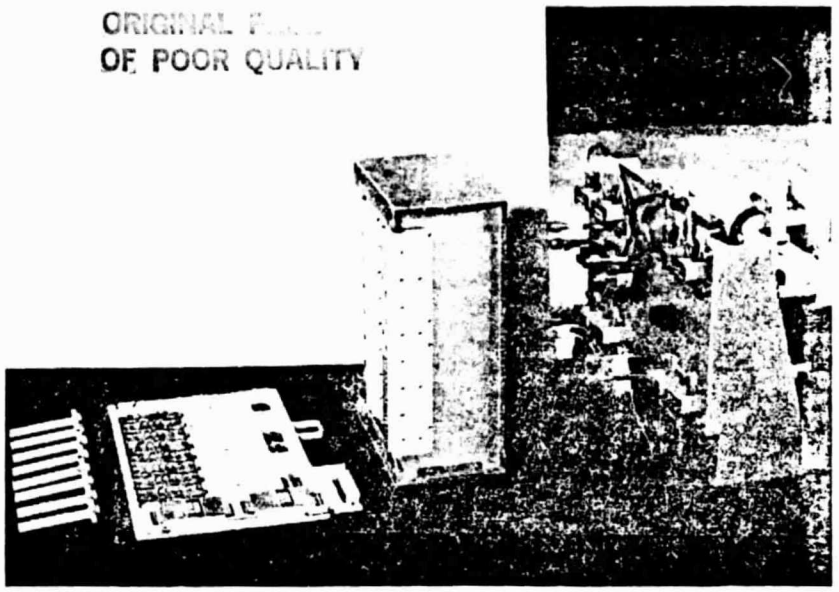

Figure 37. Wideband ECM Phased Array

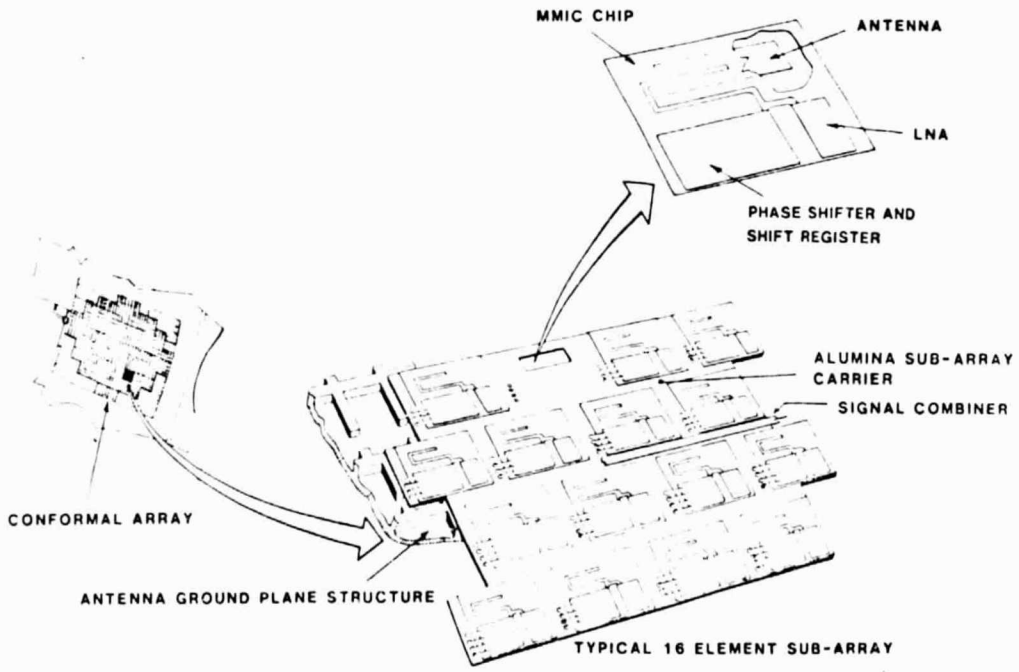

Figure 38. Conformal Receive Array Using Serial Beam Combining Network

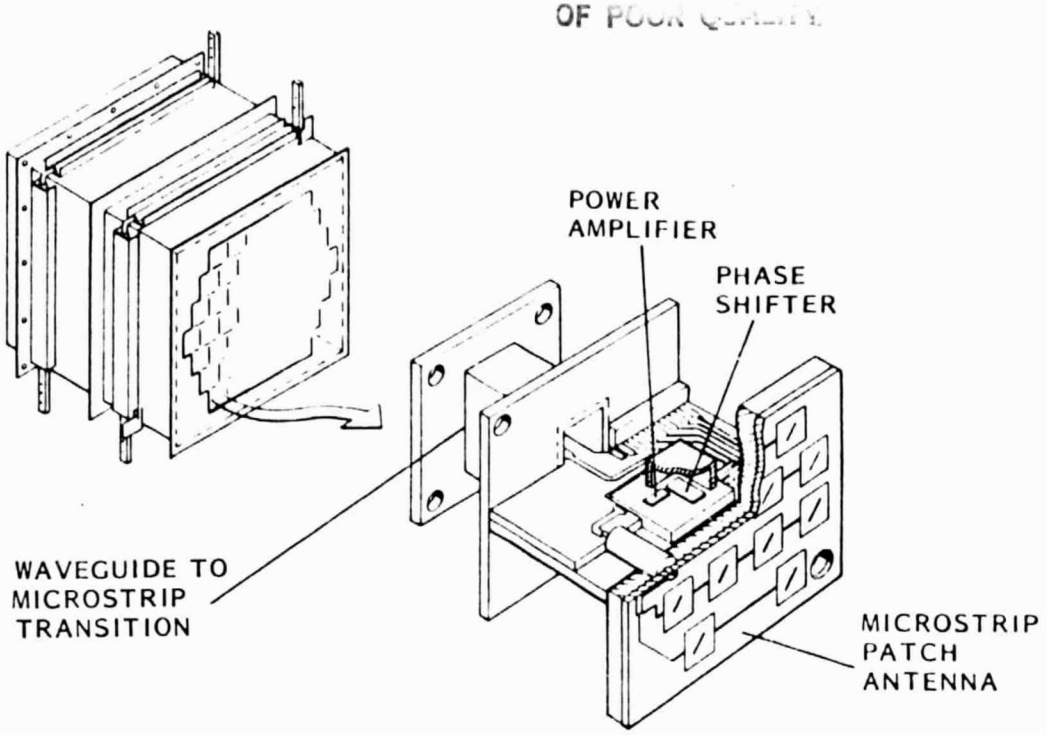

Figure 39. Waveguide Phased Array Updated with Active MMIC Modules

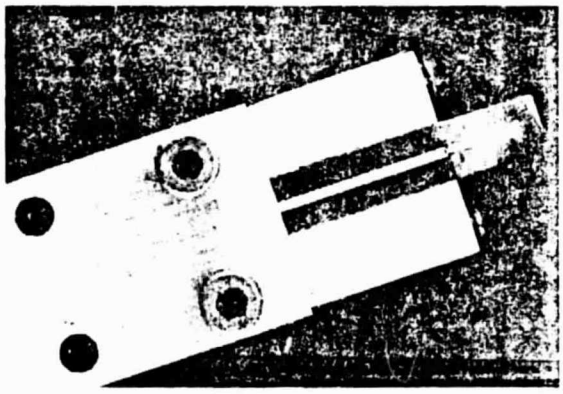

Figure 40. Single Feed Circularly
Polarized Patch Antenna Printed on GaAs

Dipole elements may also be printed onto a dielectric substrate and interfaced directly with monolithic circuitry. Figure 41 shows a 30 GHz fan or bow-tie type dipole antenna that has been fabricated along with a low noise mixer on a single GaAs substrate. A 100Ω balanced coplanar line interconnects the mixer diode with the feed point of the dipole. Future development efforts include the addition of a low noise amplifier between the dipole and the mixer. These integrated modules will be assembled into an array for a satellite communications uplink.

An interesting printed radiating element which can provide a broad main beam with circular polarization is a folded-dipole within an annular slot[11]. The element, as shown in Figure 42, consists of a rectangular slot radiator in the metallized surface of a dielectric substrate. Located within this slot is a printed folded-dipole radiator. A single microstrip feed line excites both the dipole and the slot. The continuous metallization that surrounds the element provides a ground plane for monolithic microstrip circuitry. The substrate is suspended approximately $\lambda_0/10$ from a second ground plane that serves as a reflector for the radiating element.

The area between the radiating element/circuitry substrate and the reflecting ground plane can be either left void or filled with a low-loss, low-dielectric constant material. The low radiation resistance normally associated with a dipole located close to a conducting surface is transformed to a higher value due to its folded nature. The transformation ratio may be tailored to a specific value by altering the relative widths of the radiating sections.

A photograph of an S-band slot-dipole developed at General Electric is shown in Figure 43. This element has an input VSWR which remains under 2:1 over a bandwidth of 11% with respect to its center frequency. Figure 44 shows the circularly polarized electric field components for the element operating at 2200 MHz. This cut is the E-plane for the folded dipole and the H-plane for the annular slot. The ellipticity ratio is essentially 3 dB or less for the sector of ±80° from broadside. This element design is being scaled for operation at higher frequencies.

Two types of elements that will provide linearly polarized end-fire radiation are the zig-zag[12] and the yagi. A zig-zag antenna is the two-dimensional equivalent of a helix. It may be printed onto a supporting substrate and fed directly with a microstrip line. The peak directive gain and operating bandwidth are determined by the element's section lengths, section pitch angles, and the total number of sections. A 30 GHz zig-zag antenna is shown in the photograph of Figure 45. This six-section example is printed onto a low dielectric constant woven teflon-glass supporting substrate. Measurements showed the element to have moderate gain (12 dBi) at its center frequency.

A ten element 30 GHz yagi antenna also printed onto a teflon-glass supporting substrate is shown in Figure 46. The driven element is fed by a coplanar balanced line. A reflector element is located on the backside of the substrate so as to avoid interference with the feed line. The parasitic element spacing and taper schedule were selected so as to achieve a moderate level (approximately 12 dBi) of relatively constant forward gain over a 12% bandwidth. The yagi antenna was found to have a wider gain bandwidth and lower cross-polarization components than the equivalent size zig-zag. Both the zig-zag and yagi designs were developed using method-of-moments modeling techniques.

A printed flared-notch element may be used to obtain end-fire linearly polarized radiation over a bandwidth in excess of 2:1. Figure 47 shows a flared-notch element that has been developed for use over the 8 to 18 GHz band. This microstrip fed element is printed onto a 0.25 mm thick alumina substrate. The shaded region of the photograph is the far side metallization showing through the alumina. The measured input VSWR remained generally under 2:1 over the entire 8 to 18 GHz band. Coupling for nearest neighbors in an array environment, whether colinear, broadside, or orthogonal, generally did not exceed 25 dB. The measured forward gain as a function oif frequency for an isolated flared-notch element is given in Figure 48.

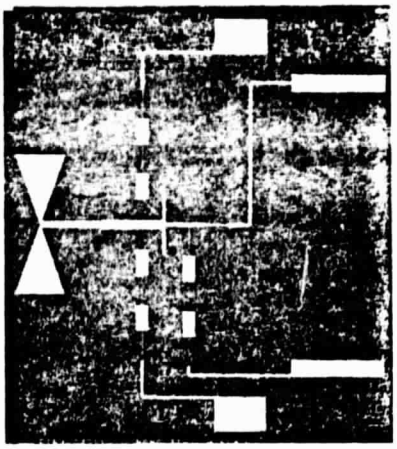

Figure 41. Bow-Tie Dipole with Mixer Circuit Fabricated on GaAs

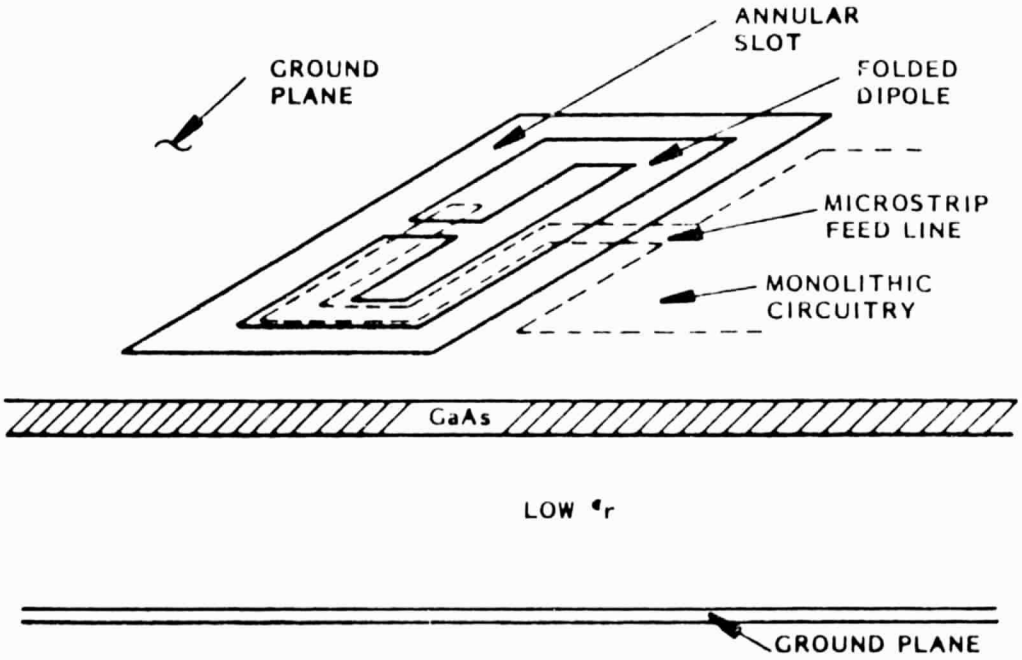

Figure 42. Printed Slot-Dipole Antenna for Broadbeam Circular Polarization

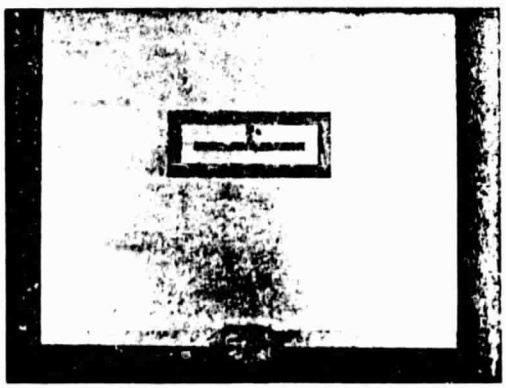

Figure 43. Slot-Dipole Antenna for S-Band

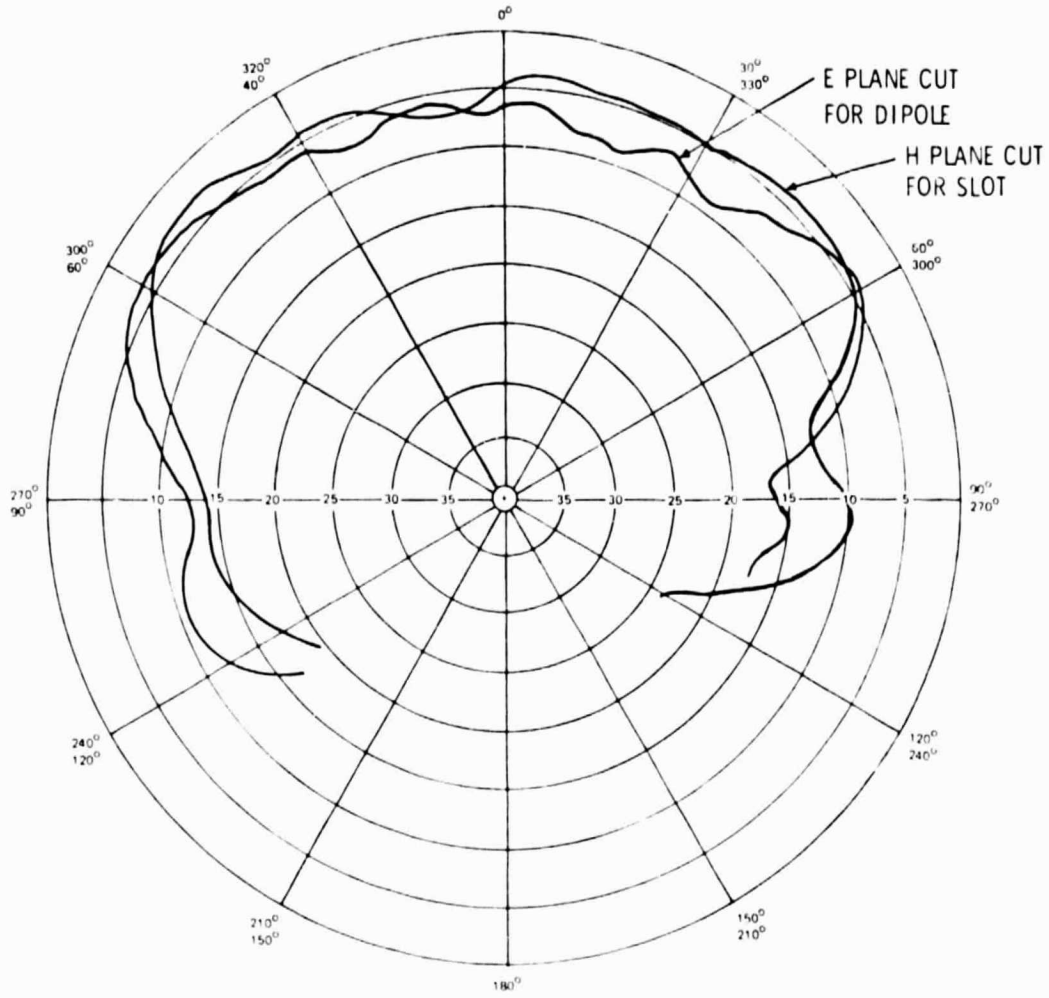

Figure 44. Electric Field Components for the S-Band Slot-Dipole Antenna Operating at 2200 MHz

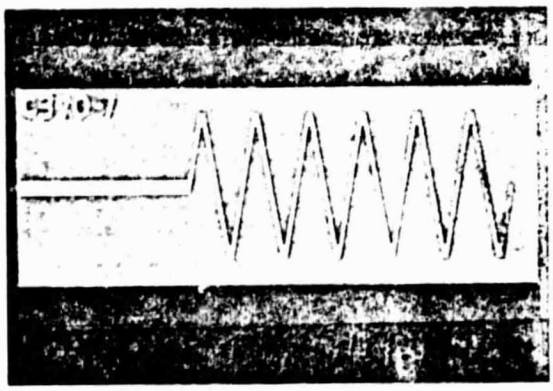

Figure 45. Six-Section Printed Zig-Zag Antenna for 30 GHz

Figure 46. Ten-Element Printed Yagi Antenna for 30 GHz

Figure 47. 8 to 18 GHz Notch Antenna
Printed on an Alumina Substrate

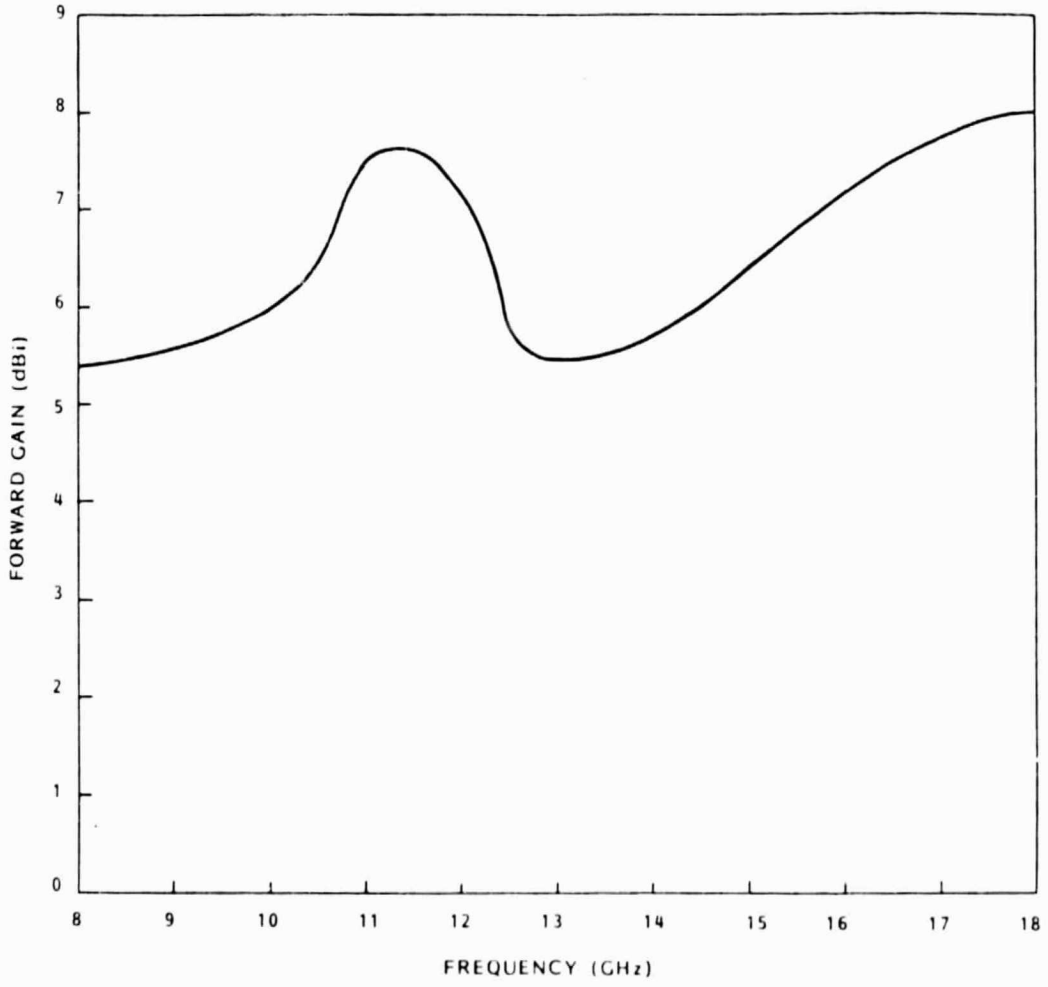

Figure 48. Measured Forward Gain vs
Frequency for Printed Flared-Notch Antenna

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2 TECHNOLOGY ASSESSMENT

2.1 HYBRID ANTENNAS

The requirements for lightweight antennas with low power-drain having low sidelobe performance and limited electronic scan capability for space systems applications have been responsible for recent advances in reflector antenna technology. These requirements have been addressed through two distinctly different approaches, viz.,

(i) Shaped reflectors (non-conic sections) with simple feeds,

(ii) Simple conical section reflectors with more complex feeds.

Beamscanning with reflector antennas (not having over-sized apertures) is generally limited to a few beamwidths if low sidelobes and high gain are to be maintained, due to the scan aberration incurred in a conventional reflector antenna design. Both approaches cited above effectively control the scan aberrations and thereby preserve gain and sidelobe performance over enhanced scan sectors; the first approach primarily by shaping the reflector surfaces and the second primarily by compensation in the feed array. Reflector antennas with phased array feed systems have been named "hybrid antennas."

Hybrid antennas largely obviate the need for any shaping of the reflector surfaces. In addition to compensating for the scan aberrations, hybrid antennas have been shown capable of compensating for other performance degradations commonly incurred in reflector antenna systems, including the following:

(i) Certain reflector surface errors,

(ii) Aperture blockage,

(iii) Feed defocus,

(iv) Feed pattern differences (mutual coupling effects in a small array),

(v) Element failure compensation,

(vi) Sub-reflector alignment errors.

Clearly, the feed array in a hybrid antenna provides superior design and performance advantages achievable beyond those provided by reflector shaping, while at the same time essentially accomplishing all that shaping the reflector accomplishes (but with a more complex feed array).

Also, the feed array design in hybrid antennas is able to take advantage of the emerging MMIC technology. The incorporation of MMIC technology into the feed array is expected to provide a wide range of phase and amplitude control, reduce power drain, increase reliability, and eventually reduce system costs. Maximum compensation of undesirable reflector characteristics by the feed array maximally exploits the MMIC implementation. The MMIC implementation provides excellent noise-figure performance in a receive antenna where a wider range of amplitude control is possible compared to a transmit array where power added efficiency become a critical performance measure.

U.S. organizations working on the design/development of hybrid antennas include:

*COMSAT

*FORD AERO

*GENERAL ELECTRIC

*HARRIS

*HUGHES

*JPL

*LINCOLN LABORATORY

*LOCKHEED

*MARTIN-MARIETTA

*NASA

*NRL

*RADC

*TRW

2.2 ASSESSMENT

- Requirements for space systems exist which can be met to advantage with hybrid antenna designs.
- Extensive development of hybrid antenna technology is in progress.
- MMIC technology is applicable to hybrid antenna implementation with significant advantages for space systems.
- Hybrid antennas with MMIC implementation will be deployed in space systems within the decade.

3 DUAL-REFLECTOR ANTENNA TECHNOLOGY FOR HYBRID ANTENNA DESIGNS

There are two major categories of hybrid antennas; viz.,

1) Focal plane feed array design,

2) Aperture-image plane feed array design.

The focal plane feed array design is ideally an amplitude-only control beamsteering system; i.e., the scan excitation of the feed array is equivalent to moving a feed horn across the focal surface of the reflector to accomplish beamsteering. In actual practice, to correct for scan aberrations, more than one feed element must be used to form a beam, and both amplitude and phase control must be used to scan the beam. The fact remains, the focal plane array design does require large variations in feed excitation to scan the beam. Intentional feed defocus has been used to reduce the required range in amplitudes. To perform beamsteering efficiently in a transmit array, variable power dividers after the final power amplifier can be used. These power dividers must be of high power and low loss design. Such variable power dividers have been incorporated in phased-array feeds for antennas used in space systems, but they are not suitable for MMIC implementation where the final power amplifiers must be at the feed elements to realize high transmit power at reasonable transmitter efficiencies. Also, transmit feed arrays with distributed power amplifiers have been designed for hybrid antennas using uniform power combiners and on-off power amplifiers to achieve the desired amplitude control with acceptable transmitter efficiencies. Nevertheless, the focal plane array design is best suited to receive array applications where low-noise pre-amplifiers can be used to compensate for the loss in a simple uniform-combiner thereby preserving noise-figure performance in the receiver. The low power operation of the receive circuits subordinates the drive power issue for amplitude control in a receive-only system.

The focal plane array design is applicable to single reflector antenna systems. However, dual-reflector systems have been used to achieve the benefits of a large effective F/D ratio without incurring the penalty of an increase in physical dimension of the antenna (length in the axial direction). The F/D ratio of the principal reflector is increased by the magnification of the dual reflector system. The usual configuration is a Cassegrain system consisting of a paraboloid for the sub-reflector. It is possible to use other reflector pairs for a dual-reflector system (such as a confocal ellipsoid instead of the hyperboloid for the sub-reflector), but generally without advantage, and sometimes with disadvantage as greater length for the alternative cited.

The aperture-image plane feed array design is ideally a phase-only control beamsteering system. It is intrinsically a dual-reflector system. The sub-reflector images the main reflector onto the feed array, or conversely the feed array onto the main reflector. Thus, the magnitude of the aperture illumination across the main reflector is ideally the same in form as the magnitude of the feed array excitation. In actual practice, the imaging is only approximate so that both amplitude and phase control are needed to beamsteer while correcting for scan aberrations of the system. However, the amplitude variations required for beamsteering the aperture-image system is significantly less than for the focal plane system. This fact makes the aperture-image design attractive for transmit arrays where the quasi-static excitation amplitude is favorable to an efficient and simple transmitter design; e.g., a weighted power divider for the nominal amplitude weights, a variable gain power stage of modest range for amplitude trimming, and the beamsteer-steering phase shifters. Also, since all elements are excited for each beam, the number of elements contributing to a beam is much larger for an image-plane design than for a focal plane design. This fact is favorable to high transmit power in MMIC implementations with the image-plane design (since radiative power addition is achieved). In contrast, the use of all feed elements for each beam in the image-plane system represents a problem for a scanned multi-beam transmit array since the amplitude variations of the composite excitation for the feed array has large variations as the beams are scanned. The power efficiency advantage of an image-plane transmit design over a focal plane design is lost in this case.

The magnification of the dual reflector system for an aperture-imaging design determines the size required of the feed array (and the size or number of the feed array elements to avoid grating lobes for the scan angles required). Assuming a paraboloid for the main reflector, the sub-reflector can be a paraboloid, ellipsoid, or hyperboloid. The feed array is located such that a ray from the center of the feed to the center of the main reflector strikes the sub-reflector at a point which has the same radius of curvature as an ellipsoid with foci at the two centers. Generally, the ellipsoid sub-reflector is the smallest while the hyperboloid sub-reflector results in the shortest axial length. (NOTE: the hyperboloid design uses the branch of the hyperboloid concave toward the feed array.)

ASSESSMENT

- The focal plane array is an excellent design for a multi-beam scanned receive antenna,
- The aperture-image array is an excellent design for a single scanned beam or multiple fixed beam transmit antenna,
- The focal plane and the image-plane array designs are competitive for scanned multi-beam transmit antennas,
- MMIC implementation is an asset to either the focal plane or the aperture-image plane designs,

- Single reflector designs are suitable for focal plane antennas,
- Cassegrain designs can be used to advantage if the axial length of the antenna is critical in a focal plane hybrid antenna,
- Gregorian designs are the most highly developed version of the aperture-image hybrid antenna, although a hyperboloid sub-reflector could offer a length advantage.

4 FEED ARRAY ANTENNA TECHNOLOGY

Feed arrays are used with reflector antenna systems to correct for scan aberrations. The problem of determining a low-sidelobe, high efficiency feed array excitation is a synthesis problem. The synthesis of the feed array excitation has been performed by different investigators in various synthesis domains: viz., far-field synthesis, aperture synthesis, and focal-plane (or image-plane) synthesis. In each case, the complex excitation of the feed array is optimized for the low-sidelobe, high efficiency specification of the resultant electromagnetic field across the synthesis domain (e.g., a circular Taylor pattern in the far-field, a circular Taylor distribution in the aperture, or the aberrated transform of a circular Taylor distribution in the focal plane) the far-field pattern synthesis has several distinct advantages. First it is the most direct performance measure (in terms of both specifying the desired result and measuring the quality of the synthesis). Second, the far-field synthesis can correct for all major degradation factors; i.e., in addition to reflector aberrations also aperture blockage, reflector deformations, reflector misalignments, feed array defocus, etc.

The synthesis techniques that have been applied to feed array excitation synthesis in reflector antenna systems include Fourier synthesis, min-max/max-min search, and maximum likelihood. The maximum likelihood technique for feed array excitation synthesis provides significant advantages and versatility.

Maximum likelihood synthesis results in the minimum weighted-average sidelobe level over the sidelobe control region. For any selected control region and set of sidelobe suppression weights, a universal optimum (in contrast to a local optimum) solution is obtained. Main-beam gain constraints can be imposed, with the maximum gain excitation a special case of the general solution. Sidelobe suppression can be applied to both spot and area control regions. Reiterative techniques allow gain and beamwidth trades against sidelobe levels. Also reiterative techniques can reduce the spread between peak and average sidelobes at the expense of increased average sidelobes. The excitations derived by the maximum likelihood method are scan-interpolatable, resulting in a simplified beamsteering computer. The maximum likelihood synthesis allows compensations for mutual coupling effects (different element patterns in the feed array), scan aberrations, reflector deformations, reflector misalignments, feed array defocus, and aperture blockage. The maximum likelihood synthesis technique is applicable to experimentally characterized hybrid antenna systems (i.e., reflectors with array feeds). For these reasons, the maximum likelihood excitation synthesis technique has been found to be a superior method for determining the performance/design trades of hybrid antennas relative to their feed array excitations.

5.0 OFFSET REFLECTORS VERSUS PHASED ARRAYS

In order to justify the use of a dual offset reflector antenna system, it must be compared to alternate implementations. The primary goal of this study is the application of MMICs to antennas. Therefore, the choice of a direct radiating phased array antenna is a logical alternative. Because there are many controllable elements present, a phased array, in principle, gives more freedom to the designer to shape the characteristics of the illumination function and hence obtain better performance. However, a number of other problems arise that must be considered in a comparison; viz., weight, loss, control, number of elements, and grating lobes. These tradeoffs will be discussed in the following section.

In order to meet the 56 dB gain requirement, the direct radiating phased array must be a large array, approximately 9 feet, or 260 wavelenths in diameter.

An important part of an array is the feed network, which may fall into two basic types - constrained feeds and optical feeds.

Constrained beam combining networks use transmission lines between the input and each element in the array. A great deal of design control over the static amplitude of each element can be exercised, but care must be used to avoid compounding mismatches. Since the size and complexity of the network increases with array aperture, the insertion loss and weight also increase.

This fact can be illustrated by means of a simple example. If one assumes the direct radiating array and the reflector feed array have the same number of elements, with the direct radiating array having an element spacing equal to the magnification factor times the feed array element spacing, the direct radiating array beam combining network will be an enlarged version of the one used in the feed array. For a typical magnification factor of 6, this enlarged version will be 36 times as large in area - this results in a weight increasing from 2.51 Kg to 903.6 Kg for the beam combining network alone. The associated DC and control lines also must increase in length, and in some cases gage, resulting in further weight increases.

The insertion loss of the transmission line is directly proportional to its length. Therefore, if the area the beam combines must cover increases, the loss of the beam combiner is going to increase. The result of this is either a less efficient array or more amplifiers required to compensate.

The simple example of the same number of radiating elements in the direct radiating array and the reflector feed array shows a clear difference. If one were going to realistically design a direct radiating array, the number of elements required would, in general, be greater than for a reflector feed array. This increase further increases the weight disadvantage. The greater number of elements is required to prevent grating lobe formation. With a reflector feed array, the grating lobe problem can be avoided by using a focal plane feed array or can be suppressed by using focal plane "stops" in an aperture-image feed array.

To keep grating lobes off the earth for a regular grid of elements in a direct radiating array, approximately 3500 elements would be required - compared with about 600 elements used in a focal-plane feed array. Alternatively, the grating lobes could be allowed to "form" on the earth provided the grating lobe energy were diffused through the use of non-periodic element spacing and suppressed by constraining the grating lobe to the sidelobe region of the radiating element. For example, concentric circular ring arrays for the elements can be used to avoid periodic element spacing.

Grating lobe suppression by 30 dB, with acceptable aperture efficiency is possible, but even so the direct radiating array will require more elements than the feed array since the grating lobe energy must be kept well out of the main lobe of the element pattern. Such diffusion of grating lobe energy nullifies one of the major perceived advantages of the phased array; viz., superior sidelobe control.

An alternative to the case just discussed is for the confluence of transmission lines from the phased array geometry to an equivalent feed array to be accomplished at IF rather than RF. The loss is less of a consideration at the lower IF frequency, but the weight disadvantage is aggravated, since in this case not only does the IF confluence of waveguides exact a weight penalty, but there is a like penalty on the distribution network for the LO power across the large phased array structure, since down conversion must take place at each element.

Another alternative would be to use a space feed. This may be more economical in mass, cost, and insertion loss. It could take the form of a reflect-array or a transmission lens type. Since the primary feed is responsible for the array illumination, it becomes more difficult to achieve the amplitude illuminations that are required for low sidelobes. The sidelobe performance can be improved by employing a complex of several feed elements at the primary focus, though this approach required a treatment of near field diffraction. In addition, care must be taken not to allow a high spillover loss. It is possible for the spillover loss to approach the loss of a constrained feed.

The F/D ratios of space feeds are typically on the order of 1. Hence, given the added complexity and questionable performance increase, it would seem that a phased array reflector system would be preferred.

In general, due to the greater weight and higher losses of a direct radiating phased array compared to a reflector antenna with a smaller phased array feed the direct radiating phased array is not suited for this application. If the requirements were a wide angle scan, this conclusion might be different.