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A New Very High Voltage Semiconductor Switch

(NASA-TM-86957) A NEW VERY HIGH VOLTAGE
SEMICONDUCTOR SWITCH (NASA) 17 p
HC A02/MF A01 CSCI 09A

N85-20246

Unclass

G3/33 14420

Gale R. Sundberg
Lewis Research Center
Cleveland, Ohio



Prepared for the
Sixteenth Annual Power Electronics Specialists Conference (PESC)
sponsored by the Institute of Electrical and Electronics Engineers
Toulouse, France, June 24-28, 1985

NASA

A NEW VERY HIGH VOLTAGE SEMICONDUCTOR SWITCH

Gale R. Sundberg
National Aeronautics and Space Administration
Lewis Research Center
Cleveland, Ohio 44135

SUMMARY

A new family of semiconductor switches using double injection techniques and compensated deep impurities is described. They have the potential to raise switching voltages a factor of ten higher (up to 100 kV) than p-n junction devices while exhibiting extremely low (or zero) forward voltage. Several potential power switching applications are indicated.

INTRODUCTION

A new family of semiconductor devices is being developed based on bulk effects of deep energy level impurities, such as gold and electron radiation, in silicon, gallium-arsenide and silicon-germanium alloys. These deep impurity semiconductors represent a departure from traditional p-n junction devices. The deep energy-level impurities enhance active-charge dynamic interactions in the midrange of the semiconductor bandgap, aside from simple bimolecular recombination. The initiation and control of these bandgap interactions, which are being investigated, expand the range of device applications as compared with ordinary p-n junction devices (refs. 1 to 4).

These new semiconductors have the potential to raise the switching voltage a factor of ten higher than p-n junction devices while exhibiting extremely low (or zero) forward voltage. Figure 1 illustrates the possibilities based on early theoretical studies, but confirmed by actual experimental data as shown. The practical upper limit appears to be nearly 100 kV.

The new Double Injection, Deep Impurity (DI)² semiconductor switches depend on the trapping characteristics of compensated deep impurities near the midpoint of the energy bandgap in a bulk semiconductor under double charge injection at the electrodes. Recent studies of gating phenomena give evidence for many potential circuit applications for the (DI)² switch because of its thyristor-like switching characteristics. Figure 2 depicts a generalized volt-ampere characteristic curve showing the switching effects using two types of gates. The MOS gate alters the threshold level, and the injection gate modifies the holding voltage, either pushing it toward zero or toward higher voltage to assist turn-off, depending on gate polarity. Thus, high voltage, very low forward drop, gate turn-off switches appear feasible.

At present, work is underway to develop (DI)² devices capable of blocking 1 to 10 kV and handling 1 to 10 A (ref. 5). Manufacturing feasibility of a 2000 V, 2 A (DI)² switch was recently demonstrated. Solid state switch-gear using such devices rather than conventional semiconductors may be much more efficient, more versatile in spacecraft applications, and much smaller and lighter weight (ref. 6). In addition to switching high voltage and power, many other deep impurity devices based on suitable manipulations of the topology, processes, and bandgap interactions are possible. For example, a wide

selection of switching devices operating down to TTL voltage levels and IC devices providing voltage controlled delays (from microseconds to nearly a second) have been demonstrated. The new semiconductor family also includes several very sensitive, microelectronic gas-flow, temperature and magnetic field transducers, and some extrinsic infrared and optical detectors (ref. 7).

This paper will describe some of the latest developments and innovations in this new family of semiconductor devices. Primary emphasis will be on the (DI)² switch technology for switching applications in power electronics for both aerospace and terrestrial power systems.

(DI)² IN SILICON

The (DI)² semiconductors described in this paper incorporate deep impurity levels compensated by shallow impurities in the intrinsic (or bulk) region to provide the basis of operation. Figure 3 shows a cross section of a simple, planar (DI)² device (ref. 8). The bulk material is gold-doped silicon, compensated by a shallow donor such as phosphorus. The anode and cathode are formed by diffusing p⁺- and n⁺-regions into the bulk material. These regions provide efficient ohmic contacts and the appropriate band bending at the surface to promote high level injection of both holes and electrons.

The lower portion of figure 3 shows an energy level diagram of the compensated, gold-doped device. The n-type shallow impurity effectively moves the Fermi level to the gold acceptor level at -0.54 eV. This compensates the trap in such a manner that it will accept and hold an electron or hole and empty only when gated, that is, by the effect of high induced fields rather than thermally. Had a p-type shallow impurity been added to the gold-doped bulk silicon the gold donor level at 0.35 eV would have been activated and dominated the device behavior.

Most of the work to date has involved the gold acceptor level near the center of the silicon band gap at 0.54 eV below the conduction band. Gold was selected because of the relative ease of diffusion and the vast amount of literature available. Thallium, zinc, and cobalt have also been studied in some detail. Considerable effort is also being focussed on electron irradiation with subsequent annealing as a method of introducing and controlling several deep levels.

In the gateless (DI)² diode, switching occurs when the applied voltage exceeds a threshold voltage, V_{TH} . Operation actually begins with high level injection primarily of electrons as voltage is applied across the electrodes. Since the deep traps of a compensated material as in figure 3 are negatively charged, they form giant coulombic traps that provide recombination sites for holes. The off state is governed by the simple ohmic resistance of the bulk material (usual greater than $10^5 \Omega \text{ cm}$ for gold-doped Si) and ultimately by an electronic space charge near the cathode. This is much like a typical vacuum tube.

Switching occurs as the voltage is increased and the injected holes neutralize the negative deep traps and allow a rapid transit of holes across the channel length. This happens when the hole transit time equals the off-state hole lifetime and the negative space charge is neutralized. This leads to the characteristic s-type switching phenomenon as shown in figure 4.

The current-voltage curves of the (DI)² devices are typically characterized by a threshold voltage, V_{Th} , followed by a negative resistance region and resulting in a high current region with a holding voltage, V_H , as shown in figure 4. The threshold and holding voltages are simply proportional to the square of the separation length (L) between anode and cathode and are primarily dependent on the deep impurity concentration. It has been shown that a very short hole lifetime results in a high value of V_{Th} and a short transit time under switching conditions. These characteristics have been studied and modeled by Lampert and Mark (ref. 9) and by Ashley and Milnes (ref. 10).

The square law dependence of V_{Th} and V_H involves respective proportionality constants for a given bulk material that depends on trapping cross section, thermal velocity, trap concentration, and hole mobility. This dependence has been verified experimentally up to 2 kV at channel lengths of 1.0 to 1.5 mm. Bulk avalanche breakdown determines the limiting value of V_{Th} . Theoretically, the proportionality constant can be scaled by trap concentration until the fundamental limit is reached. Fifty to 100 kV appears to be, however, a practical upper limit for a single device made of Si or GaAs.

When the (DI)² switch is in the ON state, plasma filaments that are essentially neutral are formed in the channel. The ON state regime is designated "c" in the curve of figure 4. This filamentary plasma may have densities as high as 10^6 to 10^7 A/cm². In typical devices, however, with channel lengths less than 0.1 mm the current densities are generally in the order of 10^3 A/cm².

The device current may, in principle, be scaled up as a function of the electrode area. The ON state holding voltage, V_H , of the plasma, however, is dependent on the channel length. Thus, individual plasma filaments will be struck wherever the microscopic interelectrode spacing is a minimum or field concentration is highest. It has been shown (ref. 4) that shaped small protrusions within the electrodes can provide preferential locations for plasma filament formation. This spreads the filaments throughout the channel in a predictable manner, preventing hot spots and increasing the current handling ability. With reasonable care in the design and fabrication current levels in the tens to hundreds of amperes should be possible.

Several electrode configurations and topologies have been investigated. For example, the placement of an n^+ diffusion guard ring around the anode increased V_{Th} and decreased V_H (11). The most significant development in improving electrode efficiency is the shorted anode double injection switching (SADIS) electrode (ref. 12). This electrode commonly referred to as a symmetrical or Shieh electrode is shown in the circular lateral device of figure 5. In this device both electrodes are symmetrical, that is, they have an n^+ region surrounding the p^+ region.

The SADIS electrode decreases the hole injection efficiency in the pre-breakdown regime at the anode. This increases V_{Th} . This electrode allows more negative space charge buildup, since sufficient holes are not available to neutralize them. Hole injection will be inhibited until the channel bias voltage exceeds a diode drop, which is developed by electron current flow through the internal resistance near the anode. This electrode combined with a circular topology as in figure 5 has demonstrated a $V_{Th} = 2$ kV and currents up to 2 A in subsequent work to that reported in reference 5. Some typical response curves are shown in figure 6 for one of the experimental devices operating at $V_{Th} = 1350$ V and a current of 425 mA at a holding voltage of

80 V. This is an early device with no gates. With only minimum heat sinking, currents in this type of $(DI)^2$ switch have been pushed over one ampere and pulsed to 10 A. Work continues in many areas to reduce the holding voltage by process improvements, topology variations, modeling, and addition of gating electrodes.

SWITCHING PRINCIPLES

There are numerous gating schemes possible for $(DI)^2$ devices. Typical gating can be any combination of optical, current injection or MOS. Most work to date has involved electrical gating of the injection or MOS type. For fast, high voltage switching, however, optical triggering may be preferred.

In the the $(DI)^2$ device optical gating is obtained by extrinsic ionization (or deionization) of the active impurity rather than electron-hole pair creation (ref. 13). The time response of the optical gating is determined by the product of the optical capture cross section and the photon flux. Multiple internal reflection techniques and selection of light of appropriate wavelengths can improve the response. Photon capture is maximized at energies in the range of 1.5 to 1.7 times the separation energy between the deep level and the band edge. For fast switching a topology should be chosen to provide complete illumination of the channel in order to affect all the charge states nearly simultaneously. Figure 7 shows a V-groove method of light gating of a conceptual $(DI)^2$ switch.

For a planar $(DI)^2$ device topology an MOS gate is strategically placed near channel center and constructed so that a voltage may be applied across a thin oxide of about 1200 Å. The current-voltage characteristic and a specific experimental design of a MOS-Gated device are shown in figure 8 (ref. 4). The MOS gate triggers the device ON when a positive pulse (V_{GC}) is applied to the gate. As shown in the diagram, a negative voltage raises the threshold voltage, V_{Th} . Even with the gate attached to the cathode and $V_{GC} = 0$, V_{Th} is nearly doubled over a similar device without a MOS gate.

Modeling of the effects of MOS gates indicate that the gating effect is caused by bending of energy bands near the surface (ref. 4). Applying a large, positive V_{GC} bends the bands downward fully ionizing the gold acceptors. Conversely, applying a large, negative V_{GC} leads to fully neutralized gold levels by bending the energy band upward. As the neutral gold levels increase, a barrier for electron current is formed pushing the current path into the bulk and away from the surface. This leads to a saturated high threshold voltage. Tuntasood (ref. 4) has calculated that the MOS gate influences current flow into the bulk 3 to 4 μm . A negative V_{GC} pushes the hole current away from the surface and into the bulk.

Injection gates are formed by diffusing in a p^+ or n^+ region in the channel between anode and cathode. Figure 9 shows a planar $(DI)^2$ switch with an injection gate. Injection gates have been shown to control V_{Th} (ref. 2), V_H (ref. 3) and the onset of N-type switching in the negative resistance region (ref. 14). This N-type characteristic is of interest for oscillators and certain sensors, but will not be discussed in detail in this paper on power switching devices.

Most of the investigations using injection gates have used p^+ hole injecting gates. Figure 10 shows some very remarkable results with the superposition of several oscilloscope traces of switching in a $(DI)^2$ injection gated device (ref. 3). As the gate-to-cathode voltage is made more negative (in -4 V increments) the holding voltage, V_H , is decreased toward zero. This represents the very intriguing possibility of a zero forward voltage switch. In this small, planar device significant gate power was required to move V_H . More recent devices have reduced the inherent V_H by factors of 4 or 5 and have cut the required gate power such that ON state power gains of 10 or more now appear feasible.

The placement of the gate in the central region of the channel gives it maximum sensitivity. Lampert (ref. 9) has shown that the peak field in the channel of a DI device moves to channel center at the onset of high conduction. Increased hole injection from the gate suppresses the negative space charge in the gate region and moves the point of charge neutrality toward the center (ref. 2).

Kapoor (ref. 15) demonstrated, however, that a $(DI)^2$ device with injection gate-controlled V_H has a reduced sensitivity for control of V_{Th} . This leads to the consideration of multiple gates for switching and control as shown in figure 2. The cross section of a $(DI)^2$ switch with both MOS and injection gates is shown in figure 11.

For gated switching the switching time can be shorter than the hole lifetime (the order of 10 nsec) if the $(DI)^2$ device is initially biased near V_{Th} . The limitation of hole lifetime, however, depends on the type and nature of the deep impurity. The delay time to turn-on after gating depends on the hole trap fill time. Once the device is ON the hole lifetime changes from the short OFF state value to a longer steady state lifetime.

The fall time appears to be much slower in general than the rise time. Fall time is controlled by the traps returning to equilibrium, which in principle could be extremely fast, but usually is not. Certainly a great variety of deep impurities, topologies and bulk materials need to be studied for improving fall time. The shortest fall times are expected with direct bandgap materials such as GaAs, which is in the early stages of study.

APPLICATIONS

The range of potential applications and the benefits of this technology in terms of expanded power ranges, reduced size, weight, and cost, and in the possibility of integrated circuit compatibility are quite extensive. Most of the effort to date, however, has been directed toward the development of high voltage, high power switches. The primary interest is switches with gate controlled V_{Th} , controllable V_H and very low forward voltage drop. The goal has been a thyristor-like switching characteristic with both turn-on and turn-off capability. Switching speeds of the order of a microsecond appear feasible in principle and are desirable for many uses. Thus far, however, microsecond switching has only been obtained in relatively small, low power devices.

$(DI)^2$ switches are being designed and characterized for specific applications as high voltage ON/OFF switches, circuit breakers, and remote power

controllers. Solid state switchgear using these devices could be smaller, lighter weight, more efficient, and more versatile in future large space power systems. Studies are presently being conducted or planned to fully measure the switching times and terminal characteristics of the $(DI)^2$ devices in inverter and converter circuits. In addition a comprehensive computer model of the $(DI)^2$ switch is rapidly becoming a valuable tool to assist both in the design of devices and in the understanding of their switching characteristics.

At the other end of the power spectrum, very low voltage switches and zero voltage drop diodes are being investigated for low voltage power supplies and TTL compatible IC applications. Additional work continues on various other low power $(DI)^2$ devices of interest for logic and control circuit applications. For example, devices exhibiting voltage controlled delays, voltage controlled oscillations, and pulse-width-modulator functions are being investigated (ref. 16).

CONCLUSIONS

The primary benefits of the new family of high voltage $(DI)^2$ semiconductor switches appear to have the potential to switch voltages in the tens of kilovolts and control power in the multi-kilowatt levels. To date 2 kV, 2 A devices have been demonstrated. The feasibility of gating the devices ON and OFF like a gate turn-off thyristor with low forward drop could yield extremely good efficiency for high power switching applications.

This technology for all its promise is still in relatively early stages of development when compared to the more mature p-n junction technology. Much R & D work is underway to bring the $(DI)^2$ semiconductor family to levels of technology readiness for future aerospace power applications. The potential benefits of $(DI)^2$ devices, however, and their fabrication methods using conventional semiconductor materials, processing and planar topologies should enable the rapid transfer of this technology from the university and the R & D laboratories into industrial production and use.

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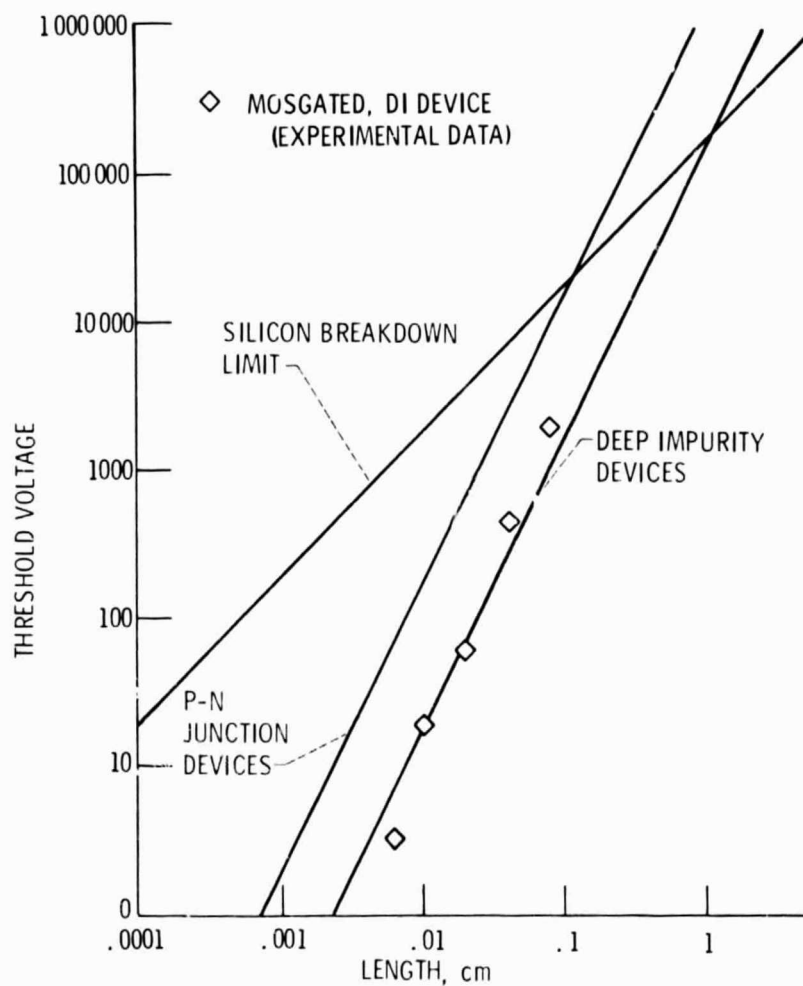


Figure 1. - High voltage capability of deep impurity devices compared to P-N junction devices in silicon.

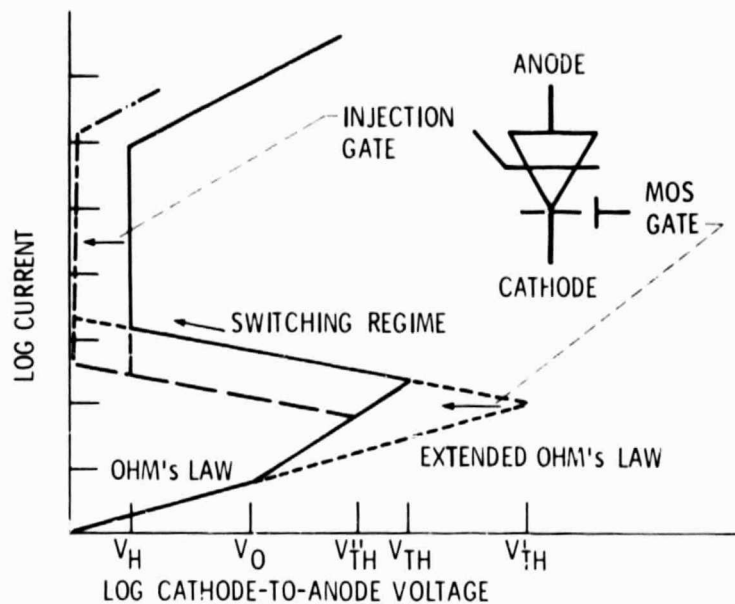


Figure 2. - Volt-ampere characteristic showing gating effects of $(DI)^2$ devices.

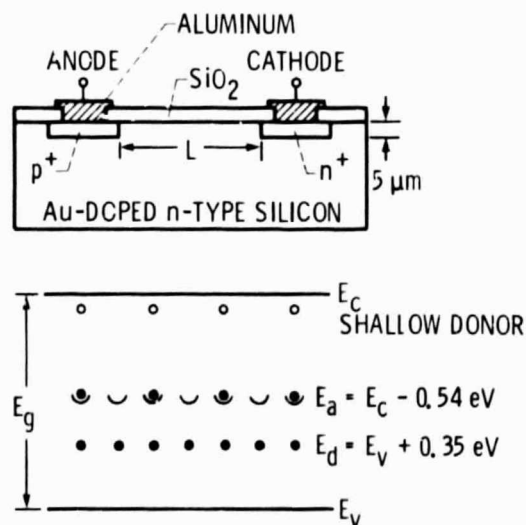


Figure 3. - Cross section of a deep impurity, double injection semiconductor fabricated in a planar configuration. Lower portion of figure depicts the energy gap E_g of silicon, showing the energy levels of the gold acceptor and donor. The acceptor at $E_C - 0.54$ eV has been partially compensated by a shallow donor such as phosphorous. The donor at $E_v + 0.35$ eV is not activated. (From ref. 8.)

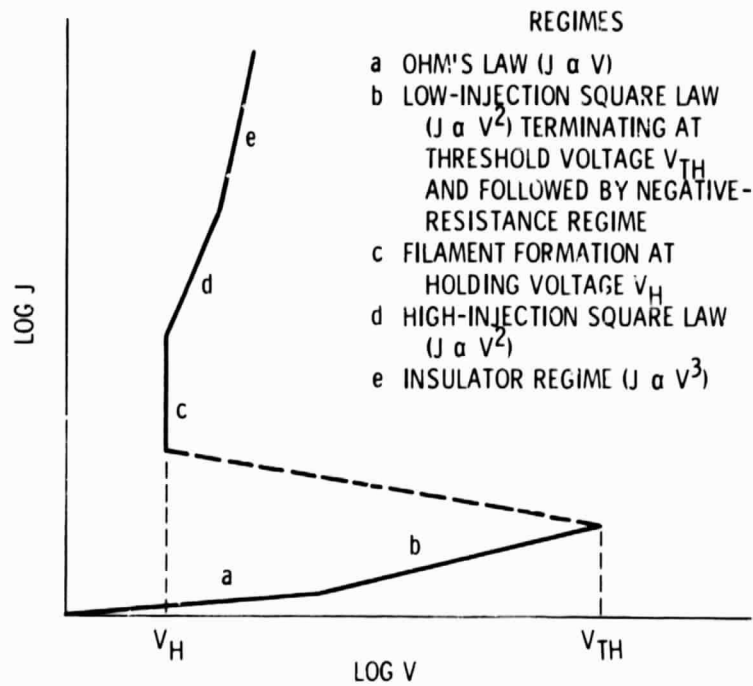


Figure 4. - Idealized current-voltage characteristics of a double-injection deep-level switching device. (From ref. 2.)

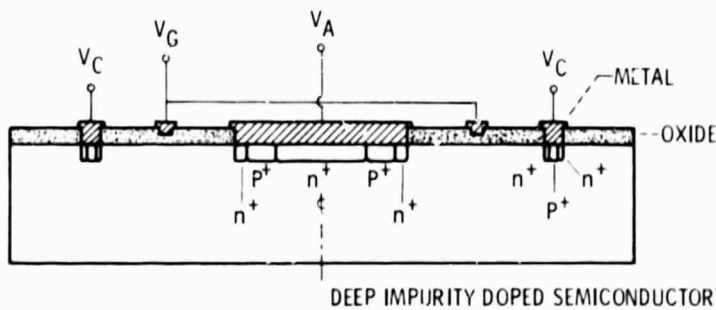


Figure 5. - Cross section of a circular lateral $(DI)^2$ switching device with MOS gate. The anode and cathode are symmetrical (Shieh) electrodes. (From ref. 5.)

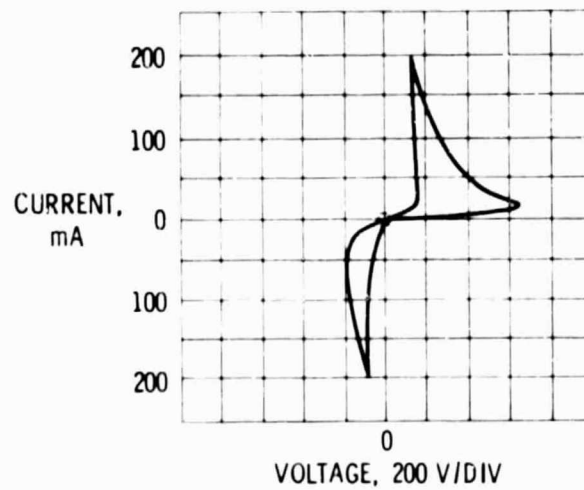
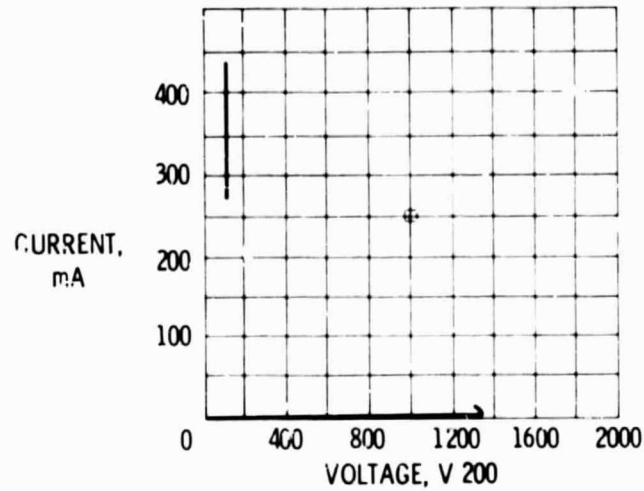


Figure 6. - The current-voltage response characteristic of the circular lateral $(DI)^2$ switch shown in figure 5. The upper curve is the dc response showing $V_{TH} = 1350$ V and $V_H \approx 80$ V at 400 mA. The lower curve shows ac response.

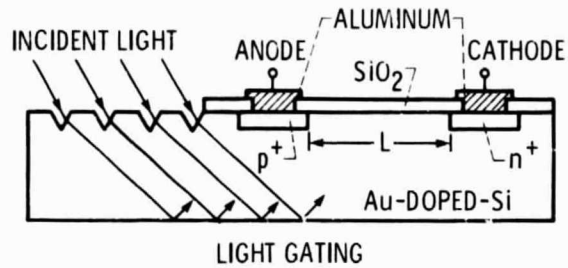
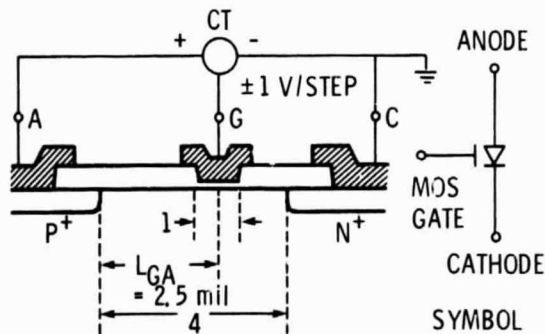
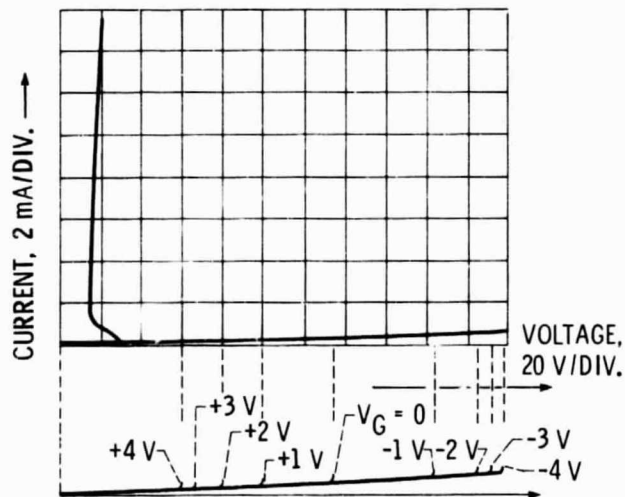


Figure 7. - Cross sectional view of a (DI)² switch showing light gating using V-grooves and multiple internal reflection techniques.



(DI)² DEVICE GEOMETRY

Figure 8. - The current-voltage characteristic of a MOS gated (DI)² switch. The device cross section and electrical configuration are shown. (From 4.)

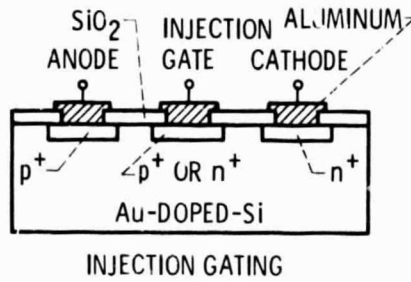


Figure 9. - Cross section of an injection gated (DI)² switch. Gate may be either p⁺ (hole) or n⁺ (electron) injecting.

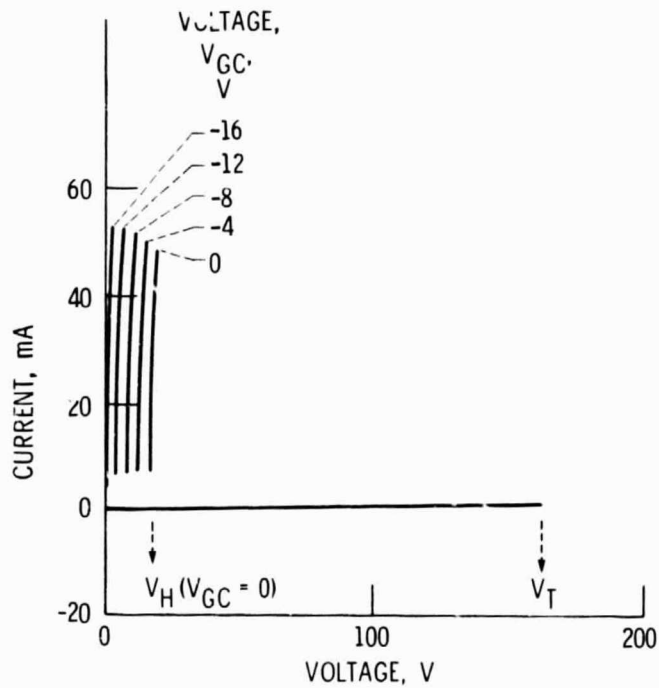


Figure 10. - Current-voltage characteristics of a p⁺ injection gated (DI)² switch. Several curves are superpositioned as the gate voltage V_{GC} is stepped at -4 V per step. (From ref. 3.)

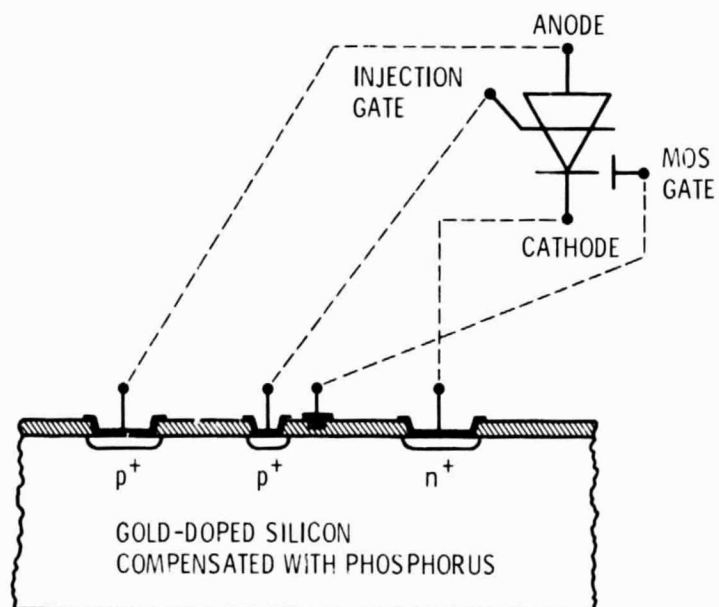


Figure 11. - Cross section of a gold doped (DI)² switch with both an injection gate and a MOS gate.