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August 11, 1983 - February 28, 1985

Taher Daud
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ABSTRACT

A new design for silicon solar cells was investigated as an approach to increasing the cell open-circuit voltage and efficiency for flat-plate terrestrial photovoltaic applications. This deviates from past designs for such applications, where either the entire front surface of the cell is covered by a planar junction or the surface is textured before junction formation, which results in an even greater (up to 70%) junction area. The heavily doped front region and the junction space charge region are potential areas of high recombination for generated and injected minority carriers.

The new design reduces junction area by spreading equidiameter dot junctions across the surface of the cell, spaced about a diffusion length or less from each other. Various dot diameters and spacings allowed variations in total junction area.

A simplified analysis was done to obtain a first-order design optimization. Efficiencies of up to 19% can be obtained.

Cell fabrication involved extra masking steps for selective junction diffusion, and made surface passivation a key element in obtaining good collection. It also involved photolithography, with line widths down to 5 μm.

A method is demonstrated for achieving potentially high open-circuit voltages and solar-cell efficiencies.

PREFACE

The objective of this program was to investigate a new design for silicon solar cells for flat-plate photovoltaic applications that features reduced junction area on the surface of the cell to reduce minority-carrier recombination and increase cell efficiency.

The innovative design consists of equidiameter dot junctions uniformly distributed over the cell surface, spaced about one diffusion length or less apart. In this design, therefore, the junctions cover only a small fraction of the total cell area. Studies of this design are motivated by prospects of reduction of reverse saturation current and increase of short-wavelength radiation absorption within the lightly-doped p-type base silicon rather than within the more heavily doped n^+ region at the device surface.

The reduced saturation current helps to improve the open circuit voltage; effective surface passivation between the junction dots and proper design of junction configuration allows good collection efficiency. To understand the effects of reduced junction areas and to improve future solar-cell designs, the program was divided into the following tasks:

(1) Design of junction dot patterns

(2) Cell fabrication

(3) Cell characterization

(4) Modeling and correlation of results

ACKNOWLEDGMENTS

The authors acknowledge helpful discussions with O. von Roos. Assistance in spectral response measurements by B. Anspaugh is also acknowledged. The authors also thank K.M. Koliwad and A.D. Morrison for helpful suggestions and encouragement, and are grateful to J. Milstein of SERI for his advice. Secretarial help by M.J. Koop is also appreciated.

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SECTION I

INTRODUCTION

Since the advent of solar cells in 1954 (Reference 1), efforts to increase the efficiency of p-n junction silicon solar cells have continued. Research in materials and device technology (References 2, 3 and 4) has been responsible for better understanding of device physics and improvement in the performance of silicon solar cells.

Development in silicon growth technology has resulted in wafers with reduced dislocation densities and chemical impurities, and thus increased minority-carrier diffusion lengths (References 5 and 6). Research in p-n junction formation, surface preparation with multilayer antireflective (AR) coatings and back-surface reflection has helped in attaining more efficient light absorption. These have contributed to better short-circuit current.

Incorporation of a back-surface field (References 3 and 7) was one very successful design feature that effectively decreased dark current and thereby improved the open-circuit voltage, in addition to increasing the short-circuit current.

In parallel with this, metal-insulator semiconductor (MIS) solar cells (References 8 and 9) have been optimized for improved V_{oc}, but current collection has suffered considerably. In addition, long-term stability problems related to metallization, oxide charges and semiconductor surfaces have not been solved. Other approaches such as tandem cells (References 10, 11 and 12), etc., suffer from larger dark currents because of increased junction areas for the same cell area.

This program was directed toward reduction of junction area to reduce dark current and improve open-circuit voltage. It was divided into the following four tasks for understanding of the effects of junction-area reduction and for evaluation of more optimal cell design:

(1) design of junction dot patterns

(2) modeling

(3) cell fabrication

(4) cell characterization

These tasks are described following a brief description of theory. Discussions and conclusions are presented. A computer program written in BASIC, which was used in the modeling, is provided in Appendix A.

A similar effort with devices called point-contact solar cells has been made with thermal-photovoltaic cells (Reference 13) and concentrator cells (Reference 14).

SECTION II

THEORY

A. OPEN-CIRCUIT VOLTAGE

A p-n junction silicon solar cell can be represented by a constant current generator in parallel with a diode. Ideally, a diode with only diffusion current, I_d, can be represented by the diode equation

$$I_d = I_o[\exp(qV/nkT) - 1] \tag{1}$$

or

$$I_d = J_o \cdot A_j[\exp(qV/nkT - 1)]$$

where I_d = reverse saturation current

J_o = reverse saturation current density

A_j = area of the p-n junction

q = electronic charge

V = applied voltage

n = diode ideality

k = Boltzmann constant

T = diode temperature, K

This ignores any series and shunt resistances and the space charge carrier recombination. The photogenerated current, I_{sc}, can be added algebraically to the diode current (Equation 1) to obtain the solar-cell output current as

$$I = I_{sc} - J_o \cdot A_d \quad [\exp(qV/nkT) - 1] \tag{2}$$

If the total area of incident radiation on the solar cell is A_T, i.e., $I_{sc} = J_{sc} \cdot A_T$, then Equation 2 becomes

$$I = J_{sc} \cdot A_T - J_o \cdot A_j[\exp(qV/nkT) - 1] \tag{3}$$

Under open-circuit conditions, $I = 0$ and $V = V_{oc}$ and hence, from Equation 3, the open-circuit voltage is given by

$$V_{oc} = (nkT/q)\ln[(J_{sc} \cdot A_T/J_o \cdot A_j) + 1] \quad (4)$$

or

$$V_{oc} = (nkT/q)\ln [J_{sc}/J_o(A_j/A_T)] + 1$$

Thus, the ratio A_j/A_T can be changed to alter V_{oc}. A plot of V_{oc} vs A_j/A_T is shown in Figure 2-1 for n = 1, where J_{sc} and J_o are used as parameters with J_{sc} of 30 and 40 mA/cm^2 and J_o of 10^{-10}, 10^{-11}, and 10^{-12} A/cm^2. It is seen that an order-of-magnitude reduction in the area ratio A_j/A_T results in a theoretical increase of about 60 mV in V_{oc}. This may translate into an 8% to 10% increase in efficiency.

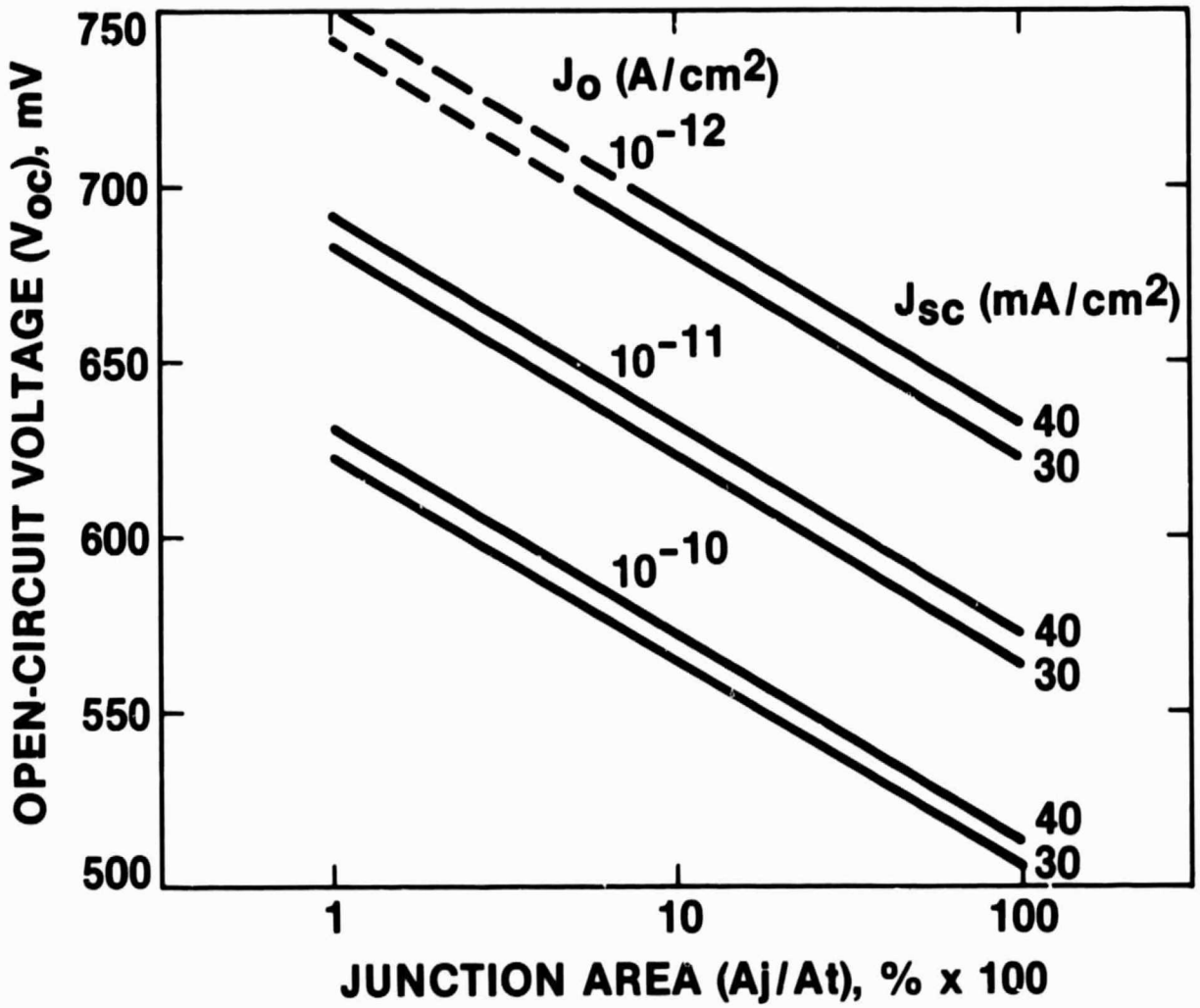


Figure 2-1. Open-Circuit Voltage vs Percentage Area Ratio

B. SHORT-CIRCUIT CURRENT

In a conventional p-n junction solar cell, most of the charge carriers generated in the bulk are shielded from front-surface effects by the shallow junction spread across the area of the cell. Also, the charge carriers generated within the heavily doped front region can be prevented from combining at the front surface if the surface is passivated. A recent study (Reference 15) shows that the blue response can be improved considerably by thermally grown thin oxide at the front surface.

In the design presented here, the junction covers only part of the front surface; the less junction area covered (as a fraction of the total area), the less separation of the bulk from the surface by the junction. Thus, most of the photogenerated carriers may not be prevented from reaching the surface. In this case, the surface must be well passivated to enable all the generated carriers to reach the junction. Similarly, the small area junctions must be judiciously spread to within at least a diffusion length of the minority carriers in the base.

Small-area junctions afford another advantage in terms of the current-flow pattern. In conventional cells, the current flow in the diffused region is lateral within the depth of the junction, which is only a fraction of a m, whereas in dot junctions the flow is nearly perpendicular to junction surface; this is likely to result in lower series resistance.

The value of the short-circuit current will depend on minority-carrier diffusion length, junction spacing, cell thickness, and design of junctions on the cell surface. A variety of junction designs were considered, and are described in Section III.

SECTION III

DESIGN OF MASKS

For thermal diffusion on selective areas of the cell, an etched-out pattern on oxide was thought to be the easiest and most conventional way. For this, a photolithography step was necessary. Three patterns were considered.

A. CONCENTRIC RINGS

This pattern consists of concentric rings spreading out from the center of the cell with increasing radii, such that the radial distance between two consecutive ring edges is of the order of two diffusion lengths or less. The metal grid and annular diffusion patterns are shown in Figure 3-1. It was clear from this design that the metal grid must run along both the base and the diffused areas of the cell and another mask with an intricate pattern will be needed to open up windows in the oxide for metal contact in areas where the grid pattern crosses the rings. With increasing ring diameter, a slight misalignment in the mask would result in either no contact with the diffused region or a shorting of a p–n junction. Further, for larger-diameter rings, a short at one place would short out a fairly large area of the junction. Because of these complications, this design was discarded.

B. PARALLEL-JUNCTION PATTERN

Figure 3-2 shows a design in which a junction is formed with all grid lines and the bus bar on the diffused area, and most of the uncovered area of the cell having no junction. The distance between two consecutive grids would be 200 to 300 μm, which is of the order of two diffusion lengths. In general, the junction area A_j would be about 3% to 8%. No metal would run over a non-diffused area, thus avoiding any chance of junction shorting. This approach has been tried (Reference 16) using aluminum as a dopant for a p^+n device. The results were not encouraging. In this design, the junction-area distribution is not uniform; hence, for the same area, the collection of current is less efficient. However, grid pattern alignment is easier, with less chance of junction shorting in case of a processing error.

C. DOT COLLECTORS

A very efficient scheme is to form equidiameter current-collecting dot junctions spaced 100 to 200 m apart on the cell surface, staggered in alternate columns with grid lines connecting the dots along each column. Different dot diameters give different ratios of junction area to total area A_j/A_T (Figure 3-3). As an example, 25-μm-dia (d) junctions spaced such that the vertical and horizontal spacings S = 100 μm will give an area coverage in percentage: $(A_j/A_T) = (\pi/8) \cdot (d/S)^2 = 2.5\%$.

As in the ring design, the metal grid will run on areas both with and without diffusion. However, because of their symmetrical nature, similar dot

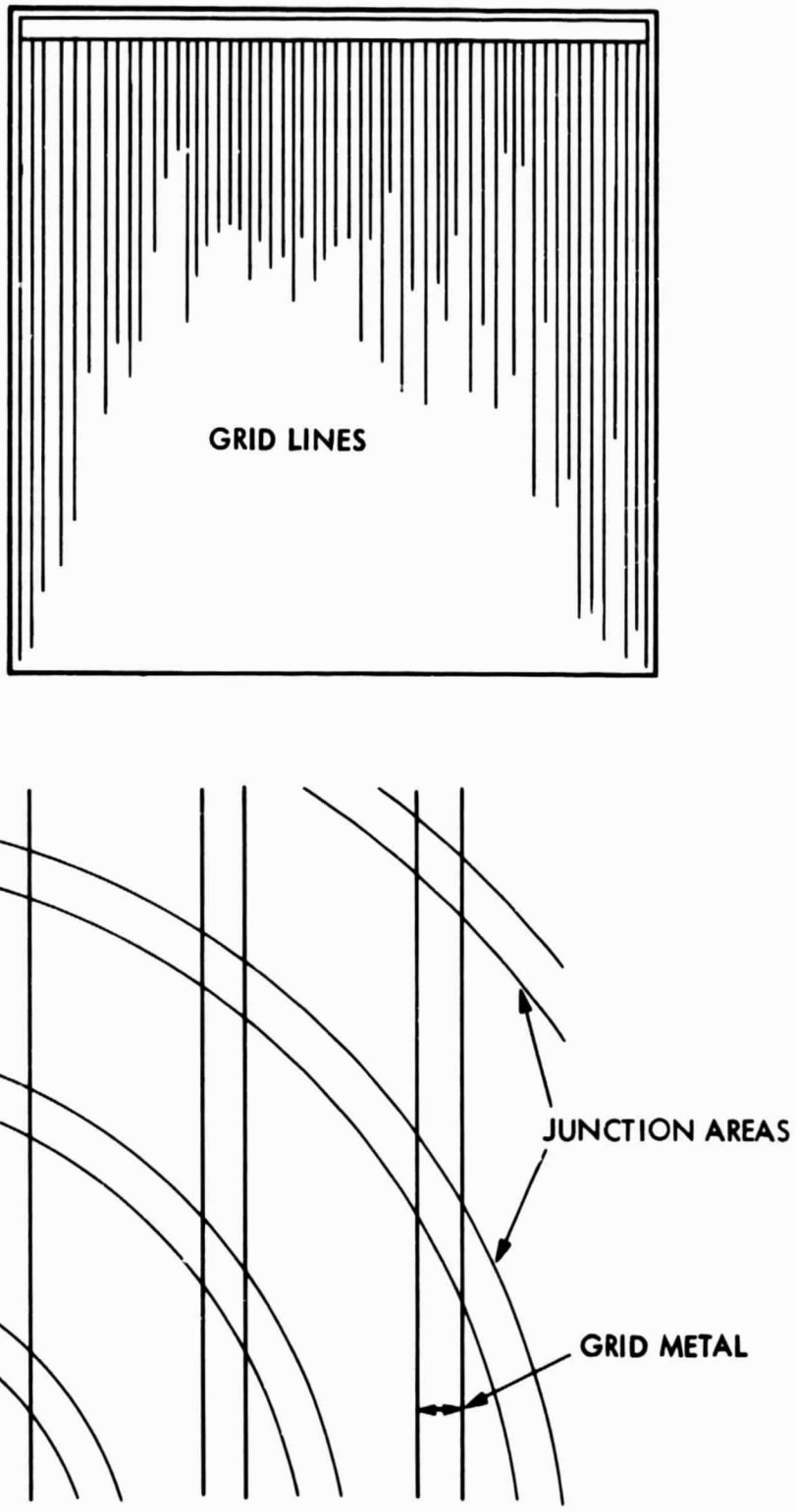


Figure 3-1. Concentric Ring Pattern

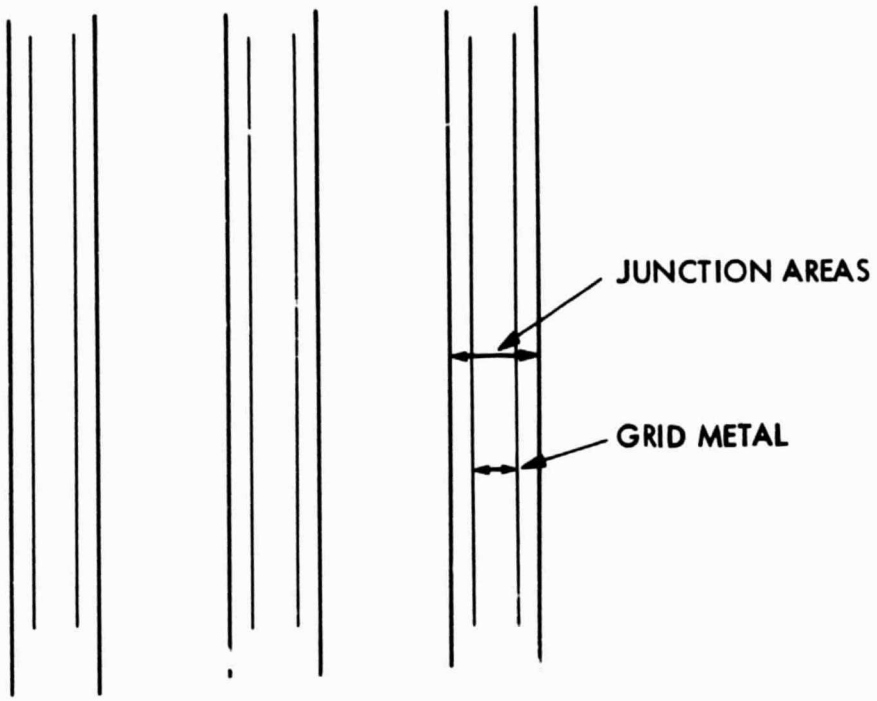


Figure 3-2. Parallel Junction Pattern

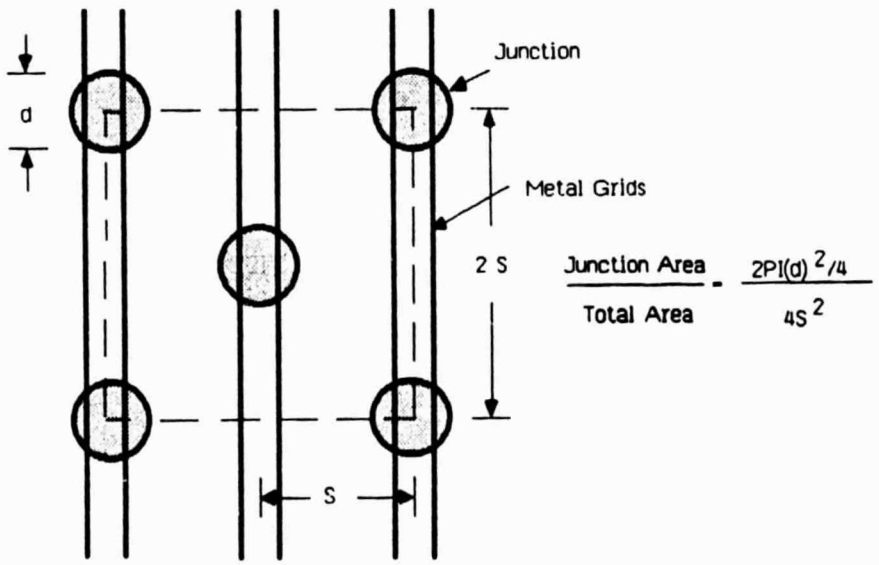


Figure 3-3. Dot-Collector Pattern

patterns with smaller dot sizes can be used to open windows in oxide for metal-grid contacts on the diffused region only. The remaining oxide acts as a barrier between the silicon surface and the metal grid.

This pattern has the advantage of easily enabling variation in area coverage and offers very efficient current collection for a given area coverage. This pattern was selected for experimentation.

A set of junction mask designs were worked out for S = 200 μm and 100 μm with d varying from 15 μm to 100 μm, to obtain area coverage varying from 1% to 20%. A suitable set of designs for metal grids was also chosen. Parameters of these sets are shown in Table 3-1, with the percentages of area coverage.

The metal grid mask design along with percentage of area shadowing is given, with W as the width of each grid finger. A line width of 5 μm was considered difficult to obtain at the time; it was thought that it might be necessary to accept higher shadowing losses until the photolithography for finer line widths was in place.

Table 3-1. Dot-Collector and Metal-Grid Mask Designs

Set No. (Dot Collector)	S, μm	d, μm	A_j/A_T, %
1	100	15	0.88
2	100	25	2.45
3	100	50	9.82
4	100	75	22.09
5	200	25	0.61
6	200	50	2.45
7	200	75	5.52
8	200	100	9.82

Set No. (Metal Grid)	S, μm	W, μm	Shadow, %
1	100	5	6.1
2	100	10	8.5
3	200	20	6.1
4	200	20	8.5

SECTION IV

MODELING

The solar-cell design calls for a three-dimensional code to solve for the cell parameters. This is a time-intensive and costly process. Therefore, it was decided to seek a simpler, two-dimensional solution.

As an initial attempt, the cell was divided into a number of unit subcells (see Figure 4-1a), each with a square collecting junction at its center. It was then modeled as a semi-infinite surface with surface recombination velocity of either infinity or zero. After analysis it was concluded that this was not workable, because of the divergence of the dark current when assuming abruptly changing boundary conditions at the edges of the square collecting junctions. This led to an independent investigation of the origin of this divergence (Reference 17). However, this approach was abandoned for solar-cell modeling.

Another approach was to assume a zero surface recombination velocity and an exponential bulk recombination decrease. This model is described below:

Consider a square unit subcell with a dot junction of diameter d in the center of its surface, with each side of the subcell equal to S. The height, Z_t, is the thickness of the cell (Figure 4-1b). This unit subcell is divided into two volumes, I and II; I is the cylinder of diameter d with the junction at the front surface, and II is the remaining volume of the unit subcell (Figure 4-1c).

The number of photons, N_{ph}, incident on the surface will generate electron-hole pairs, in accordance with Lambert's law, throughout the volume of the unit subcell. The number of electron-hole pairs collected by the junction will depend exponentially on the distance of the generation point from the junction.

For volume I, this distance equals the depth of the generation point; for volume II, the distance is the square root of the sum of squares of the horizontal (r) and vertical (z) distances. For volume II, up to a diameter S, the differential surface area consists of a ring of width dr with r varying from d/2 to S/2. For r from S/2 to $S/\sqrt{2}$, the differential surface area consists of a truncated annular ring of width dr and circular arc of length 2 r - 8r arc cos (S/2r).

For bulk diffusion length of L_b, the current collection in volume I will be proportional to $\exp(-z/L_b)$ and in volume II it will be proportional to $\exp(-\text{SQRT}(r^2 + z^2)/L_b)$. The short-circuit current density is therefore written as:

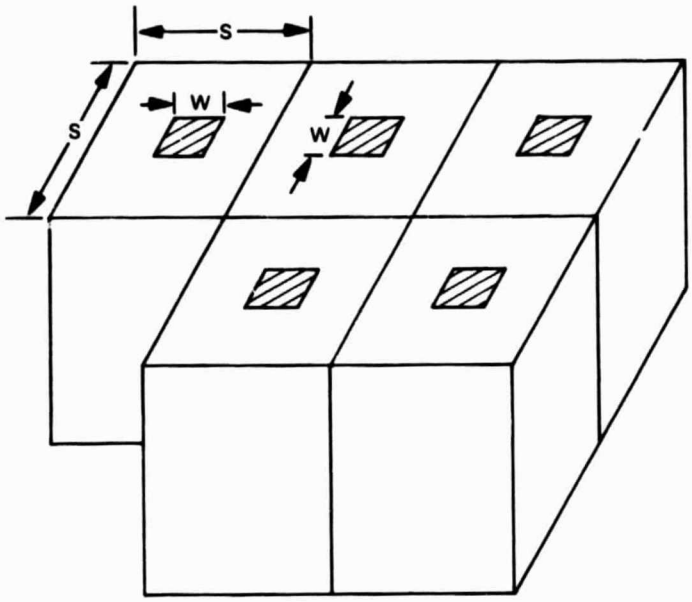


Figure 4-1a. Unit Subcells With Square Junctions

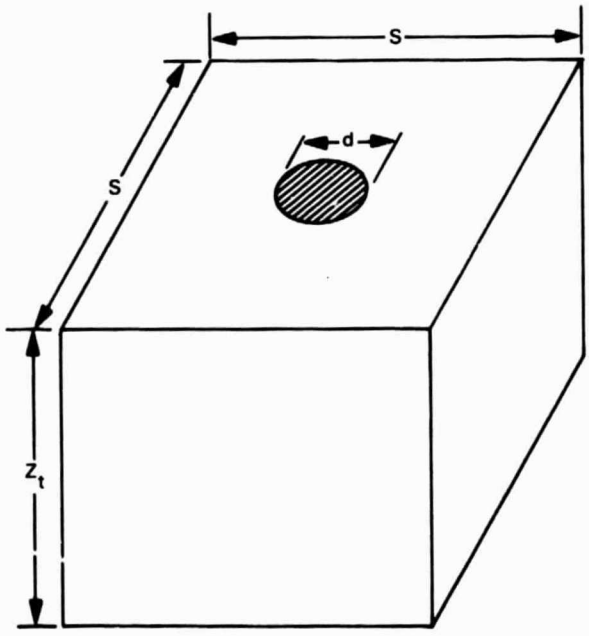


Figure 4-1b. One Unit Subcell With a Dot Collector Junction

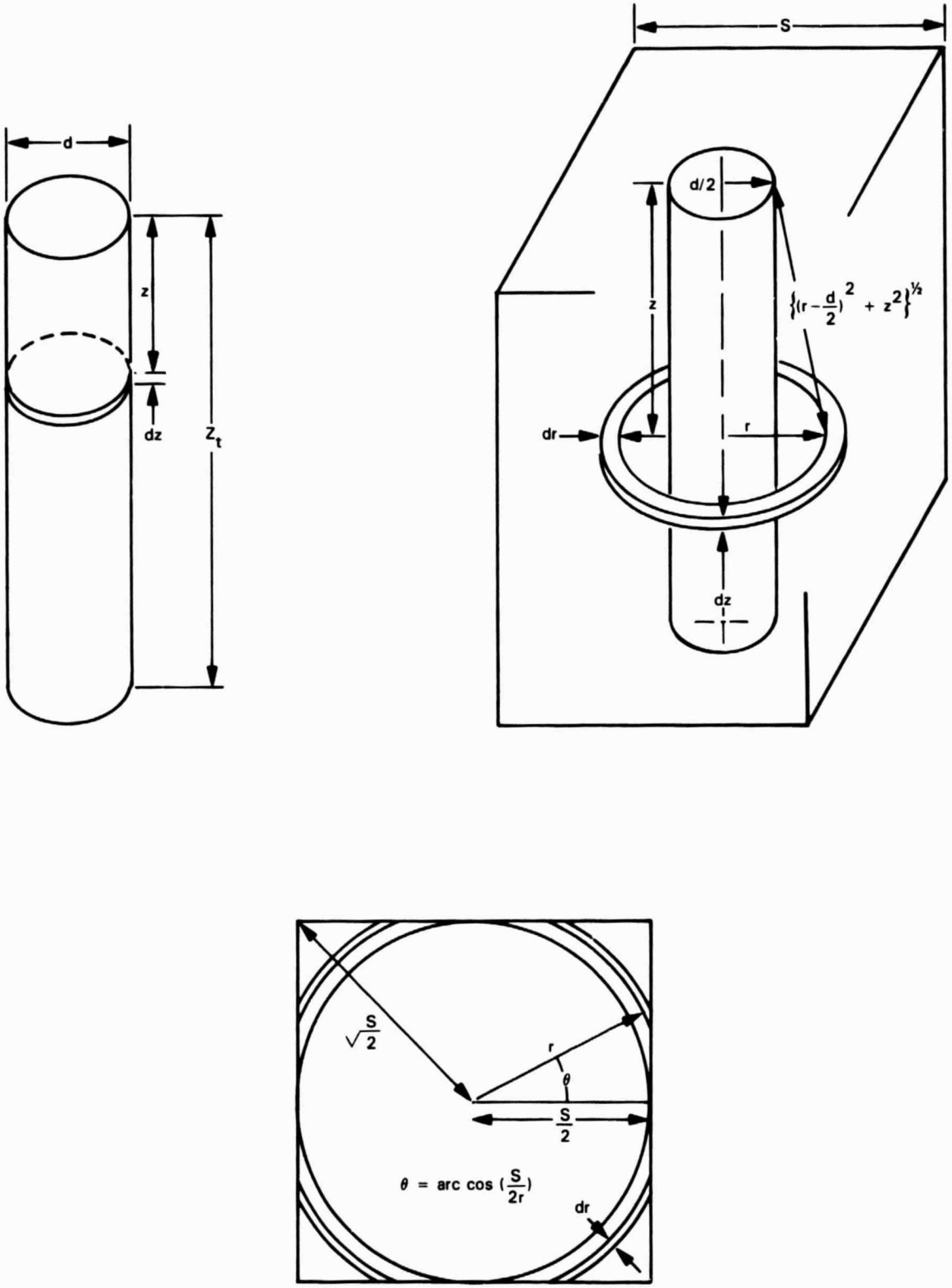


Figure 4-1c. Two Volumes, I and II, of the Unit Subcell With Carrier Collection Distances and Calculations for the Truncated Rings

$$J_{sc} = \frac{1}{S^2}\left\{ q \int_{\lambda} \alpha N_{ph} \int_{o}^{Z_t} e^{-\alpha z} dz \left[\frac{\pi d^2}{4} e^{-z/L_b} + \int_{d/2}^{S/2} 2\pi r dr e^{-\left[(r-d/2)^2 + z^2\right]^{1/2}/L_b} \right.\right.$$

$$\left.\left. + \int_{S/2}^{S/\sqrt{2}} \left[2\pi r - 8r\cos^{-1}(S/2r)\right] e^{-\sqrt{\left(r^2+z^2\right)}/L_b} dr \right] \right\} \qquad (5)$$

where α = optical absorption coefficient in silicon

N_{ph} = number of photons incident per cm^2-sec-μm

Z_t = thickness of the cell

The I-V curve is obtained from the equation

$$J = J_{sc} - J_o \left(e^{qV/kT} - 1\right) \qquad (6)$$

where V = output voltage

J_o = reverse saturation current density

$= (qn_i^2/N_A) \cdot (D_n/L_b) \cdot (\pi d^2/4S^2)$

and J = output current density.

A plot of J_{sc} vs junction diameter d for S = 50, 100, 150 and 200 μm and for L_b = 100 and 300 m is given in Figure 4-2.

Cell parameters of V_{oc}, J_{sc}, FF and efficiency at 100 mW/cm^2 for L_b = 100, 200, and 300 μm and with $N_A = 1 \times 10^{17}$ per cm^3, and D_n = 15 cm^2/sec are shown in Table 4-1. It is interesting to note that for 100 μm and 200 μm diffusion lengths, a d/S of 25/50 offers highest efficiency; for 300 μm diffusion-length material, a d/S of 25/100 is best. Thus for good material, lesser junction-area coverage is beneficial.

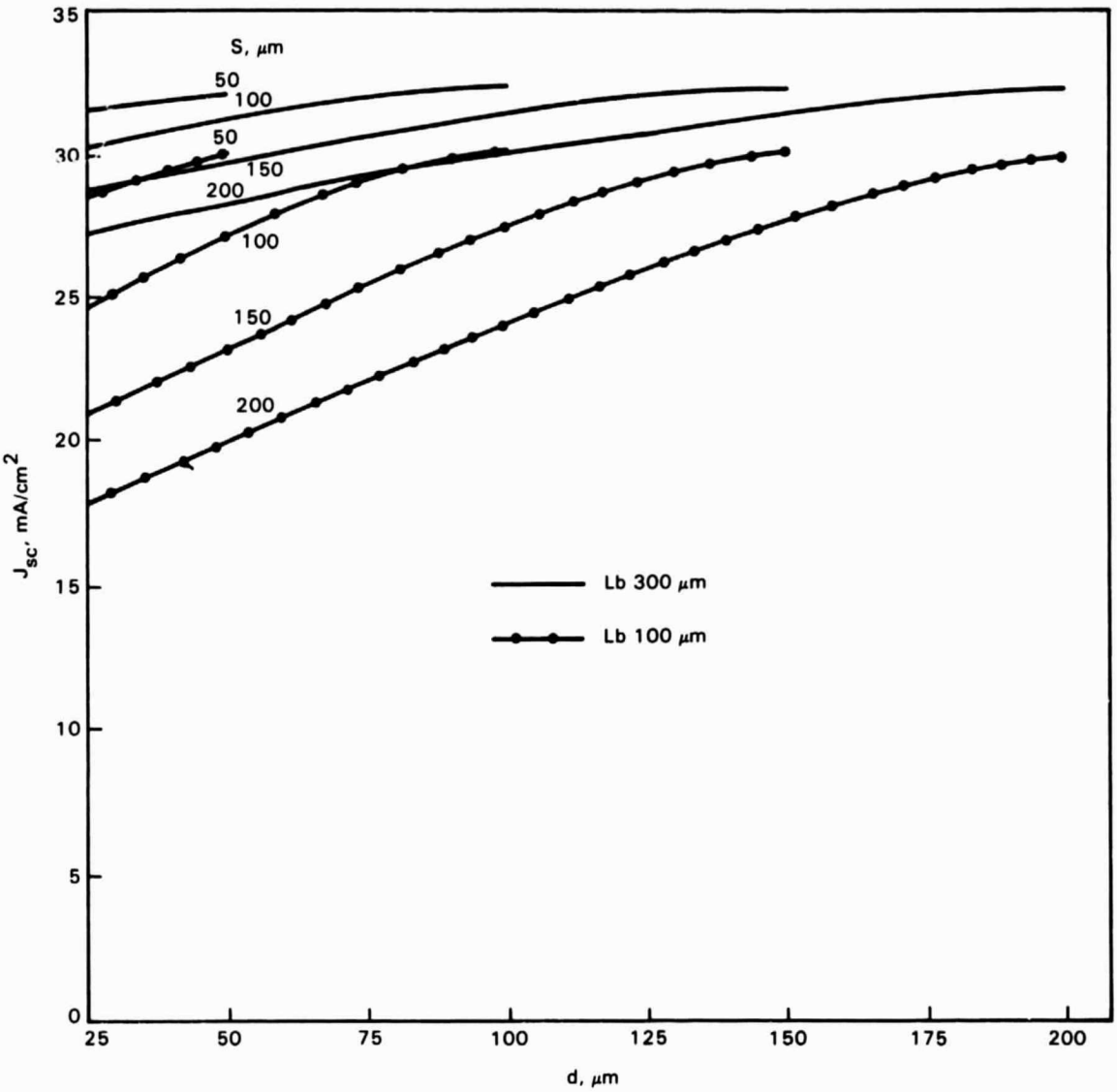


Figure 4-2. Calculated Short-Circuit Current Density for Different Dot Collector Designs and Bulk Diffusion Lengths

Table 4-1. Calculated Solar-Cell Parameters for Different Dot-Collector Designs

L_b, μm	S, μm	d, μm	V_{oc}, mV	J_{sc}, mA/cm^2	FF	Eff.,%
100	50	25	682	28.6	0.843	16.45
		50	648	30.0	0.836	16.28
	100	25	714	24.6	0.835	14.65
		50	681	27.1	0.843	15.53
		75	662	29.0	0.823	15.82
		100	648	30.1	0.837	16.33
	150	25	730	20.8	0.852	12.94
		50	697	23.2	0.847	13.69
		75	679	25.5	0.843	14.57
		100	666	27.5	0.832	15.23
		125	656	29.1	0.839	15.99
		150	648	30.0	0.836	16.27
	200	25	741	17.6	0.853	11.15
		50	708	19.7	0.848	11.85
		75	690	21.9	0.845	12.75
		100	677	24.0	0.843	13.69
		125	668	26.0	0.834	14.46
		150	660	27.7	0.840	15.33
		175	654	29.0	0.837	15.88
		200	647	29.9	0.838	16.19
200	50	25	702	30.8	0.846	18.28
		50	667	31.5	0.832	17.50
	100	25	736	28.7	0.852	17.97
		50	701	30.1	0.847	17.84
		75	681	31.1	0.843	17.88
		100	667	31.7	0.833	17.61
	150	25	755	26.4	0.854	17.00
		50	720	27.8	0.844	16.89
		75	701	29.2	0.843	17.28
		100	687	30.3	0.844	17.56
		125	676	31.2	0.841	17.72
		150	667	31.7	0.832	17.58
	200	25	767	24.2	0.846	15.68
		50	733	25.6	0.851	15.96
		75	713	26.9	0.834	16.02
		100	700	28.2	0.846	16.72
		125	689	29.4	0.845	17.11
		150	681	30.4	0.843	17.44
		175	673	31.1	0.840	17.59
		200	667	31.6	0.832	17.54

Table 4-1. Calculated Solar-Cell Parameters for Different Dot-Collector Designs (Cont'd)

L_b, μm	S, μm	d, μm	V_{oc}, mV	J_{sc}, mA/cm^2	FF	Eff.,%
300	50	25	713	31.7	0.833	18.82
		50	678	32.2	0.842	18.36
	100	25	748	30.3	0.853	19.33
		50	713	31.3	0.832	18.55
		75	693	32.0	0.844	18.72
		100	678	32.4	0.842	18.49
	150	25	767	28.6	0.846	18.58
		50	732	29.7	0.852	18.51
		75	712	30.6	0.849	18.51
		100	698	31.4	0.846	18.57
		125	687	32.0	0.844	18.58
		150	678	32.4	0.842	18.48
	200	25	781	27.0	0.857	18.10
		50	746	28.1	0.853	17.86
		75	726	29.1	0.848	17.89
		100	712	30.0	0.848	18.10
		125	701	30.8	0.846	18.28
		150	692	31.5	0.845	18.42
		175	685	32.1	0.843	18.49
		200	678	32.5	0.842	18.46

SECTION V

EXPERIMENTS AND TESTING

Solar-cell fabrication was done on 3-in.-dia, (100) orientation, 1 to 2 Ω-cm, 0.3 to 0.4 mm (12 to 16 mils)-thick Czochralski (Cz) or float-zone (FZ) wafers using masks to obtain four 2 x 2-cm cells per wafer. The general processing steps needed (see Figure 5-1) were:

(a) Oxidation of front and back surface, 3000 to 4000 Å thick, to act as a diffusion mask.

(b) Etching windows on front surface with photolithography, followed by phosphorus diffusion at 850°C for 20 min. with PH_3.

(c) Etching of oxide and phosphosilicate glass using 10% to 20% HF solution.

(d) Thermal oxidation, 100 to 150 Å thick, on the front surface to passivate the cell surface and form an insulation layer on the p substrate to avoid shorting by metallization, and yet etch windows for contact with the diffused regions.

(e) Back metallization by evaporation of Al-Ti-Pd-Ag (600-600-400-25K Å) and sintering at 600°C in H_2; front metallization and lift-off by evaporation of Ti-Pd-Ag (600-400-40K Å).

(f) Single or multilayer AR coating for good photon absorption. Single layer is 725 Å SiO_x and multilayer consists of TiO_2 and Al_2O_3 sputtered and sintered at 400°C for 20 min.

A number of runs of cells were made with minor changes in the processing steps as described.

Before receipt of the masks, a preliminary run with a larger-area dot mask was done. A batch of p-type Cz wafers were thermally diffused and mesa-etched to form a dot pattern. A 50% reduction in area reduced the cell efficiency (with no AR coating) from 8.9% to 3.6% (100 mW/cm^2). A slight improvement was noticed after growth of a thin oxide at 200°C (Table 5-1). Junction area after etching was reduced from 4 cm^2 to 2.14 cm^2.

After receipt of the masks, the first two runs could not be completed because of problems with photo-resists and mask aligner. Proper delineation of dot junctions and grid metal could not be achieved, resulting in aborted cells.

The next run was made to study the fabrication and testing of 100-μm-dia and 50-μm-dia junctions only. Wet oxidation for diffusion masking was done at 1100°C for 1 h.

Dark I-V measurements were made on representative junctions over an area of 4 x 4 cm. It was found that, in general, the diode factor degraded with smaller junctions: about 1:35 to 1:40 for 100-μm-dia junctions and about 1:38 to 1:44 for 50-μm-dia junctions. A typical dark I-V curve is shown in Figure 5-2

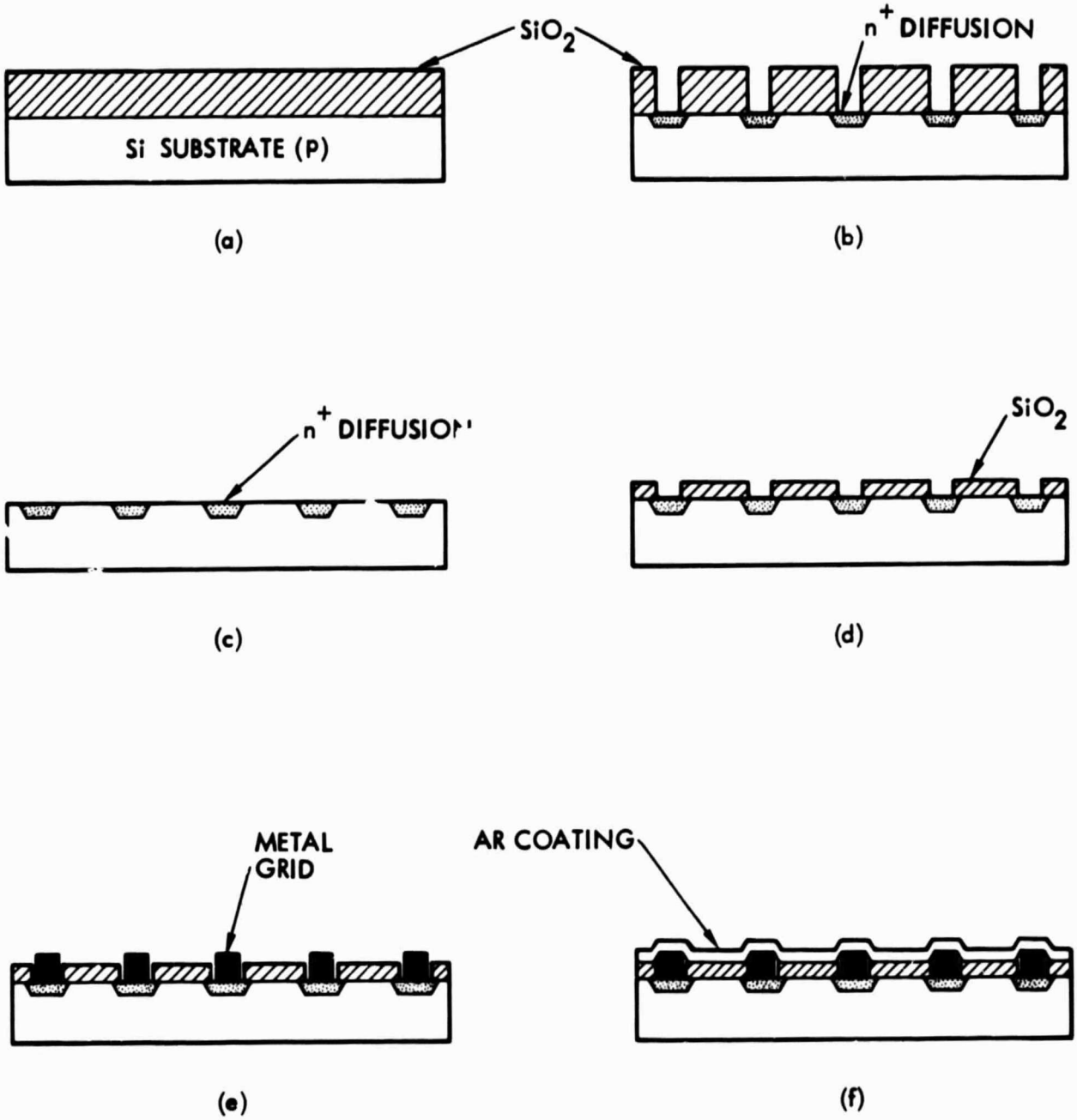


Figure 5-1. Schematic of Solar-Cell Fabrication

Table 5-1. Mesa-Etched Solar Cells

	Before Etch	After Etch	After Oxidation
V_{oc}	564 mV	527 mV	557 mV
I_{sc}	86.2 mA	38 mA	40 mA
FF	73%	71%	73%
η (No AR Coat)	8.9%	3.6%	4.1%

Junction area after etch: 2.14 cm^2
Junction area before etch: 4 cm^2
Oxide: ≈20 Å SiO_2 at 200°C

for a 100-μm-dia junction. This fabrication run involved a high-temperature (1100°C, 1 h) oxidation step, which may have not only caused degradation of bulk lifetime but also a depletion of boron at the front-surface p region. A discussion of this effect is presented in Section VI.

To avoid high-temperature oxidation and yet provide a diffusion mask, experiments with different evaporated films of oxides (SiO_x, InO, Ta_2O_5) were tried. Indium oxide and tantalum pentoxide films were strongly adherent and did not etch out properly after the photolithography step. Silicon oxide evaporation with substrate heated at about 200°C in the presence of oxygen resulted in the formation of (probably) Si_2O_3, which was found to be conducive to subsequent etching and thermal diffusion.

A run with evaporated silicon oxide was made on 1 to 2 Ω-cm, (100), 0.375 mm (15 mils)-thick, 76 mm (3 in.)-dia FZ wafers, using masks with 200-μm dot spacings (S) and dot diameter of 100 μm (referred to hereinafter as 200-100) and with spacing of 100 μm and dot diameters of 75 and 50 μm (100-75 and 100-50), respectively.

After cleaning of the wafers, evaporation of silicon oxide and opening of windows through the oxide, thermal diffusion of phosphorus was done at 850°C to obtain a sheet resistivity of 100 Ω/□. A passivating oxide (40 to 46 Å) was grown at 800°C for 30 min. followed by 15 min. annealing in nitrogen. Alignment for the front metallization on thin oxide, as well as after Ta_2O_5 AR coating, did not succeed. A third try to align, by indexing on two side edges, was finally successful. Ten 2 x 2-cm cells with dot collectors were fabricated. Figure 5-3 shows photomicrographs of two cells. The cell in Figure 5-3a is 200-50 configuration with 20-μm-wide metal grids, and the cell in Figure 5-3b is a 100-75 configuration with 10-μm-wide grids. Following this experience, a revision of the mask design for smaller-cell geometry with better registration marks and finer grid-line geometry. In addition, four 2 x 2-cm control cells were fabricated with conventional junctions and with the finer grid pattern used for dot-collector cells.

These cells were tested for light and dark I-V characteristics. It was found that the reverse saturation current density was very high (≈1 to 2 x 10^{-8}

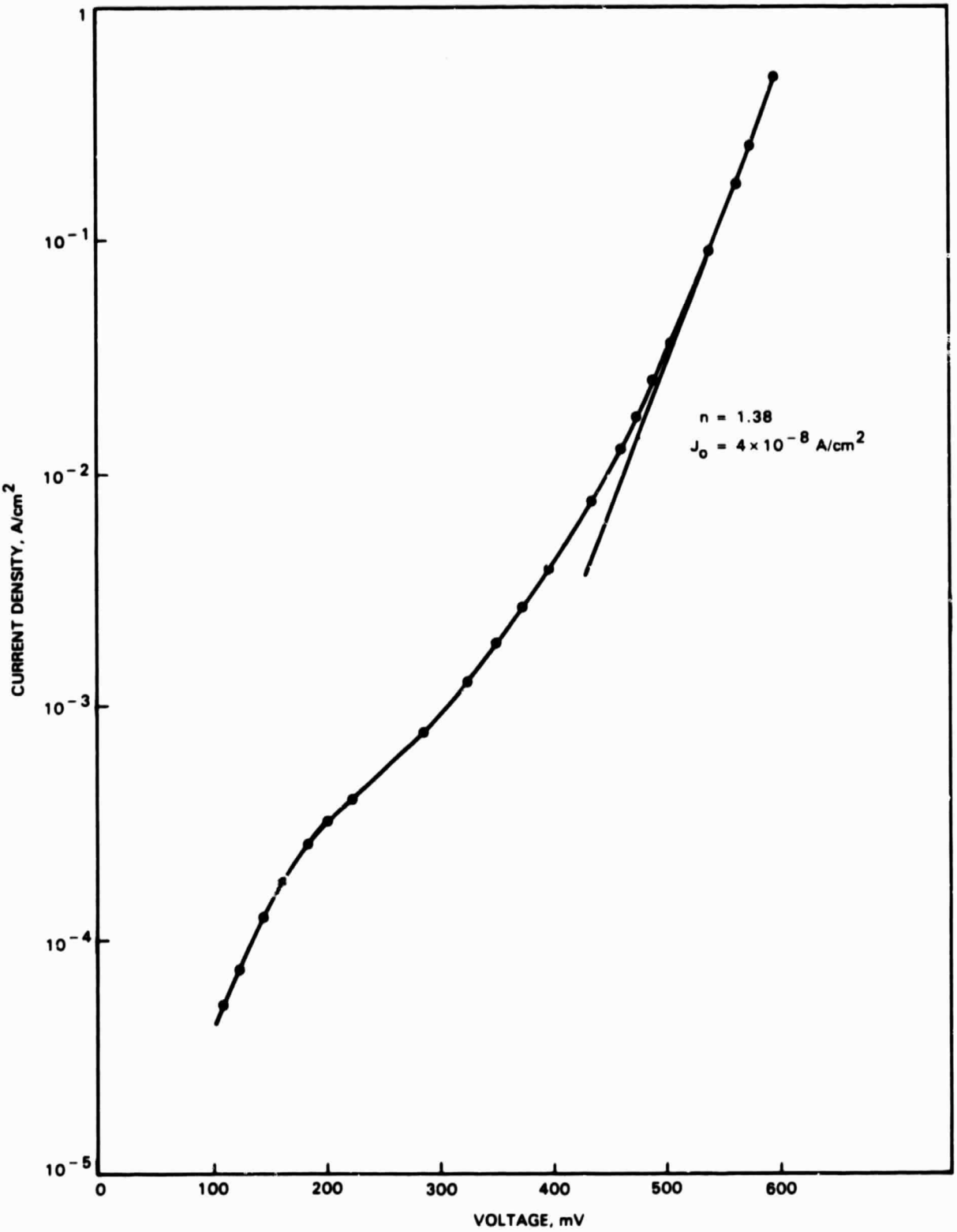
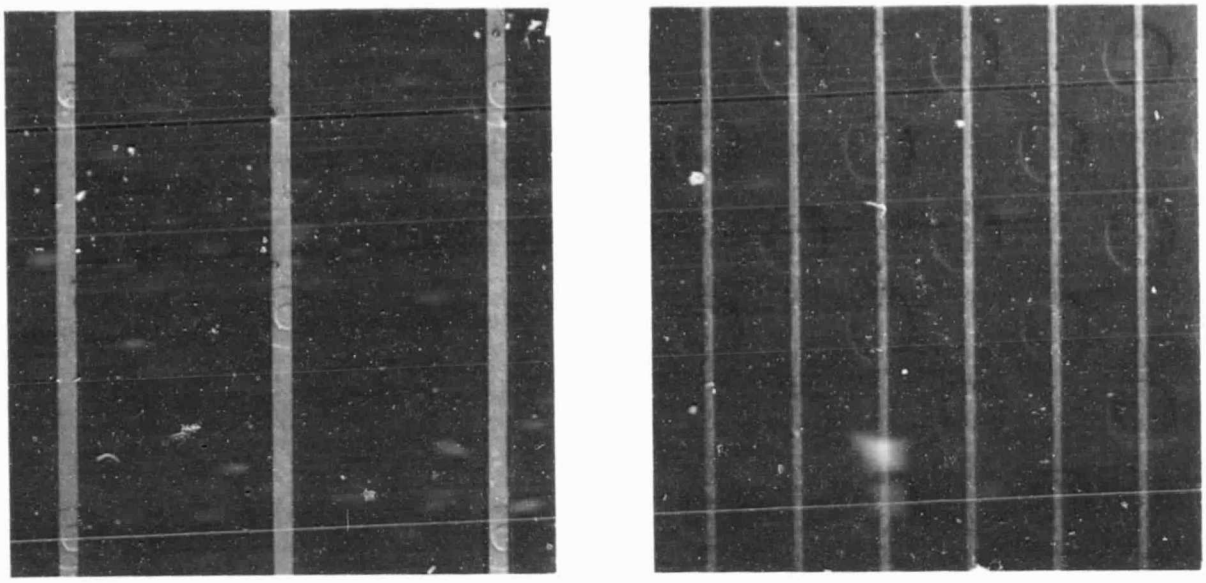


Figure 5-2. Dark I-V Characteristics of 100-μm-Dia Dot Junction



200-50-20 μm

100-75-10 μm

Figure 5-3. Photomicrographs of Two Dot Collector Cells

A/cm^2) and the light-generated current collection was very low (Table 5-2). The last column shows a calculated V_{oc} for cell-current collection of the order of 120 mA. Part of the current-collection degradation can be accounted for by greater grid widths due to undercutting during the etching of the oxide. It is estimated that the metal coverage was of the order of 12.5% on these cells. Figure 5-4 shows dark I-V characteristics of typical cells from each set. Spectral response measurement (Figure 5-5) with and without bias show the presence of trap levels. Surface photovoltage (SPV) measurement showed a degradation minority carrier diffusion length from 150 to 200 m in untreated wafers to less than 40 μm in the cells. This degradation is attributed traced to the SiO_x evaporation step and, therefore, to the SiO_x purity. High-temperature diffusion following the SiO_x evaporation may have incorporated those impurities within the Si.

The next run was done on 1 Ω-cm FZ wafers with a deposited oxide (using a low-temperature CVD system, by courtesy of Applied Solar Energy Corp.) as a diffusion barrier. Similar process steps were followed with a passivating oxide of 150 Å thickness, 10 and 15 μm-wide metal fingers (Ti-Pd-Ag), and a double AR coating. Light and dark I-V tests were performed. Table 5-3 gives the solar-cell parameters. The best efficiency obtained was 14.3% for a 75-μm-dia dot collector and 100-μm junction spacing configuration. It was interesting to note that the 200-100 cells gave approximately the same current collection as did the 100-75 cells. A retest after two days of storage showed considerable degradation in cell parameters, as shown in Table 5-3 by figures in parenthesis. Spectral response measurement showed light bias effect similar to that shown in Figure 5-5. Higher quantum efficiency at longer wavelengths with bias cannot be explained by oxide traps alone. Capacitance-voltage (C-V) measurements of oxide showed a flat-band shift of -1.45 volts (see Figure 5-6)

Table 5-2. Summary of Dot-Collector Cell Results

Set No.	Cell No.	V_{oc}, mV	I_{sc}, mA	FF	η, %	I_o, A	V_{oc}, mV, for I_{sc} = 120 mA
1	C-1	570	100	0.79	11.3		
2	C-2	576	105	0.79	11.9	2.6×10^{-8}	578
3	C-3	570	102	0.79	11.4		
4	C-4	571	102	0.79	11.4		
5	200-100/1	522	20.1	0.62	1.6	3.2×10^{-8}	572
6	200-100/2	522	19.3	0.63	1.6		
7	100-75/1	516	38.6	0.65	3.2		
8	100-75/2	507	29.2	0.66	2.4	8.0×10^{-8}	550
9	100-75/3	515	35.4	0.68	3.1		
10	100-75/4	510	30.5	0.67	2.6		
11	100-50/1	522	28.3	0.59	2.2		
12	100-50/2	516	25.8	0.58	1.9	4.6×10^{-8}	564
13	100-50/3	521	28.2	0.58	2.1		
14	100-50/4	518	26.2	0.58	2.0		

with an oxide interface state density of $10^{12}/cm^2$, as against values of -1.1 volts and $\approx 10^{11}/cm^2$, respectively, for good oxide.

The degradation in the cell performance is presumed to be due to changes in the oxide properties. Further work in understanding of thin oxides for surface passivation must be done to explore the full potential of this cell design.

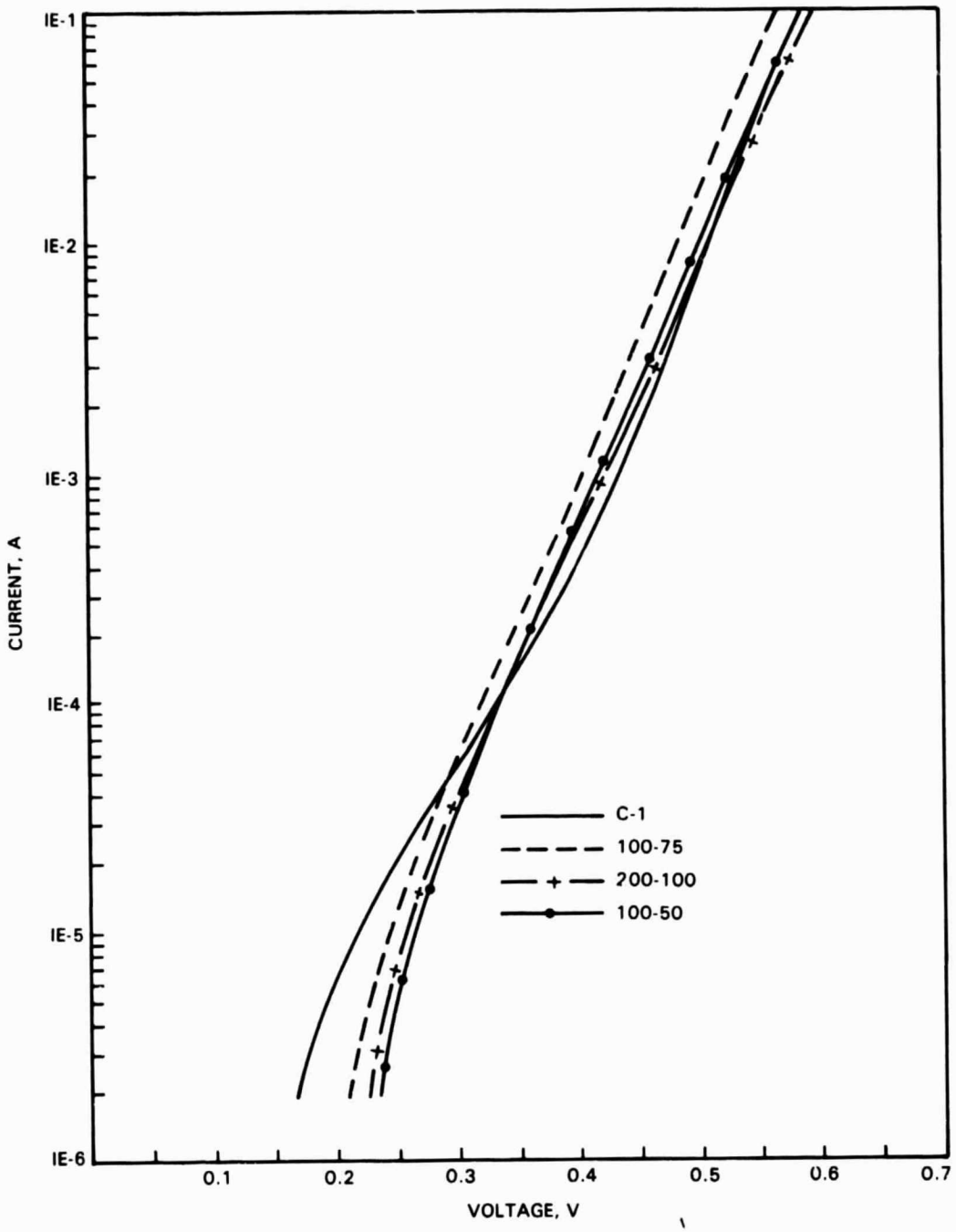


Figure 5-4. Dark I-V Curves for Dot Collector and Control (C-1) Cells

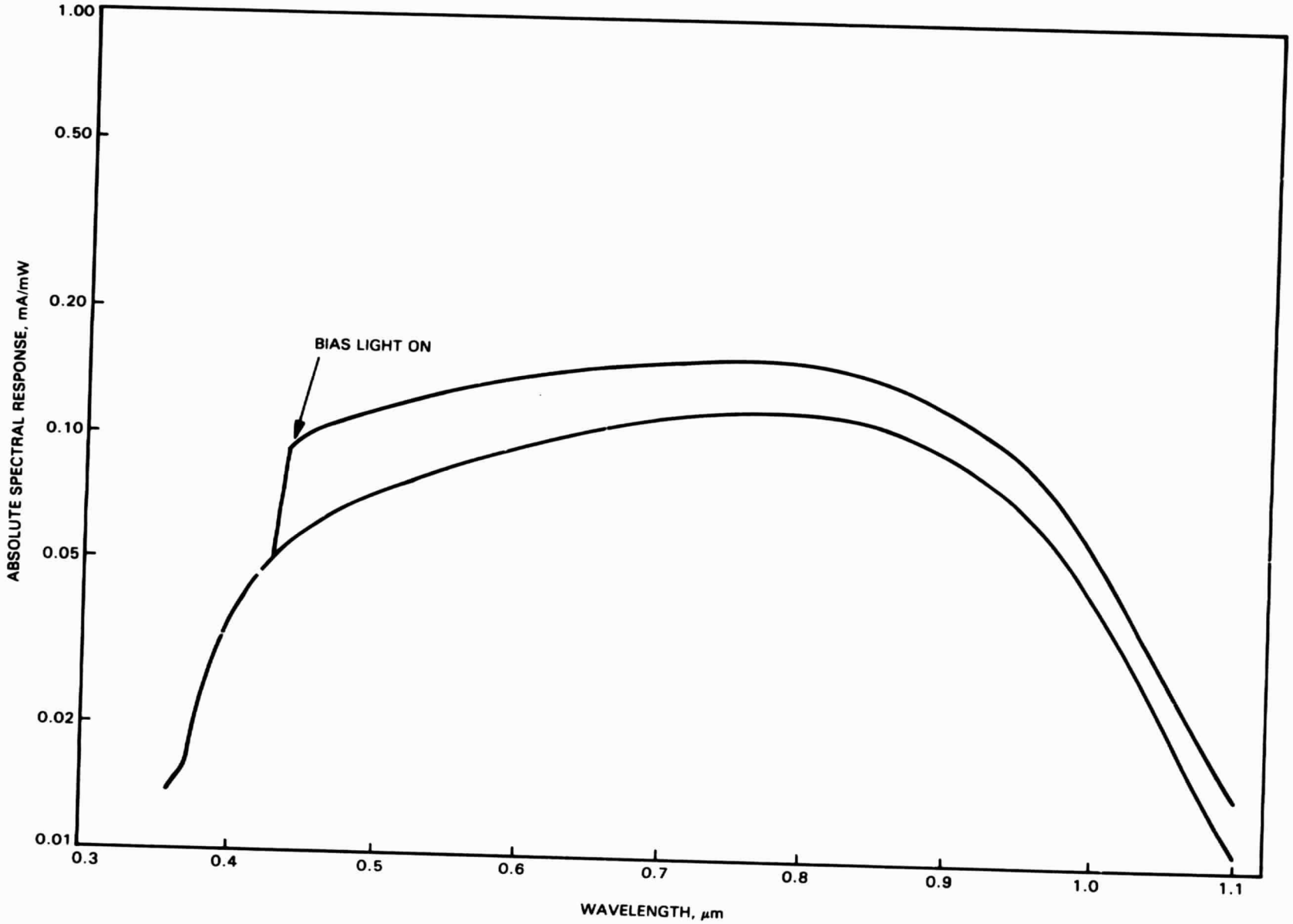


Figure 5-5. Spectral Response of Cell 100-75 With and Without Bias Light

Table 5-3. Summary of Solar-Cell Results
(1.5 Ω-cm FZ Substrates)

Set No.	Cell No.	Cell Config.	V_{oc}, mV	I_{sc}, mV	FF	Eff., %	Area Ratio, %	Shadow, %
1	036-1-1	200-50	585	123.4	0.568	10.24		
			(583)	(117.7)	(0.546)	(9.38)		8.5
2	036-1-2		594	126.1	0.554	10.37		
			(592)	(120.5)	(0.546)	(9.74)	2.5	
3	036-1-3		590	123.7	0.580	10.57		
			(589)	(118.4)	(0.572)	(9.97)		
4	036-1-4		597	125.4	0.588	11.02		
			(593)	(118.7)	(0.544)	(9.58)		
5	036-4-1	100-25	584	119.7	0.635	11.10		
			(588)	(115.3)	(0.658	(11.15)		
6	036-4-2		590	118.7	0.687	12.03		
			(589)	(112.8)	(0.676)	(11.24)	2.5	
7	036-4-3		---	-----	-----	-----		
			(582)	(109.4)	(0.577)	(8.86)		
8	036-4-4		590	120.7	0.670	11.92		
			(584)	(111.8)	(0.644)	(10.51)		
9	036-2-1	100-50	585	115.7	0.689	11.66		
			(583)	(111.2)	(0.673)	(10.90)		
10	036-2-2		548	116.0	0.565	8.97		
			(547)	(111.9)	(0.550)	(8.41)	10.0	
11	036-2-3		531	119.1	0.561	8.87		
			(530)	(113.5)	(0.556)	(8.36)		
12	036-2-4		577	117.7	0.679	11.53		
			(576)	(110.8)	(0.674)	(10.76)		
13	036-3-1	100-75	598	124.3	0.751	13.96		
			(597)	(117.8)	(0.758)	(13.32)		
14	036-3-2		596	122.1	0.764	13.89		
			(596)	(117.2)	(0.756)	(13.21)	22.0	
15	036-3-3		596	125.2	0.754	14.06		
			(594)	(119.0)	(0.754)	(13.32)		
16	036-3-4		597	124.5	0.771	14.32		
			(596)	(119.7)	(0.768)	(13.69)		

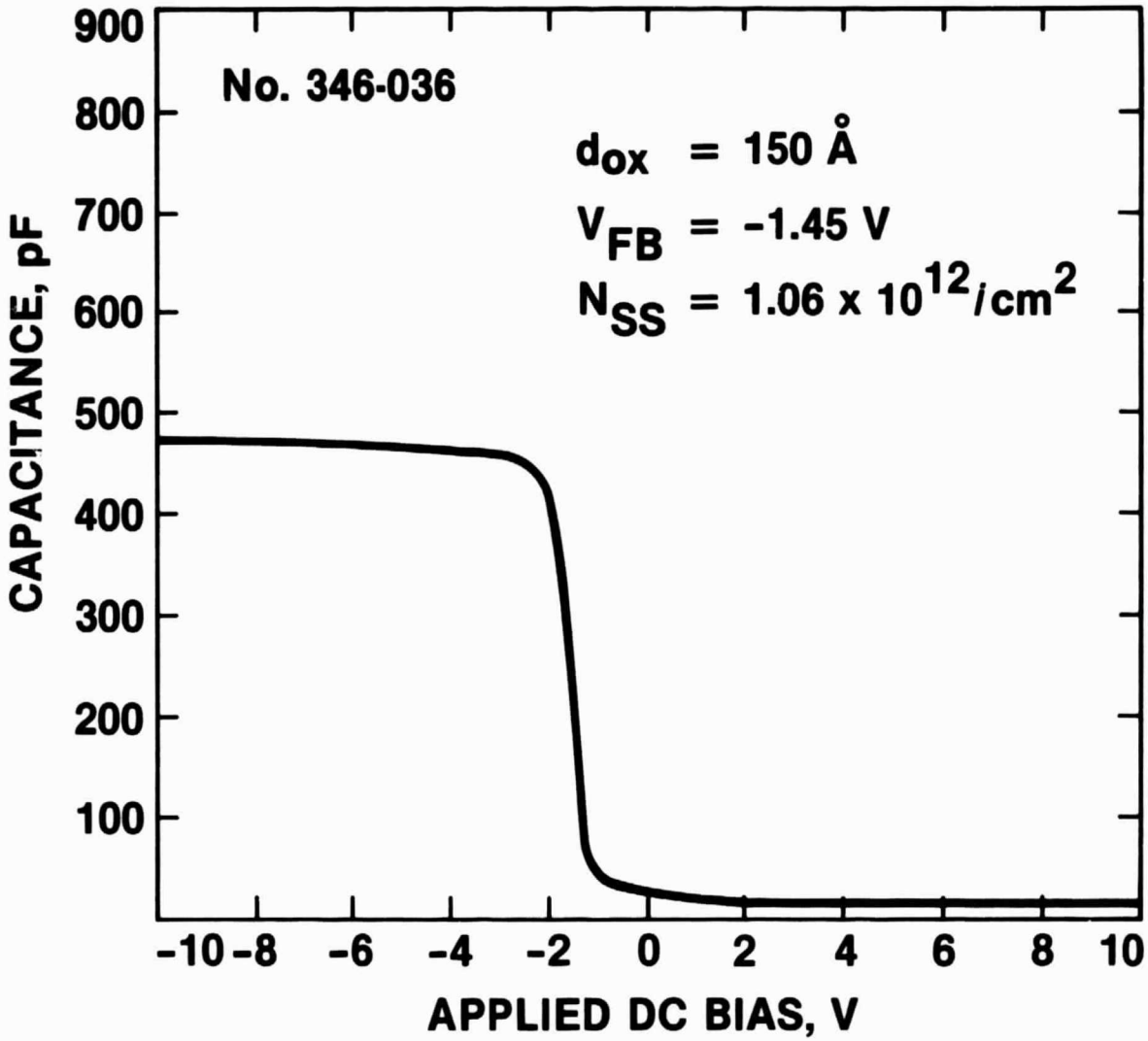


Figure 5-6. Capacitance-Voltage Measurements for Passivating Oxide

SECTION VI

DISCUSSION AND CONCLUSIONS

The modeling calculations show that smaller spacing with proper dot-junction areas give improved cell performance. Thus, a potential has been demonstrated for achieving high efficiency with these cells.

Fabrication experiments during the later part of this program were fruitful in demonstrating the feasibility of this approach and also in pointing out some of the design and fabrication pitfalls.

One of the problems faced during fabrication was that the registration marks on the masks were too far apart, leading to difficulties in alignment.

High-temperature wet-oxide growth on p-type substrates introduces an extra high-temperature step that reduces the diffusion length. In addition, with the p-type silicon/SiO_2 interface, it is known that due to redistribution, boron tends to escape into SiO_2 at high temperature (References 18 and 19), leading to a depleted region along the surface surrounding the junction. This tends to increase surface leakage along the p-type surface and to space-charge recombination in the depleted subsurface regions surrounding the dot junctions. Low-temperature-CVD-deposited oxide has solved this problem.

Dark I-V data (Figure 5-4) shows that a conventional junction gives a much better diode ideality factor than is obtained by the dot collectors. A comparison of dark I-V data from the last run is shown in Figure 6-1. The improvement in the characteristics with reduction in junction area is clear. However, the diode ideality factor was found to be 1.2 to 1.25, which is high. In addition, the cell results show considerable shorting, probably due to metal grids running over p regions with a thin (150 Å) oxide. A high series resistance was also noted. These problems led to the degradation of cell performance shown in Table 5-3. A closer look at the metal grid design or suitable alteration in the fabrication procedure may be needed.

More work is needed in theoretical analysis to further optimize the design and determine limits to cell performance. Passivation of front surfaces is important; more research in thin-oxide growth and characterization is needed to arrive at optimum thickness and fabrication procedure. More cell fabrication runs with design variations are also needed to improve performance and to understand the limiting loss mechanisms.

In summary, this work has shown that the dot-junction design has good potential for improving cell efficiency and also that work in key areas of theoretical analysis, oxide passivation and cell fabrication is required.

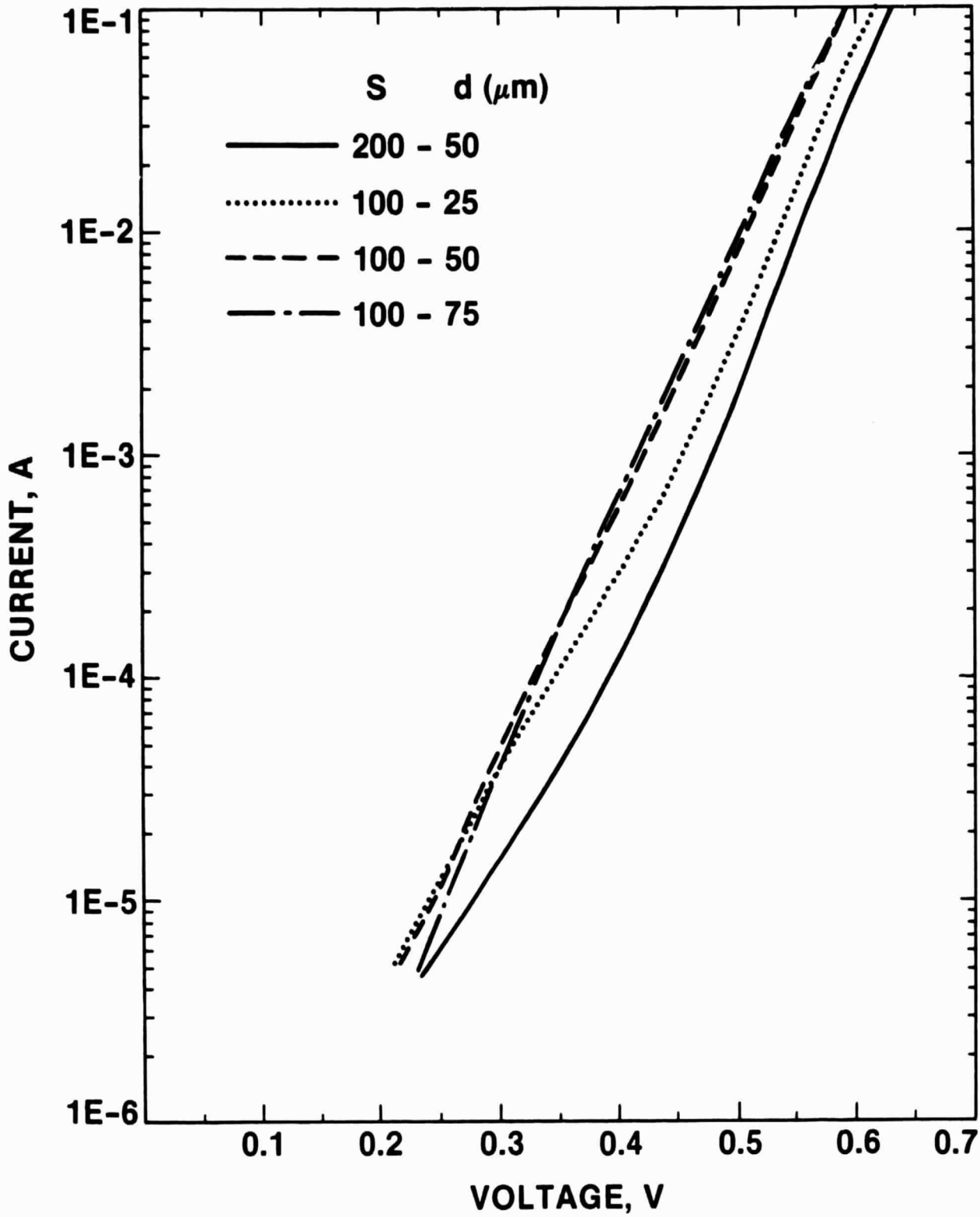


Figure 6-1. Dark I-V Characteristics of Dot Collector Solar Cells

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APPENDIX A

COMPUTER PROGRAM FOR SOLAR-CELL MODELING

```
100 REM       ****************************************
110 REM       *                                      *
120 REM       *   DOT COLLECTOR SOLAR CELL MODELING  *
130 REM       *                                      *
140 REM       *          DATE 12-26-84               *
150 REM       *                                      *
160 REM       ****************************************
170 PRINT @37,26:0
180 PAGE
190 INIT
200 N=124
210 Y=150
220 DIM W1(N),Eph(N),A1(N),A(2),C(2),E0(3),E1(3),F9(N),M1(N),P(2)
230 DIM Nph(N),W2(N),Vo(Y),Io(Y),Po(Y)
240 T=300
250 Zt=0.03
260 READ Q,Q1,H1,C0,Vt
270 REM ---------------------------------
280 REM READ AM 1.5 GLOBAL DATA FROM FILE 1
290 REM *********************************
300 FIND 1
310 FOR I=1 TO N
320    INPUT @33:W1(I),Eph(I)
330 NEXT I
340 REM ---------------------------------------
350 REM CALCULATE ABSORPTION COEFFICIENT, ALPHA
360 REM *****************************************
370 READ B2,G1,C(1),C(2),A(1),A(2),A4,K0,E0(1),E0(2),E0(3)
380 READ P(1),P(2),H2
390 FOR I=1 TO 3
400    E1(I)=E0(I)-B2*T^2/(T+G1)
410 NEXT I
420 FOR K=1 TO N
430    F9(K)=1.239644/W1(K)
440    A1(K)=0
450    FOR I=1 TO 2
460       FOR J=1 TO 2
470          M1(K)=0
480          IF F9(K)<E1(J)-P(I) THEN 530
490          M1(K)=C(I)*A(J)*(F9(K)-E1(J)+P(I))^2/(EXP(P(I)/(K0*T))-1)
500          IF F9(K)<=E1(J)+P(I) THEN 530
510          Z1=C(I)*A(J)*(F9(K)-E1(J)-P(I))^2/(1-EXP(-P(I)/(K0*T)))
520          M1(K)=M1(K)+Z1
530          A1(K)=A1(K)+M1(K)
540       NEXT J
550    NEXT I
560    IF F9(K)>E1(3) THEN 580
```

```
570     GO TO 600
580     M1(K)=A4*(F9(K)-E1(3))^0.5
590     A1(K)=A1(K)+M1(K)
600 NEXT K
610 DATA 32,1.601864E-19,6.623773E-34,2.9979022E+10,0.02586
620 DATA 7.021E-4,1108,5.5,4,323.1,7237,1052000,8.616E-5,1.1557,2.5
630 DATA 3.2,0.01827,0.05773,6.582E-16
640 REM     ------------------------------------
650 REM     CALCULATIONS FOR SHORT CIRCUIT CURRENT
660 REM     ************************************
670 IF Q=32 THEN 690
680 PRINT @37,26;1
690 Dr=2.5E-4
700 N1=100
710 N2=60
720 N3=74
730 Lb=0.01
740 PRINT @Q;"  Lb     S     D     Voc     Jsc     FF      EffJ"
750 FOR N4=1 TO 3
760     S=0.005
770     FOR L1=1 TO 4
780         S1=S*10000
790         PRINT @Q; USING 2280;Lb*10000,S1
800         R1=0.00125
810         FOR M2=1 TO 8
820             D=2*R1*10000
830             C6=0
840             C3=0
850             FOR I=1 TO N3
860                 Z2=0
870                 U=0
880                 IF A1(I)>1000000 THEN 980
890                 IF A1(I)>400000 THEN 1000
900                 IF A1(I)>100000 THEN 1020
910                 IF A1(I)>40000 THEN 1040
920                 IF A1(I)>10000 THEN 1060
930                 IF A1(I)>4000 THEN 1080
940                 IF A1(I)>1000 THEN 1100
950                 IF A1(I)>100 THEN 1120
960                 Dz=0.005
970                 GO TO 1130
980                 Dz=5.0E-8
990                 GO TO 1130
1000                 Dz=1.0E-7
1010                 GO TO 1130
1020                 Dz=5.0E-7
1030                 GO TO 1130
1040                 Dz=1.0E-6
1050                 GO TO 1130
1060                 Dz=5.0E-6
1070                 GO TO 1130
1080                 Dz=1.0E-5
1090                 GO TO 1130
1100                 Dz=5.0E-5
```

```
1110              GO TO 1130
1120              Dz=1.0E-4
1130              IF I)1 THEN 1160
1140              W2(I)=0.0032
1150              GO TO 1170
1160              W2(I)=W1(I)-W1(I-1)
1170              Nph(I)=W1(I)*1.0E-8*A1(I)*Eph(I)*W2(I)/(H1*C0)
1180              FOR J=1 TO N1
1190                 R=R1
1200                 Az=A1(I)*(Z2+Dz/2)
1210                 C8=0
1220                 IF Az)100 THEN 1680
1230                 FOR K=1 TO N2
1240                    IF R(S/2 THEN 1270
1250                    C2=8*(R+Dr/2)*ACS(S/(2*(R+Dr/2)))
1260                    GO TO 1280
1270                    C2=0
1280                    C9=(2*PI*(R+Dr/2)-C2)*Dr*EXP(-SQR((R+Dr/2-R1)^2+(
                        Z2+Dz/2)^2)/Lb)
1290                    C8=C8+C9
1300                    R=R+Dr
1310                    IF R=)S/2^0.5 THEN 1330
1320                 NEXT K
1330                 Dt=PI*R1^2*EXP(-(Z2+Dz/2)/Lb)
1340                 Ex=EXP(-Az)
1350                 C7=Nph(I)*Ex*Dz
1360                 C6=C6+C7*(Dt+C8)
1370                 IF U=)1 THEN 1410
1380                 IF Az(=0.5 THEN 1650
1390                 U=1
1400                 Dz=Dz*2
1410                 IF U=)2 THEN 1450
1420                 IF Az(=1 THEN 1650
1430                 U=2
1440                 Dz=2*Dz
1450                 IF U=)3 THEN 1490
1460                 IF Az(=2 THEN 1650
1470                 U=3
1480                 Dz=2*Dz
1490                 IF U=)4 THEN 1530
1500                 IF Az(=4 THEN 1650
1510                 U=4
1520                 Dz=4*Dz
1530                 IF U=)5 THEN 1570
1540                 IF Az(=10 THEN 1650
1550                 U=5
1560                 Dz=4*Dz
1570                 IF U=)6 THEN 1610
1580                 IF Az(=20 THEN 1650
1590                 U=6
1600                 Dz=10*Dz
1610                 IF U=7 THEN 1650
1620                 IF Az(40 THEN 1650
1630                 U=7
```

```
1640                Dz=10*Dz
1650                Z2=Z2+Dz
1660                IF Z2=>Zt THEN 1680
1670             NEXT J
1680          NEXT I
1690          C1=Q1*C6*1000/S^2
1700          GOSUB 1810
1710          R1=R1+0.00125
1720          IF S<2*R1 THEN 1740
1730       NEXT M2
1740       S=S+0.005
1750    NEXT L1
1760    Lb=Lb+0.01
1770 NEXT N4
1780 PRINT @37,26:0
1790 PRINT "JJJJJJJJJJ                    ALL DONEGGGGG"
1800 END
1810 REM   ----------------------------------------
1820 REM   CALCULATIONS FOR Voc, FF, AND EFFICIENCY
1830 REM   ****************************************
1840 Z=0
1850 Isc=C1/1000
1860 Num=PI*1.6E-19*1.45E+10^2*15
1870 Den=4*1.5E+16*Lb
1880 Revi=Num/Den*(D/S1)^2
1890 FOR I0=1 TO 20
1900    Vo(I0)=I0*0.05
1910    Io(I0)=Isc-Revi*(EXP(Vo(I0)/Vt)-1)
1920    IF Z=1 THEN 2080
1930    Po(I0)=Vo(I0)*Io(I0)
1940    IF I0=1 THEN 2080
1950    IF Po(I0)>Po(I0-1) THEN 2080
1960    FOR L=1 TO 12
1970       M=I0+L-1
1980       Vo(M)=Vo(M-1)+0.005
1990       Io(M)=Isc-Revi*(EXP(Vo(M)/Vt)-1)
2000       Po(M)=Vo(M)*Io(M)
2010       IF Po(M)>Po(M-1) THEN 2060
2020       Pm=Po(M-1)
2030       Z=1
2040       REM
2050       GO TO 2080
2060       REM
2070    NEXT L
2080    IF Io(I0)<0 THEN 2120
2090    REM
2100 NEXT I0
2110 END
2120 FUZZ 5,9.0E-4
2130 FOR K=1 TO 100
2140    J=I0+K-2
2150    Vo(J)=Vo(I0-1)+(K-1)*1.0E-3
2160    Io(J)=Isc-Revi*(EXP(Vo(J)/Vt)-1)
2170    IF Io(J)<=0 THEN 2210
```

```
2180 NEXT K
2190 PRINT "JJ   Voc NOT FOUNDGGG"
2200 RETURN
2210 Voc=Vo(J)
2220 Ff=Pm/(Voc*Isc)
2230 Eff=Pm*1000
2240 Jsc=Isc*1000
2250 PRINT @Q: USING 2270:D,Voc,Jsc,Ff,Eff
2260 RETURN
2270 IMAGE 12X,3D,2X,D.3D,2X,3D.D,2X,D.3D,2X,2D.2D
2280 IMAGE 2X,3D,2X,3D
```