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Proceedings of the Cold Electronics Workshop

October 4-5, 1983
Pasadena, California

E. Tward
R. Kirschman
Editors

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Department of the Navy
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ABSTRACT

The Proceedings of the Cold Electronics Workshop held at the Jet Propulsion Laboratory on October 3 and 4, 1984 are documented. Papers presented and discussions centered on the benefits and problems of the use of cold semiconductor electronics and the research and development effort required to bring cold electronics into more widespread use.

The report includes an overview of the status of cold electronics usage and research, summaries of the invited presentations and workshop discussions, recommendations for future research and development and copies of papers which were submitted by the invited speakers.

PREFACE

This report documents the proceedings of the Cold Electronics Workshop held at the Jet Propulsion Laboratory in Pasadena, California on October 4 and 5, 1983. The workshop was sponsored by the Office of Naval Research through Dr. E. A. Edelsack and by the Jet Propulsion Laboratory. The opinions, findings and conclusions expressed are those of the authors solely, who have attempted to represent to the best of their ability the discussions of the participants.

The workshop was organized in four half-day sessions and included presentations by invited speakers on a variety of relevant topics. Following the presentations, three topical discussion sessions and a final main discussion session were held in order to ascertain the viewpoints of the participants with respect to the potential for significant technical progress in cold electronics and the research and development efforts required for this progress to be achieved.

Because of the nature of the meeting, it was not advertised. All participants were invited personally by the undersigned, who takes all the blame for being unaware of other worthy contributors. The success of the meeting is due to the 65 participants whose efforts are gratefully acknowledged. I especially wish to thank Mrs. Genevieve McKay for her excellent help in organizing the conference.

E. Tward
Conference Chairman

CONTENTS

I. INTRODUCTION

Cooling of electronics to cryogenic temperatures is a commonly used procedure in a number of scientific areas. Semiconductor devices have been operated below room temperature to temperatures as low as 1 K. Superconducting devices are operated at temperatures below approximately 20 K where the phenomenon of superconductivity exists. The Cold Electronics Workshop focussed on the use of semiconductor devices at cryogenic temperatures and did not discuss superconductivity.

The meeting was held because it was apparent to the organizers that there was no common forum for discussion for both the users of cold electronics and those wishing to advance the state of the art in this field. The users in fields such as radio astronomy, infrared sensing and nuclear physics have themselves traditionally found a way to satisfy their special needs for essentially special purpose devices. These applications make use of cold semiconductor devices to take advantage of either low noise properties or the need for close coupling of the devices. For some applications, e.g., infrared sensing, the sensors themselves must be cooled as well and therefore an independent cooling system for the electronics is not required. For other applications, e.g., microwave receivers, the antennae are warm but the front end receivers are cooled and therefore require their own cooling systems.

The formal presentations and workshop discussions attempted to cover the field of cold electronics as broadly as possible. The topics addressed included novel fabrication techniques, new promising devices (e.g., HEMT), the status of cold Si devices, refrigeration, and the needs of users. A copy of the program is appended in Appendix A. The invited participants were drawn from industry, government laboratories and academia. A list of attendees is appended in Appendix B. Included in Appendix C are papers or summaries of presentations from the presenters who responded to the seductive entreaties of the editors to do more than their initial commitment to speak. Their additional efforts in providing these materials are gratefully acknowledged.

The broad scope of the program reflects the situation of a field in its infancy, with great promise for technical pay-off and wide ranging opportunity and need for research and development. The technical promise of cold electronics lies in its potential for yielding improved performance and reliability. For example, for VLSI devices, lowering operating temperatures can provide increased speed due to higher carrier mobilities, lowered interconnection resistances, improved heat removal, lowered power dissipation, and orders of magnitude improvement of reliability due to reduction of thermally activated degradation mechanisms. For many IR sensor applications, low noise requirements of amplifiers dictates the use of low temperatures. For microwave receivers high frequency response and low noise are

prime considerations for applications in radio astronomy.

In any event, in most applications where cold electronics is in use or is being considered for use, the enhancement of device characteristics results from the basic improved physical properties of the materials at low temperatures. For this reason there is a great need for basic research into the properties of materials as well as device design and engineering for low temperature operation.

In order to put into context the present status of the field, we include in the report an overview of cold electronics which includes a bibliography as a starting point for those who wish to investigate the field in greater depth.

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II. COLD ELECTRONICS - AN OVERVIEW

R. Kirschman

The present trends in electronics toward ultraminiaturization and higher performance are intimately tied in with lower temperature operation. As materials are made purer and more ordered, as structures are made smaller, and as signal levels are reduced in electronic devices and circuits, thermal effects can become increasingly important and hence reducing the temperature can lead to correspondingly greater benefits.

Cold electronic systems in use or contemplated range from single-transistor amplifiers to computer systems employing many VLSI integrated circuits. The primary areas, as described in this overview, are listed in Table I. Generally speaking, several roles are seen for low temperatures in electronics:

> As a means of extracting better performance from existing technology, avoiding expense and delay required for the advances in design or fabrication which would be needed to achieve the same performance at room temperature.
>
> As a necessity in the quest for improved performance, to counteract detrimental effects which arise as technology is pushed to extremes.
>
> As an opportunity to take advantage of effects made available by low temperature operation, and to develop new devices based on them.[1]

The object of this overview is to briefly describe the various devices, applications, and performance factors involved in cold electronics, and how these relate to materials and technology. The electronic devices and circuits treated in this overview are those based on semiconductivity. Superconductive devices and circuits are not included; information on these can be found in references 2 through 10.

As is reasonable to expect, most work on cold electronics has been along the lines of adapting and extending existing technology. The potential of devices and circuits which are designed and optimized with low-temperature operation in mind from the outset is still largely unknown and unexplored.

TABLE I

COLD SEMICONDUCTOR ELECTRONICS

Material	Device	Temperatures	Applications
Ge	Bipolar	> 100 K	--
	discrete JFET	liquid helium and above	low frequency amplifiers, oscillators
Si	Bipolar	> 100 K	--
	discrete JFET	liquid helium and above	low frequency amplifiers, oscillators
	discrete MOSFET	liquid helium and above	low frequency amplifiers, oscillators
	VLSI MOSFET	liquid nitrogen	high-speed logic (proposed)
GaAs	discrete MESFET	20 K and above	low-noise microwave amplifiers
	LSI/VLSI MESFET	liquid nitrogen	high-speed logic and fast/high frequency instruments (proposed)
GaAs/AlGaAs	discrete HEMT	20 K and above	low-noise microwave amplifiers (proposed)
	LSI/VLSI HEMT	liquid nitrogen	high-speed logic and fast/high-frequency instruments (proposed)

MATERIALS AND DEVICES

The use of semiconductor materials for cold electronics by and large reflects the situation at room temperature. The principal material is Si, with GaAs showing promise, and Ge being used for a few specialized purposes. Other materials,[11] as well as devices other than those discussed below, might be valuable for low-temperature electronics, but it is unlikely that the considerable effort needed to develop their fabrication technologies would be undertaken solely on the basis of low-temperature applications.

Nearly all active semiconductor devices being used and considered for cold electronics are of the FET (field-effect transistor) family. Bipolar transistors are not now being considered to any degree because those made with standard techniques and materials do not function satisfactorily at temperatures below about 100 K.[12-15]

Almost since their commercial appearance about twenty years ago, discrete Si and Ge JFETs (junction FETs) and Si MOSFETs (metal-oxide-semiconductor FETs) have been evaluated at low temperatures and used in experimental research involving low temperatures.[16-21] A prime example is the system in the Infrared Astronomical Satellite (IRAS),[22,23] which uses Si JFETS as the active elements in low-frequency impedance-matching preamplifiers for the infrared detectors which are cooled to liquid-helium temperatures.

Cooled GaAs MESFETs (metal-semiconductor FETs) have provided outstanding results in low-noise receivers at microwave frequencies[24] for applications such as radio astronomy.[25-26] The HEMT, a recently developed type of FET described below, is predicted to yield even better performance, approaching that of MASERs.[25]

GaAs MESFETs are also being considered for high-speed digital ICs expected to be several times faster than those based on Si.[12] Experiments indicate that their performance improves at low temperatures.[27] Cold GaAs could provide high performance for specialized applications feasible with low-complexity ICs. At present GaAs is not capable of the integration complexity attainable with Si since its fabrication has not matured; however, such technology is being developed rapidly.

At this time the Si MOSFET is the prime candidate for low-temperature digital applications because of its predominance in room-temperature IC technology coupled with the fact that MOS devices work at low temperatures and exhibit increased speed.[15,28,29] Conventional depletion-mode devices have exhibited undesirable threshold voltage behavior and other effects related to freeze-out of threshold-adjusting impurities,[14,30,31] which has been an impediment to cold NMOS.

Although these difficulties could probably be overcome, interest has shifted to CMOS, which is based on enhancement-mode devices and is coming to the forefront in room-temperature electronics. Enhancement-mode devices exhibit better behavior at low temperatures[14,32] and p- and n-channel types can be made to exhibit symmetrical threshold variation with temperature, allowing CMOS logic circuits to function from room temperature down to liquid-helium temperatures.[33] Thus, it is likely that Si CMOS will be the leading technology for cold electronics for computers.

When bulk CMOS circuits are operated at low-temperature, latch-up is suppressed because the gains are reduced in the parasitic bipolar structures.[28,33,34] On the other hand charge trapping in insulators, such as SiO_2 which is a key ingredient in MOS technology, and consequent unacceptable shifts in device characteristics can become exaggerated at low temperatures.[32,35,36]

DEVICE SPEED

The switching speed of semiconductor devices, a central concern for digital applications, can be increased by lowering their temperature (Fig. 1). Increased device speed is useful only in the context of an integrated circuit, and here too, reduced temperatures could provide benefits related to the interconnections, heat removal, and power as described later. The temperature most frequently considered in this context is that of liquid nitrogen since it is convenient and can provide significant improvements in performance.

Higher speed in FET devices at low temperatures results from higher mobility and transconductance which in turn result from reduced thermal scattering of carriers. Factors of 2 to 3 improvement in speed have been demonstrated in Si MOSFETs[14,28,29,33,37,38] as well as GaAs MESFETs.[27,38]

In conventional FETs this improvement occurs primarily on cooling to liquid nitrogen temperatures, with relatively little increase in speed for further reduction in temperature.[38] This is because carrier flow is still disrupted by non-thermal scattering, such as from ionized impurities, which persists at low temperatures.

The situation can be improved by spacially separating the carriers from the impurities necessary for their generation, so that non-thermal scattering is drastically reduced (Fig. 2).[39-41] This is achieved in the HEMT (high electron-mobility transistor),[42] a recently-developed FET device which is faster than a conventional FET even at room temperature, and improves rapidly as temperature is lowered. A switching time of 13 ps at liquid-nitrogen temperature has been reported.[12,43] As mentioned

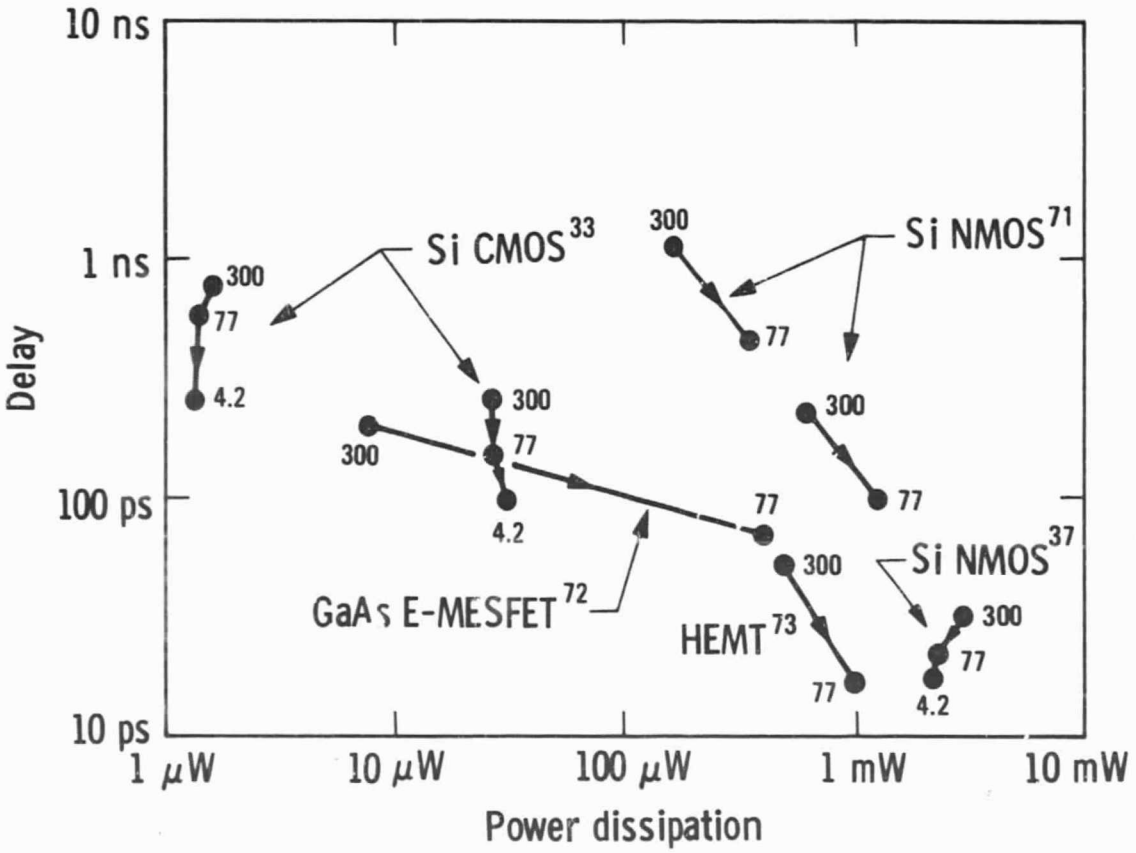

Fig. 1. Effect of reduced temperature on speed and power for logic gates based on semiconductor devices. Small numbers next to data points indicate temperatures in K.

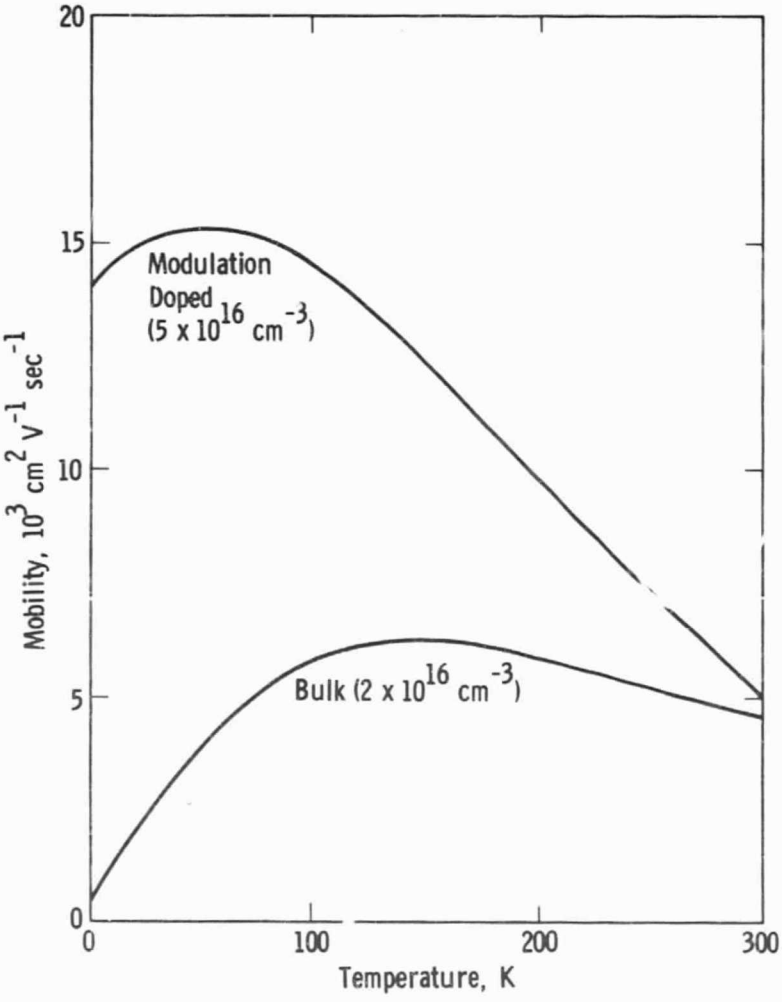

Fig. 2. Comparison of electron mobility at low temperatures for modulation-doped GaAs/AlGaAs structure, as used in the HEMT, and uniformly doped bulk GaAs, as used in conventional FETs.[41]

earlier, the HEMT also shows great promise for low-noise microwave amplification,[25] with predicted 12-GHz noise figures of a fraction of a db even when cooled only to liquid-nitrogen temperatures.[39]

The present realization of the HEMT is with GaAs technology; but its fabrication is more complicated than that of a conventional GaAs FET, requiring the sophisticated techniques of molecular-beam epitaxy (MBE) or organo-metallic vapor-phase epitaxy (OMVPE) to deposit the layers essential to the device's operation.[39] Thus, at present, the technology is in its infancy; however, it is likely that development will be pursued vigorously because of the HEMT's superior performance at room temperature.

Under certain conditions, one of which is low temperature, carrier transport in these devices may not reach steady state, and the effects of velocity overshoot and "ballistic" transport become important.[44-46] Investigations in this area are still in the early stages, but could lead to even faster, lower-noise devices.[39]

INTERCONNECTIONS

As individual device speed increases, interconnections between devices on an IC chip become no less important than the devices themselves in determining the overall speed in complex digital circuits.[12,47] Particularly so since as devices shrink, ICs are expected to become more dense and at the same time larger, resulting in interconnecting lines of smaller cross section and greater length.

Thus, ultimately it may not matter which device or semiconductor material is chosen for complex ICs since the speed could be limited by the parasitic resistance and capacitance of interconnections rather than by the inherent speed of the individual devices.

Whether the speed is interconnection limited or not, reducing the temperature is seen as a possible means to improve performance because it lowers the resistance of interconnecting materials.[12,48] The experimental data available (Fig. 3) indicate about an order of magnitude reduction of resistance of aluminum lines of the type used in integrated circuits and slight reduction for polysilicon and for doped silicon such as used in device contacts.[28,33,49] These results are for dc; none are available for fast pulses and high frequencies found in high-speed logic and microwave applications. Likewise, data are lacking for more recently developed metallization and contacting schemes such as those incorporating refractory metals and silicides, or those used with newer semiconducting materials such as GaAs.

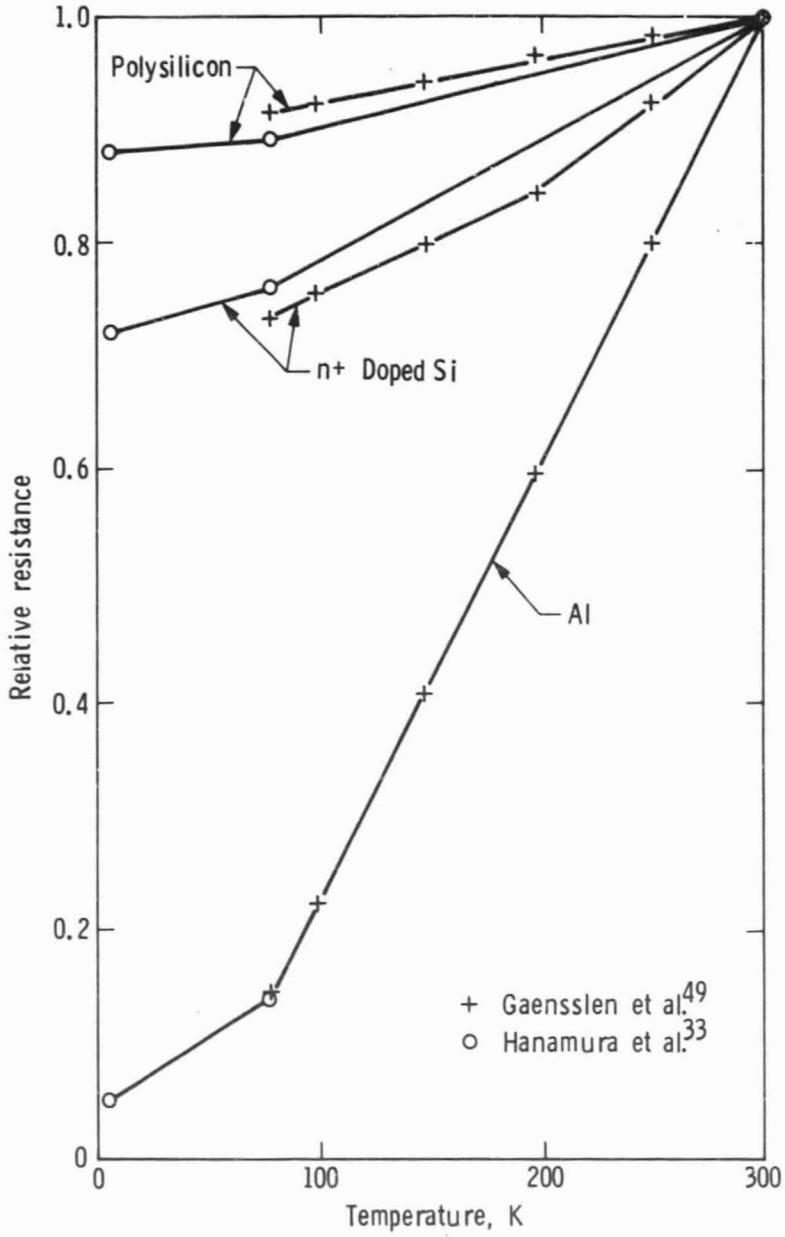

Fig. 3. Resistance as a function of temperature for some materials commonly used as interconnections in integrated circuits. The resistance data are normalized to their room temperature values.

An attractive possibility for circuits operating at temperatures below about 20 K is the use of superconducting interconnections for highly efficient conduction and signal transmission.[7,48,50]

Dielectric characteristics of materials used in ICs also affect the propagation of signals and circuit performance. Although capacitance is not expected to change significantly, dielectric losses should decrease at low temperatures.

HEAT REMOVAL

To achieve high speed in digital ICs the circuit elements must be close together to keep signal propagation times short; however, an increase in the density of circuit elements is accompanied by an increase in power density, and for room temperature this has become a limiting factor in circuit performance because of the difficulty of heat removal.[12]

Even for room temperature electronics, improvements in heat removal can be made;[51] additional improvement may be possible at lower temperatures by taking advantage of the fact that many materials used in electronics exhibit an increase in thermal conduction. This is the case for fairly pure, ordered materials; those commonly encountered in electronics include single-crystal semiconductors--Si, Ge, GaAs; single crystal dielectric materials--sapphire, quartz, diamond; some polycrystalline materials--alumina and beryllia; and relatively pure metals--copper or aluminum, usually. As shown in Fig. 4, their thermal conductivity increases as temperature is reduced and peaks at as high as an order of magnitude or more times its room temperature value.[52,53] How much practical use can be made of this effect in actual electronic systems remains to be seen.

Unfortunately, the thermal conductivity of many of the other materials commonly used in electronics, including metal alloys, glasses, and polymers, decreases monotonically as temperature is lowered.[52] In any case, careful attention to packaging will be required for cold electronics as it is for room temperature systems.

Liquids might also be employed in heat removal either by direct contact with circuit chips or indirectly. However, the amount of heat that can be removed by this means is reduced at low temperatures, being approximately proportional to the absolute emperature.[48]

POWER

Besides improving heat removal, another approach is to attack the thermal problems of dense circuits at their source and reduce power dissipation. Hence, reduction of power, besides

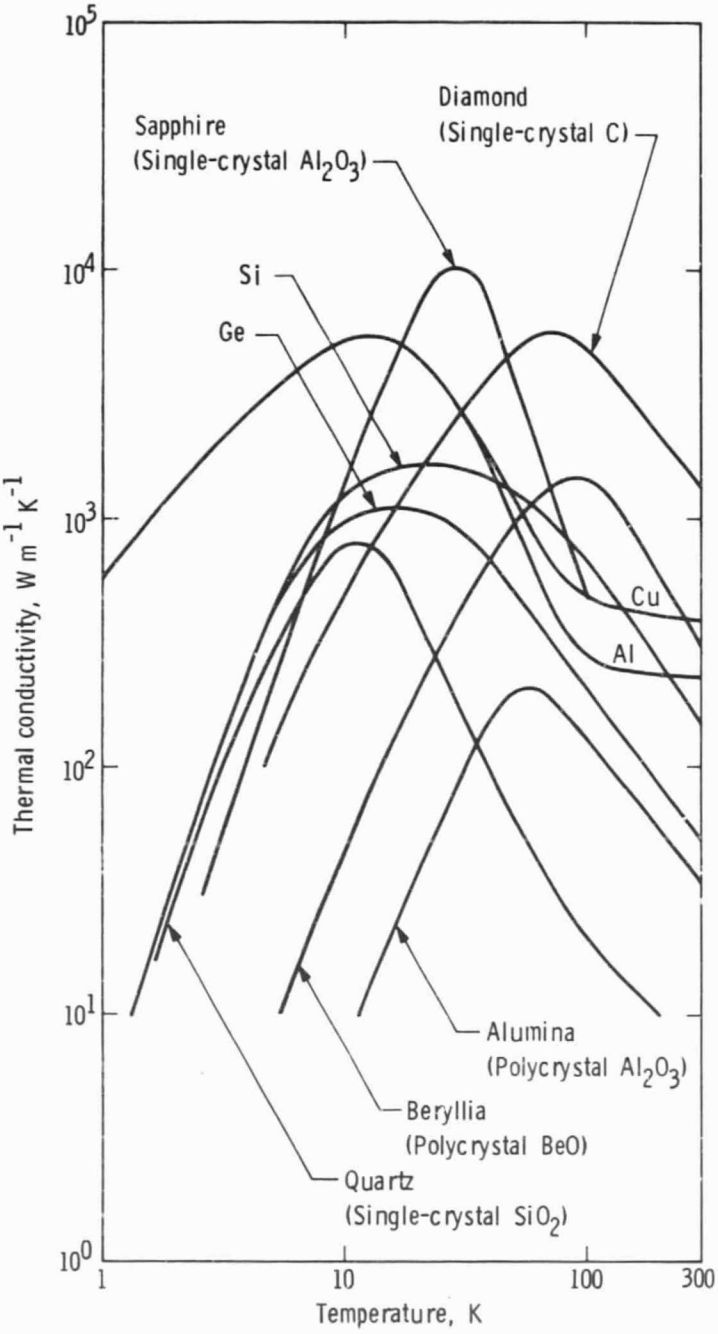

Fig. 4. Behavior of thermal conductivity at low temperatures for various materials which might be used in cold electronics.[53] These curves only indicate general trends since the low-temperature thermal conductivity of a material is very sensitive to its form and purity.

being desirable in itself, has also become a central issue in attaining higher speed.

One means of reducing power is through lowering operating voltages. Operating temperature becomes a factor because voltages in logic circuits must remain large compared to the thermal voltage kT/e.[12,27,38] Consequently, if circuit voltages are to be reduced beyond a certain point, about 1 volt, temperature must be reduced also.

Another effect pertinent to power consumption is that leakage in p-n junctions and insulators is significantly reduced as temperature is lowered. Thus, for example, memories based on p-n junctions or MOS capacitors will require less power to maintain stored data.[28,34,54]

NOISE

Although noise has non-thermal as well as thermal origins, substantial improvements have been made in some circumstances by means of cooling. A prime example is the use of GaAs FET microwave amplifiers at about 20 K for radio astronomy as mentioned earlier.[25-26] In some cases such as these the improvements also result partly from changes in device parameters such as transconductance which effectively reduce the noise.

Low frequency noise measurements on discrete Si and Ge JFETs and Si MOSFETs have yielded mixed results, frequently showing an increase in noise at low temperatures. A 1/f dependence is commonly observed. Overall, JFETs appear to exhibit lower noise than MOSFETs.[16,17,20,21,55-58]

LIMITATIONS

There are bounds to the improvements in performance that can be derived from the effects described above. Lowering of operating temperature along with reduction of dimensions, voltages, and energies can only be carried so far before limitations of a non-thermal nature appear.[12,27,28,47] Scattering of carriers by impurities or defects has been mentioned; other examples are (1) statistical variation in device characteristics which limits the extent to which voltages can be reduced if noise margins are to be retained, (2) cross-talk as spacings of devices and interconnections shrink, and (3) quantum effects.

RELIABILITY

Since nearly all degradation mechanisms in electronic devices, such as interdiffusion, corrosion, and electromigration, have a thermal-activation component and an exponential dependence on temperature, orders-of-magnitude improvement in reliablity is expected upon cooling.[48]

Although the effect of temperature on reliability has been thoroughly verified empirically for elevated temperatures, it is difficult to demonstrate that it holds true for reduced temperatures as well because of the extremely low rates involved. However, electronic devices now being developed with circuit patterns smaller than 1 μm and layers 10 nm thick may provide the testing ground. Such devices may exhibit an unacceptably high failure rate for room temperature operation and storage.[59] Thus, reduced temperatures may prove essential in maintaining the structure and characteristics of advanced electronic circuits as the drive to ever-smaller dimensions continues.

THERMAL CYCLING

In actual practice the predicted improvement in reliability outlined above is offset by the detrimental effect of mechanical stresses and strains which result from differences in thermal expansion of the various materials used in electronic components, coupled with local and overall temperature differences arising when the system is taken from room temperature to the lower operating temperature or vice versa.

Such effects are already well known for the temperature excursions experienced by conventional electronics, and although troublesome, means have been developed of effectively dealing with them. Thus, although the problem is more severe for cold electronics because of the greater temperature differences, it is reasonable to believe that it can likewise be dealt with effectively if appropriate development is undertaken.

Some background is already available as a result of Josephson computer development,[60,61] as well as from work on non-electronic cryogenic equipment.

A Josephson computer would probably need the ability to survive several hundred cycles for commercial practicality.[62] Systems based on semiconducting devices might not require as many cycles since, unlike Josephson devices, it is feasible to design them to function at room temperature as well as at their lower operating temperature. Thus, many basic tests could be performed at room temperature both during initial testing and for maintenance, although testing of ultimate performance would require cooling to the operating temperature.[28]

COOLING

Realizing the potential of cold electronics means that a cold environment must be provided. In some situations this environment is already available, such as for preamplifiers used with sensors which must operate at reduced temperatures, or possibly for spacecraft where heat can be radiated to space.[63,64] However, for the remaining systems cooling is a major concern.

Heat loads range from a few milliwatts for a single electronic device or small component to an estimate of about a hundred watts for the electronic system of an advanced computer.

For most applications, "open-cycle" cooling by consumption of a liquid cryogen is seen as impractical, leaving as the only alternative at present the mechanical refrigerator. Although other means of cooling exist, for one reason or another they are not considered suitable.

A variety of mechanical refrigeration units is available to cover the range of heat load and temperature requirements for cold electronics; however, further development is needed, primarily along the lines of further improvement in reliability, efficiency, and low-temperature capability (below about 20 K).[65-68] Present designs also exhibit some undesirable characteristics including: (1) mechanical vibration, (2) magnetic interference, and (3) a periodic temperature fluctuation or "ripple".

A cryogenic refrigeration system is not a major obstacle in the case of an advanced computer since it is a relatively large, fixed piece of hardware. Besides which, such computers already incorporate sophisticated cooling systems.

The concept of the hybrid cooling system has been proposed for cold electronic systems such as computers.[69] In this system the electronics package is immersed in a liquid cryogen bath which is maintained by a closed-cycle refrigerator. The undesirable characteristics of direct mechanical refrigeration mentioned above can be minimized and it also provides: (1) good heat transfer since the electronics may be directly immersed in the cryogen, (2) greater dependability since the cryogen bath would remain cold if the refrigerator malfunctioned or the power failed, and (3) easier maintainability since either the refrigerator or the electronics package could be removed for maintenance without shutting down the remainder of the system.

For smaller-scale systems such as instruments, the widespread use of cold electronics is hindered by a scarcity of suitable small, self-contained coolers, particularly for the lower temperatures, and by lack of experience with those that are available. The Peltier effect, which provides cooling by passing an electric current through a semiconductor, is an attractive method since the cooler is small and has no moving parts. Although it has been established as a practical means for cooling electronic components, the temperatures possible with present materials are not low enough for most of the applications discussed in this overview. Joule-Thomson[67,70] coolers are a possibility if continuous, closed-cycle operation can be developed.

Because refrigeration for the temperatures appropriate for cold electronics is characterized by low efficiency,[65,66] it is important that the heat load be minimized. A significant portion of the heat load can arise from leakage through electrical and mechanical interfaces which couple the cold electronics with room temperature. Electrical connections carrying signals are particularly troublesome, since they need low electrical resistance without high thermal conductance. In the case of high-speed or high-frequency measuring instruments it is also a major challenge to preserve an input signal to be analyzed while transferring it from room temperature to the cold electronics.[5] A proposed means of signal transfer which could prove advantageous is the use of optoelectronic techniques.

CONCLUSION

Cold electronic devices and circuits have already provided substantial benefits in certain applications, and theory and experiment indicate additional benefits to be derived from wider use of reduced temperatures, although a great deal of research and development remains in overcoming the technical hurdles to achieve practicality. Overall, it appears that lower operating temperatures will go hand-in-hand with other advances in electronic device and circuit technology for a variety of applications requiring the highest performance and reliability.

ACKNOWLEDGEMENTS

In addition to the references indicated, many of the ideas in this overview originated in the discussion sessions, formal and informal, at the Workshop. The manuscript was reviewed by E. Tward and V. Hadek, of the Jet Propulsion Laboratory, D. Ferry and R. Grondin of Arizona State University, S. Weinreb of the National Radio Astronomy Observatory, F. Gaensslen and P. Solomon of IBM Corporation, W. Steyert of Air Products and Chemicals, and M. Nisenoff of the Naval Research Laboratory, who provided valuable comments. Support for the preparation of this overview was provided by the Office of Naval Research (Dr. E. Edelsack).

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III. SUMMARY OF PRESENTATIONS

The first session of presentations included three on advanced semiconductor materials and devices and one on refrigeration.

M. YODER--Recent Developments in Semiconductor Research

M. Yoder from the Office of Naval Research presented some advanced topics in semiconductor materials and devices. A new technique called "atomic layer epitaxy" is claimed to produce crystalline films of certain semiconductor or other materials with exceptional purity, uniformity, and control of structure. A reliability problem is emerging for advanced electronic devices incorporating extremely small geometries and thin crystal layers, since diffusion, even at room temperatures, is sufficient to alter their structure and properties. Possible solutions are reduced temperatures or impeding the motion of impurities by complexing them. Recent advances in growing single-crystal β-SiC would make possible its wider use in electronic devices to take advantage of its excellent stability under adverse environments and high temperatures.

J. LAMBE--Novel Low Temperature Devices

J. Lambe of the Jet Propulsion Laboratory discussed the conditions under which quantum size effects would play a dominant role in electronic structures and how these might be employed in novel devices. An example is a "Stark-effect" transistor, a quantum-well structure in which the transfer characteristics arise from a shifting of the energy levels by an electric field from a control electrode. It is conceivable that devices could employ quantum effects even at liquid nitrogen temperatures.

R. RADEBAUGH--Refrigeration

R. Radebaugh of the National Bureau of Standards gave an overview of refrigeration principles and technology. There are a variety of refrigeration cycles and designs applicable to electronics, of which the most popular are variations of the Stirling and Gifford-McMahon. Effort is being devoted to improving reliability. Refrigeration becomes less efficient the lower the temperature and the smaller the capacity of a refrigerator; also, heat transfer in materials and to liquids is difficult at low temperatures. Proposed systems for cooling electronics include not only existing commercial refrigerators, but also a hybrid of mechanical refrigerator and liquid cryogen bath and novel methods such as closed cycle Joule Thomson refrigerators.

L. EASTMAN--Physical Electronics of Cooled Operation of Very Short Compound Semiconductor Transistors

L. Eastman of Cornell University described the dynamics of electron motion in short compound-semiconductor FET devices, and its bearing on their performance. Advanced fabrication techniques and low-temperature operation are expected to increase the already excellent high-frequency, low-noise capabilities of FETs. Of particular interest is the modulation-doped heterojunction (HEMT) device, in which extremely high electron velocities and mobilities have been obtained. Noise figures at liquid nitrogen temperatures of a fraction of a db at 12 GHz are predicted.

Session 2 contained three presentations on topics related to large-scale digital integrated circuits.

F. GAENSSLEN--Why Consider MOSFET Operation in Liquid Nitrogen?

F. Gaensslen of IBM described some of the reasons for cooling MOSFET devices to liquid nitrogen temperatures. When MOS devices are scaled down in size, some characteristics, such as subthreshold current, do not scale. These effects become a problem at about 1 μm gate length, but can be counteracted by a reduction in temperature. Reduced temperatures can also help to suppress latch-up as CMOS circuits are scaled down and to reduce leakage in p-n junctions which allows higher efficiency in semiconductor memory circuits. Advantage can also be taken of increased electrical and thermal conductivity at low temperatures.

R. GRONDIN--Effect of Cooling on Delay Time Limits in Integrated Circuits

R. Grondin of Arizona State University examined various factors which limit the highest speed attainable in integrated circuits. Speed is not only determined by the device technology and material, but also depends on heat removal and characteristics of the on-chip interconnections, particularly so as devices become smaller and IC chips become larger as the level of integration increases. In such situations speed may be increased by reducing the voltage, which in turn requires that the temperature be reduced also. In principle, this would allow a substantial increase by cooling to liquid nitrogen temperatures and another order of magnitude for liquid helium temperatures.

A. KAMGAR--SiMOS Devices at Low Temperatures

A. Kamgar of A T & T Bell Laboratories described improvements in the characteristics of silicon MOS devices which occur as temperature is reduced. Subthreshold slope increases so that less gate voltage swing is needed, especially for short-

channel devices. Punchthrough current in short-channel MOSFETs is also reduced. Measurements at liquid nitrogen temperatures of switching speed show about a factor 2 increase with a corresponding increase in power dissipation when compared to room temperature.

Session 3, the final two presentations, described the applications of cold devices and circuits to astronomy.

S. WEINREB--Cryogenically Cooled Low Noise Microwave Receivers--Present Status and Future Needs

S. Weinreb of the National Radio Astronomy Observatory reviewed the current status of low-noise electronics used in radio astronomy. Above about 100 GHz the SIS (superconductor-insulator-superconductor) device is being used as a mixer. For lower frequencies GaAs FETs are providing excellent results in receivers, when cooled to approximately 20 K to achieve ultra-low noise amplification. To make the actual receivers a number of technical problems with materials and electronic components had to be solved: for example, achieving minimum microwave signal loss while interfacing between 300 K and 20 K. The newly developed HEMT (high electron-mobility transistor) promises to provide outstanding low-noise performance and plans are under way to evaluate it for microwave applications.

F. LOW--Cryogenic Amplifiers for IR Detection

F. Low of the University of Arizona described the preamplifiers used with infrared detectors in the Infrared Astronomical Satellite (IRAS). The preamplifiers are based on silicon JFETs operating at approximately 60 K and are mounted adjacent to the IR detectors which are cooled to 2 K. Work is under way on a device with improved characteristics.

IV. SUMMARY OF THE DISCUSSION SESSIONS

A. Silver

Specialized technical presentations occupied the first part of the workshop. Three topical discussion sessions were organized on the second day:

1. Silicon and VLSI,
2. Non-silicon materials (principally GaAs),
3. Refrigeration.

The topical sessions discussed the material which was presented in the plenary sessions and developed a consensus. The conclusions were reported back to the workshop as a whole. The context in which the conclusions were discussed was:

a) advantages and disadvantages of cooling semiconductor electronics,

b) other technology which will be required to implement cold semiconductor electronics, and

c) recommendations for emphasis in R & D support.

The workshop covered widely diverse topics ranging from cooling production CMOS near 77 K for computing machines, to cooling commercial Si JFET's to 60 K for IR detectors, quasiparticle tunnel junctions to 4 K for millimeter and submillimeter wave detectors, and cooling GaAs HEMTs to 20 K. The separate discussion sessions extrapolated from the technical presentations to discuss other materials, processes, and applications.

Josephson technology was not a topic of this workshop, although passive superconductivity was discussed in the context of lower temperature semiconductors. The anomalous absence of this subject (Josephson technology) at a workshop on cold electronics was noted in the discussion session. Superconductive electronics was interpreted as a distinct technical area already receiving considerable interest and attention. The recent IBM project achieved notable successes in developing high performance logic at the 10^3 gates per chip level and a 1 K RAM using 2.5 micron lithography. The development of the technology at this point, particularly at IBM, points to near-term development of Josephson technology for small system applications rather than large general-purpose computing machines.

SILICON AND VLSI

Silicon CMOS can yield improved performance with existing manufacturing facilities if the devices and circuits are cooled to approximately 77 K (this temperature is chosen because it is

the boiling temperature of liquid nitrogen, commonly available in research and development laboratories and is above the carrier freezeout temperature of Si devices). The improvement is an increase of 2 to 3 in speed, with a corresponding increase in power dissipation. The use of cryogenic cooling to attain this improvement would be most likely to occur at the point of redesigning the circuitry for submicron lithography in order to achieve the next level of improvement in LSI, i.e., it may prove to be more desirable to redesign the 1.5 micron chip for cryogenic operation as compared to producing a submicron technology given the investment required in both chip design and production facilities. In addition, latching in CMOS will be greatly alleviated by cooling. Refrigeration for operation at liquid nitrogen temperatures (LN_2) for a mainframe digital computer may not present a significant penalty in total cost, size, and reliability when compared to the contemporary use of air conditioning equipment. One can expect to be able to test at room temperature in production, and reliability should be enhanced with respect to thermally activated failure mechanisms.

In addition to LN_2 operation of CMOS to achieve the increase in speed which would also be provided by submicron technology, there may be unknown advantages in operation of silicon devices at much lower temperatures below carrier freezeout. This will require new research and possibly novel devices in silicon. One motivation for this endeavor is the need for integration of low temperature sensors, both Si and other materials, with the associated signal processing circuitry. Variations in dopant can alter the carrier freezeout temperature. One may find new dependencies on such effects as fluctuation in doping concentration, radiation hardness dependence on lower temperatures, and possibly replacement of oxide insulators with nitrides.

Disadvantages in low temperature operation revolve about the refrigerator, access to the electronic system, reduced heat removal ability in LN_2 compared to fluorocarbons coupled with increased heat dissipation for faster logic, and the added problem of cryocooling for small digital systems.

Topics recommended for R & D reflected the areas of interest and possible improvement in silicon devices, low temperature CMOS, "carrier freezeout" devices, low temperature effects on radiation hardness, possible process technology changes for low temperature devices, and the design and process changes which might further enhance reliability through reduction in thermally activated degradation mechanisms.

NON-SILICON MATERIALS, PRINCIPALLY GaAs

This discussion session covered a wide range of materials and structures including III-V and II-VI compound semiconductors, epi-technologies and heterojunction devices, and both analog and

digital electronics. Since silicon is the established electronic technology, suggestions were tested by comparison to silicon, and to cooled silicon as presented at this workshop.

GaAs is presently finding a niche in analog microwave circuitry. Cooling to low temperatures lowers the device noise, except for 1/f noise, which will permit either deployment of smaller antennas or greater probability of intercept for weak signal transmissions. One may be able to develop a viable insulated gate technology at low temperatures in non-silicon because the surface state problems may be alleviated by extremely long lifetimes. Better noise margins in low noise devices may permit reduction of the digital voltage swings and hence lower power dissipation in digital circuitry. Coupled with the much greater mobilities of these materials, this could lead to faster real-time digital signal processors. This large mobility increase will also lead to higher frequency operation of microwave devices. As with silicon, reliability is expected to improve by reduction of thermal degradation mechanisms. Since many of these materials continue to improve in a significant manner well below 77 K, the reliability improvement should be substantially better than in Si. Compared with Si, carrier freezeout is much less of a problem, leading to the possibility of both FET and bipolar devices.

As with silicon, the disadvantages of cooling are the inconvenience of the refrigerator, the reduced heat removal rate, the difficulty of optimizing designs and testing at the low temperature, and the thermal cycling of the associated structures. In addition, the problems of optimizing thermal transition designs are more severe in analog applications where one is required to minimize both thermal conductance and microwave signal attenuation. Compared with silicon, where the application of cooling appears to be large main frame computers, the application of other cold semiconductors is projected in smaller analog and digital systems. Thus, the refrigerator is not merely a replacement for a conventional cooling system, but an added burden on system integration. Nevertheless, in areas of significant improvement this burden can be accommodated. An example of this is the present trend in high performance radio astronomy receivers which use both superconducting quasiparticle mixers and cooled GaAs low noise amplifiers.

Recommendations for R & D in the area of non-silicon materials relate to materials, processes, and system problems. Specifically included were heterojunction structures such as modulation doped and high-β bipolar devices. Of particular interest here were processing technology, noise performance, and bandwidth. In the area of materials technology, epi-techniques are used to significantly improve material purity, uniformity, and stoichiometry, and to eliminate alloy scattering. Ternary materials with improved transport properties, traveling wave devices, and semiconductor insulators were suggested as

potentially productive areas. Other materials which should be considered are small bandgap semiconductors because of their high mobility and low voltage operation. This could include InAs, InSb, and Ge, and also IGFET structures. The problem of both intra-chip and inter-chip signal propagation was recognized as one pushes to higher frequency or greater speed with high density lithography. Both optical and superconducting interconnects were suggested as possible solutions, particularly if monolithic structures could be developed.

REFRIGERATION

The introduction of cryogenic refrigeration will be a major step required for cold semiconductor electronics. The availability of closed-cycle cryocoolers will extend the operating temperature to 77 K, 20 K, and even below 4 K, depending on the semiconductor technology and application. Generally speaking, at least in the near-term, silicon computers would expect to operate near 77 K, with GaAs amplifiers and signal processors near 20 K, and detectors and sensors at the lowest temperatures. The nature of the refrigerator will depend strongly on the application and the operating environment--commercial, military, or space.

Refrigeration design choices will depend on the required reliability, allowable service interval, and acceptable cost, size, weight, and efficiency. Cryocoolers for large main frame computers at 77 K fall into the Gifford-McMahon (G-M) type and are available based on existing technology. This technology can also provide cooling down to 10 K at the 1 W refrigeration level; a combination of Joule-Thomson (J-T) and G-M cycles can provide cooling below 10 K and down to the 1 W power level in an office or laboratory environment with existing technology. Below 1 W, the split Stirling provides cooling to 15 K and 100 mW capacity. The region bounded by 1 W capacity and 15 K temperature is presently unsupported by existing technology and requires development for small system application. The very low power region may be satisfied by "plastic split Stirling" and small J-T machines.

A major problem with long continuous operation of a cryocooler is contamination of the working gas, commonly from seals or the compressor. Characteristically, regenerative systems are less sensitive to contaminants than J-T. It is desirable to keep the operating cryostat gas separate from the refrigerator gas, and to avoid a common vacuum. For operational purposes, it is desirable to have a liquid cryogen reservoir. The entire refrigerator should be designed and constructed as a self-contained unit.

Recommendations include a continuation of R & D on regenerative cycles to achieve 4 K operation at the 10 mW to 1 W power level, on closed cycle J-T systems, and on compressor

development for low power, continuous operating systems. $LaNi_5$ hydride H_2 solid state compressors, magnetic cold stages, and pulse tubes were cited as examples of alternative approaches to new refrigerator components.

V. NEEDED RESEARCH AND DEVELOPMENT

A primary goal of the Cold Electronics Workshop was to serve as a forum for recommendations of needed research and development. As a result of the Workshop, the following areas for future work were identified:

1. Basic investigations should be carried out on low-temperature properties of conductive and insulating materials used in integrated circuits to complement the work done on device characteristics. Systematic studies of resistivity and electromigration are needed for conductors, particularly for the newer metallization schemes being adopted in advanced-design ICs, and of dielectric properties and charge trapping for insulators.

2. Experimental confirmation of predicted improvements in reliability of electronic devices and circuits at low temperatures should be undertaken.

3. The tolerance at low temperatures of semiconductor devices and circuits to ionizing radiation should be investigated since it is suspected that reducing the temperature will have a detrimental effect.

4. Development should be continued and expanded on applications of cold electronics for use in conjunction with low-temperature sensors. Small-to-medium scale electronic systems for processing of signals from IR detectors, superconducting magnetometers, and similar scientific instruments would be valuable for both earth-based and spacecraft-borne applications.

5. Research and development on devices and circuits should be pursued vigorously, since they constitute the heart of any electronic system. Evaluation of their low-temperature applicability and performance should be continued as technological advances are made for room-temperature electronics, such as those arising from improved capabilities related to device dimensions coupled with control of crystal growth on an atomic scale. Equally important, additional research should be undertaken on materials, devices, and fabrication methods more suitable or optimized for low temperatures, many of which might not be useful for room temperature electronics. Quantum effects which could be troublesome in conventional devices might be taken advantage of in novel device designs.

6. Development of assembly and packaging materials and techniques is necessary to realize satisfactory performance in practical electronic systems at low temperatures. The electrical, thermal, and mechanical properties of materials at low temperatures need to be considered to take full advantage of the potential for improved performance of cold electronics. Techniques for effective electrical and mechanical interfaces

between cold electronics and room temperature electronics are needed.

7. Refrigeration must continue to be developed concurrently in order to make practical use of developments in cold electronics. New techniques are needed to provide cooling for measuring instruments for use outside the cryogenics laboratory and by persons who do not have a background in cryogenic techniques. For such applications, a need exists for the development of coolers that are compact, convenient, and reliable. In addition, many applications cannot tolerate the vibration, and temperature and magnetic fluctuations common in available designs. Cooling methods other than those based on mechanical systems and gas-liquid phases should be investigated.

Finally, the many interesting opportunities for fundamental research provided by electronic structures and devices at low temperatures should not be overlooked. For example, there are effects related to quantum behavior, "collisionless" carrier dynamics, superlattices, and confined particles.

APPENDIX A

COLD ELECTRONICS WORKSHOP

PROGRAM

Tuesday, October 4, 1983

9:00 a.m.	Welcome to JPL	T. Cole JPL
9:10	A Word From Our Sponsor	E. Edelsack ONR
9:15	Recent Developments in Semi-conductor Research	M. Yoder ONR
9:55	Novel Low Temperature Devices	J. Lambe JPL
10:35	coffee break	
10:55	Refrigeration	R. Radebaugh NBS
11:35	Physical Electronics of Cooled Operation of Very Short Compound Semiconductor Transistors	L. F. Eastman Cornell University
12:15	lunch	
1:30	Why Consider MOSFET Operation in Liquid Nitrogen?	F. H. Gaensslen IBM
2:10	Effect of Cooling on Delay Time Limits in Integrated Circuits	R. Grondin Arizona State Univ.
2:50	coffee break	
3:10	SiMOS Devices at Low Temperatures	A. Kamgar A T & T Bell Laboratories
4:15	Tour of JPL	
7:00	Reception and Dinner	Holiday Inn

Wednesday, October 5, 1983

9:00 a.m.	Cryogenically Cooled Low Noise Microwave Receivers - Present Status and Future Needs	S. Weinreb NRAO
9:40	Cryogenic Amplifiers for IR Detection	F. Low Univ. of Arizona
10:15	coffee break	
10:35	Individual Discussion Sessions	

	Si and VLSI	Refrigeration	Other Materials
locations:	180-101	230-115	264-739

12:15	lunch	
1:30	Main Discussion Session 180-101	Chairman: A. Silver, TRW

Workshop Organizer: E. Tward (818) 354-6581
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APPENDIX B

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APPENDIX C

WRITTEN CONTRIBUTIONS OF SPEAKERS

D2

N85-24222

Recent Developments in Semiconductor Research

by

M. N. YODER
Office of Naval Research

Abstract

Recent findings drawn from various laboratories around the world can be focused toward a new understanding of the nature of crystal growth and how impurities are incorporated or excluded from the lattice. From these findings a heuristic approach is given for improving the uniformity and charge carrier concentration of thin semiconductor films. Such improvement is considered essential to achieve respectable yield on large scale integrated circuits. A tentative conclusion is drawn which indicates that if the host compound crystal reactants are provided to the growing crystal surface in a reasonably stoichiometric manner, it is virtually impossible to include impurities into a growing crystal surface held at a sufficiently low temperature; impurities are incorporated into the crystal by "gettering" action of crystal defects located one and two monolayers beneath the growing surface. Devices in III-V semiconductors based on heterojunctions and two-dimensional electron gases are noted and reliability concerns are voiced. Alternatives and novel device structures such as truly single crystal high quality silicon on insulator and beta silicon carbide devices are presented.

ATOMIC LAYER EPITAXY
(A L E)

I. CLAIMS:

A. PURITY

B. PHENOMENAL CONTROL OF ABSOLUTE THICKNESS

C. EXTREME UNIFORMITY OVER LARGE AREA

D. INEXPENSIVE PROCESS

ALE GROWTH PRINCIPLE

- A SUBSTRATE GROWTH TEMPERATURE CAN BE FOUND WHEREIN THE CATION – CATION BONDS AND THE ANION – ANION BONDS WILL BREAK DURING THE SUBLIMATION PORTION OF THE CYCLE.

- AT THE SAME SUBSTRATE TEMPERATURE, CATION – ANION BONDS ARE TOO STRONG TO BREAK; THUS THE DESIRED CRYSTAL GROWS.

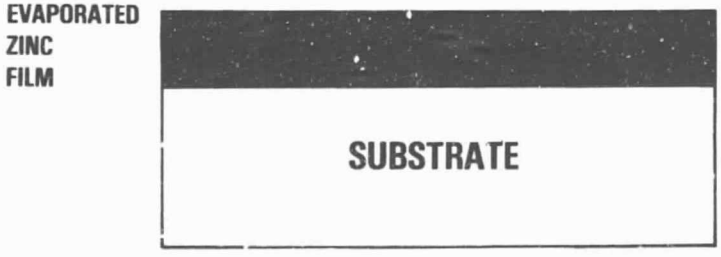
ALE GROWTH PRINCIPLE (con't)

- **GROWTH RATE AND STOICHIOMETRY ARE *INDEPENDENT* OF REACTANT FLOW RATES – THE ONLY KNOWN CRYSTAL GROWTH TECHNIQUE KNOWN TO BE INDEPENDENT OF FLOW RATE *AND* REACTANT UNIFORMITY.**

ALE PROCESS

(ZINC SULPHIDE ILLUSTRATION)

1. THOROUGHLY COVER SUBSTRATE WITH SEVERAL MONOLAYERS OF ZINC

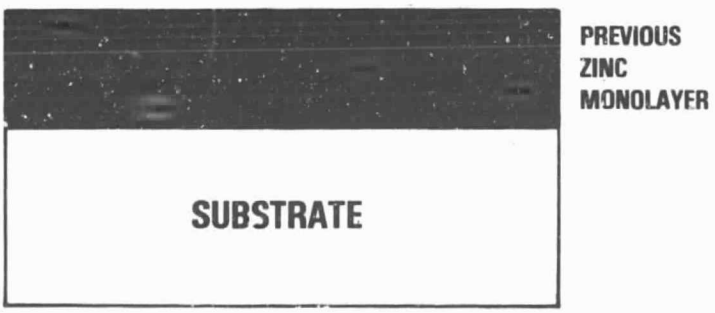


ALE PROCESS (CON'T)

2. STOP ZINC EVAPORATION
3. ALLOW ALL EXCEPT ONE MONOLAYER OF ZINC TO SUBLIME

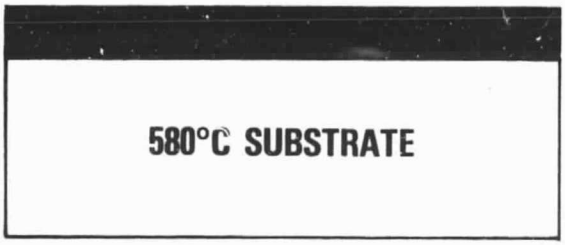
ALE PROCESS (CON'T)

4. EVAPORATE SUFFICIENT SULFUR TO COVER THE SUBSTRATE



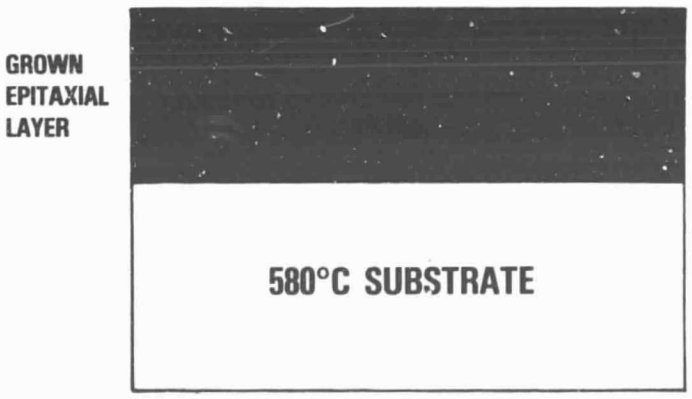
ALE PROCESS (CON'T)

5. ALLOW ALL EXCEPT ONE MONOLAYER OF SULFUR TO SUBLIME



ALE PROCESS (CON'T)

6. REPEAT ABOVE SEQUENCE AT 4 CYCLES/SECOND



REFINED ALE

- ZINC INTRODUCED AS ZnCl
- SULFUR INTRODUCED AS H_2S
- HCl FORMED IN SUBLIMATION PERIODS AND PUMPED OUT

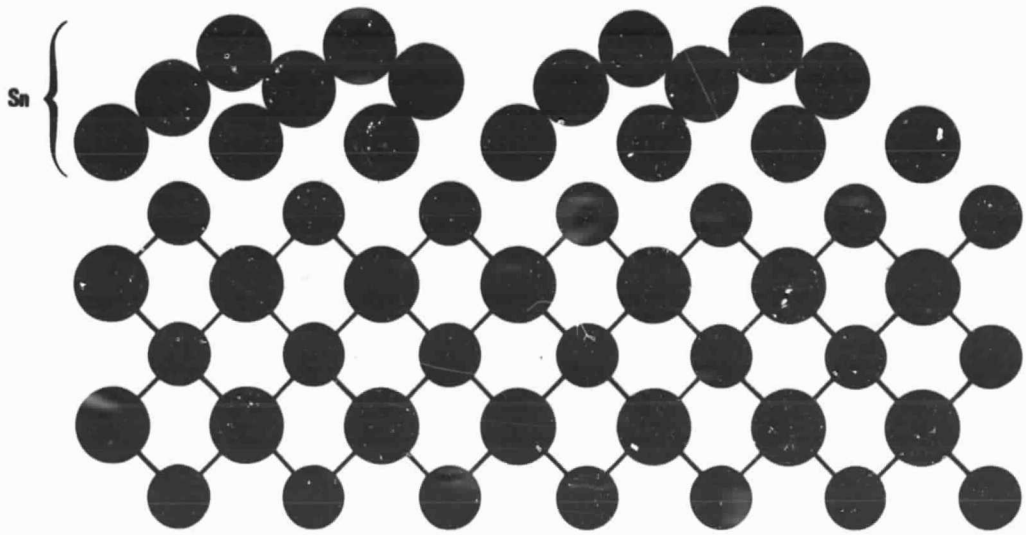
III–V DEFECT MODEL

- IMPURITY ATOM INCORPORATES INTO GROWING SURFACE ONLY WHEN STOICHIOMETRIC CONTROL IS POOR AND HOST CRYSTAL REACTANT ION SURFACE MOBILITY IS LOW RELATIVE TO GROWTH RATE.
- DIFFUSIVITY OF IMPURITIES IN CRYSTAL IS FREQUENTLY LARGER THAN THAT OF HOST CRYSTAL IONS.

  COROLLARY:

  IMPURITIES CAN BE RAPIDLY "GETTERED" TO UNDERLYING VACANCIES AND ANTISITE LOCATIONS; THEIR SUBSTITUTION THERE REPRESENTS A LOWER LOCAL ENERGY STATE.

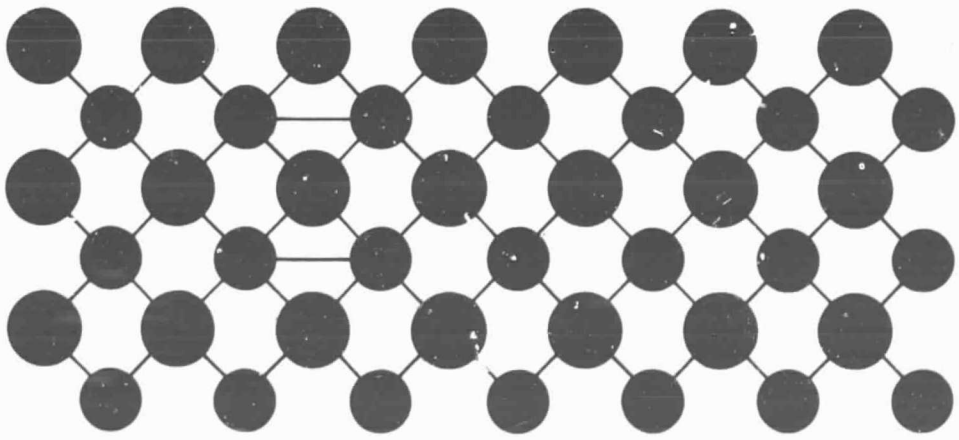
COMPOUND SEMICONDUCTOR DEFECTS



Sn INCORPORATION IN MBE – GROWN Ga As

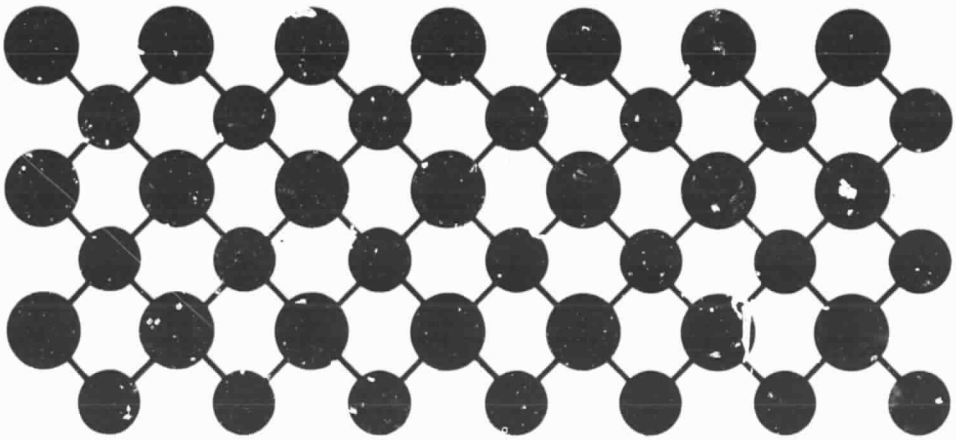
COMPOUND SEMICONDUCTOR DEFECTS

VACANCIES LEADING TO IMPURITY GETTERING CENTERS



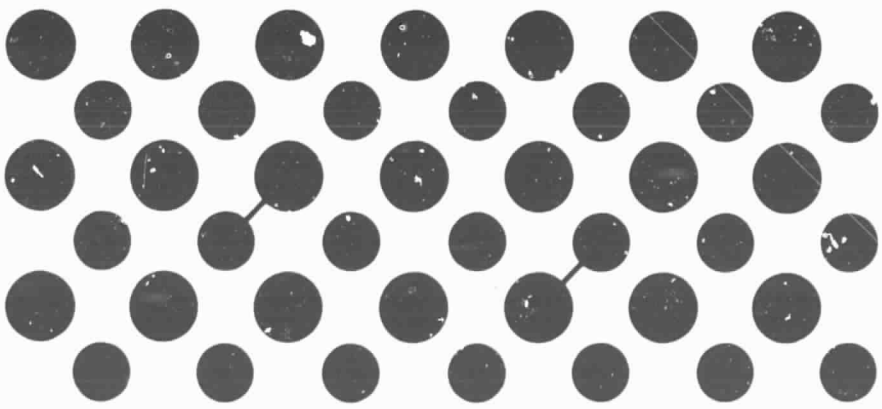
COMPOUND SEMICONDUCTOR DEFECTS

UNBROKEN DIMER BONDS LEADING TO
(1) ANTISITE DEFECTS
(2) IMPURITY GETTERING CENTERS

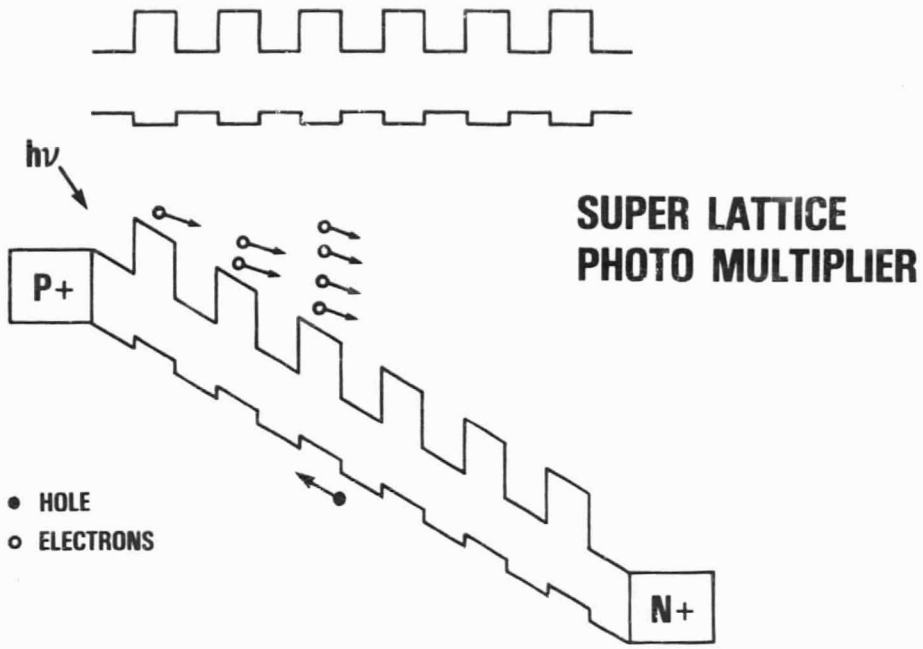


RELIABILITY SOLUTION?

IMPURITY COMPLEXES TOO LARGE TO DIFFUSE



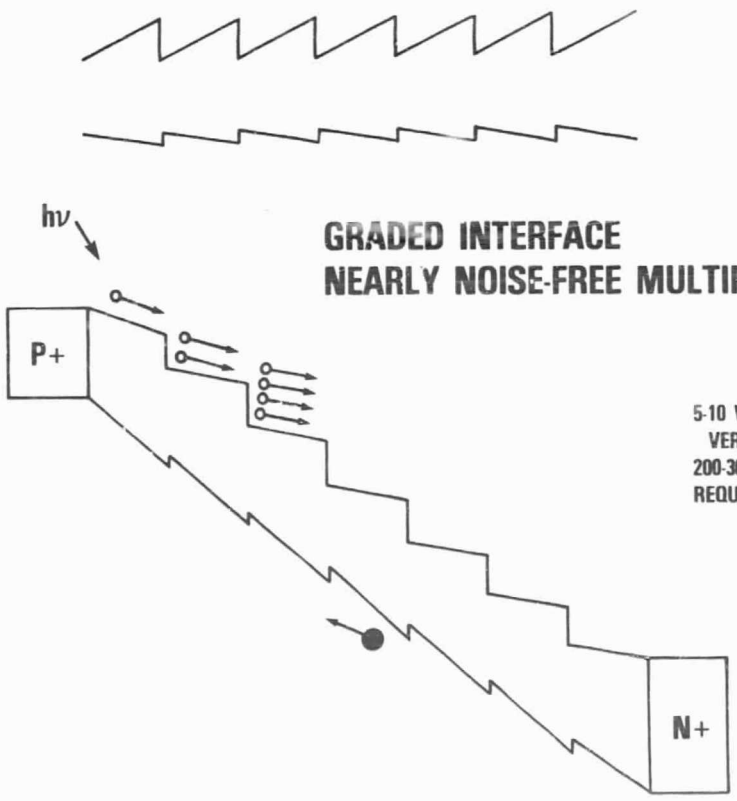
DOUBLE-WHAMMY; III-V ADVANTAGE?



SUPER LATTICE PHOTO MULTIPLIER

LESS NOISE SINCE *ONLY* ELECTRONS IONIZE

NOISE ACCRUES FROM THOSE ELECTRONS IN EACH STAGE THAT DO *NOT* IONIZE



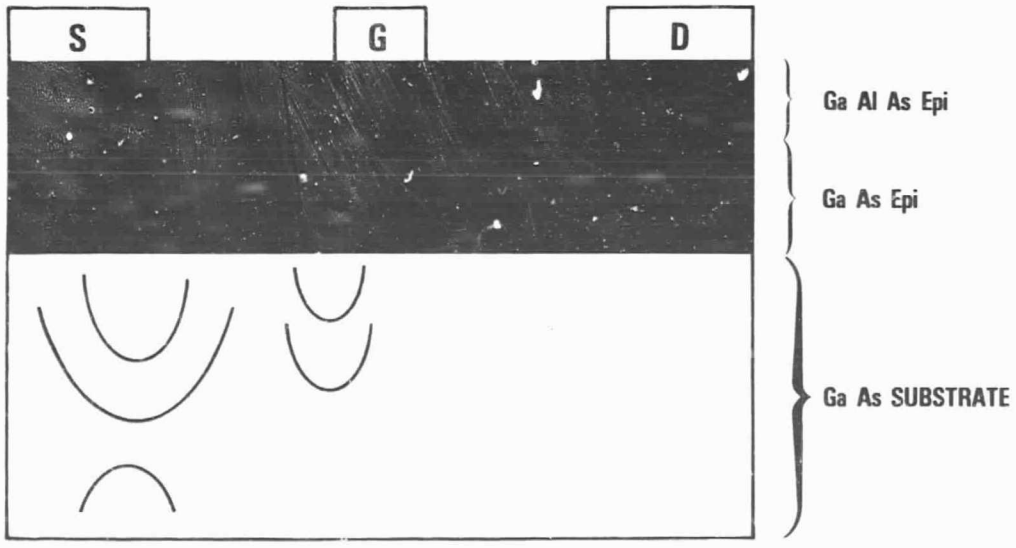
GRADED INTERFACE NEARLY NOISE-FREE MULTIPLICATION

RELIABILITY

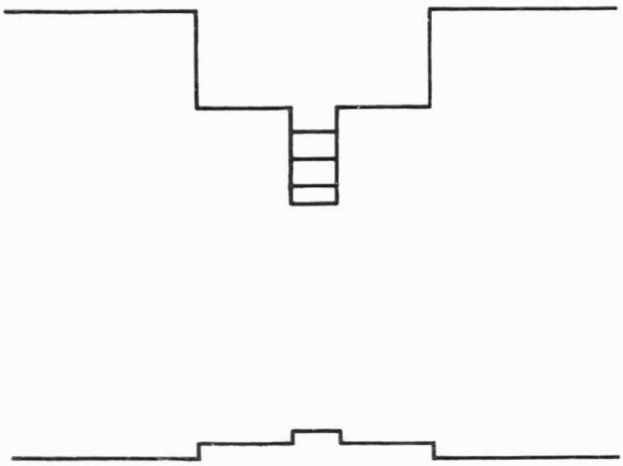
- HEMT, 2DEG, QUANTUM WELL, SUPERLATTICES, AND RELATED STRUCTURES HAVE LAYERS $\sim$ 200 Å THICK.
- AT T $<$ 100 C°, IMPURITIES CAN DIFFUSE $<$ 10,000 HOURS!
- 1 μm HIGH SPEED Si A/D CONVERTERS EXPERIENCING $<$ 4000 HRS LIFE IN FIELD

HEMT 2DEGT SDHT

PROBLEMS: $R_{S\text{-}G}$, 77°K, RELIABILITY

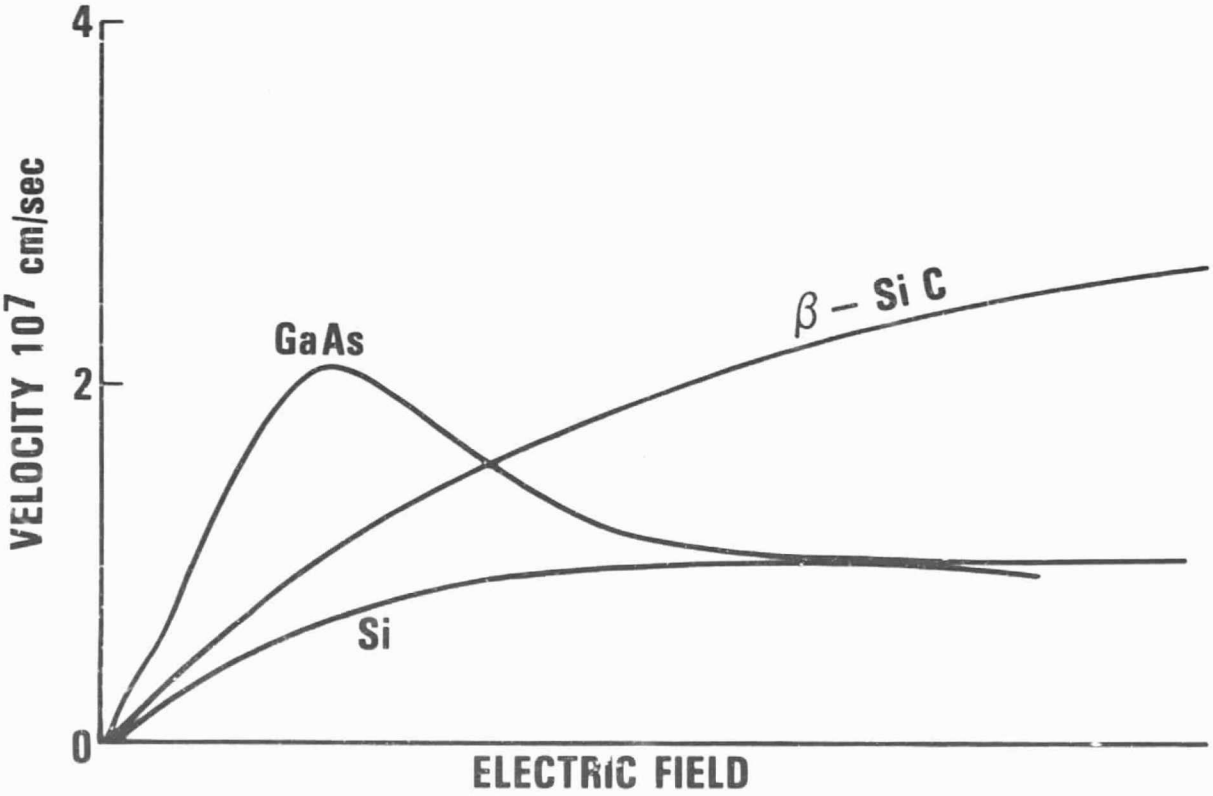


MULTILEVEL QUANTUM WELL DEVICES



5 A/CM^2 TYPICAL THRESHOLD CURRENT

- LOW DISSIPATION
- LONG LIFE?



PHYSICAL ELECTRONICS OF COOLED OPERATION OF VERY SHORT COMPOUND SEMICONDUCTOR TRANSISTORS

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Very high performance is being developed in compound semiconductor transistors. High frequency and low noise figure operation in the GaAs FET have already been established. Substantially more performance increases are expected. This presentation covers a comparison of compound semiconductor materials, and their alloys, the physical concepts of high average electron velocity, and the special benefits of modulation doped heterojunction FET devices.

Table 1 shows the properties of key compound semiconductors. Not shown are the highest reproducible 77°K mobility values for pure epitaxial material. These are about 150,000 $cm^2/V\text{-}s$, 70,000 $cm^2/V\text{-}s$, and 90,000 $cm^2/V\text{-}s$ respectively for GaAs, $In_{0.53}Ga_{0.47}As$, and InP. The lower value for the $In_{0.53}Ga_{0.47}As$ is due to alloy scattering in this material, made more severe by lowering the temperature.

In order to make abrupt heterojunctions with precise doping profiles, molecular beam epitaxy (MBE) is used. Figure 1 shows a cross sectional drawing of such a machine. It has a large vacuum chamber, with various attachments for analysis of the semiconductor surface and the residual

gases. It has several sources for thermally evaporated chemicals to make up the semiconductor and dope it. Growth rates are near one atomic layer per second. Mechanical shutters allow interruption of growth in less than one second, allowing atomic abruptness in composition.

Table 2 is a list of properties obtainable in MBE research efforts to date, including the selectively doped (or modulation doped) heterojunctions. Organometallic vapor phase epitaxy (OMVPE) is also being developed for ultimate use in production of compound semiconductors, their alloys and heterojunctions. Results to date with OMVPE are given in Table 3.

In order to get higher frequency response in FET devices the g_m/C ratio must be improved. This ratio is proportional to the average electron transit velocity through the drift region that has an elevated electric field. Table 4 gives a list of electron velocity values, for several conditions in GaAs.

When pure GaAs is cooled to 77°K, even long devices have high velocity, as shown in Figure 2. An average electron velocity of 2.4×10^7 cm/s or more is possible in GaAs FET's, at 77°K, with pure material. This compares with the 1.2×10^7 cm/s at 300°K with a GaAs channel doped at $1 \times 10^{17}/cm^3$, common in FET's.

Modulation doped structures are shown schematically in Figure 3 with their potential profiles with +.8V gate bias (top) and +.3V gate bias (bottom). The electrons are in

pure GaAs, thus they have higher velocity as shown in Figure 2. The electrons are separated from the donor ions by the potential barrier at the heterojunction. The 100 Å spacer layer keeps the electrons beyond the coulomb scattering sphere of these ions.

Figure 4 shows the current in a modulation doped channel as a function of electric field. The temperature is a parameter. These data were taken at U. of Illinois by Prof. H. Morkoc. Most of the electron velocity increase with temperature has been accomplished by cooling to 77°K. The dashed line represents the current expected in GaAs doped at $1 \times 10^{17}/cm^3$, for the same electron sheet density.

Figure 5 shows the collision-less group velocity vs electron energy in the [100] crystal direction in GaAs. A value near 10^8 cm/s is the upper limit. Electrons at 0.34 eV can scatter into the upper valleys in the [111] direction.

Experiments were done at Cornell on $N^+N^-N^+$ structures that were progressively made shorter. Figure 6 shows the case for $1 \times 10^{16}/cm^3$ doping and 1.1 μm N^- layer thickness, while Figures 7 and 8 are for $2 \times 10^{15}/cm^3$ doping and 0.40 and 0.24 μm N^- layer thicknesses, respectively. The longer device reflects collision domination and the expected change caused by mobility change. The shorter devices show near ballistic conditions, with very little effect from cooling the sample. Monte Carlo calculations made by Awano et al. at the Japanese N.T.T. laboratory are shown for the case of

the 0.24 μm sample. Their detailed calculations agree with our analysis that yields an average electron velocity value of just over 4 x 10^7 cm/s. The ballistic limit with no collisions would be (9.5 x 10^7 cm/s)/2 or 4.75 x 10^7 cm/s. Figure 9 shows the approximate velocity values obtainable as a function of the high field drift length in GaAs. The high velocity portion applies to lightly doped or pure GaAs. For 1 x $10^{17}/cm^3$, the size scale necessary to change to high velocity is 0.5 or 0.6 times that shown.

Figure 10 shows a very short quantum well version of a modulation doped FET. It will use self-aligned ion implanted ohmic contacts as shown. Since the undoped well, housing the electrons, is pure GaAs, very fast, near-ballistic electron transport will be possible for this device, even at room temperature.

As long as parasitic resistance values are substantially lowered, performance to be expected from low temperature operation of GaAs modulation doped FET's will be excellent, and are presented in Table 5. The gate metal could have a skin depth of less than .1 μm at 15°K and at 25 GHz, so this should be taken into account in the design. Transfer resistance at contacts should be made to be less than 0.1 Ω-mm for this best performance. Thus the most optimistic prediction is that 0.15 db NF at 77°K could be obtained at 12 GHz with short, near ballistic modulation doped FET's.

Table 1

COMPOUND SEMICONDUCTOR ELECTRONIC PROPERTIES

	GaAs	$In_{.53}Ga_{.47}As$	InP
BAND GAP (eV)	1.43	.75	1.33
MOBILITY (300^oK, PURE)($cm^2/V\text{-}s$)	10,000	15,000	6,000
MOBILITY (300^oK, $10^{17}/cm^3$)($cm^2/V\text{-}s$)	5,000	7,500	3,000
DIELECTRIC CONSTANT	13	13.5	12.4
EFFECTIVE MASS	.07	.045	.08
GUNN THRESHOLD (V/cm)	3,500	2,800	10,500
(E_L-E_Γ)(eV)	.31	.55	.60
MEAN FREE PATH (μm)	.10	.125	.040
ELECTRON CONFINEMENT MATERIAL	$Al_xGa_{1-x}As$	$In_{.52}Al_{.48}As$	$In_{.52}Al_{.48}As$ OR InP

Table 2

MOLECULAR BEAM EPITAXY RESEARCH

- SINGLE WAFER GROWN IN 2-4 HRS 2" DIAMETER
- UNDOPED GaAs $77^{o}K$ ELECTRON MOBILITY 75-125,000 $cm^2/V\text{-}s$
- N TYPE DOPING TO $2\text{-}3x10^{18}/cm^3$ (Si IN GaAs)
- P TYPE DOPING TO $3x10^{21}/cm^3$ (Be IN GaAs)
- HETEROJUNCTIONS ABRUPT TO 3-6 Å
- COMPUTER CONTROL FOR ELABORATE COMPOSITION STRUCTURES - QUANTUM WELLS, SUPERLATTICES
- DOPING PROFILES FOR PLANAR DOPED BARRIERS
- EPITAXIAL METAL CRYSTALS ON SEMICONDUCTOR
- NON-ALLOYED OHMIC CONTACTS
- SELECTIVELY DOPED HETEROJUNCTIONS

  AL,GaAs/GaAs - ELECTRON MOBILITY 8000 ($cm^2/V\text{-}s$) AT $300^{o}K$, 200,000 AT $77^{o}K$, AND 2,000,000 AT $4^{o}K$. VELOCITY $1.6\text{-}1.8x10^7$ cm/s AT $300^{o}K$, AND $2.4\text{-}3.0x10^7$ cm/s AT $77^{o}K$.

  IN,ALAs/IN,GaAs - ELECTRON MOBILITY 11,000 $cm^2/V\text{-}s$ AT $300^{o}K$ AND 55,000 $cm^2/V\text{-}s$ AT $77^{o}K$

- COSTS \$.25 - .75 x 10^6

Table 3

ORGANOMETALLIC VAPOR PHASE EPITAXY - PRODUCTION

- SINGLE WAFER 2" DIAMETER TO 20 WAFERS 3" DIAMETER GROWN IN 2-4 HRS.
- UNDOPED GaAs $77^{o}K$ ELECTRON MOBILITY 80-100,000 $cm^2/V\text{-}s$
- N TYPE DOPING TO $2\text{-}3x10^{18}/cm^3$ (SI IN GaAs)
- P TYPE DOPING TO $\sim 10^{19}/cm^3$ (ZN IN GaAs)
- HETEROJUNCTIONS ABRUPT TO 10-20Å.
- COMPUTER CONTROL FOR ELABORATE COMPOSITION PROFILES - QUANTUM WELLS AND SUPERLATTICES
- SELECTIVELY DOPED HETEROSTRUCTURES - PRELIMINARY GaAs AND In,GaAs RESULTS - $77^{o}K$ ELECTRON MOBILITY 40,000 - 80,000 $cm^2/V\text{-}s$
- COSTS $.1 - .3 \times 10^6$

Table 4

FET FREQUENCY RESPONSE

$$F_T \propto G_M/C \propto v_E$$

ELECTRON VELOCITY FOR GaAs

1.2×10^7 cm/s - $N_D \sim 1 \times 10^{17}/cm^3$, $L_E \geq .8\ \mu m$

2.4×10^7 cm/s - 77^oK, pure, $L_E \geq 1\ \mu m$

$\geq 4.0 \times 10^7$ cm/s - 300^oK, Pure, $L_E \leq .4\ \mu m$

(NEAR BALLISTIC, GRADUAL ACCELERATION)

$\geq 8.0 \times 10^7$ cm/s - 300^oK, Low Doping, $L_E \leq .6\ \mu m$

(NEAR BALLISTIC, IMPULSE ACCELERATION/DRIFT)

9.5×10^7 cm/s, [100] DIRECTION $\sim .25$-$.3$ eV

(CRYSTAL LIMITED GROUP VELOCITY)

Table 5

EXPECTED LOW TEMPERATURE PERFORMANCE OF GaAs MODULATION DOPED FET's

.5 μM GATE, SELF ALIGNED BY ETCHING

1.46DB NF 12 GHz 300°K

.34 DB NF 12 GHz 77°K

.5 μM GATE, SELF ALIGNED BY ION IMPLANTING

1.0 DB NF 12 GHz 300°K

.25 DB NF 12 GHz 77°K

.3 μM GATE, SELF ALIGNED BY ETCHING

1.0 DB NF 12 GHz 300°K

.25 DB NF 12 GHz 77°K

.3 μM GATE, SELF ALIGNED BY ION IMPLANTING

.6 DB NF 12 GHz 300°K

.15 DB NF 12 GHz 77°K

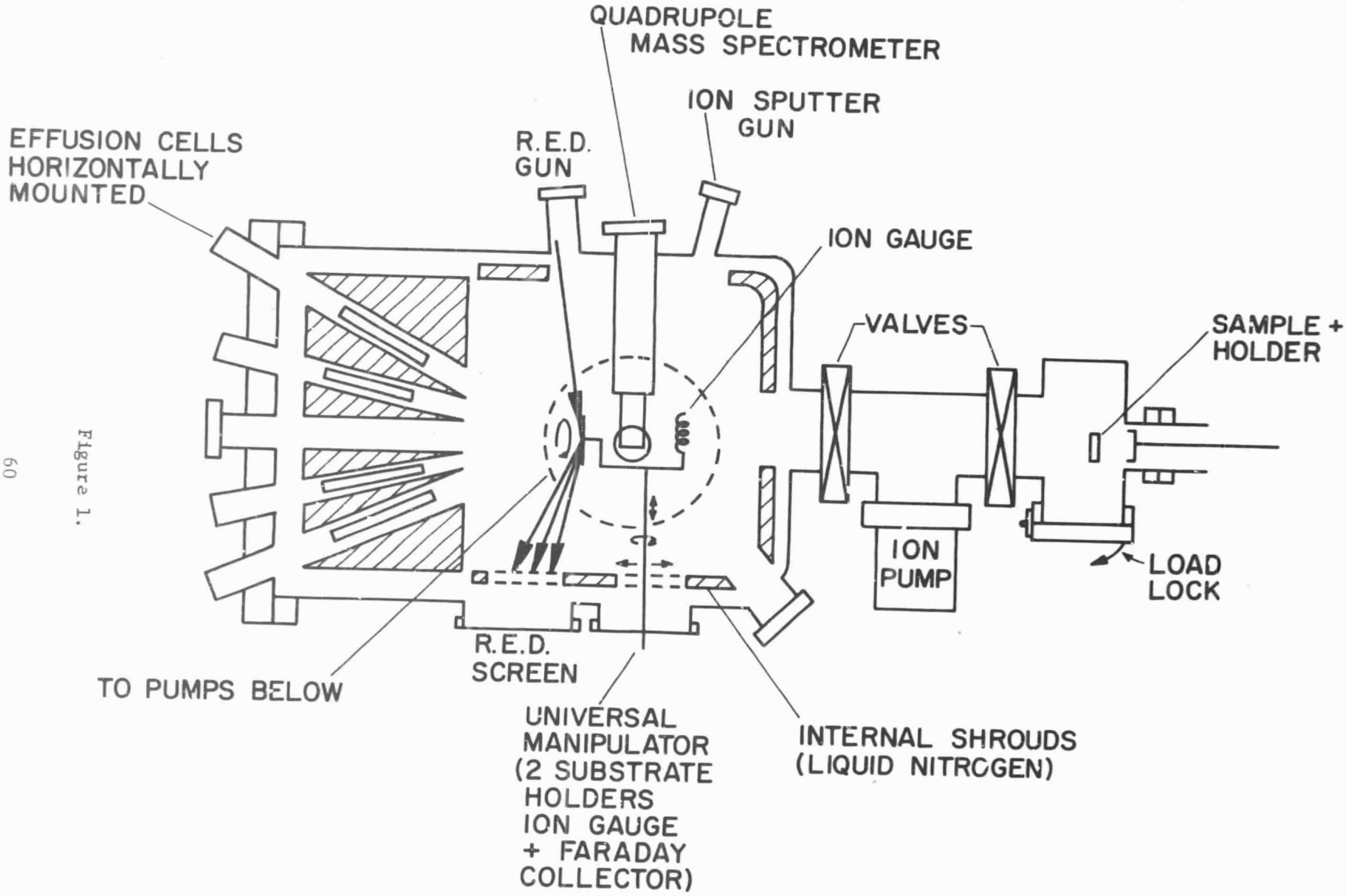
QUADRUPOLE
MASS SPECTROMETER
ION SPUTTER
GUN
EFFUSION CELLS
HORIZONTALLY
MOUNTED
R.E.D.
GUN
ION GAUGE
VALVES
SAMPLE +
HOLDER
ION
PUMP
LOAD
LOCK
R.E.D.
SCREEN
TO PUMPS BELOW
UNIVERSAL
MANIPULATOR
(2 SUBSTRATE
HOLDERS
ION GAUGE
+ FARADAY
COLLECTOR)
INTERNAL SHROUDS
(LIQUID NITROGEN)

Figure 1.

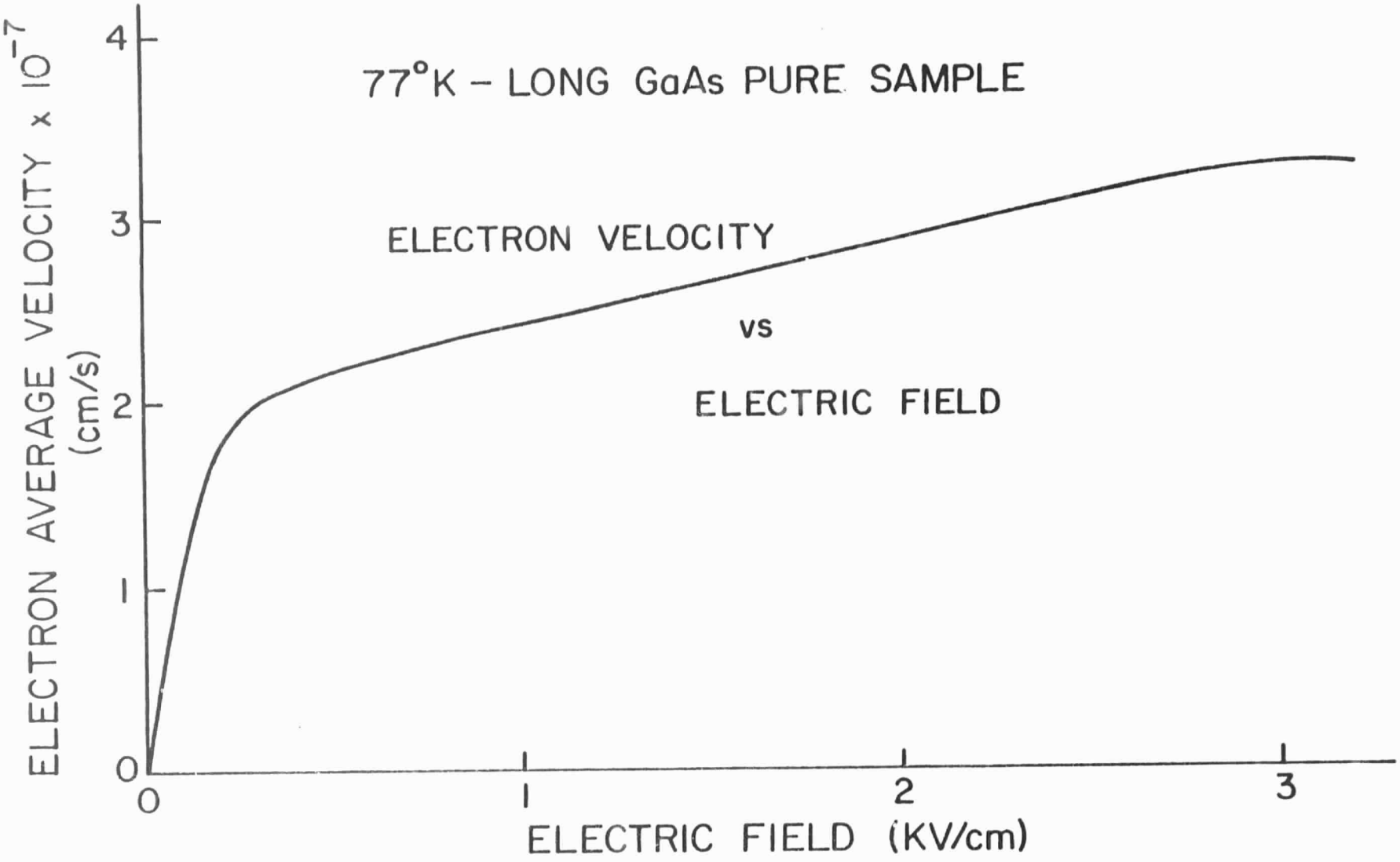
77°K – LONG GaAs PURE SAMPLE
ELECTRON VELOCITY
vs
ELECTRIC FIELD
ELECTRON AVERAGE VELOCITY x 10^{-7} (cm/s)
ELECTRIC FIELD (KV/cm)
0
1
2
3
4
0
1
2
3

Figure 2.

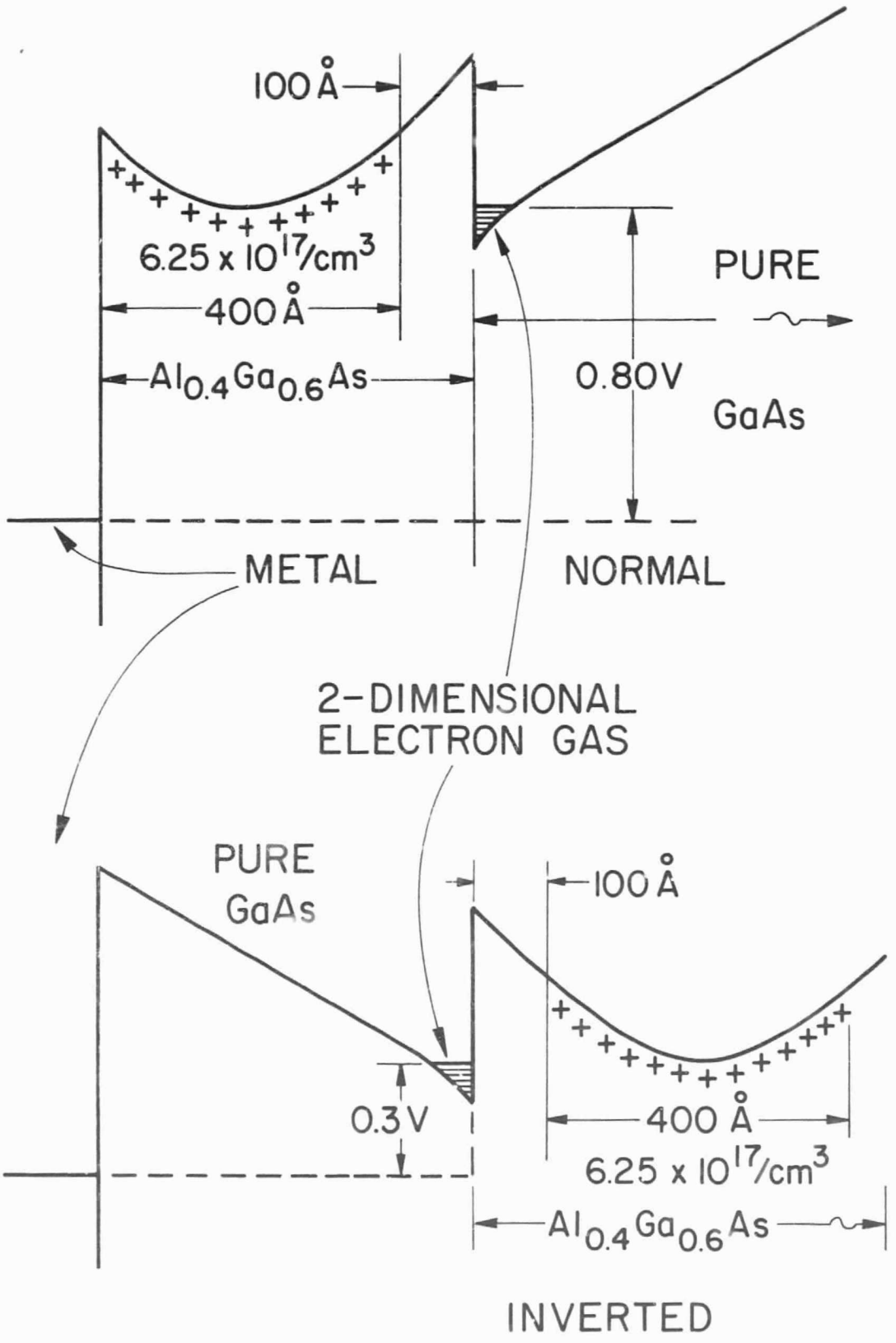
100 Å
6.25 x 10^17/cm^3
400 Å
Al0.4Ga0.6As
PURE
0.80V
GaAs
METAL
NORMAL
2-DIMENSIONAL
ELECTRON GAS
PURE
GaAs
100 Å
0.3V
400 Å
6.25 x 10^17/cm^3
Al0.4Ga0.6As
INVERTED

Figure 3.

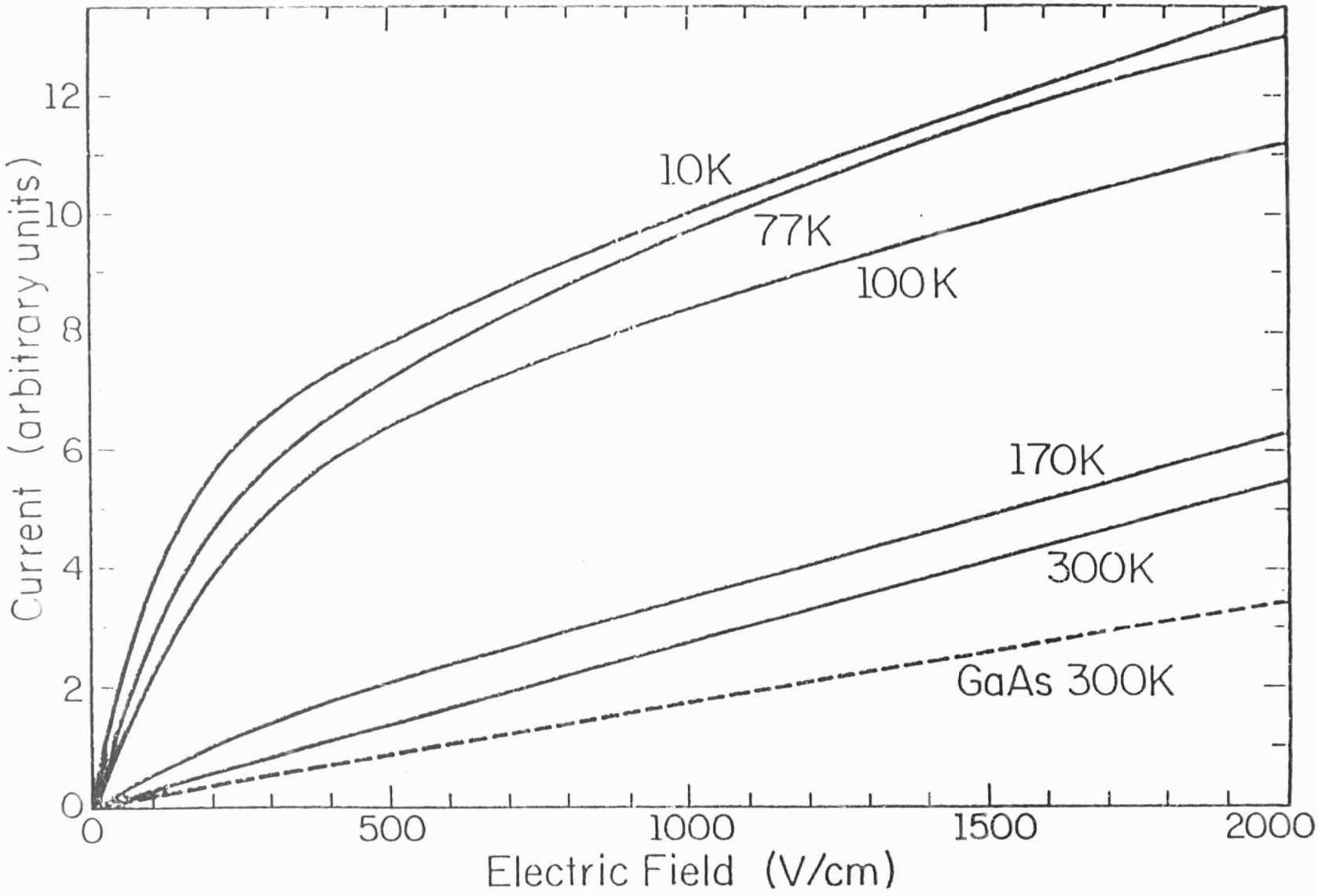
Current (arbitrary units)
0
2
4
6
8
10
12
0
500
1000
1500
2000
Electric Field (V/cm)
10K
77K
100K
170K
300K
GaAs 300K

Figure 4.

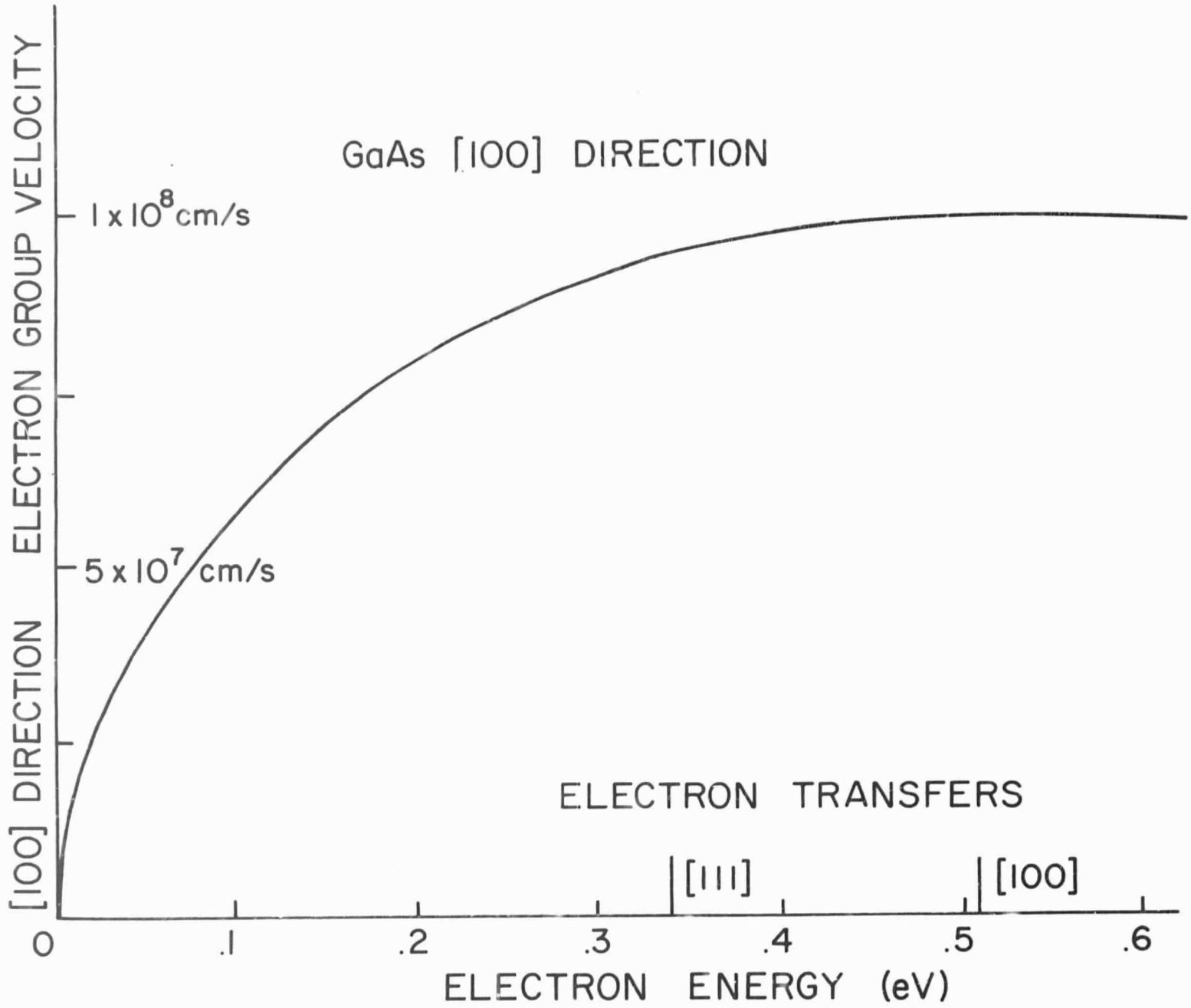
GaAs [100] DIRECTION
[100] DIRECTION ELECTRON GROUP VELOCITY
1 x 10^8 cm/s
5 x 10^7 cm/s
ELECTRON TRANSFERS
[111]
[100]
0
.1
.2
.3
.4
.5
.6
ELECTRON ENERGY (eV)

Figure 5.

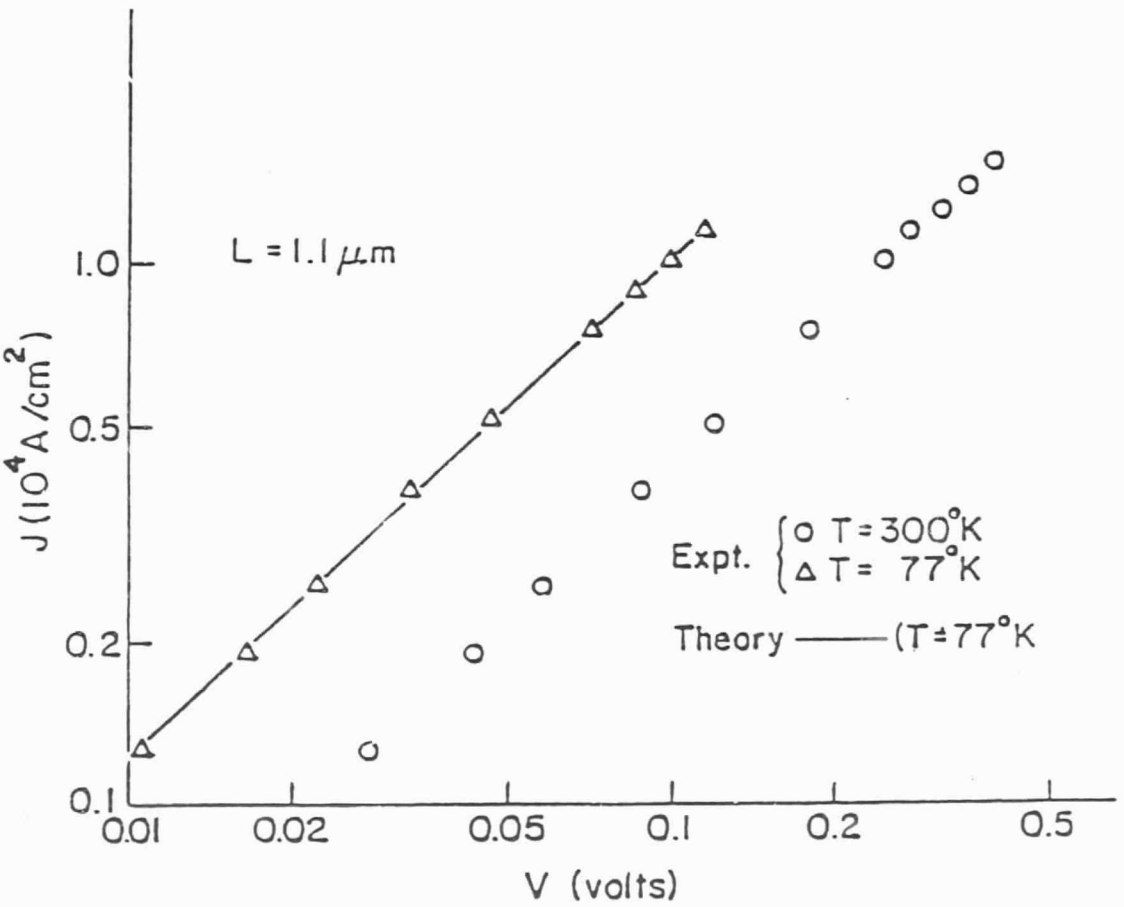
L = 1.1 μm
J (10^4 A/cm^2)
1.0
0.5
0.2
0.1
0.01
0.02
0.05
0.1
0.2
0.5
V (volts)
Expt. { o T = 300°K
Δ T = 77°K
Theory —— (T = 77°K

Figure 6.

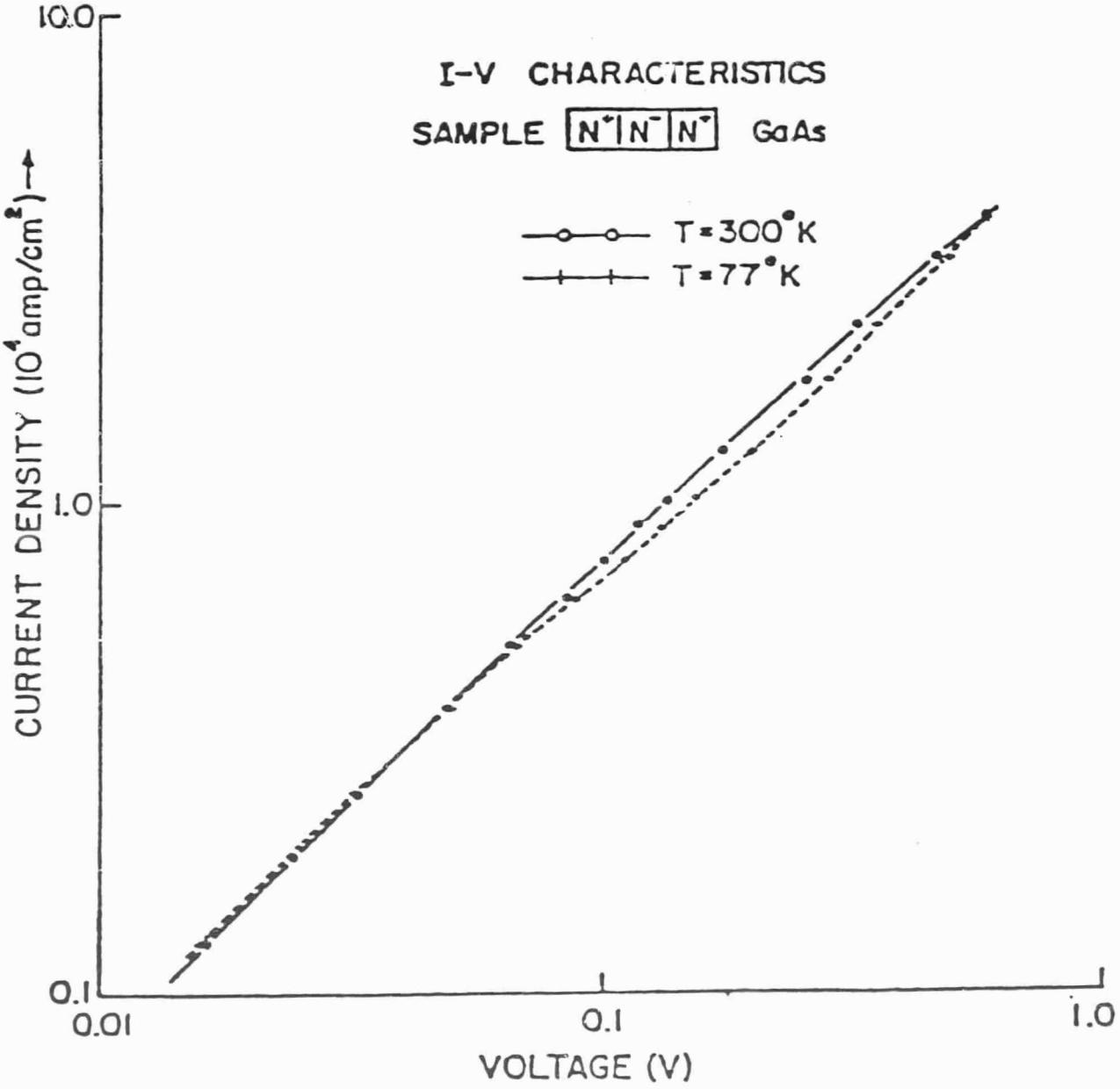
I-V CHARACTERISTICS
SAMPLE N⁺ N⁻ N⁺ GaAs
T=300°K
T=77°K
CURRENT DENSITY (10⁻⁴amp/cm²)
10.0
1.0
0.1
0.01
0.1
1.0
VOLTAGE (V)

Figure 7.

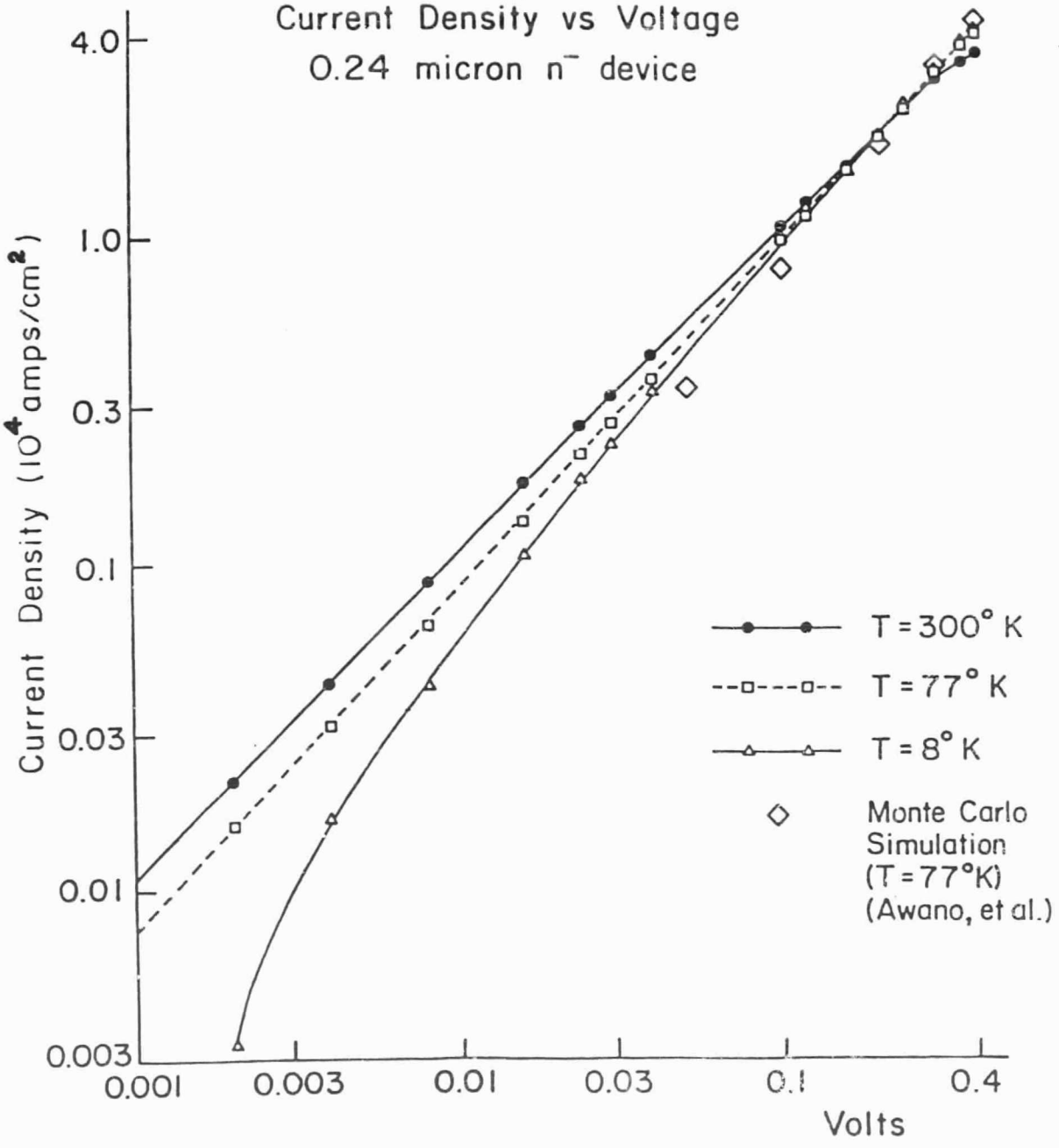
Current Density vs Voltage
0.24 micron n⁻ device
Current Density (10^4 amps/cm^2)
4.0
1.0
0.3
0.1
0.03
0.01
0.003
0.001
0.003
0.01
0.03
0.1
0.4
Volts
T = 300° K
T = 77° K
T = 8° K
Monte Carlo Simulation (T = 77°K) (Awano, et al.)

Figure 8.

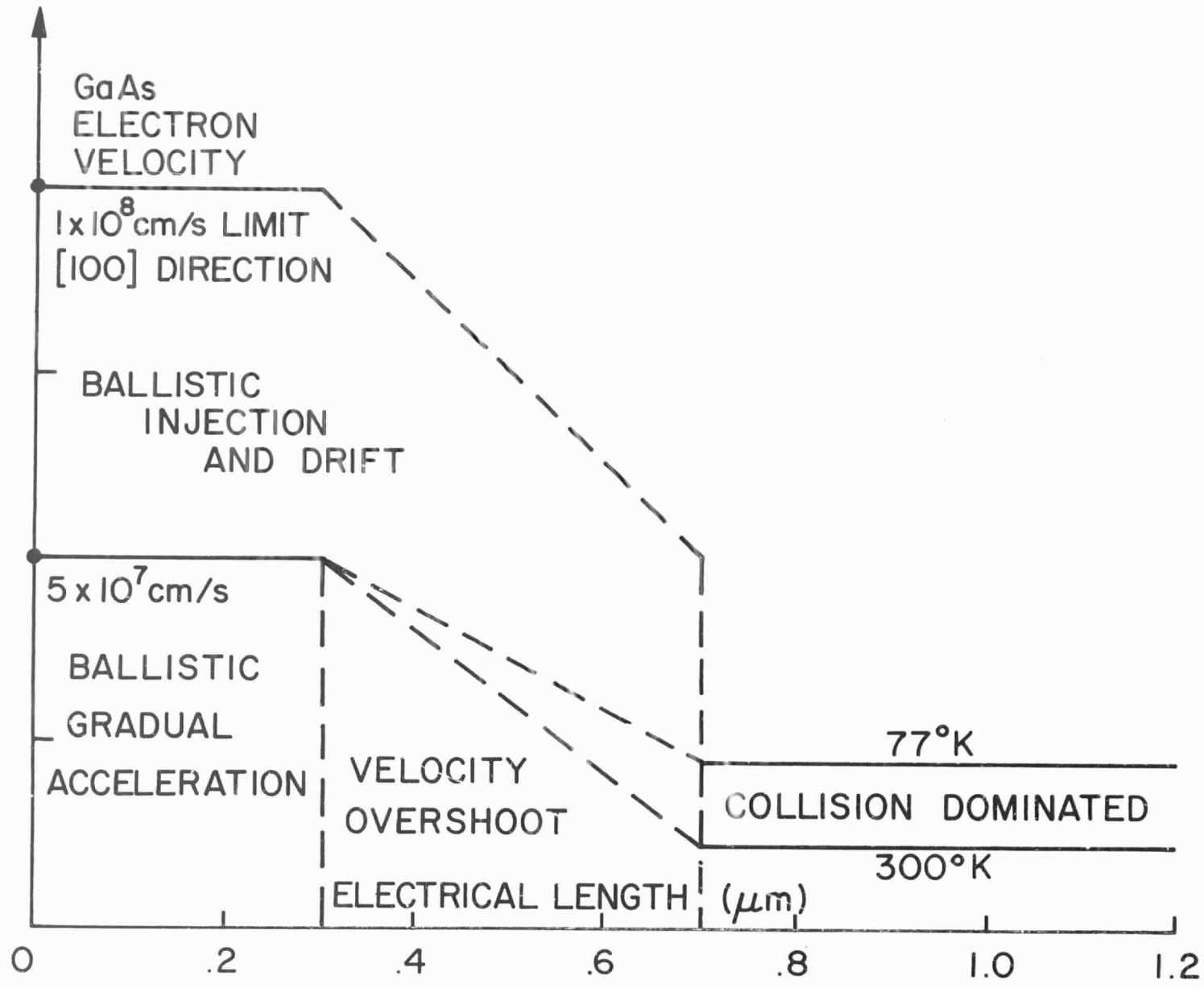
GaAs
ELECTRON
VELOCITY
1x10^8cm/s LIMIT
[100] DIRECTION
BALLISTIC
INJECTION
AND DRIFT
5x10^7cm/s
BALLISTIC
GRADUAL
ACCELERATION
VELOCITY
OVERSHOOT
77°K
COLLISION DOMINATED
300°K
ELECTRICAL LENGTH (μm)
0
.2
.4
.6
.8
1.0
1.2

Figure 9.

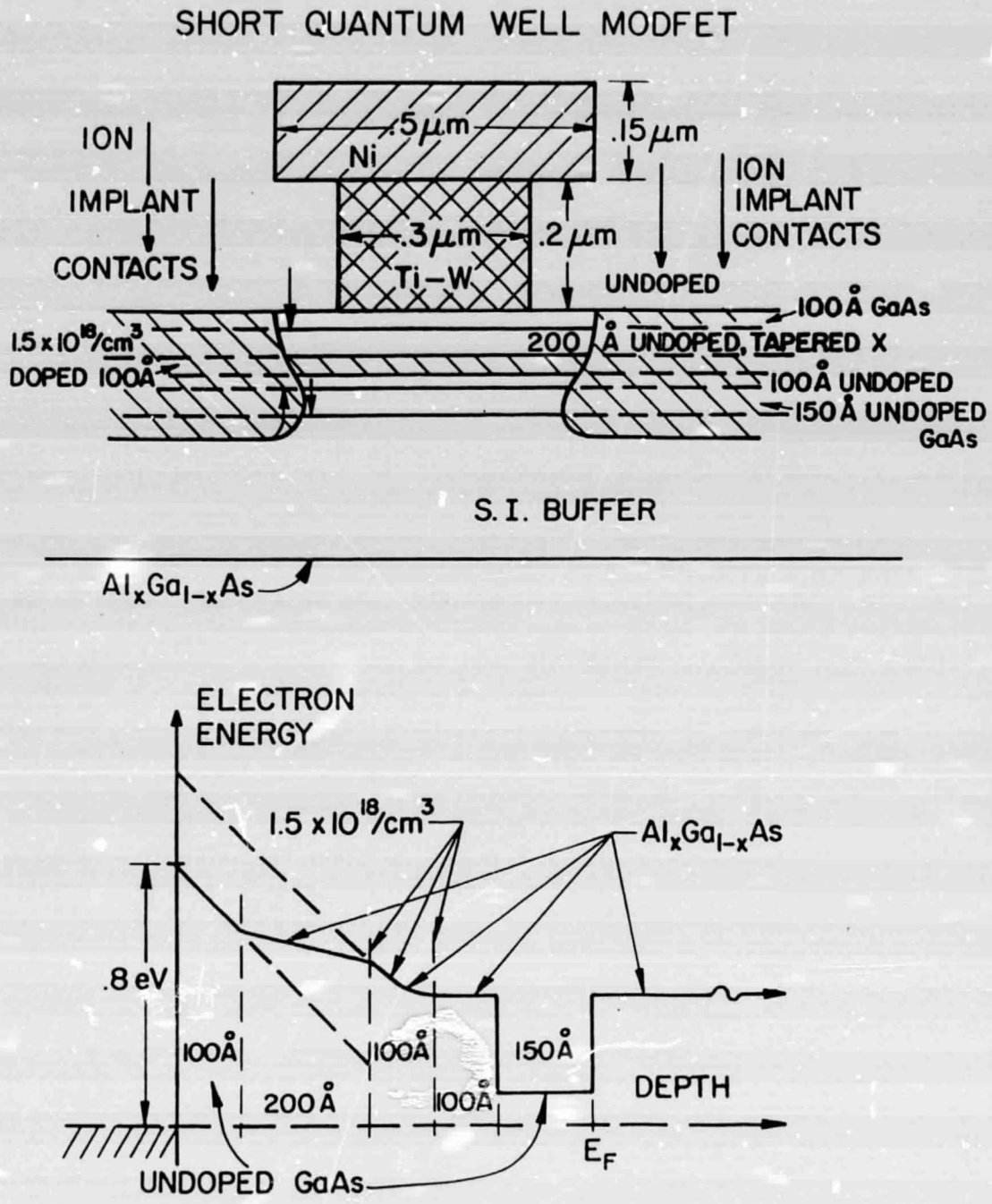
SHORT QUANTUM WELL MODFET
ION
IMPLANT
CONTACTS
.5μm
Ni
.15μm
.3μm
Ti–W
.2μm
ION
IMPLANT
CONTACTS
UNDOPED
100Å GaAs
200 Å UNDOPED, TAPERED X
100Å UNDOPED
150Å UNDOPED
GaAs
1.5 x 10^18/cm^3
DOPED 100Å
S.I. BUFFER
AlxGa1-xAs
ELECTRON
ENERGY
1.5 x 10^18/cm^3
AlxGa1-xAs
.8 eV
100Å
100Å
150Å
200Å
100Å
DEPTH
EF
UNDOPED GaAs

Figure 10.

The Effects of Cooling on Delay-Time Limits in IC's

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We consider the effect of cooling as a fundamental limit to delay-times in IC's. Generally, it appears that the delay time should be decreased at cryogenic temperatures.

There is a fundamental limit to the delay time of an IC which arises from the necessity for heat removal, the necessary requirements for signal propagation, as well as the speed-power product of the gate. At the fundamental limit, the delay time is insensitive to modest variations in the actual speed-power product. At the opposite extreme, in the wire-dominated chip, the cell size is determined by wiring constraints rather than device constraints and the delay time is also independent of the speed-power product. Here we consider how cooling an IC technology may affect this delay-time limit.

Power-Delay Products

Integrated circuit technologies are often compared to each other through the speed-power product of a single gate, typically an inverter. Such comparisons rely upon the fact that, when properly defined and measured, the speed-power product can be equated with the minimum energy needed to perform a logic operation [1]. Although measured power-delay products are determined by technological considerations, Bate [2] has argued that there are fundamental limits to how small the energy dissipation (and therefore the speed-power product) can be made. He considered the switching of a group of particles between two collisionally broadened, quantum mechanical energy levels and found that the minimum energy cannot be reduced below 10^{-19} Joule for an error probability of 10^{-30}. On the other hand, computer simulations of Josephson junction logic elements have yielded power-delay products of 10^{-18} joule [3]. While the model of Bate is abstract, it is hard to see how the additional complexities present in real inverter circuits would either increase the speed or decrease the power dissipation. Indeed, the limit is conservative in many respects.

The power-delay product discussed above would actually be associated with an inverter circuit composed of the bare devices themselves. However, a practical integrated circuit also has lines or wires associated with each gate. These lines have a power-delay product associated with them and generally dominate the actual energy dissipation in the logic gate [4,5]. This extreme arises when the necessity for wiring dominates the cell size and the device is no longer critical for setting energy dissipation. This latter case is referred to as the wire-dominated chip [5]. We return to this latter case below.

There are other constraints that must also be placed on the power dissipation and the delay time in an integrated circuit. To illustrate these, we consider a square array of N logic cells of area A each. If we can remove Q Watts of heat per unit area, we must require that the dissipated power of P satisfies

$$P < QA \quad . \tag{1}$$

Note that this condition only ensures that a steady-state temperature exists, not that it is low. Thus, this is a "worst case" limit. A second limit that must be invoked is that, in the worst case, a signal must be able to propagate across the entire chip in the delay time t_d. This signal propagation requirement is expressed as

$$(NA)^{\frac{1}{2}} \leq ct_d \quad , \tag{2}$$

where c is the speed of propagation and is typically lower than the speed of light due to the dielectric properties of the semiconductor chip.

From the above discussion, we can now define a fundamental limit on the delay time itself [6]. The argument is similar to one proposed earlier by Keyes [7], but differs in that a firm limit on t_d is set. Equations (1)

and (2) imply a range of areas that must satisfy the joint inequalities

$$P/Q < A < c^2 t_d^2/N \quad . \tag{3}$$

However, there is another constraint set by the energy dissipation, or $Pt_d = E_m$. Using this quantity in (3) leads to the final limit

$$NE_m/Qc^2 < t_d^3 \quad . \tag{4}$$

We illustrate the situation in figure 1. The combination of a power-delay product, E_m, and the heat removal or cooling rate Q demands a minimum area for a given delay time. The necessity of signal propagation sets a maximum on the area for a given delay time. It is interesting to note that the degree of integration represented by N and the heat removal rate Q are as important as the power-delay product of the individual cells in determining how fast the overall chip can be operated. In particular, we note that it requires a three order-of-magnitude reduction in E_m to reduce the minimum t_d by a single order-of-magnitude. Increasing the integration level actually tends to worsen the minimum delay time that can be achieved, although this minimum is well below the levels discussed in today's technology.

The Wire-Dominated Chip

In some applications, such as gate array chips, the chip itself is dominated by the interconnection wiring and is referred to as a wire-dominated chip [5]. In these chips, the cell size is determined not by the devices but by the number of wires that must run through the cell itself. When this limit occurs, further reductions in the active area of the devices themselves will not significantly increase the number of logic cells per unit area of chip. In these situations, the actual power-delay product of the device itself is not as important as constraints of charging

the interconnection capacitances of the wiring. Keyes [5] has argued that the power-delay product of such a wire-dominated chip is

$$Pt_d = C_w f K^2 w V_B V_S / M \quad , \tag{5}$$

where P is the power dissipation, t_d is the delay time, M is the number of metallization or wire layers in the chip, K is the number of wire channels occupied by wires with capacitance C_w per unit length of wire. Here, V_B and V_S are the supply and signal voltages, respectively. The form of (5) is easily understood, as the right-hand side is just the energy stored in the capacitance of the wires, if the average length of a wire is K/M and the average number of wires per cell is w.f.k.

Since the cell area is dominated by the interconnection wiring, the cell size itself is approximately given by

$$A = (Kw/M)^2 \quad . \tag{6}$$

The ability to dissipate the heat generated by the input power P must also be included in the discussion. This can be done through the incorporation of (1) and (5). The other fundamental limit is that a signal must be able to propagate across the entire chip in the delay time t_d, as discussed above. This leads to (2). Thus, for a chip containing N square cells, this signal propagation limit is expressed by combining (1), (2), (5), and (6) as

$$t_d^2 > N^{\frac{1}{2}} f K C_w V_B V_S / Qc \quad . \tag{7}$$

As above, this constraint is essentially independent of geometrical factors such as w, although these latter factors do affect C_w slightly. Using (7), a lower limit to the delay time can also be obtained by taking the appropriately most favorable limits on the individual parameters. Heller _et al_. [8] have shown that a value of K=20 is typical for a system of 1000 gates. Master slices with this number of gates have been reported [9] and do

approach the wire-dominated limit. Heat dissipation rates of Q = 20 W/cm^2 are appropriate for a freon cooled computer. The question of line capacitance is more arguable, but for future small chips, the fringing and interline capacitance will probably limit the lower value of C_w to 0.1 fF/micron [10]. Using these values and setting c to the speed of light, a lower limit of about 0.2 nanoseconds is obtained for the delay time.

The significance of this result is obvious. Even if the individual logic gates in a wire-dominated chip are fast, the chip itself cannot have a delay time shorter than 0.2 nanoseconds, corresponding to a clock frequency of about 1.0 GHz. While the constraints used here are appropriate to a master slice chip, the conclusion is expected to be more general and apply to a wide variety of array type logic designs in which each cell must be able to communicate with each other cell or with cache memories at some distance.

The Effects of Cooling

When existing high speed circuits are examined using this approach, delay time limits at the order of 5 ps are obtained [6]. We now consider how cooling would affect these limits. It is interesting to note that cooling may not necessarily improve the delay time. For the device dominated chip, we obtain

$$\frac{1}{t_D}\frac{\partial t_D}{\partial T} = \frac{1}{3}\,\frac{1}{(E_m/Q)}\,\frac{\partial}{\partial T}\left(\frac{E_m}{Q}\right) \tag{8}$$

and for the wire dominated chip

$$\frac{1}{t_D}\frac{\partial t_D}{\partial T} = \frac{1}{2}\,\frac{1}{\left(\frac{C_w V_B V_S}{Q}\right)}\,\frac{\partial}{\partial T}\left(\frac{C_w V_B V_S}{Q}\right) \tag{9}$$

Here we have assumed that the signal propagation velocity is insensitive

to temperature. Cooling will decrease the delay time therefore if

$$\frac{1}{Q}\frac{\partial Q}{\partial T} < \frac{1}{E_m}\frac{\partial E_m}{\partial T} \tag{10}$$

for the device dominated chip, and if

$$\frac{1}{Q}\frac{\partial Q}{\partial T} < \frac{1}{(C_w V_B V_S)}\frac{\partial (C_s V_B V_S)}{\partial T} \tag{11}$$

for the wire dominated chip. Physically, we have assumed that temperature appears mainly in the adjusting the minimum area limit, a point which we return to later. Equations (10) and (11) are conditions which ensure that the minimum area limit moves to the left in figure 1 as T decreases.

Bate [2] has considered the effects of cryogenic operation on the ultimate limiting power-delay product. He redefined this product in terms of the overall system energy, E_{syst}, which is

$$E_{syst} = E_m + E_{cool} \tag{12}$$

where E_{cool} is the energy loss associated with the cooling system removing E_m. By applying the Carnot theorem

$$E_{cool} = \frac{E_m}{\omega} \tag{13}$$

where

$$\omega = \frac{T}{T_A - T} \tag{14}$$

and T_A is the ambient temperature, he obtained

$$E_{sys} = E_m \left(1 + \frac{1}{\omega}\right) = E_m \frac{T_A}{T} \quad , \tag{15}$$

Bate noted that his quantum mechanical limits revealed no fundamental advantages for cooling and that the above argument implies potential energy penalties for cold electronics. Indeed the system power delay product is always greater than E_m. However, there are practical reasons for operation

at cryogenic temperature, which we consider here.

While there are many factors which affect Q, the one universal factor is the thermal conductivity of the material used in the active devices. The thermal conductivity of several common semiconductors is shown in Table I. Generally, there is an order of magnitude or more increase in the thermal conductivity as the samples are cooled to temperatures in the 20 to 100°K range. For temperatures of 20K or less, the thermal conductivities decrease with decreasing temperatures and have returned to their 300°K values at temperatures of several degrees. The thermal conductivity of GaInAs may be misleading for some cooling configurations as this material is generally grown on an InP substrate. Therefore, if the main heat flow path is through the substrate, the thermal conductivity of InP may be a more meaningful measure than that of GaInAs itself. Generally, this "semiconductor" Q should peak at cryogenic temperatures. This increase may be wiped out however by the changes in Q associated with the changes in coolant and refrigeration techniques.

The E_m of an active device is quite commonly viewed as a parameter which should improve with cooling [see e.g. 11]. There are important reasons for this. Carrier mobility generally increases as the material is cooled, until one enters (at temperatures of the order 10 to 100K) the impurity scattering dominated regime [12]. In GaAs, the saturated carrier velocity is enhanced by 20 to 30% (the change in Si is less significant because of differences between polar and nonpolar phonon scattering [10]). In most materials we also will see velocity saturation occur at lower fields. This allows us to use lower bias voltages. The logic swing may also be reduced if it is limited by thermal voltage fluctuations and not by variations in device parameters which result from nonuniformity of the fabrication

processes across the chip. Cooling generally is expected to allow us to use lower bias voltages, smaller logic swings, should reduce parasitic resistances and may enhance any performance advantages associated with GaAs.

For the wire dominated chip, the above discussion shows that both V_B and V_S should be reduced or "reducible" by cooling. The capacitance should be relatively insensitive to cryogenic effects. The dielectric constant of most semiconductors obeys a law of the form

$$\varepsilon_R \ (T) = \varepsilon_R \ (0) \ \left[1 + \alpha T \right] \qquad (16)$$

where $\alpha \sim 10^{-4}$. No significant change in ε_R is expected. A more significant variation would be seen if the coolant actually flows over the top of the chip, where the active devices and metal lines themselves are located. The dielectric constants for several potential coolants are [13]: $N_2 = 1.45$; He = 1.05; and $H_2 = 1.23$. Therefore, if the lines are running over SiO_2 ($\varepsilon_R = 3.9$), some changes in C_w may be obtained. In particular, we would expect more fringing fields and line-to-line crosstalk to be present. The above comments are also applicable to signal propagation velocity and are the reasons why we have generally neglected any possible variation in c with T.

In summary, we have considered the effects of cooling on a fundamental limit on the delay time. Most of the effects should be beneficial, although in principle cryogenic operation could increase delay times.

We thank Dr. W. Porod for useful conversations and Drs. M. Yoder and L. Eastman for a helpful suggestion.

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Table 1

Thermal Conductivities at Room Temperature and 100°K

Units are W/(cm-K)

Material	100°K	300°K
Si	8.0	1.5
GaAs	2.0	0.46
InP		0.68
GaInAs		0.06
SiO_2	0.36	0.15

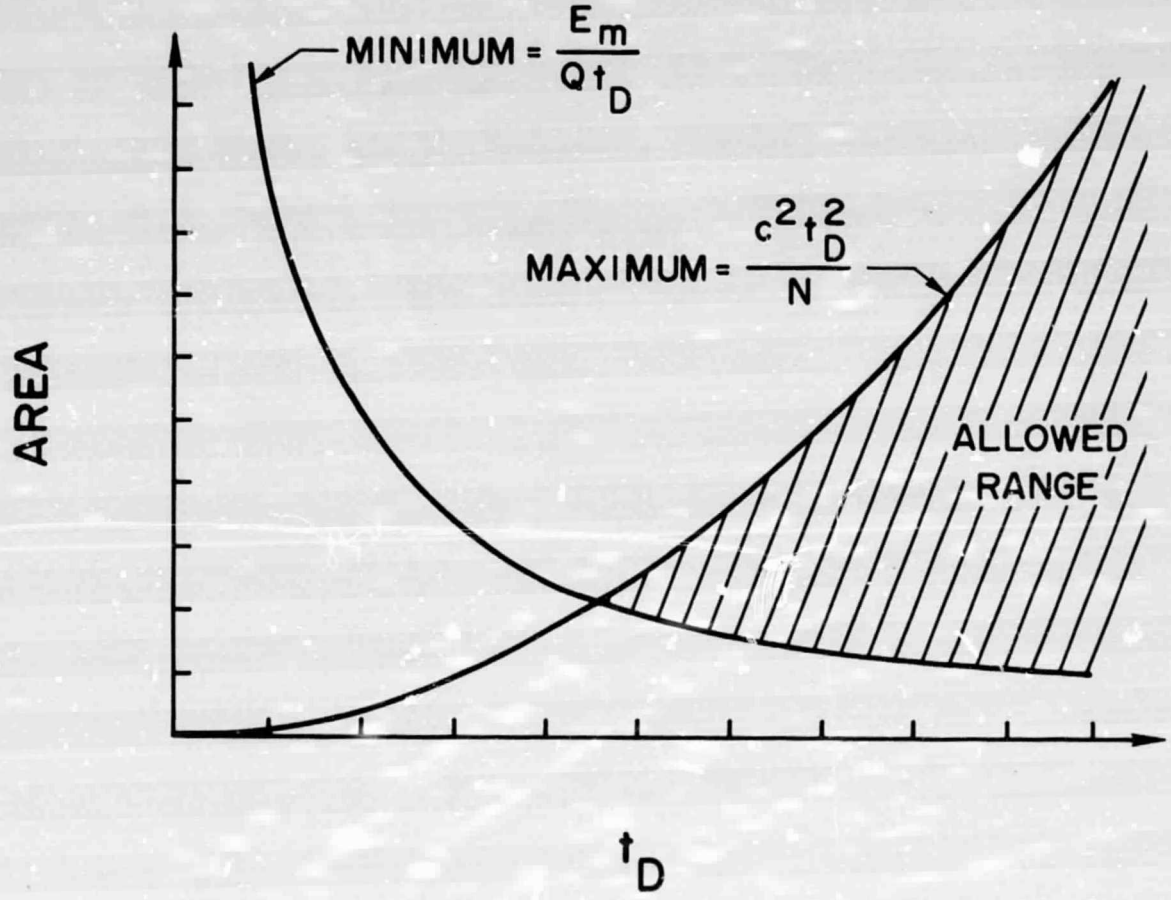

Fig. 1. Maximum and minimum areas for an IC in terms of t_D (arbitrary units).

Si MOS Devices at Low Temperatures

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ABSTRACT

Improvements in various properties of Si MOS devices as a result of operation at low temperatures are discussed. The particular device aspects considered here are subthreshold behavior, effective channel length and delay times. The temperature range is 4.2K to 300K.

I. INTRODUCTION

Low temperature operation of micron and submicron size Si MOSFETs (metal-oxide-semiconductor field-effect-transistors) results in their improved device characteristics. Various low temperature device properties such as increase in mobility, shift in the threshold voltage, increased reliability, etc., have been considered.[1] Here we discuss few other device characteristics such as the subthreshold behavior, delay times and miniaturization at low temperatures. Discussion includes presenting experimental results along with physical models explaining the observed effects.

II. EXPERIMENTAL NOTES

Measurements were done on MOSFETs fabricated on p-type (100) Si substrates with various dopings, ranging from $N_A = 10^{14}$ cm^{-3} to 6×10^{16} cm^{-3}. The fabrication was done using n-channel Si gate technology, and X-ray lithography. The gate oxides were grown in dry atmosphere to different thicknesses, ranging from 130Å to 500Å, and the junction depths varied from 0.25μm to 0.75μm.

The subthreshold behavior and the effective channel length measurements were done using series of eight MOSFETs with the channel length being the only varying parameter between them. The channel width was 80μm, the channel lengths varied from 0.5μm to 6μm in different MOSFETs. These values were the coded channel lengths. The actual channel lengths were usually shorter, and they were estimated from the maximum mobility plots vs. the coded channel lengths for each individual chip.

The ring oscillators employed a chain of 19 inverters which used depletion and enhancement mode MOSFETs as the load and the drive respectively. A total of 15 oscillators from 3 wafers with different fabrication parameters and different geometries were measured. The important parameters for these wafers, are given in Table I.

The measurements at 77K and 4.2K were made by immersing the devices in liquid nitrogen and liquid helium respectively. A RANSCO temperature varying chamber was used to provide temperatures between ~80K to 400K.

III. RESULTS AND DISCUSSIONS

III.1 Subthreshold Behavior

The subthreshold region is of particular importance for low-voltage and low-power applications. In this region the current is dominated by the diffusion component, and its behavior is characterized by a gate voltage swing (S) needed to reduce the current by one decade. The subthreshold swing is given in the following equation[2]

$$S \equiv \ln 10 \frac{dV_{gs}}{dI_d} = \frac{kT}{q} \ln 10 \frac{1 + \frac{C_d}{C_{ox}} + \frac{C_{it}}{C_{ox}}}{1 - \frac{2}{a^2}\left(\frac{C_d}{C_{ox}}\right)^2}, \quad (1)$$

where V_{gs} is the gate voltage, I_d the drain current, k the Boltzmann constant, T the temperature, q the electronic charge, $a \equiv \sqrt{2}(C_{FB}/C_{ox})$, and C_d, C_{ox}, C_{it} and C_{FB} are the capacitances due to the depletion layer, the oxide, the interface traps, and the capacitance at the flat-band voltage respectively.

Figure 1 shows a typical set of experimental traces of the drain current as a function of the gate voltage at three different temperatures. Here we also show the calculated subthreshold currents (dashed lines) using a one dimensional analytical expression for the gate voltage dependence of the drain current.[3] The calculated curves were shifted by 0.2V to account for threshold shifts. These shifts could be due to a combination of the effects of oxide charges, interface traps, as well as the metallic work function, not taken into account in the calculations. To find the temperature dependence of various parameters we first calculated the Fermi level as a function of temperature using the neutrality condition and Boltzmann statistics and then other parameters such as the surface potential and the depletion width. However, the main temperature dependence is through the term T in Eq. 1.

At 300K, log I_d is a linear function of V_{gs} at low currents. This is the subthreshold region which in this sample extends to a current of about 5×10^{-8}A. The increase in I_d becomes more gradual as V_{gs} approaches the threshold voltage ($V_{th} \approx 0.6$V) at the onset of the strong inversion. Both experiment and calculation yield a value of S about 95 mV/decade. At 77K the linear region stops at a current more than one decade lower than at 300K. Here the agreement between the calculated and the measured S is not as good as the room temperature results. The theoretical value of S = 20 mV/decade is calculated by assuming the number of interface traps to be zero, while experimentally S = 24 mV/decade. At 4.2K there is little similarity between the calculations and the experiments, in that the measured log I_d vs. V_{gs} does not even show a linear region. We extended the measurements down to $I_d = 10^{-13}$A, and found that the value of S becomes increasingly smaller. Yet even in the 10^{-12}–10^{-13}A decade the subthreshold swing, S = 6.0 mV/decade, is nearly one order of magnitude larger than the calculated S = 0.83 mV/decade. A number of effects could perhaps explain this discrepancy,[4] however, as far as circuit performance is concerned there seem to be little gain in reducing S by lowering the temperature far below 77K.

Another dramatic change due to cooling is a reduction in the punch-through component of the drain current in the subthreshold region of short channel devices. Devices with some punch-through current (up to $\sim10^{-7}$A at $V_{ds} = 0.1$V) at room temperature turned off to below 10^{-11}A (the measurement accuracy) at 77K. One example of this is shown in Fig. 2. The dash-dot traces show the I_d vs. V_{gs} characteristic of a short channel and a long channel device at room temperature, and the solid curves are the traces at 77K. At 77K the threshold voltage of the long channel device shifted by about 0.25V, and the gate voltage swing reduced as observed earlier. The short channel device with L = 0.3 μm, however, represented a more drastic change. The punch-through current disappeared, and the gate voltage swing became equal to that of the long channel device. The shift in the threshold voltage appeared to be the same as the long channel device. This effect could be an indication that the minimum channel length for the "long channel" behavior changes with decreasing temperature as we will discuss in the next section.

III.2 Minimum Channel Length at 77K

In scaling device parameters the minimum channel length, L_{min}, has been proposed as an empirical relation as[5]

$$L_{min} = A[x_j t_{ox}(w_s+w_d)^2]^{1/3}, \quad (2)$$

where A is a proportionality constant, x_j the junction depth, t_{ox} oxide thickness, w_d and w_s the drain

and source depletion widths for a one-dimensional abrupt junction defined as

$$w_d = \sqrt{\frac{2\epsilon_{Si}}{q}} \sqrt{\frac{V_{ds}+V_{bi}}{N_A}}, \qquad (3)$$

$$w_s = w_d \quad \text{at} \quad V_{ds} = 0$$

where V_{bi} is the built-in voltage of the junction, and ϵ_{Si} the dielectric constant of Si. The constant A was found to be 0.41 at room temperature.[5]

As the temperature decreases w_s and w_d increase, implying a larger L_{min} at 77K, however, the experiments show the opposite effect. Figure 3 shows the relative changes in the drain current for a 100% change in V_{ds} (at $V_{gs} \cong V_{th}$) in eight MOSFETs at 290K and 77K. This figure clearly indicates that the subthreshold current is much less dependent on the changes in V_{ds} at 77K compared with 290K. The substrate doping for this sample is $10^{14}cm^{-3}$, $t_{ox} = 500Å$ and $x_j = 0.75\ \mu m$. This effect is strongest in lower doped channels.

We have chosen the $\frac{\Delta I_d}{I_d} = 10\%$ as the criteria dividing the long channel from the short channel behavior, and have plotted the summary of the results for samples with different parameters in Fig. 4. The solid line represents the room temperature results from Ref. 5, and the dashed line is drawn through the experimental points at 77K.

We recently showed that the parameter which is of importance in comparison of high and low temperature characteristics is the effective channel length L_{eff}, and not L_{min}.[6] In a MOSFET when the surface layer is inverted, the lateral depletion width (see Fig. 5) is given by[7]

$$y_d = \sqrt{\frac{2\epsilon_{Si}}{q}} \sqrt{\frac{V_{ds}+V_{bi}-\Psi_S}{N_A(T)}}$$

$$y_d = y_s, \quad \text{at} \quad V_{ds} = 0 \qquad (4)$$

where the surface potential, Ψ_S, is roughly equal to $2(E_g/2 - E_{Fp})$. Unlike w_s and w_d, y_s and y_d decrease as the temperature is reduced[6] resulting in a larger L_{eff} which is defined as

$$L_{eff} = L - y_d - y_s \qquad (5)$$

This is represented, schematically, in Fig. 5 where we show the channel in equilibrium ($V_{ds} = 0$) both at 300K and 77K. In this figure we have indicated the lateral and vertical depletion layers, and demonstrated how L_{eff} changes by lowering the temperature. As a numerical example we indicated the values for w_s and y_s at the two temperatures, for $N_A = 1\times10^{14}cm^{-3}$, in the following

$$w_s(300K) = 3.2\ \mu m \quad y_s(300K) = 1.39\ \mu m$$

$$w_s(77K) = 3.75\ \mu m \quad y_s(77K) = 0.68\ \mu m\ .$$

III.3 Temperature Dependence of Delay Times

High-speed VLSI (very large scale integration) places extreme demands on devices for short delay times and low power-delay products. Here we present an experimental study of the advantages gained by reducing the operating temperature. We have measured the delay times (τ_d) and power-delay ($P\tau_d$) products as a function of temperature in the range 4.2K to 400K in different ring oscillators, having room temperature delay times between 30 ps and 270 ps, and found a considerable decrease in the delay times with decreasing temperature.

We have found that in order to explain our results not only did we need to consider the increase in transconductance (electron drift velocity), but also the decrease in the component of the capacitive load which is due to the source-drain junction capacitance to the substrate, due to a decrease in the number of ionized impurities.[9]

III.3.1 Delay Times

The changes in τ_d are summarized in Fig. 6. In order to show the general characteristics of the changes we have normalized the delay times, for each oscillator, at various temperatures to their room temperature delay time. In this figure we note that all three ring oscillators show the same behavior between 77K and 400K. At 4.2K, however, they demonstrate very different changes.

To discuss these characteristics we consider the following basic equation for the propagation delay time

$$\tau_d = B \frac{C_\ell}{I_{dd}/V_{dd}}, \tag{6}$$

where C_ℓ is the load capacitance at the output node, I_{dd} the current of the depletion mode device, V_{dd} the supply voltage, and B is a correction factor. Any changes in C_ℓ and/or I_{dd} with temperature would directly affect τ_d.

The short channel lengths (0.25–1.5 μm), and the relatively high drain voltages (3-5V) used in measuring τ_d, result in electron velocities equal or nearly equal to the saturation drift velocity, (v_{ds}). Saturation drift velocity increases with lowering temperature as a result of decrease in scattering. In Fig. 6 we have also plotted the changes in the inverse v_{ds} in the bulk Si as a function of temperature.[8] (Similar data for surface transport is not available. It is not expected, however, to be drastically different from the bulk.) The changes in v_{ds}^{-1} show a notable agreement with the changes in τ_d between 400K and 77K, suggesting that the decrease in τ_d in this range is mainly due to the increase in the electron saturation drift velocity.

Between 77K and 4.2K, v_{ds} remains fairly constant. The propagation delay time, however, continues to drop in this region, more in some ring oscillators than others. We believe that this further drop is due to changes in C_ℓ rather than I_{dd} in Eq. 6, as the following argument demonstrates.

The load capacitance is a function of the gate capacitance, C_g, the wiring capacitance, C_w, and the source/drain junction capacitance, C_j. C_g and C_w are relatively temperature independent, but since junction depletion width increases with reducing temperature the capacitance associated with it decreases. At 77K the decrease in C_j, compared with 295K, for a substrate doping of $10^{14}cm^{-3}$ is about 30%, but the change in this capacitance is particularly large below 10K where the freeze-out occurs. In this limit the junction depletion width becomes practically equal to the thickness of the wafer, and the capacitance associated with it becomes negligible. In some of our ring oscillators the magnitude of C_j was as large as 40% of C_ℓ. Hence its reduction to zero decreases τ_d drastically.

This explains qualitatively why τ_d continues to drop beyond the saturation of v_{ds}. The unequal reduction in τ_d in different ring oscillators is likely to be due to the differences in the junction area, therefore, unequal contribution of C_j to C_ℓ in these ring oscillators.

III.3.2 Power and Power-Delay Products

We have summarized the results, on P and $P\tau_d$, for 3 different ring oscillators in Fig. 7. Figure 7(a) shows the measured values of power as a function of temperature, and Fig. 7(b) the power-delay products. This figure indicates that both changes of power and power-delay product with temperature are small, and while the power shows a small increase with temperature, the power-delay product decreases.

IV. CONCLUSIONS

We have made comparisons between room temperature and liquid nitrogen temperature operation of Si MOS in 3 different areas. These were subthreshold currents, effective channel lengths and delay times. Our experimental results showed that in all three areas there was a definite improvement in the electrical characteristics of the devices. Namely that 1) the gate voltage swing for the device turn on reduced by nearly a factor of four, 2) the effective channel length became longer thus relaxing miniaturization conditions, as well as helping nearly short channel devices with some

punch-through current at 300K to completely turn off at 77K, and 3) the delay time of the ring oscillators decreased proportionally to the inverse of the increase in the electron saturation drift velocity.

I wish to thank S. M. Sze for helpful discussions, and R. L. Johnston for technical assistance.

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TABLE I

FABRICATION PARAMETERS

DEVICE LOT		7164 XA10	7039 XA11	3998 XP10
GATE OXIDE (Å)		236	240	230
FIELD OXIDE (μm)		0.30	0.18	0.26
CODED GATE LENGTH (μm)		1.25	1	2
ELECTRICAL CHANNEL LENGTH (μm)		0.25	0.4	1.4
CODED GATE WIDTH (μm)	DEPLETION	2.5	2	4
	ENHANCEMENT	7.5	5	20

C-2

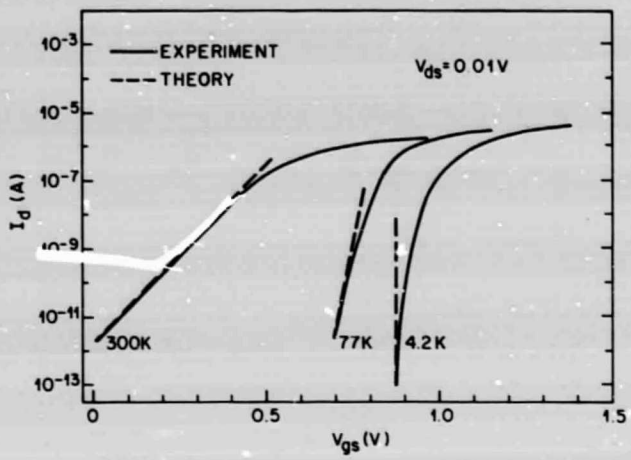

Fig. 1 Log I_d vs. V_{gs} traces at three different temperatures. The device parameters are: $N_A = 1E16cm^{-3}$, $t_{ox} = 500Å$, $L = 8\ \mu m$, $W = 80\ \mu m$ and $V_{sd} = 0.01V$, with maximum mobilities 800, 3000, 5200 $cm^2/V.s$ at 300, 77 and 4.2K respectively.

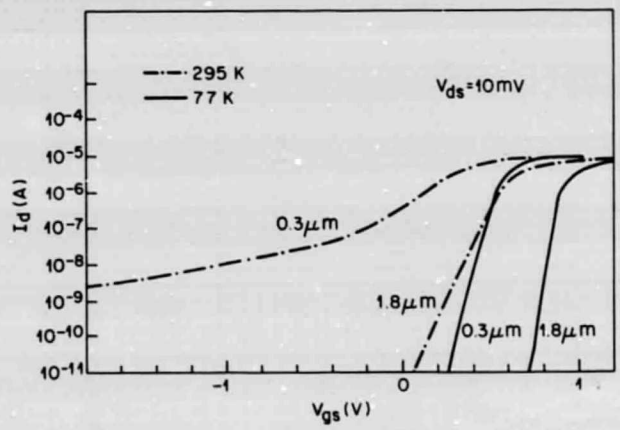

Fig. 2 Subthreshold current for a short and a long channel device at two different temperatures.

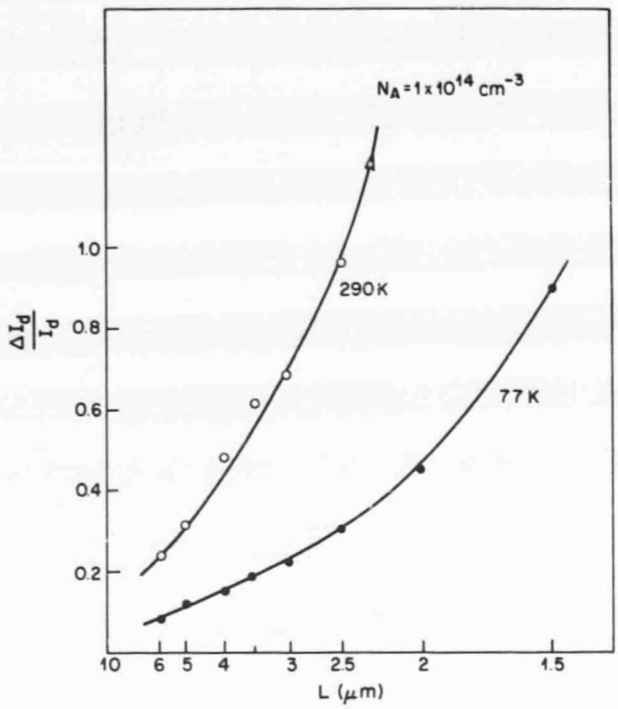

Fig. 3 The relative change in the drain current (at $V_g \cong V_{th}$) for a 100% change in V_d, for various device lengths, at two different temperatures.

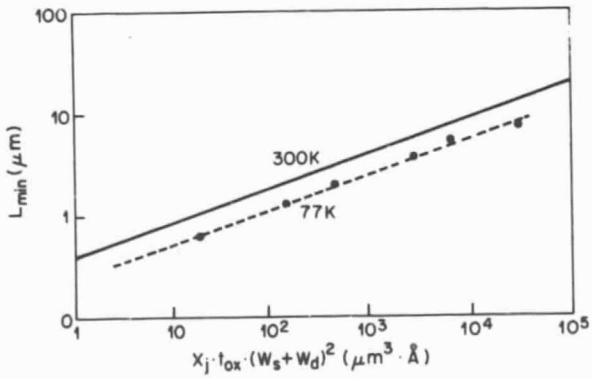

Fig. 4 L_{min} as a function of $x_j t_{ox}(w_s+w_d)^2$. The solid line is the room temperature result (Ref. 4) and the dashed line is drawn through the experimental points at 77K.

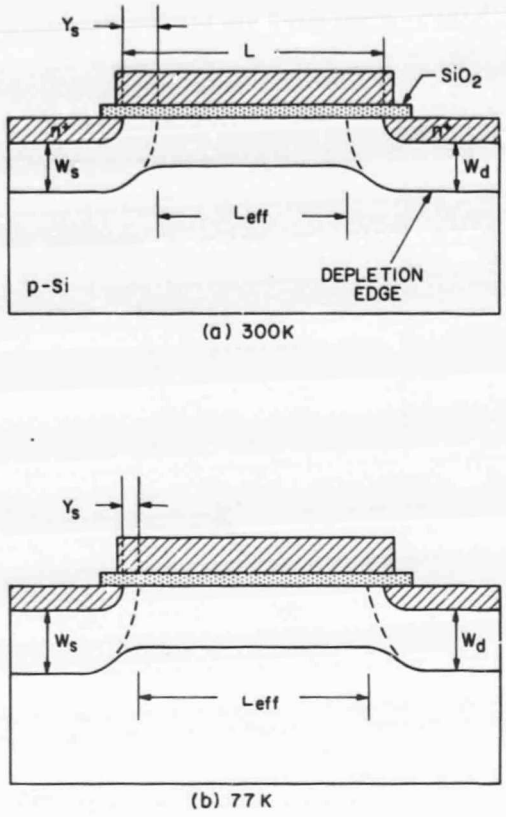

Fig. 5 The schematic representation of the channel, and the parameters y_s, w_s and L_{eff} at 300K and 77K.

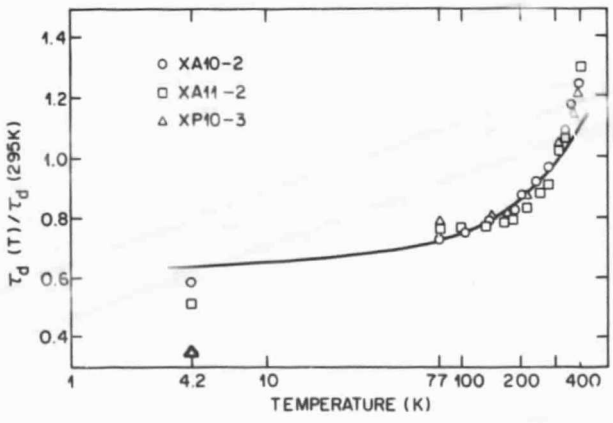

Fig. 6 The relative change in the delay times with respect to the room temperature delay as a function of temperature for three-ring oscillators. The solid line represents the corresponding change in the inverse saturation drift velocity in bulk Si.

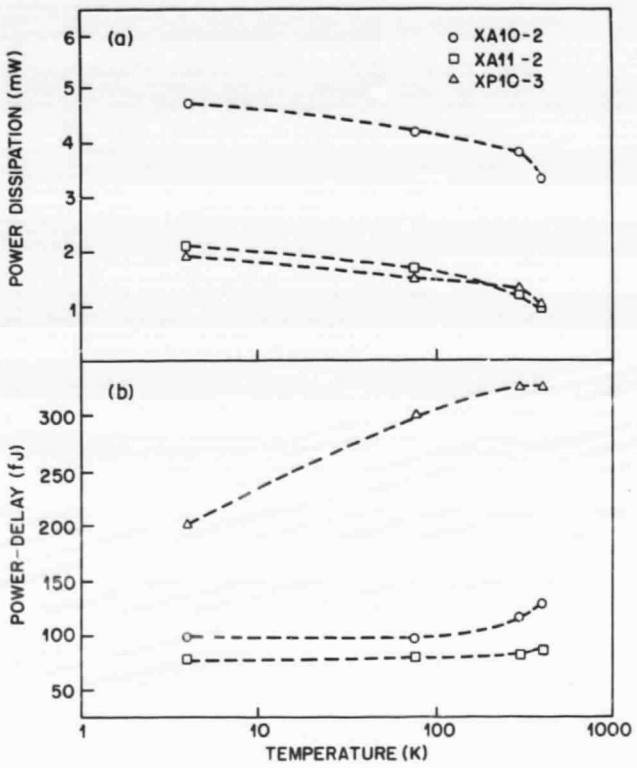

Fig. 7 (a) Power dissipation and (b) power-delay product as a function of temperature. The lines are drawn through the experimental points for clarity.

CRYOGENICALLY-COOLED, LOW-NOISE MICROWAVE RECEIVERS - PRESENT STATUS AND FUTURE NEEDS

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A complete writeup of the conference presentation is not available. However, an outline, the key figures, recommendations, and some references are given below:

Outline

I. State-of-the-Art Summary

A. Noise temperature vs. frequency in the 0.1 to 300 GHz range, Figure 1.

B. Same in the 100 to 3,000 GHz range, Figure 2.

II. Cooled GaAs FET Devices

A. DC characteristics of commercial GaAs FET's at 300K and 15K.

B. Noise vs. temperature for several commercial GaAs FET's, Figure 3.

C. Sources of noise, see reference [8].

D. Description of HEMT device.

E. Comparison of experimental cold noise performance of GaAs FET's and HEMT's, Figure 4.

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*The National Radio Astronomy Observatory is operated by Associated Universities, Inc. under contract with the National Science Foundation.

III. Examples of Cooled Microwave Amplifiers

A. 1.5 GHz amplifier, reference [6] and Figure 5.

B. 10.7 GHz amplifier, reference [7] and Figure 6.

IV. Cooling Technology

A. Test dewar with CTI 1020 refrigerator.

B. Coaxial input lines

V. Recommendations, see Figure 7 and text below.

Recommended Research and Development

A summary of a recommended low-noise cold microwave electronics program is given in Figure 7. Item 1) is for FET or HEMT devices giving a factor of 3 lower noise than present GaAs FET's with operation at 15K. The 1.5 GHz device must have low 1/F type noise and perhaps the ballistic transport short FET suggested by Eastman would be appropriate. The higher frequency devices could be HEMT's or perhaps improved conventional FET's.

A second R and D item is multiple-device integrated circuits having very low noise over octave bandwidths. The multiple devices allow balanced hybrid coupled amplifiers for power match and frequency-diplexed paths through separate HEMT devices for each $\sim$ 30% bandwidth where optimum noise match can be achieved. Five octave-band IC's would allow the entire 1-40 GHz microwave range to be covered.

Item 3 is for a microminiature refrigerator, either thermoelectric or gas flow, to be integrated into the FET package. A cooling capacity of 20 mW and temperatures of 150K with thermoelectric cooling or 50K with gas flow would be appropriate.

The fourth recommended area for cold electronics research is for low-noise amplifiers or mixers in the submillimeter wavelength region of 300 to 3,000 GHz. As shown in Figure 2, the noise temperatures presently achieved are very high and a breakthrough is needed for use in future space telescope or compact short-range radar systems.

A final area of recommended research is in the field of cooled microwave or millimeter wave focal plane arrays. A large number (10 to 1,000) of receivers could be deposited on a cooled substrate located in the focal plane of a paraboloidal reflector. The outputs of the array of mixers or amplifiers could then be combined to form many antenna beams, thus greatly increasing the speed of a scanning or image forming system.

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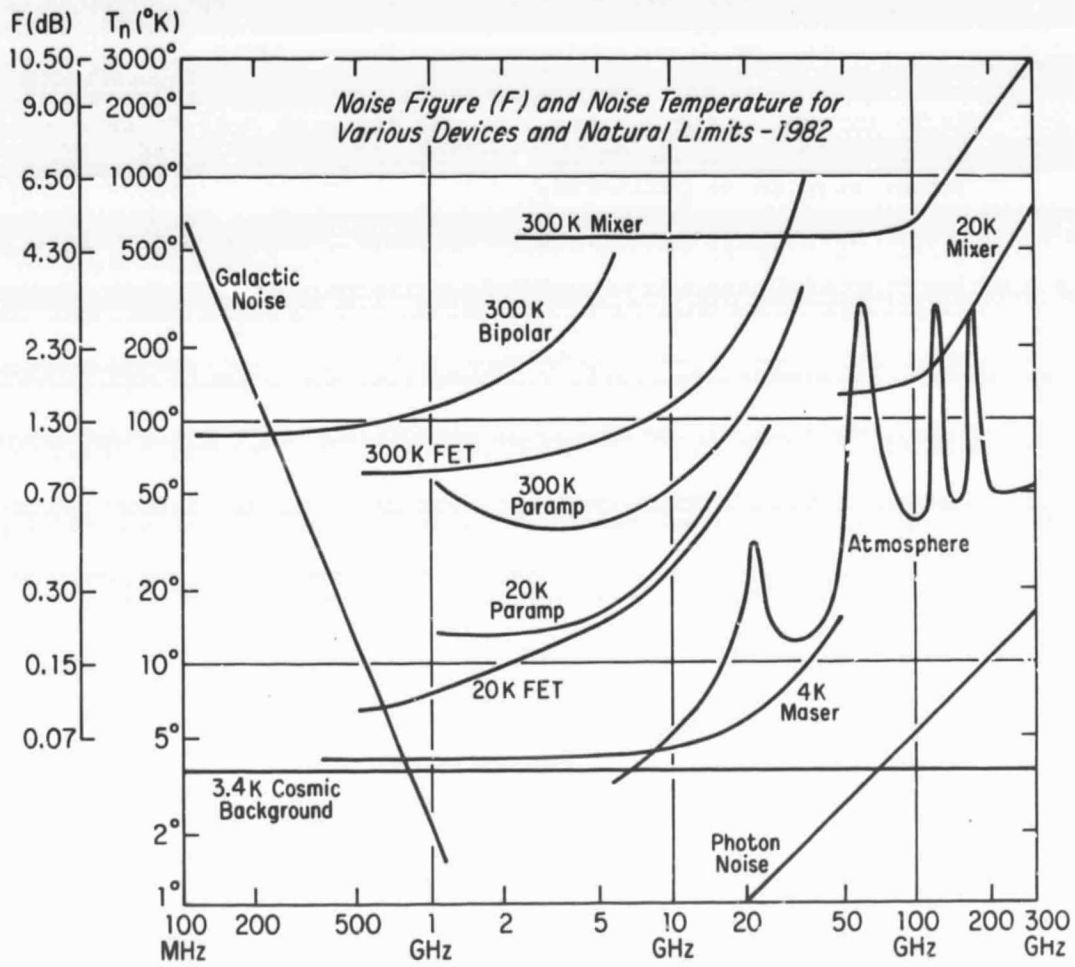

Fig. 1. Noise temperature of natural limits and cooled and uncooled devices from [1].

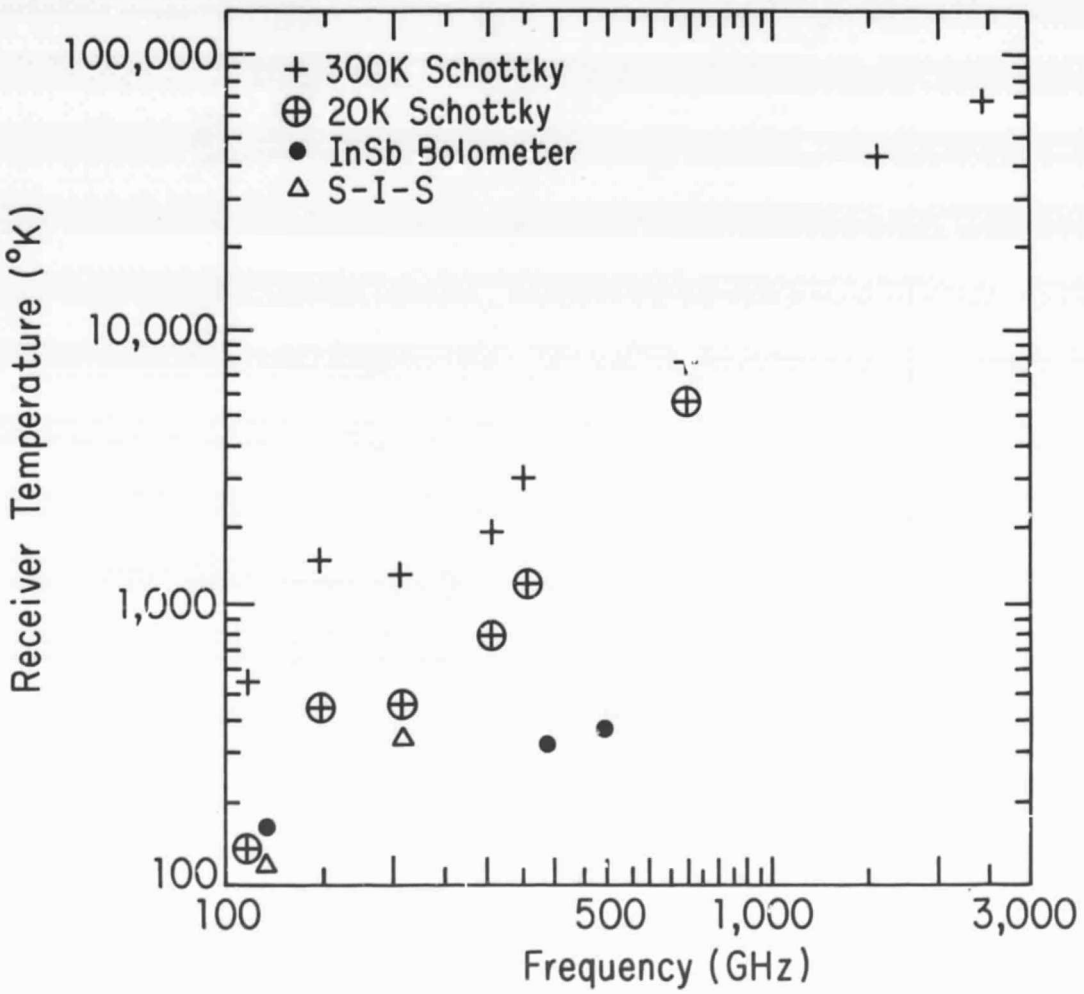

Fig. 2. Noise temperature of various cooled and uncooled millimeter and submillimeter receivers from [2].

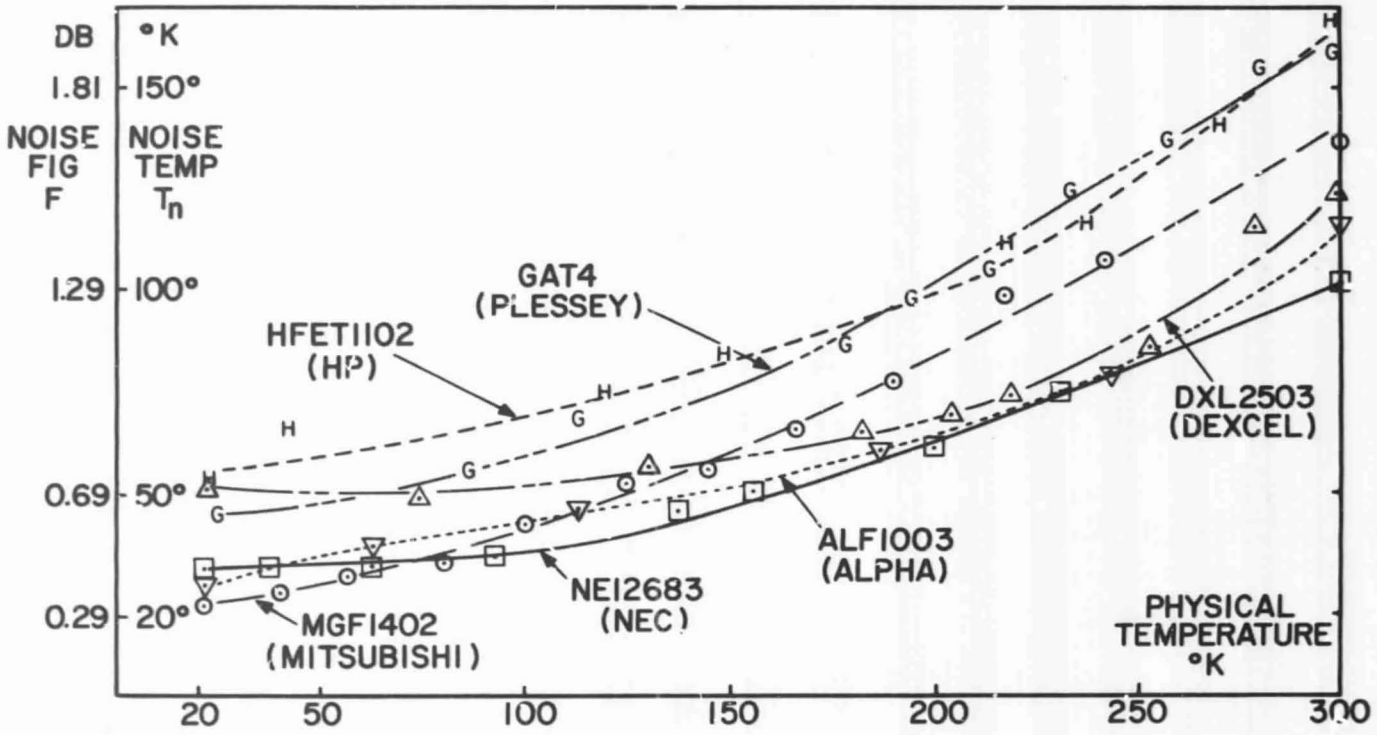

Fig. 3. Noise temperature vs. physical temperature for several manufacturers of GASFET's. Only one or two samples of the HP, Dexcel, Alpha, and Plessey devices were evaluated and units from another batch may give better cryogenic performance. See reference [3].

MFG	DEVICE	TEMP °K	F GHz	NOISE °K	12 GHz NOISE °K	REFERENCE
MITSUBISHI	GASFET MGF1412	15	8	19	28	NRAO MEAS.
NEC	GASFET NE67383	15	15	35	28	NRAO MEAS.
FUJITSU	HEMT	100	12	24	24	[4]
THOMSON-CSF	TEGFET	110	10	17	21	[5]

Fig. 4. Experimental noise performance of GaAs FET's and HEMT devices - 9/83. The 12 GHz noise temperature is an extrapolation of measurements made at 8, 10, or 15 GHz.

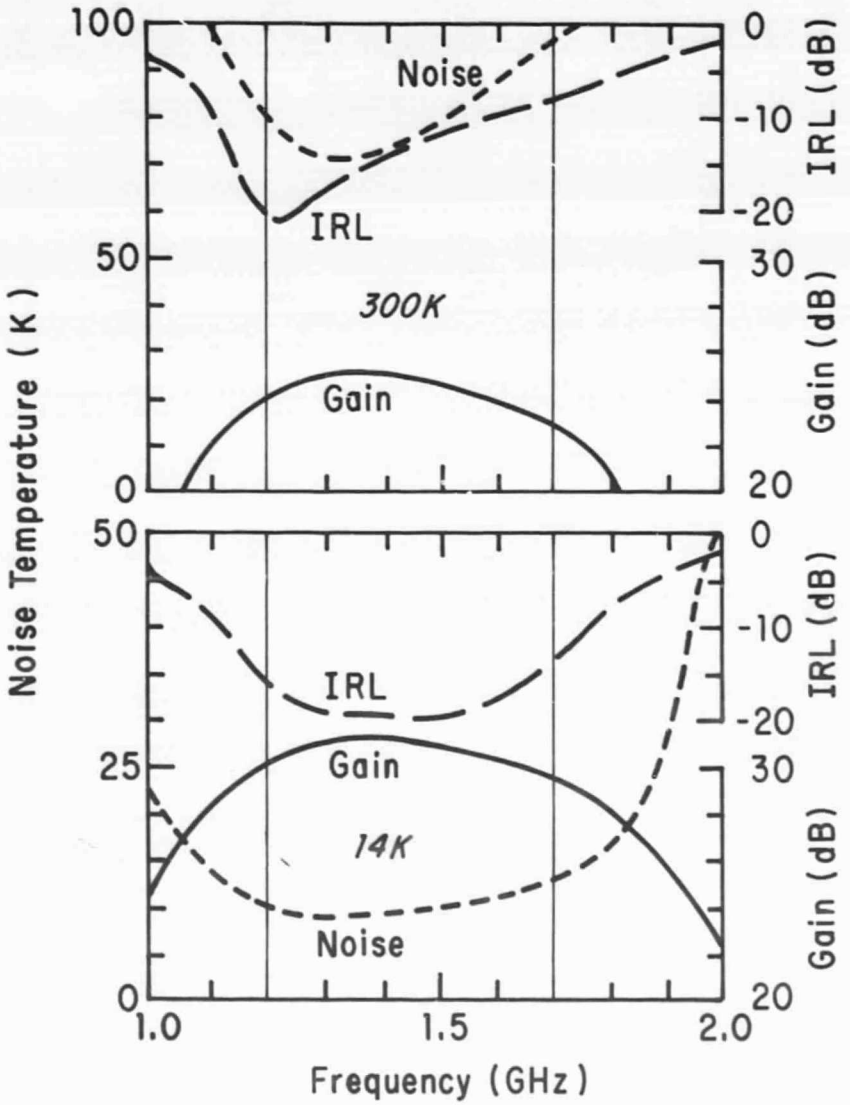

Fig. 5. Noise temperature, gain and input return loss of a 1.5 GHz GaAs FET amplifier at physical temperatures of 300K and 15K from [6].

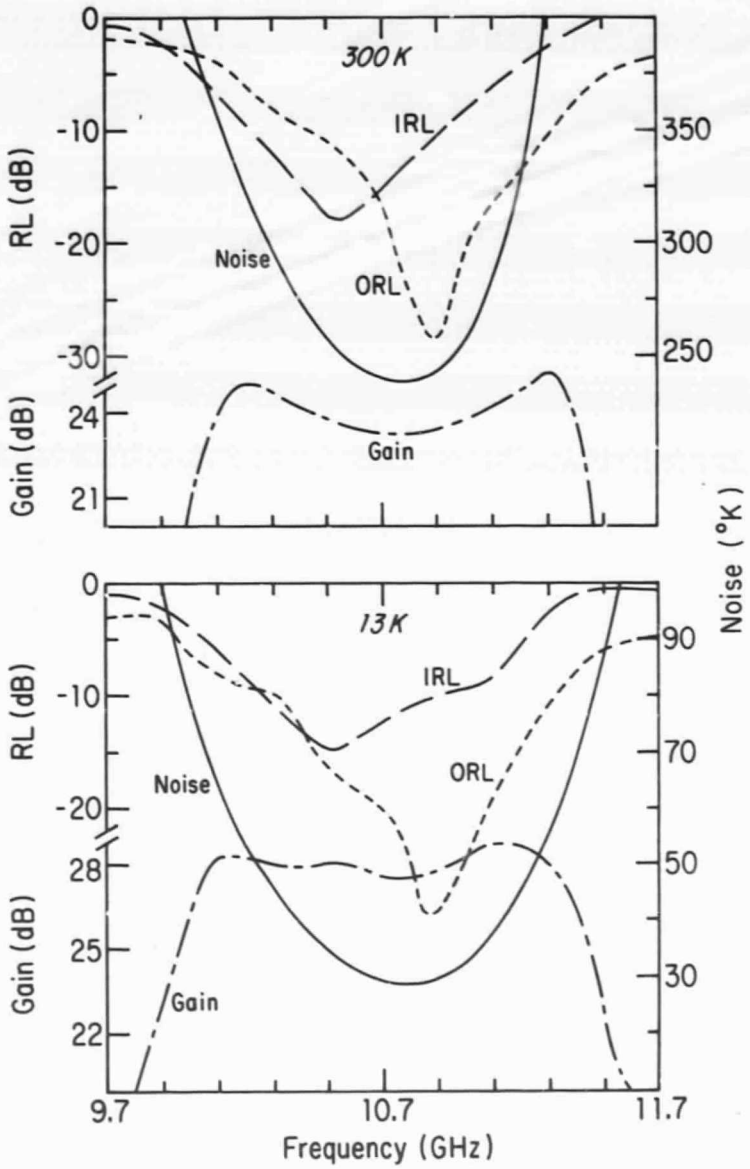

Fig. 6. Noise temperature, gain, input return loss, and output return loss of a 10.7 Ghz GaAs FET amplifier at 300K and 13K from [7].

RECOMMENDATIONS FOR COLD, LOW-NOISE

MICROWAVE ELECTRONICS PROGRAM

1) Devices with design goals @ 15K

GHz	T_n, °K	Type
1.5	3	Ballistic GASFET
8	8	HEMT
23	23	GASFET
40	40	HEMT

2) Multiple-device, octave-band MIC's

GHz	T_n, °K
1-2	5
2-4	10
4-8	15
8-18	20
18-40	40

3) Integrated device micro-refrigerator

4) 300-3,000 GHz (submillimeter) device research

5) Cooled focal plane arrays - integrated multibeam receivers

Fig. 7