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SUMMARY

Three 2 × 64 element charge-injection-device infrared detector arrays were tested at low and moderate background to evaluate their usefulness for space-based astronomical observations. Testing was conducted both in the laboratory and in ground-based telescope observations. The devices showed an average readout noise level below 200 equivalent electrons, a peak responsivity of 4 A/W, and a noise equivalent power of 3×10^{-17} W/$\sqrt{\text{Hz}}$. Array well capacity was measured to be significantly smaller than predicted. The measured sensitivity, which compares well with that of nonintegrating discrete extrinsic silicon photoconductors, shows these arrays to be useful for certain astronomical observations. However, the measured readout efficiency and frequency response represent serious limitations in low-background applications.

INTRODUCTION

A great potential exists for integrated multielement infrared (IR) detector arrays in astronomical applications. If an array of detectors had enough elements to match the number m of resolution elements in the telescope field of view, a mapping observation could be made in 1/m the time needed by a single detector system. Also, if flux from faint sources could be integrated in an array for extended periods and then sensed with only a small read-noise penalty, significant sensitivity improvements should be possible. These improvements apply for the ideal case, in which the single and arrayed detectors are of equal sensitivity and both have the same noise levels. There is also the serendipity factor: integrated arrays will likely make possible measurements or research programs which cannot be fully anticipated.

Our prime interest is in evaluating advanced IR arrays under conditions expected for IR space astronomy to determine how fully this potential might be realized. There are a number of anticipated low-background IR astronomical experiments which could effectively utilize integrated array technology. One such future orbital astronomical project is the Space Infrared Telescope Facility (SIRTF) (ref. 1). This ~1-m-aperture telescope will have all interior optical surfaces cooled to <7 K to reduce telescope thermal background radiation to levels comparable with the fundamental astrophysical backgrounds shown in figure 1 (ref. 2). Since the expected photon flux on a detector will be typically less than (or, for high spectral resolution, very much less than) 10^6 ph/s in this low-background environment, it is desirable to operate detector arrays with extended integration times. Also, it is obviously desirable to have arrays with minimum read noise levels.

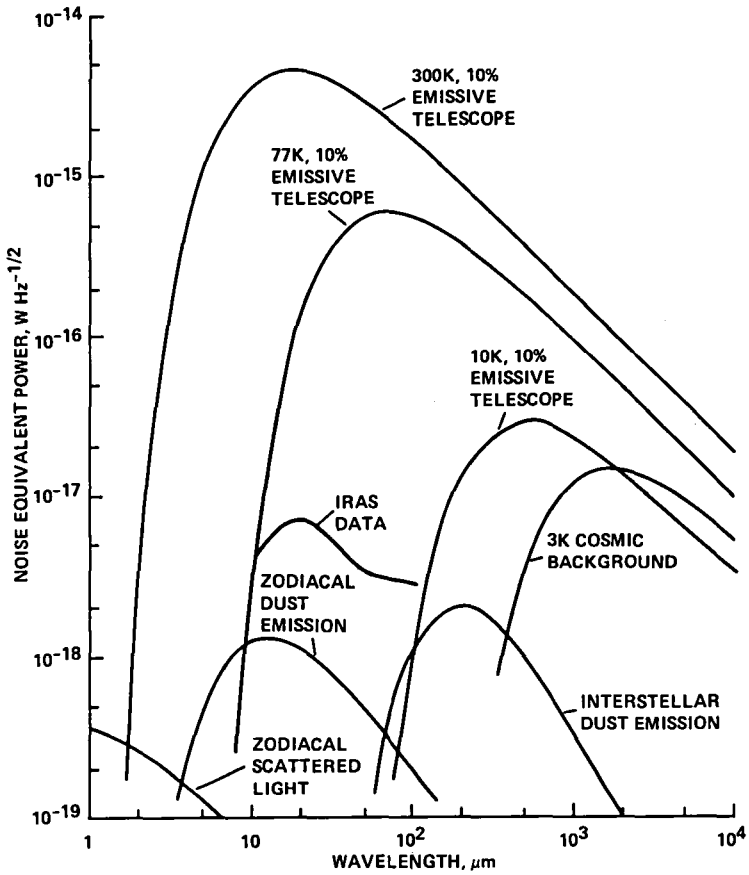


Figure 1.- Noise equivalent power limitations from astrophysical backgrounds. IRAS data taken from SIRTF Free Flyer Phase A System Concept Description, Ames Research Center, Document No. PD-1006, p. 2-37, May 3, 1984.

Furthermore, for the spectrometer and mapping instruments anticipated for SIRTF,[1] it is essential that these arrays be calibratable so that the absolute flux levels from astronomical sources can be measured.

The status of discrete extrinsic IR detector technology is summarized in references 3, 4, and 5. This technology has provided the foundation for development of the bismuth-doped silicon (Si:Bi) charge-injection-device (CID) arrays described below, and for various other integrated arrays (refs. 6,7,8). Si:Bi technology has successfully extended CID spectral response beyond the range of InSb, where a majority of the IR CID development work has been done (ref. 9). Our work was undertaken to establish how the Si:Bi CID operates under the unique conditions associated with space astronomy; namely, low-background, extended-integration-time, staring-mode operation.

[1]Shuttle Infrared Telescope Facility, Focal Plane Instruments and Requirements Science Team, Final Report. Ames Research Center, 1979.

DESCRIPTION OF DEVICE AND TEST SYSTEM

Detector Array

Three accumulation-mode CID Si:Bi integrated IR detector arrays were produced (under contract NAS2-10643) by Aerojet ElectroSystems Company, Azusa, Calif. (ref. 10). A photograph of one of the arrays and its cold electronics is shown in figure 2. Figure 3 is a schematic cross section of the unit cell of the array. Individual detectors are arranged in two rows of sixty-four, separated by a metalization 250 μm wide. Metalized gates (180 μm square), applied over a SiO_2 layer of 0.2 μm nominal thickness, define the individual detectors. On the opposite side of the substrate, a transparent electrode connects each row in common to the gate of a 3N163 MOSFET. Each side of the detector substrate incorporates an electrically isolated guard electrode to minimize within-row and between-row crosstalk.

The cutoff wavelength for this material lies near 18 μm, as shown in figure 4. [This spectral response curve was obtained on an Aerojet Si:Bi discrete photoconductive detector with a thickness (0.3 mm) and doping concentration (about 4×10^{16} cm^{-3}) similar to the CID detector.] Photons enter the Si:Bi through the transparent electrode and some fraction is absorbed, ionizing donor sites and producing free electrons. During the integration period these electrons are swept to, and collected at, the bulk-oxide interface by a positive "store" voltage (V_s) applied to each gate. A given detector is read out by briefly applying a negative "read" voltage (V_r) to its gate, driving the stored charge through the transparent

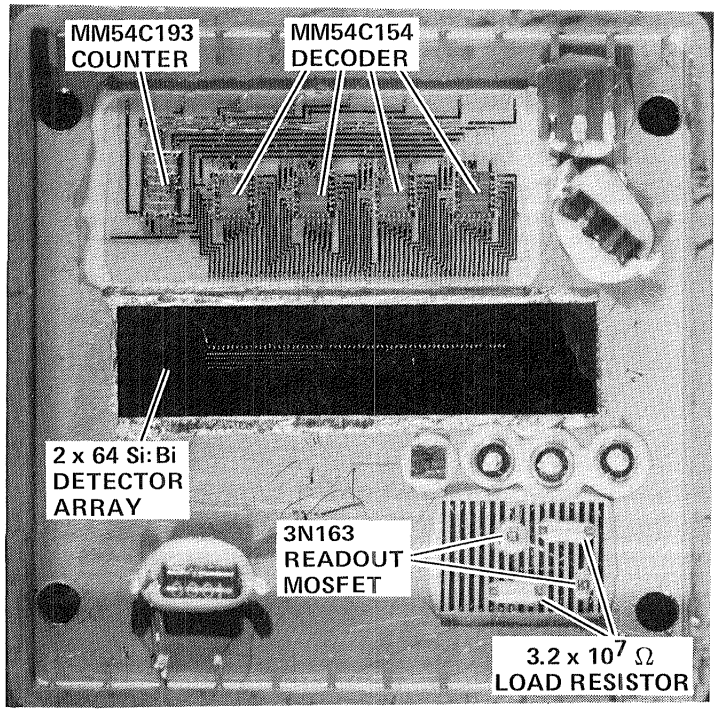


Figure 2.- 2 × 64 Si:Bi CID.

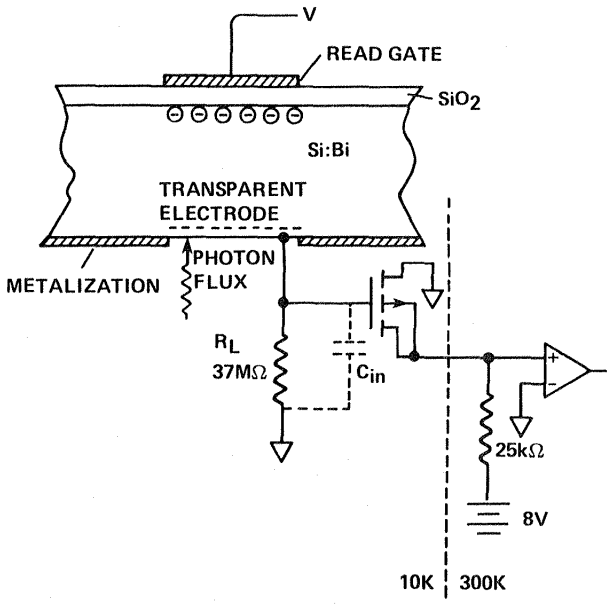


Figure 3.- Si:Bi accumulation-mode CID unit cell.

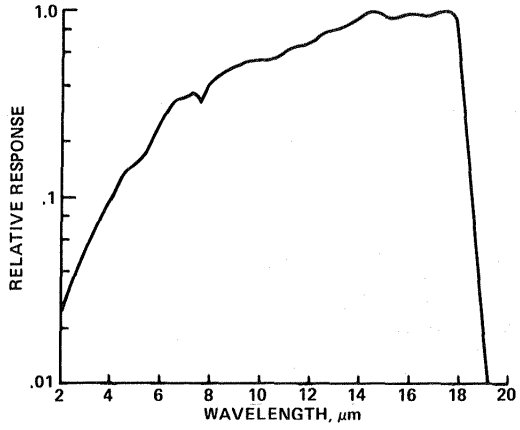


Figure 4.- Typical spectral response for Si:Bi detector.

electrode and onto the input capacitance (C_{in}) of the readout MOSFET. Operated as a source follower, the change in the MOSFET source voltage is directly proportional to the number of photons incident on the pixel during the integration period. The read pulse is sequentially applied to each pair of 64 detectors in the two rows, and then reset to the first pair to start a new frame.

Cold Electronics

As shown in figure 2, two cryogenic readout MOSFETs and their associated load resistors are mounted on a sapphire substrate in close proximity to the array. The load resistors (R_L, each about 3.2×10^7 Ω at 10 K) reset the MOSFETs between readouts

by allowing the accumulated charge to leak to ground (fig. 3). The $R_L C_{in}$ time constant for the passive reset is chosen to be long relative to the sample and hold (S/H) acquisition time and short relative to the dwell time on a given pixel.

Also mounted on the array butterfly package are the CMOS scanning electronics that sequentially apply the store and read voltages to the array gates. An MM54C193 four-bit counter simultaneously clocks four MM54C154 four-to-sixteen line decoders, each of which in turn routes store and read voltages to one of four banks of 16 detector pairs. An externally generated pulse sequentially enables the decoders to read out the array, resulting in two parallel output streams from the readout FETs. A timing diagram for a single frame is shown in figure 5.

The total power dissipation in the array package is about 6 mW, consisting of about 1 mW per MOSFET and a frequency-dependent maximum of 4 mW (at 1 kHz frame rate) for the CMOS components.

Warm Electronics

An ambient temperature preamplifier with a 0.7-50 kHz bandwidth is located on the test dewar near the array. The preamp has a gain of 200 and provides the input to the correlated double sampling (CDS) circuit in the main electronics box. Pictures of the array signal output in continuous analog and discrete-sampled forms are shown in figure 6. The CDS circuit generates the difference in MOSFET source voltage just before and just after the read pulse is applied and holds it for subsequent processing. This method has been shown to suppress 1/f noise (ref. 11). Note that this sampling scheme, commonly known as "delta reset," is different from the conventional CDS approach in which the sample pair does not straddle the read

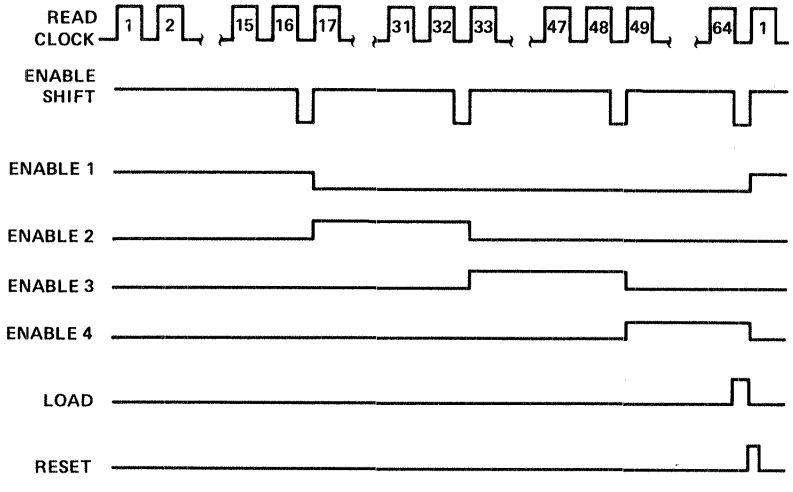
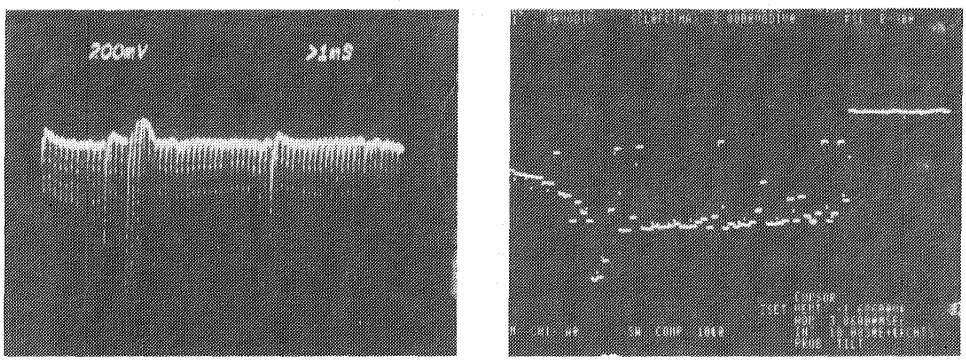


Figure 5.- Timing diagram for one read frame.



(a) PREAMP OUTPUT (UNSAMPLED) (b) PREAMP OUTPUT (CDS)

Figure 6.- Effect of correlated double sampling (vertical scales differ).

pulse. The present sampling scheme allows rapid sampling of a full matrix of array elements, at the expense of the kTC uncertainty introduced by the reset pulse.

Also contained in the electronics box is the digital circuitry which generates the timing and drive pulses for the array. Analog and digital circuits are optically coupled and have separate grounds to keep clocking noise out of the sample/hold section. Integration time (t_i) can be varied either continuously (by adjusting the master clock frequency f_c), or by factors of two (via a pair of thumbwheel switches on the main electronics box) (ref. 10). One switch increases t_i by dividing the master clock frequency by 2^N (N being a selectable integer). The other achieves a similar result by inserting 2^M "rest" frames between successive read frames, during which all pulses to the array are inhibited. Together these effects yield a resultant t_i of $2^{N+M}\times(64/f_c)$. The minimum integration time is about 8 ms, limited by the effective $R_L C_{in}$ time constant. Controls are also provided to set the voltage levels of the guard electrodes and those of V_s and V_r.

Test Setup

Laboratory tests were performed with the array mounted in a Lakeshore Cryotronics Model 310 cryostat. The overall test system has been described previously (ref. 12). A block diagram of the test system is shown in figure 7, and a schematic cross section of the cryostat is shown in figure 8. For this work, an aperture arrangement defining a solid angle of 7.44×10^{-5} sr (f/103 beam) was used to restrict background flux and limit the detector field of view to the vacuum window (KRS-5, 72% transmittance) and the chopper blade/blackbody cavity. Narrow bandpass interference filters (see table 1) were placed in the beam to check three points on the spectral response curve. For low-background testing, a nichrome-on-silicon neutral density filter (0.6% transmittance) was also used. A range of blackbody temperatures and the various filter combinations provided each pixel with signal fluxes between 7×10^5 and 2×10^9 ph/sec. Diffraction losses were calculated to be less than 5% (by using the methods of ref. 13).

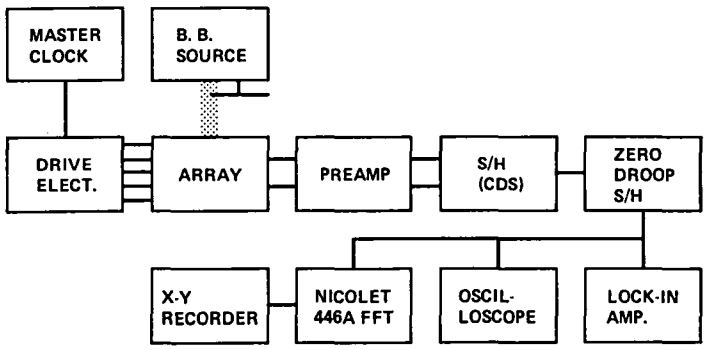


Figure 7.- Electronics block diagram.

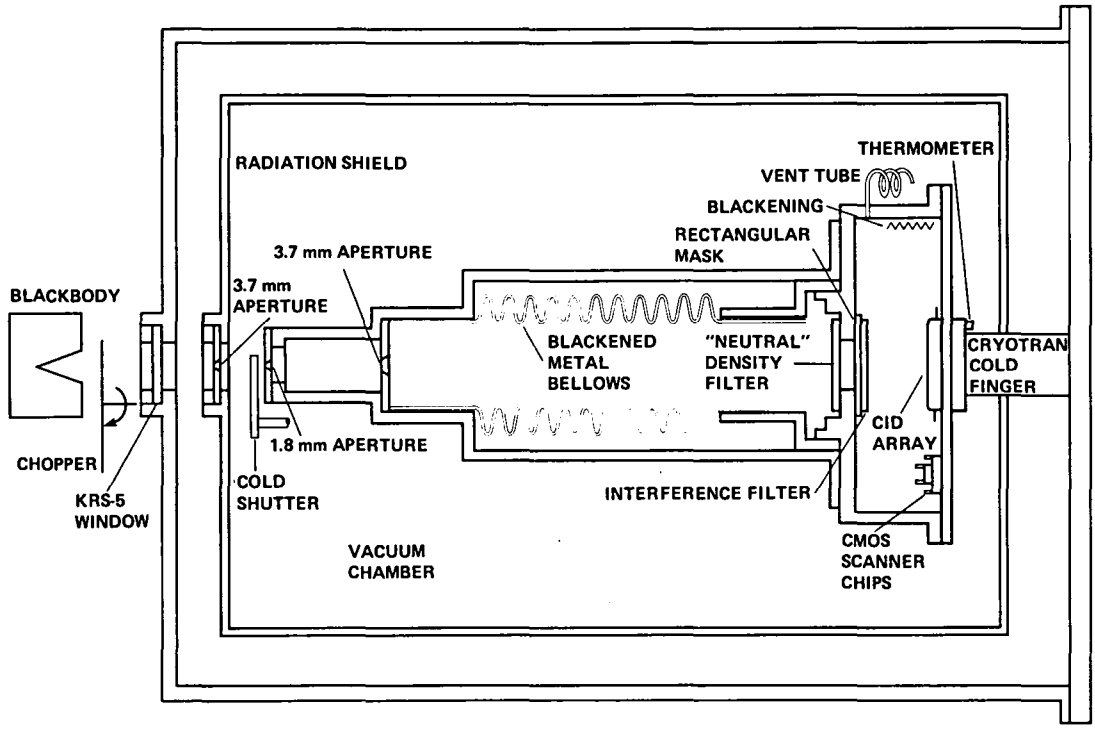


Figure 8.- Test dewar configuration.

TABLE 1.- SPECTRAL FILTERS

Center wavelength, μm	Bandwidth, μm	Peak transmittance, %
3.6137	0.0341	94
4.6170	.0373	81
11.03	.064	72

Background fluxes from the room-temperature chopper blade ranged over four orders of magnitude (from 2×10^3 to 4×10^7 ph/sec) in the various filter configurations. Noise spectral density and wideband integrated noise were measured with a Nicolet 446A FFT spectrum analyzer.

RESULTS

A substantial amount of time was spent in characterizing and intercomparing the three arrays. While the arrays exhibit minor manufacturing-related differences, it appears that present technology allows the production of rather similar devices. While each array has a somewhat different set of optimum operating parameters, optimized performance does not vary significantly from one array to another. Table 2 contains a summary of representative data taken over the course of the testing program, and table 3 shows the pixel-to-pixel and array-to-array variances observed.

While the contents of tables 2 and 3 represent typically good performance levels, they do not reflect best-case performance in any one parameter save that of noise equivalent power (NEP). They are meant to indicate levels of performance obtainable in typical operation. Further, table 3 falsely suggests that array 8107 is significantly superior to the other two. Actually, this array rather arbitrarily became the focus of the most detailed and efficient test efforts. In light of time constraints and of our overall assessment of the potential of this technology it was not worthwhile to retest the other two arrays under the operating conditions that yielded the best performance for array 8107. However, there is no reason to believe that arrays 8106 and 8101 would not perform as well if retested under similar conditions. While the existing data base is insufficient to fully demonstrate this, the limited amount of comparable data that were obtained supports this assertion.

The three 2 × 64 arrays exhibited a high degree of uniformity, on both pixel-to-pixel and array-to-array bases. Once good uniformity had been established for an array, efforts were concentrated on the characterization of a few representative array elements. Signal and noise were analyzed under a variety of conditions and the various detector figures of merit were calculated. Key independent variables were V_s, V_r, integration time, blackbody temperature, background level, filter configuration, chopping frequency and array temperature.

Signal-to-Noise Ratio (SNR) Optimization

As a first step, the optimal operating conditions for each array were established. This was accomplished by varying read and store voltage levels, array temperature, read pulse width, and S/H delay to obtain the highest sensitivity, i.e., maximum SNR.

TABLE 2.- 2 × 64 Si:Bi CID DETECTOR ARRAY GENERAL CHARACTERISTICS

Characteristic	Data	Units	Conditions
		General	
Material	Si:Bi		
Dopant concentration	4×10^{16}	$Atoms/cm^3$	
Layout	2×64	Element	
Pixel dimensions	180	Micrometer	Square
Pixel spacing	220	Micrometer	Lengthwise
Wavelength range	3-18	Micrometer	
Test backgrounds	2×10^{3}-4×10^{7}	Ph/sec	
	6×10^{6}-1×10^{11}	Ph/cm^2-sec	
		Performance	
Responsivity	2.4	A/W	@11 micrometers
	4.0	A/W	@16 micrometers (est)
Responsive quantum efficiency	27	%	@11 micrometers
Read noise	150	Electrons/sample	rms
NEP	3×10^{-17}	$W/\sqrt{Hz}$	t_i = 256 ms Bkgrnd = 2.3×10^{5} ph/sec λ = 11 μm
Input capacitance	4	pF	
Dark current	$<1.6\times10^{-17}$	A	
	<100	Electrons/sec	
Well capacity	5×10^{5}	Electrons	
Maximum integration time	80	Minutes	Dark current limited
Frequency response	0-20	Hz	Bkgrnd = 4×10^{7} ph/sec
	0-2	Hz	Bkgrnd = 2×10^{5} ph/sec
Max read rate	500	Frames/sec	
Operating temperature	8-14	K	
Uniformity	10	%	One sigma/mean

All data taken at (V_s, V_r) = (0, -10) and T = 11 K except as noted.

TABLE 3.- 2 × 64 Si:Bi CID ARRAY INTERCOMPARISON

	Array serial number		
	8101	8106	8107
Uniformity (1 σ)	35%	40%	25%
Responsivity (A/W)	1.9	1.9	2.4
Quantum efficiency	23%	23%	27%
Noise electrons	248	293	150
NEP (W/$\sqrt{Hz}$)	7E-16	7E-16	3E-17
Dead pixel pairs	3	0	6
$R_L C_{in}$ - limited 3 dB frequency (Ch 1, Ch 2) (Hz)	(1243,1184)	(938,1058)	(1243,1275)
C_{in} (Ch 1, Ch 2) (pF)	(4.0,4.2)	(5.3,4.7)	(4.0,3.9)

All three arrays showed decreased sensitivity as the store voltage was increased above 0 V. Increasing the magnitude of the read voltage enhanced response, although beyond about -11 V sensitivity began to drop due to an increase in noise. Also, as figure 9 indicates, values of V_r beyond -9 V adversely affected array uniformity. An optimum value for V_r of -10 V was selected for the majority of subsequent testing. Figure 10 shows SNR as a function of V_s and V_r.

SNR was measured as a function of array operating temperature from 5 to 20 K. Good response was observed between 8 and 16 K, with slightly superior performance at 11 K (see fig. 11).

The read pulse width and the location of the sample point on the output waveform have only minor effects on performance. A read pulse width of ~5 μs followed by a S/H pulse ~1 μs later was found to be optimal.

Responsivity, Quantum Efficiency

The measured output voltage is used to determine the current responsivity (R_i) in units of A/W:

$$R_i = [V(T_{bb}) - V(300\ K)]C_{in}/[\Phi(T_{bb}) - \Phi(300\ K)]gt_i \qquad (1)$$

Here g is the system gain between the readout MOSFET gate and the S/H output, and V(T) and Φ(T) are the measured voltage and calculated incident radiation power (in watts) corresponding to a blackbody source of temperature T_{bb} filling the

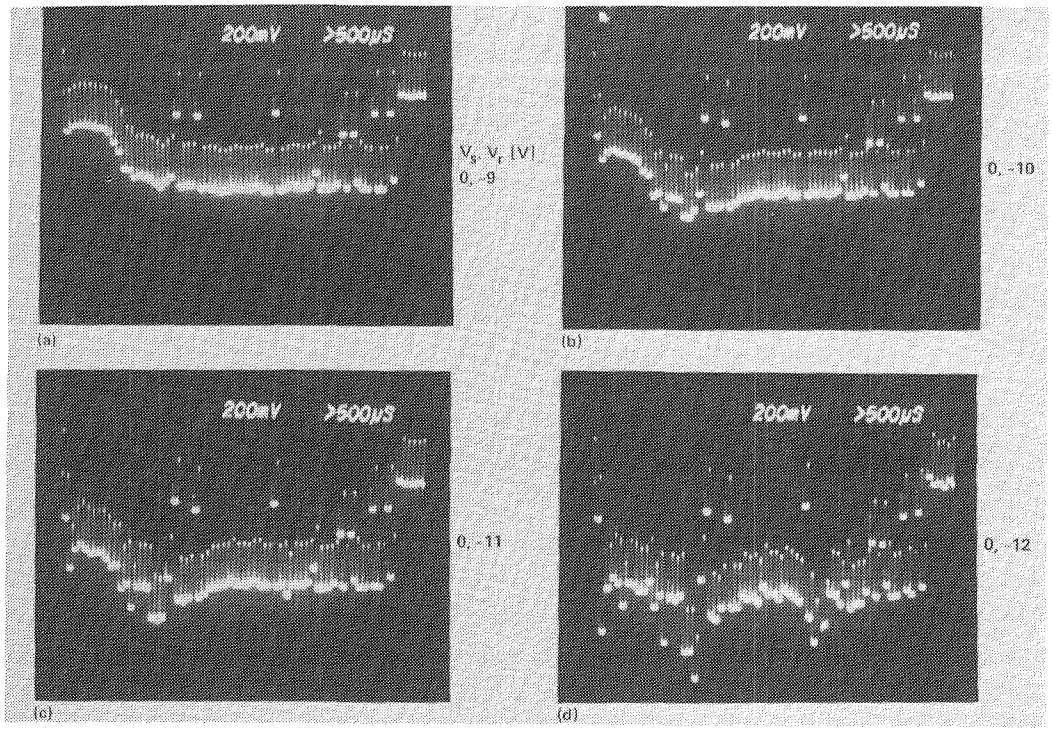


Figure 9.- Uniformity variation with V_r.

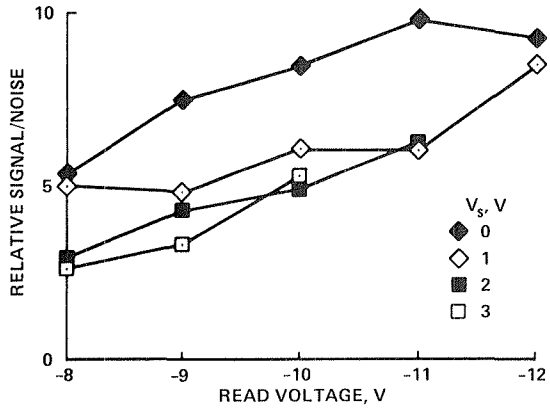


Figure 10.- Relative signal to noise ratio vs. V_r.

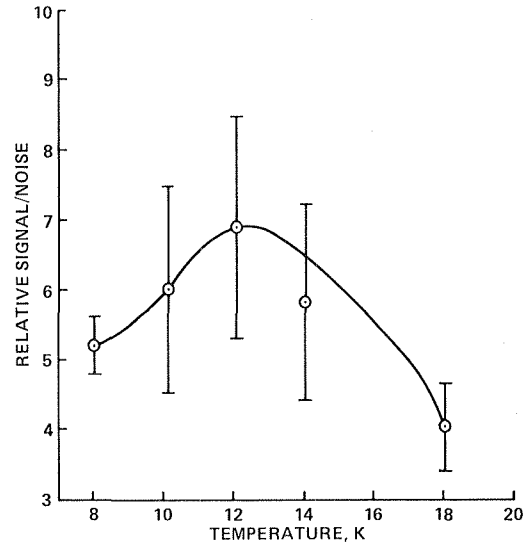


Figure 11.- Relative signal to noise ratio vs. operating temperature.

field of view. The accuracy of the responsivity is limited primarily by uncertainty in the flux calculation, and is estimated to be ±20%.

An average value of the responsivity measurement for typical pixels measured at 11 μm is R_i = 2.4 A/W. Normalizing to peak response at 16 μm using the

manufacturer's stated spectral response (fig. 4) for Si:Bi yields a peak responsivity of 4.0 A/W. Figure 12 shows the pixel-to-pixel variation in peak responsivity for one of the arrays. Pixel-to-pixel uniformities ranged from 10-40% (1 σ/mean) for the three arrays. The uniformity was found to vary significantly with V_s and V_r settings, with the trend being greater nonuniformities at the highest-sensitivity operating point (i.e., largest $[|V_s| + |V_r|]$ values).

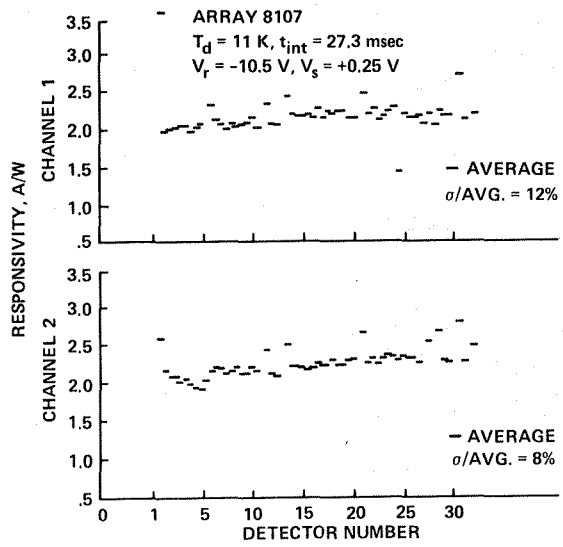


Figure 12.- 2 × 64 array uniformity measurements.

Current responsivity is represented by

$$R_i = e\eta_r\lambda/hc$$

$$= 0.806\ \lambda\eta_r \qquad (2)$$

where λ is wavelength in μm, η_r is responsive quantum efficiency, e is the electronic charge, h is Planck's constant, and c is the speed of light. (Note that for a CID, no photoconductive gain mechanism is assumed (ref. 12).) Using this equation we calculate an average low-background responsive quantum efficiency of 27% at 11 μm. At λ = 4.6 and 3.6 μm, the measured quantum efficiency drops to 3.2 and 1.2%, respectively. These results are in general agreement with a semi-empirical model, developed by C. T. Sah (ref. 14) and refined by Aerojet, which predicts optical cross section as a function of photon energy. Assuming a donor ionization energy of 0.071 eV and a Bi concentration of 4×10^{16} cm^{-3}, this model predicts quantum efficiencies of 26.6, 4.6, and 2.9%, for 11.0, 4.6, and 3.6 μm, respectively.

Well Capacity

Figure 13 shows device response as a function of integrated flux (ph/sec × t_i). It indicates that the linearity of the detector is good up to an integrated charge of about 5×10^{15} electrons. Beyond this point there is a continuing roll-off of response with increased integrated flux. This well capacity (the amount of charge that can be stored in a pixel) is consistent with theoretical predictions based on the premise that, with a 0 V store voltage on the gate, the well capacity is determined by the difference in work function between metal and semiconductor. This work function difference is about 0.01 eV. This translates to a well size of a few times 10^5 electrons for an SiO_2 layer of this thickness containing a negligible amount of "trapped" charge. Were the array able to run a +2 V store voltage without suffering a significant loss in sensitivity, the predicted well size would increase to about 10^8 e^-, or by a factor of 150-200. Why the SNR of this generation of CID arrays suffers at substantial store voltages is not understood; this is an important item for additional research if this technology is to be advanced.

Noise

Typical noise spectra obtained with the FFT spectrum analyzer are shown in figure 14. The $[(\sin \chi)/\chi]^2$ form of these traces is characteristic of sampled output devices whose integrated noise voltage, V_n, is expressed

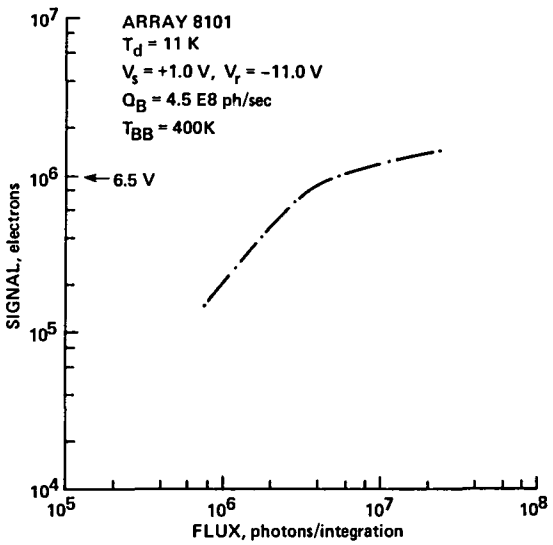


Figure 13.- Well capacity measurement: response vs. integrated flux.

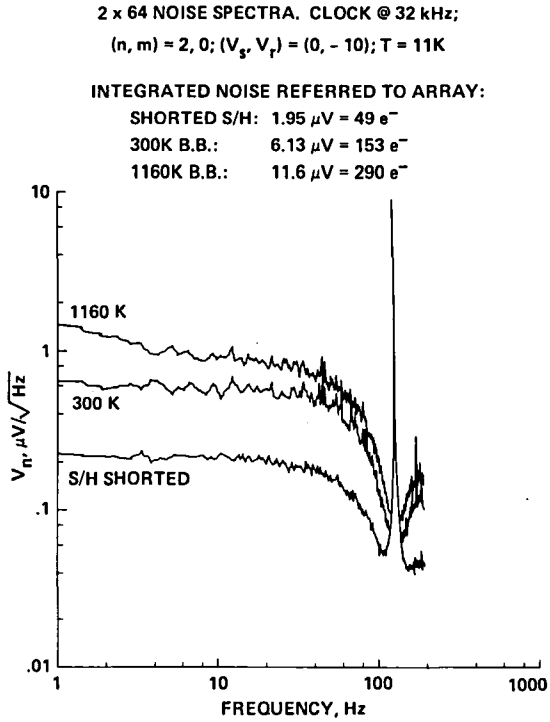


Figure 14.- System noise vs. frequency.

$$V_n = \left\{ \int_0^\infty [v_n(f)(\sin \chi)/\chi]^2 \, df \right\}^{1/2} \tag{3}$$

where v_n is the noise voltage spectral density at frequency f and χ is $\pi f t_i$. The relevant noise bandwidth Δf_e is obtained from this expression under the assumptions that samples are uncorrelated, and that v_n is at most weakly dependent on frequency:

$$V_n = v_n \left\{ \int_0^\infty [(\sin^2 \chi)/\chi^2] df \right\}^{1/2} = v_n \sqrt{1/2t_i}$$

or

$$\Delta f_e = \sqrt{1/2t_i} \tag{4}$$

Reference to the S/H input-shorted noise curve in figure 14 gives a value for v_n in the flat (low-frequency) portion of the spectrum of 0.24 $\mu V/\sqrt{Hz}$. This value substituted into equation (4), along with the integration time (8 ms), yields an integrated noise voltage of 2 μV rms. This can be converted to equivalent electrons with the expression

$$n = (C_{in} V_n)/ge \tag{5}$$

where g is product of the preamplifier and readout MOSFET gains (200 × 0.8). With a C_{in} value of 4 pF, 2 μV corresponds to 50 rms electrons. With the array connected to the S/H input and receiving minimal photon flux, the noise from the readout MOSFET sets the array readout noise at about 150 rms electrons.

A hot blackbody source placed in the FOV raises the noise level due to the increased contribution of photon noise. For the blackbody temperature (1160 K, 1×10^7 ph/sec) and integration time (8 ms) used to obtain figure 14, the photon noise contribution is about equal to the fixed readout noise. For other conditions (i.e., higher backgrounds and/or longer integrations) photon noise is the dominant noise source.

The CDS sampling technique effectively suppresses 1/f noise, and spectra are flat down to the lowest frequencies tested (about 0.2 Hz). Aliased 60 Hz noise, which had been a problem early in the testing program, was eliminated with an improved grounding scheme.

The large spike apparent in figure 14 at the sampling frequency is due to S/H "droop" (charge leakage from the hold capacitor in the S/H circuit). This spike has since been removed through the incorporation of a digital S/H unit. In the digital S/H, a 256 kHz A/D converter is triggered at every S/H pulse. A D/A converter connected to the outputs of the A/D is strobed by the end of conversion pulse from the A/D. The result is a zero-droop output signal that leaves detector

well size as the only limit on the length of integration (in the absence of ionizing radiation).

Noise was found to be essentially independent of operating temperature below ~16 K, and to increase gradually as the temperature was raised beyond this point. A carrier freezeout temperature of 15 K has been estimated by Aerojet for this material, so increased dark current due to thermal charge generation is a likely cause of this noise. It should be noted, however, that spectral analysis of the high temperature noise shows a 1/f dependence not expected in thermal noise.

Photon Noise Limit

The array noise performance must ultimately be compared to fundamental physical limits. The total noise n is composed of various (presumably) uncorrelated noise sources such as read noise n_r, background-induced photon noise n_p, current (1/f) noise n_c, thermal generation-recombination noise n_t, and others which combine in quadrature:

$$n = \{n_r^2 + n_p^2 + n_c^2 + n_t^2 + \ldots\}^{1/2} \tag{6}$$

For an ideal detector array whose excess noise sources can be neglected, the system noise would be limited by

$$n = n_p = (t_i \eta_r \lambda\Phi/hc)^{1/2} \tag{7}$$

where $\lambda\Phi/hc$ is the photon flux in ph/(pixel - s). With 25% quantum efficiency and a background level of 10^6 ph/sec, photon noise begins to dominate the fixed read noise for $t_i > 0.25$ sec. Figure 15 compares the actual noise performance of these arrays (upper curve) with the theoretical limit imposed by photon noise. This limit is calculated from equation 7 (lower curve) as a function of integrated flux. The two curves approach each other rapidly, indicating that photon noise is dominant at all but the shortest integration times.

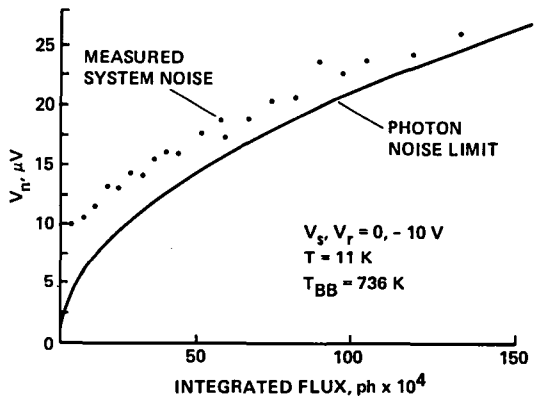


Figure 15.- Noise vs. integrated flux.

It should be noted that a correction has been applied in figure 15 to take into account the nonlinearity of the array at extended integration times reflected in figure 13. Over-filling of the wells leads to an apparent decrease in the measured responsive quantum efficiency, because the excess charge is not collected. For this reason the apparent quantum efficiency at each integration time has been used in the calculation of the performance limit through equation 7.

Noise Equivalent Power (NEP)

Defined as the incident radiation power necessary to produce an SNR of one in a unit noise bandwidth, the NEP of an integrating array is given by:

$$\begin{aligned} \text{NEP} &= \{\text{rms noise/responsivity}\} \;/\; (\text{noise bandwidth})^{1/2} \\ &= \{ne/R_i t_i\}/\Delta f_e^{\,1/2} \\ &= (ne/R_i) \times (2/t_i)^{1/2} \end{aligned} \tag{8}$$

A 1-sec integration at negligible background (where fixed read noise dominates) would thus yield an NEP of 1.0×10^{-17} W/$\sqrt{\text{Hz}}$ at peak responsivity. The best observed NEPs over the experimental range of background and integration time were about 3×10^{-17} W/$\sqrt{\text{Hz}}$, demonstrating a sensitivity that compares well with that of good nonintegrating discrete detector systems at these wavelengths.

Equation 8 shows a key sensitivity advantage of integrating devices over continuous-readout schemes, in that NEP varies inversely with the square root of integration time. In principle an integrating detector, with a well capacity of at least a few times n_r^2 and low leakage current, can integrate long enough so that its fixed read-noise contribution is negligible in comparison to the accumulated photon noise. The measured relation between NEP and t_i is shown in figure 16.

NEP can be used to define another system figure of merit, the detective quantum efficiency, $\eta_d \cdot \eta_d$ is given by the square of the ratio of the background-limited NEP and the measured NEP of the array:

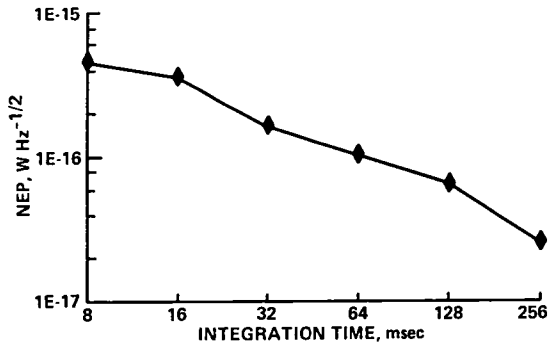


Figure 16.- Noise equivalent power vs. integration time.

$$\eta_d = (2\Phi_b hc/\lambda)/NEP^2 \qquad (9)$$

where Φ_b is the radiant power due to background (in watts) falling on the detector. Calculations at optimum NEP yield detective quantum efficiencies of 26% at 11 μm. This agrees well with the measured responsive quantum efficiency, indicating that the array is essentially free from extraneous noise sources.

Dark Current

In the evaluation of these devices for space-based astronomy, an important consideration is the maximum possible integration time. This is limited by the well capacity and the magnitude of the "dark current" (I_d), the rate of charge generation from nonoptical sources. The manufacturer estimates a value of less than 200 electrons/sec.[2] Due to the inherent difficulty of measuring such small currents, our tests (using integration times of several minutes with the device viewing the 11 K cold shutter) did not yield a strictly repeatable value of I_d. However, the tests did set an upper limit for I_d at less than or equal to 100 e^-/sec (1.6×10^{-17} A). This indicates that at negligible background, in the absence of ionizing radiation, integrations longer than 80 min should be possible with these arrays. Had the array well capacity been as large as expected, one could then in principle integrate for many hours. As array operating temperature is raised to near the carrier freezeout temperature, I_d increases dramatically due to thermal generation of carriers. Dark current was measured to be about 1000 e^-/sec at 15 K, and excessive dark current renders the array essentially inoperable at temperatures above 18 K.

Frequency Response

The maximum possible sampling rate for these arrays is set by the effective $R_L C_{in}$ time constant associated with the readout circuit. To measure this, a sine wave signal (~100 mV p-p) was injected through the 32 MΩ load resistor. The 3 dB point was determined to be near 1100 Hz for each of the arrays, as noted in table 3. This implies a node capacitance of about 4 pF, spread among the components (FET gate, load resistor, detector array, and wiring) connected at the node.

Array frequency response is strongly dependent on background flux, with higher backgrounds resulting in wider chopped-signal bandwidth. For an 8 ms integration time, the 3 dB point in the frequency response curve lies above 20 Hz with a background flux of 4×10^7 ph/sec; but it drops below 2 Hz when the background is reduced to 2×10^5 ph/sec. The roll-off frequency was found to be constant for varying signal levels at a fixed background flux.

[2] C. M. Parry, Aerojet ElectroSystems Company, private communication.

This dependence would be expected if dielectric relaxation effects limited the device's ability to restore space-charge neutrality. Since the dielectric relaxation time is inversely proportional to conductivity, an increase in photon-generated carrier density should improve frequency response. However, an analysis of an earlier device by C. Parry of Aerojet predicted a dielectric relaxation limited roll-off at frequencies an order of magnitude higher than those observed. No firm conclusion can be drawn at present on the nature of the bandwidth-limiting mechanism, but Parry has proposed a model (ref. 15) based on bulk traps in the array which decrease readout efficiency and frequency response.

Figure 17 shows device response to step transitions in incident flux level. The output signal curves can be fitted with high correlation to exponentials on both rise and fall, with fall times shorter than rise times. The time constant associated with the rise (light-on) transition is much longer than the 10^{-5} sec expected from dielectric relaxation effects. Analysis of the rise characteristic shows that after a step change in illumination, about 10^6 photons strike each pixel before the output signal reaches 63% (1-1/e) of its asymptotic value. Since these photons are essentially lost to the detection system, the bandwidth limiting mechanism constitutes a severe limitation on the usefulness of these arrays for the detection of very faint astronomical objects.

Telescope Observations

One of the arrays (8101, see table 3) was successfully used for IR observations near 4 μm on the 120-in. Shane telescope at Lick Observatory in October 1982 and July 1983. It was mounted in an existing 0.5 m spectrograph to give a plate scale of 1.5 arcsec per pixel and a spectral resolution ($\lambda/\Delta\lambda$) of 1000 (ref. 16). Figure 18 shows a measured spectrum of S Cep. The weak absorption feature near 3.9 μm has previously been associated with CS and C_2H_2 (ref. 17). However, the hoped-for detection of the Brα molecular hydrogen line at 4.05 μm in various sources was not successful due to the low effective quantum efficiency at these short wavelengths.

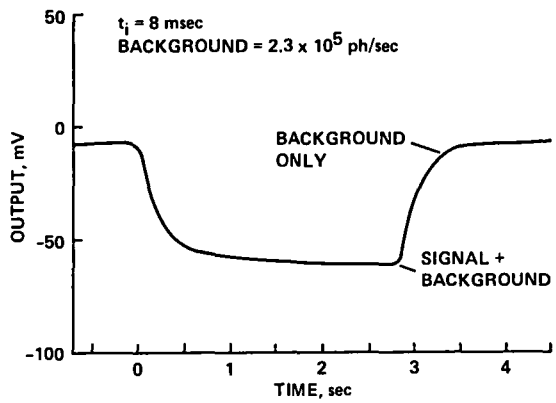


Figure 17.- Device response to step change in illumination.

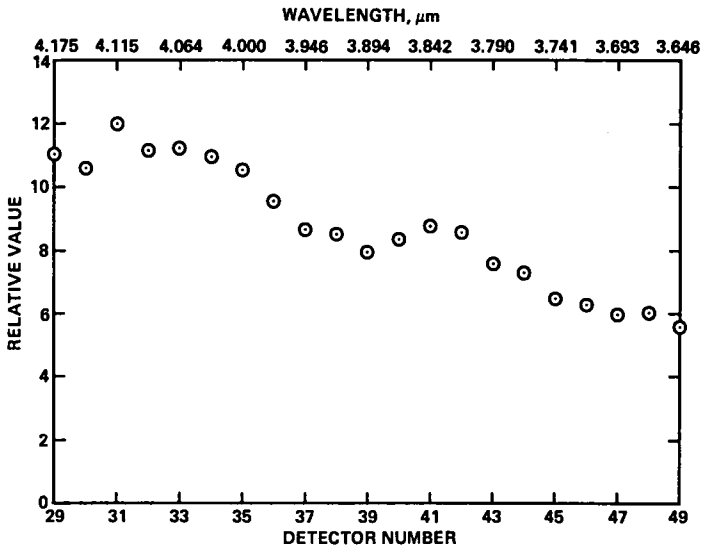


Figure 18.- Array observation of S Cep.

Calibration of the plate scale was accomplished by using the spectrometer grating to disperse a segment of the xenon spectrum over the long dimension of the array. A microcomputer was used to correct for array nonuniformities, and the output of the array after this operation is shown in figure 19. The array was able to reproduce the relative intensities of the measured lines to within 35%, and

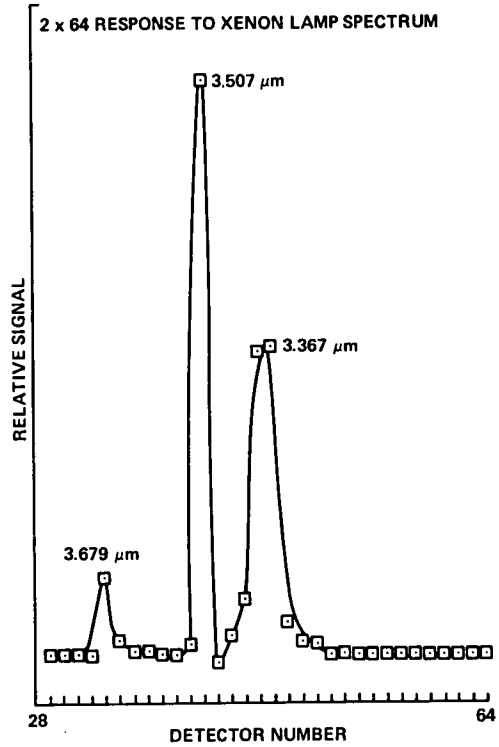


Figure 19.- Array response to xenon spectrum.

from the levels of the pixels to either side of the 3.507 μm line it can be seen that pixel-pixel crosstalk is small.

The small array well capacity and the substantial terrestrial background at longer wavelengths made testing in the array's optimum quantum efficiency range (~11-17 μm) impractical. Nevertheless, good read-noise performance (~160 e^- rms) was achieved on the telescope, and the array performed as reliably on the telescope as it had in the laboratory. The observations proved that reliable, "calibratable" operation was possible with a CID array in a spectrometer application.

DISCUSSION

The 2 × 64 Si:Bi CID arrays have demonstrated a level of performance that establishes the suitability of the technology for certain IR astronomical applications. Laboratory evaluations have shown an average readout noise level below 200 rms electrons, an 11 μm responsive quantum efficiency of 25-30%, and an NEP of 3×10^{-17} $W/\sqrt{Hz}$. This sensitivity compares well with that reported for good nonintegrating discrete detectors under low background at these wavelengths.

While an ideal array would be much more uniform than these prototype devices, the demonstrated level of nonuniformity could be accommodated in data post-processing with little difficulty. Also, the extremely low level of measured dark current (<100 e^-/sec) indicates that these devices are well-suited to extended-integration-time, staring-mode operation.

Telescope demonstrations were performed which showed that the ease of operation of the array does not differ between the laboratory and an actual IR observation. However, if the power and sensitivity of the device is to be fully realized in this type of application, it will be necessary to obtain a well capacity large enough to accommodate ground-based telescope background levels between about 10 μm and 18 μm. This presumes an effective quantum efficiency equivalent to the levels measured in the laboratory under low background.

It is interesting to compare the performance of these 2 × 64 arrays with that of a similar 1 × 32 CID tested earlier (refs. 12 and 18). General performance characteristics are similar between these two generations of CIDs, but some significant differences are apparent. Major detector performance parameters (responsivity, quantum efficiency, frequency response, and optimum operating temperature) are essentially the same for the two array types. However, the small well capacity observed in the 2 × 64 arrays was not apparent in the 1 × 32 array, and the optimum store voltages (about +4 V for the 1 × 32) also differed significantly. This suggests that small well capacity is not a fundamental limitation on CID technology. Other observed differences favor the 2 × 64. The 150 rms e^- read noise of the 2 × 64 is significantly lower than the 670 rms e^- measured on the 1 × 32. The best 2 × 64 pixel-pixel uniformity also represents an improvement over that displayed by the 1 × 32.

Despite the demonstrated capabilities of AMCID arrays, they also possess a number of weaknesses. Bulk-trapping limitations (ref. 16) in the CID require that a significant number ($\sim 10^6$) of photons be absorbed before full signal levels are reached. For measuring faint signals under exceedingly low background conditions, this would clearly be an unacceptable limitation. In addition, CID response (i.e., responsivity, frequency response) has been shown to be strongly background-dependent (ref. 15), which significantly complicates the calibration process. Particularly for ground-based 10 μm applications, the limited well capacity of these arrays forces the use of high readout rates and correspondingly fast and complex digital data systems.

A final consideration regards the producibility of the devices. It proved difficult during the course of the contract to produce high-integrity, pinhole-free oxide layers and short-free guard ring and gate structures over the relatively large areas of semiconductor material involved. It took about twice as long as expected (24 months vs. 12 months) to produce three deliverable devices.

Because of these limitations, the current development trend is toward switched-FET integrated arrays (refs. 8 and 19) which promise to provide the favorable quantum efficiency and read noise performance of CIDs without their irregular effects and low yields.

Despite the inherent limitations of CID arrays, the laboratory evaluation program and astronomical observing project provided valuable experience on integrated array characteristics and operational requirements. While it appears unlikely that CID arrays will be incorporated in flight instrumentation for SIRTF, the arrays provided notably good performance and valuable experience for the continuing evolution of IR arrays for space astronomical applications.

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16. Abstract

Three 2 × 64 element charge-injection-device infrared detector arrays were tested at low and moderate background to evaluate their usefulness for space-based astronomical observations. Testing was conducted both in the laboratory and in ground-based telescope observations. The devices showed an average readout noise level below 200 equivalent electrons, a peak responsivity of 4 A/W, and a noise equivalent power of 3×10^{-17} W/$\sqrt{\text{Hz}}$. Array well capacity was measured to be significantly smaller than predicted. The measured sensitivity, which compares well with that of nonintegrating discrete extrinsic silicon photoconductors, shows these arrays to be useful for certain astronomical observations. However, the measured readout efficiency and frequency response represent serious limitations in low-background applications.

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