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(NASA-CR-175859) COMMUNICATIONS AND LOGIC SYSTEMS AT MILLIMETER WAVE FREQUENCIES Final Report (Howard Univ.) 104 p HC A06/MF A01 CSCL 20L G3/76
N85-28824 THRU N85-28827 Unclas 23470

COMMUNICATIONS AND LOGIC SYSTEMS

AT

MILLIMETER WAVE FREQUENCIES

GRANT NO. NAG 5-246

FINAL REPORT

SEPTEMBER 1983

SUBMITTED TO

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

GREENBELT SPACE FLIGHT CENTER

HOWARD UNIVERSITY
SOLID-STATE ELECTRONICS GROUP
ELECTRICAL ENGINEERING
WASHINGTON, D.C. 20059

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N85-28825

Summary

During the contract period we have constructed an $AsCl_3$ epitaxial system used to provide buffer layers for our FET structures, we have developed a submicron lithographic processes using deep U.V. techniques and, employing these techniques we have produced working .5 micron gate devices. In addition, we have continued our developing of submicron mixer diodes. In addition, we have investigated the "gettering" of substrates as a technique to improve the mobility of ion implantated layers. The result of this experiment showed was a correlation between improved hall mobilities and gettered substrates. Finally, several theorectical studies are reported.

Materials Development

In section A, we will report on the progress in development of a $AsCl_3$ system for the production of high quality buffer & active layers for our microwave devices. It is anticipated that the $AsCl_3$ material will provide thick buffer layers for isolating the substrate effects while growth technologies such as MBE will provide the thin critical active regions. Part B of this section concentrates on our gettering experiments on GaAs substrates for direct ion implantation applications while, part C reports on the status and capabilities of our recently acquired MBE system.

A

Project Status of CVD Reactor

Introduction

We report here the status of our redesigned halide transport VPE reactor and results obtained to date. This effort parallels construction of a pyrolytic CVD reactor now completed.

As previously mentioned, GaAs FET performance shows a great dependence on submicron doping thicking products, backround impurities and substrate properties. The system is designed to grow thick (greater than 10 micron) high-resistivity buffer layers which isolates our FET devices from substrate related problems.

The achievement of high resistivity buffer layers has been well demonstrated in the literature to require use of the well known "mole fraction effect" first described by Dilorenzo and Moore in 1971. A two bubbler systems similar to that of Cox and Dilorenzo (1971) is adapted, but with certain changes and simplifications.

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VPE System Technology

A systematic outline of our system as originally designed is shown in figure (1). It was at first intended to demonstrate high-purity and reasonable process control with a simple reactor design. Systems improvements were later added as they proved necessary.

The original design was a teflon plumbing system using a continuous hydrogen purge to avoid adding reactor bypass valves as a possible source of contamination. The use of teflon is intended to minimize the presence of any metallic impurities, as well as decrease the "memory effect" of any system reagents. This teflon plumbing and buffer valves still seem to be a useful system feature and were retained in use.

The first growths utilized $AsCl_3$ obtained in prepackaged plug-in bubblers from Apache Chemicals, Inc. These $AsCl_3$ bubblers were designed to plug into solid-state temperature controllers also manufactured by Apache chemicals, Inc. This was deemed to be a valuable feature which would minimize toxic hazards associated with loading the CVD system with $AsCl_3$. We

experienced many hardware problems with these temperature controllers. After being sent several updated versions, we have only this year obtained models which work as prescribed.

To check the reactor kinetics 45 grams of liquid Gallium as source material was loaded. We then attempted source saturation at 820°C and observed the saturation time and other characteristics. We found it necessary to add a source baffle to increase source saturation efficiency. Growth parameters of liquid source runs 3 thru 6 are shown in Table I.

The source boat was later loaded with approximately 40 grams of crushed GaAs as a solid phase source. Solid sources have been found to offer better thickness control, without the troublesome source saturation/etch cycle of liquid sources. Better surface morphology is also observed.

Initially we used as source material the upper "cone" portion of Bridgeman process semi-insulating GaAs crystals provided by Cominco, Inc. This solid source material was used in growths under a variety of reactor temperatures, carrier gas flows, and bubbler temperatures shown in Table I, runs 7 thru 21. Over certain parameter ranges good morphology and thickness control were obtained. Certain growth and hardware problems were encountered which w. attacked with several design changes.

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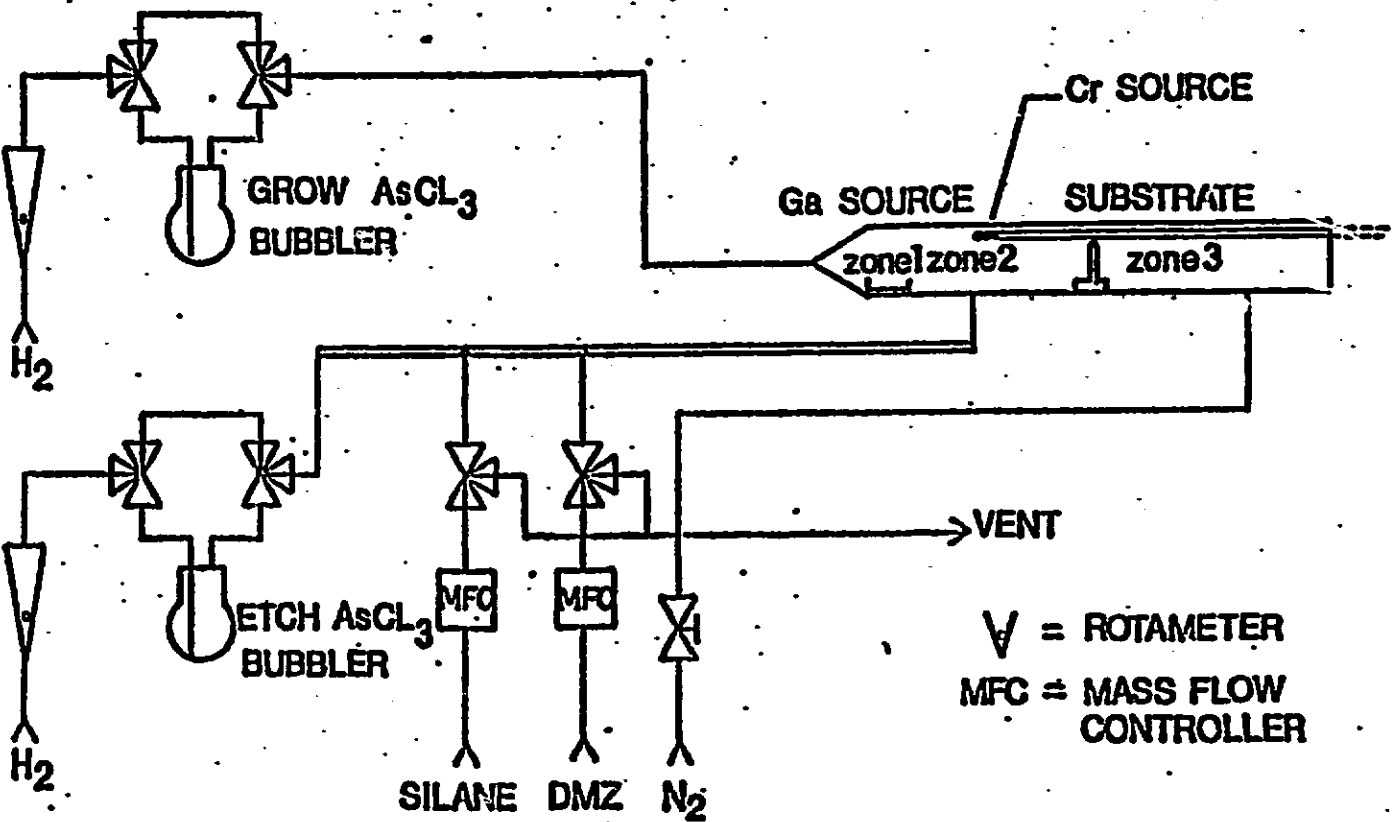

Figure 1

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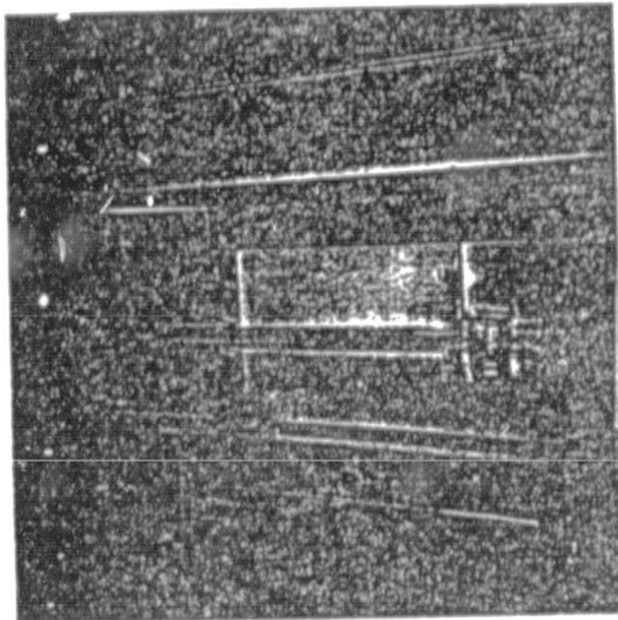

Figure 2

We decided to reduce the normal buildup of reaction by products at the exit end of the reactor tube by use of a hydrogen counterflow system. This build up could produce particle contamination. Several endcap designs were tried in which the substrate holder, dump tube and endcap were fuzed into one quartz containment assembly as shown in figure (2). The solid-source was changed to sealed-vessel synthesized GaAs dices supplied by Morgan Semiconductor for the runs remaining runs after run #20. This high purity source material gave only a superficial improvement in the electrical characteristics. Subsequently we were able to eliminate the solid source as a cause of the extrinsic compensation since no source, temperature or other growth parameter dependence was observed.

While at this point the faulty temperature controllers were still being used, it was suspected that the $AsCl_3$ itself was contaminated and causing the epilayers to become heavily compensated.

The $AsCl_3$ was returned in the plug-in bubblers to the manufacturer for analysis. Flame spectrochemical analysis revealed approximately 50ppm Fe, 20ppm Si and a few ppm traces of Mg and other elements. The source Fe levels are very consistent with the electrical characteristics observed in the epilayers.

Fe backrounds generally in the 10^{-8} mole fraction range will yield high resistivity layers with mobilities of approximately 1000-2000 $cm^2 V^{-1} Sec^{-1}$. We tentatively concluded, therefore, that our low mobilities and high resistivities were caused by unintentional incorporation of bubbler Fe due to contaminated $AsCl_3$.

System Modifications

To alleviate the above difficulties we have made changes in our source materials and process. The most important of these by far is the use of good quality $AsCl_3$ obtained from other domestic manufacturers.[4] We will fill our plug-in bubblers with the pure $AsCl_3$ demonstrated in the field as having the requisite purity.[5] This change alone is expected to solve most of the compensation problem.

The reactor tube itself has been modified extensively. At the inlet side a vacuum chamber thermally isolates the inlet tubes from the source region. This aids greatly in reducing any premature thermal decomposition of main or bypass injection line reagents. As already shown in figure (2), the substrate holder, dump tube and endcap were fuzed into one assembly for maximum leakage integrity. Not shown is the new flat O-ring joints which

Run No.	Sample No.	F_M (cc/M)	F_B (cc/M)	Pannel P (PSI)	Counter Flow F_C (cc/M)	Source	T_M (°C)	T_B (°C)	Prebake time (min)	Etch time (min) τ_E	Growth time (min) τ_G	Thickness d μm	Growth rate R_g μm/min	Source Temp T_S	Sub Tem T_D	Break down Voltage (V) V_B	Mobility $\mu_{77°K}$	Mobility μ_{300}	N_{300}	
3	T_1	330/15	100/15	Ga	max at 15		20	10	30	19	15	18	1.2	820	760	10	-	-	-	No morphplogy picture,thickness is questionable
4	T_5	"	330/15	"	"		19.4	18.6	"	"	"	3	0.2	"	"	N/O	-	-	-	N/o = No breakdown observed
5	T_6	"	"	"	"		19.3	10	"	17	"			"	"	400		-	-	Pyramid Growth Hall sample was not effected by the magnetic field
6	T_7	"	"	"	"		19	10	"	19	"	N/o	-	"	"	N/o	-	-		
7	T_8	"	"	solid	"			15	"	2	60	4		"	"	"	-			fair morphology, slow growth rate
8	T_9	420	"	"	"		"	"	"	"	90	no growth	-	"	"	-	-	-		
9	T_{10}	280	"	"	"		"	"	"	"	"	‹		"	"	-	-	-		
10	T_{11}	"	"	"	"		15	"	"	"	90	15		"	"	25				morphology bad, hall sample were not ohmic
11	T_{12}	330	330	"	"		20	14	45	11	60	"		"	"		-	-		poor morphology
12	T_{15}	"	400	"	"		20	15	"	"	"	14-20		830	745	50				hillocks growth, black non uniform growth
13	T_{16}	"	"	"	"		"	"	"	5	"	14		830	740	100				fairly clean surface except for black spots which could be due to etch, uniform growth

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Run No.	Sample No.	F_M (cc/M)	F_B (cc/M)	Source	Counter Flow F_C	Pannel P PSI	T_M °C	T_B °C	Prebake time (min)	Etch time (min) τ_e	Growth time (min) τ_G	Thickness d µm	Growth rate R_g µm/min	Source Temp T_S	Sub Temp T_D	Breakdown Voltage (V) V_B	Mobility µ77°K	M300	N300	
14	T_{20}	330	330	solid	max at15	one	20	15	60	10	60	7.5–10		830	710	70	-	-	-	poor morphology compared to T_{15} black spots got more non uniform growth
15	T_{23}	"	"	"	"	both	"	"	"	5	"	12		"	725	100				fairly clean surface, some part looks peeling off uniform growth
16	T_{24}	"	"	"	"	"	"	"	"	"	"	17.5		"	730	30	-	-	-	change of the solid source surface morphology improved, has black spots uniform growth
17	T_{25}	$\frac{330}{15}$	$\frac{400}{15}$	GaAs	max at15 psi		"	"	"	"	55	12		"	"	32-110				poor morphology, blackspots uniform growth
18	T_{17}	"	"	"	"		"	13	"	2	60	8		"	"	24-66				poor morphology worse than T_{25}, high density of black spots. Uniform growth
19	T_{26}	"	330	"	"		"	15	"	"	"	9		830	"	22-120				" "
20	T_{21}	"	"	"	"		"	"	"	"	"			"	"					layer is bad did not look at morphology & thickness
21	T_{28}	"	"	"	"		"	"	"	"	"	12.5		"	"	24				good morphology, uniform growth double layer feature
22	T_{29}	"	"	"	"		18	"	"	"	"	10		"	"	30-60				good surface, uniform growth no double layer feature
23	T_{30}	"	"	"	"		16	"	"	"	"	11		"	"	20-120				part of the layer is foggy, dumptube were saturate with deposit around sub area uniform growth
24	T_{35}	"	"	"	$\frac{188}{20}$		16	"	"	"	"	10		"	"	5-12				partly foggy, uniform growth hillocks growth

No.	ple No.		(cc/M)	rce	unter flow F_C	nel P	°C	°C	bake time (n)	ch time (n) τ_E	wth time (n) τ_G	ickness d	wth rate R_g	rce Temp T_S	Temp T_D	akdown tage (V) V_B	$\mu_{77°K}$	N_{300}	
24	T_{31}	$\frac{330}{15}$	330	GaAs	$\frac{188}{20}$		16	15	60	2	60	9		830	730	5-100			partly foggy, uniform growth, hillocks growth
25	T_{32}	.	.	.	$\frac{186}{20}$		15	.	.	.	.	10		.	.	10-180			lower part is cleaner, back dots in the uppor port good morphology, uniform growth
25	T_{33}	.	.	.	.		.	.	.	.	.	10		.	.	60-190			. .
26	T_{34}-2	.	.	.	$\frac{183}{20}$		.	.	.	.	120	27.5		.	.	30-60			good morphology
27	C_1-1	.	.	.	$\frac{184}{20}$		.	.	.	.	.	19		.	.	26-65			hillocks growth, uniform growth 15 black spots
28	C_2-2	.	.	.	$\frac{185}{20}$		12	.	.	.	90	14.5		.	.	42-100	1277,1823	$N_{300}=1.2\times10^{17}$	. .
29	M_1-3	.	$\frac{330}{15}$	solid GaAs	$\frac{185}{20}$		10	.	.	.	.	12.5		.	.	4-10			morphology is very good; no hillocks or pyramid uniform growth, bad crystal quality
30	T_{28}-4	.	.	.	$\frac{180}{20}$		15	.	.	30	-	detch= all		.	.	-			poor morphology, all the layer etched
31	M_1-5	.	.	.	.		.	10	.	20	-	detch ~9		.	.	-			poor morphology 9.5 detch 10 at same part mostly the layer we attached

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Run No.	Sample No.	F_M (cc/M)	F_B (cc/M)	Source	Counter flow F_C	Pannel P PSI	T_M °C	T_B °C	Prebake time (min)	Etch time (min)	Growth time (min)	Thickness d (μm)	Growth rate R_g μm/min	Source Temp T_S	Sub Temp T_D	Breakdown Voltage (Y) V_B	Mobility $\mu_{77°K}$ μ_{300}	N_{300}	
32	M_{1-6}	320	290	solid GaAs	185/20		15	10	60	15	--	d_{etch} ~9.5		830	730	4-10			poor morphology, etch=9.5 μm non uniform etch
33	T_{35-7}	330	270	"	183/20		"	"	"	10	-	no uniform etch		"	"	-			Morphology improved compare to M_{1-6} but not over all layer, non uniform etch
34	T_{29-8}	"	250	"	182/20		"	"	"	30	-	$d_e > 9$							morphology improved more, non uniform etch
35	T_{33-9}	325	210	"	181/20		"	"	"	15	-	d_e ~ 8.5		"	"	-			good morphology, not uniform regrowth
36	T_{32-10}	335	220	"	"		"	"	"	"	-	d_e ~ 6.5		"	"	20-70			good morphology, uniform etch, regrowth
37	M_{2-11}	330	"	"	180/20		"	"	"	"	90	12.5		"	"	60			good morphology; uniform growth
38	M_{3-12}	"	220	"	182.5/20	both	15	10	"	"	120	13		"	"	-			"
39	M_{4-13}	"	220	"	181/20	"	"	"	"	"	"	no growth		"	"	-			increasing F_B after etch from 22[illegible] cc/M to 580cc/M, no growth, some etch
40	M_{5-14}	"	"	"	181/20	"	"	"	"	"	90	2-4		"	"				F_B was increased to 480 cc/M right after etch, non uniform, at some part no growth
41	M_{7-1}	"	"	"	182/20	"	0	10	"	"	120								

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will replace the taper joints used so far.

Up until now rotameters were used for main and bypass hydrogen gas metering in an initial attempt to keep costs low. These have been replaced by electronic mass flow controllers which will give superior accuracy.

The original plan to use Fe or Cr solid-phase doping for the high resistivity buffer layer has been scrapped in favor of more promising methods. Combinations of the mole fraction effect and addition of oxygen during growth have been observed to suppress incorporation of backround impurities [6,7]. This oxygen gettering occurs without the memory effect caused by contamination of the tube when heavy metals are introduced as hi-resistivity dopants. There is also evidence of deep oxygen donors further serving to reduce the free carrier concentration. We will study other methods of introducing oxygen into the system, e.g., using CO_2 gas, without adversely affecting the mobility of the epitaxial active layers.

Summary

We conclude from the studies completed thus far that the more conventional designs for $AsCl_3$, which our redesigned system more closely resembles, are best used for the growth of high purity GaAs buffer and active layers in conjunction with "clean" gettering techniques such as oxygen injection. Various oxygen compounds such as CO_2 and CO will allow better oxygen incorporation and at the same time introduce small quantities of deep carbon acceptons to more adequately compensate shallow Si donor and other acceptor levels. The mole fraction effect shows great promise in further dopant suppression when used in conjunction with the oxygen incorporation.

With this considerations taken into account we believe this modified approach is a much more fruitful method to reliably produce hi-quality epitaxial GaAs.

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B Ion Implantation

Semi-insulating gallium arsenide grown by liquid encapsuled Czochralski (LEC) method has been plagued by a number of problems. For example, heating LEC substrates at typical annealing and growth temperatures (700-900°C) frequently proceduces a highly conductive thin layer near the surface. This phenomenon is usually accompanied by poor reproducibility of carrier concertrations, low mobilities, and photoluminescence changes. We have began to study this and other problems related to GaAs substrates for direct ion implantation applications. A simple "gettering" technique that employs heat-treatments at 300° for 24 hours in flowing H_2 with an overpressure of As provided by InAs was used. An outline of our gettering experimental procedure is provided in table #2 on page 15 of this report.

Routine hall measurements were taken at room temparature and 77°K. The hall samples employed the standard Van der Pauw technique with clover-leaf shaped samples. Contacts to the specimen are made with tin beads alloyed to the leaves, which in turn provide edge contacts to the central part of the sample. For our purposes, the carrier concentration and the mobility are

particulary important values, and can be obtained from these measurements.

The heat treated or "gettered" implanted and annealed layers typically showed a higher room temperature and 77°K mobility. The improvement in mobility varies from wafer to wafer and is shown in the figures (3a) and (3b) of mobility vs substrate or boule number. For instance, Q9 showed at 35% improvement while Q11 showed no improvement. The wide range of data reveals the large differences in the substrate properties, residual impurities, and trap concentrations.

Standard photoluminescence spectra were also obtained for both the gettered and ungettered layers. The PL. was performed at 7°K using a Argon layer at a power level less than 100mw. The luminescence radiation was dispersed by a 3/4 meter grating monochromator and detected with a LN_2 cooled photomultiplier using phase-sensitive detection. The resulting PL spectra of the gettered samples exhibited a reduction in the Mn and Cu peak intensities. This result is illustrated in the PL spectrum of Q8 and Q4 (figure 4).

SIMS analysis experiments were performed on ungettered and gettered samples at Cornell University. The SIMS analysis

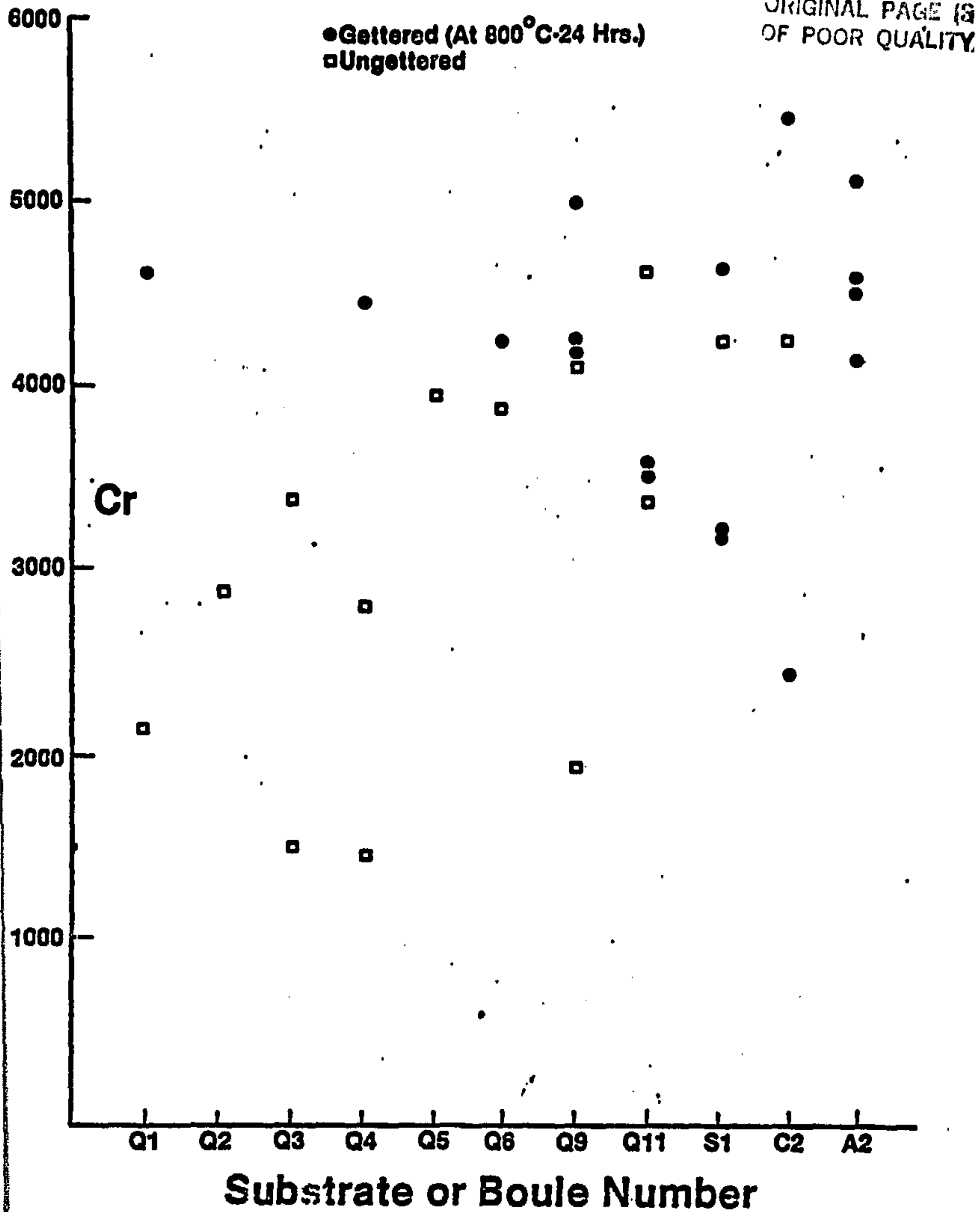

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Figure 3a

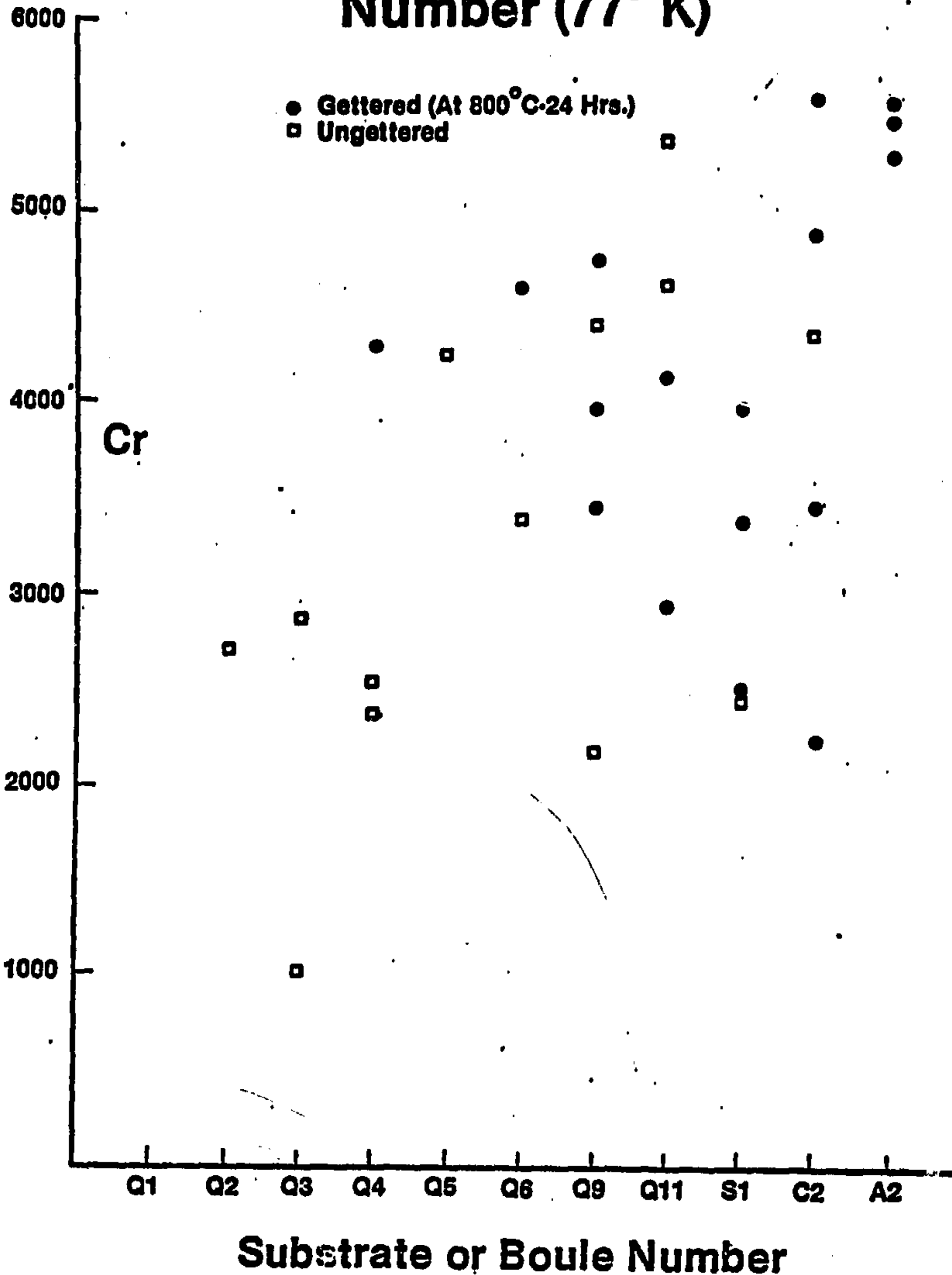

Figure 3b

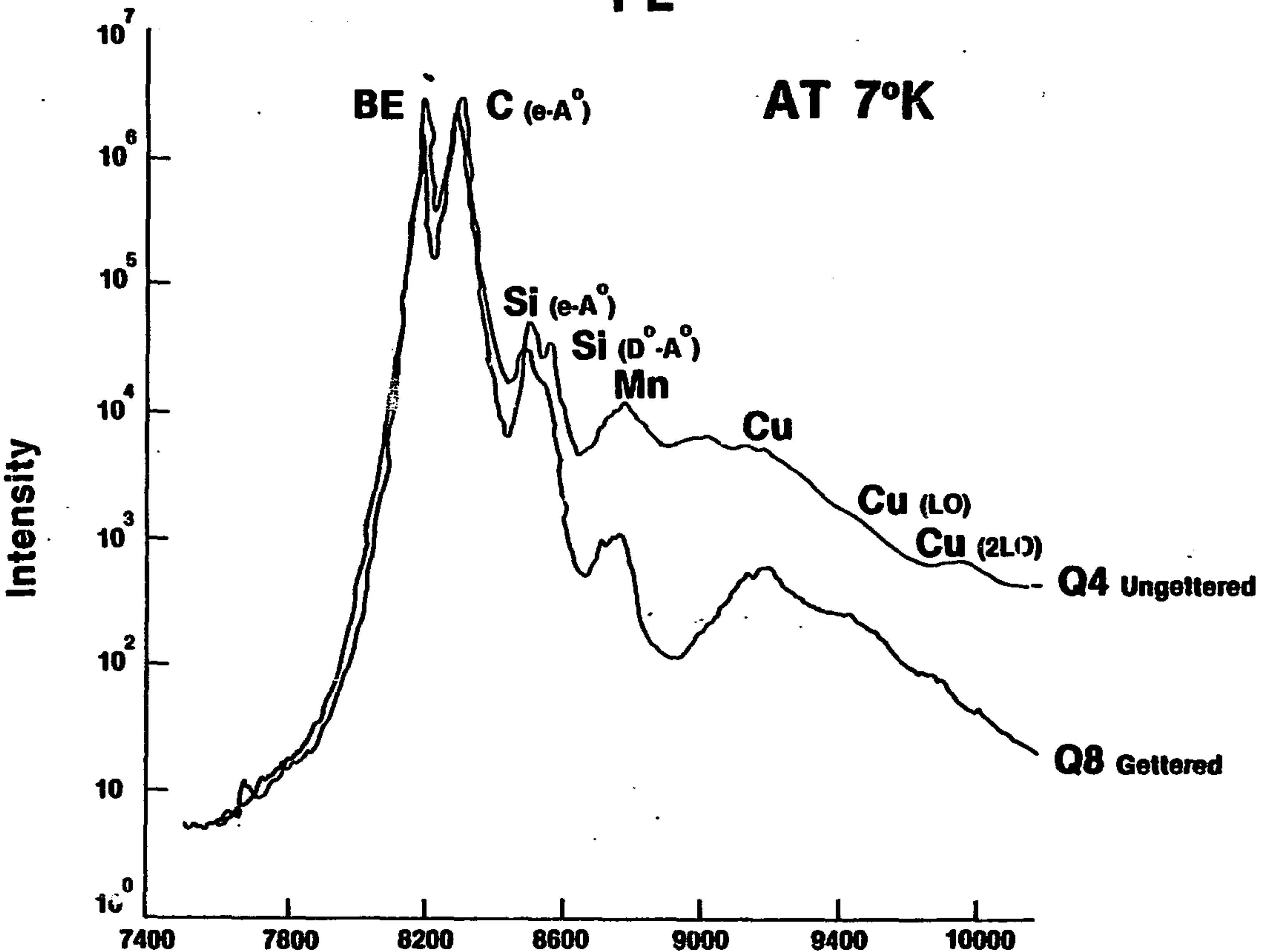

Figure 4

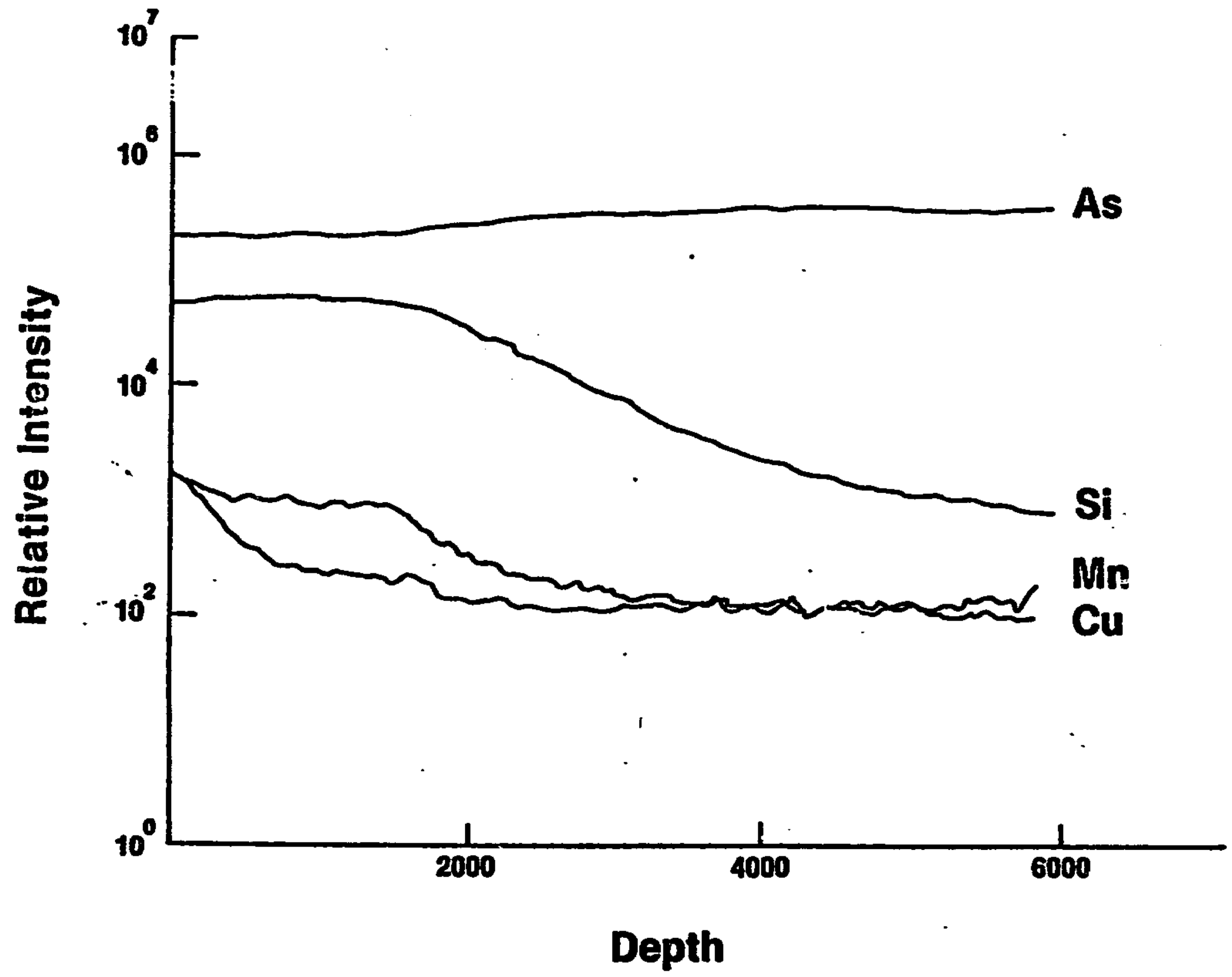

Figure 5

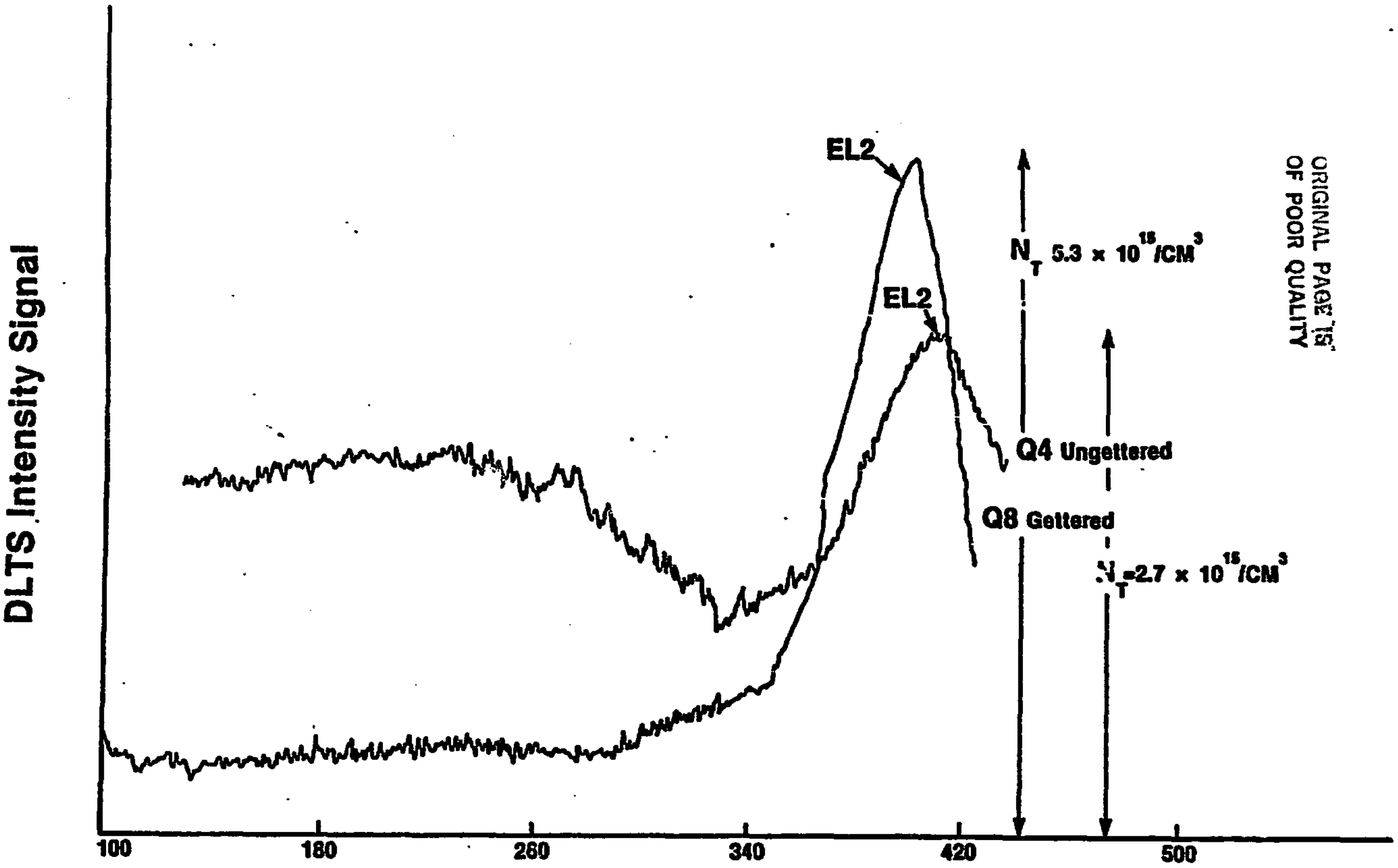

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Figure 6

revealed the presence of several residual impurities. These impurities : Carbon, chromium, boron, managanse, copper and magnesium were clearly present in the 10^{14} - 10^{15} range. In addition, we observed outdiffusion for the substrate of copper, managenese, and magnesium. These results are shown in figure (5).

Electrically DLTS results figure (6) on schottky barriers diodes formed on the gettered and ungettered layers reveals an increase in the EL2 level and a reduction in the broad shallow peak. We believe that this broad peak is related to the presence of several residual impurities.

In summary, we have concluded from the studies completed that LEC substrates can be improved by heat treating. There are,however, a couple of precautions: 1) It is necessary to remove all of the gettered layer and, 2) provide an sufficent overpressure of As. This work was presented at the Electronic Materials Conference held at Santa Barbara.

GETTERING EXPERIMENTAL PROCEDURE TABLE #2

POLISH SUBSTRATES

DIVIDE POLISHED SUBSTRATES INTO HALVES

BAKE ONE HALF OF THE SUBSTRATES AT

800° FOR 24 HOURS

POLISH BOTH SIDES OF THE GETTERED SUBSTRATES

(REMOVE 35 mm)

STANDARD CLEAN

IMPLANT

S_i^{29}	6.09×10^{11}	40 KV
	9.03×10^{11}	110 KV
	4.5×10^{12}	200 KV

ANNEAL AT 800°C FOR 30 MINUTES IN A CAPLESS ANNEALING SYSTEM WITH

FLOWING H_2

COMPARE ELECTRICAL PROPERTIES

C Molecular Beam Epitaxy

We have a acquired and installed a MBE system. We anticipate that this system will be used to grow the critical layers for our FET structure. With MBE capabilities it will be possible to investigate normal GaAs FET's as well as the high electron mobility structures (HEMPT). We anticipate that we will be growing both single as well as multiple interface HEMPT devices. Our machine has the capability of growing on 2 inch substrates and we can load up to six wafers in a single pump down. We are presently baking out the furnaces in preparation for our first growth.

Lithography

One of our principal problems during this work has been the development of our lithographic techniques. This section will summarize our efforts.

At the beginning of the contract a FET mask set and a test pattern were fabricated at the National Submicron Center located at Cornell University. The best results were obtained using a wet chemical etch. The smallest resolved features of the masks have linewidths of better than 0.25 microns. We then went through a period of considerable experimentation with the exposure and development parameters. Our final process consists of a two layer photoresist technique utilizing a co-polymer of PMMA and PMAA. The PMMA was used as the imaging resist and develops more slowly, the co-polymer was used to form a lift off lip similar to that shown in figure (7). Our final process is summarized in Table III. Examples of our better gate lift off are shown in figures (8),(9) and (10).

The key element that we found necessary to reproduceably form .5 micron lines was to obtain "good" coformal contact between the mask and the GaAs substrate. In order to ascertain

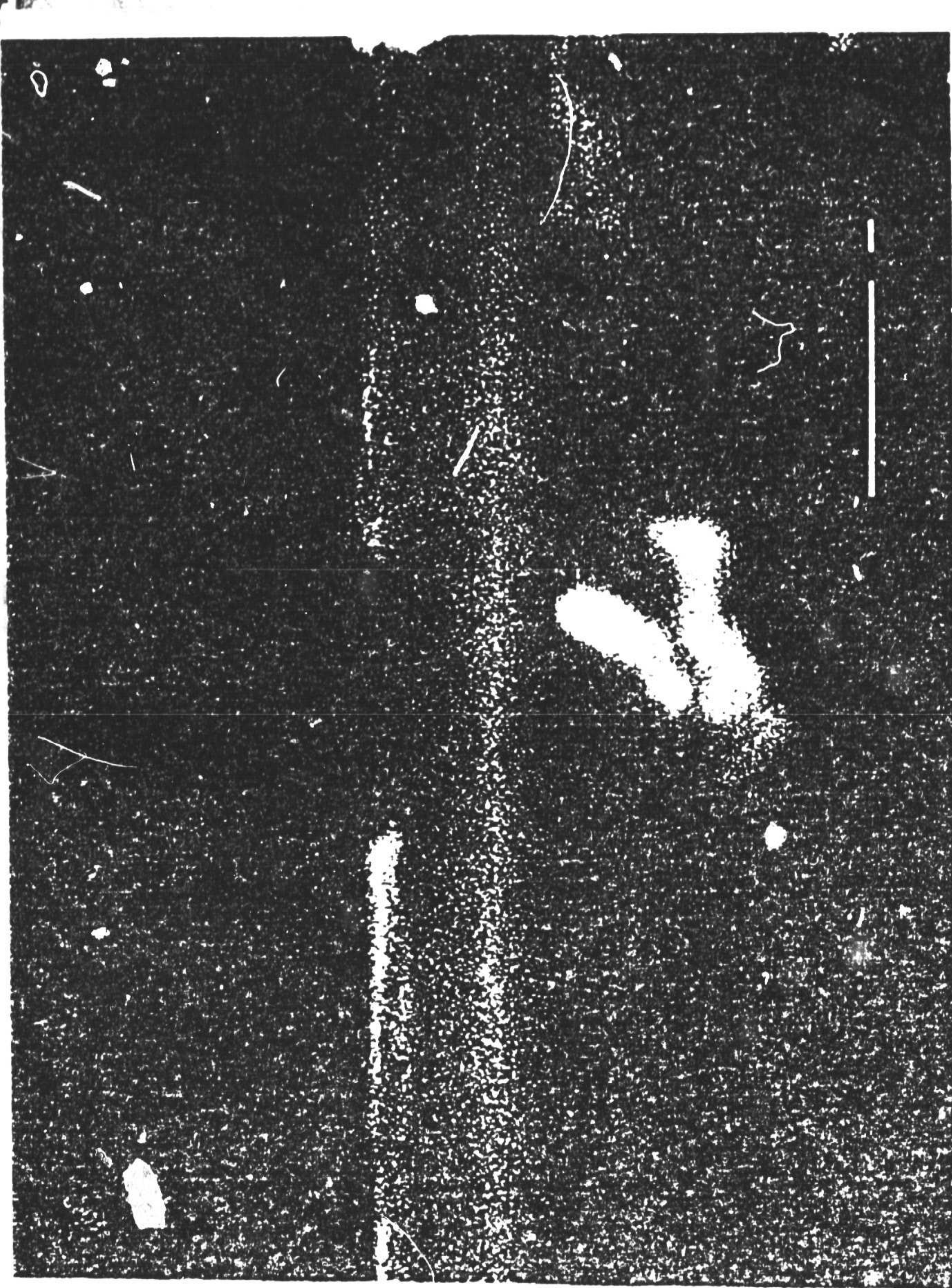

Figure 7
Calibration mark is one micron

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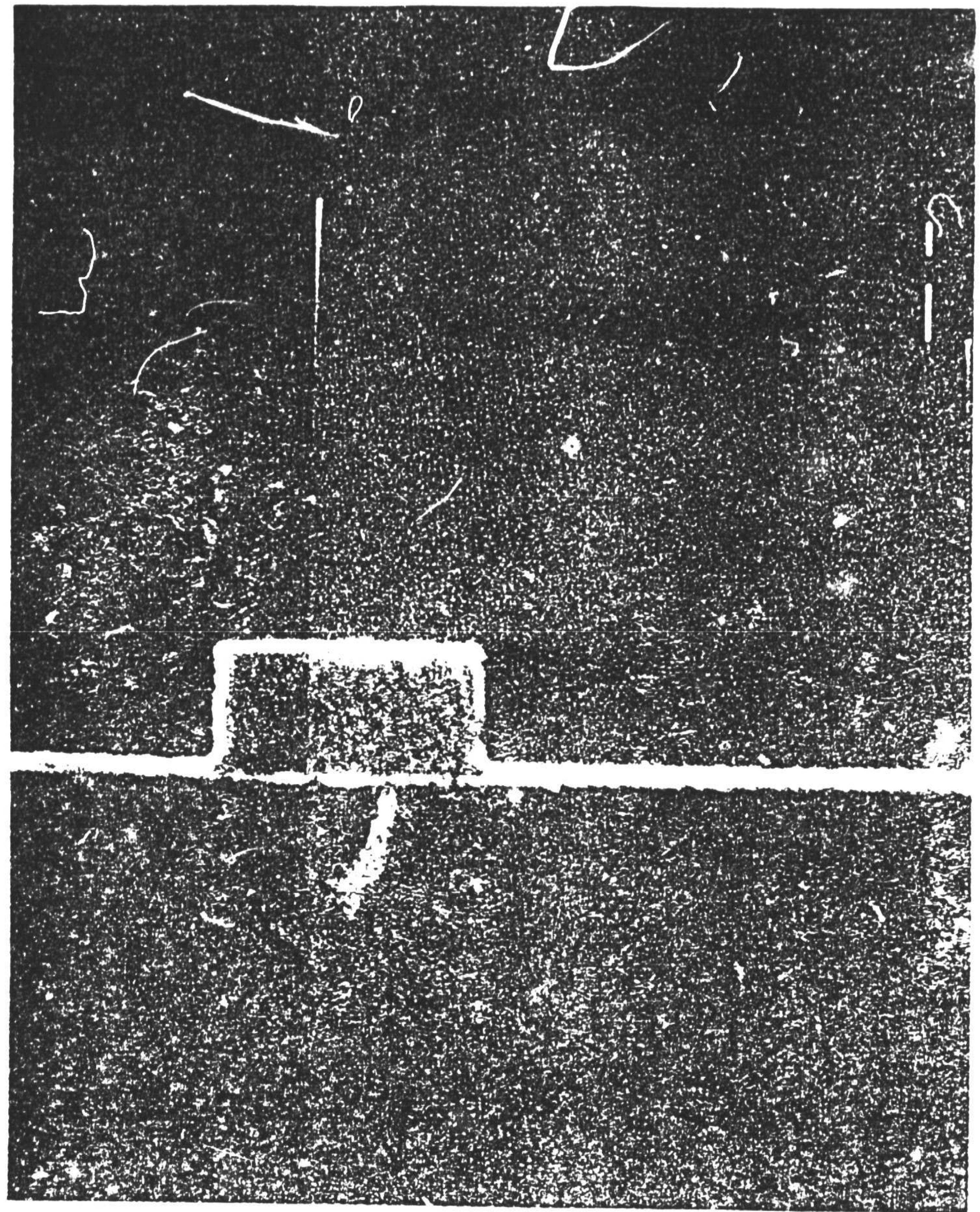


Figure 8
Calibration mark is one micron

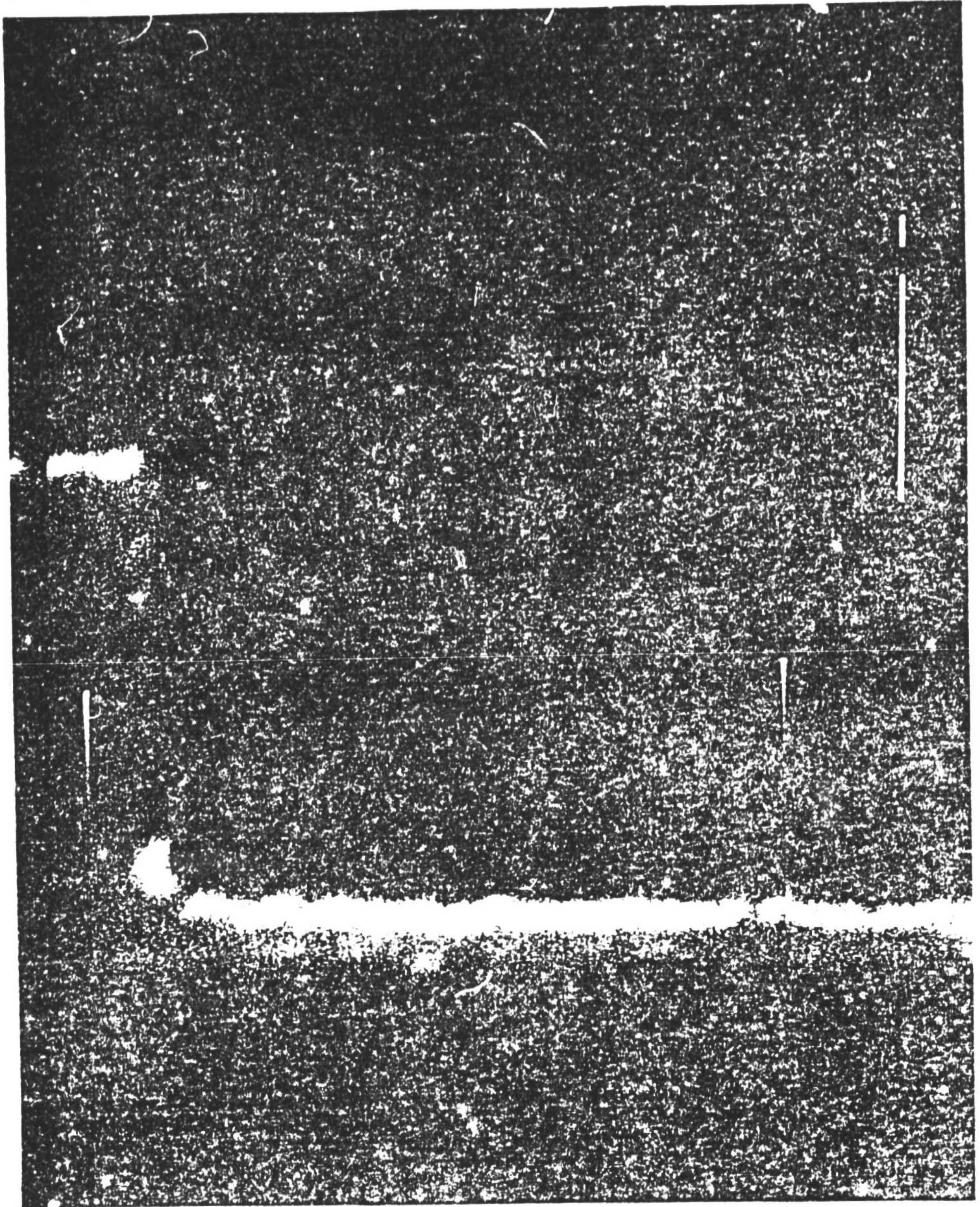


Figure 9
Calibration mark is one micron

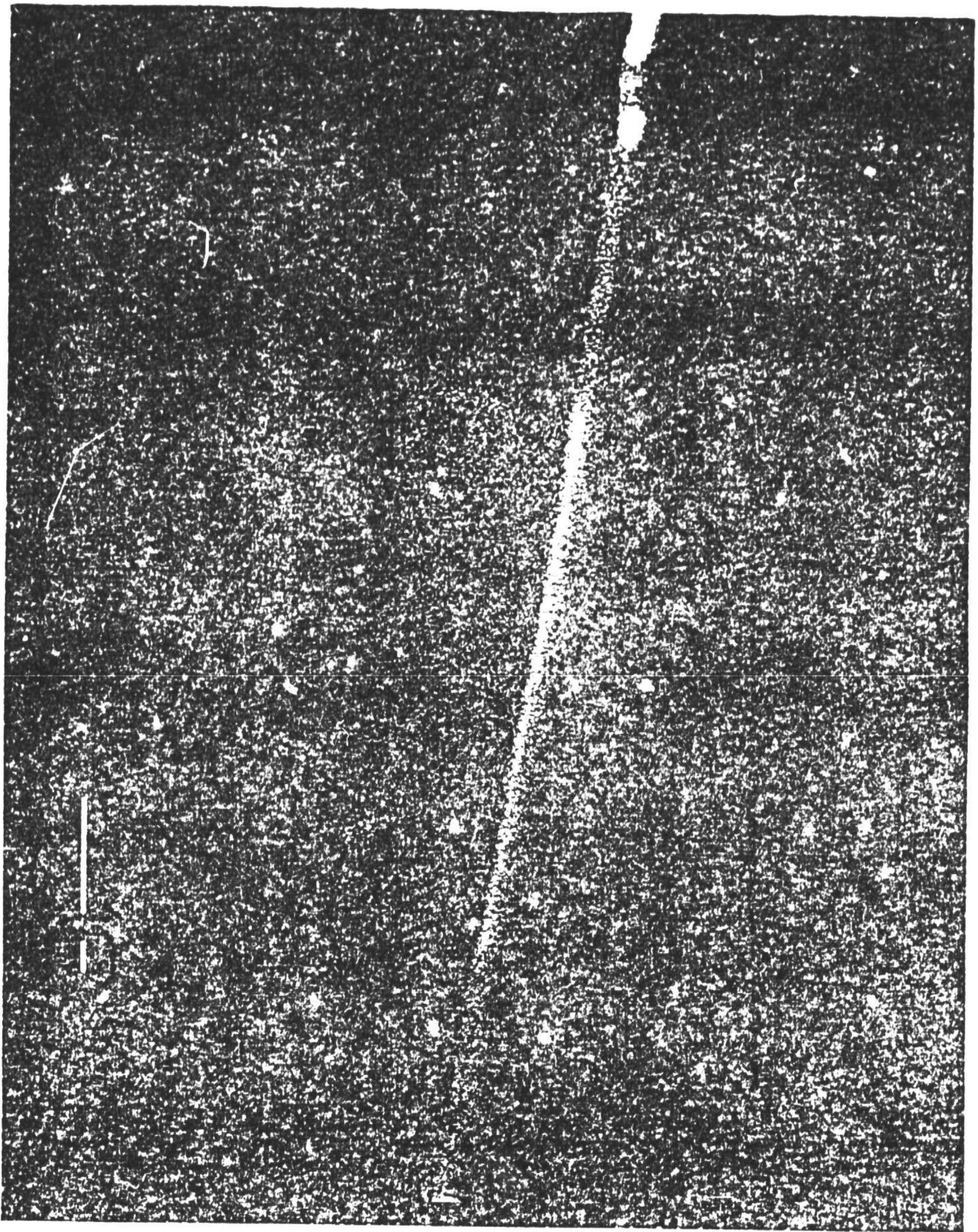


Figure 10
Calibration mark is one micron

whether we are had contact a quartz plate was used. The substrate was observed through a quartz plate the same size as the mask. Figure (1) is representative of the type of contact we were able to obtain. On the areas where no fringes formed we observed a darken region which were the areas where we obtained good contact. We found excellent correlation between these contact areas and production of high quality lines. As indicated in Table III one of the process steps is dissolving the resist by using a O_2 plasma. For this process we have calibrated the etch rate in a barrel plasma reactor and this is illustrated in figure (12).

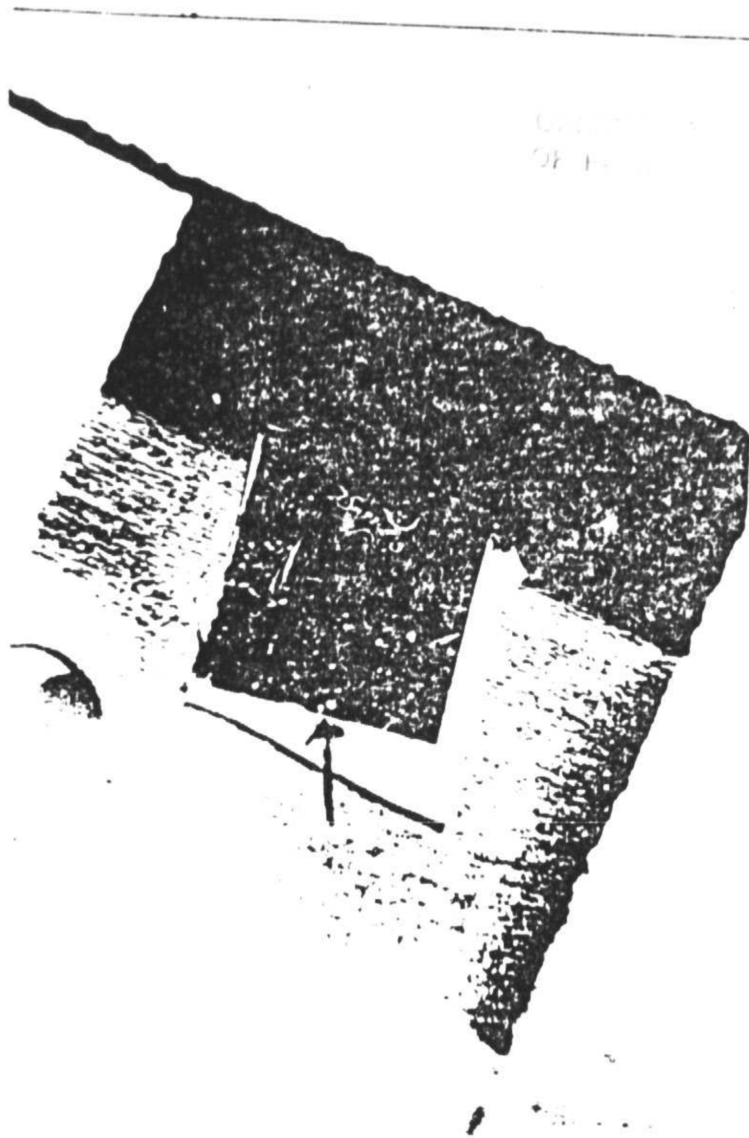


Figure 11

Arrow shows boundary between regions of different contact

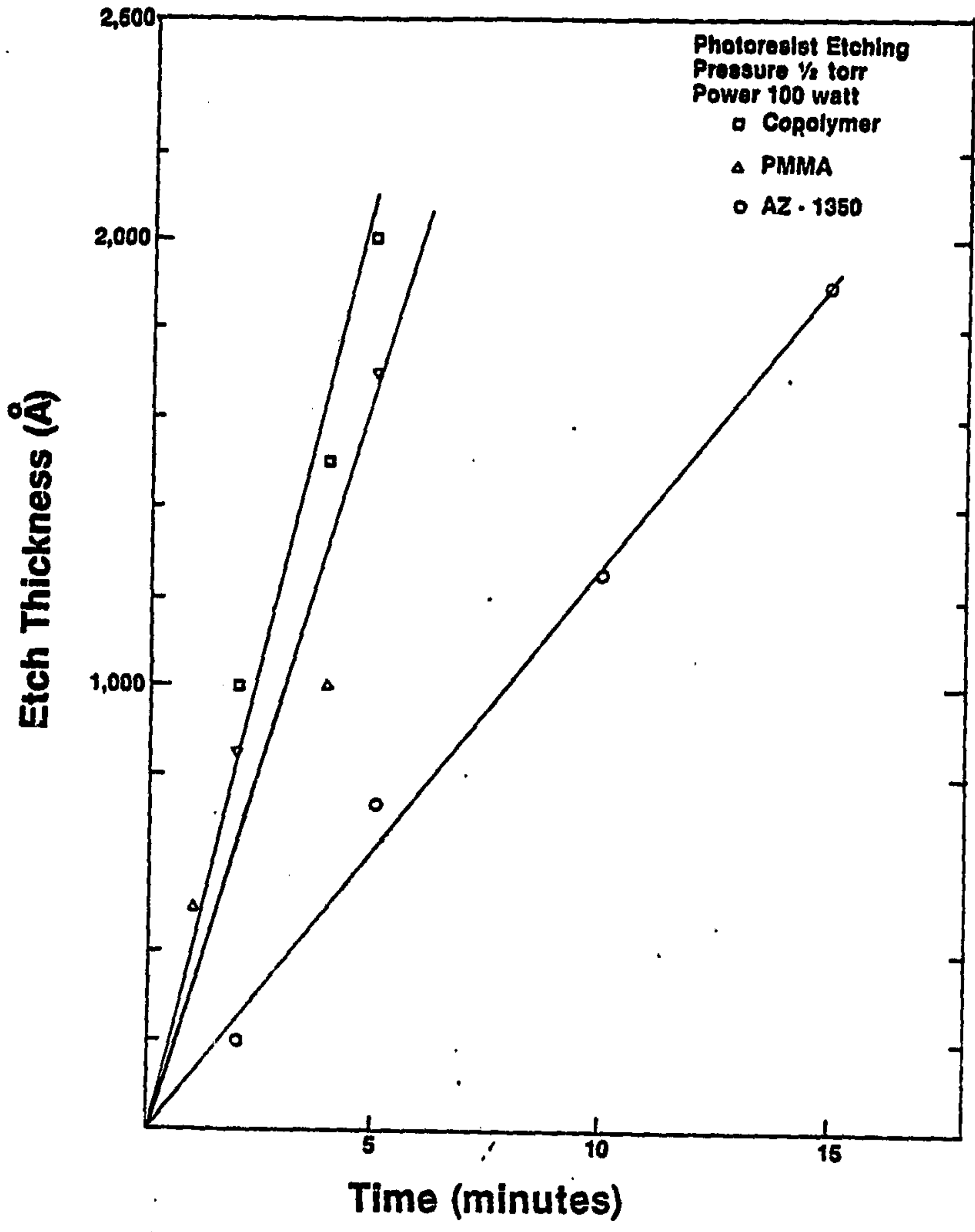


Figure 12

TABLE III

Procces Summary for two layer photoresist

1. Cleaning and Degreasing

2. Bakeout in Air at 200°C for 30 min.

3. PMMA - PMMA Copolymer

   is spun on at 5000A° thickness

4. Bakeout at 160°C for 45 min

5. 4% PMMA is spun at 3000A° thickness

6. Bakeout at 160°C for 60 min.

7. Wafer is placed under quartz plate to check confor

   mal contact

8. Contact adjustment

9. Mask position checked and wafer exposed for 5 minutes at

   a lamp intensity of 19.3mw/cm^2

10. Sample is developed in solution of 2 parts Propanol 1 part Toluene

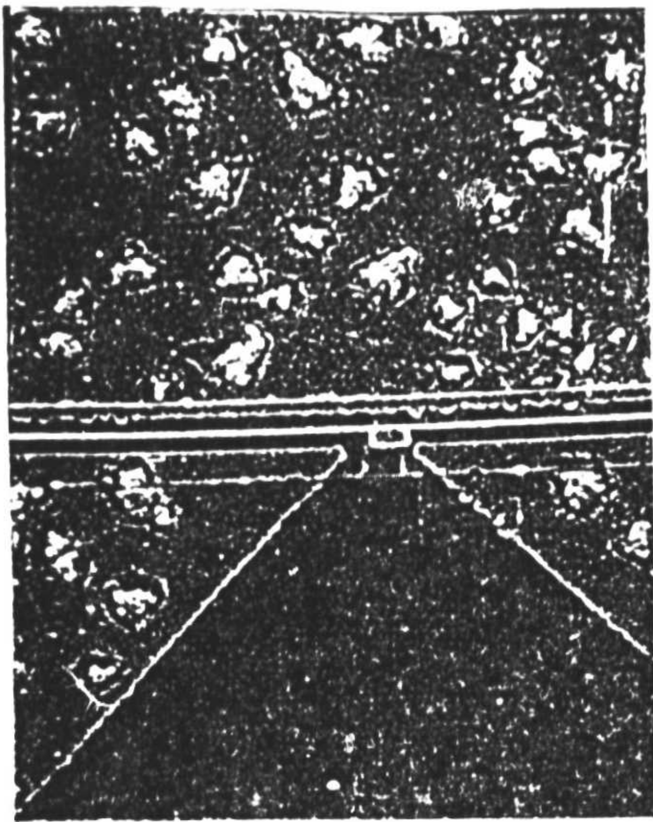
11. Oxygen Plasma Clean-up 1 minute at 100 watts a 1/2 torr pressure

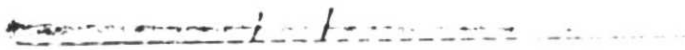
12. Sample is now ready for metallization

Device Structure and Results

In this section, we will summarizies our device results. Since as mentioned in a previous section our vapor systems were not fully operational all of devices results are on ion implanted material. This material was baked out in order to attempt to getter residual impurities.

Our first submicron structure attempted to illustrated our lithography technology using a self aligned Ti/Au gate. In this structure the gate was deposited first and the source and drain were aligned around the gate. This structure was alloyed with the gate in place. We found it necessary to deposited a minimum of 2000'A of Ti, to provide adequate protection during our source/drain alloying process. In the future, we intend to experiment with Pt as a barrier metal. Using this fabrication sequence we have fabricated working devices. Data and pictures for representation devices are shown in Table IV and figures (13),(14),and (15) respectfully. We observed some problems with edge effects on the ohmic contact metalization layers. We believe these problems can be corrected by the addition of nickel to the metalization system.





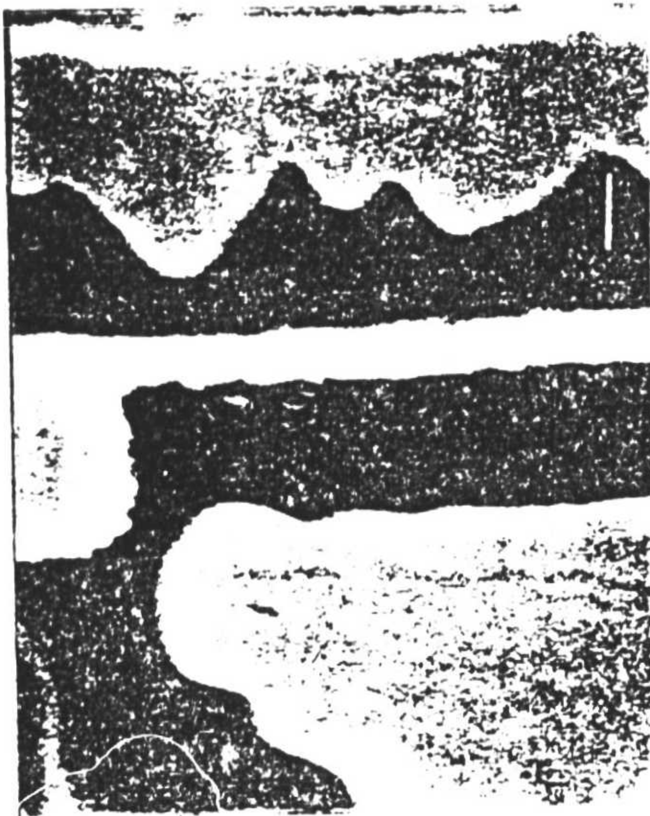
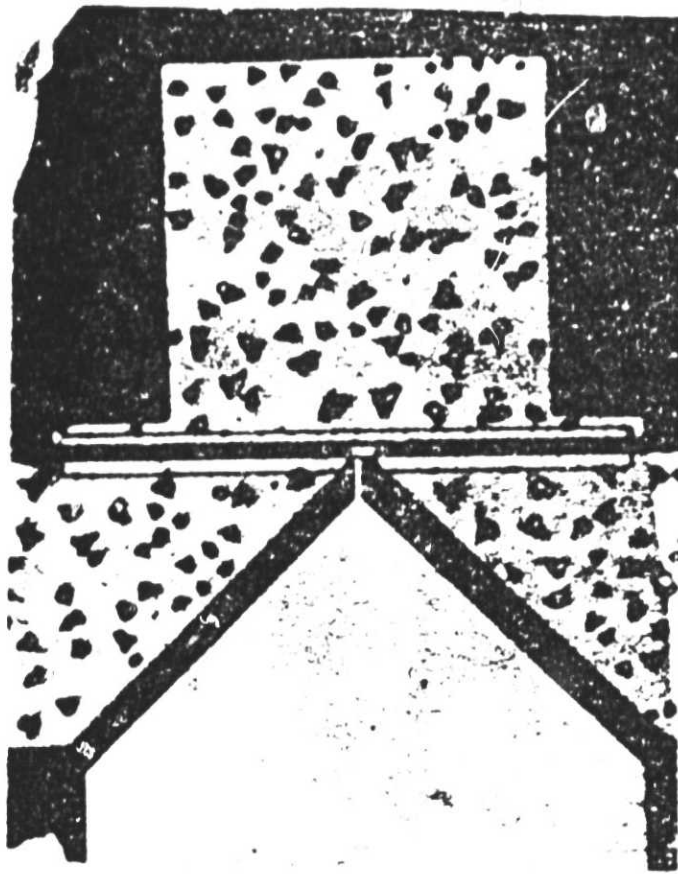


Figure 13



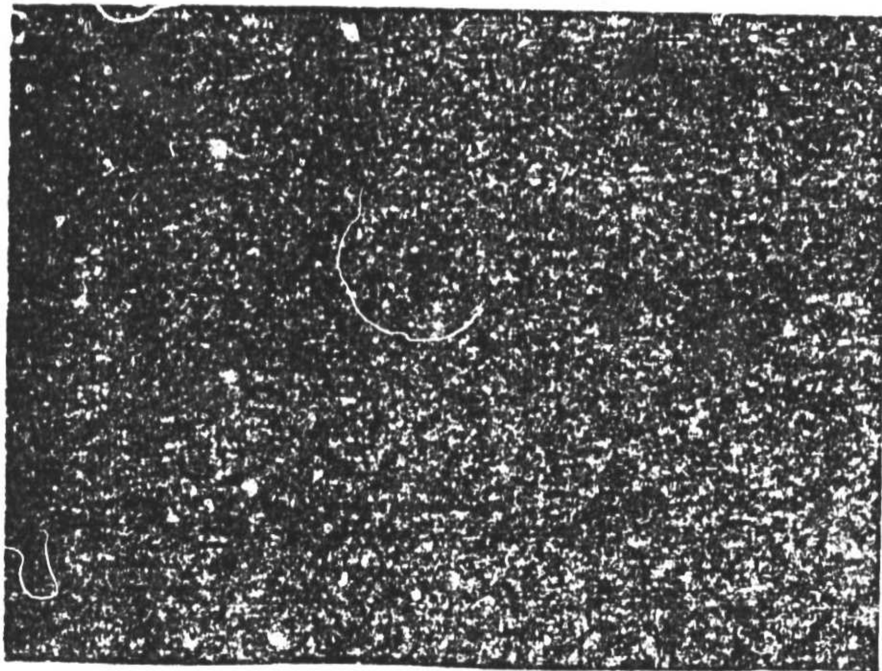
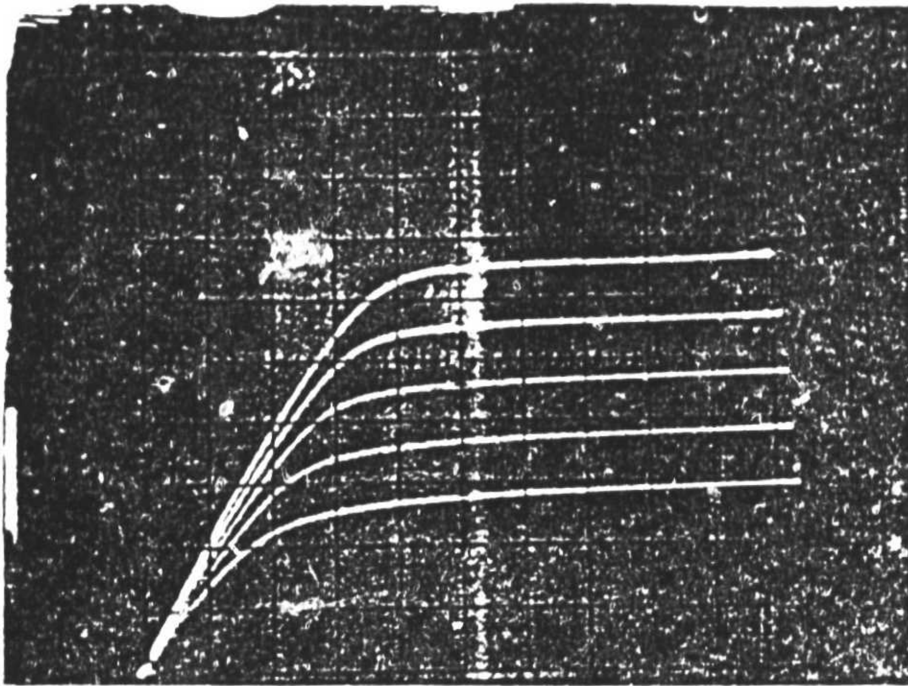
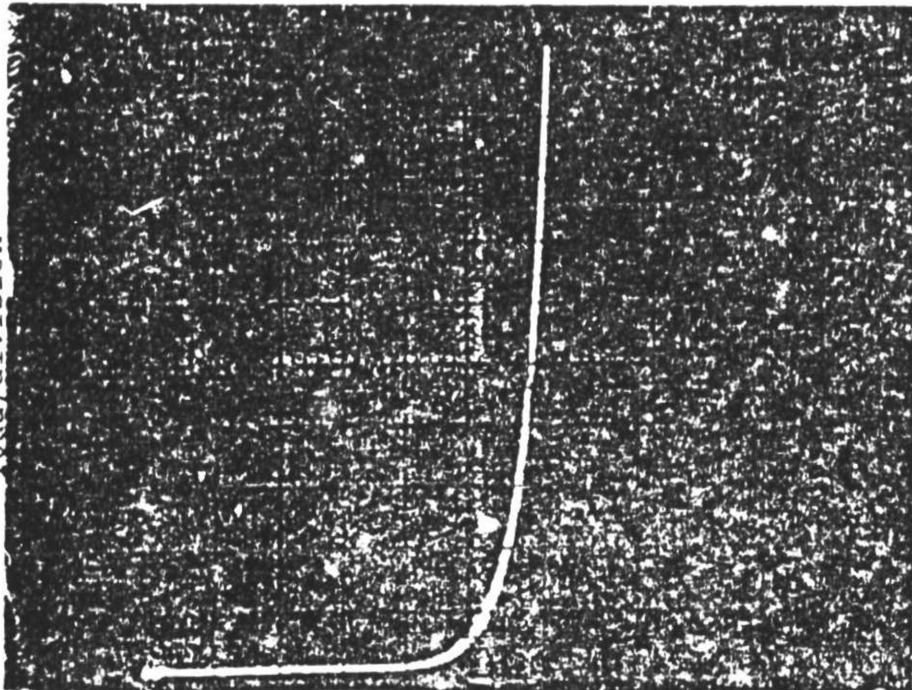


Figure 14



2 ma/division

V_g=.5 volt/per step



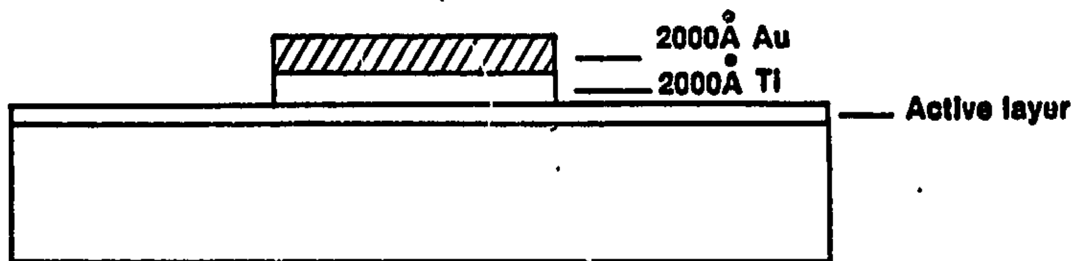
10ua/division

100mm volt/division

Figure 15
I-V characteristics of .5 micron FET (top)
I-V characteristics of gate of FET (bottom)

After demonstrating working devices we proceeded to develop a standard process for our short gate FET experiments. In this structure again the gate is deposited first then a "T" structure is formed by selectively etching the Ti in a CF_4 plasma. This is followed by a blanked evaporation of Au-Ge.

The source drain regions are then defined making this structure a self aligned gate as well as self aligned source drain structure. We anticipate that this structure should lower the parasitic resistance in the source region enough to enable isolation of the effects of gate length on device performance.



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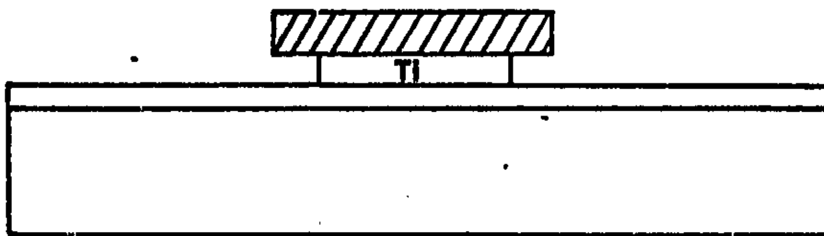

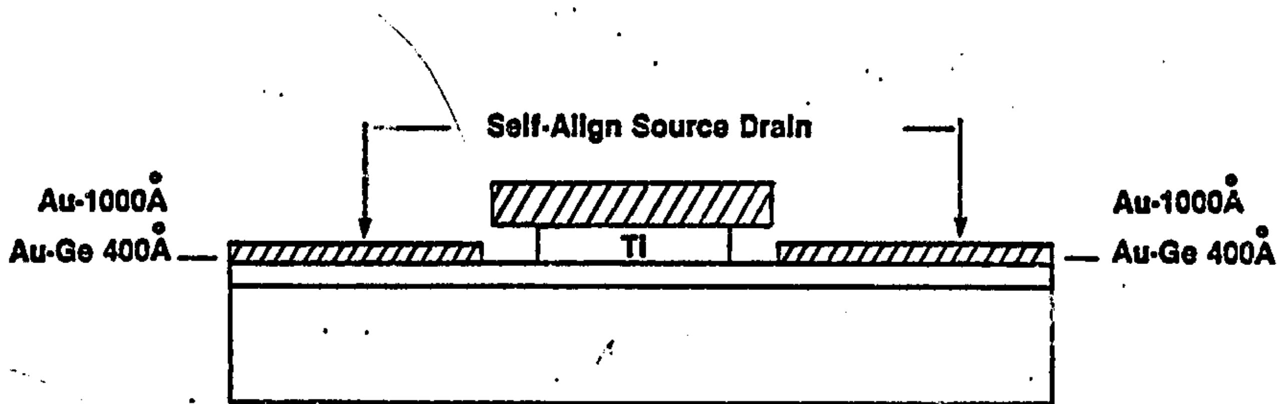

Figure 16

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Table IV

D.C. Characteristics of representative .5 micron Fet's

Gate ideality factor	1.34
Built in gate barrier	.783ev
Source resistance	58 ohms
Drain resistance	42 ohms
Pinch off voltage	3.75 volts
Transconductance	73.2 mseimens

MIXER RESULTS

The results of our mixer effort are summarizied in the following publication

Theorectical Studies

We have investigated several areas related to FET device performance. The details of these investigations appear in the following papers.

Coupling activities

As reported in the interm reports we have had several coupling activities with other government laboratories. With Harry Diamond Laboratories we have fabricated ohmic contacts on superlattice structures. With the Naval Reasearch Laboratories we have been investigating the annealing and characterization of high energy implants. In addition, we have been investigating DLTS spectra of irradiated materials . One of these irradiation studies has been concluded and a paper is attached. Finally we have begun to establish a relationship with the University of Virginia. We will supply them with MBE layers for the purpose of fabricating mixer diodes they in turn will aid us in our development of mixer technology.

FORMATION OF PLANAR n^+ POCKETS IN GaAs FOR MIXER DIODE FABRICATION

JAMES A. GRIFFIN, MICHAEL G. SPENCER, GARY LYNN HARRIS and JAMES COMAS

Reprinted from IEEE Transactions on Electron Devices, Vol. ED-31, No. 8, August 1984

N85-28826

A CONTRIBUTION

" LEAKAGE EFFECTS IN n-GaAs MESFET WITH n-GaAs BUFFER LAYER "

BY

YEN-CHU WANG and MAHMOUD BAHRAMI

SUBMITTED TO

INTERNATIONAL JOURNAL OF ELECTRONICS

DEPARTMENT OF ELECTRICAL ENGINEERING

HOWARD UNIVERSITY

WASHINGTON, D.C. 20059

REVISED MAY 3, 1984

Abstract

Whereas improvement of the interface between the active layer and the buffer layer has been demonstrated, the leakage effects can be important if the buffer layer resistivity is not sufficiently high and/or the buffer layer thickness is not sufficiently small. We find two buffer leakage currents exist from the channel under the gate to the source and from drain to the channel in addition to the buffer leakage resistance between drain and source. It is shown that for 1 μ gate-length n-GaAs MESFET if the buffer layer resistivity ρ is 12 Ω-cm and the buffer layer thickness h is 2 μ, the performance of the device degrades drastically. We suggest that h should be below 2 μ.

I. Introduction

The main advantage of using a buffer layer in n-GaAs MESFET is that the interface between the active layer and substrate can be improved. However, since the buffer layer placed between the active layer and the substrate has thickness of several microns and resistivity much higher than that of the active layer and lower than that of the substrate, leakage currents may flow from and to the active layer through the buffer layer due to its lower resistivity. The leakage effects on device parameters and in particular on device performance will be examined in this work.

In previous works dealing with leakage in a semi-infinite substrate (Liechti, 1976 and Reiser, 1973) the model of the leakage current was considered simply as a leakage resistance between the source and drain. Whereas this simple model is useful for explaining the effect of the leakage resistance on the I-V characteristics, a more detailed model is desirable. In this work we have considered the leakage problem of a finitely thick buffer layer and made detailed calculations which enable us to present a better model. In addition to the drain-to-source leakage resistance, the channel-to-source and drain-to-channel leakage currents are included in our model. Furthermore we have considered in our model, the varying channel potential which is of importance for short gate FET.

In order to simplify the calculation, we have neglected the possible effects of interface trapping and the space charge. Also we assume that the diffusion current from the active layer to the buffer layer is negligible and that the transverse field in the channel is much smaller than the longitudinal field so that the voltage along y-direction(transverse direction)can be considered to be the

same across the channel. This implies that the voltage on the channel-gate interface is the same as that on the channel-buffer layer interface under the gate. Thus a virtual gate electrode(see Fig. 1) can be assumed to exist along the interface between the active and buffer layer. In addition it is assumed that the gate-drain and gate-source spacing are negligibly small. Based upon these assumptions it is therefore possible to deal with merely a static field problem in the buffer layer. Along the interface between the buffer layer and S.I.substrate, no leakage is assumed to exist, i.e. the substrate is assumed to be a perfect insulator. Leakage occurs only in the buffer layer and its interface with the active layer.

By solving the field problem with the help of conformal mapping we can calculate the buffer leakage resistance r_{dsb} and the two leakage current sources I_{GS}^{s} and $I_{DG}^{'}$ on using superposition principle for current on the three electrodes(Sec. II). With this model in mind we derive the equivalent circuit including the leakage effect from which the h-parameters for the device with and without buffer layer can be determined. The performance parameters such as gains and F_{MAX} can be obtained and compared for MESFET's with and without buffer layer(Sec. III). Numerical results and conclusions are presented in sections IV and V, respectively.

II. Analysis of Leakage Elements

We will derive the leakage elements, i.e., leakage resistance and the leakage current sources, by solving two-dimensional Laplace equation for potential distribution in the buffer layer with appropriate boundary conditions set on the interface between the active and buffer layers. In Fig.1, S' and D' are the virtual source and drain electrodes and G' is the virtual gate electrode on which the voltage varies along x-direction due to voltage variation in the channel. Since the field solution assiciated with Fig.1 with finite buffer layer thickness h is difficult, we will use conformal mapping three times to transform this original structure (A) to the parallel plate structure (c) as shown in Fig.2-c from which the field and potential can easily be obtained.

As shown in Fig.2-a (structure A) S', G' and D' are the virtual source, gate and drain, respectively where source and drain are extended into infinity along $\pm x$ and the buffer layer has a finite thickness h. Structure A can be conformally mapped into structure B' (Overmeyer, 1970) with the transformed dimensions given by

$$a_2 \approx b_2 = \frac{\pi}{2h}\tanh\left(\frac{\pi a_1}{2h}\right) \tag{1}$$

$$c_2 = \frac{\pi}{2h} \tag{2}$$

where a_1 is one half of the given gate length. A further transformation gives structure B with new dimensions as given by

$$\frac{c_2}{a_2} = \frac{1}{p} \tag{3}$$

or

$$p = \frac{a_2}{c_2} = \tanh\left(\frac{\pi a_1}{2h}\right) \tag{4}$$

From structure B the final parallel-plate structure (c) is obtained again by using conformal mapping (Okoro, 1980). From structure c we have

$$L=2K(p) \qquad \text{(gate length)} \qquad (5)$$

$$T=K'(p) \qquad \text{(buffer layer thickness)} \qquad (6)$$

where $K(p)$ and $K'(p)$ are the elliptical integral of the first kind and p is given in (4).

When bias voltages are applied to the gate and drain, the channel potential will vary along the longitudinal direction(from S' to D'). As a result of conformal mapping the field variation is preserved in the various structures. The virtual gate potential distribution in the original structure(structure A) can be approximated by two linear regions based on the model of Pucel, 1975(see also Wang, 1979) as shown in Fig. 3 where $V_0(0)=0$, $V_0(\alpha)=V_p$ and $V_0(2a_1)=V_{DS}$ where V_p and V_{DS} are the pinch-off and drain to source potentials, respectively, α is the position of pinch-off point and $2a_1$ is the total given gate length. The virtual gate potential distribution on structure C can be transformed from Fig. 3 into Fig. 4 by requiring that the source, pinch-off and drain voltages remain invariant, i.e. $V_0(0)=0$, $V_0(\alpha')=V_p$ and $V_0(2K(p))=V_{DS}$ where $L=2K(p)$ is the length of the parallel-plate structure (C). In region I of Fig. 3 we have

$$V_0(x)=m_1x \qquad 0\leq x<\alpha \qquad (7)$$

where $m_1=V_p/\alpha$ and in region I of Fig.4 we have

$$V_0(x)=m_1'x \qquad 0\leq x<\alpha' \qquad (8)$$

where $m_1'=V_p/\alpha$. But

$$\frac{\alpha}{2a_1}=\frac{\alpha'}{2K(p)} \qquad (9)$$

from which m_1' can be obtained and is given by

$$m_1' \simeq \frac{V_p}{\frac{K(p)}{a_1}\alpha} \tag{10}$$

Similarly in region II of Fig.3 we obtaine

$$V_0(x)=m_2(x-\alpha)+V_p \qquad \alpha \leq x \angle 2a_1 \tag{11}$$

where $m_2=(V_{DS}-V_p)/(2a_1-\alpha)$, and in region II of Fig.4 we obtain

$$V_0'(x)=m_2'(x-\alpha')+V_p \qquad \alpha' \leq x \angle 2K(p) \tag{12}$$

where

$$m_2'=m_2\frac{2a_1-\alpha}{2K(p)-\alpha'} \tag{13}$$

The parameters for the two linear-region approximation of gate potential distribution are summarized in table 1.

Here we will make use of superposition principle by which we will block one of the three electrodes,i.e., source, gate, or drain, at a time and calculate the leakage element so that the three leakage elements,i.e., r_{dsb} , I_{GS}' and I_{DG}', can be determined from the final parallel-plate structure.

A. Leakage resistance r_{dsb}

Leakage resistance is defined as the resistance between source and drain when the gate electrode is blocked,i.e., there is no current flow on the gate or $(\partial V/\partial y)|_{y=T}=0$ as shown Fig.5. Therefore, the structure reduces to a parallel-plate structure in which the leakage resistance between drain and source is given by

$$r_{dsb}=\rho\frac{2K(p)}{A} \tag{14}$$

where ρ is the resistivity of the buffer layer, $2K(p)$ is the distance between drain and source and A is the cross-sectional area which is given by

$$A=K'(p)z \tag{15}$$

where z is the width of the structure (in z direction). Thus the leakage resistance r_{dsb} in (14) becomes

$$r_{dsb} = \frac{\rho}{z}\frac{2K(p)}{K'(p)} \tag{16}$$

B. Leakage currents

Leakage between the gate and source, and between the drain and gate are modelled as two leakage sources I'_{GS} and I'_{DG}, instead of two resistors, because on the gate, the voltage varies along x-direction and therefore uniform leakage resistances can not be defined. On using the superposition principle I'_{GS} is obtained by calculating the voltage distribution in the structure C with the drain electrode being blocked, and I'_{DG} is obtained with source blocked.

(i). Source-to-gate leakage current I'_{GS}

The structure C when the drain is blocked is shown in Fig.6. Note that there is no leakage between the buffer and the S-I substrate. The general eigen solution of Laplace equation as applied to Fig.6 is given by

$$V_n(x,y)=\left[A_n\cosh(\alpha_n y)+B_n\sinh(\alpha_n y)\right]\left[C_n\cos(\alpha_n x)+D_n\sin(\alpha_n x)\right] \tag{17}$$

Using the boundary conditions shown in Fig.6,i.e.,

$$V_n(x,y)\Big|_{x=0}=0 \tag{18}$$

$$\left.\frac{\partial V_n(x,y)}{\partial y}\right|_{y=0}=0 \tag{19}$$

$$\left.\frac{\partial V_n(x,y)}{\partial x}\right|_{x=2K(p)}=0 \tag{20}$$

$$\left.V_n(x,y)\right|_{y=K'(p)}=V_0(x) \tag{21}$$

where $V_0(x)$ is the channel and therefore the buffer layer potential. The potential distribution in the buffer layer can be obtained and is given by

$$V(x,y)=\frac{1}{K(p)}\sum_{n=odd}\frac{u_n}{\cosh\left[\frac{n\pi}{4}\frac{K'(p)}{K(p)}\right]}\sin\frac{n\pi x}{4K(p)}\cosh\frac{n\pi y}{4K(p)} \tag{22}$$

where

$$u_n=\int_0^{2K(p)}V_0(x)\sin\frac{n\pi x}{4K(p)}\,dx \tag{23}$$

or from Fig.4

$$u_n=u_{nI}+u_{nII}=\int_0^{\alpha}V_0(x)\sin\frac{n\pi x}{4K(p)}\,dx+\int_{\alpha}^{2K(p)}V_0(x)\sin\frac{n\pi x}{4K(p)}\,dx \tag{24}$$

Substituting the appropriate values of $V_0(x)$ as shown in (8) and (12) into (24), we obtain

$$u_n=\left[\frac{4K(p)}{n\pi}\right]^2 m_2'\sin\frac{n\pi}{2}+\left[\frac{4K(p)}{n\pi}\right]^2(m_1'-m_2')\sin\frac{n\pi\alpha'}{4K(p)} \tag{25}$$

The total leakage current I'_{GS} is given by

$$I'_{GS}=\frac{z}{\rho}\int_0^{K'(p)}\left.\frac{\partial V(x,y)}{\partial x}\right|_{x=0}dy \tag{26}$$

where z is the width of the structure and ρ is the resistivity of the

buffer layer. On using (22), (25) and (26) the total leakage current from the gate to source can be obtained and is given by

$$I'_{GS}=\frac{z}{\rho K(p)}\sum_{n=odd} u_n \tanh\left[\frac{n\pi}{4}\frac{K'(p)}{K(p)}\right] \tag{27}$$

(ii). Drain-to-gate leakage current I'_{DG}.

The structure C when source is blocked is shown in Fig.7. Fig.7-a shows the drain is biased at V_{DS}. This is equivalent to the situation as shown in Fig. 7-b from which a solution similar to that in the previous subsection can be obtained. Thus using boundary conditions as shown in Fig.7-b, we have

$$K(p).V(x,y)=\sum_{n=odd}\frac{u'_n}{\cosh\left[\frac{n\pi}{4}\frac{K'(p)}{K(p)}\right]}\cos\frac{n\pi x}{4K(p)}\cos\frac{n\pi y}{4K(p)} \tag{28}$$

where u'_n is given by

$$u'_n=u'_{nI}+u'_{nII}=\int_0^{2K(p)}\left[V_0(x)-V_{DS}\right]\cos\frac{n\pi x}{4K(p)}\,dx \tag{29}$$

On using the appropriate values of $V_0(x)$ given in (8) and (12) in (29), we obtain

$$u'_n=\left[\frac{4K(p)}{n\pi}\right]^2\left[(m'_1-m'_2)\cos\frac{n\pi\alpha'}{4K(p)}-m'_1\right] \tag{30}$$

And the total drain to gate leakage current I'_{DG} is given by

$$I'_{DG}=\frac{z}{\rho}\int_0^{K'(p)}-\frac{\partial V(x,y)}{\partial x}\bigg|_{x=2K(p)}dy \tag{31}$$

or

$$I'_{DG}=\frac{z}{K(p)}\sum_{n=odd}u'_n\sin\frac{n\pi}{2}\tanh\left[\frac{n\pi}{4}\frac{K'(p)}{K(p)}\right] \tag{32}$$

Note that the total leakage currents given by (27) and (32) are inversely proportional to the buffer layer resistivity which implies that higher buffer layer resistivity will give rise to a decrease in leakage currents resulting in better device performance. However, as will be shown later, the buffer layer thickness is critical to leakage resistance and currents.

It should also be noted that the gate-to-source and the drain-to-gate leakage currents are the same as the channel-to-source and drain-to-channel leakage currents, respectively.

III. Performance Parameters

The equivalent circuit of MESFET including the leakage elements obtained in Sec.II is shown in Fig.8. The performance parameters of the device can be obtained using h-parameters(Ohkawa, 1975). Using simple network theory, the h-parameters of Fig.8 can be obtained as follow

$$h_{11}=\left.\frac{V_1}{I_1}\right|_{V_2=0}=\frac{1+j\omega c_{gs}r_i}{j\omega c_{gs}+j\omega c_{dg}-\omega^2 c_{gs}r_i c_{dg}} \tag{33}$$

$$h_{12}=\left.\frac{V_1}{V_2}\right|_{I_1=0}=\frac{(c_{dg}/c_{gs})-B}{A+(c_{dg}/c_{gs})} \tag{34}$$

$$h_{21}=\left.\frac{I_2}{I_1}\right|_{V_2=0}=\frac{g_m-j\omega c_{dg}(1+j\omega c_{gs}r_i)}{j\omega c_{gs}+j\omega c_{dg}(1+j\omega c_{gs}r_i)} \tag{35}$$

$$h_{22}=\left.\frac{I_2}{V_2}\right|_{I_1=0}=\frac{(c_{dg}/c_{gs}-B)(Ag_m-j\omega c_{dg})}{A+(c_{dg}/c_{gs})}+\left(\frac{1}{z_{dbs}}+Bg_m+g_{dg}+j\omega c_{dg}\right) \tag{36}$$

Where

$$A=\frac{1}{r_i\left(j\omega c_{gs}+\frac{1}{r_i}\right)} \tag{37}$$

$$B=\frac{g_{gs}-g_{dg}}{j\omega c_{gs}+\frac{1}{r_i}} \tag{38}$$

$$z_{dbs}=\frac{R_{ds}+r_{dsb}}{r_{dsb}+j\omega c_{ds}r_{dsb}R_{ds}+R_{ds}} \tag{39}$$

For the intrinsic device parameters see Table 2. The drain to gate leakage transconductance g_{dg} is given by

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$$g_{dg}=\left.\frac{I'_{DG}}{V_{DS}}\right|_{V_{GS}=\text{constant}} \quad (40)$$

When no leakage exists in the buffer layer, I'_{DG} and I'_{GS} are equal to zero and $r_{dsb}\rightarrow\infty$, the resultant h-parameters approaches to the well-known intrinsic h-parameters(Ohkawa, 1975).

The performance parameters are:

A. Maximum stable gain GMS

$$GMS=\frac{|h_{21}|}{|h_{12}|} \quad (41)$$

B. Unilateral gain U

$$U=\frac{|h_{12}+h_{21}|^2}{4[Re(h_{11})-Re(h_{22})+Im(h_{12})Im(h_{21})]} \quad (42)$$

where Re denotes the real part and Im denotes the imaginary part.

C. Maximum frequency of oscillation F_{MAX}

$$F_{MAX}=\frac{F_T}{2\sqrt{r_i/R_{ds}}} \quad (43)$$

IV. Numerical Results

The MESFET numerically analyzed in this section has a gate length of 1 μ and a width of 500 μ with an active layer thickness of 0.2 μ and a buffer layer resistivity of 12 Ω-cm. The typical intrinsic parameter values for the MESFET is shown in table 2 (Liechti, 1976). Unless otherwise stated, the buffer layer thickness is assumed to be 2 μ.

The comparisons between the performance parameters of the MESFET with and without buffer layer are based on the intrinsic equivalent circuit in which the parasitic elements have been neglected(see Fig.8)

The leakage current sources are strongly dependent on the resistivity of the buffer layer as shown in (27) and (32). Therefore, by increasing the resistivity of buffer layer, the leakage currents will decrease which improves the device performance. In Fig.9 the leakage resistance and currents are given as functions of the buffer layer thickness. In order to reduce the leakage, the buffer layer thickness must be less than 2 μ. If otherwise leakage will short-circui the active layer current. It is noted that $I_{DG}' \gg I_{GS}'$. This can be accounted for by the existance of high field region between the drain and gate. The variation of the leakage currents with the normalized drain bias voltage V_{DSN} is shown in Fig.10, where the slopes of the curves give the leakage transconductances.

It is shown in Fig.11 that F_{MAX} for the buffered device degrades by a factor of 2 to 4 due to leakage effect. By increasing the buffer layer resistivity and/or decreasing the buffer layer thickness F_{MAX} will improve proportionally.

The unilateral and the maximum stable gains vs. frequency are found decreasing with frequency. But they are much lower for the buffered device due to leakage effect when compared with those of the intrinsic device, as shown in Figs. 12 and 13.

VI. Conclusions

The leakage effect in MESFET has been investigated. It has been shown that if the buffer layer resistivity is low and/or the buffer layer thickness is large, leakage effect will considerably degrade the device performance. We have shown that for the 1 μ gate-length n-GaAs MESFET if the buffer layer resistivity ρ is 12-Ω-cm and the buffer layer thickness h is 2 μ, the gains of device decrease drastically from their intrinsic values. Since the leakage resistance is proportior to ρ and the leakage currents are inversely proportional to ρ thus leakage effects can be reduced by increasing ρ. However, both the leakage resistance and currents depend on h more strongly than ρ thus it is advantageous to decrease h for improving performance. We suggest that h should be lower than 2 μ.

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Table. 1

Parameters for two-linear region approximation of gate potential distribution

(known) Original structure	(calculated) Final structure
α	$\alpha' = \alpha \frac{K(p)}{a_1}$
m_1	$m_1' = \frac{V_p}{\alpha'}$
m_2	$m_2' = \frac{m_2(2a_1 - \alpha)}{2K(p) - \alpha'}$

Table. 2

Typical intrinsic parameter values for the MESFET with the gate length of 1 μ, width of 500 μ, active layer thickness of 0.2 μ with the doping density of 10^{17} cm^{-3}

c_{gs}	0.31[illegible] Pf
c_{dg}	0.038 Pf
r_i	8.0 Ω
g_m	22 m℧
R_{ds}	350 Ω
c_{ds}	0.11 Pf

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List Of Figures

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13. Maximum stable gain vs. frequency for 1 μ gate length MESFET with the buffer layer thickness of 2 μ and resistivity of 12 Ω-cm.

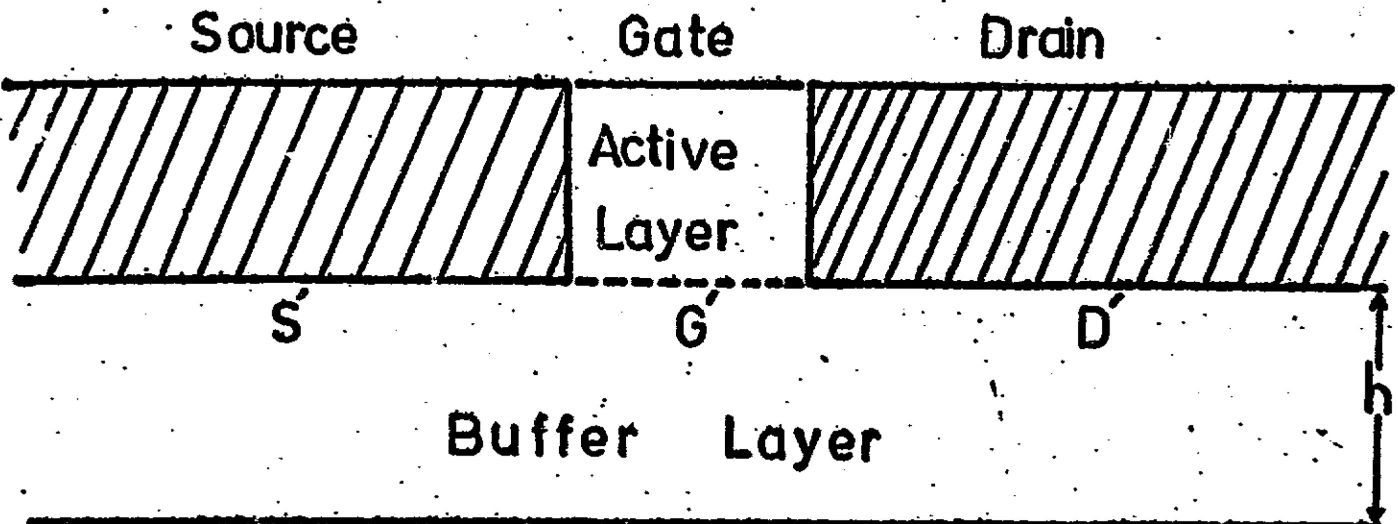

Fig. 1

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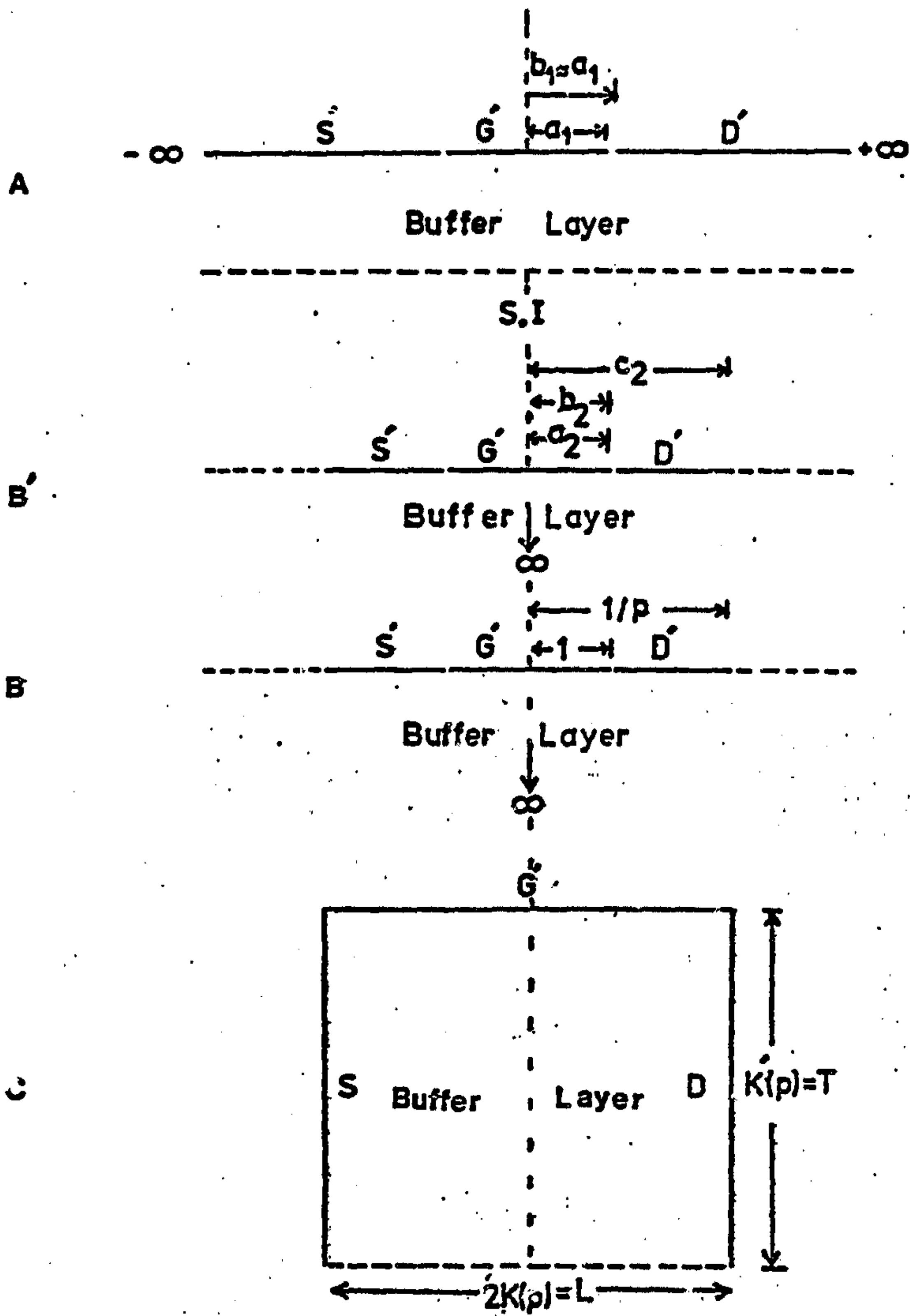

Fig.2

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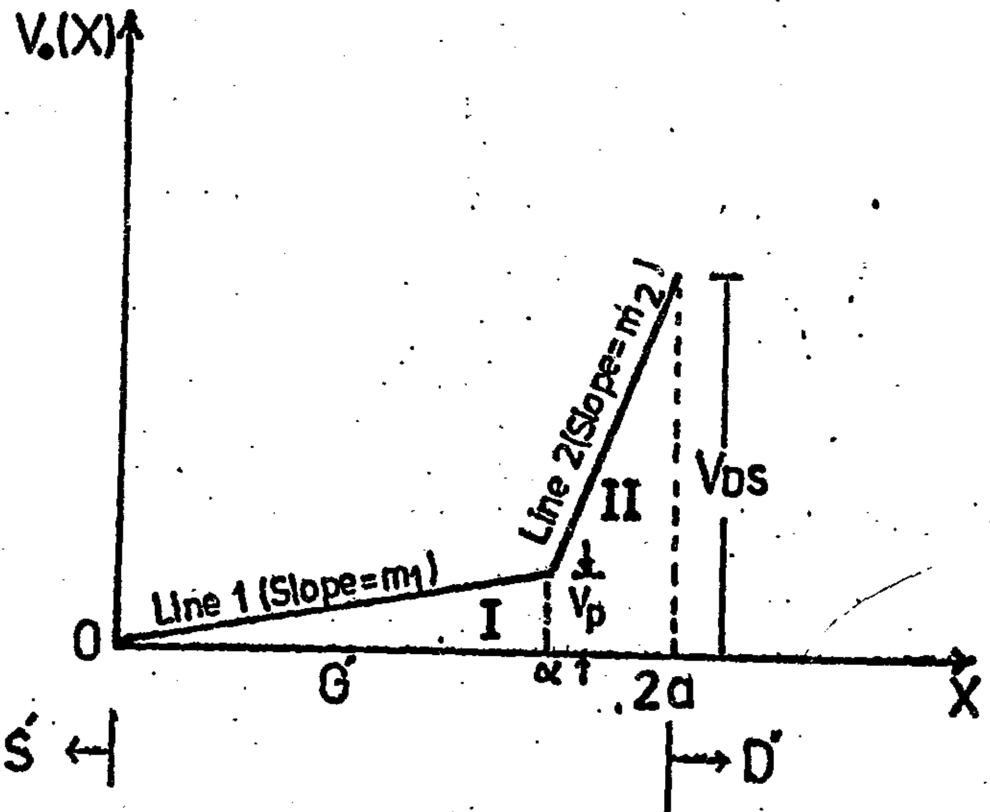

Fig.3

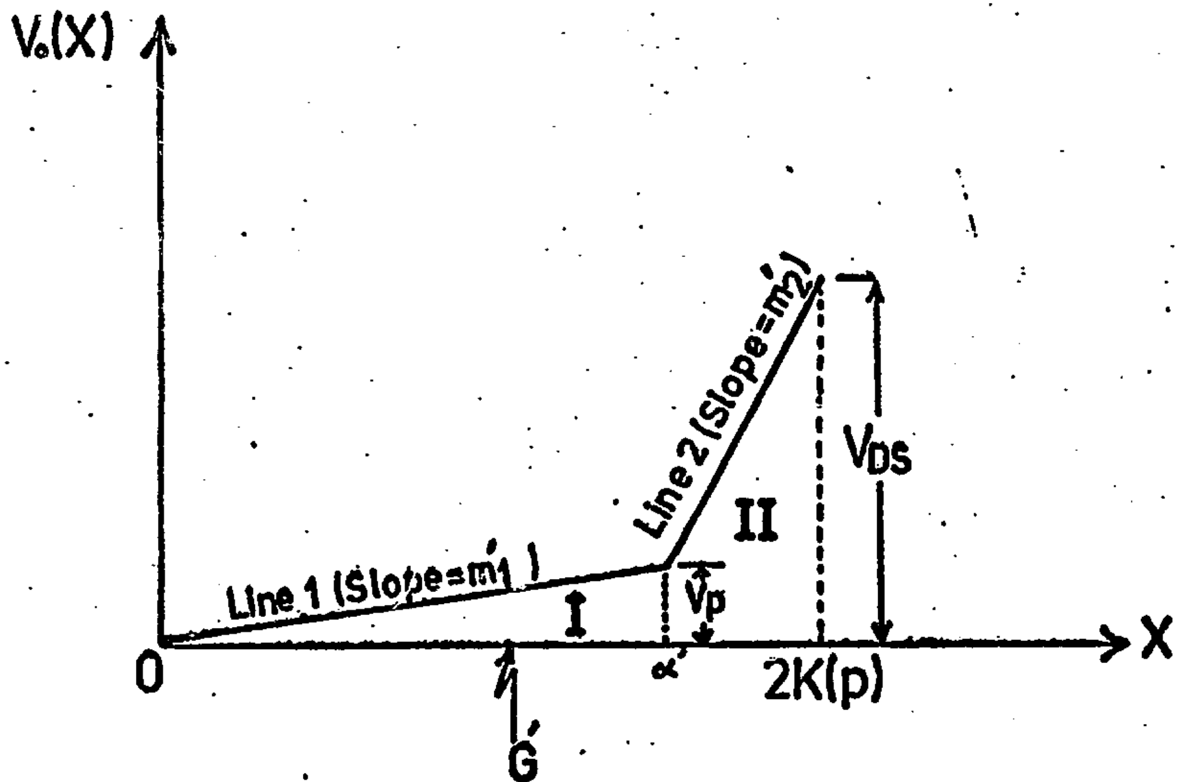

Fig. 4

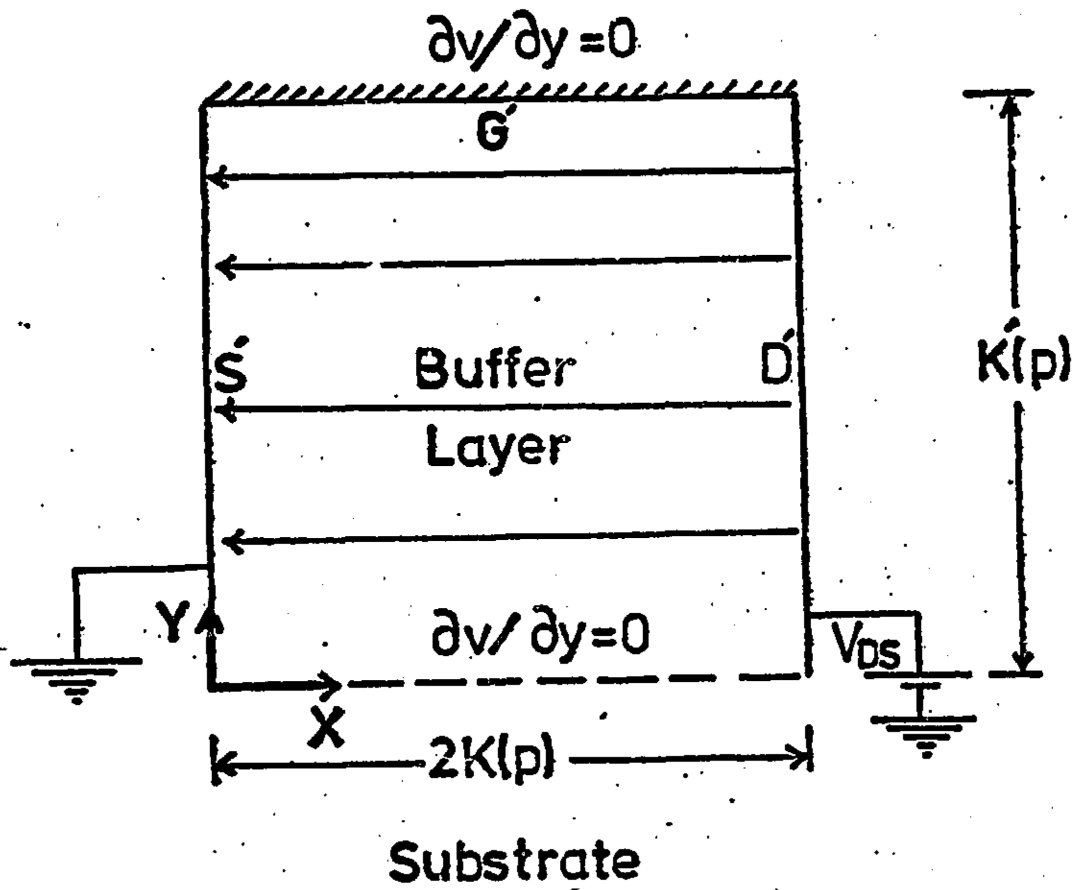

Fig. 5

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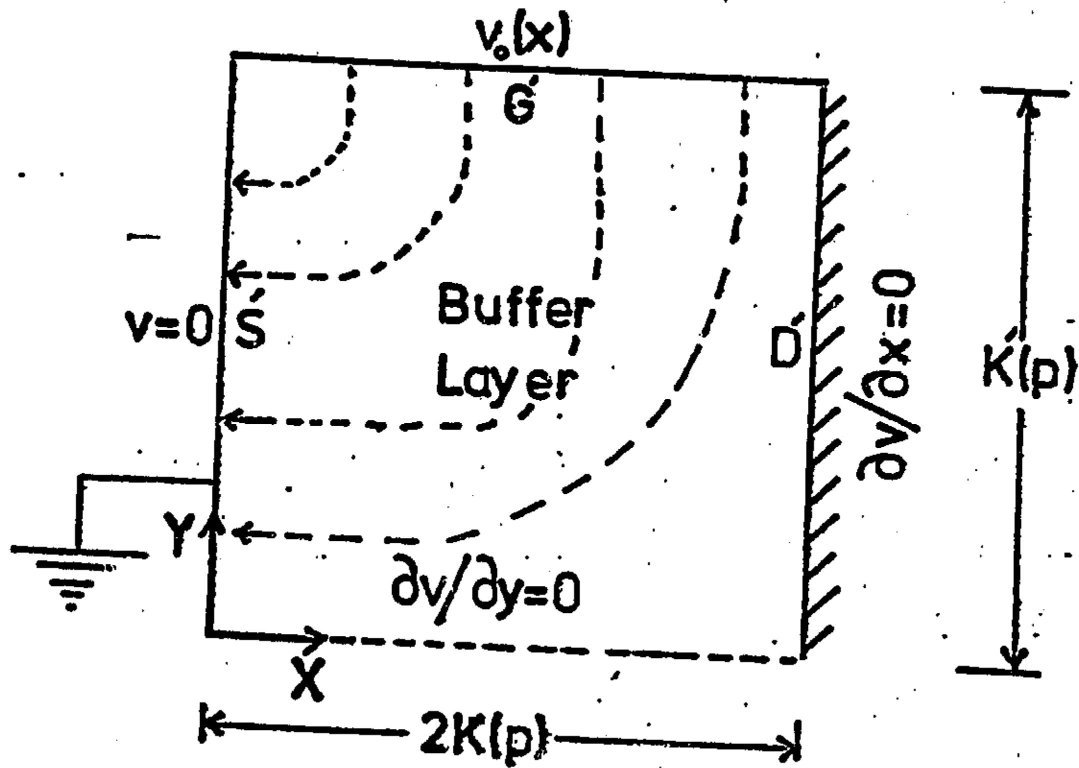
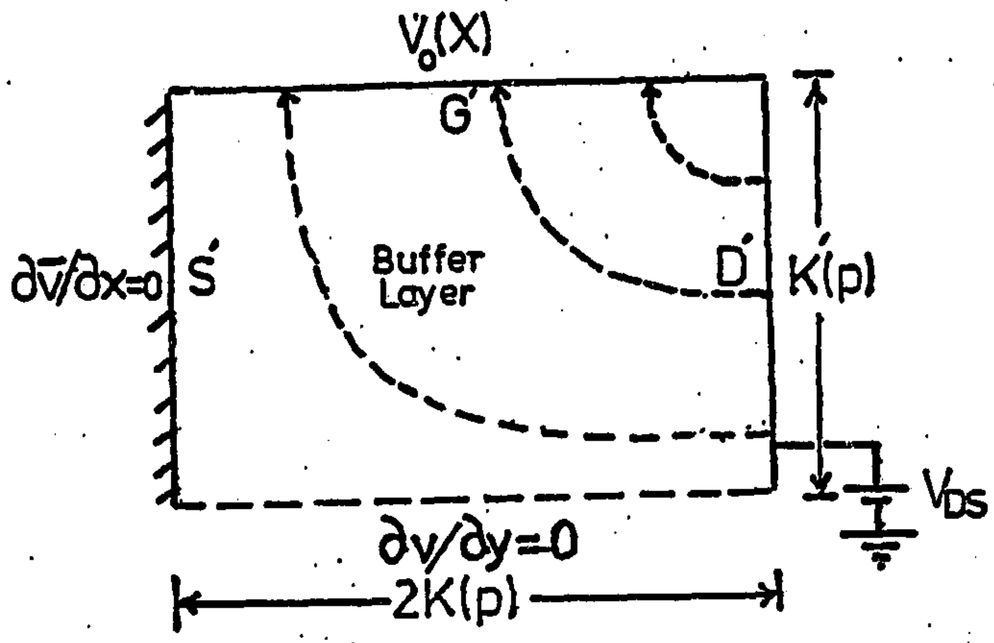
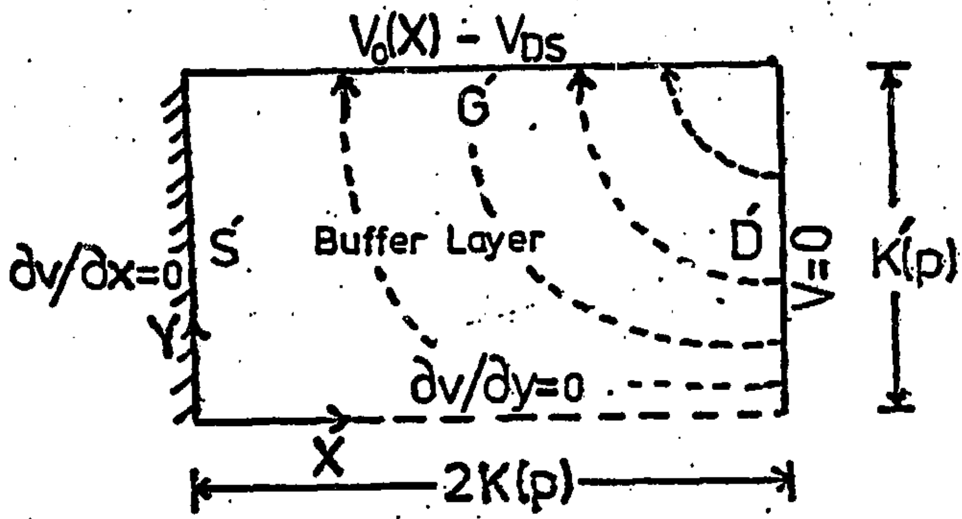


Fig. 6



(a)



(b)

Fig. 7

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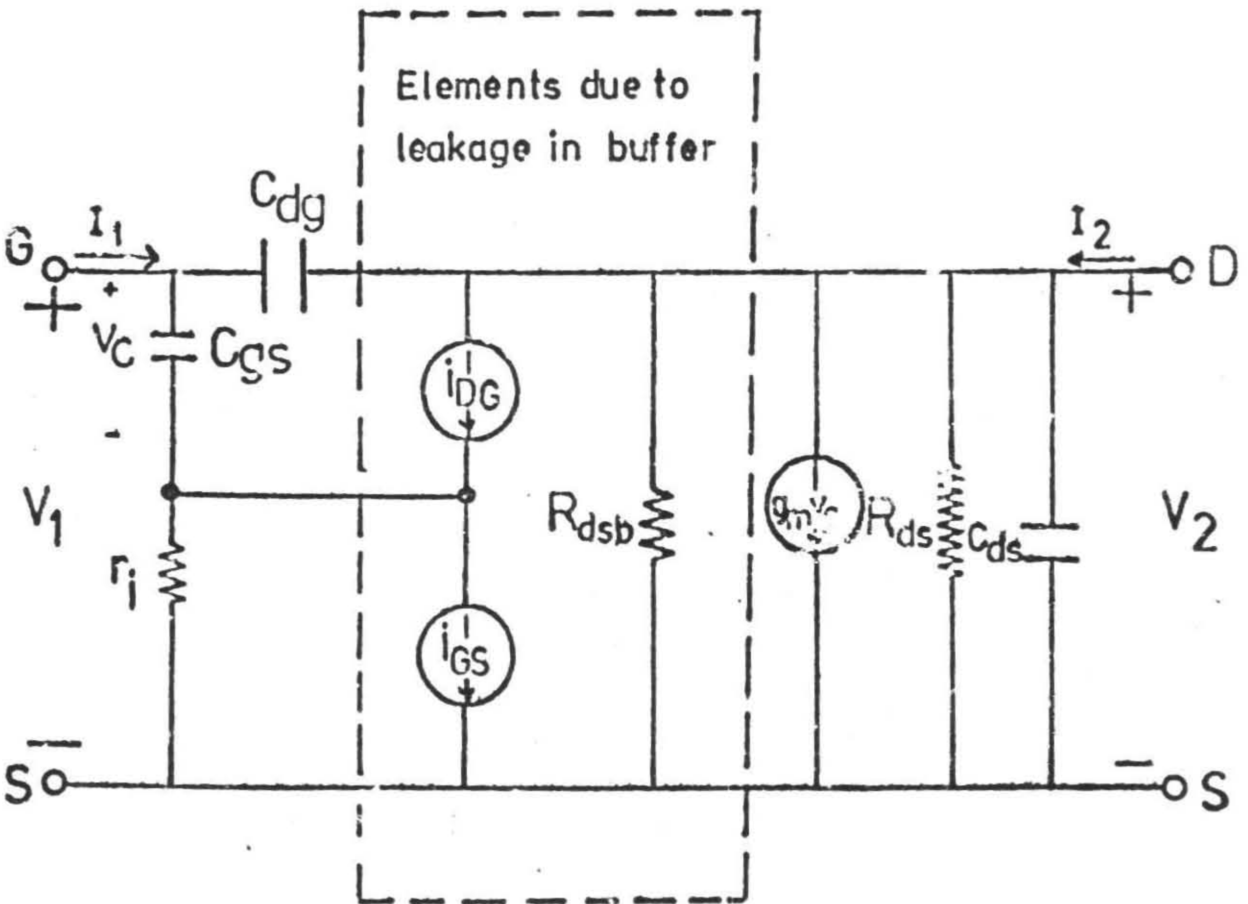

Fig. 8

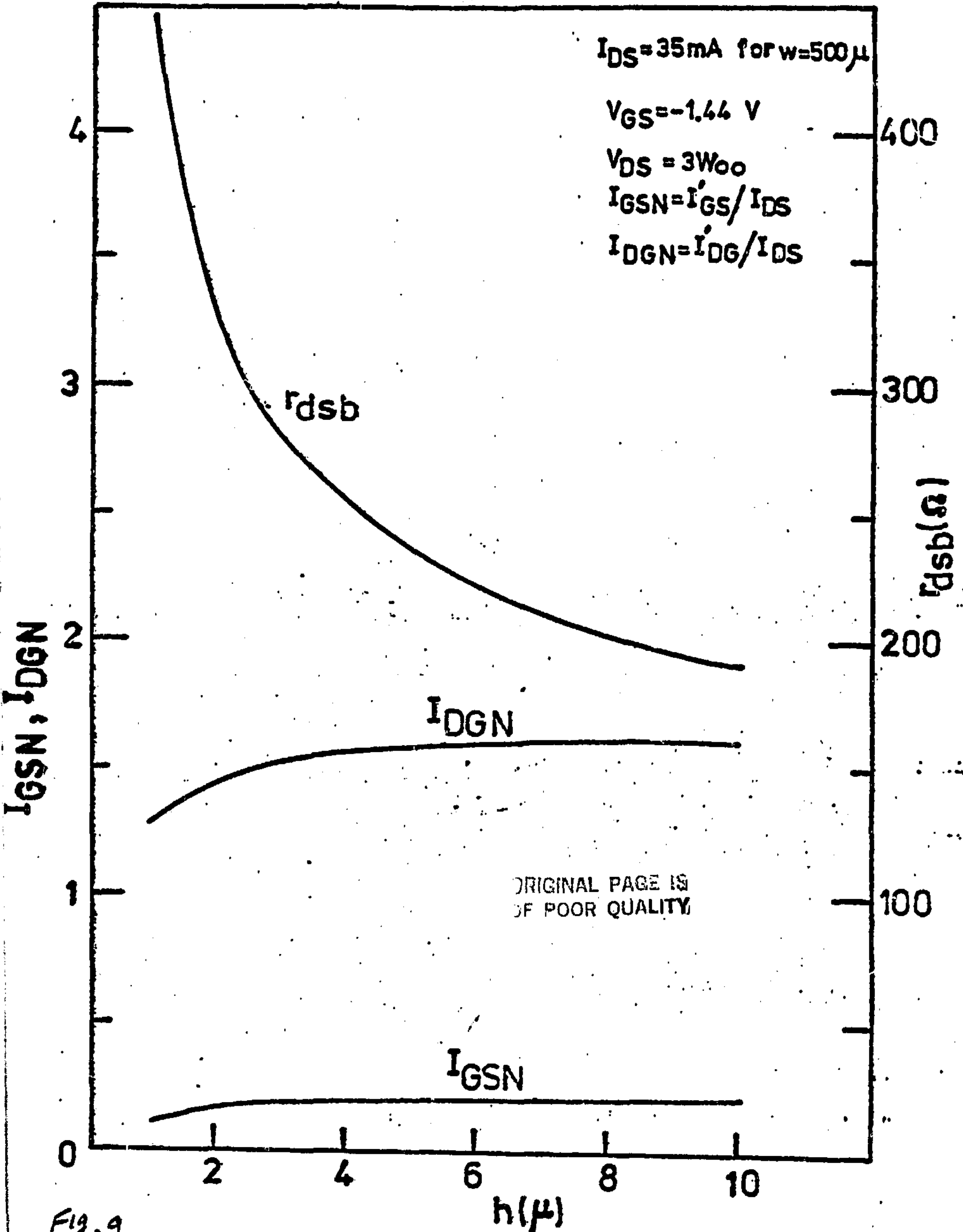

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Fig. 9

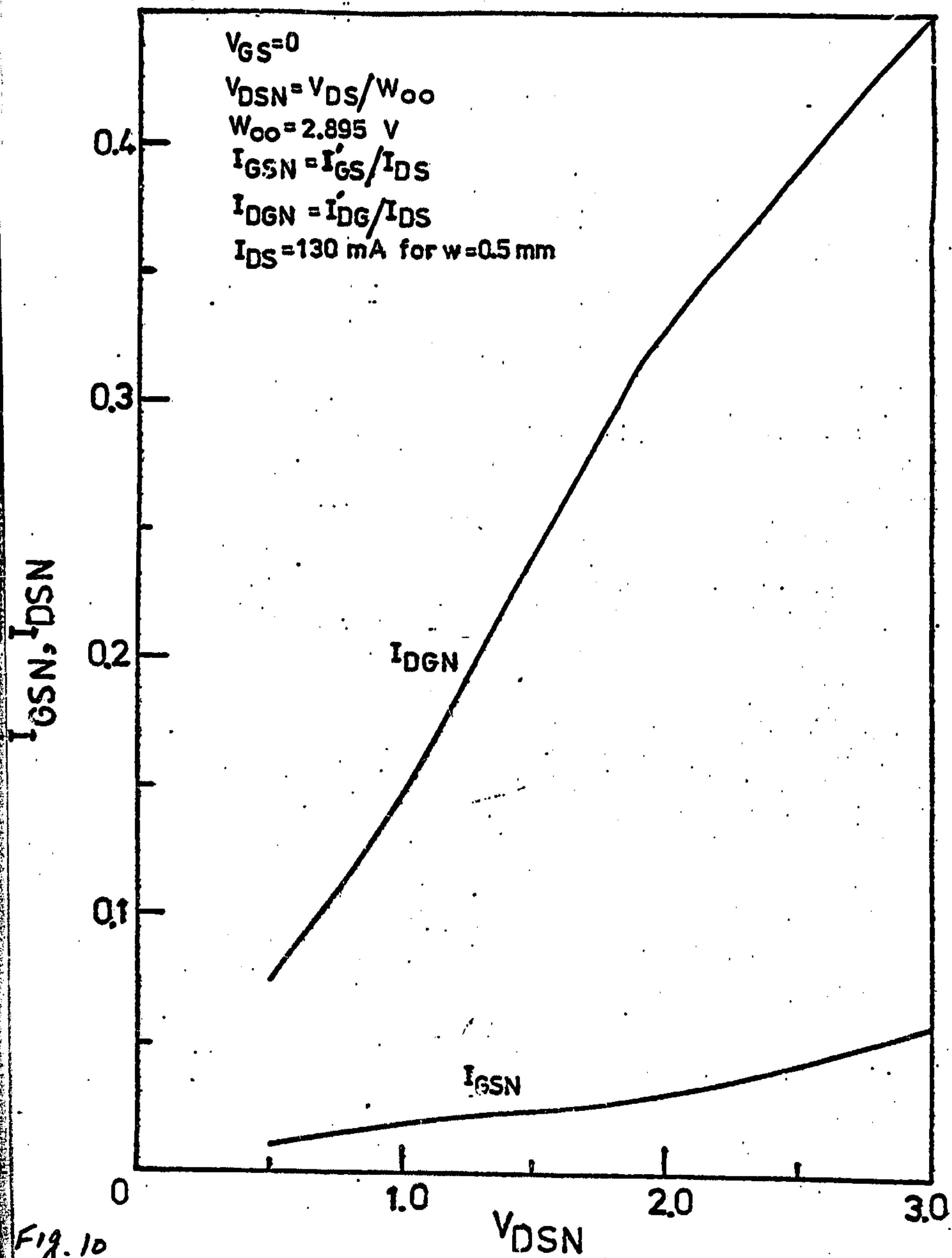

Fig. 10

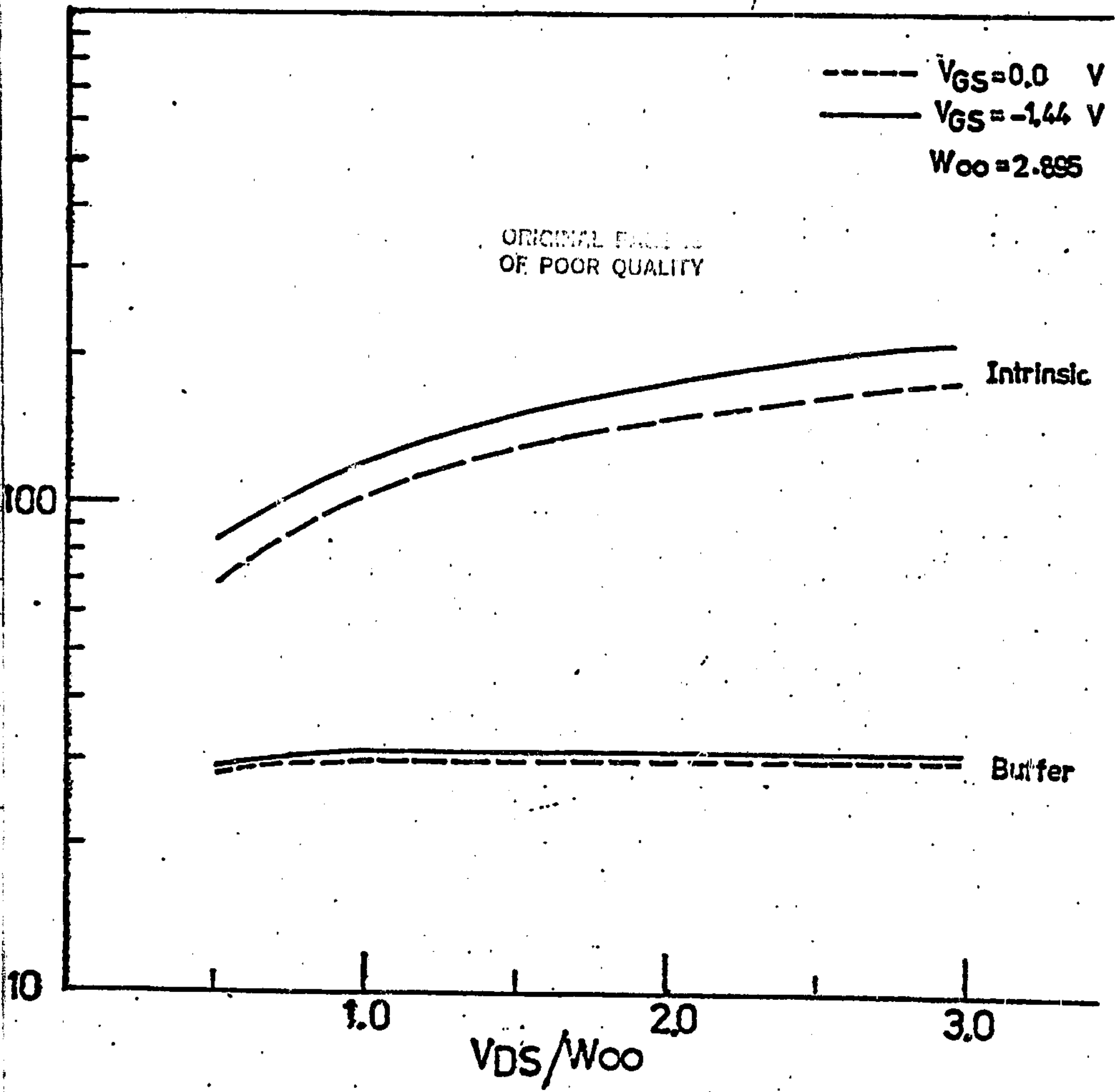

Fig. 11

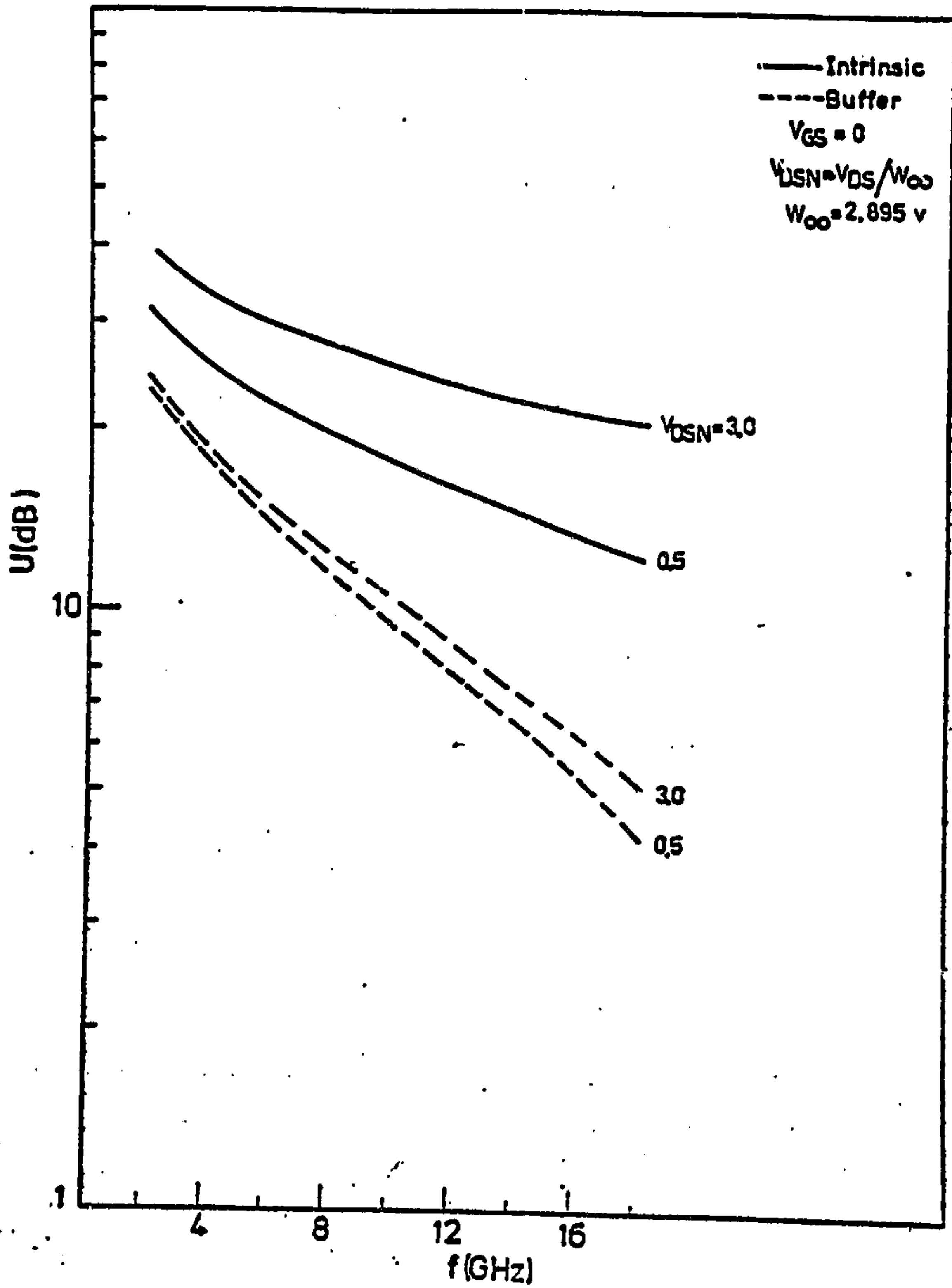

Fig. 12

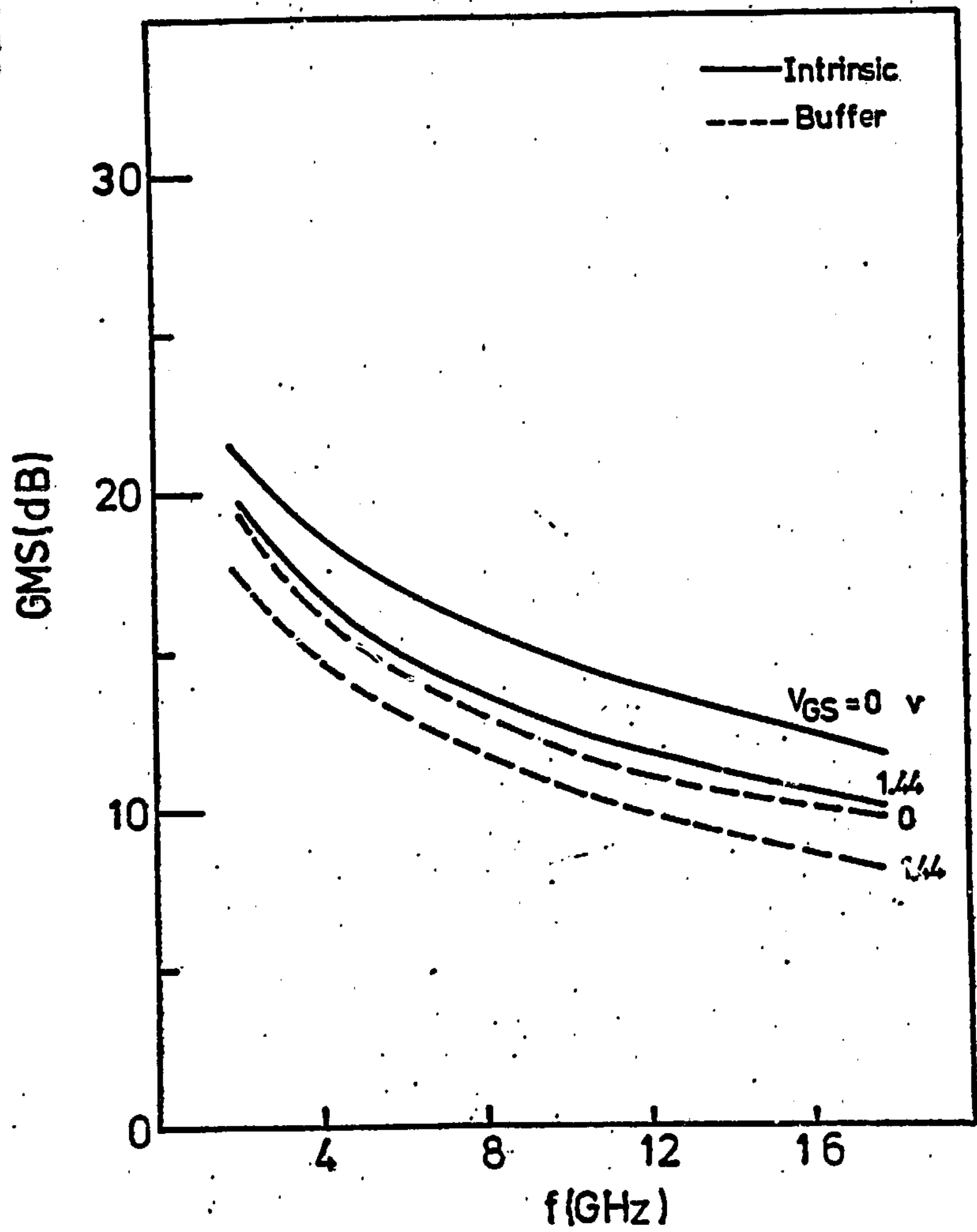

Fig. 13

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N85-28827

A CONTRIBUTION

"GaAs MESFET WITH LATERAL NON-UNIFORM DOPING"

BY

YEN-CHU WANG AND MAHMOUD BAHRAMI

SUBMITTED TO

INTERNATIONAL JOURNAL OF ELECTRONICS

DEPARTMENT OF ELECTRICAL ENGINEERING

HOWARD UNIVERSITY

WASHINGTON, D.C. 20059

DECEMBER 23, 1983

REVISED APRIL 16, 1984

ABSTRACT

An analytical model of the GaAs MESFET with arbitrary non-uniform doping is presented. Numerical results for linear lateral doping profile are given as a special case. Theoretical considerations predict that better device linearity and improved F_T can be obtaiued by using linear lateral doping when doping density increases from source to drain.

I. INTRODUCTION

Improved linearity and noise figure in FET's with vertical non-uniform doping has been demonstrated by Williams and Shaw(1978), Roberts, Lynch, Tan and Gladstone(1978), Pucel(1978) and Santis(1979). In this paper we consider the non-uniform doping (along the electron motion) in the GaAs layer of the FET. Two advantages in this type of FET are anticipated. First if an appropriate profile is used, the depletion-channel interface can become more uniform along the lateral direction hence better linearity. Secondly, The cut-off frequency F_T increase can be realized for certain lateral doping profile.

A general mathematical analysis is presented in which the depletion region potential is solved from Poisson's equation as a boundary value problem. In the channel we adopt the saturation velocity model introduced by Williams and Shaw(1978) which is valid for short gate (Sze, 1981). The analysis takes into account two-dimensional general non- uniform doping profile. In obtaining numerical results however, a simple linear doping profile along the lateral direction is assumed. Device parameters such as g_m, C_{gs} and F_T are given in terms of the gate bias voltage for the FET with gate length of 0.6 μ.

In Sec. II the two dimensional potential in the depletion region is analyzed. In Sec. III the depletion height h/a, reduced potential and channel current for linear lateral doping case are presented. Device parameters are obtained in Sec. IV. Conclusions are given in Sec. V.

II. TWO DIMENSIONAL ANALYSIS OF THE DEPLETION REGION POTENTIAL

A. General solution

The two dimensional Poisson's equation is given by

$$\nabla^2 W(x,y) = \frac{\partial^2 W(x,y)}{\partial x^2} + \frac{\partial^2 W(x,y)}{\partial y^2} = -f(x,y) \qquad (1)$$

where $f(x,y)=qN(x,y)/\epsilon$, $N(x,y)$ is the x-and-y dependent doping density and $W(x,y)$ is the potential in the depletion region as shown in Fig. 1. This inhomogeneous second order partial differential equation can be solved by using Green's function method where equation (1) will be written as

$$\frac{\partial^2 G(x,y)}{\partial x^2} + \frac{\partial^2 G(x,y)}{\partial y^2} = -\delta(x-\zeta)\delta(y-\eta) \qquad (2)$$

where ζ and η are the dummy variables. The boundary conditions associated with (1) are given as follow

Schottky gate: $$W(x,y)\Big|_{y=0} = 0 \qquad (3)$$

Depletion-channel interface: $$\frac{\partial W(x,y)}{\partial y}\Big|_{y=h} = 0 \qquad (4)$$

Ohmic contact source: $$\frac{\partial W(x,y)}{\partial x}\Big|_{x=0} = 0 \qquad (5)$$

Ohmic contact drain: $$\frac{\partial W(x,y)}{\partial x}\Big|_{x=\ell} = 0 \qquad (6)$$

where h is the variable depletion layer height and ℓ is the gate

length (see Fig. 1). It is the unique property of the operator (∇^2) which is the sum of the two commutative operators which enable us to find an explicit solution to (1). Equation (1) can be written as

$$\nabla^2 W(x,y)=K_1 W(x,y)+K_2 W(x,y) \tag{7}$$

where $K_1=\partial^2/\partial x^2$ and $K_2=\partial^2/\partial y^2$. Friedman (1956) shows that if K_1 and K_2 commute, K_2 (or K_1) can be treated as a constant so that the partial differential equation (1) becomes an ordinary differential equation given by

$$\frac{d^2 W(x,y)}{dx^2}+m^2 W(x,y)=-f(x,y) \tag{8}$$

where $m=\sqrt{K_2}$. Using the boundary conditions given in (5) and (6), the solution of (8) becomes

$$W(x,y)=\frac{1}{m}\int^{x} -f(\zeta,y)\sin[m(x-\zeta)]d\zeta \tag{9}$$

where $f(\zeta,y)$ is the spectral representation of K_2. The eigenvalues of $m=\sqrt{K_2}$ will be purely imaginary i.e., $m=(jn\pi)/2h$, and consequently the sin term in (9) will become sinh. The eigenfunction of K_1 can be determined by considering the following homogeneous ordinary differential equation

$$\frac{d^2 W(x,y)}{dy^2}+\lambda^2 W(x,y)=0 \tag{10}$$

where $\lambda=\sqrt{K_1}$. Using boundary conditions given in (3) and (4), the

eigenfunctions of W can be obtained and they would be of the form $\sin\lambda y$ where $\lambda=(n\pi y)/2h$ (n=1,3,5,..). Because of the fact that W is orthogonal and it can be normalized to unity, let

$$f(\zeta,y)=\sum_{n=odd}\left[\beta_n \sin\frac{n\pi y}{2h}\right] \tag{11}$$

where

$$\beta_n=\frac{2}{h}\int_0^h \sin(\frac{n\pi y}{2h})f(\zeta,y)dy \tag{12}$$

where 2/h is the normalization factor. Substituting (12) into (11), the spectral representation of K_2 can be obtained and is given by

$$f(\zeta,y)=\frac{2}{h}\sum_{n=odd}\sin(\frac{n\pi y}{2h})\int_0^h d\eta\ f(\zeta,\eta)\sin(\frac{n\pi\eta}{2h}) \tag{13}$$

Note that $f(\zeta,\eta)$ includes the general doping density in dummy variables ζ,η , i.e., $f(x,y)=qN(x,y)/\epsilon$. The depletion region potential W(x,y) of the FET with general two dimensional doping density can be obtained by substituting (13) into (9) and it is given by

$$W(x,y)=-\frac{4q}{\pi\epsilon}\sum_{n=odd}(1/n)\sin(\frac{n\pi y}{2h})\left\{\int^x d\zeta\int_0^h d\eta\cdot N(\zeta,\eta)\sin(\frac{n\pi\eta}{2h})\sinh[\frac{n\pi}{2h}(x-\zeta)]\right\} \tag{14}$$

B. Uniform doping profile

Whereas equation (14) satisfies (1) and its boundary conditions as can be verified, it reduces to the solution for uniform doping (Pucel, 1975) by setting $N(\xi,\eta)=N_0$ in (14). Thus at the interface (y=h) equation (14) becomes

$$W(x,h)=-\frac{4qN_0}{\pi\epsilon}\sum_{n=odd}(1/n)\sin(\frac{n\pi}{2})\int^{x}d\xi\int_{0}^{h}d\eta\ \sin(\frac{n\pi\eta}{2h})\sinh[\frac{n\pi}{2h}(x-\xi)] \quad (15)$$

After integration and some algebra, equation (15) becomes

$$W(x,h)=\frac{16qh^2N_0}{\epsilon\pi^3}\sum_{n=odd}(1/n^3)\sin(-\frac{n\pi}{2}) \quad (16)$$

The identity

$$\sum_{n=odd}(1/n^3)\sin(\frac{n\pi}{2})=\frac{\pi^3}{32} \quad (17)$$

can be applied to (16) to give the depletion region potential in a uniformly doped FET, i.e.,

$$W(x,h)=W_{OO}(\frac{h}{a})^2 \quad (18)$$

which is identical to that obtained by Pucel (1975). W_{OO} is the pinch-off potential of a uniformly doped FET.

$$W_{OO}=\frac{qa^2N_0}{2\epsilon} \quad (19)$$

Note that there is no well-defined pinch-off potential for non-uniformly doped FET.

III. LINEAR LATERAL DOPING PROFILE

For the special case of lateral doping, $N(\zeta,\eta)=N(\zeta)$ in equation (14), where $N(\zeta)$ is the lateral doping profile. Therefore, the depletion region potential for lateral doping becomes

$$W(x,y)=-\frac{4q}{\pi\epsilon}\sum_{n=odd}(1/n)\sin\left(\frac{n\pi y}{2h}\right)\int^{x}d\zeta\int_{0}^{h}d\eta\ N(\zeta)\sin\left(\frac{n\pi\eta}{2h}\right)\sinh\left[\frac{n\pi}{2h}(x-\zeta)\right] \quad (20)$$

A. Depletion height and reduced potential distribution

For linear doping let

$$N(\zeta)=N_0(1+\alpha\zeta) \quad (21)$$

where α is the rate of change of doping density which increases with ζ (or x) if $\alpha>0$ and decreases if $\alpha<0$. N_0 is assumed to be 10^{17} cm^{-3}. Substituting (21) into (20),

$$W(x,y)=-\frac{4qN_0}{\pi\epsilon}\sum_{n=odd}(1/n)\sin\left(\frac{n\pi y}{2h}\right)\int^{x}d\zeta\int_{0}^{h}d\eta\ (1+\alpha\zeta)\sin\left(\frac{n\pi\eta}{2h}\right)\sinh\left[\frac{n\pi}{2h}(x-\zeta)\right] \quad (22)$$

After integration with respect to η, (22) becomes

$$W(x,y)=-\frac{8qhN_0}{\pi^2\epsilon}\sum_{n=odd}(1/n^2)\sin\left(\frac{n\pi y}{2h}\right)(A_1+A_2) \quad (23)$$

where

$$A_1=\int^{x}d\zeta\,\sinh\left[\frac{n\pi}{2h}(x-\zeta)\right] \quad (24)$$

$$A_2=\alpha\int^{x}d\zeta\cdot\zeta\,\sinh\left[\frac{n\pi}{2h}(x-\zeta)\right] \quad (25)$$

Or

$$A_1=-\frac{2h}{n\pi}\cosh\left[\frac{n\pi}{2h}(x-\zeta)\right]\Big|_{\zeta=x} \quad (26)$$

$$A_2=\alpha\left\{-\frac{2h}{n\pi}\zeta\cdot\cosh\left[\frac{n\pi}{2h}(x-\zeta)\right]-\left(\frac{2h}{n\pi}\right)^2\sinh\left[\frac{n\pi}{2h}(x-\zeta)\right]\right\}\Bigg|_{\zeta=x} \quad (27)$$

Thus

$$A_1=-\frac{2h}{n\pi} \quad (28)$$

and

$$A_2=-\frac{2h\alpha x}{n\pi} \quad (29)$$

Therefore equation (23) becomes

$$W(x,y)=-\frac{8qhN_0}{\pi^2\epsilon}\sum_{n=odd}(1/n^2)\sin(\frac{n\pi y}{2h})(-\frac{2h}{n\pi}-\frac{2h\alpha x}{n\pi}) \quad (30)$$

or

$$W(x,y)=\frac{16qh^2N_0}{\pi^3\epsilon}\sum_{n=odd}(1/n^3)\sin(\frac{n\pi y}{2h})(1+\alpha x) \quad (31)$$

At depletion-channel interface, i.e., $y=h$, the depletion region potential $W(x,y)$ becomes

$$W(x,h)=\frac{16qh^2N_0}{\pi^3\epsilon}(1+\alpha x)\sum_{n=odd}(1/n^3)\sin(\frac{n\pi}{2}) \quad (32)$$

Using the identity described in (17), equation (32) reduces to

$$W(x,h)=\frac{qh^2N_0}{2\epsilon}(1+\alpha x) \quad (33)$$

The reduced potential u which is the same as w of Pucel (1975) can be obtained as follows

$$u^2(x,h)=\frac{W(x,h)}{W_{00}}=\left[\frac{h(x)}{a}\right]^2(1+\alpha x) \quad (34)$$

where W_{00} is given in (19). Because α plays an important role in our analysis, its range and limitation need to be considered. When

α is too small, the doping becomes almost uniform, however, α can not be too large for otherwise the semiconductor will become degenerate. We shall consider the two cases, i.e., small α ($|\alpha\ell|$=0.1) and large α ($|\alpha\ell|$=0.9) where the gate length is assumed to be 0.6μ.

(i). Small α ($|\alpha\ell|$=0.1)

In this case the normalized depletion height h/a becomes almost uniform in the saturation velocity model (Sze, 1981), i.e., u=s where s=u(0,h). Therefore (34) becomes

$$h/a = \sqrt{\frac{s^2}{1+\alpha x}} \approx s \qquad (35)$$

Where s is the reduced potential at the source and is given by (Pucel, 1975)

$$s=\sqrt{\frac{V_{gs}+\phi}{W_{00}}} \qquad (36)$$

Where V_{gs} is the gate-source bias voltage and ϕ is the barrier potential.

(ii). Large α ($|\alpha\ell|$=0.9)

In this case it is necessary to calculate the potential V(x) in the channel. From Fig. 1 and equation (34),

$$V(x)= -(V_{gs}+\phi)+W(x,h)=W_{00}\left[u^2(x,h)-s^2\right] \qquad (37)$$

Under the commonly used assumption of neutral channel, where the carrier and doping densities are the same, the Poisson's equation becomes

$$\frac{d^2V(x)}{dx^2} =0 \qquad (38)$$

The assumption of neutral channel is reasonable for high doping density. It is obvious that the solution of (38) is V(x)=Ax+B,

Where A and B are constant to be determined. Using the conditions that $V(0)=0$ (source is grounded) and $V(\ell)=V_{ds}$ (drain-source bias potential), one obtains $B=0$, and $A=V_{ds}/\ell$. Therefore the channel potential $V(x)$ becomes

$$V(x)=(V_{ds}/\ell)x \tag{39}$$

From (37) and (39), the reduced potential $u(x,h)$ can be obtained and is given by

$$u(x,h)=\sqrt{\frac{W_{00}s^2+(V_{ds}/\ell)x}{W_{00}}} \tag{40}$$

And from (34) the normalized depletion height h/a can be obtained and is given by

$$\frac{h(x)}{a}=\sqrt{\frac{s^2+(V_{dsn}/\ell)x}{1+\alpha x}} \tag{41}$$

Where $V_{dsn}=V_{ds}/W_{00}$. Equation (41) implies that as α increases, the height of the depletion region is no longer a constant and varies with α and x.

B. Channel Current

The total current consists of the conduction current and diffusion current. However, in the neutral channel the diffusion current can be neglected. Also neglected here is the small band-gap narrowing effect due to doping variation.

The conduction current is given by

$$I(x)=qn(x)v_sA \tag{42}$$

Where q is the electron charge, $n(x)=N_0(1+\alpha x)$ is the carrier

(or doping) density, v_s is the saturation velocity and $A(x)=z[a-h(x)]$ is the cross-sectional area(z is the device width). Thus from (42) we have

$$I(x)=qN_0(1+\alpha x)\left[1-\frac{h(x)}{a}\right]azv_s \tag{43-a}$$

In equation (43-a)(which is equivalent to (6) of Pucel, 1975), the current is a function of $h(x)$ and $n(x)$. Therefore the total average current I (which is constant) is obtained by integrating (43-a) from $x=0$ to $x=\ell$

$$I=\frac{1}{\ell}\int_0^{\ell} I(x)dx \tag{43-b}$$

Thus for small α ($|\alpha\ell|=0.1$), $h(x)/a\approx s$ (see (35)), and the total average current becomes

$$I=qv_s zaN_0(1-s)(1+\frac{\alpha\ell}{2}) \tag{44}$$

And for large α ($|\alpha\ell|=0.9$), the total average current can be obtained from (43), and is given by

$$I=\frac{qv_s zaN_0}{\ell}\int_0^{\ell}(1+\alpha x)\left[1-\frac{h(x)}{a}\right]dx \tag{45}$$

It is convenient that we preform the integration in u instead of x. From (40) we solve x in terms of u,

$$x=\frac{\ell(u^2-s^2)}{V_{dsn}} \tag{46}$$

Substituting (46) into (45) we get

$$I=\frac{2qzav_sN_0}{V_{dsn}}\int_s^d u\left\{1+\frac{\alpha\ell}{V_{dsn}}(u^2-s^2)-\left[\sqrt{1+\frac{\alpha\ell}{V_{dsn}}(u^2-s^2)}\right]u\right\}du \tag{47}$$

Where d is the reduced potential at the drain, and is given by (Pucel, 1975)

$$d = \sqrt{\frac{V_{gs} + \phi + V_{ds}}{W_{OO}}} \qquad (48)$$

Equation (44) for small α and (47) for large α are dependent on the gate bias voltage, their transfer characteristics as functions of $(V_{gs}+\phi)/W_{OO} = s^2$ are shown in Fig. 2. For the purpose of numerical calculation, it is specified that α=1.67X10^3 cm^{-1} for small α and α=1.5X10^4 cm^{-1} for large α. Thus for example, for α=-1.67X10^3 cm^{-1}, N(x) decreases from 10^{17} cm^{-3}(source) to 9X10^{16} cm^{-3} (drain), or for α=1.5X10^4 cm^{-1}, N(x) increases from 10^{17} cm^{-3}(source) to 1.9X10^{17} cm^{-3}(drain). The gate length is assumed to be 0.6 μ and the drain-source bias voltage is assumed to be high enough to ensure saturation, i.e., $V_{ds}=W_{OO}$.

Fig. 2 shows significant improvement in linearity when α is large. However, when $\alpha<0$, channel pinches off quickly at low gate-source bias voltage. The reason why it pinches off so fast is that both the channel openning and the carrier density are decreasing functions of x (see ~~(38)~~ 41). Therefore, the voltage swing is very much limited and devices with $\alpha<0$ are of little use.

When α is small, there is no significant difference in the transfer characteristics when compared with uniform doping (α=0) as it should be.

IV. DEVICE PARAMETERS

The small-signal parameters for the case of linear doping is presented in this section. The parameters of a typical FET is assumed to be $z=500\ \mu$, $a=0.2\ \mu$, $\ell=0.6\ \mu$, $N_0=10^{17}\ cm^{-3}$, $E_s=4.44$ KV/cm, $\epsilon_r=12.5$, $\mu_0=4500\ cm^2/V\text{-sec.}$, $\phi=0.8$ V, and $v_s=\mu_0 E_s$. $(0.1\le\alpha\ell\le 0.9)$.

A. Transconductance g_m

The transconductance g_m is defined as

$$g_m=-\left.\frac{\partial I}{\partial V_{gs}}\right|_{V_{ds}}=-\left(\frac{\partial I}{\partial s}\frac{\partial s}{\partial V_{gs}}+\frac{\partial I}{\partial d}\frac{\partial d}{\partial V_{gs}}\right)\Bigg|_{V_{ds}} \tag{49}$$

When α is small, the transconductance can be obtained by using (44) and (49) and is given by

$$g_m\Big|_{(h/a)=s}=\frac{qzv_s aN_0}{2W_{00}s}\,(1+\alpha\ell/2) \tag{50}$$

When α is large, equation (47) can be numerically differentiated according to (49). The transconductance for small and large α are shown in Fig. 3. As expected, for small α, the variation of g_m with gate bias voltage approaches to that of the uniform doping. However, as $|\alpha\ell|$ approaches unity there is significant improvement in linearity of g_m.

B. Gate-to-source capacitance C_{gs}

According to Pucel (1975), the total charge on the gate electrod is given by

$$Q_g=\epsilon_r\epsilon_0 z\int_0^{\ell} E_y\,dx \tag{51}$$

C-2

Where E_y is the y-component of the electric field defined as

$$E_y = \frac{\partial W(x,y)}{\partial y}\bigg|_{y=0} = \frac{2W_{00}}{a}(h/a)(1+\alpha x) \qquad (52)$$

Differentiating (14) with respect to y, E_y hence Q_g can be evaluated.

C_{gs} is defined as (Pucel, 1975)

$$C_{gs} = \frac{\partial Q_g}{\partial V_{gs}}\bigg|_{V_{ds}} = \left(\frac{\partial Q_g}{\partial s}\frac{\partial s}{\partial V_{gs}}\right)\bigg|_{V_{ds}} \qquad (53)$$

For small α, Q_g can be obtained from (51) and (52),

$$Q_g = \frac{2\epsilon_r\epsilon_0 W_{00} zs}{a}\left(\ell + \frac{\alpha}{2}\ell^2\right) \qquad (54)$$

And from (53), C_{gs} becomes,

$$C_{gs}\bigg|_{h/a=s} = \frac{\epsilon_r\epsilon_0 z}{as}\left(\ell + \frac{\alpha}{2}\ell^2\right) \qquad (55)$$

For large α, Q_g becomes

$$Q_g = \frac{2\epsilon_r\epsilon_0 W_{00} z}{a}\int_0^{\ell}(1+\alpha x)(h/a)dx \qquad (56)$$

Where h/a is given in (41). Substituting (56) into (53), C_{gs} for large α can numerically be evaluated. Fig. 4 shows that the rate of change of Q_g with $(V_{gs}+\phi)/W_{00}$ is larger for small α than that for large α. This implies that C_{gs} decreases as $|\alpha|$ increases, as shown in Fig. 4.

C. Cut-off frequency F_T

The unit gain cut-off frequency is given by

$$F_T = \frac{g_m}{2\pi C_{gs}} \tag{57}$$

It is shown in Fig. 5 that for $\alpha > 0$ F_T does not vary with V_{gs} and F_T for large α (where $\alpha \ell = 0.9$, as an example) is almost twice as large as F_T for small and vanishing α. This improvement in F_T can be accounted for by the increase in g_m and decrease in C_{gs} due to the non-uniformity of doping.

V. CONCLUSIONS

Analytical solution of potential in MESFET's with arbitrary doping profile have been presented. The linear doping profile has been treated as a special case, in detail. Numerical results on device parameters for linear lateral doping profile are presented and compared with those for uniform doping. It is shown that there is significant improvement in linearity as $|\alpha \ell|$ approaches toward unity. The transconductance of the FET is found to be larger for $\alpha\ell = 0.9$ than that for $\alpha\ell = 0.1$. This improvement in g_m can be accounted for by the increase in carrier density in the channel. Significant improvement in F_T can be realized for FET's with increasing doping density from source to drain(i.e., $\alpha > 0$). The analytical solution presented here is sufficiently general and it can be applied to other types of profiles such as exponential, power law and step for either vertical or lateral doping or their combinations. In future these topics will be investigated. Although experiments on vertical non-uniform doping have appeared, none has been available on lateral or general doping. Our theory predicts that the device performance depends on doping profile. Optimum lateral and vertical doping will be shown to be important for FET power amplifier.

LIST OF FIGURES

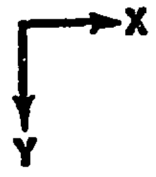
1. Cross-sectional diagram of MESFET showing geometrical dimensions ($a=0.2\ \mu$, $\ell=0.6\ \mu$, $z=500\ \mu$).

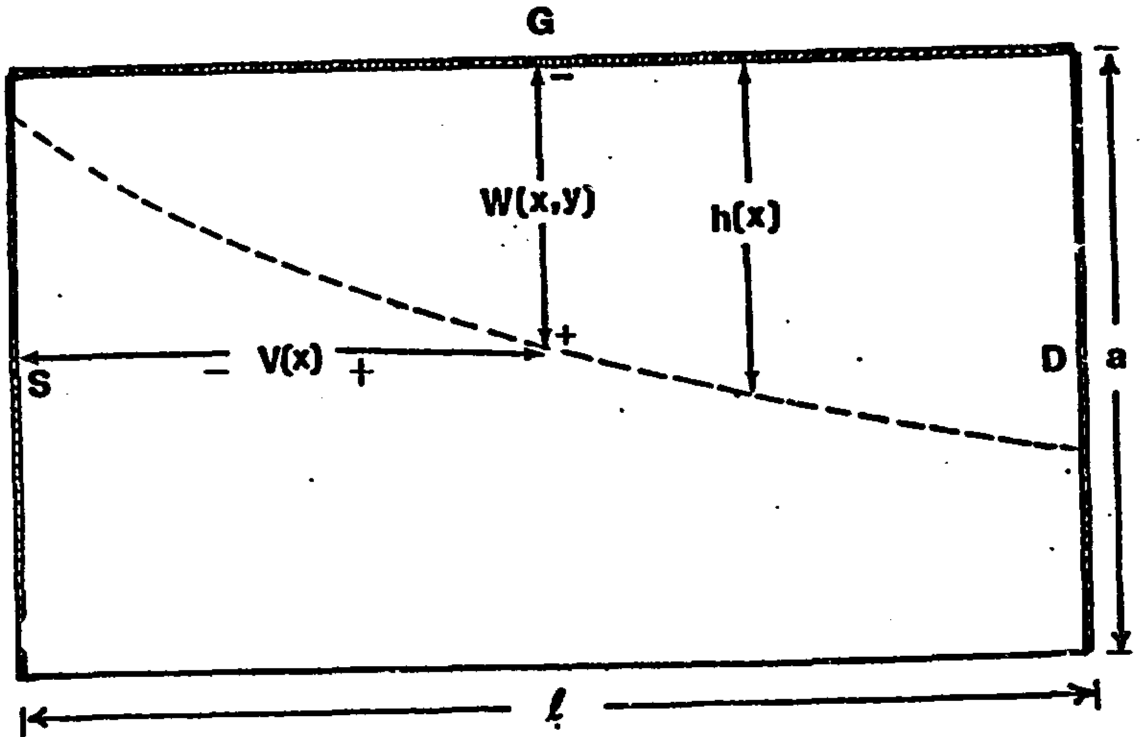
2. Transfer characteristics for uniformly ($\alpha=0$) and non-uniformly ($\alpha\neq0$) doped GaAs MESFET ($a=0.2\ \mu$, $\ell=0.6\ \mu$, $z=500\ \mu$, $N_0=10^{17}\ cm^{-3}$, $W_{00}=2.895$ V, $V_{ds}=W_{00}$).

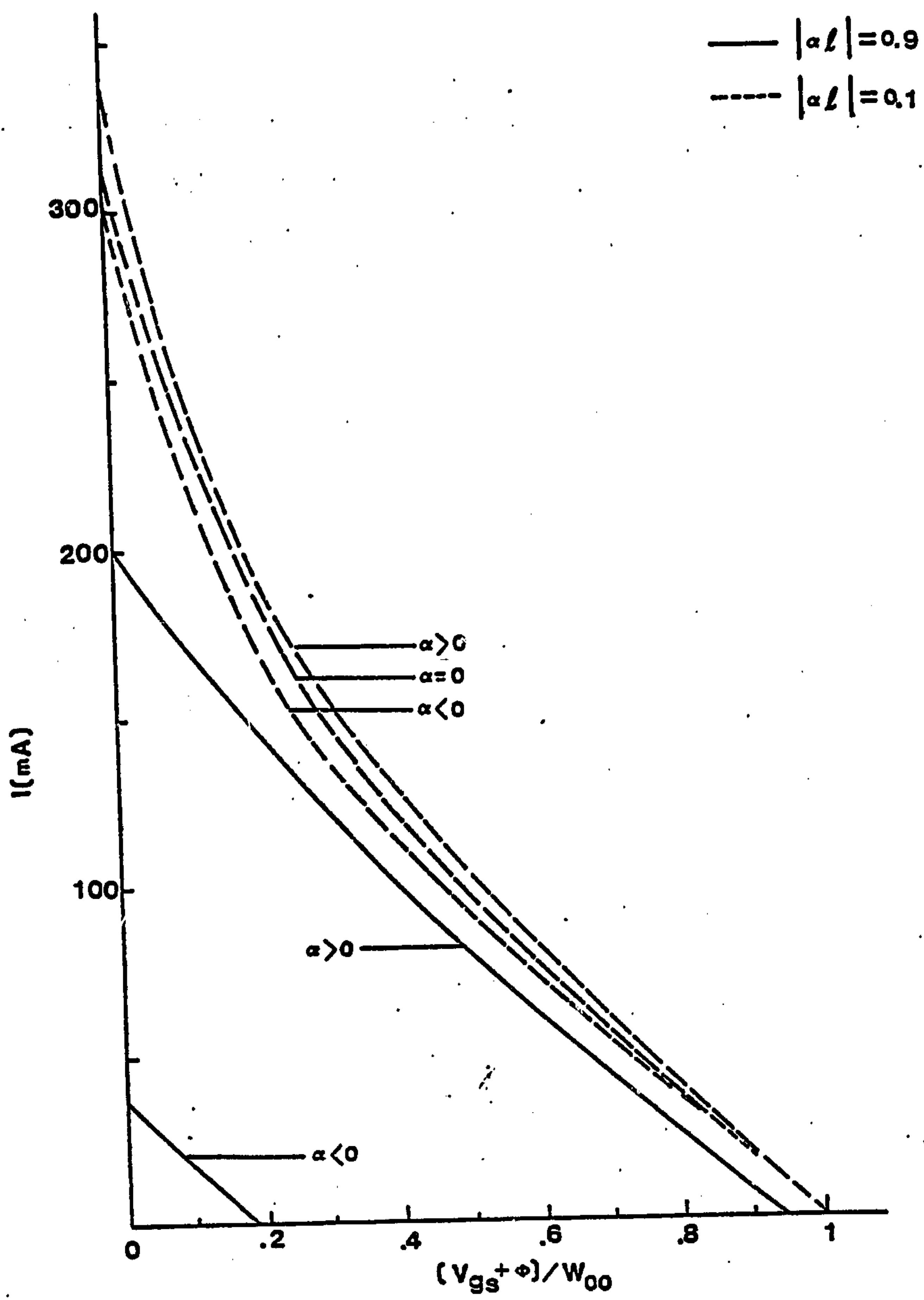
3. Transconductance vs. normalized gate voltage for uniformly ($\alpha=0$) and non-uniformly ($\alpha\neq0$) doped GaAs MESFET ($a=0.2\ \mu$, $\ell=0.6\ \mu$, $z=500\ \mu$, $N_0=10^{17}\ cm^{-3}$, $V_{ds}=W_{00}=2.895$ V).

4. C_{gs} and Q_g vs. normalized gate bias voltage for uniformly ($\alpha=0$) and non-uniformly ($\alpha\neq0$) doped GaAs MESFET ($a=0.2\ \mu$, $\ell=0.6\ \mu$, $z=500\ \mu$, $N_0=10^{17}\ cm^{-3}$, $V_{ds}=W_{00}=2.895$ V, $\epsilon_r=12.5$).

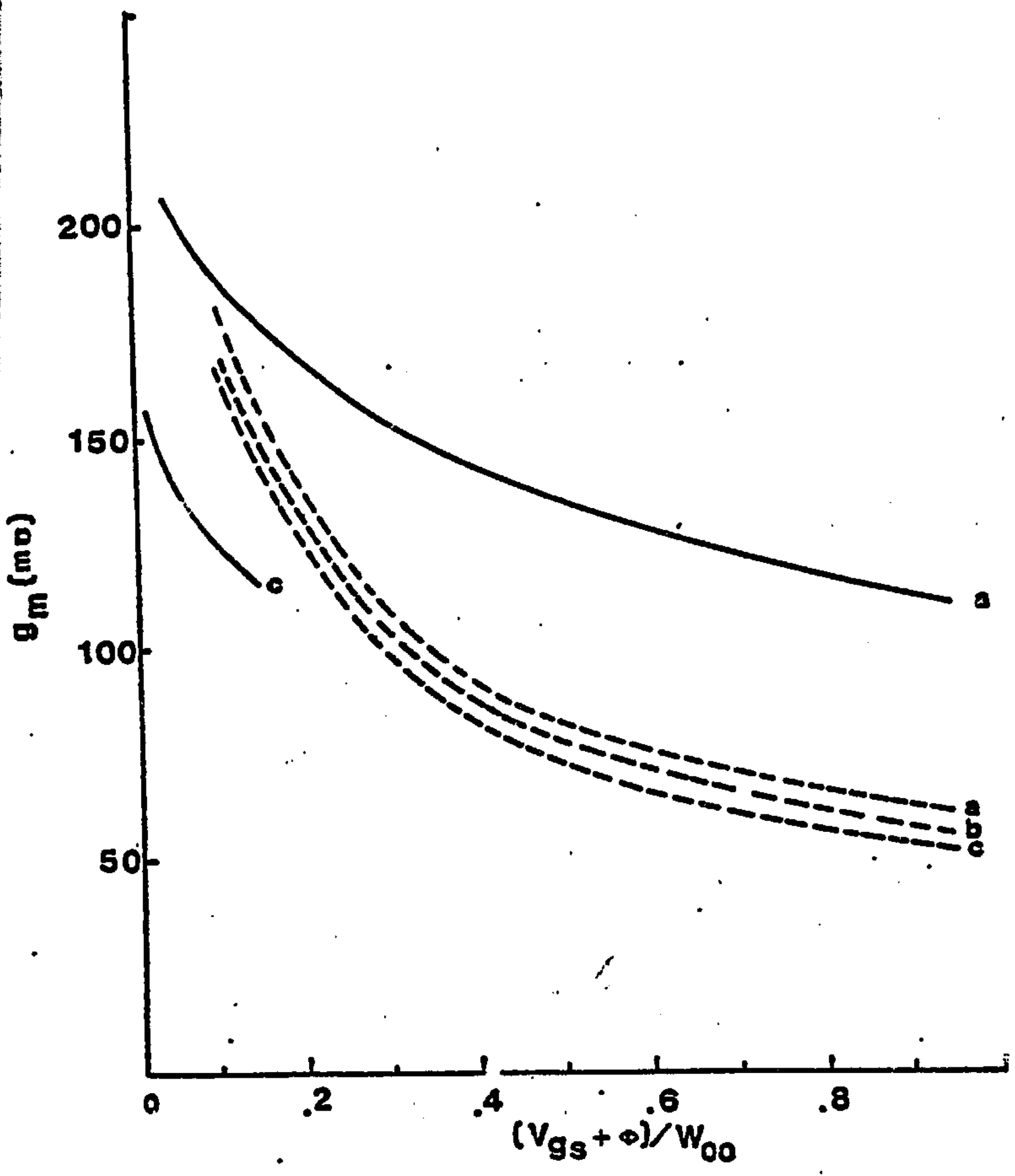
5. Cut-off frequency F_T vs. normalized gate bias voltage for uniformly ($\alpha=0$) and non-uniformly ($\alpha\neq0$) doped GaAs MESFET ($a=0.2\ \mu$, $\ell=0.6\ \mu$, $z=500\ \mu$, $V_{ds}=W_{00}=2.895$ V).


X
Y

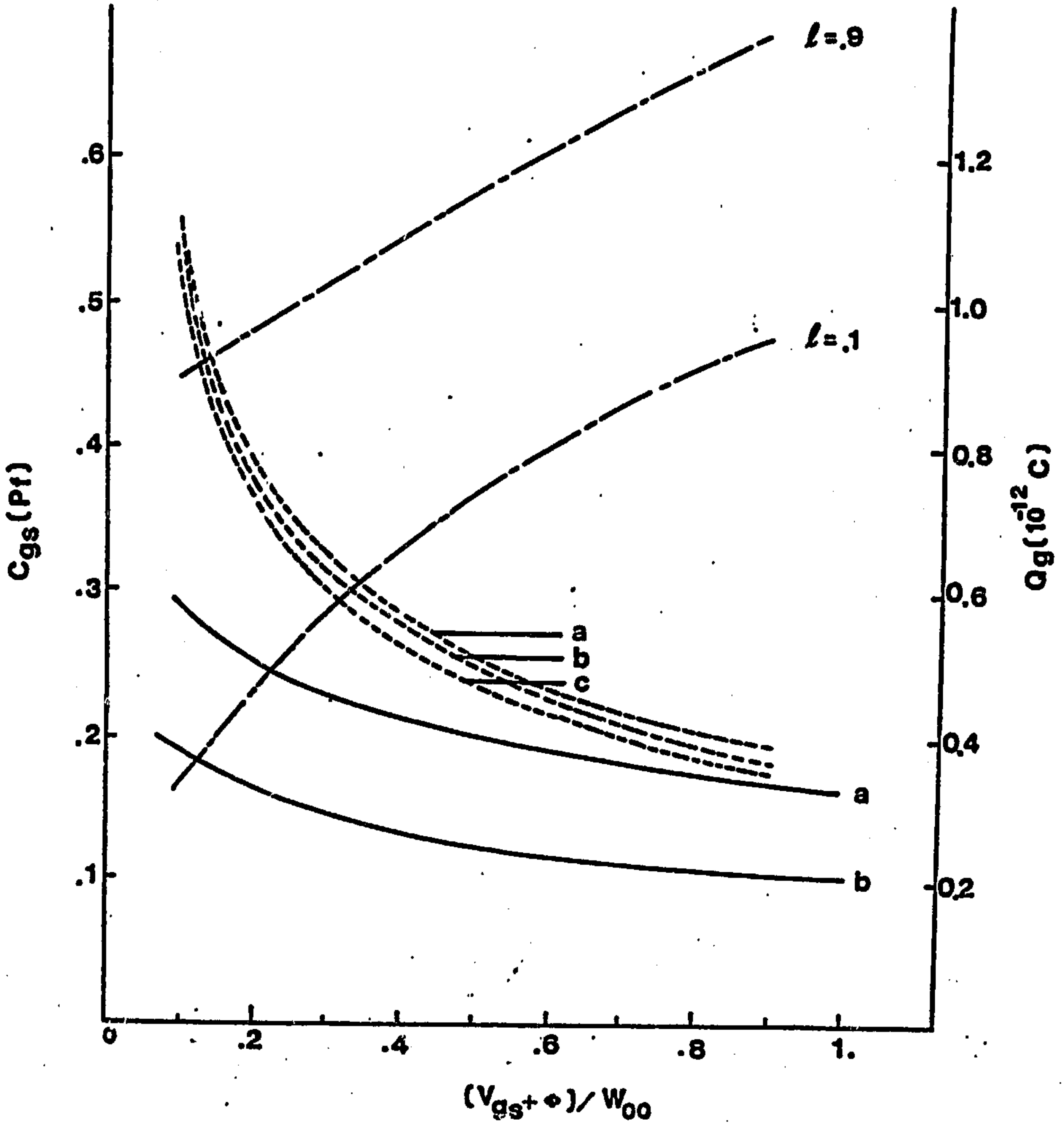

G
W(x,y)
h(x)
V(x)
S
D
a
ℓ



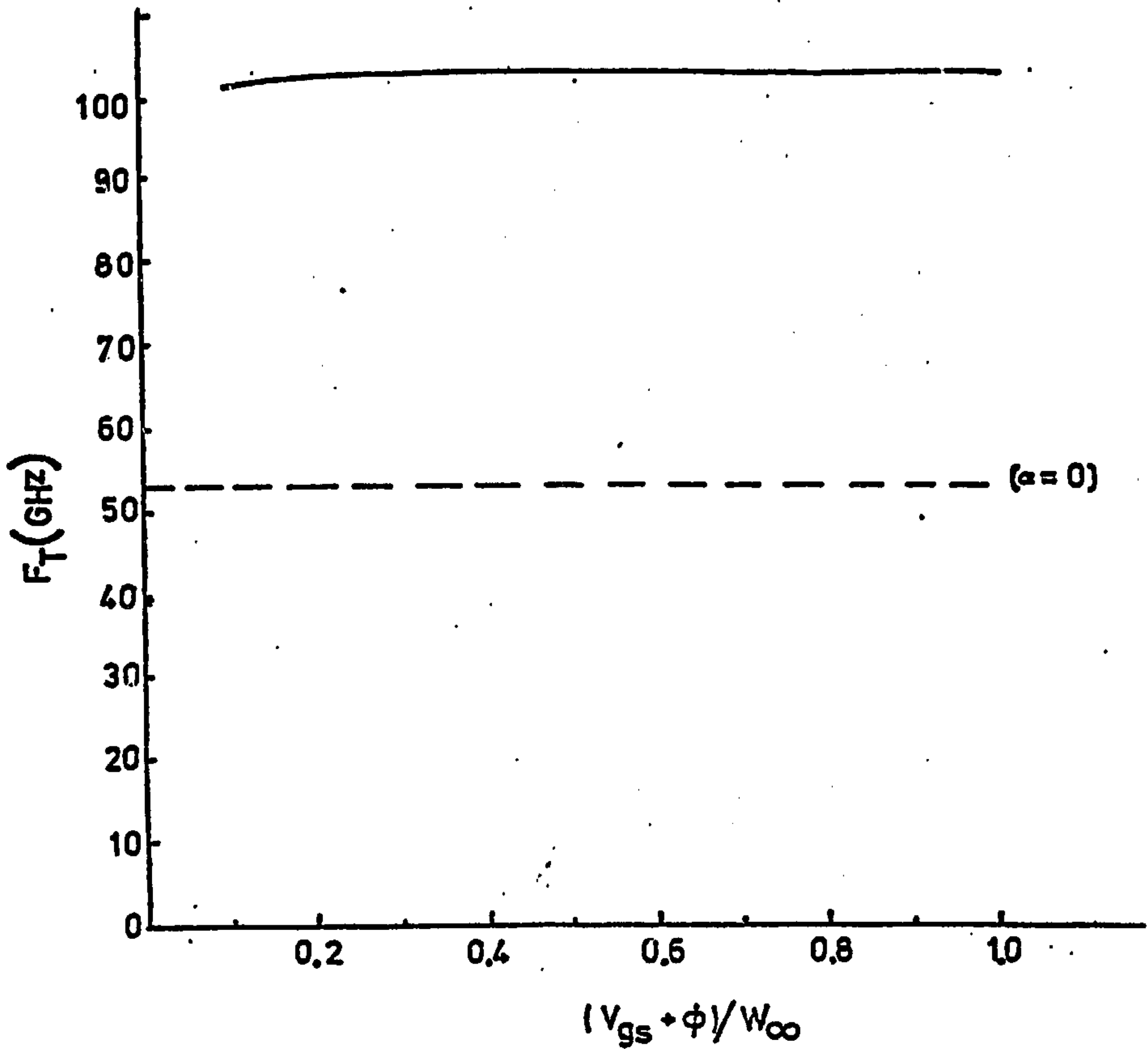
|αℓ|=0.9
|αℓ|=0.1
300
200
100
I(mA)
α>0
α=0
α<0
α>0
α<0
0
.2
.4
.6
.8
1
(Vgs+Φ)/W00



|αℓ| = 0.1
|αℓ| = 0.9
a α > 0
b α = 0
c α < 0
200
150
100
50
g_m (mʊ)
0
.2
.4
.6
.8
$(V_{gs} + \Phi)/W_{00}$
a
b
c



a α>0
b α=0
c α<0
|αℓ| = .9
|ℓ| = .1
Qg
ℓ=.9
ℓ=.1
a
b
c
a
b
.6
.5
.4
.3
.2
.1
1.2
1.0
0.8
0.6
0.4
0.2
0
.2
.4
.6
.8
1.
Cgs (Pf)
Qg (10^-12 C)
(Vgs+ Φ)/ W00



------ |αℓ| = 0.1
—— αℓ = 0.9
F_T (GHZ)
100
90
80
70
60
50
40
30
20
10
0
(α = 0)
0,2
0,4
0,6
0,8
1,0
$(V_{gs} + \phi)/W_\infty$

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