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ELECTRON LITHOGRAPHY STAR DESIGN GUIDELINES

PART I of IV:

THE STAR USER DESIGN MANI

(NASA-CR-170765) ELECTRON LITHOGRAPHY STAR DESIGN GUIDELINES. PART 1: THE STAR USER DESIGN MANUAL Final Report (Mississippi State Univ., Mississippi State.) 171 p HC A08/MF A01

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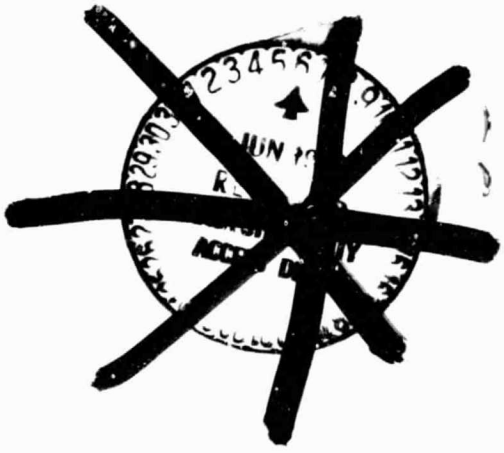

FINAL REPORT - PART I

Submitted to:

National Aeronautics and Space Administration
George C. Marshall Space Flight Center

Date of general release May, 1985

Mississippi State University
Mississippi State, MS 39762

MSSU-EIRS-EE-83-2

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REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER: MSSU-EIRS-EE-83-2

2. GOVT ACCESSION NO.:

3. RECIPIENT'S CATALOG NUMBER:

4. TITLE (and Subtitle): Electron Lithography STAR Design Guidelines Part 1: The STAR User Design Manual

5. TYPE OF REPORT & PERIOD COVERED: Final Report - Part 1 of 4

6. PERFORMING ORG. REPORT NUMBER:

7. AUTHOR(s): J. Donald Trotter: Principal Investigator
Warren Newman: Associate Investigator

8. CONTRACT OR GRANT NUMBER(s): NAS8-33450

9. PERFORMING ORGANIZATION NAME AND ADDRESS:
Mississippi State University
Drawer EE
Mississippi State, MS 39762

10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS:

11. CONTROLLING OFFICE NAME AND ADDRESS:
NASA/MSFC
MSFC, AL 35812
ATTN: Harley R. Hope AP29-C

12. REPORT DATE: August 31, 1982

13. NUMBER OF PAGES: 168

14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office):
ONRRR, Georgia Institute of Technology
206 O'Keefe Building
Atlanta, GA 39332

15. SECURITY CLASS. (of this report): Unclassified

15a. DECLASSIFICATION/DOWNGRADING SCHEDULE:

16. DISTRIBUTION STATEMENT (of this Report):

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report):

18. SUPPLEMENTARY NOTES:

19. KEY WORDS (Continue on reverse side if necessary and identify by block number):
Gate array
STAR
Semicustom
CMOS cell library

20. ABSTRACT (Continue on reverse side if necessary and identify by block number):

This user's design manual describes the STAR design system developed by NASA which enables any user with a logic diagram to design a semicustom digital MOS integrated circuit.

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE
S/N 0102-LF-014-6601

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FINAL REPORT

CONTRACT NAS8-33450

ELECTRON LITHOGRAPHY STAR DESIGN GUIDELINES

PART 1: THE STAR USER DESIGN MANUAL

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NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
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SUMMARY

This user's design manual describes the STAR system developed by NASA which enables any user with a logic diagram to design a semicustom digital MOS integrated circuit. The system is comprised of a library of standard logic cells and computer programs to place, route, and display designs implemented with cells from the library.

Library cells of the CMOS metal gate and CMOS silicon gate technologies were simulated using SPICE, and the results are shown and compared.

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CHAPTER 1. INTRODUCTION TO THE STAR DESIGN SYSTEM

A. Purpose and Philosophy

The Standard Transistor ARray (STAR) design system is a two layer metal interconnect semicustom approach to the design and fabrication of digital MOS integrated circuits. The development of STAR has stemmed from an attempt to incorporate the best features of both custom and semicustom approaches to integrated circuits. The true custom circuit forces the generation of a complete set of masks and full range processing for each design iteration. Characteristics of true custom circuits are high device density, long design cycle times, the maximum number of processing steps, and high costs. In the semicustom circuit, each application forces the generation of a set of interconnect masks only, and limited processing. The basic array is preprocessed and stockpiled until utilized. Characteristics of single metal interconnect semicustom circuits are low device density, short design cycle time, minimum number of processing steps, and low development cost. The STAR system is an attempt to optimize these characteristics into an integrated design system that would yield high device density, short design cycle times, and, in addition, provide for changes in device and processing technology.

The STAR consists of a predefined array of transistors superimposed on a common grid system. To realize a given circuit design requires the transistors be interconnected in the required manner. Since the arrays have been preprocessed to the point of metallization, each STAR circuit design is realized by the creation of three custom masks that

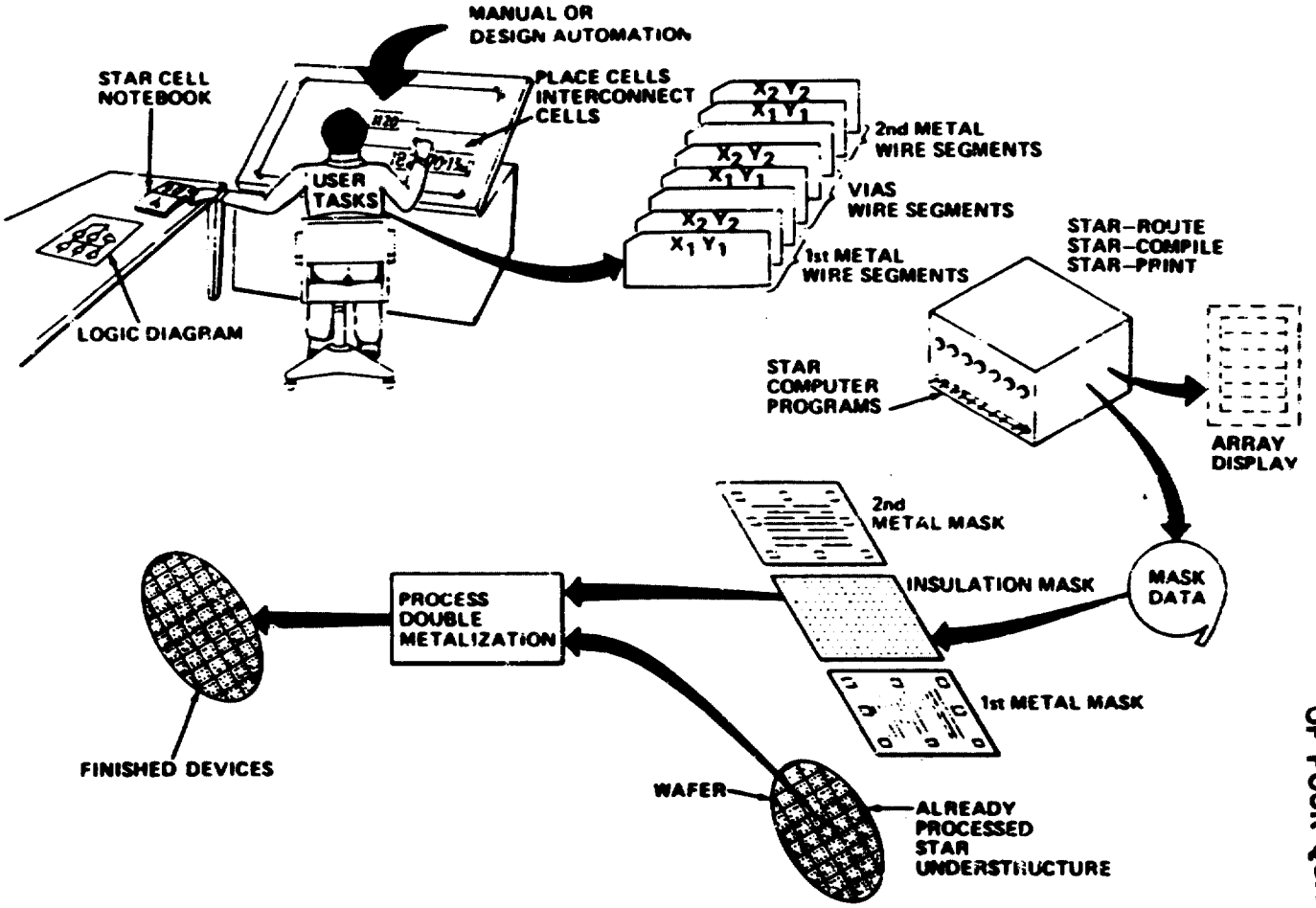

Figure 1.1 STAR Design Procedure

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define the first layer of metal, the VIAS, and the second layer of metal.

A standard-cell approach is used to simplify the specification of the interconnection on the STAR. Hence, the design procedure consists of the selection of standard-cells from a cell library, the placement of these cells on the STAR, and finally the specifications of the interconnection routes between the cells. This procedure can be performed utilizing either manual or computer-aided design techniques. Interconnection data is then input into artwork generation software to create the three custom masks needed for the final processing of the device. The simple grid system provides for adequate displays on line printer output without the need for expensive interactive graphics.

The STAR is designed to accept a wide range of application methods that include manual placement and routing, line printer display, interactive graphics placement and routing, and automatic placement and routing. The software to support these techniques has been developed and is currently being used. Figure 1.1 describes the STAR design procedure.

As technologies change there is a need for the design system to follow the technologies without the need for a major overhaul of the software already developed. The STAR system provides such flexibilty since only the array understructure need be redefined and processed in the new technology. Wire routes, gate locations, and source-drain contacts are maintained at fixed locations. [1]

B. Overview of Manual

The intent of this manual is to enable a user who has no prior experience with the STAR design system or integrated circuit fabrication to design a semicustom digital MOS integrated circuit from a logic diagram. Information is supplied on the structure of the array itself, available logic cells, and the software necessary to complete the design.

The second chapter of this manual describes the transistor array and the cells which currently comprise the Standard Cell Library. Included is an example cell layout and instructions on how to interpret the symbols used to display a STAR layout. A section on creation of new standard cells is also included in this chapter.

The information on how to use the STAR design system software is contained in Chapter 3. The five STAR programs are explained and an example design is taken from the logic diagram phase to the STAR symbolic composite layout. Also included in the third chapter are guidelines for file management on the XEROX SIGMA/7 computer system for the STAR programs.

Chapter 4 gives a brief description of the STAR periphereal circuitry. This section is included for manual layout considerations and for determining the drive capability of the cell.

The last chapter describes how the dynamic performance data for the standard cells were obtained. The parameters for determining the device model are given in tabular form.

The Appendix contains the Standard cell data sheets which includes the logic functions, pin numbers and dynamic data.

CHAPTER 2. ARRAY/STANDARD CELL STRUCTURE AND DESIGN CONSIDERATIONS

A. Introduction

This chapter describes the physical structure of the Standard Transistor Array and how it is interconnected to implement a logic function. The concept and format of the Standard Cell Library is explained, as well as the method for adding new cells to it. Each of the cells presently in the Library are explained in detail. A section is presented on items to consider before choosing the logic cells used in a design. Also included is a section on interpreting the symbolic display of a STAR cell.

B. Array Description

The Standard Transistor Array consists of alternating rows of P and N type devices that have been designed around a common grid system. The array has been defined in CMOS-bulk metal gate, CMOS-SOS silicon gate, CCL (Closed Contoured Logic)-SOS, and CCL-bulk MOS technologies. Initial emphasis has been placed on the CMOS-bulk and CMOS-SOS technologies with arrays having been processed in these technologies. Figure 2.1 shows the basic array elements and the grid structure of these two technologies.

The grid used in the array has been initially established at 0.8 mil to accomodate 0.5 mil metal lines and 0.3 mil VIAS. The array density is 7.68 mil^2/device in the basic element. The gates of the devices, source and drain contacts, and interconnecting routes are

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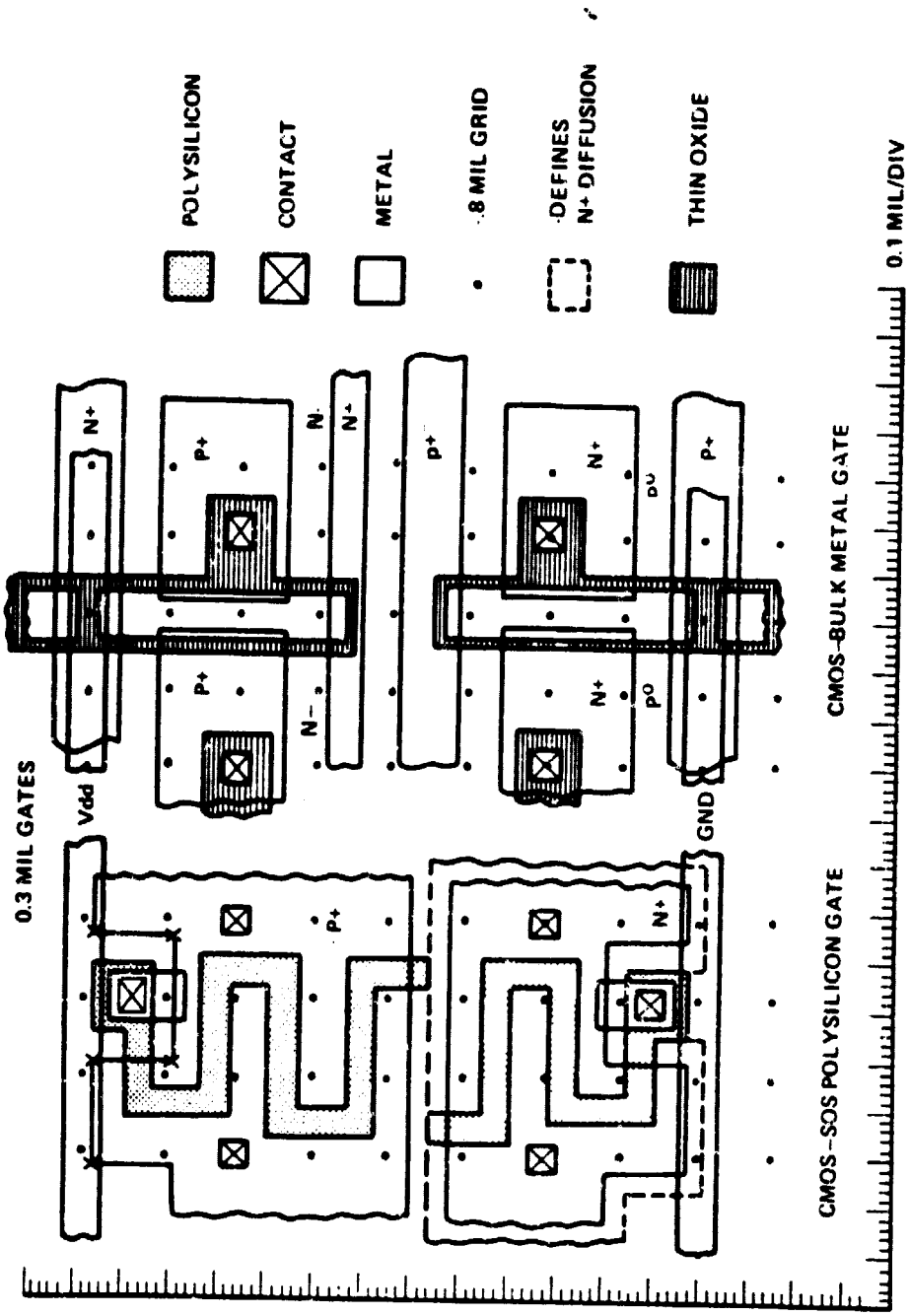

Figure 2.1 STAR CMOS-SOS and CMOS-Bulk Array Layouts

restricted to the grid system which is organized to provide local and global wiring channels to efficiently interconnect the devices. In general, the vertical routing is done in the first level metal and the horizontal routing in second level metal. There are three horizontal routing channels between the P and N devices that are used for local routing or to create logic cells. Two horizontal global channels exist above and below the power buses, for a total of four, to allow for interconnection to other logic cells. In the vertical direction, a global channel exists one grid to the left of each gate. All of the possible routing channels are illustrated in Figure 2.2.

The devices within the array are sized for logic loads and are connected in parallel to create buffers for driving large off-chip loads. The array is surrounded by multiple use pad cells that are convertible into input, output, and power pads by the proper placement of wiring segments within the pad cell as it is routed. More information on the STAR periphery is given in Chapter 4.

Three sizes of the array have been created that include a 384 transistor (90x80 mils), a 1728 transistor (162x131 mils), and a 5264 transistor (254x208 mils) version. The three arrays are shown in Figures 2.3, 2.4, and 2.5 respectively.

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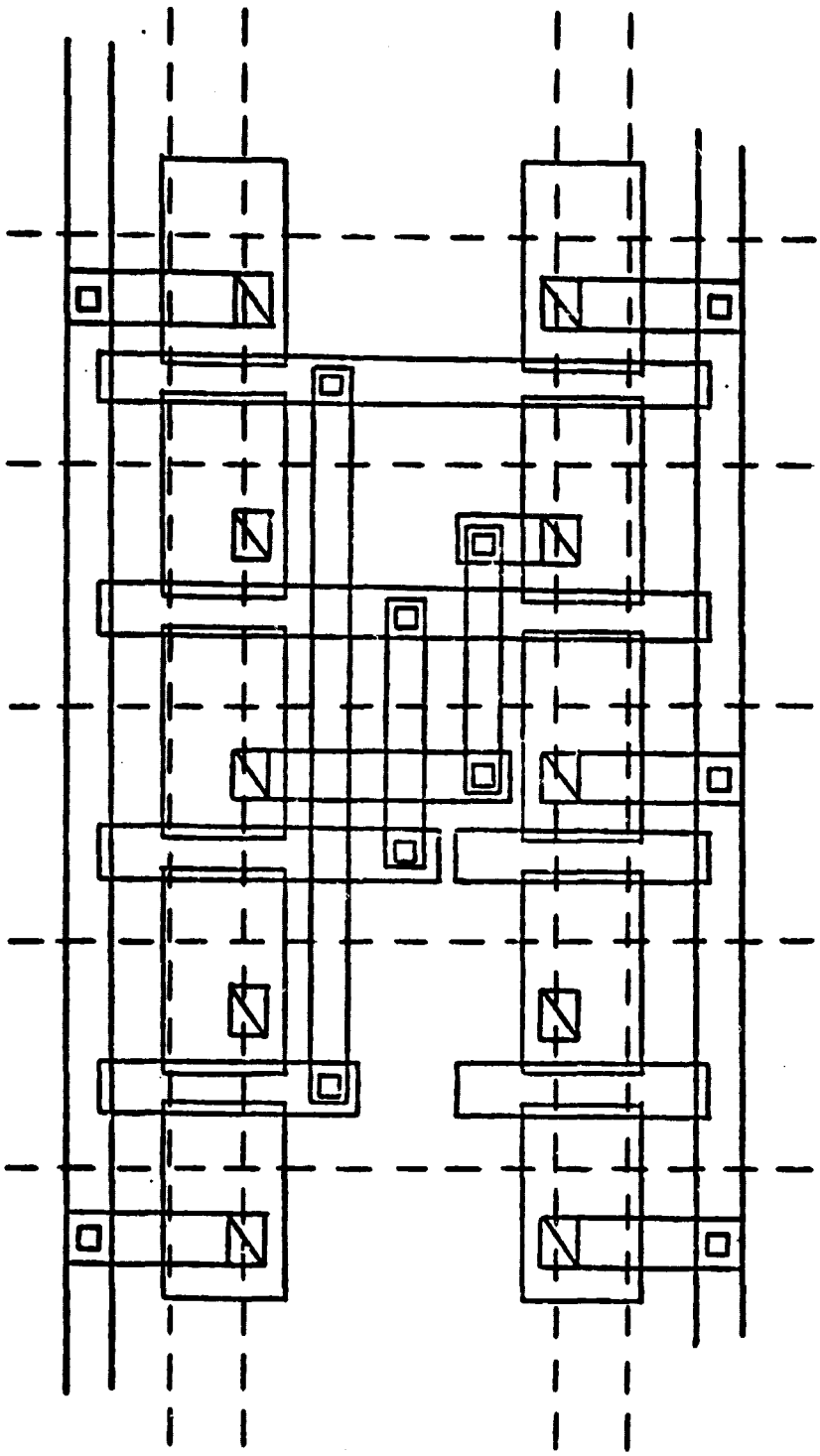

---- Global Path Centerline

Figure 2.2 STAR Logic Cell Global Paths

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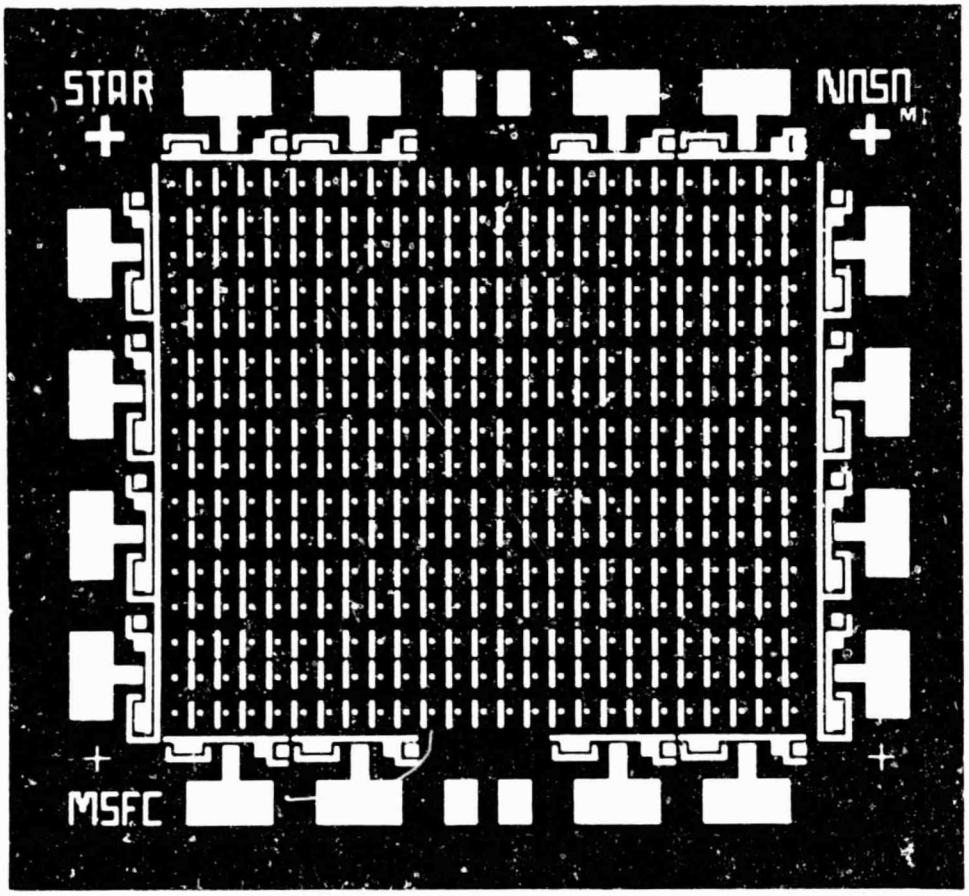

384 TRANSISTORS 90 X 80 MILS

16 INPUT/OUTPUT PADS

Figure 2.3 384 Transistor STAR

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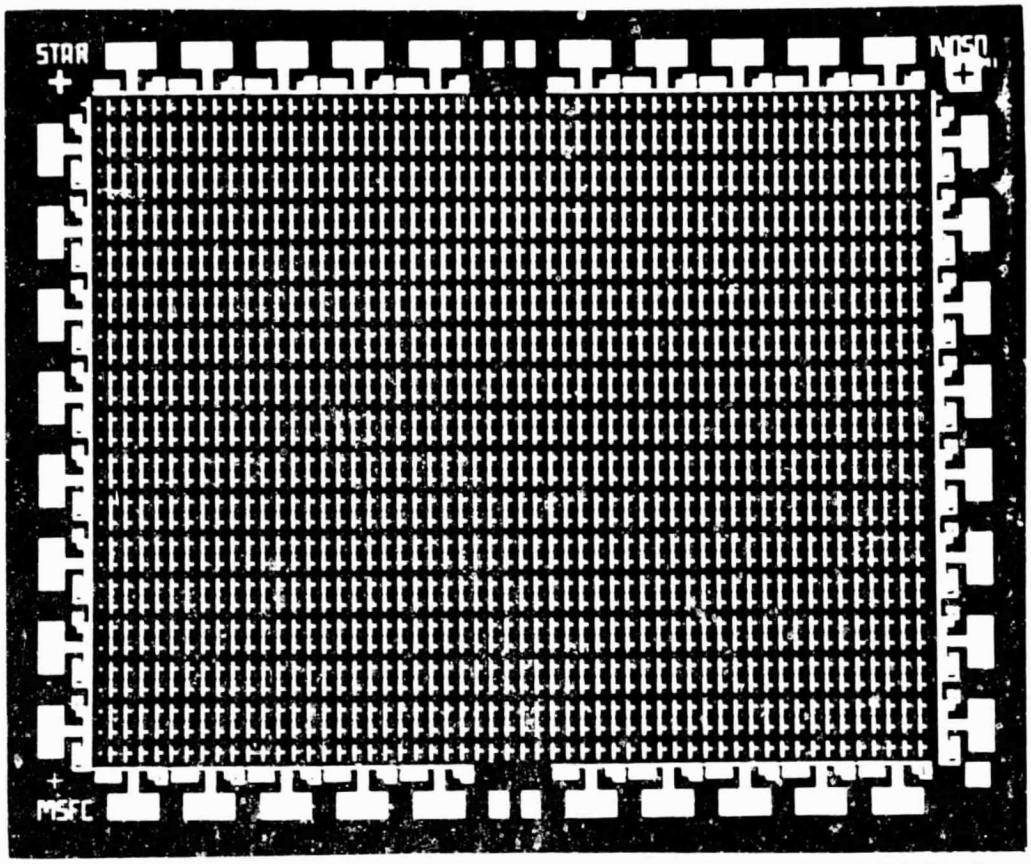

36 INPUT/OUTPUT PADS

Figure 2.4 1728 Transistor STAR

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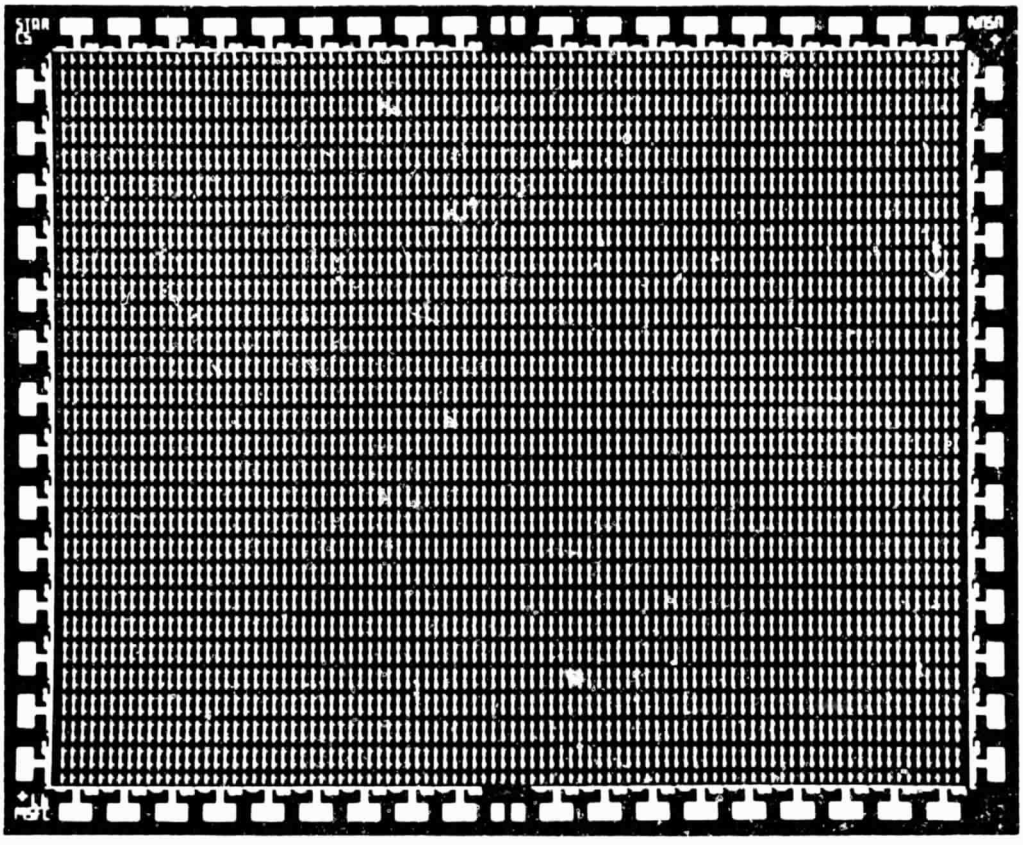

Figure 2.5 5264 Transistor STAR

C. STAR Standard Cell Library

A logic cell family for the STAR, called the Standard Cell Library, has been created and put on disc storage. It consists of the normal building blocks for digital logic design. However, the library is open-ended to allow the user to define and design new cells to meet particular requirements in the most efficient manner possible. Creation of new cells will be discussed in a later section of this chapter.

Figure 2.6 illustrates an example of a typical logic cell contained in the library. It shows the CMOS-Bulk metal gate array layout and a two-input NOR STAR cell configuration. Each cell begins and ends with source connections to their respective power buses and the cell extends horizontally utilizing the number of transistors required for the logic. In the example shown, eight transistors (or four transistor pairs) are required. It can be seen how the channels are used to make intracell connections.

The software working form of the library contains the wiring segments of the cell in X-Y coordinates along with a segment identifier for each segment. Also, a reference point is established at the cell's starting point on the ground bus, with this point being used as the placement point for reuse of the cell. This information is utilized by the STAR automatic routing software to correctly route user specified logic cell interconnecting nets. The format of the Standard Cell Library is shown in Figure 2.7 for the two-input NOR cell, which was pictured in Figure 2.6.

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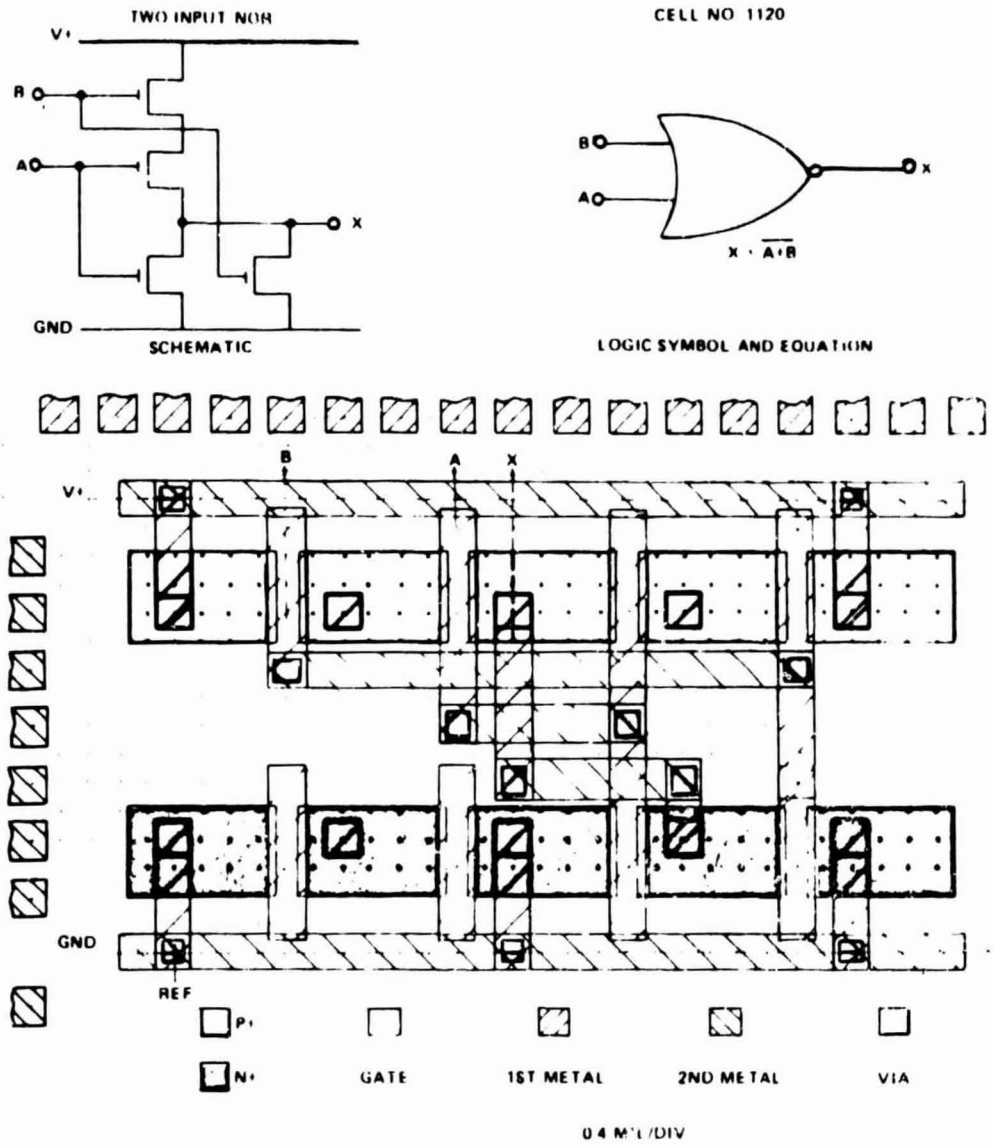

Figure 2.6 Typical STAR Logic Cell

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LEVEL NO.	X1	Y1	X2	Y2	SEGMENT IDENTIFIER
7	0	8.0	0	8.0	POO1
6	0	8.0	0	6.0	POO1
6	0	2.0	0	0.0	C112
7	0	0.0	0	0.0	C112
6	2	7.5	2	5.0	PLUS
6	2	7.0	3	7.0	PLUS
6	3	7.0	3	8.0	PLUS
7	3	8.0	3	8.0	PLUS
6	2	3.0	2	0.5	GNND
6	2	1.0	3	1.0	GNND
6	3	2.0	3	0.0	CNND
7	3	0.0	3	0.0	GNND
6	9	2.0	9	0.0	GNND
7	9	0.0	9	0.0	GNND
6	9	8.0	9	6.0	PLUS
7	9	8.0	9	8.0	PLUS
6	5	7.5	5	0.5	POO2
6	8	7.5	8	0.5	POO2
6	3	6.0	3	4.0	POO3
7	3	4.0	3	4.0	POO4
8	3	4.0	6	4.0	POO4
7	6	4.0	6	4.0	POO4
6	6	4.0	6	2.0	POO4
6	6	6.0	6	6.0	P333

Figure 2.7 Standard Cell Library Format

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D. STAR Symbolic Display

Because the STAR system was designed to display on line printer output without the need for expensive graphics, the output must be symbolic. Furthermore, the symbols used must be universal to line printers. To more fully interact with the STAR system, such as verifying design results or creating a new logic cell, the user must be able to interpret this symbolic output.

Figure 2.8 illustrates the symbolic display of the two-input NOR cell 1120 shown in Figure 2.6. This figure was displayed using the data from the STAR cell library, as shown in Figure 2.7. Figure 2.8a shows the symbolic layout with the cell number (the reference point) in the lower left-hand corner in the vertical direction (C112). Pin numbers and bus connections are also displayed. P001 is always the first connection to the plus supply. Pin numbers greater than 100 denote internal connections (for example, P333). The two inputs are P002 and P003 and the output of the cell is P004. PLUS and GNND refer to connections to the plus and ground buses, respectively.

Figure 2.8b depicts the same layout, but without the pin numbers. The p and n diffusions are on grid rows 6 and 2, respectively. Transistors are then formed on every third grid column, starting at column 2. The power buses are represented by the rows of equal signs (=). The I's represent the top layer metal, while sixth layer metal is shown as a line of dashes (---). Where these two metal lines cross but do not form a connection is given by a plus sign (+). A connection between the two metal lines or a connection from a metal line to a power bus (called a VIA) is represented by a #.

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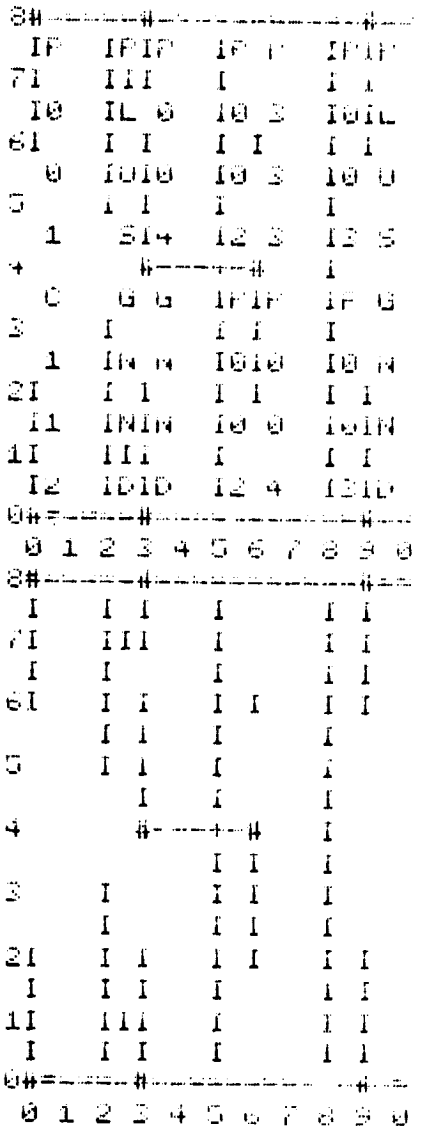

(a) Line Segments and Pin Numbers

(b) Line Segments Only

Figure 2.8 STAR-CELL Symbolic Display

The line segment data for the layout shown in Figure 2.8 was obtained from the file shown in Figure 2.7. The first column indicates the level of the segment. Level 6 is horizontal metal (---), level 7 is a VIA (#), and level 8 is the top layer metal (I). The next four columns represent the X and Y coordinates of the endpoints of the segment. The next column is the segment identifier. For example, on the first line, level 7 indicates a VIA and it is located from coordinates 0,8 to 0,8, which is a connection of P001 to the plus supply.

When a design is displayed using the STAR-PRINT program, the output will resemble Figure 2.8a, except net numbers will also be included, and the power buses will be represented by dashes (---). Nets are connections to other cells and usually occupy the global channels. The net identifiers all begin with an N, such as N010.

E. Creating A New STAR Cell

If the need arises for a cell which is not contained in the Standard Cell Library, the user can easily create it and add it to the library.

After the logic function of the new cell has been determined, the circuit schematic should be drawn like the schematics on the data sheets and the example shown in Figure 2.9. If an existing cell is similar to the new cell, it can be used as the format for the layout of the new cell or modified to form the new cell.

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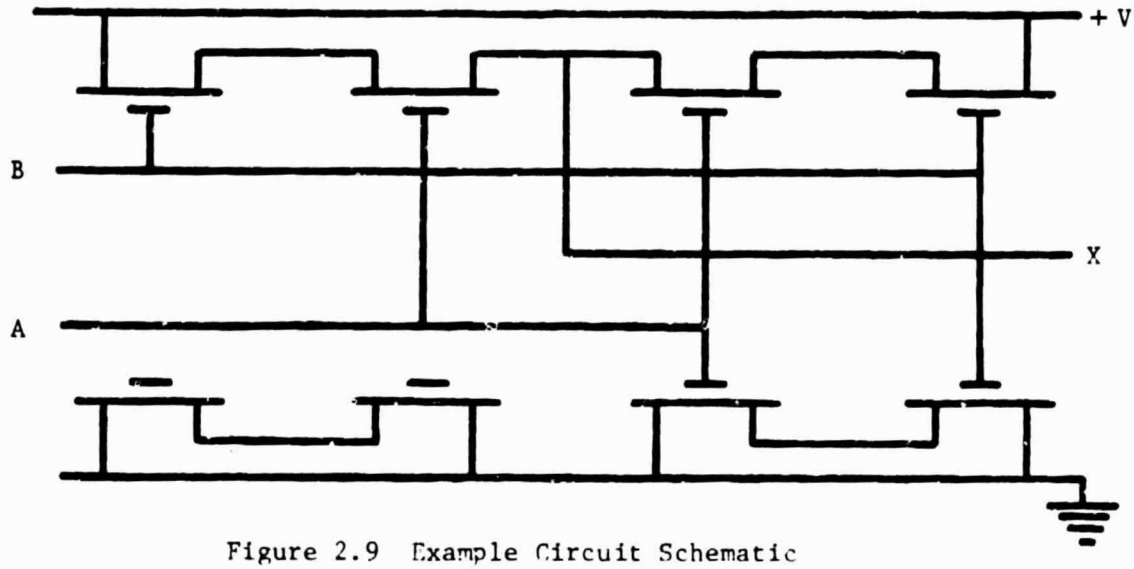

Figure 2.9 Example Circuit Schematic

Using the grid coordinates discussed in the preceding sections, the layout of the cell should next be developed, as illustrated in Figure 2.6. VIAS should be clearly marked so as not to be mistaken as crossovers. The levels of interconnection should also be represented differently (such as crosshatching).

Each of the line segments should be identified as discussed the preceding section and shown in Figure 2.10. It should be made certain that the cell reference point and POO1 are clearly identified.

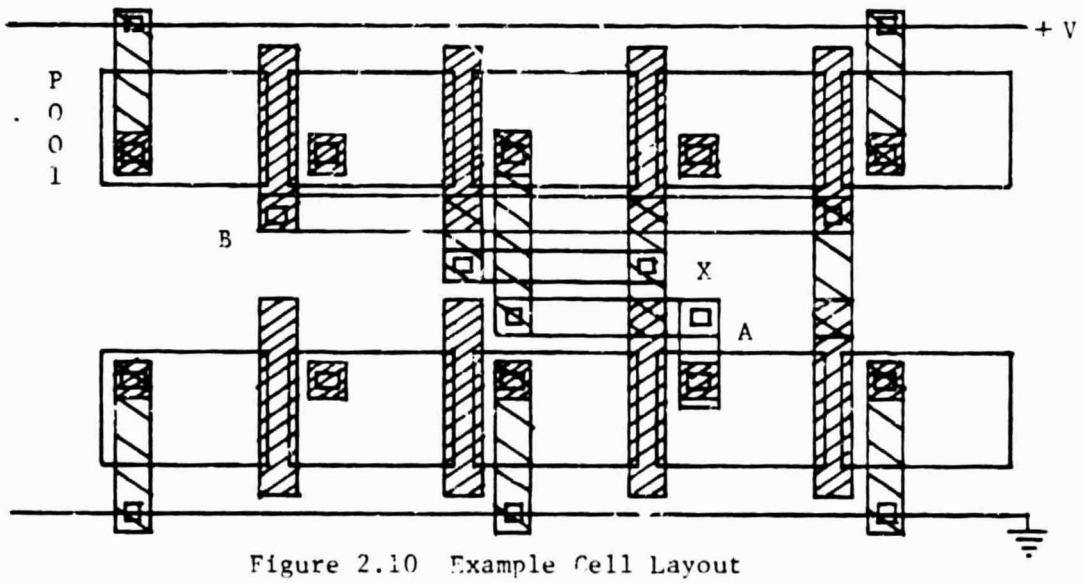

Figure 2.10 Example Cell Layout

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A tabular listing of the line segments should now be compiled, including the X and Y starting and stopping coordinates as partially shown below.

NO.	LEVEL NO.	X1	Y1	X2	Y2	SEGMENT IDENTIFIER
1	7	0	0.0	0	0.0	C112
2	6	0	0.0	0	2.0	C112
3	6	0	6.0	0	8.0	POO1
4	7	0	8.0	0	8.0	POO1
⋮	⋮	⋮	⋮	⋮	⋮	⋮

Creating this listing requires knowing the line segment's level and its X and Y coordinates. By comparing Figure 2.7 with Figure 2.8, the format for representing the line segment by coordinates should become clear. Only four letters are allowed for the segment identifiers.

When it has been made certain that the list includes each line segment of the design, the cell is ready to be entered into the Standard Cell Library. A computer program has been created to facilitate the addition of new cells, or the modification and display of existing cells. The program is named STARCEL2 and is implemented in the XEROX BASIC programming language, which is explained in more detail in Chapter 3.

To execute this program, the user must first enter the BASIC subsystem. After gaining access to a time-sharing terminal, the user must log-on the SIGMA computer. When the computer returns a prompt (!), indicating that it is ready for an executive-level command, the user types the word BASIC (followed by a carriage return) as shown below.

```
!BASIC
 VER.DØ3
>
```

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BASIC then responds with the version and a > to indicate that it is ready to accept input from the user terminal. The user should then type the following commands.

```
>LOAD STARCEL2
>WID 132
>SET $=132
>RUN
```

BASIC will respond with a message similar to the one below.

```
10:17  MAY 18  STARCEL2 ...
HAVE YOU SET $=132 AND WID 132
CELL-IN CELL-OUT L LA LD D QUAD LABEL
?
```

The last line of text are the options available to the user of the program, which are defined below.

CELL-IN	INPUT EXISTING STAR CELL XXXX
CELL-OUT	OUTPUT NEW OR EXISTING STAR CELL XXXX
L	PROVIDE LISTING OF LINE SEGMENT DATA
LA	ADD LINE XX AND DATA
LD	DELETE LINE XX
D	PROVIDE SYMBOLIC DISPLAY OF STAR CELL
QUAD	INCLUDE QUADRANT X IN DISPLAY
LABEL	DELETE PIN NUMBERS FROM QUADRANT X

The cells are displayed as shown in Figure 2.8 and because some cells are wider than 80 columns, each half is again halved, creating quadrants (0-3).

Therefore, to create a new cell or modify an existing one, the user must first input an existing STAR cell. An example is shown below. The lines in italics are printed by the computer.

?CELL-IN 1120

? (carriage return twice)

?QUAD 0

CELL-IN CELL-OUT L LA LD D QUAD LABEL

? (carriage return)

? QUAD 1

CELL-IN CELL-OUT L LA LD D QUAD LABEL

? (carriage return)

CELL-IN CELL-OUT L LA LD D QUAD LABEL

? LABEL 1

CELL-IN CELL-OUT L LA LD D QUAD LABEL

The above commands input STAR cell 1120 and quadrants 0 and 1 are all that are needed to display it. The command LABEL 1 removes the pin numbers from quadrant 1.

The user can now display the cell as shown in Figure 2.8 or produce a listing of the line segment data similar to Figure 2.7. A display is produced in the following manner.

?D

? (carriage return)

The following command will produce a listing of the line segment data.

?L

? (carriage return)

This listing can be modified as necessary to create the new cell by using the LA and LD commands. To delete an existing line, all that is needed is LD and the line number. For example, ?LD 3 will delete line 3. The following example illustrates how to add a line of data.

```
?LA 3 6 0 6.0    0 8.0    P001
```

After all necessary line segments have been modified or added, the new cell is ready to be output. The following command will output the new cell and display both halves.

```
?CELL-OUT XXXX
```

The new cell is now part of the Standard Cell Library, and the user can exit BASIC or create another new cell.

To exit from BASIC, the user should depress the BREAK or ESC key four times and wait for the executive level prompt (!).

At this point, another processor may be invoked that operates under the Batch Time-Sharing Monitor (BTM) or Control Program - Five (CP-V) control, or the user may vacate the terminal by typing

```
?BYE (or OFF under CP-V) .[8]
```

F. Design Considerations[1]

When determining the STAR logic cells that will be included in the design, three basic items must be considered:

---

[1]The following material is based on information found in NASA Technical Memorandum 78126 "CMOS Bulk Metal Design Handbook".

1. Method of cell implementation; either functional logic or transmission gate logic. The guidelines are given in Section F.3.

2. On-chip and off-chip loading requirements versus the drive capability of each cell.

3. Unused (floating) inputs are "tied off" correctly.

Before the proposed design is submitted for an initial computer placement run, critical signal paths should be found and examined. The delay characteristics as specified on the data sheet of each cell are used to locate and evaluate possible race conditions. An example illustrating the use of these characteristics is presented in Figure 2.11 and discussed in the following section.

1. Delay Characteristics. After selecting the standard cells required to implement the desired logic, analyses can be made of the critial path delays, race conditions, and loading conditions. This begins by calculating the total capacitance associated with each node of the signal path. The total capacitance is defined as the sum of the input capacitance of all gates connected to this node and the metalization capacitance loading associated with the intercell wiring connections. The input capacitance for each cell may be obtained directly from the data sheets contained in the Appendix. However, the interconnection capacitance can only be determined after the routing is completed. In order to develop a first order estimate of propagation delays to establish feasibility of a logic design, one can assume an interconnection capacitance which is proportional to the fan-out. Doubling the total input capacitance is suggested to cover the interconnection capacitance. If the cell is driving an off-chip load, then this load must also be included. The example in Figure 2.11 aids in illustrating this procedure.

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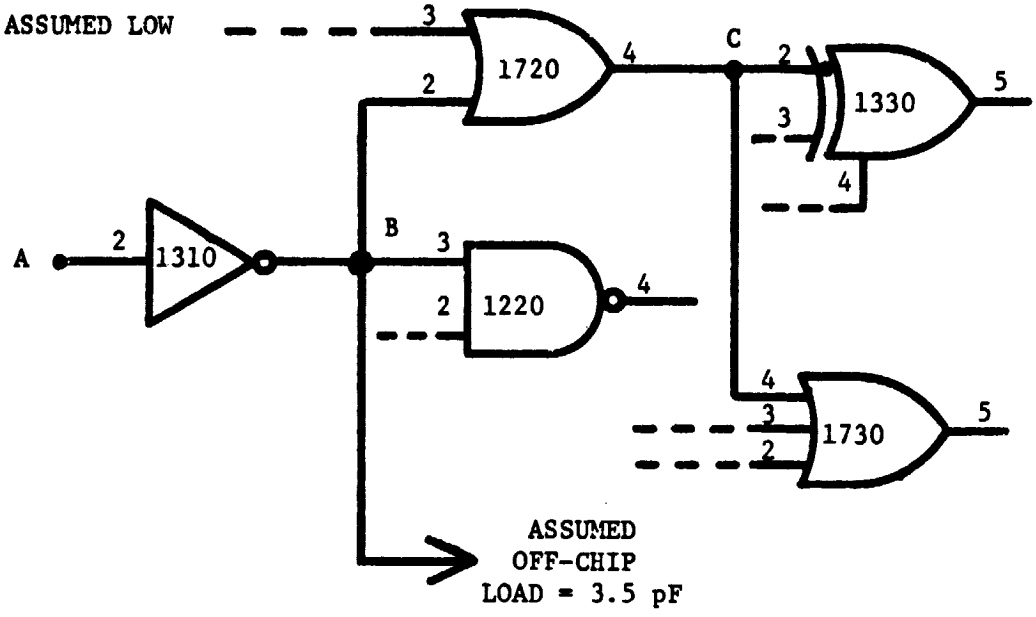

(a) LOAD AT NODE B:	ABS. (pF)	NORM.
INPUT OF CELL NO. 1720 (PIN 2)	0.56	1.00
INPUT OF CELL NO. 1220 (PIN 3)	0.56	1.00
INTERCONNECT CAP. (2 x INPUT CAP.)	1.12	2.00
ASSUMED OFF-CHIP LOAD	3.50	6.25
TOTAL	5.74	10.25

(b) LOAD AT NODE C:	ABS. (pF)	NORM.
INPUT OF CELL NO. 1730 (PIN 4)	0.56	1.00
INPUT OF CELL NO. 1330 (PIN 2)*	2.42	4.32
INTERCONNECT CAPACITANCE	5.96	10.64
TOTAL	8.94	15.96

*IF DRIVING A STANDARD LOAD

(c)

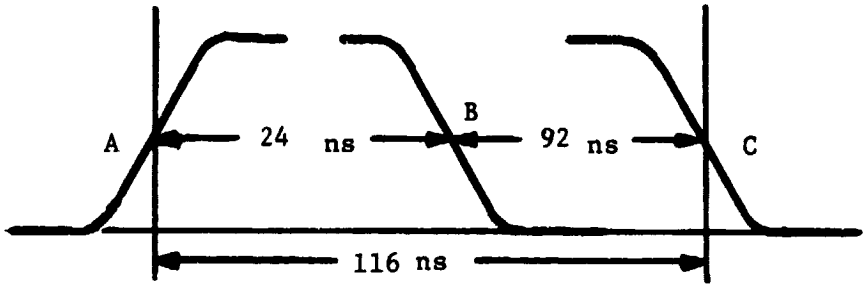

Figure 2.11 Example Illustrating Delay Calculations

By referring to the data sheet for the buffer inverter cell (1310), assuming a five volt supply, and using the normalized load of 10.25, the calculations shown in Figure 2.12 were arrived at. The propagation (stage) delay (node A to node B) was estimated to be 24 ns. Similarly, by referring to the data sheet for the two-input OR gate (1720), and using the normalized load of 15.96 with a five volt supply, the calculations in Figure 2.13 were obtained. Therefore, the propagation delay (node B to node C) was estimated to be 92 ns.

The overall delay from node A to node C is then the sum of these two delays, or 116 ns.

2. Off-Chip Loading. An illustration of the off-chip capacitance is shown in the following tabulation for a system using ceramic dual-in-line packages.

TYPE of Off-Chip Load	Value
Each ceramic in-line package (24)	3.5 pF
Each ceramic in-line package (40 pin)	5.5 pF
Each socket terminal	1.0 pF
All interchip (point to point with no ground plane wiring)	0.7 to 1.7 pf/in.
Each input/output board pin[2]	3.0 pF
Each input/output board pin socket	5.0 pF

[2]This measurement pertains to an 80 pin, 0.0625 in. thick commercially available board.

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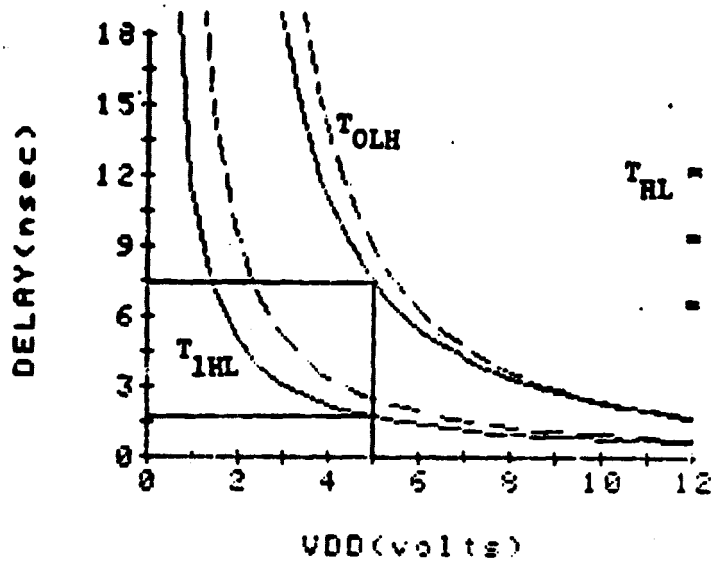
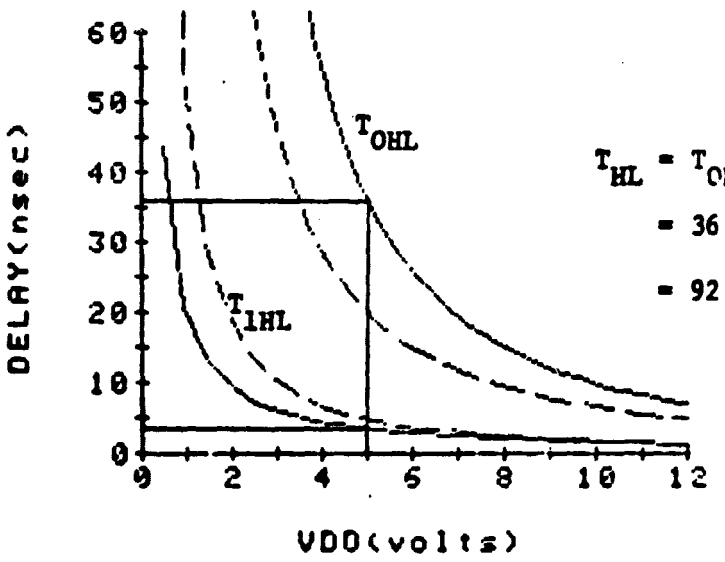


$$T_{HL} = T_{OHL} + T_{1HL}(F/O)$$
$$= 7.5 + 1.6(10.25)$$
$$= 24 \text{ ns}$$

Figure 2.12. Delays for 1310 with $V_{DD} = 5$.



$$T_{HL} = T_{OHL} + T_{1HL}(F/O)$$
$$= 36 + 3.5(15.96)$$
$$= 92 \text{ ns}$$

Figure 2.13. Delays for 1720 with $V_{DD} = 5$.

From the preceding values it is seen that in addition to interchip wiring capacitance and on-chip laoding capacitance, an additional 5.5 pF (or 3.5 pF) must be included each time the signal goes on or off a chip.

3. Transmission Gates and Functional Logic. The CMOS Standard Cell Library is implemented with circuits designed using either a functional logic (FL) and/or a transmission gate (TG) relay logic approach. Each method has its unique characteristics and advantages, some of which are as follows:

A. Standard Cells Implemented with Functional Logic

1) The outputs of functional logic cells may not be tied together (the wired OR).

2) Each circuit provides, virtually, electrical isolation between output and input nodes - a noise immunity approximately equal to 20 to 40 percent of the supply voltage - varies with logic function and fan-in.

3) Each circuit amplifies the input waveform and may therefore be used to reshape the signal waveform.

4) The inherent nature of functional C-MOS logic is to provide one signal inversion for each stage of circuitry. Therefore, when a cell implemented with functional logic supplies the AND function, it must contain at least two levels of circuitry; the invert or NAND function requires one level of circuitry.

B. Standard Cells Implemented with Transmission Gate Logic

1) The outputs of transmission gate cells may be tied together provided that no two transmission devices with outputs connected are placed in the conducting state at the same time.

2) Transmission gate logic does not provide signal amplification. Therefore, when cascading several such devices, a functional logic circuit may be placed between them. This suggestion is based primarily on the need to maintain sharp waveforms and fast stage delays. It is not necessary or required to ensure proper operating levels.

3) In contrast to functional logic, transmission gate logic provides noninversion functions.

C. Drive Capability The Standard Cell Library can be divided into four groups of circuits, with members of each group having essentially the same dynamic and/or static drive capability. This means that cells in the same group will have approximately the same output rise or fall times for the same load.

. Group I cells are characterized by those circuits implemented with transmission gate logic. Cells in this group have no drive capability of their own. Each cell may be considered to be a relay circuit that has a finite conducting resistance and an infinite "off" resistance.

- Group II cells are characterized by output circuitry implemented with standard size nonbuffered transistors. This group comprises the bulk of the standard cell family. Generally these cells should be used when their total output load is less than 8 pF. Otherwise they should be followed with a buffering circuit.
- Group III cells feature output transistors roughly three times as large (powerful) as those of Group II. These cells should be used when their total output load is less than 25 pF but greater than 8 pF.
- Group IV presently contains only one cell. This cell serves as a buffer for all loads greater than 25 pF.

As a guide to the user, each cell's drive capability is given in the cell descriptions, and listed in Table 2.1. I indicates that the cell is in Group I, II indicates that the cell is in Group II, III indicates that the cell is in Group III, and IV indicates that the cell is in Group IV.

E. FLIP-FLOPS. The flip-flops which consist of two levels of logic require two clock transitions to transfer the data from input to output. The minimum values given for the pulse widths are for a ten volt supply and a single load. If more loading is required or a lower voltage supply is used, the pulse width should be longer. This can be determined from the data sheets.

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CELL NO.	CELL FUNCTION	CELL WIDTH (GRIDS)	CELL WIDTH (MILS)	IMPLEMENTATION	DRIVE GROUP
1120	2-INPUT NOR GATE	3	2.4	FL	II
1130	3-INPUT NOR GATE	4	3.2	FL	II
1140	4-INPUT NOR GATE	5	4.0	FL	II
1220	2-INPUT NAND GATE	3	2.4	FL	II
1230	3-INPUT NAND GATE	4	3.2	FL	II
1240	4-INPUT NAND GATE	5	4.0	FL	II
1300	INVERTING BUFFER	2	1.6	FL	III
1310	SINGLE BUFFER INVERTER	2	1.6	FL	III
1330	2-INPUT TRANSMISSION GATE	5	4.0	TG	I
1360	TRIPLE BUFFER INVERTER	6	4.8	FL	IV
1520	DOUBLE BUFFER INVERTER	4	3.2	FL	III
1620	2-INPUT AND GATE	4	3.2	FL	III
1630	3-INPUT AND GATE	5	4.0	FL	III
1640	4-INPUT AND GATE	6	4.8	FL	III
1720	2-INPUT OR GATE	4	3.2	FL	III
1730	3-INPUT OR GATE	5	4.0	FL	III
1740	3-INPUT OR GATE	6	4.8	FL	III
1820	D TYPE MASTER/SLAVE FLIP-FLOP	14	11.2	FL	II
1810	D TYPE FLIP-FLOP	8	6.4	FL	II
1900	PROGRAMMABLE D-TYPE MASTER/SLAVE FLIP-FLOP	12	9.6	FL	II
1910	PROGRAMMABLE D-TYPE MASTER/SLAVE FLIP-FLOP WITH RESET	13	10.4	FL	II
1920	D-TYPE MASTER/SLAVE FLIP-FLOP WITH RESET	15	12.0	FL	II
2310	EXCLUSIVE-OR	5	4.0	FL	II
9100	SIDE INPUT PAD	10	8.0	N/A	N/A
9110	LEFT OUTPUT PAD	10	8.0	N/A	N/A
9120	RIGHT OUTPUT PAD	10	8.0	N/A	N/A
9200	TOP/BOTTOM INPUT PAD	10	8.0	N/A	N/A
9210	TOP/BOTTOM OUTPUT PAD	10	8.0	N/A	N/A

Table 2.1. STAR Metal-Gate CMOS Standard Cell Library Listing

F. Floating Inputs. All inputs should be connected either to the output of another gate or to one of the low impedance signal levels. A floating input can result in improperly functioning gates.

G. STAR Logic Cells

This section describes each of the standard cells in the present Standard Cell Library. More inclusive data sheets that describe the function, node capacitance, and performance of each cell are included in the Appendix. The current CMOS standard cells are listed in Table 2.1, and the cell descriptions follow. The table gives the cell number, the cell function, its width in grids and mils, and the logic used to implement the cell.

1. TWO-, THREE-, AND FOUR-INPUT NOR's (1120, 1130, and 1140).

Two-, three-, and four-input NOR's (1120, 1130, and 1140) are group II functional circuits that provide the logical NOR operation. The four-input NOR cell has the largest device delay in this group. It may therefore be advisable to buffer the output of this cell before the total output node capacitance reaches 8 pF.

2. TWO, THREE-, AND FOUR-INPUT NAND's (1220, 1230, and 1240).

Two-, three-, and four-input NAND's (1220, 1230, and 1240) are Group II functional circuits that provide the logical NAND operation. The four-input NAND cell has the largest device delay in this group. It may be advisable to buffer the output of the cell before the total output node capacitance reaches 8 pF.

3. SINGLE INVERTING BUFFER (1300).

Single inverting buffer (1300) is a Group II cell that provides the logical signal inversion with a single level of circuits. It is recommended for use with loads of less than 8 pF.

4. BUFFER INVERTER (1310).

Buffer inverter (1310) is a Group III functional circuit that provides the logical signal inversion and should be used where buffering is required (for loads greater than 8 pF). Cells 1310 and 1520 are interchangeable and logically identical.

5. SINGLE CLOCK, DUAL TRANSMISSION GATE - MULTIPLEXER (1330).

This cell furnishes the designer with a 2 to 1 electronic relay switch. It is mechanized with transmission gate devices and therefore is a Group I circuit. When the control signal C is low (or 0), the relay path B-X is conducting. When the control signal C is high (or 1), the relay path A-X is conducting. Hence, a high control signal connects the "dotted" input terminal to the output. Because the output node X is always connected to one and only one input node, the output is always defined. Therefore it is generally not possible to tie the output of this cell to the output of another cell. Although the cell functions as a nonlinear resistor, when conducting the effective "on" resistance may be accurately represented by a fixed 1 to 2 kΩ resistor.

6. TRIPLE BUFFER INVERTER (1360).

Triple buffer inverter is a Group IV functional circuit that provides the logical signal inversion and should be used in those cases where a large amount of buffering is required (for loads much

greater than 25 pF). Cell 1360 is the largest buffering circuit presently in the library.

7. DOUBLE BUFFER INVERTER (1520).

This cell is also a group IV functional circuit that provides the logical signal inversion, but it should be used in buffering intermediate loads that do not greatly exceed 25 pF.

8. TWO-, THREE-, AND FOUR-INPUT AND's (1620, 1630, and 1640).

These provide, with two stages of functional circuitry, the logical AND operation. Each cell is a member of drive capability Group III and should therefore be used for loads less than 25 pF. Cells 1620, 1630, and 1640 are topologically interchangeable with cells 1220, 1230, and 1240. This permits the interchange of NAND and AND functions at later stages in the array design.

9. TWO-, THREE-, AND FOUR-INPUT OR's (1720, 1730, and 1740).

These provide, with two stages of functional circuitry, the logical OR operation. Each cell is a member of drive capability Group III and should therefore be used for loads less than 25 pF. Cells 1720, 1730, and 1740 are topologically interchangeable with cells 1120, 1130, and 1140. This permits the interchange of NOR and OR functions at later stages in the array design.

10. D-TYPE MASTER/SLAVE FLIP-FLOP (1820).

This cell uses functional circuitry to provide two levels of logic in a master/slave configuration. When control signal C makes a transition from low to high, the logical inversion of the data on the D input line is transferred to the output of the master portion. At this time, the output (or slave) portion is isolated

from the input (or master) portion by means of the AND gate whose output is held low by the inversion of the control signal.

When control signal C goes from high to low (1 to 0), the complement of the data stored in the master will then be transferred to the output of the slave. The slave portion will then hold the data at the output until the next high to low transition of the control signal C.

In summary, the information on input line D may be loaded into the master when the signal on control line C goes high. The information stored in the master is transferred to the slave, and hence the output, by bringing the control line low. Therefore, on one cycle of the control signal (or clock), the data placed on the D input can be transferred to the output of the flip-flop while undergoing two logical inversions.

The minimum recommended positive-going clock pulse width to load the master is 75 ns. The minimum negative clock width is specified to be 50 ns. It is also recommended that the data line be held constant for at least 50 ns prior to and succeeding all clock transitions.

11. D-TYPE FLIP-FLOP (1830).

This cell has been implemented with functional logic and provides an AND-OR type configuration. While control line C is high, the output of the cell remains the same, regardless of the input placed on data line D. However, with the control line low, the output of the cell will follow the input.

12. PROGRAMMABLE D-TYPE MASTER/SLAVE FLIP-FLOP (1900).

This cell has been implemented with functional circuitry and is identical to cell 1820 except the $\bar{C}$ control signal terminal on the slave portion of the flip-flop is accessible, and is not necessarily the inversion of the control signal C. This allows the slave section of the flip-flop, and hence the output, to be set to a high state, independent of the master by holding both control lines low. If the control signal $\bar{C}$ to the slave is the logical inversion of the control signal C to the master portion, the flip-flop will function as a regular D-type master/slave flip-flop (1820).

When control signal C goes from low to high (and $\bar{C}$ goes from high to low), the logical inversion of the data on the D input line is transferred to the output of the master portion. On the following high to low transition of C (and low to high transition of $\bar{C}$), the complement of the data stored in the master will be transferred to the output of the slave portion, which will then hold the data until the next high to low transition of the control signal C (and low to high transition of $\bar{C}$).

Therefore, the information on input line D may be loaded into the master when C goes high (and $\bar{C}$ goes low). This information may then be transferred to the slave, and hence to the output, by bringing C low (and $\bar{C}$ high). So if the control signals are synchronized, one cycle of the control signals will transfer the data from the D input to the output of the flip-flop.

The minimum recommended positive-going clock pulse width required to load the master flip-flop is 75 ns. The minimum negative

clock width for transferring to the output is 50 ns. The data line should be held constant for at least 50 ns prior to and succeeding all clock transitions.

13. PROGRAMMABLE D-TYPE MASTER/SLAVE FLIP-FLOP WITH RESET (1910).

This cell is identical to cell 1920 except that control line $\bar{C}$ on the slave flip-flop is accessible. This allows the output of the 1910 to be set to a 1 on a single clock pulse by holding both control lines low. However, if the logical inversion of control line C is connected to $\bar{C}$, the 1910 will function as a 1920.

This cell uses functional logic to provide two levels of logic in a master/slave configuration. The master portion has a two-input NOR in the feedback path which, when a 1 is placed on its R input, resets the output of the 1910 to 0. If the reset line is held low, the flip-flop functions as a regular D flip-flop.

When control signal C makes a low to high transition, (and control signal $\bar{C}$ makes a high to low transition), and the reset line is low, the complement of the data on the D input line is transferred to the output of the master portion. When C next goes low ($\bar{C}$ goes high and reset is low) the logical inversion of that signal is then transferred to output of the slave, and hence the output of the flip-flop. The slave will then hold the data until the next high to low transition of control signal C (while $\bar{C}$ goes from low to high).

To briefly summarize, assuming the reset line is low and C and $\bar{C}$ are complement signals, a low to high transition of C loads the master and then when C goes low, the data is transferred to the output of the flip-flop. The output can be set to 0 by holding C low and the reset line R high. The output can be set to a 1 by bringing both control lines low.

It is recommended that the minimum positive-going clock pulse width required to load the master be 75ns. The negative-going clock pulse to transfer the data to the output should be at least 75 ns wide. The data line should be held constant for at least 50 ns prior to and succeeding all clock transitions. The reset line should be held high for at least 50 ns to ensure reset.

14. D-TYPE MASTER/SLAVE FLIP-FLOP WITH RESET (1920).

This cell has been implemented with functional logic and is identical to cell 1820 except that the inverter in the feedback path of the master portion has been changed to a NOR circuit with one input used as a reset line. When C is low and R is high the output of the flip-flop resets to 0. While the reset line is held low the flip-flop functions normally.

When control signal C goes from low to high and R is held low, the data at input D is inverted and transferred to the output of the master. On the next high to low transition of C that data is again inverted and transferred to the output of the slave portion. The data is held there until the next high to low-transition of C.

Therefore in summary, a low to high transition of control signal C loads the master portion of the flip-flop and that data is transferred to the output of the slave on the following high to low transition of C. The output of the slave can be reset to 0 by holding C low and the reset line R high.

It is recommended that the minimum positive-going clock pulse width to ensure loading of the master be 75 ns. The negative-going clock width to transfer the data to the output should be about

50 ns before and after all clock transitions. To ensure reset, the reset line should be held high for at least 30 ns.

15. EXCLUSIVE-OR (2310).

This cell generates the required logical operation by utilizing a unique interconnection of four transistors. Although the cell is essentially a transmission gate arrangement, it is a group III cell because of its buffered output. It is recommended however that cell 2310 be further buffered, with a cell from group IV, when the output load exceeds 15 pF. Analysis has revealed an unequal propagation delay for the two inputs of the cell with input B providing the smaller propagation delay.[2]

16. 9000 SERIES CELLS.

The remaining standard cells are referred to as 9000 series cells and are used for inputing and outputing electrical signals and power.

A. 9100 - side input pad with a 1.1 KΩ series resistor and input diodes for protection

B. 9110 - Left output pad

C. 9120 - Right output pad

D. 9200 - Top/Bottom input pad with a 1.1 KΩ series resistor and input diodes for protection

E. 9210 - Top/Bottom output pad

CHAPTER 3. SYSTEM USER GUIDE

A. INTRODUCTION

This chapter gives an explanation of the STAR design system software and how to use it on the XDS SIGMA/5 Computer system located at NASA, Marshall Space Flight Center, Huntsville, Alabama. Included are sections on file management for the STAR-system, how to create the STAR input file, and explanations of each of the STAR programs and how to execute them. Using this chapter, the user can transform a logic diagram into data which generates masks necessary for integrated circuit fabricaton.

These guidelines assume that the user has

1. access to the SIGMA system via a local demand terminal or a compatible remote terminal over a telephone line,
2. an authorized account and file space,
3. a minimal knowledge of the SIGMA system and/or the appropriate manuals, although some basic instructions will be given.

Although the commands used in these guidelines are for the SIGMA system (128K, 32 bit words), they are sufficiently explained so that, if the software is installed on another system, similar commands can be used. A list of the necessary commands and their descriptions is given in Table 3.1. The part of the command in brackets is optional.

Disc files have been established in certain accounts to facilitate the use of the STAR software on the SIGMA system. These files contain

SYSTEM COMMANDS	EXPLANATION
BATCH filename	Enters specified file in the batch job stream.
B[UILD] filename	Calls EDIT and names a file to be created
BYE	Disconnects terminal from system
C[OPY] filename	Displays contents of filename
C[OPY] file1 OVER file2	Copies contents of file1 over file2
C[OPY] file1 INTO file2	Merges contents of file1 into file2
CANCEL jid	Cancels previously submitted batch job
DELETE filename	Deletes named file from system
DI[SPLAY]	Displays current values of various system parameters
E[DIT] filename	Calls EDIT processor and names a file to be edited
JOB jid	Displays status of specified batch jobs
L	Alphabetically lists all files in account
L filename	Lists attributes of specified file
XEQ filename	Executes commands in file
EDIT COMMANDS	**EXPLANATION**
END	Terminates execution of EDIT and returns control to system level
IN	Inserts new line into file
TY	Displays contents of file

TABLE 3.1 Some SIGMA Commands

the job control language and the required input data for the programs, and can be copied into the user's account, modified as necessary, and then executed. The use of these files will be explained in the next section.

An overall system software flowchart is shown in Figure 3.1. The software is written in FORTRAN and BASIC and was developed using the SIGMA machine.

B. File Management

This section explains how the files necessary to execute the STAR system are established, and how, after they are created, to manage them. If more information on the SIGMA system is needed, the reader is referred to the XEROX Time-Sharing Reference Manual and the XEROX Time-Sharing User's Guide.[6,7]

After logging on into a new or existing account, the user is ready to create the files needed to execute the STAR design system. These files can be created by the user, or a file (MOVE.TROTTER) can be executed which will create all necessary files. To use this file the user should first type

!C MOVE.TROTTER[1] .

This will copy the file into the user's account. When a prompt (!) is returned, this file can then be executed by typing

!XEQ MOVE .

---

[1]The ! symbol is the prompt given by the Sigma system and does not have to be typed by the user. A carriage return is implied after each command.

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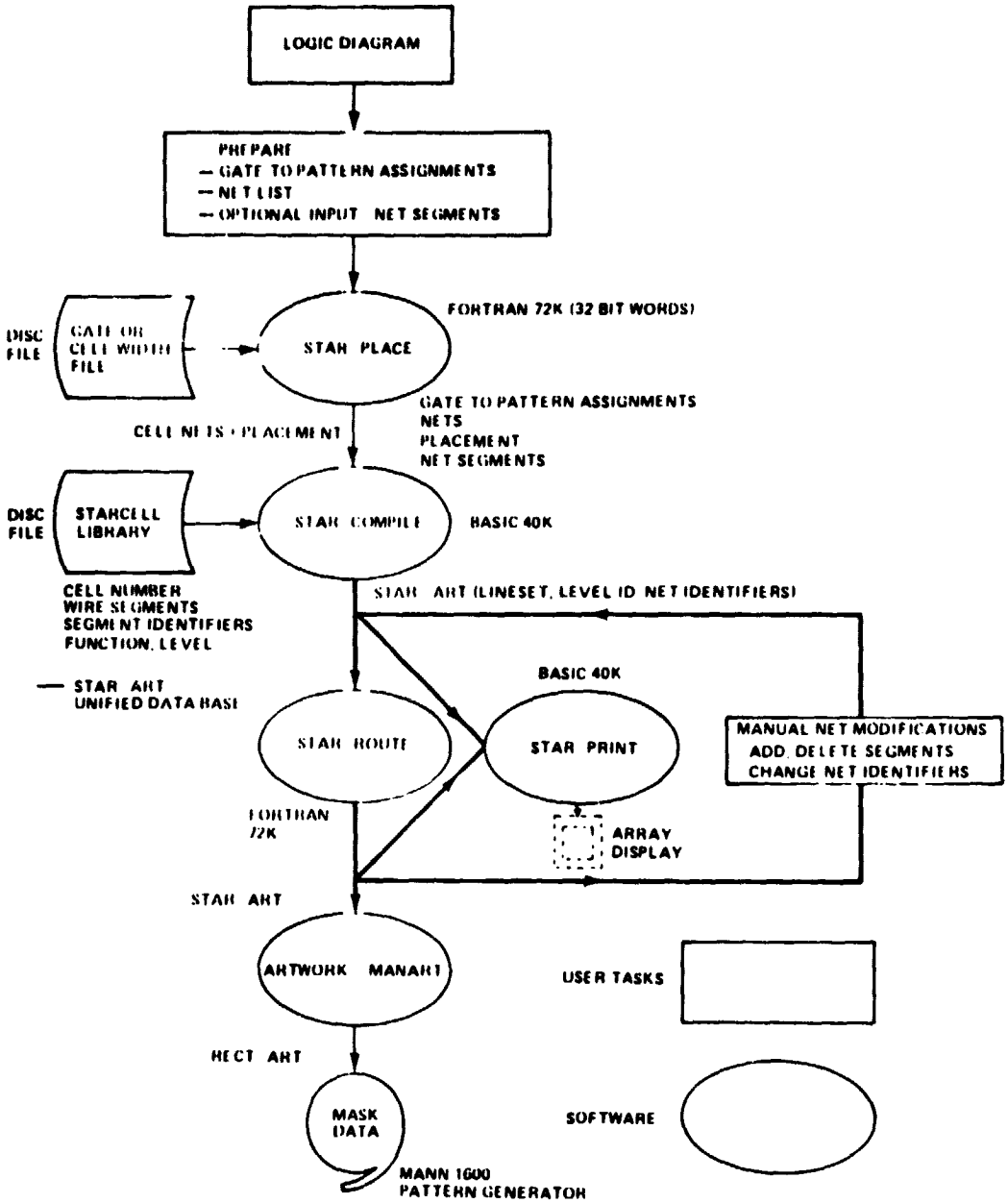

Figure 3.1 STAR Design System Flowchart and Software Components

When the computer responds with *** XEQ TERMINATED ***, all of the files necessary to use the STAR programs have been created in the user's account. Therefore those files do not have to be created by the user.

The user is advised to be aware of available file space in order to prevent premature termination of programs by a lack of file space. At the present time, each user is allotted 3064 granules of file space. At any time, to determine the amount of file space (in granules) available type

!DI .

A shortage of file space should not occur unless the user saves the output of the STAR programs, because ordinarily each new execution of a STAR program overwrites its old output. Therefore if the output of a program is desired to be saved the user should type

!C oldfile TO newfile .

However, the user should be reminded that these files should be deleted when no longer needed to free file space.

C. Creating STAR Input File

This section deals mainly with the creation of a new input file and only briefly explains the relevant terms. The circuit description terms and the STAR-PLACE control data contained in the files are explained in more detail in the STAR-PLACE section under Input Data Format.

1. Creating Input File From Logic Diagram. Starting with a logic diagram composed of logic cells found in the logic cell library, the user should number each of the logic gates, including input and output pads. Interconnections between logic gates, called nets, should also be numbered. A list of the presently available cells and their functions is shown in Table 2.1. If new cells are required, they must be added to the library, as shown in Chapter 2.

Next, the user must prepare a gate to logic cell assignment list, which corresponds the number of the gate on the logic diagram to the STAR logic cell number from the cell library. The user also prepares a connectivity or net list that consists of the net numbers (from the logic diagram) and the gate numbers and pin numbers of the gates which a net connects. The pin numbers are obtained from the Standard Cell data sheets in the Appendix. An example logic cell diagram is shown in Figure 3.2 with each cell, pin, and net numbered.

The importance of having a correctly labeled logic diagram and net list cannot be over-emphasized, as the majority of mistakes occur in this phase. The user should double-check the results before proceeding.

It should be noted that, because of limited storage available, certain limits are placed on the input circuits. A maximum of 999 cells, 500 nets, and 98 pads are allowed. Also, gate numbers greater than 999 are not allowed. The STAR selected for use cannot exceed 30 cell rows by 100 columns.

2. Using Example Input File. The STAR input file is now ready to be constructed. An example input file for circuit EXAMPLE has been

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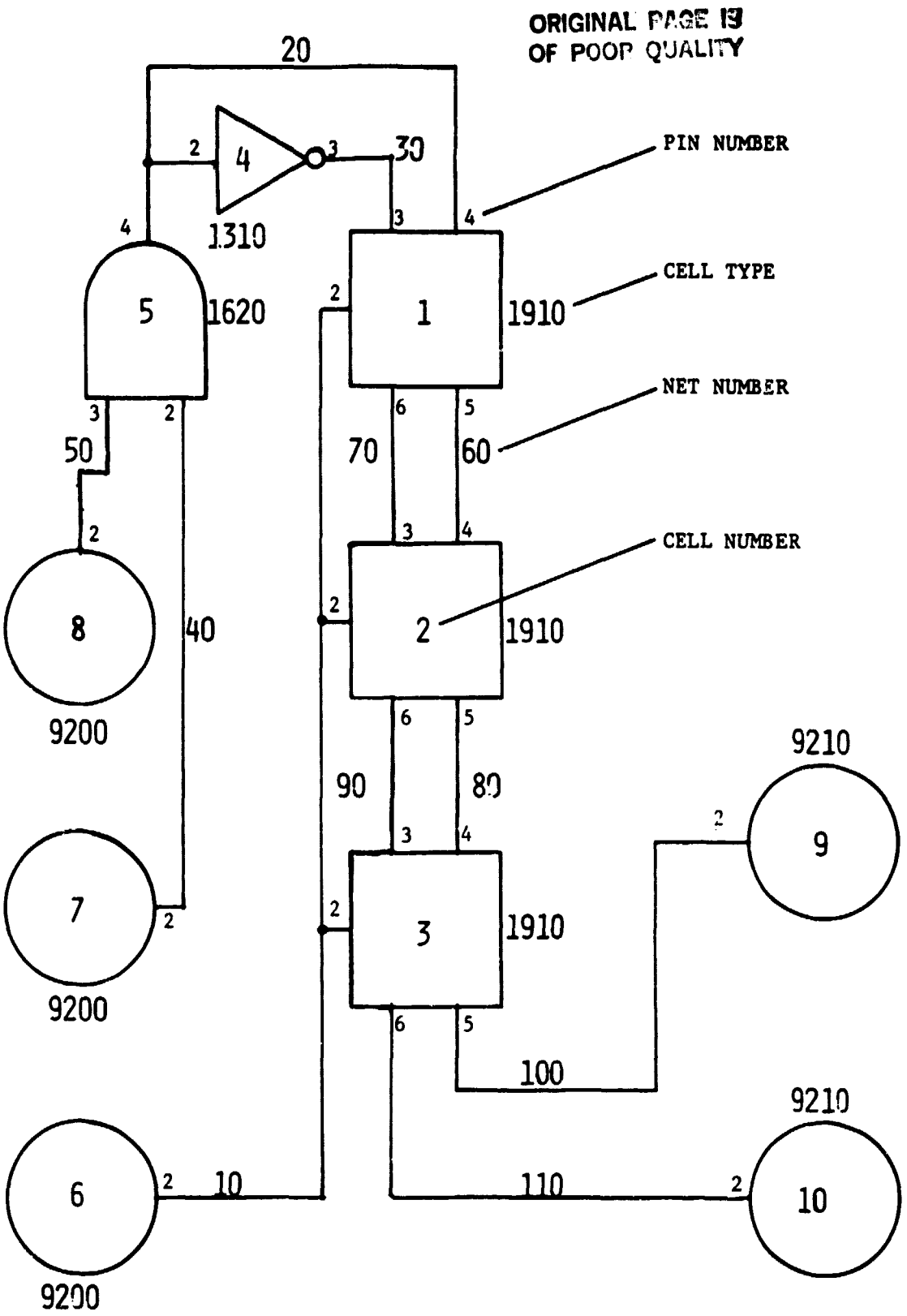

Figure 3.2 Example Logic Diagram

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```
C
NAME, EXAMPLE
C
FIND, 50
C
IMPROVE, 5
C
NEIGHBORHOOD, 1,5
C
STAR SIZE, 8 24
C
GATES TO PATTERNS
1 1910 2 1910 3 1910 4 1310 5 1620 6 9200 7 9200 8 9200 9 9210
10 9210
C
NETS
 10 6 2 1 2 2 2 3 2
 20 5 4 4 2 1 4
 30 4 3 1 3
 40 7 2 5 2
 50 8 2 5 3
 60 1 5 2 4
 70 1 6 2 3
 80 2 5 3 4
 90 2 6 3 3
100 3 5 9 2
110 3 6 10 2
```

Figure 3.3 Example Input File

created, as shown in Figure 3.3. This file can be modified for the user's own, or used merely for reference.

Circuit 'EXAMPLE' has 11 nets: net 10 connects pin 2 of cells 1, 2, 3, and 6, net 20 connects pin 4 of cells 1 and 5 and pin 2 of cell 4, net 30 connects pin 3 of cells 1 and 4, net 40 connects pin 2 of cells 5 and 7, net 50 connects pin 3 of cell 5 to pin 2 of cell 8, net 60 connects pin 5 of cell 1 to pin 4 of cell 2, net 70 connects pin 6 of cell 1 to pin 3 of cell 2, net 80 connects pin 5 of cell 2 to pin 4 of cell 3, net 90 connects pin 6 of cell 2 to pin 3 of cell 3, net 100 connects pin 5 of cell 3 to pin 2 of cell 9, and net 110 connects pin 6 of cell 3 to pin 2 of cell 10. Cells 1-3 are type 1910, cell 4 is a type 1310, cell 5 is a type 1620, cells 6-8 are type 9200 (input pads), and cells 9 and 10 are type 9210 (output pads). The STAR to be used consists of 8 rows and 24 columns. Fifty folding solutions are to be formed and the best 5 improved. The row and cell neighborhood sizes are 1 and 5, respectively.

To modify the example input file type

```
!EDIT EXAMPLE      .
```

This will call the Edit processor and the computer will respond with the words EDIT HERE and the editor prompt (*). Now type

```
*TY
```

which will cause the file to be displayed (including line numbers called keys). If the user desires to view only certain lines the format is

```
*TY start-end      .
```

To modify lines in the file type

*IN key

where key is a new or existing line number. The editor will echo that number on the next line and await input. The user should now insert the desired contents of that line.

In this way, new lines can be created and existing lines can be changed. The editor will automatically try to insert a succeeding line if one does not already exist, and then only each new string need be entered until finished. Another carriage return will get the user out of the input mode. By using the TY command, the input file can be checked for errors. To exit the editor, type

*END .

If the user would rather create the input file from scratch, it can be done by typing

!BUILD filename .

The computer will respond with 1.000 and is ready for the first line to be inserted. When a return is hit the computer responds with 2.000 and so on until a return is hit without a line of text being entered.

If a typing mistake was made or the user wishes to change a line, the EDIT processor must be used as shown before. A more detailed description of the EDITOR can be found in the XEROX Time-Sharing User's Guide.

The user should now copy this file to the input file for the placement program by typing

!C EXAMPLE OVER PLACEIN .

The STAR placement program is now ready to be executed, but first some guidelines for running programs on the SIGMA system will be given.

3. Program Execution. Some of the STAR programs can be executed in the Demand mode from the terminal as well as the Batch mode. If the Demand mode is used, the user must stay online until program execution is terminated, thus tying up computer resources. Therefore, unless speed is of the essence, the Batch mode should be used whenever possible. To submit a job via the Batch mode type

!BATCH filename .

The STAR programs which are executable from the Batch mode begin with "J:", such as J:PLACE.

The system will respond by assigning the job a job identification (jid) and sending one of the following messages to the terminal:

ID = jid SUBMITTED time-date

WAITING: n to RUN

or

ID = jid SUBMITTED time-date

RUNNING .

The user may check the status of the job by using the JOB command or may cancel the job using the CANCEL command. The format of the JOB command is

!JOB jid .

The system will respond that the job is either completed, running, still waiting to be run, or waiting to be printed out. If the job is completed or waiting to be output, the user can view the output file

(using the Copy command) or run the next program.

If it is desired that execution of the program be prematurely terminated for some reason, the following command can be used.

!CANCEL jid

The user should record the id of each job as it is submitted, so that the wrong job will not be canceled, and the job's status can be checked.

D. STAR Design System Software

This section describes the STAR design system software and how to execute it on the SIGMA computer system. The STAR design system consists of five computer programs which enable a user to go from a logic diagram to the mask data necessary for integrated circuit fabrication. The system includes a STAR-PLACE automatic placement program, a STAR-COMPILE compiling program, a STAR-ROUTE automatic routing program, a STAR-PRINT display program, and the ARTWORK-MANART artwork generating software. A flowchart which identifies the input and output files, diagnositc files, and load modules of the STAR system is shown in Figure 3.4.

1. STAR-PLACE. The STAR-PLACE program is designed to provide two-dimensional placements of digital logic circuits on the Standard Transistor Array (STAR).

The program is written in the FORTRAN-IV programming language, and with the exception of the use of Implied-DO constructs in I/O statements, it is ANSII standard. This, minimal modification of the source language should allow use of the program with most FORTRAN-IV compilers.

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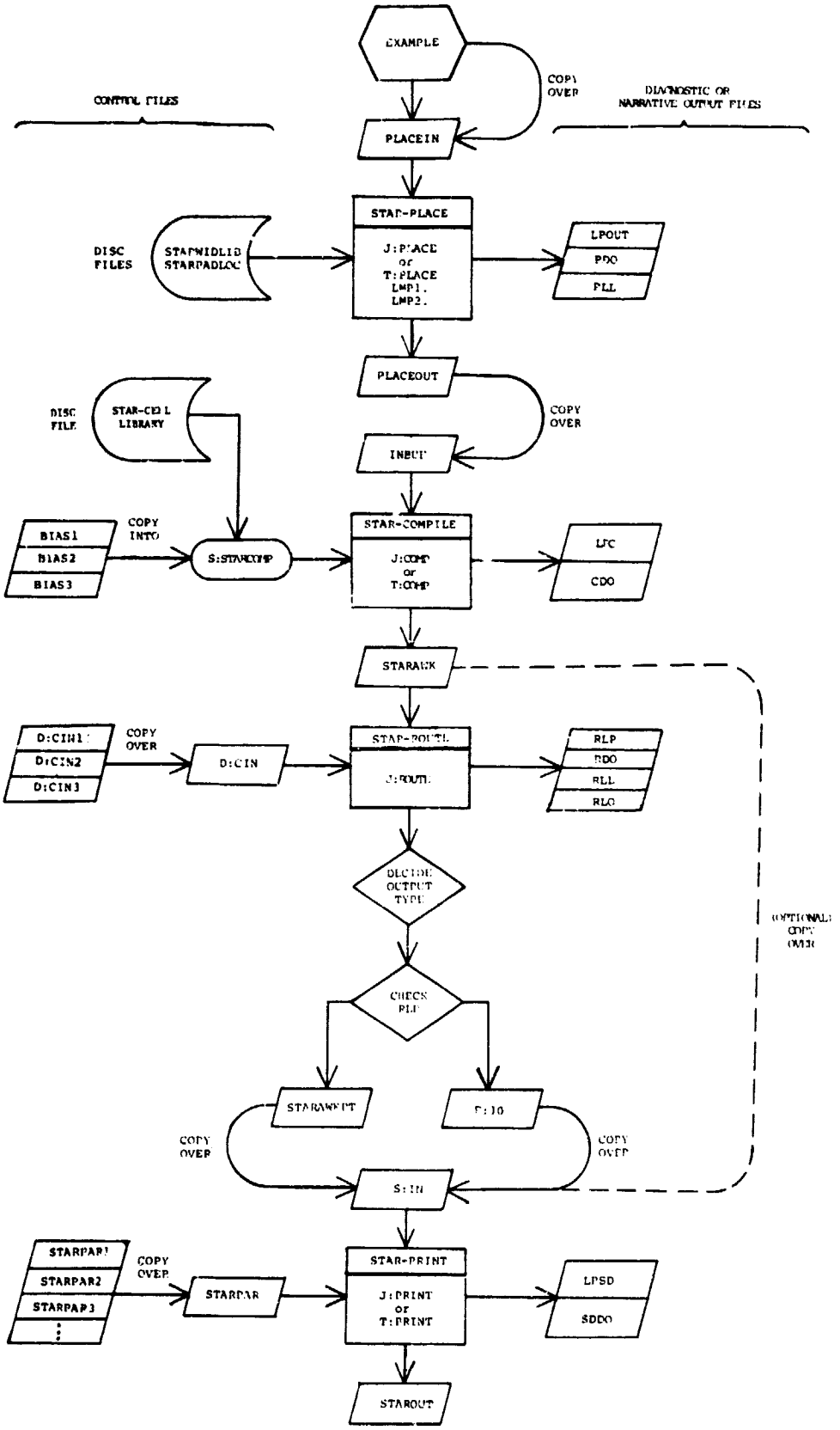

Figure 3.4 STAR Design System Software Flowchart

Input to the program consists of a description of circuit cells and interconnections as explained in the preceding section, and is called PLACEIN.

The following material on the placement program was largely taken from NASA Contractor Report 161291 "Standard Transistor Array, CAPSTAR User's Guide". [3]

a. Input Data Format. The input file consists of a series of 80-character records, of which only the first 72 are significant. Positions 73-80 can be used for record numbering or other user information. Each record consists of format-free numeric or character items. The end of a numeric item is sensed whenever a blank, comma, or the end of the record is seen. The end of a character item is indicated by a comma or record end. A record can be continued by leaving the first four positions of the next record blank. A record may be continued any number of times.

The input file may consist of STAR-PLACE control records, circuit definition records, and passed records. The control records either specify settings for STAR-PLACE variables or act as headers for groups of circuit definition records. The passed records are those which are not recognized as control or definition records and are included in the STAR-PLACE output file for use by later programs.

b. Control Records. Each control record consists of a single STAR-PLACE control statement beginning in column 1 with pertinent data following as necessary. A list of the STAR-PLACE control statements, their function, and necessary data is shown below. Where allowed the shortened form of the control statement is shown in parentheses.

C

Function - Denotes a comment to be shown in the narrative output.

Data - Comment in columns 5-72 of the record (no continuation allowed).

Passed - No

DEBUG (DEBU)

Function - Turns on STAR-PLACE debugging output.

Data - None.

Passed - No

FIND,

Function - Sets the upper limit on number of folding solutions to be found (initially 50). Specifying 0 causes all possible folding solutions to be generated.

Data - Upper limit following comma.

Passed - No

GATES TO PATTERNS (GATE)

Function - Header for cell type list.

Data - Cell type list in following records.

Passed - Yes

IMPROVE, (IMPR,)

Function - Specifies number of folding solutions to be improved (initially 3, max = 10).

Data - Number of solutions following comma.

Passed - No

LINEAR ORDER (LINE)

Function - Header for user-entered linear order. Causes disabling of STAR-PLACE clustering and linear ordering steps.

Data - Linear order in following records.

Passed - No

NAME,

Function - Specifies circuit title for output listing.

Data - Circuit title (8 characters) after comma.

Passed - Yes

NEIGHBORHOOD, (NEIG,)

Function - Specifies row and cell neighborhood sizes for placement improvement step (initially 1,1).

Data - Row, cell neighborhood sizes following comma.

Passed - No

NETS

Function - Header for circuit net lists.

Data - Net lists in following records.

Passed - Yes

STAR SIZE, (STAR,)

Function - Specifies STAR dimensions.

Data - STAR size (cell rows, transistor columns) following comma.

Passed - Yes

STEP,

Function - Specifies STAR-PLACE steps to be performed (initially all).

Data - Step names (CLUSTER, LINEUP, WIRECROSS, FOLD) separated by commas following 'STEP,'.

Passed - No

The presently available STAR sizes are shown in Table 3.2.

STAR SIZE	ROWS	COLUMNS	TRANSISTORS	PADS	SIZE (MILS)
8,24	8	24	384	16	90x80
16,54	16	54	1728	36	162x131
28,94	28	94	5264	64	254x208

TABLE 3.2 Presently Available STAR Sizes

In order to choose the correct STAR size, an estimation of the transistors needed should be made, and the number of I/O pads should be counted. The user can then choose the correct STAR from Table 3.2.

c. Circuit Definition Records. The cell type list, net list, and user-defined linear order are entered as a series of numeric records following the appropriate header record. The end of a list is assumed when a non-numeric item or the end of the input file is seen. The format of each of the three lists is shown below.

(1) Cell Type List (Following 'GATES TO PATTERNS'). In this list, each of the circuit cells and pads is associated with a STAR standard cell or pad type number. The format of each record in this list is

cell1 type1 cell2 type2 . . . .

For example, if cell number x is type 1000+x, a typical cell type list record is

1 1001 2 1002 3 1003 4 1004 .

Sufficient records to specify each cell or pad in the circuit should be included.

The list is passed to the output file with certain adjustments. These adjustments involve re-assignment of pad type numbers based on the pad position in the final placement. In the input file, input pads are type 9200 and output pads are type 9210. For pads placed at the top or bottom of the STAR, the type numbers are unchanged. For input pads placed at the sides of the STAR, the type number is changed to 9100. For an output pad placed at the left, the type number is changed to 9110. For output pads placed at the right, the type number is changed to 9120.

(2) Net List (Following 'NETS'). The connection points (cell number, pin number) of each net in the circuit are identified in this list. The format of each record is

net cell1 pin1 cell2 pin2 . . . .

For example, if net 5 is connected to pin 1 of cells 6, 7, and 8, the net list record for net 5 is

5 6 1 7 1 8 1 .

For large nets, more than one input file record may be required. Extension of the net may be accomplished either by use of the record continuation feature or by repetition of the net number at the beginning of the next record. Thus, either

5 6 1
7 1 8 1

or

```
5 6 1
5 7 1 8 1
```

can be used to enter net 5, above. If the second of these net continuation forms is used, the continuation records must immediately follow the initial record for the net.

Information specified in the net list is passed to the output file after modification of all continuations to the second form, above.

(3) Linear Order (Following 'LINEAR ORDER'). Each cell and pad in the network should be included in this list if the user-entered linear order option is selected. The list format is

```
cell1 cell2 cell3 cell4
```

Record continuation is allowed, but not required in this list. The linear order is not passed to the output file.

d. Placement Output. The output information provided by STAR-PLACE consists of two files, regardless of the mode in which the program was executed. The file called PLACEOUT is in a format suitable for use by other programs. The file called LPOUT consists of user (narrative) output.

(1) Output file. The STAR-PLACE output file (PLACEOUT) contains the circuit cell type and net lists, the grid coordinate format of the placement, the locations of all constructed barriers, and any passed data from the input file. The format of this file for the example application is shown in Figure 3.5. If, after completion of the STAR design cycle, it is found that the circuit has not been successfully routed and hand-placement is chosen as a possible solution,

this is the file which must be modified. Therefore, it is important that the format of this file be understood.

TITLE, STAR SIZE, and GATES TO PATTERN are data passed from the input data. The PLACEM data are the positions of each cell, pad, and groups of unused transistors, shown in actual STAR grid coordinates. A group of XXX unused transistors is denoted by 999XXX. Starting on the second row under PLACEM, the first column gives the y coordinate of the source connection which begins the cell. A minus sign (-) in front of the number implies that the cell is above the power supply. The other columns alternate between denoting the cell number and its beginning X coordinate, respectively.

The data under NETS was passed from the input data, WIRES contain data showing the coordinates of the barriers constructed to prevent router usage of unused pad positions. For example, the first line denotes that a barrier is constructed on level 6 from 69,24 to 83,24.

By modifying the data in this file, mainly under PLACEM and wires, hand-placement can be accomplished, thus perhaps providing successful routing.

(2) Narrative Output. The narrative output of STAR-PLACE which is helpful to the user is contained in file LPOUT. Each STAR-PLACE step is identified by a header line showing the step and circuit names. An explanation and example of the narrative output provided by each step is shown in the following paragraphs.

(a) Data Entry Step. Each control and passed record in the input file is echoed on the listing. The cell type definitions are displayed with cell width information as obtained from the STAR cell width library (STARWIDLIB). The cells composing each

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```
TITLE EXAMPLE
STAR SIZE     8    24
GATES TO PATTERNS
   999   9970
     1   1910      2   1910    3   1910      4   1310     5   1620     6 9200
     7   9200      8   9100    9   9210     10   9210
PLACEM
0 999 0
     25        1      25        4    64 999005      70      5      85
    -41        2      25   999011    64
     41        3      25   999011    64
    -57   999024      25
     57   999024      25
    -73   999024      25
     73   999024      25
    -89   999024      25
    -25        6      39
    -25        7      84
     25        8      96
     89        9      39
    -25       10      24
 NETS
    10      6      2      1      2      2      2      3      2
    20      5      4      4      2      1      4
    30      4      3      1      3
    40      7      2      5      2
    50      8      2      5      3
    60      1      5      2      4
    70      1      6      2      3
    80      2      5      3      4
    90      2      6      3      3
   100      3      5      9      2
   110      3      6     10      2
 WIRES
    6      69      24      83      24  BARR
    6      24      90      38      90  BARR
    6      69      90      83      90  BARR
    6      84      90      98      90  BARR
    6      22      26      22      40  BARR
    6      22      42      22      56  BARR
    6      22      74      22      88  BARR
    6     101      58     101      72  BARR
    6     101      74     101      88  BARR
```

Figure 3.5 STAR-PLACE Output File (Placeout)

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```
C
NAME, EXAMPLE
C
FIND, 50
C
IMPROVE, 5
C
NEIGHBORHOOD,1, 5
C
STAR SIZE     8   24
C
GATES TO PATTERNS
                      CELL      1          TYPE 1910        WIDTH   13
                      CELL      2          TYPE 1910        WIDTH   13
                      CELL      3          TYPE 1910        WIDTH   13
                      CELL      4          TYPE 1310        WIDTH    2
                      CELL      5          TYPE 1620        WIDTH    4
                      PAD       6          TYPE 9200
                      PAD       7          TYPE 9200
                      PAD       8          TYPE 9200
                      PAD       9          TYPE 9210
                      PAD      10          TYPE 9210
C
NETS
                      NET LISTS
                      NET  10          6   1   2    3
                      NET  20          5   4   1
                      NET  30          4   1
                      NET  40          7   5
                      NET  50          8   5
                      NET  60          1   2
                      NET  70          1   2
                      NET  80          2   3
                      NET  90          2   3
                      NET 100          3   9
                      NET 110          3  10
END OF INPUT DATA
            DATA CROSS-CHECK INITIATED
            DATA CROSS-CHECK COMPLETED
```

Figure 3.6 Data Entry Step Output

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```
      CHIP AREA= 45 TOTAL METAL = 54. CHIP DENSITY = 1.2
      CELL TO BE COMBINED = 6 WIDTH = 0 # NETS = 2
##########################################################################
DELTA METAL     CAND. WIDTH     CAND. NETS     NETS IF COMB.    CANDIDATE

   3.6056            13              5              5              3
D3= 1.7  D1= .0  D2= 1.4  DT= 1.3  NEW METAL = + 4.  A1= 0  A2= 13
            CELL  1001 REPLACES     6 &     3          WIDTH = 13
            NET    10 ABSORBED
```

Figure 3.7 Output Shown For Single Cluster Formation From Cluster File

```
CELL     COMPOSED OF CELLS
1001-     6   3   0
1002-     7   5   0
1003-     8   7   5   0
1004-     9   6   3   0
1005-    10   9   6   3   0
1006-     4   1   0
1007-     8   4   7   1   5   0
1008-    10   2   9   6   3   0
1009-     8  10   4   7   2   9   1   5   6   3   0
                NORMAL CLUSTERING STEP TERMINATION
```

Figure 3.8 Clustering Step Summary Output

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LINEAR ORDER

8 7 5 4 1 2 6 3 9 10

Figure 3.9 Linear Ordering Step Output

NO CONNECTION

CONNECTION

FWID	RWID	CELL						
0	45							
0	45	8	-50					
0	45	7	50	-40				
4	41	5	-50	-40	-20			
6	39	4	-30		-20			
19	26	1	-30	-10	-20	-60	-70	
32	13	2	-80	-10	-90	-60	-70	
32	13	6	80	-10	90			
45	0	3	-80	-10	-90	-100	-110	
45	0	9				-100	110	
45	0	10					-110	

DATA TRANSFER FILE CONSTRUCTED
NORMAL CAPSTAR PART 2A TERMINATION

RUN PART 2B TO CONTINUE

Figure 3.10 Wirecross Output

net in the circuit are also shown. At the end of the section, the result of a cross-check between the various lists is given.

The data entry step output for the cell type and net lists of the example application is shown in Figure 3.6.

(b) Clustering Step. For each cell (cell number <1ØØØ) or cluster (cell number >1ØØØ) to be combined, the cell number, width and number of nets is shown. The statistics for each candidate for combination and the effect of combination on the total chip metal are calculated and displayed in tabular format. The combined cells and resultant cluster are then shown along with the cluster width and nets absorbed by combination. The information printed for a typical combination is shown in Figure 3.7.

Following clustering of all cells, a summary of cell combination is printed as shown in Figure 3.8.

(c) Linear Ordering Step. The generated linear cell order is shown in 15(I4) format. The output for the example application is shown in Figure 3.9.

(d) Wirecross Step. The linear order is displayed vertically with both forward (FWID) and reverse (RWID) cumulative cell widths shown. Each circuit net is shown to the right of the linear order with connections to a cell indicated by "-".

The wirecross output for the example circuit is shown in Figure 3.10.

(e) Placement Step. At the beginning of the placement step, STAR-PLACE forms the requested number of folding solutions. The highest rated IMPROVE of these are selected and ratings are shown.

Start and end of placement improvement are noted and the rating data for the highest rated improved placement is shown. The format of this output is shown in Figure 3.11.

In this output, "QUALITY" is the estimated fraction of all layouts of the circuit with ratings lower than the placement of interest. Horizontal and vertical ratings reflect the predicted fraction of the available channel area which will be used in placement routing. Pads are not included in the placement at this step, so statistics do not reflect pad placement.

After printing of result placement rating information, a pictorial representation of the cell layout is shown. This output for the example circuit is shown in Figure 3.12.

In this output, cell boundaries are shown as "#" and transistor boundaries as ":". Cell numbers are read vertically and occur to the left of the dashes. Numbers to the right of the dashes indicate nets which are incident to the cell. Transistors completely surrounded by #'s are not used for cell placement.

Following placement depiction, the (row, column) positions assigned to circuit pads are shown. The position of each cell, pad, and group of unused transistors (A group of XXX unused transistors is denoted by 999XXX) is then shown in actual STAR grid coordinates. Finally, the set of barriers constructed to prevent router usage of unused pad positions is shown. This section of the output, as shown in Figure 3.13, is the same as some of the data in the file Placeout, as shown in Figure 3.5.

```
DATA TRANSFER COMPLETED
  51 SOLUTIONS FOUND IN      51  TRIES
   5  BEST SELECTED


NUMBER      RATING*10**6    QUALITY*10**6

   1          784023          923313
  36          780422          872544
   8          778341          834318
   6          775439          769833
   5          774765          753064


PLACEMENT IMPROVEMENT INITIATED
PLACEMENT IMPROVEMENT COMPLETED


PLACEMENT NUMBER    36
              NET    10  STRAIGHT
              NET    20  STRAIGHT
              NET    30  STRAIGHT
              NET    60  STRAIGHT
              NET    70  STRAIGHT
              NET    80  STRAIGHT
              NET    90  STRAIGHT


RATINGS

TOTAL          ---     78.68  %

HORIZONTAL     ---      7.49  %

VERTICAL       ---      5.73  %

STRAIGHT NETS  ---    100.00  %

QUALITY        ---       .93656
```

Figure 3.11 Folding Summary and Result Rating Output

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Figure 3.12 Pictorial Placement Output

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```
PAD     6 PLACED AT     .0 ,    8.0
PAD     7 PLACED AT     .0 ,   23.0
PAD     8 PLACED AT    1.5 ,   25.0
PAD     9 PLACED AT    9.0 ,    8.0
PAD    10 PLACED AT     .0 ,    3.0
PLACEM
     25       1      25       4     64 999005       70        5      85
    -41       2      25  999011     64
     41       3      25  999011     64
    -57  999024      25
     57  999024      25
    -73  999024      25
     73  999024      25
    -89  999024      25
    -25       6      39
    -25       7      84
     25       8      96
     89       9      39
    -25      10      24
BARRIER CONSTRUCTED ON LEVEL   6 FROM    69 ,    24 TO    83 ,    24
BARRIER CONSTRUCTED ON LEVEL   6 FROM    24 ,    90 TO    38 ,    90
BARRIER CONSTRUCTED ON LEVEL   6 FROM    69 ,    90 TO    83 ,    90
BARRIER CONTSRUCTED ON LEVEL   6 FROM    84 ,    90 TO    98 ,    90
BARRIER CONSTRUCTED ON LEVEL   6 FROM    22 ,    26 TO    22 ,    40
BARRIER CONSTRUCTED ON LEVEL   6 FROM    22 ,    42 TO    22 ,    56
BARRIER CONSTRUCTED ON LEVEL   6 FROM    22 ,    74 TO    22 ,    88
BARRIER CONSTRUCTED ON LEVEL   6 FROM   101 ,    58 TO   101 ,    72
BARRIER CONSTRUCTED ON LEVEL   6 FROM   101 ,    74 TO   101 ,    88
OUTPUT FILE CONSTRUCTED
NORMAL CAPSTAR TERMINATION
```

Figure 3.13 Pad Placement, Grid Coordinate Translation, and Barrier Construction Output

e. Program Execution. STAR-PLACE can be executed from either the Demand mode or the Batch mode. For this routine, it may be advisable to use the Demand mode, because in order to restrict storage execution requirements and provide operator convenience the program has been divided into two segments. The first of these segments implements the data entry, clustering, and linear ordering functions of the placement procedure, as shown in Figures 3.5-3.10. The second segment performs the cell and pad placement tasks and builds the output database, as shown in Figures 3.11-3.13.

If STAR-PLACE is executed in the Demand mode, the output of first segment can be viewed or copied to another file before running the second segment. If STAR-PLACE is executed in the Batch mode only the output of the second segment is available.

The Demand version, called T:PLACE, facilitates all necessary channel assignments when it is executed. This is done by typing

!XEQ T:PLACE .

The computer will respond with the message

*** XEQ TERMINATED*** .

The first portion of the program is executed by the command

!LMP1.

which executes a load module. When the computer returns the message *STOP* Ø and a prompt (!), the narrative output file (LPOUT) in its intermediate form can be viewed or copied, or the

next module can be executed. To execute the second segment type

!LMP2.

When execution of this module has terminated all necessary output files have been constructed.

The Batch version is J:PLACE and is executed by the command

!BATCH J:PLACE

The computer will respond with a job id and the status of the job, as explained in a preceding section. All output will be directed to a line printer and also stored in files.

After execution of the placement program, the user can examine the final form of the narrative output file (LPOUT), and compare each step to the examples shown, in order to check for correct execution.

As a double-check on the STAR size, the user should check the WIRECROSS step and compare the cumulative cell width (RWID at top) to the total available width of the STAR used. If the cumulative cell width is more than 75% of the total available width, problems may be encountered in routing later. Therefore the user may wish to run the placement program again, using the next largest STAR size, if possible.

If the placement program fails to run successfully, the user can copy the diagnostic files PDO, and PLL for possible clues as to the reason why. The input file should also be checked for errors.

If the placement program was successful, it's output becomes the input to the next routine, which is called STAR-COMPILE. To

create the STAR-COMPILE input file use the command

!C PLACEOUT OVER INBUF

2. STAR-COMPILE. The STAR-COMPILE program accesses the STAR-cell library which contains the line segments that describe the device connections to achieve the cell's logic. The cell library also contains identifiers associated with each line segment. The identifiers are used to label inputs, outputs, barriers, and power bus line segments for line printer display as well as program use. The STAR-COMPILE program is written in XEROX Basic in order to take advantage of its unique feature of keyed file access. For this reason, the program is nontransportable.

For each cell that has been placed, the STAR-COMPILE program copies the cell library line segments with identifiers (as shown in Figure 2.7) onto the array at the positions specified by the placement program. Using the net lists, the line segments identifiers (that were copied from the cell library) are changed to the identifiers that describe all line segments associated with the original net. These identifiers will be used later by the STAR-ROUTE program which will supply line segments to interconnect all line segments that have the same identifiers. An example STAR-COMPILE output is shown in Figure 3.14.

To accomplish its task, the STAR-COMPILE program must have copied into it, the correct bias for the chosen STAR size. The correct values have been put into files called BIAS1, BIAS2, and BIAS3. This file consists of a single line that must be inserted into the source program.

The files are shown in Table 3.3 with their corresponding STAR sizes. Choose the bias file associated with the STAR size used

BIAS FILE	STAR SIZE
BIAS1	8,24
BIAS2	16,54
BIAS3	28,94

TABLE 3.3 STAR-COMPILE Bias Files

in the placement program and use the following command to put it into the STAR-COMPILE routine.

!C biasfile INTO S:STARCOMP

It is extremely important that INTO is used in this command as it merges the BIAS file into the source program, S:STARCOMP, and does not overwrite it.

a. Program Execution. The compile routine can be executed from either the Demand mode or the Batch mode, but again the Batch mode should be used whenever possible. The Batch command is

!BATCH J:COMP .

To execute STAR-COMPILE from the Demand mode the command

!T:COMP

is all that is needed. All output will come back to the screen.

b. Compile Output. The narrative output file for the STAR-COMPILE routine is called LPC. Also, diagnostics if any, are printed to a file called CDO. Both of these files can be examined. The output used by subsequent programs is STARAWK. Figure 3.14 is an example of the data in the STARAWK file and is the format of the data for the STAR-ROUTE input and output, STAR-PRINT input, and ARTWORK-MANART input.

From the program flowchart (Figure 3.1) it can be seen that, if desired, the output of the compile program can be used as the input to the STAR-PRINT display routine for a symbolic printout of the compile data. This may be helpful to the user, but it is not a necessary step.

3. STAR-ROUTE. The output file of the compile routine (STARAWK) is also the input file to STAR-ROUTE, therefore no copy command is needed.

The STAR-ROUTE program performs the discretionary interconnections of wiring through the use of net identifiers on available routing channels of the array. The program will seek the shortest distance between the line segments that have the same identifiers, and generate line segments to complete the net. The generated line segments will utilize the two levels of metal and VIAS (metal interconnects) available to complete the net as specified. The program will avoid areas of the array that have been labeled as barriers and will also perform a short check and open check between the completed nets.

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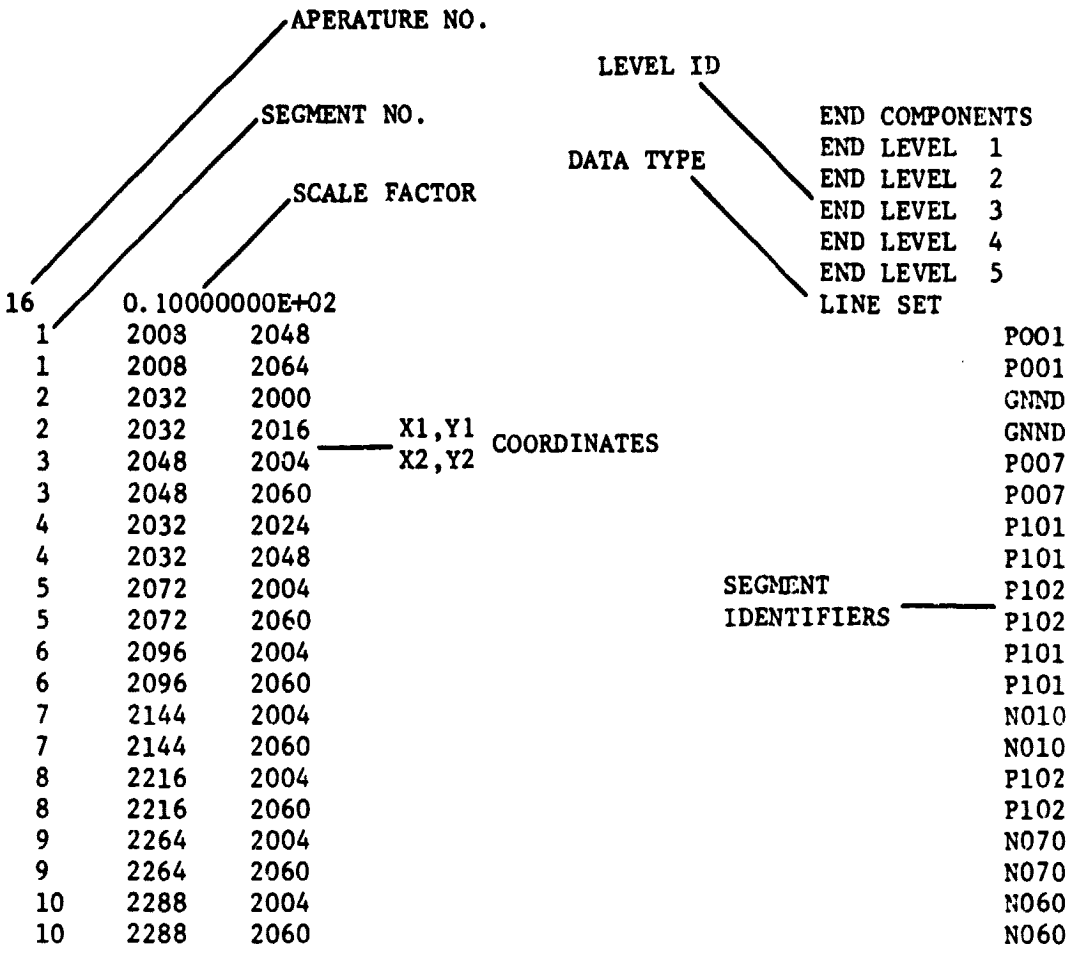

Figure 3.14 Example STAR-COMPILE Output

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Like the STAR-PLACE routine, STAR-ROUTE is also written in the FORTRAN-IV programming language.

The route program has a control input file associated with each of the STAR sizes. These are shown in Table 3.4.

CONTROL FILE	STAR SIZE
D:C1N1	8,24
D:C1N2	16,54
D:C1N3	28,94

TABLE 3.4 STAR-ROUTE Control Files

The user should choose the control file corresponding to the STAR size used. The following command can then be used to update the parameter file used by the STAR-ROUTE program.

!C control file OVER D:CIN

If the user has a data set for which it is desired to perform short distance routing before longer routing, the multipass capability of the STAR Router should be used. To activate multipass, the user must edit the control input file (D:CIN), to add the necessary information.

It should be noted, however, that this feature is not usually helpful. If the user desires to use multipass routing, more information can be found in the "STAR Router User's Guide" NASA Contractor Report 161213.[4]

STAR-ROUTE should always be run from the Batch mode, because of the required memory size. Therefore, use the command

```
!BATCH J:ROUTE
```

to execute the route program.

a. Router Output. During execution, router progress messages and error messages will be written to file RLP. The run time messages and progress messages are shown in Table 3.5. If the Demand mode were used, these messages will also be returned to the screen. Program diagnostic messages, if any, and accounting information are output to files RDO, RLL, and RLO.

After execution of STAR-ROUTE, the user should copy the file RLP and either find which I/O unit the PR2D output file (routed output) is on or, if routing was unsuccessful, determine why from the error messages. I/O unit 11 corresponds to file F:11 and I/O unit 10 is file STARAWKRT.

The output of the Route routine will be composed of data from the STAR-COMPILE program plus line segment data generated to complete all nets. Therefore, the file will resemble the STARAWK file, except it will be larger.

4. STAR-PRINT. The STAR-PRINT routines produce a symbolic layout of the STAR design. The input to the programs can either be the output of STAR-COMPILE or the output of STAR-ROUTE. In either case, the desired file should be copied over the input file (S:IN) of STAR-PRINT by using the command

The following messages may appear on the run printout. Their meaning is described at right.

Error Messages	Meaning
ERROR OR END-OF-FILE WHILE READING CONTROL INPUT	Bad or missing cards were found in the control input file.
MAXIMUM GRID SIZE EXCEEDED	The product of the X and Y grid dimensions exceeds 160,000.
PREMATURE END-OF-FILE HIT ON PR2D INPUT	Input file scan did not find the end of Level 8 in the file.
GRID DIMENSIONS EXCEEDED IN RIDP	Coordinates were found in the input file which exceed the specified grid dimensions.
CORE LIMITS EXCEEDED WHILE PROCESSING PR2D INPUT	The maximum space allocated for processing input data has been overflowed. Input file is too large.
NON-ORTHOGONAL SEGMENT FOUND IN NODE XXXX.	Nonorthogonal data has been found, but the segment will be processed as a Y-axis segment.
STACK OVERFLOW IN XXXXX	A fatal overflow of available work space has occurred.
MAXIMUM NODE SIZE EXCEEDED IN XXXXX	Fatal overflow of node data storage area.
FANOUT FAILURE ON NODE XXXX	Fanout from a home segment is completely block. Routing continues with the next net.
ROUTE FAILURE ON NODE XXXX	This message accompanies the previous one. If it occurs singly, an unexplained failure to complete a route has occurred.

The following progress messages will normally be printed out in sequence.

```
..PROCESSING INPUT DATA
..BUILDING AUXILIARY INPUT FILE
..ROUTING PROCESS INITIATED
 FINAL AUXILIARY FILE IS ON I/O UNIT XX.
 PR2D OUTPUT FILE IS ON I/O UNIT XX.
..ROUTINE COMPLETE
..BUILDING PR2D OUTPUT FILE
```

TABLE 3.5 Run Time Messages

!C file OVER S:IN .

The STAR-PRINT routines consist of programs STARSCROL and STARDISP, which produce scrolls of line printer paper that are joined to form a mosaic of the STAR layout, which is a symbolic printout of the interconnection data. Like the compile routine, both of these programs are written in XEROX Basic. Therefore they are not readily transportable.

The display produced by STAR-PRINT details the array grid structure, the power bus structure, input/output and power pads, device gate positions, first metal line segments, VIAS, second metal line segments, and all net and pin identifiers. Therefore the basic instructions given in Chapter 2 still apply in reading the mosaic.

Before executing the STAR-PRINT routines, the width of the output device should be known in order to set the correct scroll size. The file which does this is called STARPAR. Several files have already been set up for commonly used output devices and the smallest STAR. These are shown in Table 3.6.

FILE	OUTPUT DEVICE
STARPAR1	132 COLUMN LINE PRINTER
STARPAR2	SILENT 700
STARPAR3	80 COLUMN CRT

TABLE 3.6. STAR-PRINT Scroll Size Files

If one of these files will not satisfy the user's need, another file can easily be created to better suit the STAR size chosen and the output device.

The format of the STARPAR file is

x y width length

where x and y are the grid points of the upper left corner of the scroll, width is the width of the scroll determined by the width of the output device, and length is the length of the scroll determined by the size of the STAR chosen. The length of the scrolls for the three STARs are: 100 for the smallest, 165 for the medium, and 260 for the largest.

For the first line of the file, x and y will both be 16. The width and length are user determined. Then on the second line, x is the value of x from the first line plus the width. The value of y will always be 16, and the width and length will remain constant. On the third line the value of x is the sum of the second x and the width, and so on. An example is shown in Figure 3.15.

```
 16   16   62   260
 78   16   62   260
140   16   62   260
202   16   62   260
164   16   62   260
```

Figure 3.15 STARPAR Example

This file can be created using the BUILD command described earlier in this chapter, or one of the existing files can be updated with the EDITOR.

The desired width file should be copied over the existing width file with the command

!C file OVER STARPAR .

The STAR-PRINT routine can now be executed by either

!BATCH J:PRINT

for the Batch mode, or

!T:PRINT

for the Demand mode. Once again it is better to use the Batch mode.

a. Program Output. The output of STAR-PRINT, as described earlier, is the STAR mosaic and is contained in file STAROUT. Figure 3.16 shows part of a mosaic created by the STAR-PRINT routine. Files LPSD and SDDO are used for diagnostic output, if any,

If after reviewing the symbolic output generated by STAR-PRINT, the user determines that the layout is correct, the mask data can be generated. If the routed output is not satisfactory, the user may choose to

1) make manual net modifications in the STAR-COMPILE output and resubmit to the STAR-ROUTE program,
2) edit the output of STAR-PLACE and manually rearrange the placement of the cells, or
3) repeat the entire design cycle beginning with the STAR-PLACE program, using the linear order option.

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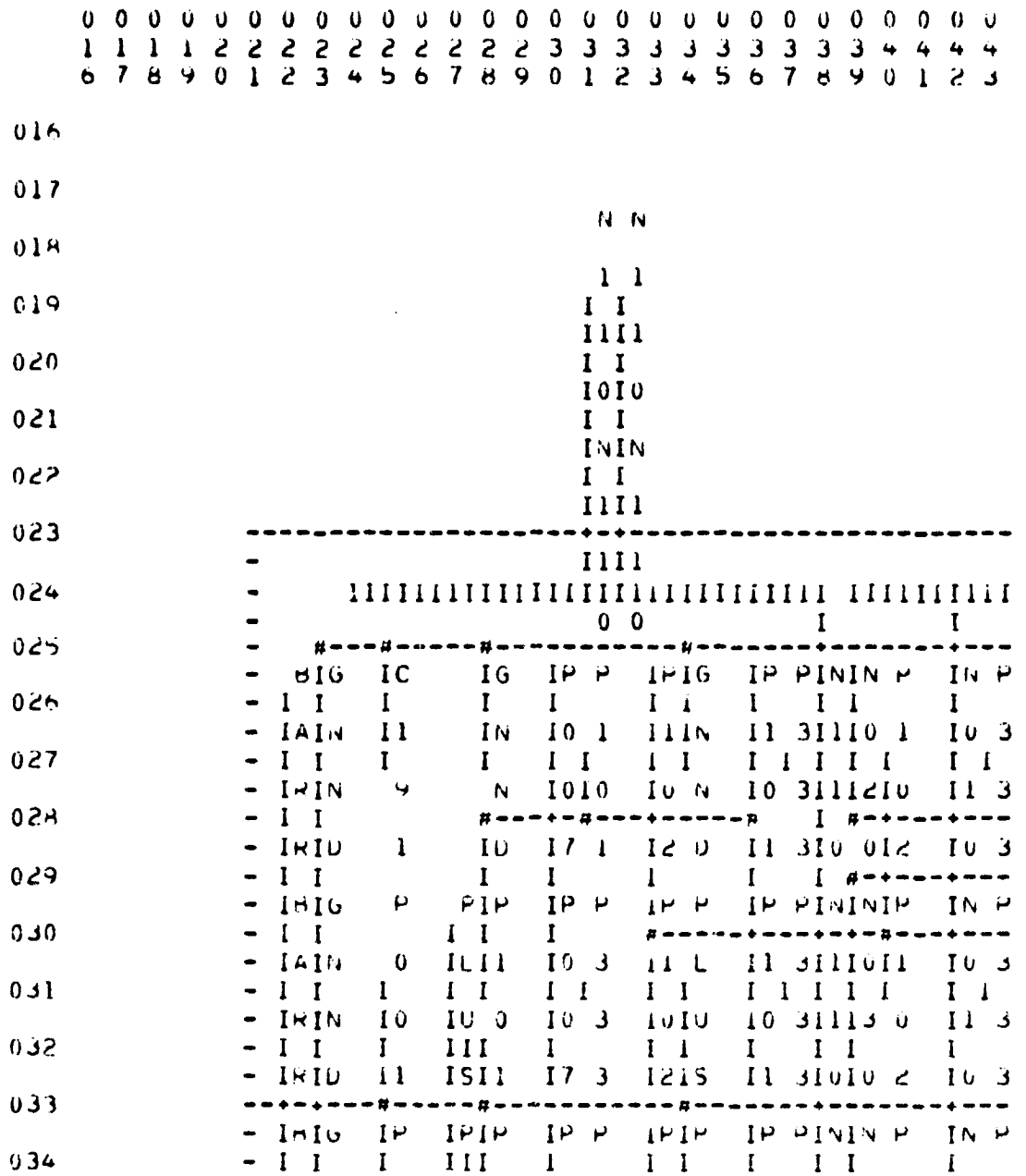

Figure 3.16 Example STAR-PRINT Output (Mosaic)

The first option requires a good understanding of the STAR-COMPILE and STAR-ROUTE outputs and is probably the hardest of the three. The second choice requires a knowledge of the format of the STAR-PLACE output file, which is described in the section on STAR-PLACE under Placement Output, with an example in Figure 3.5. The user would also have to know a more logical placement of the cells. The third method is probably the easiest, although it also requires knowing a more logical cell order, and still may not produce desirable results.

5. ARTWORK-MANART. The output from the STAR-ROUTE program is used as the input for the ARTWORK-MANART artwork generation program, which creates the mask data for the first metal layer mask, the VIA mask, and the second metal layer mask. These three masks are used to convert the STAR understructure into the user's circuit. Information on how to use the ARTWORK-MANART program can be found in NASA Contractor Report 150782.

CHAPTER 4. STAR PERIPHERY

A. INTRODUCTION

This chapter describes the structure and placement of the circuitry surrounding the Standard Transistor Array. This circuitry includes the input/output pads and the power pads. This information could prove helpful if manual placement or routing is attempted.

B. PERIPHERY STRUCTURE

The STAR periphery circuitry consist of multiple use pad cells that can be converted into input, output, and power pads, along with the STAR power structure. All examples will be in CMOS bulk metal-gate.

1. Pad Cells. The pad cells consist of side input pads, top/bottom input pads, side output pads, top/bottom output pads, side dummy pads, top/bottom output pads, side dummy pads, top/bottom dummy pads, a ground pad, and a V_{DD} pad. The dummy pads are merely unused input/output pads. The small STAR has 16 pads, the medium STAR has 36 pads, and the large STAR has 64 pads. Of these pads, two are allocated for use as power pads: V_{DD} and ground.

On the STAR symbolic display, all of these pads are represented by a string of symbols for top layer metal (IIIII). These are located around the outer edges of the array.

a. Input Pads. In the STAR input file, input pads are type 9200. For input pads placed by the STAR-PLACE program at the top or bottom of the STAR, the type numbers are unchanged, however, for input pads placed at the sides of the STAR, the type number is changed to 9100.

Each input pad has protective circuitry associated with it as shown in Figure 4.1, to protect the device against burnout resulting from accumulation of static charge on package terminals. Figure 4.1 illustrates the schematic of the input pad as well as the actual layout.

b. Output Pads. The output pads are entered in the input file as type 9210. If they are placed at the top or bottom of the array, the type numbers are not changed. For an output pad placed at the left, the type number is changed to 9110. For output pads placed at the right, the number is changed to 9120.

An output pad is shown in Figure 4.2, and from the layout it can be seen how the input circuitry is bypassed when the pad is defined as an output. Metal is used to short out the diffused resistor.

c. Ground Pad. The leftmost pad on the bottom of the STAR array is designated as the ground pad, and it does not have a type number, nor does it have to be assigned in the input file.

d. V_{DD} Pad. The rightmost pad on the top of the STAR is designated as the V_{DD} power pad. It does not have a type number, nor does it need to be assigned in the input file.

2. STAR Power Structure. The STAR is surrounded and interlaced by a power structure consisting of ground and V_{DD}, and connected to their respective pads. Figure 4.3 illustrates the STAR power structure as represented by the STAR symbolic output, as explained in Chapter 2. The pad locations for the small STAR are also shown. Although 18 pad locations are shown, only 16 are available for use. The center pads on the top and bottom of the STAR are used for testing purposes. This is true for all three STAR sizes.

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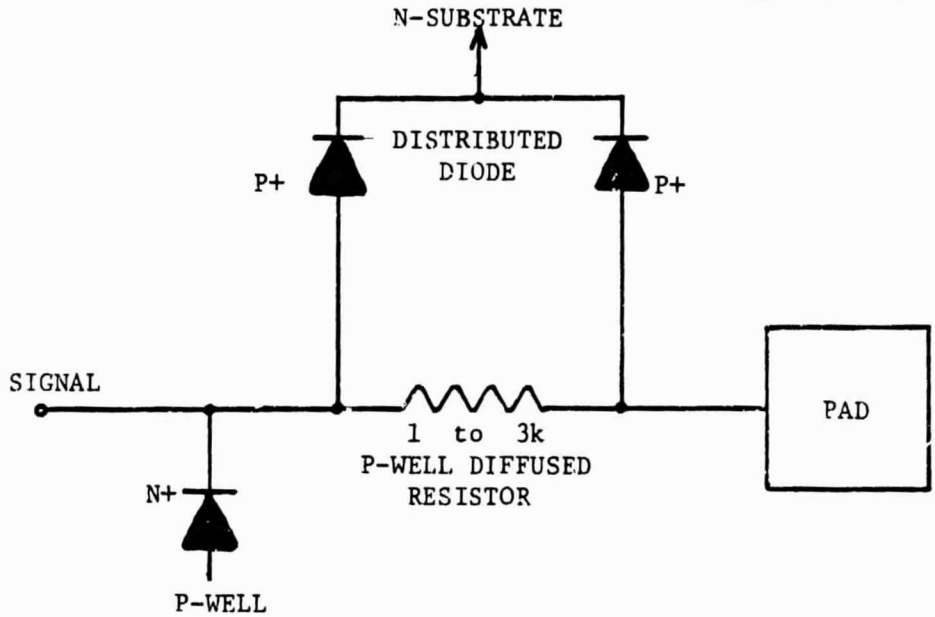

Figure 4.1(a). Metal Gate Input Pad Schematic

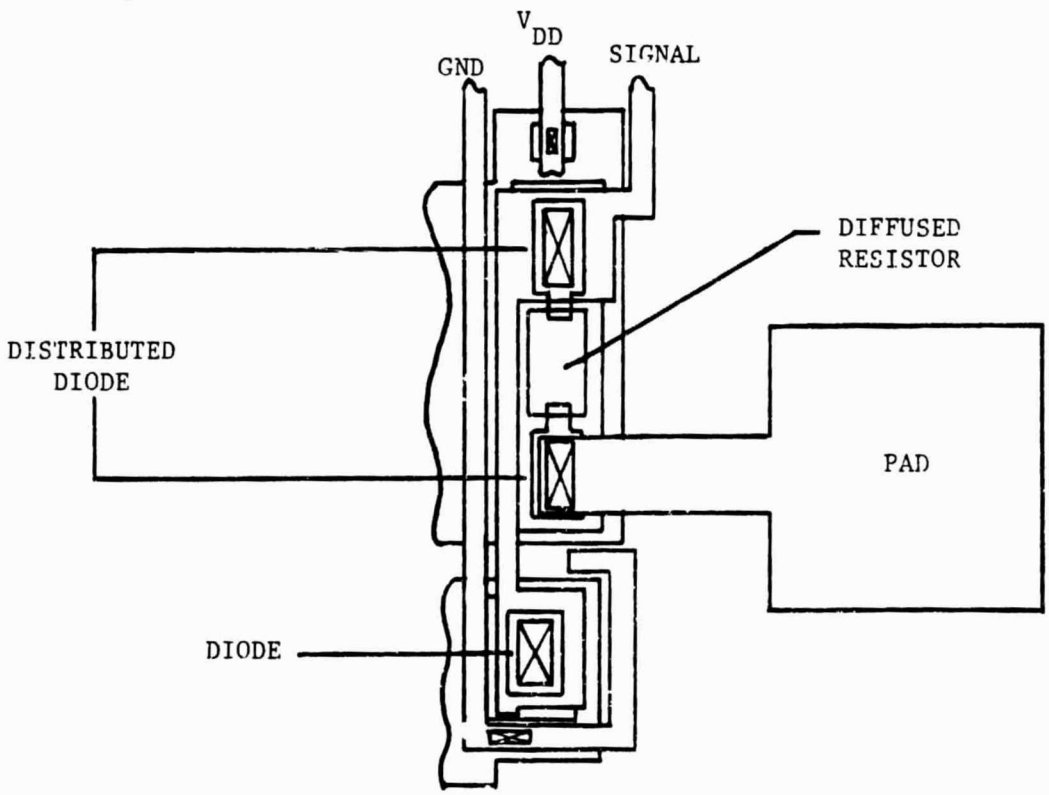

Figure 4.1(b). Metal Gate Input Pad Layout

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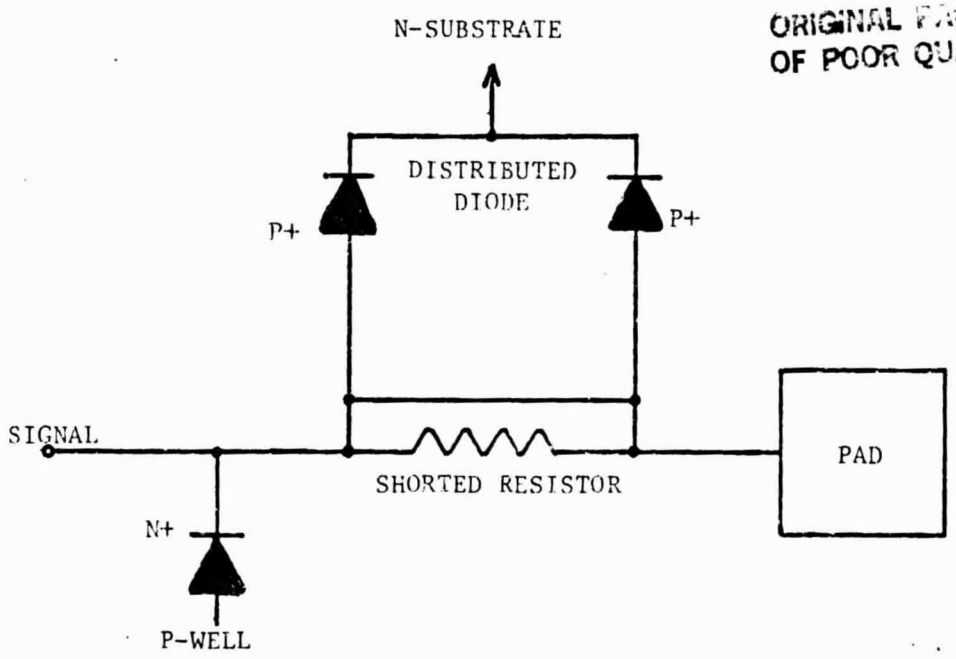

Figure 4.2(a). Metal Gate Output Pad Schematic

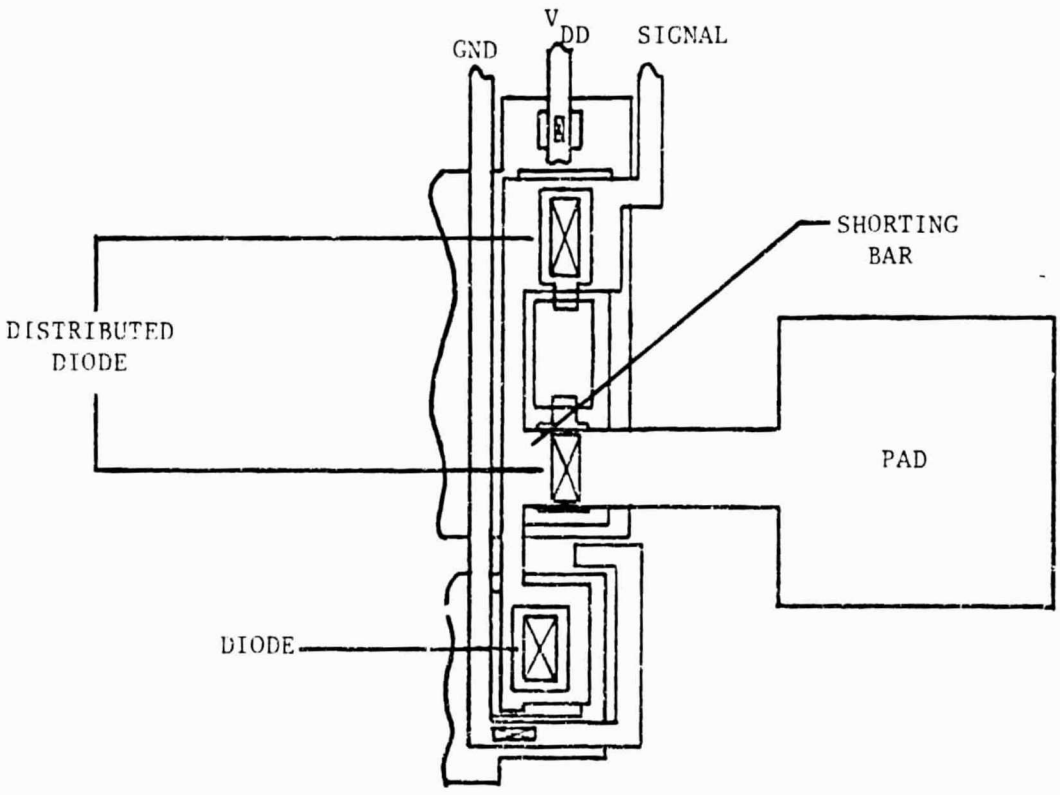

Figure 4.2(b). Metal Gate Output Pad Layout

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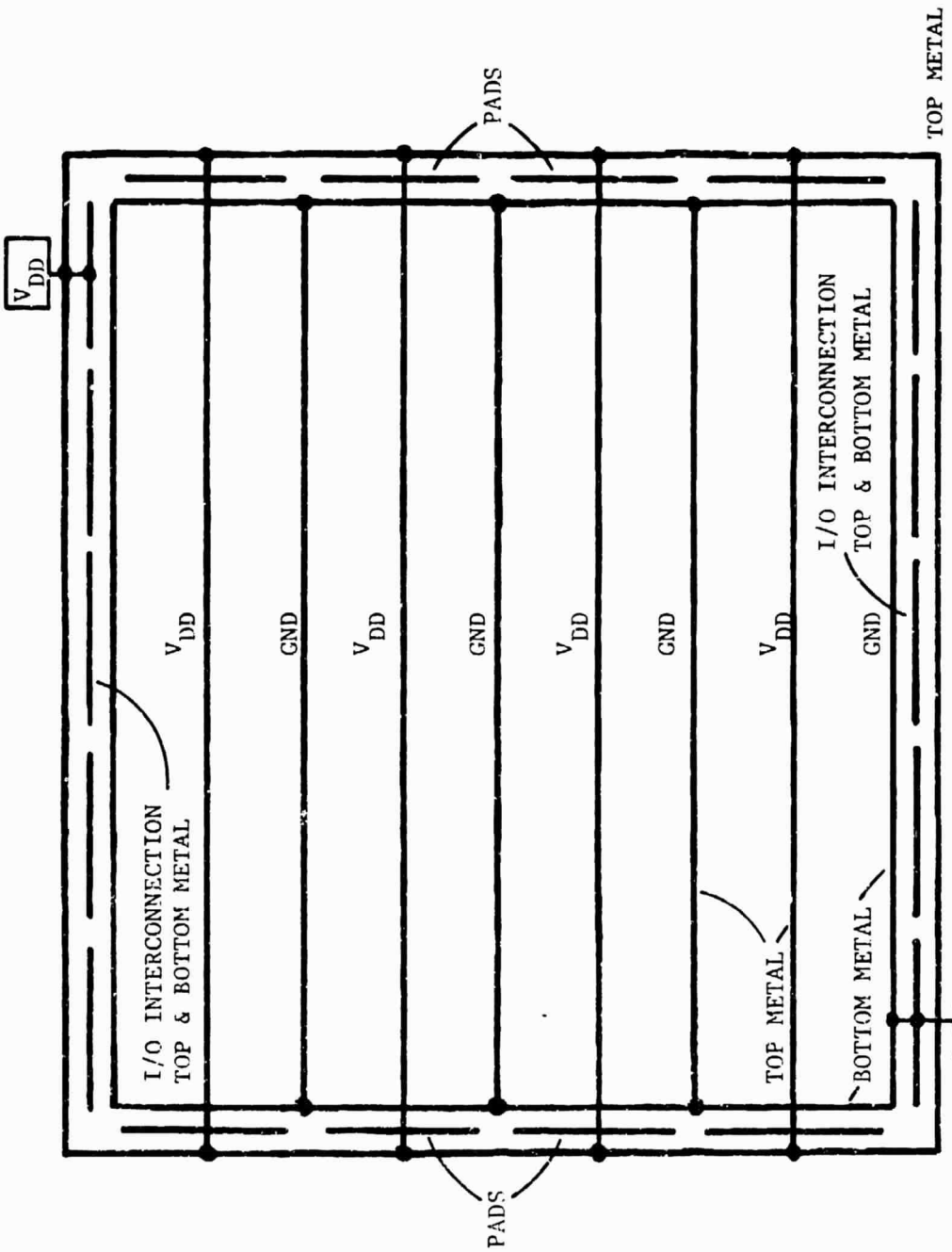

Figure 4.3. STAR Power Structure and Pad Locations

As illustrated in Figure 4.3 the horizontal parts of the power structures are top layer metal, while the vertical portions of the structure consist of bottom layer metal.

All of the pads are implemented in top layer metal except the I/O interconnection pads (in the center) which consist of both layers of metal.

More detailed pictures of the three arrays are shown in Figures 2.3-2.5, with the pads being clearly visible.

C. PAD LOCATIONS

Since the STAR is based on a grid system Tables 4.1-4.3 show the x and y locations of the pads for the three STAR structures as assigned by the STAR-PLACE program. The STAR grid system, however, begins at the point 16, 16 to allow the symbolic display of output pads on the top and left side of the array. The pad assignments are then output to the file PLACEOUT, where they can be viewed or modified if necessary. An example PLACEOUT file is shown in Figure 3.5.

The tables also contain the type numbers which are assigned to the pads by the STAR-PLACE program according to their location and function.

The minus sign in front of the y value (-25) of the top pads indicates that the pad is located above the ground power structure.

D. MODIFYING PAD LOCATIONS

If the user is not satisfied with the computer generated placement of the cells and pads, the STAR-PLACE output file, PLACEOUT, can be modified as explained in Chapter 3.

If the pad locations are to be changed, the type numbers may also have to be changed. This can be verified from the tables. The following example illustrates a modification of the pad locations and types in the PLACEOUT file.

From Figure 4.4 it can be seen that cells 6-8 are input pads with cells 6 and 7 placed at the top of the STAR and cell 8 placed on the right side. Cell 9 is an output pad placed at the bottom and cell 10 is an output pad placed at the top of the STAR.

The user would rather have all input pads on the top and all output pads on the bottom, so the locations of cells 8 and 10 must be changed. The type number of cell 8 must also be changed. The corresponding modifications are shown in Figure 4.5, emphasized by underlining.

Cell 8 has been changed to a type 9200 at location 24,-25. Cell 10 has been changed to location 24, 89.

The rest of the STAR programs can now be executed to provide routing.

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```
TITLE EXAMPLE
STAR SIZE      8    24
GATES TO PATTERNS
   999  9970
     1  1910      2  1910      3  1910      4  [illegible]      6  9200
     7  9200      8  9100      9  9210     10  [illegible]
PLACEM
0 999 0
     25       1      25       4      64 [illegible]
    -41       2      25 999011      64
     41       3      25 999011      64
    -57 999024      25
     57 999024      25
    -73 999024      25
     73 999024      25
    -89 999024      25
    -25       6      39
    -25       7      84
     25       8      96
     89       9      39
    -25      10      24
```

Figure 4.4. Original PLACEOUT File

```
TITLE EXAMPLE
STAR SIZE      8    24
GATES TO PATTERNS
   999  9970
     1  1910      2  1910      3  1910      4  [illegible]      6  9200
     7  9200      8  9200      9  9210     10  [illegible]
PLACEM
0 999 0
     25       1      25       4      64 [illegible]
    -41       2      25 999011      64
     41       3      25 999011      64
    -57 999024      25
     57 999024      25
    -73 999024      25
     73 999024      25
    -89 999024      25
    -25       6      39
    -25       7      84
    -25       8      24
     89       9      39
     89      10      24
```

Figure 4.5. Modified PLACEOUT File

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384 TRANSISTOR STAR			16 PADS	
			TYPE NUMBER IN PLACEOUT FILE	
LOCATION	x	y	INPUT	OUTPUT
TOP	24	-25	9200	9210
	39	-25	9200	9210
	69	-25	9200	9210
	84	-25	V_{DD}	V_{DD}
LEFT SIDE	17	25	9100	9110
	17	41	9100	9110
	17	57	9100	9110
	17	73	9100	9110
BOTTOM	24	89	GND	GND
	39	89	9200	9210
	69	89	9200	9210
	89	89	9200	9210
RIGHT SIDE	96	25	9100	9120
	96	41	9100	9120
	96	57	9100	9120
	96	73	9100	9120

TABLE 4.1 PAD LOCATIONS AND TYPES FOR SMALL STAR

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1728 TRANSISTOR STAR			36 PADS	
			TYPE NUMBER IN PLACEOUT FILE	
LOCATION	x	y	INPUT	OUTPUT
TOP	24	-25	9200	9210
	39	-25	9200	9210
	54	-25	9200	9210
	69	-25	9200	9210
	84	-25	9200	9210
	114	-25	9200	9210
	129	-25	9200	9210
	144	-25	9200	9210
	159	-25	9200	9210
	174	-25	V_{DD}	V_{DD}
LEFT SIDE	17	25	9100	9110
	17	41	9100	9110
	17	57	9100	9110
	17	73	9100	9110
	17	89	9100	9110
	17	105	9100	9110
	17	121	9100	9110
	17	137	9100	9110

TABLE 4.2. PAD LOCATIONS AND TYPES FOR MEDIUM STAR

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1728 TRANSISTOR STAR			36 PADS	
			TYPE NUMBER IN PLACEOUT FILE	
LOCATION	x	y	INPUT	OUTPUT
BOTTOM	24	153	GND	GND
	39	153	9200	9210
	54	153	9200	9210
	69	153	9200	9210
	84	153	9200	9210
	114	153	9200	9210
	129	153	9200	9210
	144	153	9200	9210
	159	153	9200	9210
	174	153	9200	9210
RIGHT SIDE	186	25	9100	9120
	186	41	9100	9120
	186	57	9100	9120
	186	73	9100	9120
	186	89	9100	9120
	186	105	9100	9120
	186	121	9100	9120
	186	137	9100	9120

TABLE 4.2 (Continued). PAD LOCATIONS AND TYPES FOR MEDIUM STAR

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5264 TRANSISTOR STAR			64 PADS	
			TYPE NUMBER IN PLACEOUT FILE	
LOCATION	x	y	INPUT	OUTPUT
TOP	24	-25	9200	9210
	39	-25	9200	9210
	54	-25	9200	9210
	69	-25	9200	9200
	84	-25	9200	9210
	99	-25	9200	9210
	114	-25	9200	9210
	129	-25	9200	9210
	144	-25	9200	9210
	179	-25	9200	9210
	189	-25	9200	9210
	204	-25	9200	9210
	219	-25	9200	9210
	234	-25	9200	9210
	249	-25	9200	9210
	264	-25	9200	9210
	279	-25	9200	9210
	294	-25	V_{DD}	V_{DD}

TABLE 4.3. PAD LOCATIONS AND TYPES FOR LARGE STAR

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5264 TRANSISTOR STAR			64 PADS	
			TYPE NUMBER IN PLACEOUT FILE	
LOCATION	x	y	INPUT	OUTPUT
LEFT SIDE	17	25	9100	9110
	17	41	9100	9110
	17	57	9100	9110
	17	73	9100	9110
	17	89	9100	9110
	17	105	9100	9110
	17	121	9100	9110
	17	137	9100	9110
	17	153	9100	9110
	17	169	9100	9110
	17	185	9100	9110
	17	201	9100	9110
	17	217	9100	9110
	17	233	9100	9110
BOTTOM	24	249	GND	GND
	39	249	9200	9210
	54	249	9200	9210
	69	249	9200	9210
	84	249	9200	9210
	99	249	9200	9210
	114	249	9200	9210

TABLE 4.3 (Continued). PAD LOCATIONS AND TYPES FOR LARGE STAR

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5264 TRANSISTOR STAR			64 PADS	
			TYPE NUMBER IN PLACEOUT FILE	
LOCATION	x	y	INPUT	OUTPUT
BOTTOM	129	249	9200	9210
	144	249	9200	9210
	174	249	9200	9210
	189	249	9200	9210
	204	249	9200	9210
	219	249	9200	9210
	234	249	9200	9210
	249	249	9200	9210
	264	249	9200	9210
	279	249	9200	9210
	294	249	9200	9210
RIGHT SIDE	306	25	9100	9120
	306	41	9100	9120
	306	57	9100	9120
	306	73	9100	9120
	306	89	9100	9120
	306	105	9100	9120
	306	121	9100	9120
	306	137	9100	9120
	306	153	9100	9120

TABLE 4.3 (Continued). PAD LOCATIONS AND TYPES FOR LARGE STAR

5264 TRANSISTOR STAR			64 PADS	
			TYPE NUMBER IN PLACEOUT FILE	
LOCATION	x	y	INPUT	OUTPUT
RIGHT SIDE	306	169	9100	9120
	306	185	9100	9120
	306	201	9100	9120
	306	217	9100	9120
	306	233	9100	9120

TABLE 4.3 (Continued). PAD LOCATIONS AND TYPES FOR LARGE STAR

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CHAPTER 5. STAR-CELL SIMULATION

A. INTRODUCTION

This chapter briefly describes how the dynamic performance data for the STAR logic cell family were obtained and the circuit simulation program used. A table is included which lists all of the derived STAR device model parameters used in the simulation program. A more detailed analysis of the derivation of the parameters and the simulation is to be documented in a later report.

B. PROGRAM AND MODEL CHOICE

The circuit simulation program SPICE was selected for the simulation of the dynamic response of the standard cells contained in the STAR library because of its capability to handle nonlinear transient analysis and the device models it provides. The physical parameters for the NASA process specification dated January 22, 1980.

The MOSFET model used in SPICE is very similar to the model proposed by Shichman and Hodges [9]. It includes a representation of the effect of substrate bias on threshold voltage and the channel length modulation effect.

The SPICE device model, as used, provides an adequate d.c. representation of MOSFET devices without excessive complexity as long as the MOSFET devices are not in the short-channel region of operation.

C. STAR Device Model Parameters

The complete STAR parameters used in the SPICE program are tabulated below in Table 5.1.

PARAMETER	NMOS	UNITS	PMOS
V_{TO}	1.07	Volts	-1.26
ϕ	.71	Volts	- .58
β	45.3×10^{-6}	$A/Volts^2$	-22.1×10^{-6}
γ	1.61	$Volts^{\frac{1}{2}}$	-.43
R_D	10	Ω	20
R_S	10	Ω	20
C_{GS}	.1	pf	.1
C_{GD}	.1	pf	.1
C_{GB}	.0	pf	.1
C_{BD}	.2463	pf	.0681
C_{BS}	.2463	pf	.0681
$PB = \phi_B = \chi_0$	.7288	Volts	-.6178
I_S	10^{-14}	Amps	10^{-14}

TABLE 5.1 SPICE Model Parameters for STAR

D. Circuit Simulation

1. Description of SPICE. SPICE, the program chosen for use, is a general purpose simulation program for integrated circuits. It contains the three basic analysis capabilities which provide the bulk of information of a circuit's performance: a) non-linear d.c. analysis, with the provision of "stepping" an input source to obtain a set of static transfer curves, b) small-signal, sinusoidal steady-state analysis, and c) nonlinear, time-domain transient analysis.

Built-in models are included for the most common semiconductor devices: diodes, bipolar junction transistors (BJT's), junction field-effect transistors (JFET's), and metal-oxide-semiconductor field-effect transistors (MOSFET's). The BJT models are based on the model of either Gummel-Poon or Ebers-Moll, and the models for the FET's are derived from the formulations of Shichman and Hodges.

2. Procedure for Generating Dynamic Data. Each standard cell was analyzed with a capacitive load which approximates the gate capacitance of the load and the stray capacitance of the metal interconnections. A unit load, or fan-out of 1, is defined as 0.56 pf, and therefore additional fan-outs are just multiple values of 0.56 pf.

The input signal to the circuits during the generation of the dynamic data was the output of an inverter stage which acted as a buffer against the programmed input pulse. Therefore this buffer minimizes the effect of the transition time of the input of the dynamic data. Figure 5.1 illustrates the circuit configuration used to test the logic cells.

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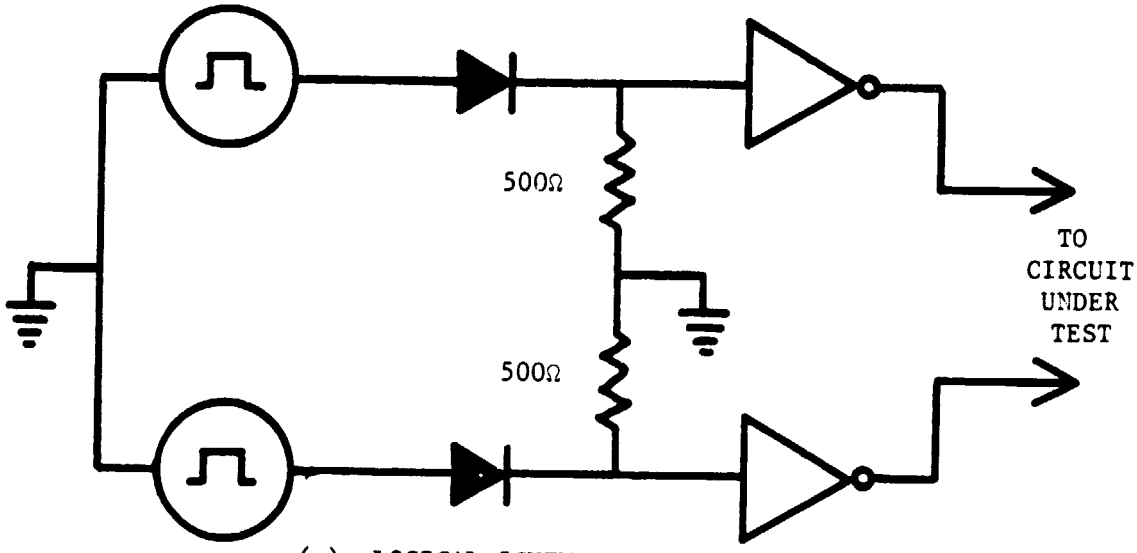
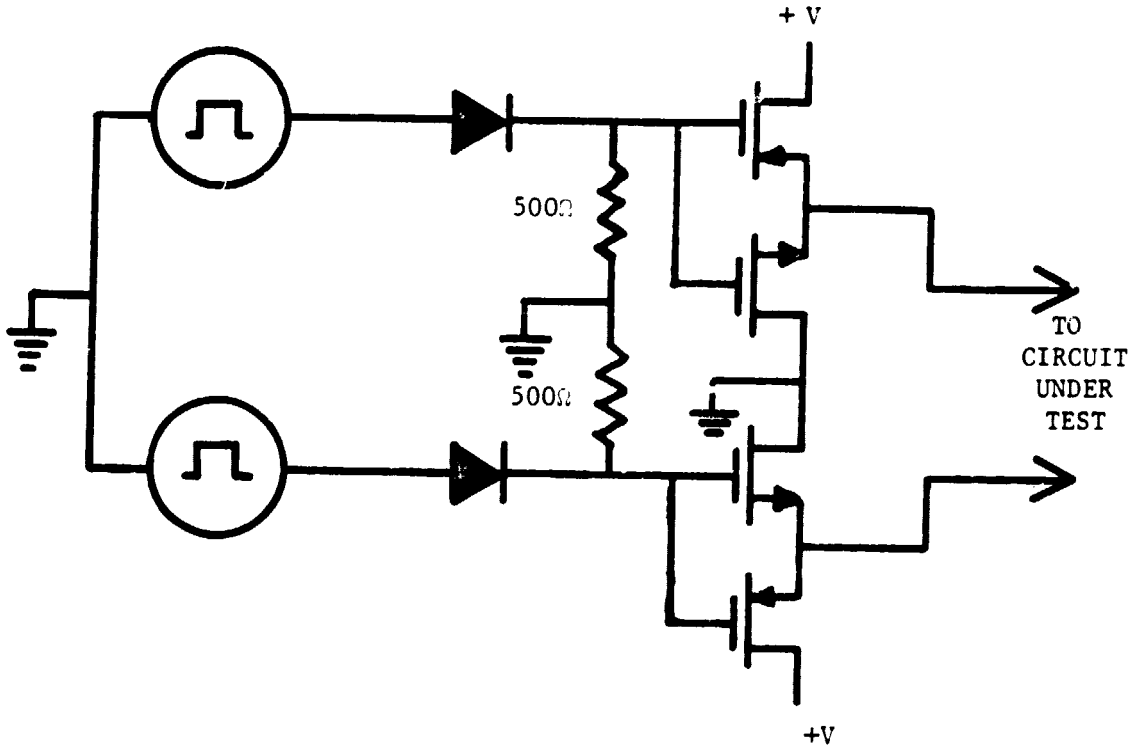


(a) LOGICAL SCHEMATIC

Figure 5.1 SPICE Input Circuit Configuration

(b) CIRCUIT SCHEMATIC



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From experimental simulations at fan-outs ranging from 1 to 8, it was found that the transition times and propagation delays were approximately linear. Therefore only fan-outs of 1 and 8 at supply voltages of 4,5,6 and 10 volts d.c. were used in all subsequent simulations. The data obtained from these simulations is shown in Table 5.2 for each of the STAR cells.

From plotting this data over the operating voltage range it was found that a power curve of the form

$$y = ax^b$$

provided an almost perfect fit, where a and b are of the form

$$a = \exp\left[\frac{\sum \ln y_i}{n} - b\,\frac{\sum \ln x_i}{n}\right]$$

$$b = \frac{\sum(\ln x_i)(\ln y_i) - \dfrac{(\sum \ln x_i)(\sum \ln y_i)}{n}}{\sum(\ln x_i)^2 - \dfrac{(\sum \ln x_i)^2}{n}}$$

and x is the value being used for V_{DD}.

The equations describing the dynamic performance curves shown in the Appendix are given in Table 5.3, with v substituted for x.

Therefore, it is seen that the dynamic performance data can be obtained in three ways. The values can be read directly from the curves, or for more precise values, the equations in Table 5.3 can be utilized. However, if a V_{DD} of 4,5,6 or 10 volts was used the corresponding values can be found directly from Table 5.2.

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CELL	V_{DD}	MEASURED TRANSITION DELAYS				MEASURED PROPAGATION DELAYS			
		T_{OR}	T_{1R}	T_{OF}	T_{1F}	T_{OHL}	T_{1LH}	T_{OHL}	T_{1HL}
1120	4	41.4	30.2	16.6	6.2	42.3	15.0	15.0	2.8
	5	29.1	20.9	11.6	4.8	37.6	10.4	8.4	2.2
	6	22.6	16.0	9.4	3.6	26.4	7.8	5.6	2.0
	10	10.0	8.4	5.7	1.8	11.3	3.8	4.4	.8
1130	4	105.1	46.1	24.5	6.4	71.9	22.8	16.0	2.8
	5	71.3	31.8	15.4	5.0	49.6	14.6	11.6	2.0
	6	39.9	26.7	12.4	3.6	36.0	11.2	8.7	1.8
	10	26.0	12.6	4.1	2.2	17.0	5.6	7.9	.1
1140	4	146.1	61.5	24.1	6.9	104.7	29.8	15.9	2.9
	5	98.3	43.0	17.6	4.8	69.7	20.0	10.6	2.0
	6	73.3	33.2	12.1	4.1	51.3	15.0	8.9	1.5
	10	35.9	16.9	6.3	2.4	23.6	7.6	3.4	.8
1220	4	26.1	13.9	26.3	15.0	23.4	6.4	21.4	7.8
	5	18.0	9.8	18.3	10.8	14.7	4.6	11.9	5.7
	6	14.7	7.4	13.0	8.4	10.6	3.6	9.9	4.3
	10	7.1	4.1	6.9	4.3	4.7	1.8	5.6	2.0
1230	4	35.1	13.9	45.9	23.9	26.1	6.9	36.0	12.6
	5	25.1	9.7	33.0	16.8	17.7	4.6	23.9	8.6
	6	19.6	7.6	24.6	13.2	12.4	3.6	18.1	6.9
	10	10.3	3.8	13.8	6.6	5.6	2.0	8.7	3.2
1240	4	42.3	14.1	72.0	32.8	28.9	7.1	55.7	17.2
	5	30.9	10.0	51.4	23.2	19.6	4.8	37.3	12.2
	6	24.7	7.4	39.3	17.8	14.4	3.6	28.6	9.0
	10	13.1	4.1	19.3	9.4	6.6	2.0	13.9	4.5

Table 5.2. Metal Gate Dynamic Performance Data

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CELL	V_{DD}	MEASURED TRANSITION DELAYS				MEASURED PROPAGATION DELAYS			
		T_{OR}	T_{1R}	T_{OF}	T_{1F}	T_{OLH}	T_{1LH}	T_{OHL}	T_{1HL}
1300	4	24.0	19.2	16.1	6.8	16.1	9.6	14.0	4.2
	5	16.5	14.2	13.2	5.5	12.3	7.1	9.5	3.3
	6	11.1	11.0	11.9	4.4	9.1	4.0	5.1	2.6
	10	5.1	5.4	5.3	2.4	4.4	2.2	3.7	.4
1310	4	14.0	7.0	13.6	3.4	13.3	3.8	11.3	2.4
	5	10.6	4.8	13.7	1.8	9.3	2.4	7.9	1.6
	6	7.3	3.8	7.4	2.2	6.7	1.8	5.0	1.4
	10	4.9	1.5	4.3	1.0	2.3	1.0	2.4	.8
1330	4	48.0	27.0	28.6	14.6	12.0	7.8	11.6	6.2
	5	31.6	17.4	20.3	12.1	8.2	5.6	7.6	4.8
	6	23.7	14.4	14.1	8.2	5.4	3.6	4.7	3.2
	10	12.9	7.2	10.6	3.4	1.7	1.8	3.1	1.2
1360	4	21.0	2.8	30.0	1.4	19.7	1.8	15.7	1.8
	5	15.7	1.8	22.4	.3	13.1	1.2	8.0	1.4
	6	13.3	1.0	17.6	.6	8.3	1.0	5.3	1.0
	10	7.4	.8	10.7	.4	4.9	.1	.6	.6
1520	4	17.4	3.6	22.7	1.8	17.4	2.2	14.7	1.8
	5	13.3	2.4	16.1	1.2	10.9	1.6	9.7	1.4
	6	10.7	1.8	13.4	.8	8.7	1.8	5.3	1.0
	10	6.4	.8	7.6	.6	3.7	.4	1.4	.8
1620	4	18.0	13.4	12.7	6.0	42.9	7.1	30.4	3.6
	5	12.0	9.8	8.9	4.4	27.3	5.2	20.1	2.6
	6	9.7	7.4	7.7	3.2	21.4	3.6	15.7	1.8
	10	5.3	3.8	4.7	1.8	9.7	1.8	6.1	1.3

Table 5.2(Continued). Metal Gate Dynamic Performance Data

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CELL	V_{DD}	MEASURED TRANSITION DELAYS				MEASURED PROPAGATION DELAYS			
		T_{OR}	T_{1R}	T_{OF}	T_{1F}	T_{OHL}	T_{1LH}	T_{OHL}	T_{1HL}
1630	4	23.3	13.6	12.6	6.2	59.3	8.0	33.1	4.1
	5	17.3	9.4	8.9	6.2	39.1	5.4	22.1	2.6
	6	12.9	7.1	7.7	3.2	29.1	4.1	16.6	2.0
	10	7.3	3.8	4.7	1.8	13.6	2.0	7.4	.8
1640	4	28.9	14.1	12.4	6.4	77.7	8.8	33.0	4.2
	5	19.9	10.0	8.6	4.8	51.7	6.0	23.1	2.6
	6	16.6	7.6	7.4	3.6	37.9	4.3	17.6	2.0
	10	9.1	4.1	5.9	1.5	17.4	2.2	8.4	.8
1720	4	13.1	13.9	19.3	6.6	30.1	6.9	54.4	5.0
	5	9.0	9.8	13.6	4.8	19.6	4.8	35.6	3.4
	6	6.6	7.6	10.3	3.8	14.4	3.6	27.3	2.4
	10	4.3	3.8	6.7	1.8	6.7	1.8	9.7	1.8
1730	4	25.4	19.0	31.4	13.4	44.4	9.2	115.3	9.4
	5	18.3	14.1	25.0	8.1	30.6	7.2	70.0	6.1
	6	12.4	10.6	21.7	6.0	21.4	5.0	57.3	3.8
	10	7.1	5.4	11.9	3.0	9.0	2.8	35.6	2.0
1740	4	26.0	19.6	47.3	10.8	45.0	7.0	152.7	9.8
	5	19.4	15.0	34.6	8.1	37.1	5.3	123.6	7.1
	6	13.4	10.6	27.1	6.8	22.3	4.2	73.6	4.3
	10	7.1	5.4	14.9	3.0	10.1	2.8	32.9	3.1
1820	4	99.1	48.8	69.4	14.8	63.7	14.4	57.3	6.7
	5	76.9	21.2	47.7	11.8	40.3	9.4	35.3	6.5
	6	58.3	16.4	36.3	10.8	32.0	7.0	28.1	4.0
	10	19.4	13.2	21.0	4.2	23.4	3.6	13.6	2.0

Table 5.2(Continued). Metal Gate Dynamic Performance Data

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CELL	V_{DD}	MEASURED TRANSITION DELAYS				MEASURED PROPAGATION DELAYS			
		T_{OR}	T_{1R}	T_{OF}	T_{1F}	T_{OHL}	T_{1LH}	T_{OHL}	T_{1HL}
1830	4	26.4	10.6	30.7	10.2	61.3	17.8	84.0	20.6
	5	18.3	7.2	25.4	7.1	40.8	12.1	48.9	13.3
	6	15.9	5.8	19.0	5.6	30.7	10.2	36.7	10.2
	10	8.9	3.0	12.1	2.6	12.0	4.2	17.1	5.4
1900	4	79.6	27.2	68.6	11.8	79.1	15.2	57.0	8.4
	5	65.3	17.8	51.4	10.6	39.7	10.2	30.9	5.8
	6	53.3	16.4	43.7	7.4	28.6	7.6	21.9	4.4
	10	27.9	8.6	24.6	3.4	15.4	3.6	10.6	2.0
1910	4	141.1	33.4	83.0	18.2	72.4	21.8	165.0	7.0
	5	76.9	21.2	47.6	10.4	33.0	16.4	98.2	5.4
	6	63.6	14.6	36.4	7.8	29.9	7.2	73.4	3.6
	10	31.3	8.0	18.9	4.4	13.7	4.6	42.9	1.6
1920	4	110.1	30.6	72.0	18.2	57.7	14.4	155.0	7.0
	5	76.7	21.4	57.9	10.0	42.5	10.3	105.1	5.2
	6	58.4	16.2	45.0	8.4	28.6	7.6	74.4	3.6
	10	29.1	7.8	25.3	3.8	13.7	4.6	43.9	1.6
2310	4	40.3	30.4	28.3	13.6	32.7	14.4	23.0	7.0
	5	25.9	19.8	20.9	10.0	23.3	12.2	13.0	4.2
	6	20.4	14.8	15.6	7.6	16.3	6.6	10.3	3.8
	10	11.0	8.4	9.3	3.8	7.4	3.6	4.7	1.8

Table 5.2(Continued). Metal Gate Dynamic Performance Data

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CELL NO.	OUTPUT DELAY EQUATIONS			
	T_{OR} =	T_{IR} =	T_{OF} =	T_{IF} =
1120	$354.61(v)^{-1.55}$	$196.74(v)^{-1.38}$	$75.44(v)^{-1.14}$	$41.94(v)^{-1.37}$
1130	$784.09(v)^{-1.52}$	$313.95(v)^{-1.40}$	$363.98(v)^{-1.94}$	$31.99(v)^{-1.17}$
1140	$1150.20(v)^{-1.52}$	$414.59(v)^{-1.40}$	$182.42(v)^{-1.47}$	$30.77(v)^{-1.12}$
1220	$178.36(v)^{-1.40}$	$82.86(v)^{-1.32}$	$189.00(v)^{-1.45}$	$96.76(v)^{-1.36}$
1230	$215.66(v)^{-1.33}$	$94.63(v)^{-1.40}$	$269.26(v)^{-1.30}$	$161.09(v)^{-1.39}$
1240	$242.17(v)^{-1.27}$	$86.49(v)^{-1.34}$	$518.04(v)^{-1.43}$	$207.26(v)^{-1.35}$
1300	$246.77(v)^{-1.70}$	$131.80(v)^{-1.39}$	$95.26(v)^{-1.23}$	$34.25(v)^{-1.15}$
1310	$65.02(v)^{-1.16}$	$72.75(v)^{-1.68}$	$98.36(v)^{-1.36}$	$16.37(v)^{-1.21}$
1330	$314.46(v)^{-1.40}$	$178.44(v)^{-1.40}$	$112.04(v)^{-1.06}$	$155.26(v)^{-1.65}$
1360	$98.58(v)^{-1.13}$	$15.20(v)^{-1.34}$	$135.80(v)^{-1.11}$	$7.07(v)^{-1.29}$
1520	$76.70(v)^{-1.08}$	$33.69(v)^{-1.63}$	$110.20(v)^{-1.17}$	$7.94(v)^{-1.16}$
1620	$102.68(v)^{-1.30}$	$89.15(v)^{-1.38}$	$51.15(v)^{-1.05}$	$35.93(v)^{-1.31}$
1630	$131.29(v)^{-1.26}$	$87.55(v)^{-1.37}$	$50.45(v)^{-1.04}$	$38.05(v)^{-1.34}$
1640	$151.97(v)^{-1.23}$	$86.89(v)^{-1.34}$	$31.35(v)^{-0.75}$	$61.62(v)^{-1.60}$
1720	$62.33(v)^{-1.19}$	$95.49(v)^{-1.41}$	$85.73(v)^{-1.13}$	$47.23(v)^{-1.42}$
1730	$167.50(v)^{-1.39}$	$127.77(v)^{-1.38}$	$138.75(v)^{-1.06}$	$111.30(v)^{-1.59}$
1740	$186.22(v)^{-1.43}$	$142.47(v)^{-1.43}$	$262.04(v)^{-1.25}$	$78.04(v)^{-1.40}$
1320	$1371.55(v)^{-1.82}$	$204.68(v)^{-1.27}$	$385.11(v)^{-1.28}$	$109.77(v)^{-1.39}$
1830	$124.48(v)^{-1.15}$	$66.20(v)^{-1.35}$	$128.23(v)^{-1.03}$	$78.68(v)^{-1.48}$
1900	$413.53(v)^{-1.16}$	$136.90(v)^{-1.21}$	$312.96(v)^{-1.11}$	$93.52(v)^{-1.42}$
1910	$1088.83(v)^{-1.56}$	$255.32(v)^{-1.53}$	$635.96(v)^{-1.55}$	$124.26(v)^{-1.48}$
1920	$791.25(v)^{-1.44}$	$235.50(v)^{-1.48}$	$361.46(v)^{-1.16}$	$158.46(v)^{-1.64}$
2310	$252.43(v)^{-1.38}$	$187.17(v)^{-1.37}$	$145.49(v)^{-1.21}$	$93.57(v)^{-1.39}$

Table 5.3. Metal Gate Dynamic Performance Curve Equations

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CELL NO.	PROPAGATION DELAY EQUATIONS			
	T_{OLH} =	T_{1LH} =	T_{OHL} =	T_{1HL} =
1120	$380.44(v)^{-1.51}$	$115.49(v)^{-1.49}$	$69.26(v)^{-1.26}$	$20.48(v)^{-1.38}$
1130	$620.11(v)^{-1.57}$	$171.33(v)^{-1.50}$	$38.71(v)^{-0.73}$	$789.44(v)^{-3.76}$
1140	$950.29(v)^{-1.61}$	$219.01(v)^{-1.47}$	$162.67(v)^{-1.67}$	$19.04(v)^{-1.39}$
1220	$244.29(v)^{-1.73}$	$42.70(v)^{-1.38}$	$125.31(v)^{-1.38}$	$62.18(v)^{-1.49}$
1230	$261.80(v)^{-1.68}$	$40.26(v)^{-1.32}$	$288.74(v)^{-1.53}$	$96.11(v)^{-1.48}$
1240	$261.19(v)^{-1.60}$	$43.95(v)^{-1.36}$	$426.39(v)^{-1.46}$	$138.53(v)^{-1.51}$
1300	$119.49(v)^{-1.43}$	$90.20(v)^{-1.64}$	$92.05(v)^{-1.45}$	$217.77(v)^{-2.66}$
1310	$204.41(v)^{-1.94}$	$24.75(v)^{-1.42}$	$117.12(v)^{-1.70}$	$11.10(v)^{-1.15}$
1330	$253.97(v)^{-2.16}$	$71.77(v)^{-1.62}$	$73.84(v)^{-1.42}$	$85.43(v)^{-1.84}$
1360	$145.63(v)^{-1.50}$	$209.62(v)^{-3.23}$	$2596.99(v)^{-3.59}$	$9.45(v)^{-1.21}$
1520	$166.88(v)^{-1.66}$	$34.82(v)^{-1.87}$	$594.29(v)^{-2.62}$	$5.62(v)^{-0.88}$
1620	$373.27(v)^{-1.59}$	$57.04(v)^{-1.51}$	$341.48(v)^{-1.74}$	$15.05(v)^{-1.09}$
1630	$517.41(v)^{-1.59}$	$61.45(v)^{-1.50}$	$306.95(v)^{-1.62}$	$46.22(v)^{-1.75}$
1640	$712.72(v)^{-1.62}$	$67.63(v)^{-1.50}$	$255.16(v)^{-1.49}$	$48.21(v)^{-1.78}$
1720	$272.93(v)^{-1.62}$	$50.56(v)^{-1.46}$	$745.68(v)^{-1.88}$	$19.79(v)^{-1.08}$
1730	$501.84(v)^{-1.75}$	$57.04(v)^{-1.32}$	$993.90(v)^{-1.60}$	$89.51(v)^{-1.68}$
1740	$498.07(v)^{-1.69}$	$26.18(v)^{-0.99}$	$1781.60(v)^{-1.74}$	$50.99(v)^{-1.25}$
1820	$229.87(v)^{-1.03}$	$106.40(v)^{-1.49}$	$442.54(v)^{-1.53}$	$52.86(v)^{-1.41}$
1830	$720.34(v)^{-1.78}$	$155.74(v)^{-1.56}$	$797.89(v)^{-1.69}$	$138.83(v)^{-1.43}$
1900	$691.13(v)^{-1.69}$	$127.51(v)^{-1.56}$	$585.29(v)^{-1.77}$	$72.17(v)^{-1.56}$
1910	$631.13(v)^{-1.69}$	$231.70(v)^{-1.75}$	$1030.74(v)^{-1.41}$	$71.16(v)^{-1.65}$
1920	$522.35(v)^{-1.59}$	$75.17(v)^{-1.23}$	$943.37(v)^{-1.36}$	$68.83(v)^{-1.63}$
2310	$313.85(v)^{-1.63}$	$132.55(v)^{-1.58}$	$212.32(v)^{-1.67}$	$46.53(v)^{-1.42}$

Table 5.3 (Continued). Metal Gate Dynamic Performance Curve Equations

APPENDIX

A. Introduction

This appendix contains the data sheets of the cells that currently comprise the STAR Standard Cell Library. The information that is given on the data sheets is described along with an explanation of how to interpret the dynamic performance curves.

B. Data Sheets

Data Sheets are given for each of the cells listed in Table 2.1. Each data sheet contains the following information:

- Cell family technology.
- Descriptive name of the cell indicating its function.
- Cell identification or pattern number. This number identifies the cell in the input data to the automatic placement and routing program.
- Number of devices comprising each cell and the number of pins each cell has.
- Width of the cell in grids (1 grid = 0.8 mils).
- Logic symbol, including pin numbers by which the net list is generated, plus the Boolean equation describing the cell function.
- Cell truth table.

- Circuit schematic of the logic configuration as it relates to the actual STAR cell, including the labeling of each input and output node.
- Dynamic performance data as functions of supply voltage.
- Legends on how to interpret the dynamic data including equations for use with the data from the curves to obtain the overall results.
- Capacitance at each input connection in both absolute units and values normalized about 0.56 pF.

Dynamic performance data for the logic cells are given in the form of curves showing transition times and propagation delays as functions of supply voltage. These curves were generated from the data shown in Table 5.2. The equations for the curves are given in Table 5.3. The transition time is measured over the 10 to 90 percent rise and fall times. The transition graph is comprised of four curves. The curve labeled T_{OR} is the rise time if the device was driving no load. The curve labeled T_{1R} is the additional rise time if the device was driving a single load of 0.56 pF. To obtain the total rise time, add the time obtained from the T_{OR} curve at the desired voltage to the time obtained from the T_{IR} curve at the same voltage, multiplied by the desired fan-out (F/O). The fan-out is the normalized load that the cell under consideration is driving. The same procedure holds for the fall-time curves (T_{OF} and T_{1F}).

Because of space limitations only one of the rise curves and one of the fall curves on each graph could be labeled. If two curves overlap, both labels are given in the order of the position of the curves.

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For example, to determine the rise and fall times of a two-input NOR cell (1120) driving a total load of 4.30 pF for a normalized load of 7.68, at V_{DD} = 10v, the following values would be obtained from the graph for the 1120.

T_{OR} = 10 ns T_{OF} = 6 ns

T_{IR} = 8 ns T_{IF} = 2 ns

These values would be used in the following equations to obtain the overall results.

$T_R = T_{OR} + T_{IR}(F/O)$ $T_F = T_{OF} + T_{IF}(F/O)$

$= 10 + (8)(7.68)$ $= 6 + (2)(7.68)$

$= 71.4$ ns $= 21.4$ ns

The propagation delays were measured at the 50 percent signal swing level for positive and negative going input signals. The previous explanation is valid for these curves, where T_{OLH} is the low to high propagation delay for no load and T_{OHL} is the high to low propagation delay for no load. T_{ILH} and T_{IHL} are the additional delays for a single load.

On the reverse side of the data sheets are the STAR symbolic displays of each of the cells that can be displayed. Presently, the pads cannot be displayed.

The cells appear as they are displayed by the STARLIBLIS program without the tabular listing of the segment data. The symbolic displays of the cells are explained in Chapter 2.

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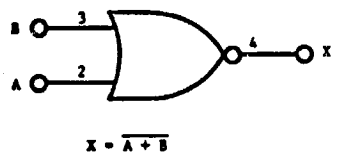
2-INPUT NOR GATE

STAR STANDARD CELL NO. 1120

6 DEVICES
3 PINS CELL WIDTH = 3 GRIDS METAL GATE CMOS

LOGIC SYMBOL

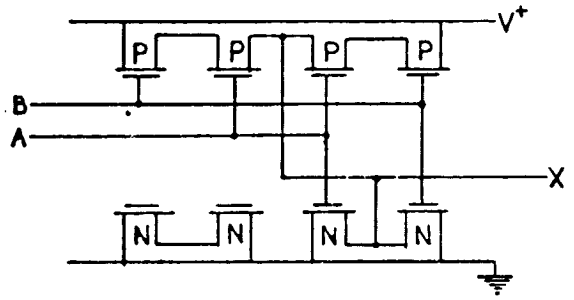


$X = \overline{A + B}$

TRUTH TABLE

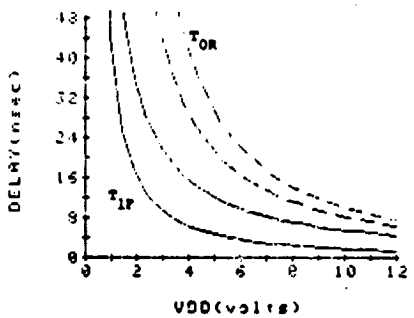
A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

SCHEMATIC

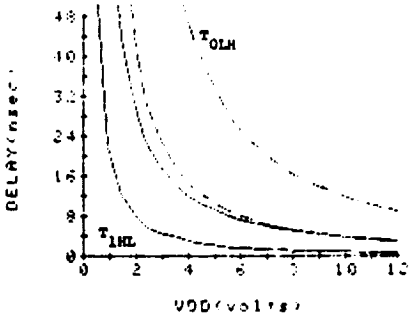


DYNAMIC DATA

RISE & FALL



PROP. DELAY



RELATIVE TO OUTPUT VOLTAGE

TRANSITION TIME
--- RISE
___ FALL

$T_R = T_{OR} + T_{IR}(F/O)$

$T_F = T_{OF} + T_{IF}(F/O)$

CAPACITANCE

PIN No.	ABSOLUTE (PF)	NORMALIZED
2	0.56	1.00
3	0.56	1.00

PROPAGATION DELAY
---- LOW TO HIGH
____ HIGH TO LOW

$T_{LH} = T_{OLH} + T_{ILH}(F/O)$

$T_{HL} = T_{OHL} + T_{IHL}(F/O)$

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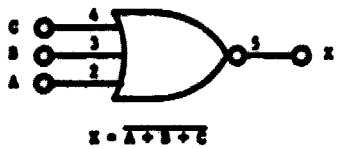
3-INPUT NOR GATE

STAR STANDARD CELL NO. 1130

8 DEVICES
4 PINS CELL WIDTH = 4 GRIDS METAL GATE CMOS

LOGIC SYMBOL

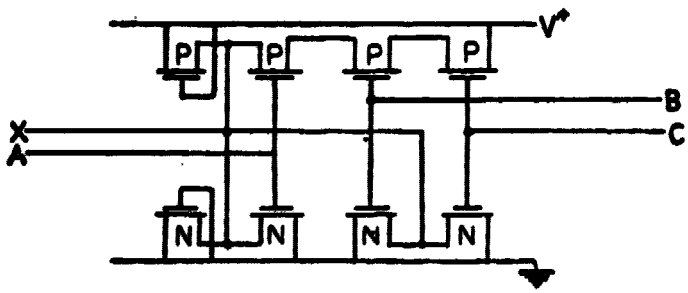


$X = \overline{A+B+C}$

TRUTH TABLE

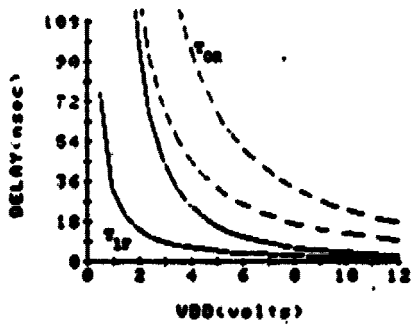
A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

SCHEMATIC

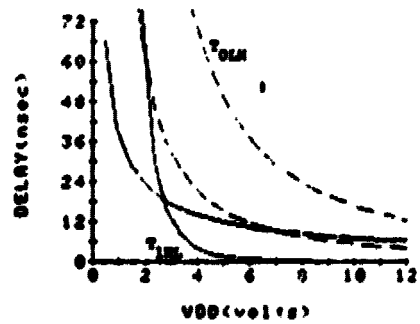


DYNAMIC DATA

RISE & FALL



PROP. DELAY



RELATIVE TO OUTPUT VOLTAGE

TRANSITION TIME

--- RISE
___ FALL

$T_R = T_{0R} + T_{1R}(F/O)$

$T_F = T_{0F} + T_{1F}(F/O)$

CAPACITANCE

PIN NO.	ABSOLUTE (PF)	NORMALIZED
2	0.86	1.00
3	0.86	1.00
4	0.86	1.00

PROPAGATION DELAY

---- LOW TO HIGH
___ HIGH TO LOW

$T_{LH} = T_{0LH} + T_{1LH}(F/O)$

$T_{HL} = T_{0HL} + T_{1HL}(F/O)$

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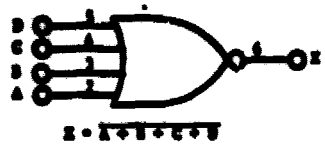
- 4-INPUT NOR-GATE

STAR STANDARD
CELL NO. 1140

30 DEVICES
5 PINS CELL WIDTH = 5 GRIDS METAL GATE CMOS

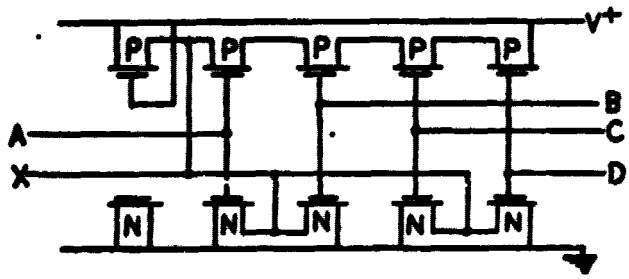
LOGIC SYMBOL



TRUTH TABLE

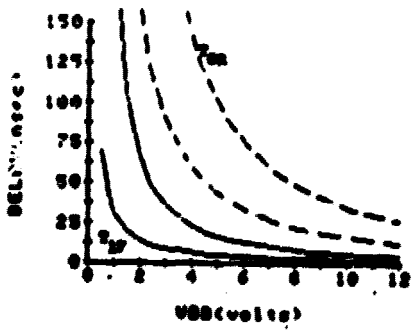
A	B	C	D	X
0	0	0	0	1
All other input combinations				0

SCHEMATIC

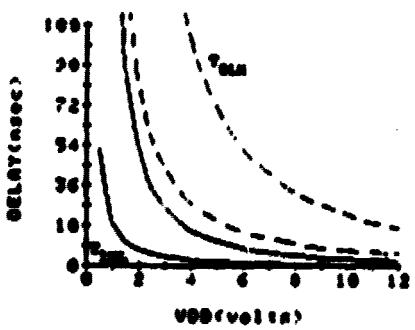


DYNAMIC DATA

RISE & FALL



PROP. DELAY



RELATIVE TO OUTPUT VOLTAGE

TRANSITION TIME

--- RISE
___ FALL

$T_R = T_{0R} + T_{1R}(F/O)$

$T_F = T_{0F} + T_{1F}(F/O)$

CAPACITANCE

Pin No.	Absolute (pF)	Normalized
2	0.00	1.00
3	0.00	1.00
4	0.00	1.00
6	0.00	1.00

PROPAGATION DELAY

----- LOW TO HIGH
_____ HIGH TO LOW

$T_{LH} = T_{0LH} + T_{1LH}(F/O)$

$T_{HL} = T_{0HL} + T_{1HL}(F/O)$

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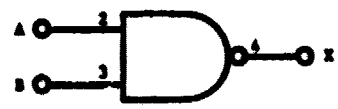
STAR STANDARD CELL NO. 1220

2-INPUT NAND GATE

6 DEVICES
3 PINS CELL WIDTH = 3 GRIDS METAL GATE CMOS

LOGIC SYMBOL

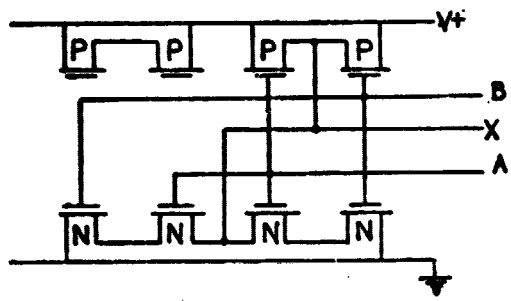


$X = \overline{A \cdot B}$

TRUTH TABLE

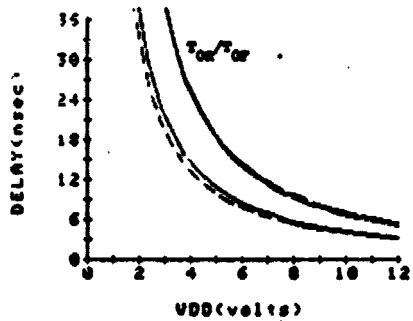
A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

SCHEMATIC

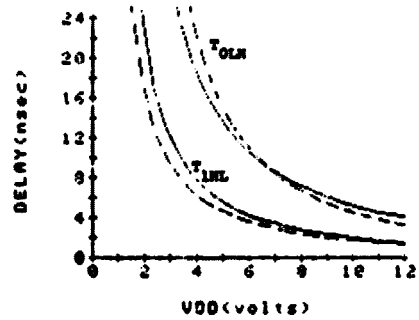


DYNAMIC DATA

RISE & FALL



PROP. DELAY



RELATIVE TO OUTPUT VOLTAGE

TRANSITION TIME

--- RISE
___ FALL

$T_R = T_{OR} + T_{1R}(F/O)$

$T_F = T_{OF} + T_{1F}(F/O)$

CAPACITANCE

PIN NO.	ABSOLUTE (PF)	NORMALIZED
2	0.86	1.00
3	0.86	1.00

PROPAGATION DELAY

---- LOW TO HIGH
___ HIGH TO LOW

$T_{LH} = T_{OLH} + T_{1LH}(F/O)$

$T_{HL} = T_{OHL} + T_{1HL}(F/O)$

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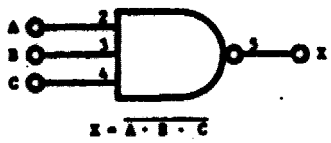
3-INPUT NAND GATE

STAR STANDARD CELL NO. 1230

8 DEVICES
4 PINS CELL WIDTH = 4 GRIDS METAL GATE CMOS

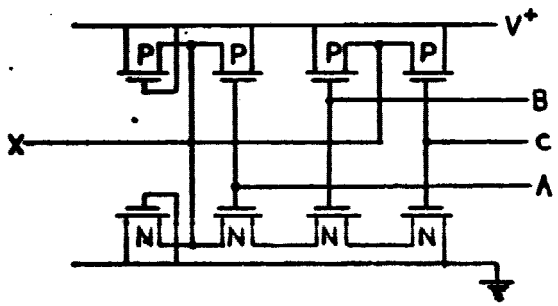
LOGIC SYMBOL



TRUTH TABLE

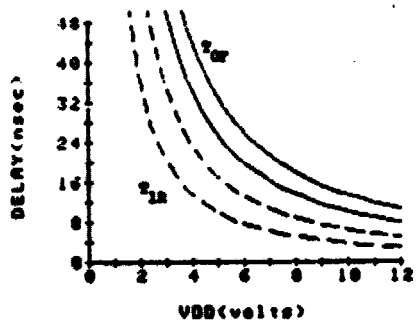
A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

SCHEMATIC

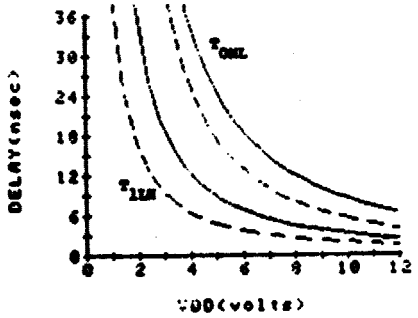


DYNAMIC DATA

RISE & FALL



PROP. DELAY



RELATIVE TO OUTPUT VOLTAGE

TRANSITION TIME

--- RISE
___ FALL

$T_R = T_{0R} + T_{1R}(F/O)$

$T_F = T_{0F} + T_{1F}(F/O)$

CAPACITANCE

PIN NO.	ABSOLUTE (PF)	NORMALIZED
2	0.86	1.00
3	0.86	1.00
4	0.86	1.00

PROPAGATION DELAY

---- LOW TO HIGH
___ HIGH TO LOW

$T_{LH} = T_{0LH} + T_{1LH}(F/O)$

$T_{HL} = T_{0HL} + T_{1HL}(F/O)$

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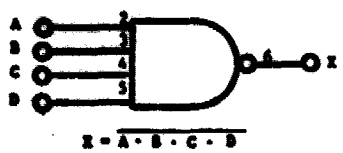
4-INPUT NAND GATE

STAR STANDARD
CELL NO. 1240

10 DEVICES
5 PINS CELL WIDTH = 5 GRIDS METAL GATE CMOS

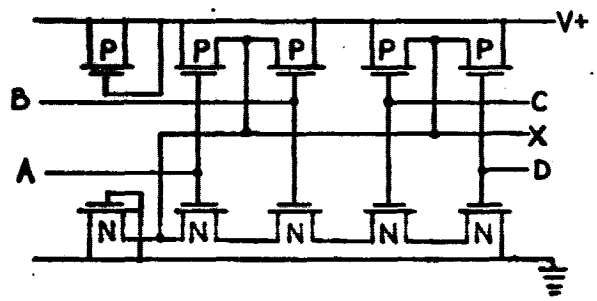
LOGIC SYMBOL



TRUTH TABLE

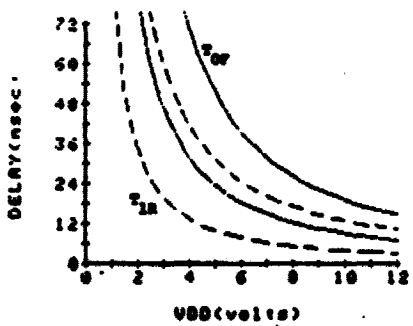
A	B	C	D	X
1	1	1	1	0
All other input combinations				1

SCHEMATIC

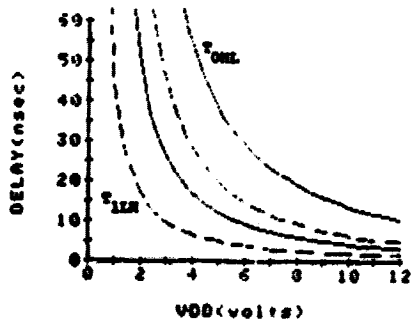


DYNAMIC DATA

RISE & FALL



PROP. DELAY



RELATIVE TO OUTPUT VOLTAGE

TRANSITION TIME

--- RISE
___ FALL

$T_R = T_{0R} + T_{1R}(F/O)$

$T_F = T_{0F} + T_{1F}(F/O)$

CAPACITANCE

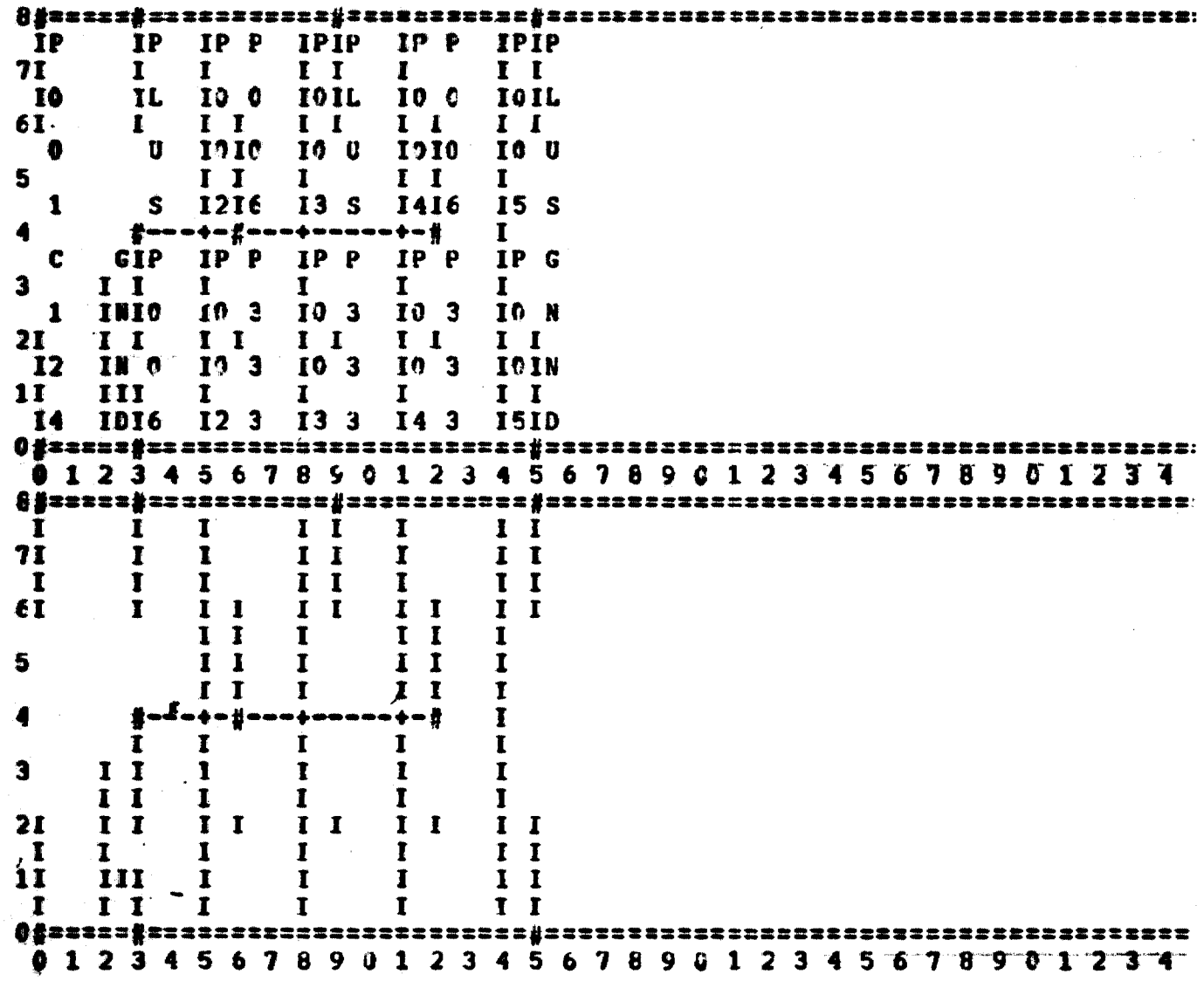
PIN NO.	ABSOLUTE (PF)	NORMALIZED
2	0.96	1.00
3	0.96	1.00
4	0.96	1.00
5	0.96	1.00

PROPAGATION DELAY

----- LOW TO HIGH
___ HIGH TO LOW

$T_{LH} = T_{0LH} + T_{1LH}(F/O)$

$T_{HL} = T_{0HL} + T_{1HL}(F/O)$



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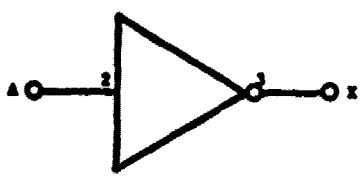
STAR STANDARD CELL NO. 1300

INVERTING BUFFER

4 DEVICES
2 PINS CELL WIDTH = 2 GRIDS METAL GATE CMOS

LOGIC SYMBOL

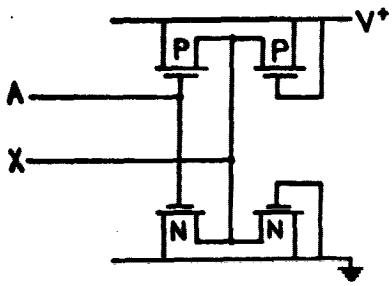


X = $\bar{A}$

TRUTH TABLE

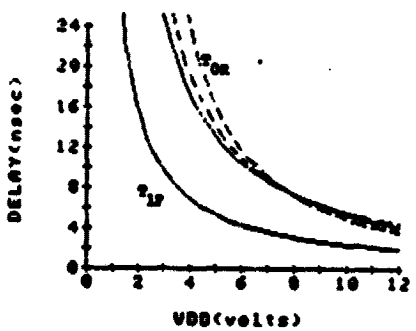
A	X
0	1
1	0

SCHEMATIC

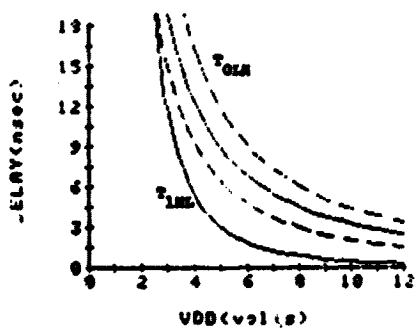


DYNAMIC DATA

RISE & FALL



PROP. DELAY



RELATIVE TO OUTPUT VOLTAGE

TRANSITION TIME

--- RISE
___ FALL

$T_R = T_{0R} + T_{1R}(F/O)$

$T_F = T_{0F} + T_{1F}(F/O)$

CAPACITANCE

PIN NO.	ABSOLUTE (PF)	NORMALIZED
2	0.56	1.00

PROPAGATION DELAY

----- LOW TO HIGH
___ HIGH TO LOW

$T_{LH} = T_{0LH} + T_{1LH}(F/O)$

$T_{HL} = T_{0HL} + T_{1HL}(F/O)$

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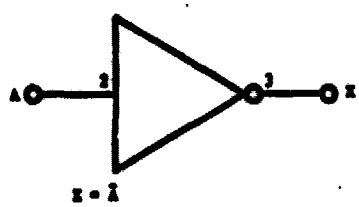
SINGLE BUFFER INVERTER

STAR STANDARD
CELL NO. 1310

4 DEVICES
2 PINS CELL WIDTH = 2 GRIDS METAL GATE CMOS

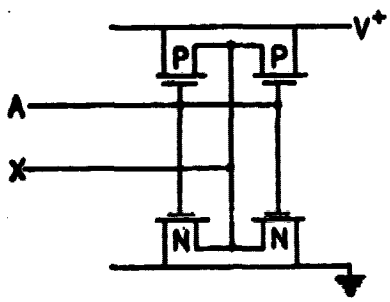
LOGIC SYMBOL



TRUTH TABLE

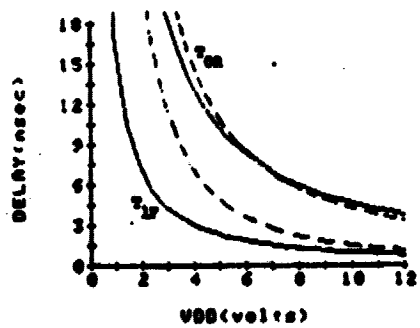
A	X
0	1
1	0

SCHEMATIC

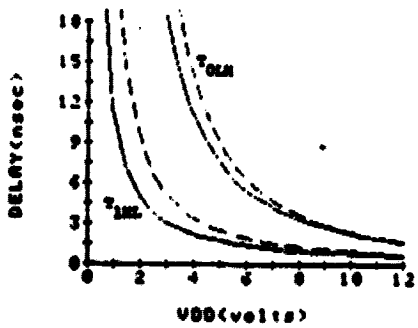


DYNAMIC DATA

RISE & FALL



PROP. DELAY



RELATIVE TO OUTPUT VOLTAGE

TRANSITION TIME
— RISE
— FALL

$T_R = T_{0R} + T_{1R}(F/O)$

$T_F = T_{0F} + T_{1F}(F/O)$

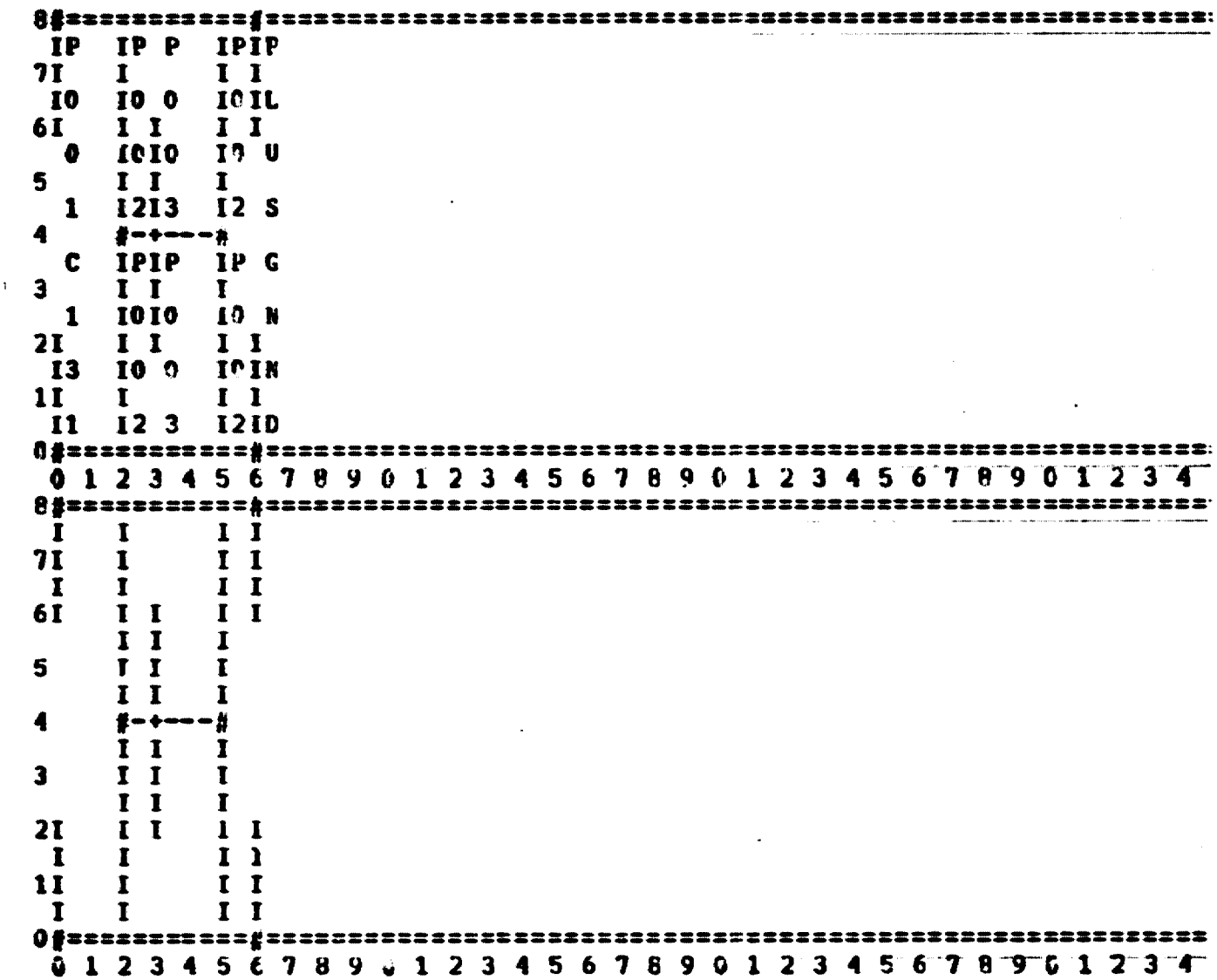
CAPACITANCE

PIN NO.	ABSOLUTE (PF)	NORMALIZED
2	1.12	2.00

PROPAGATION DELAY
---- LOW TO HIGH
____ HIGH TO LOW

$T_{LH} = T_{0LH} + T_{1LH}(F/O)$

$T_{HL} = T_{0HL} + T_{1HL}(F/O)$



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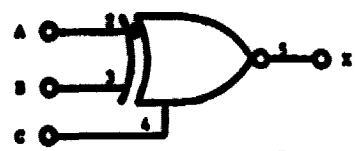
STAR STANDARD CELL NO. 1330

2-INPUT TRANSMISSION GATE

10 DEVICES
3 PINS CELL WIDTH = 5 GRIDS METAL GATE CMOS

LOGIC SYMBOL

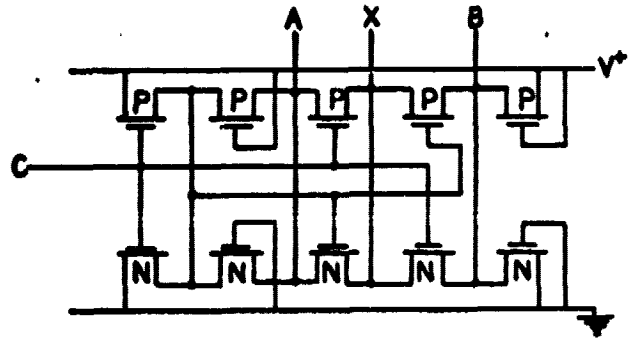


X = AC + BC

TRUTH TABLE

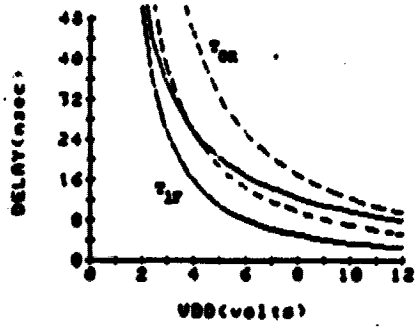
A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

SCHEMATIC

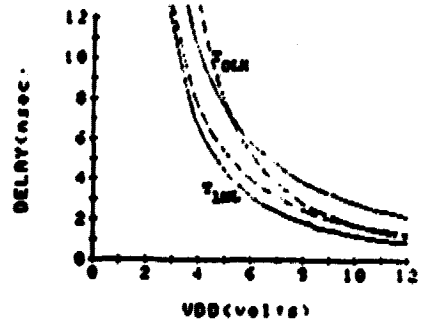


DYNAMIC DATA

RISE & FALL



PROP. DELAY



RELATIVE TO OUTPUT VOLTAGE

TRANSITION TIME

--- RISE
___ FALL

$T_R = T_{0R} + T_{1R}(F/O)$

$T_F = T_{0F} + T_{1F}(F/O)$

CAPACITANCE

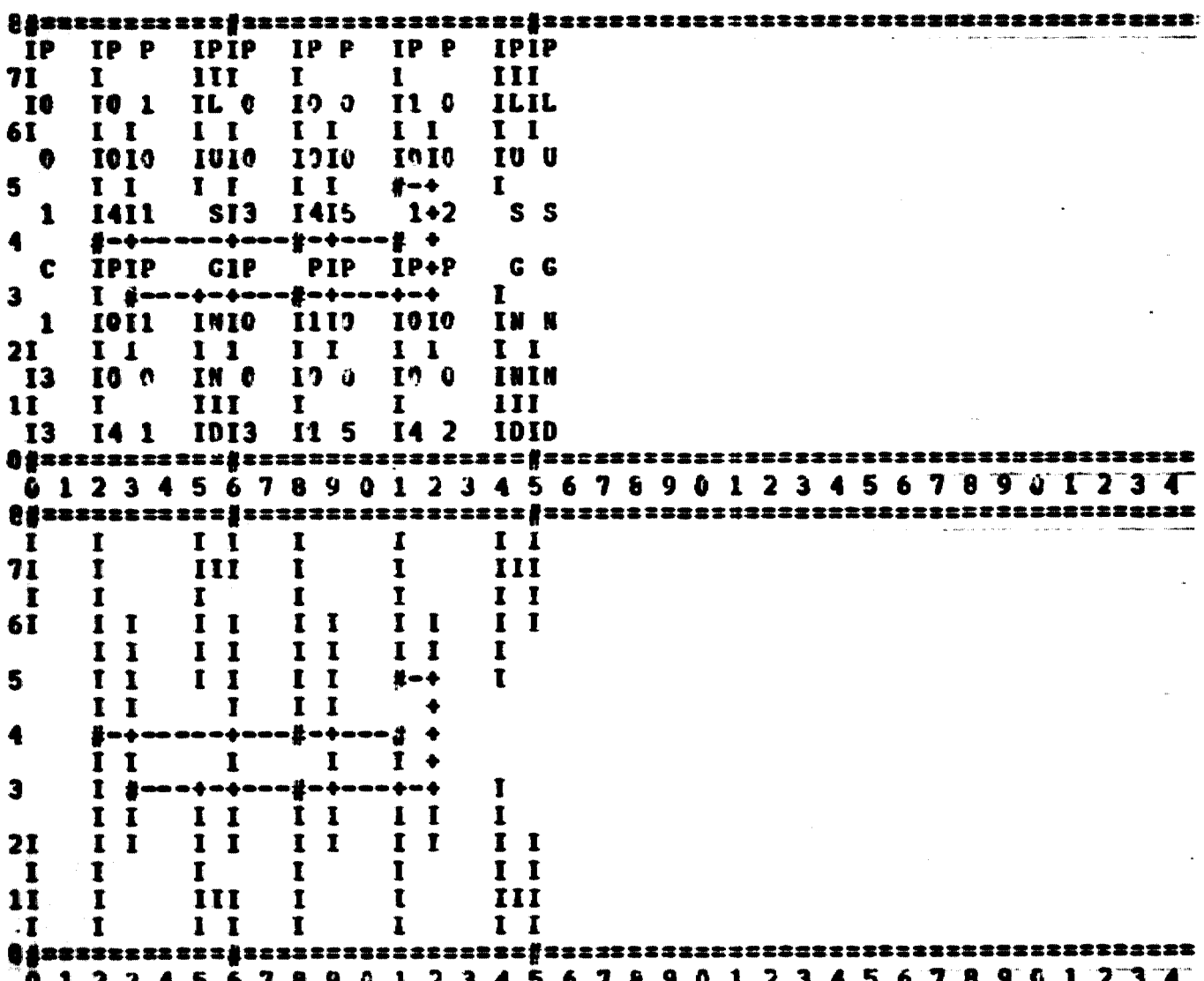
PIN NO.	ABSOLUTE (PF)	NORMALIZED
2	1.86 + F/O	3.32 + F/O
3	1.86 + F/O	3.32 + F/O
4	0.84	1.80

PROPAGATION DELAY

---- LOW TO HIGH
____ HIGH TO LOW

$T_{LH} = T_{0LH} + T_{1LH}(F/O)$

$T_{HL} = T_{0HL} + T_{1HL}(F/O)$



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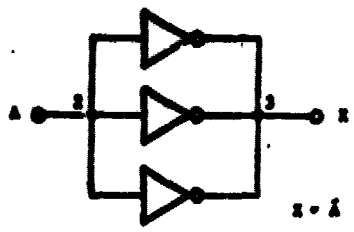
TRIPLE BUFFER INVERTER

STAR STANDARD CELL NO. 1360

22 DEVICES
2 PINS CELL WIDTH = 6 GRIDS METAL GATE CMOS

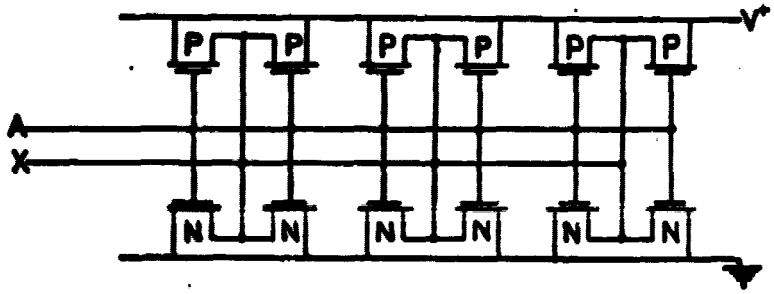
LOGIC SYMBOL



TRUTH TABLE

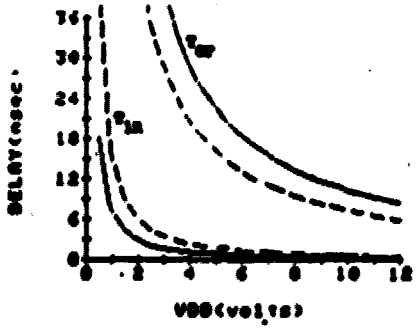
A	X
0	1
1	0

SCHEMATIC

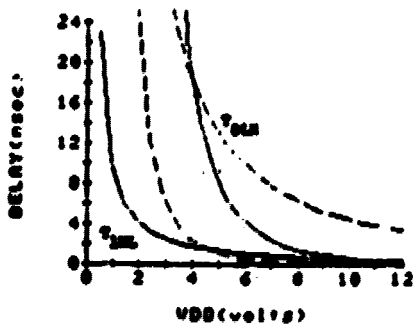


DYNAMIC DATA

RISE & FALL



PROP. DELAY



RELATIVE TO OUTPUT VOLTAGE

TRANSITION TIME

--- RISE
___ FALL

$T_R = T_{0R} + T_{1R}(F/O)$

$T_F = T_{0F} + T_{1F}(F/O)$

CAPACITANCE

PIN NO.	ABSOLUTE (PF)	NORMALIZED
2	3.36	6.00

PROPAGATION DELAY

---- LOW TO HIGH
___ HIGH TO LOW

$T_{LH} = T_{0LH} + T_{1LH}(F/O)$

$T_{HL} = T_{0HL} + T_{1HL}(F/O)$

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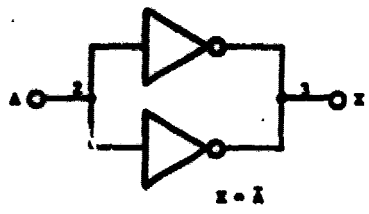
DOUBLE BUFFER INVERTER

STAR STANDARD CELL NO. 1520

8 DEVICES
2 PINS CELL WIDTH = 4 GRIDS METAL GATE CMOS

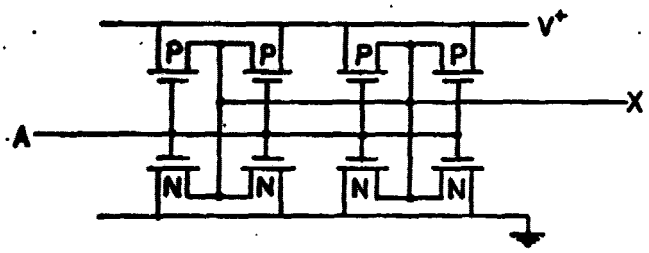
LOGIC SYMBOL



TRUTH TABLE

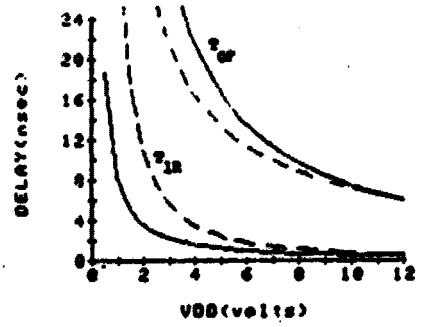
A	X
0	1
1	0

SCHEMATIC

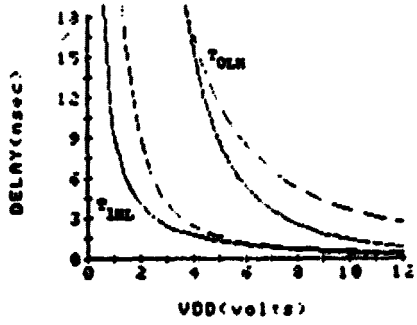


DYNAMIC DATA

RISE & FALL



PROP. DELAY



RELATIVE TO OUTPUT VOLTAGE

TRANSITION TIME

--- RISE
___ FALL

$T_R = T_{0R} + T_{1R}(F/O)$

$T_F = T_{0F} + T_{1F}(F/O)$

CAPACITANCE

PIN NO.	ABSOLUTE (PF)	NORMALIZED
2	2.24	4.00

PROPAGATION DELAY

----- LOW TO HIGH
___ HIGH TO LOW

$T_{LH} = T_{0LH} + T_{1LH}(F/O)$

$T_{HL} = T_{0HL} + T_{1HL}(F/O)$

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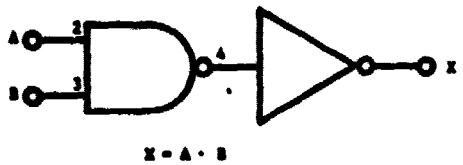
2-INPUT AND GATE

STAR STANDARD
CELL NO. 1620

8 DEVICES
3 PINS CELL WIDTH = 4 GRIDS

METAL GATE CMOS

LOGIC SYMBOL

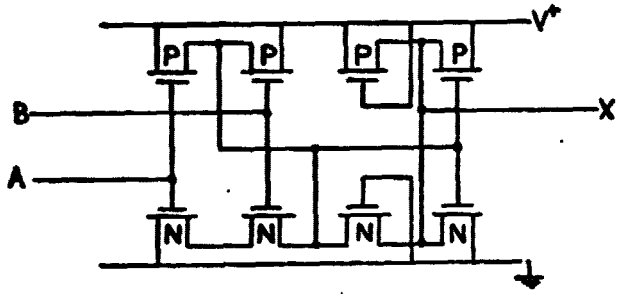


X = A · B

TRUTH TABLE

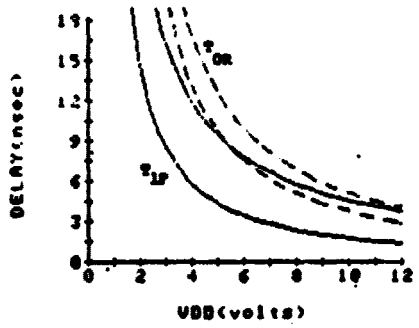
A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

SCHEMATIC

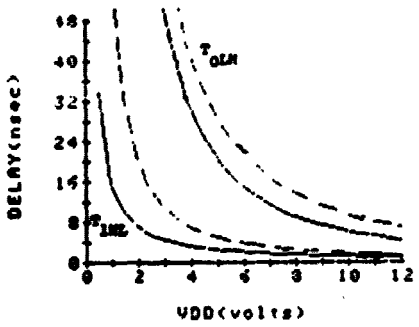


DYNAMIC DATA

RISE & FALL



PROP. DELAY



RELATIVE TO OUTPUT VOLTAGE

TRANSITION TIME

--- RISE
___ FALL

$T_R = T_{0R} + T_{1R}(F/O)$

$T_F = T_{0F} + T_{1F}(F/O)$

CAPACITANCE

PIN NO.	ABSOLUTE (PF)	NORMALIZED
2	0.56	1.00
3	0.56	1.00

PROPAGATION DELAY

---- LOW TO HIGH
___ HIGH TO LOW

$T_{LH} = T_{0LH} + T_{1LH}(F/O)$

$T_{HL} = T_{0HL} + T_{1HL}(F/O)$

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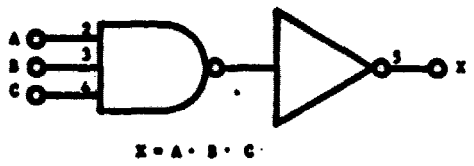
3-INPUT AND GATE

STAR STANDARD CELL NO. 1630

10 DEVICES
4 PINS CELL WIDTH = 5 GRIDS METAL GATE CMOS

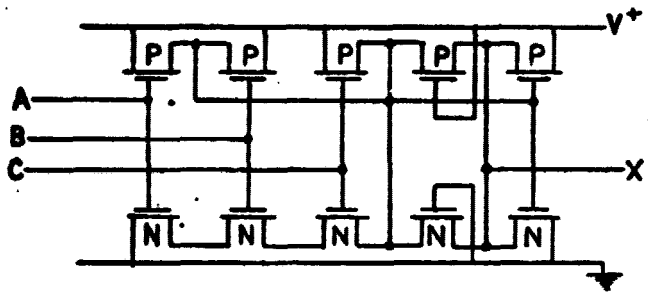
LOGIC SYMBOL



TRUTH TABLE

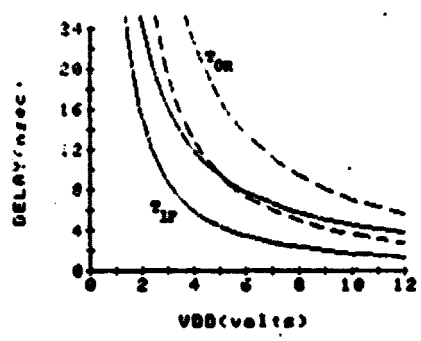
A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

SCHEMATIC

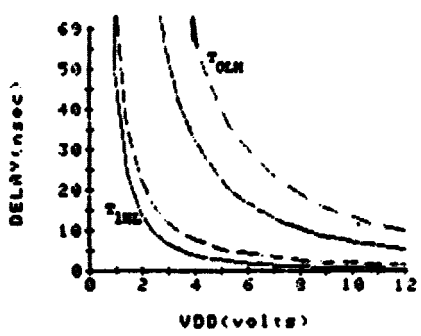


DYNAMIC DATA

RISE & FALL



PROP. DELAY



RELATIVE TO OUTPUT VOLTAGE

TRANSITION TIME

--- RISE
___ FALL

$T_R = T_{0R} + T_{1R}(F/O)$

$T_F = T_{0F} + T_{1F}(F/O)$

CAPACITANCE

PIN No.	ABSOLUTE (PF)	NORMALIZED
2	0.56	1.00
3	0.56	1.00
4	0.56	1.00

PROPAGATION DELAY

---- LOW TO HIGH
____ HIGH TO LOW

$T_{LH} = T_{0LH} + T_{1LH}(F/O)$

$T_{HL} = T_{0HL} + T_{1HL}(F/O)$

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STAR STANDARD CELL NO. 1640

4-INPUT AND GATE

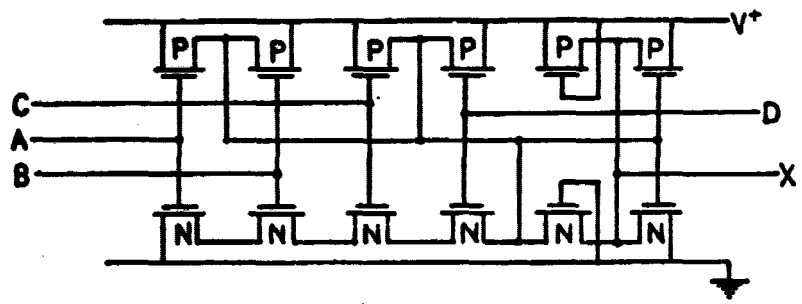
12 DEVICES
5 PINS CELL WIDTH = 6 GRIDS METAL GATE CMOS

LOGIC SYMBOL

TRUTH TABLE

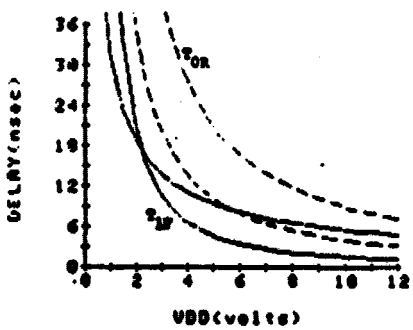
A	B	C	D	X
1	1	1	1	1
All other input combinations				0

SCHEMATIC

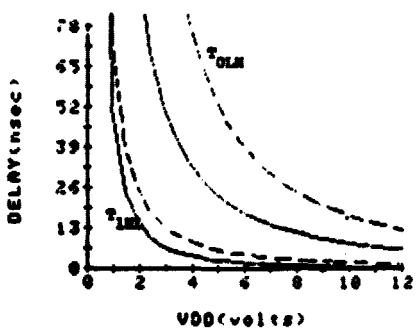


DYNAMIC DATA

RISE & FALL



PROP. DELAY



RELATIVE TO OUTPUT VOLTAGE

TRANSITION TIME

--- RISE
___ FALL

$T_R = T_{0R} + T_{1R}(F/O)$

$T_F = T_{0F} + T_{1F}(F/O)$

CAPACITANCE

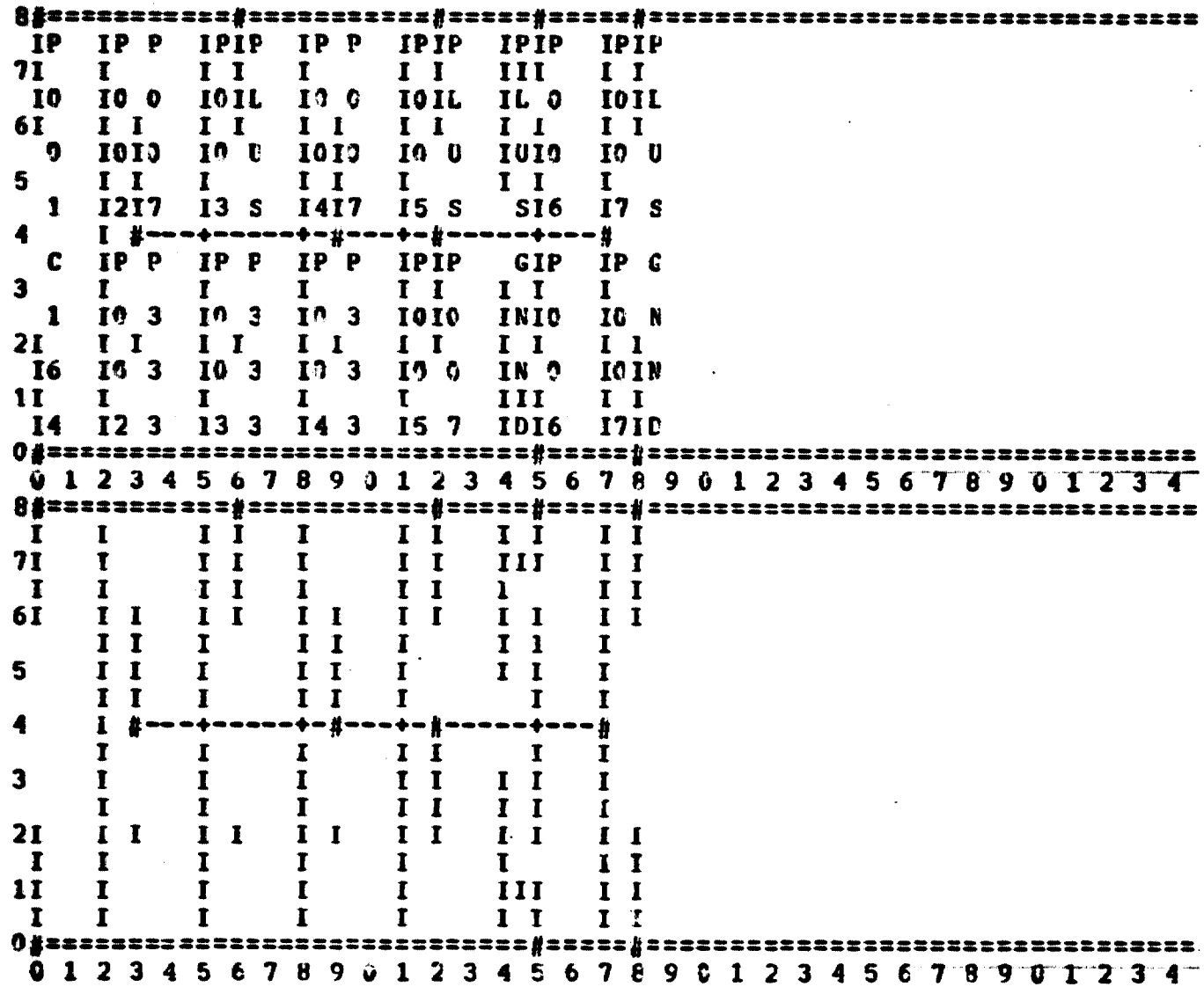
PIN NO.	ABSOLUTE (PF)	NORMALIZED
2	0.56	1.00
3	0.56	1.00
4	0.56	1.00
5	0.56	1.00

PROPAGATION DELAY

---- LOW TO HIGH
___ HIGH TO LOW

$T_{LH} = T_{0LH} + T_{1LH}(F/O)$

$T_{HL} = T_{0HL} + T_{1HL}(F/O)$



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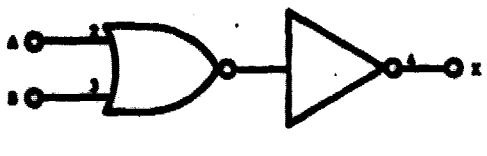
2-INPUT OR GATE

STAR STANDARD CELL NO. 1720

6 DEVICES
3 PINS CELL WIDTH = 4 GRIDS METAL GATE CMOS

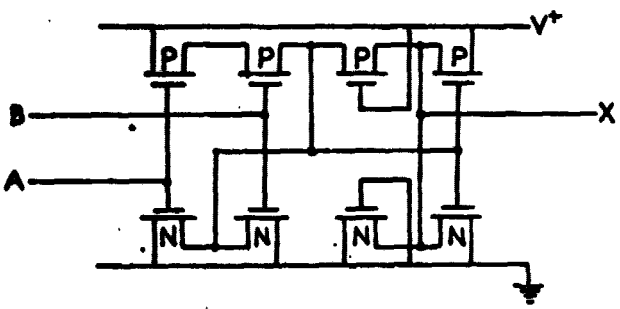
LOGIC SYMBOL



TRUTH TABLE

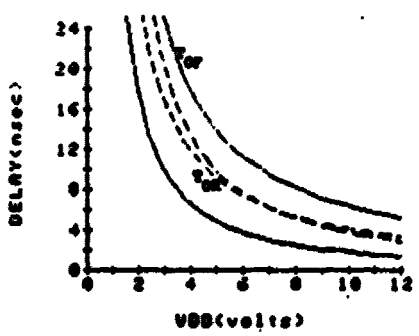
A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

SCHEMATIC

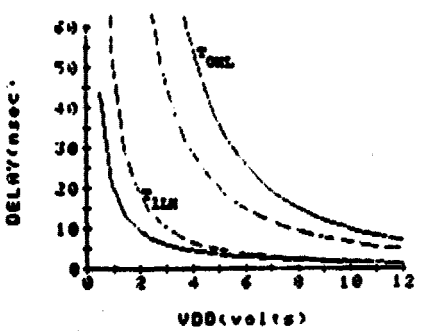


DYNAMIC DATA

RISE & FALL



PROP. DELAY



RELATIVE TO OUTPUT VOLTAGE

TRANSITION TIME

--- RISE
___ FALL

$T_R = T_{0R} + T_{1R}(F/O)$

$T_F = T_{0F} + T_{1F}(F/O)$

CAPACITANCE

PIN NO.	ABSOLUTE (PF)	NORMALIZED
2	0.56	1.00
3	0.56	1.00

PROPAGATION DELAY

---- LOW TO HIGH
____ HIGH TO LOW

$T_{LH} = T_{0LH} + T_{1LH}(F/O)$

$T_{HL} = T_{0HL} + T_{1HL}(F/O)$

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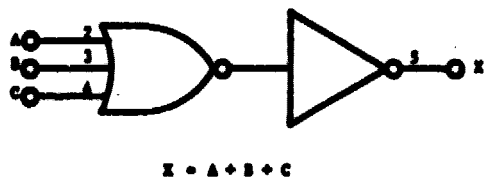
3-INPUT OR GATE

STAR STANDARD CELL NO. 1730

10 DEVICES
4 PINS CELL WIDTH = 5 GRIDS METAL GATE CMOS

LOGIC SYMBOL

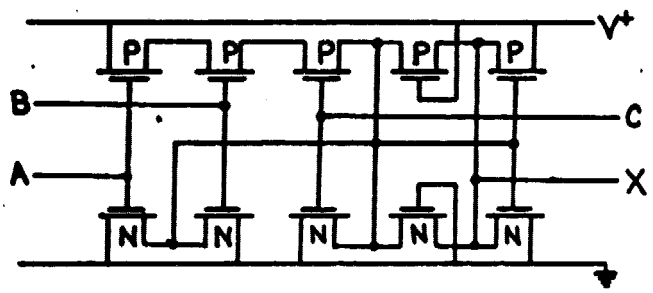


X = A + B + C

TRUTH TABLE

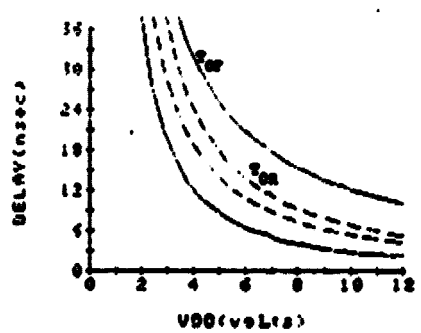
A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

SCHEMATIC

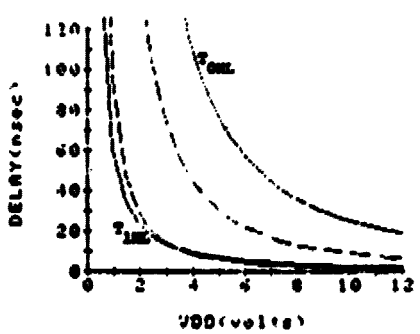


DYNAMIC DATA

RISE & FALL



PROP. DELAY



RELATIVE TO OUTPUT VOLTAGE

TRANSITION TIME

— RISE
— FALL

$T_R = T_{0R} + T_{1R}(F/O)$

$T_F = T_{0F} + T_{1F}(F/O)$

CAPACITANCE

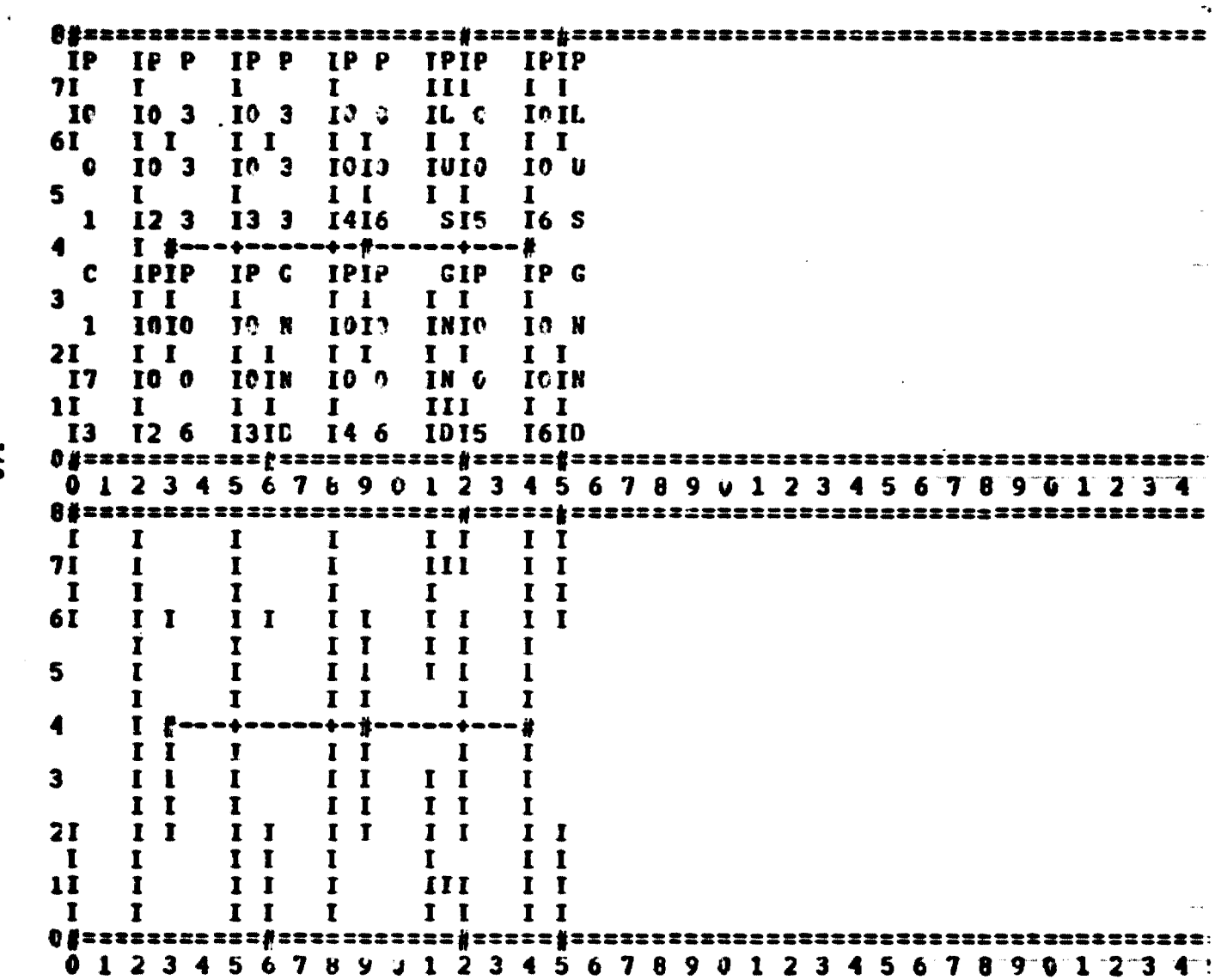
PIN NO.	ABSOLUTE (PF)	NORMALIZED
2	0.56	1.00
3	0.56	1.00
4	0.56	1.00

PROPAGATION DELAY

---- LOW TO HIGH
—— HIGH TO LOW

$T_{LH} = T_{0LH} + T_{1LH}(F/O)$

$T_{HL} = T_{0HL} + T_{1HL}(F/O)$



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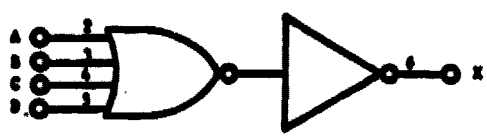
4-INPUT OR GATE

STAR STANDARD CELL NO. 1740

12 DEVICES
5 PINS CELL WIDTH = 6 GRIDS METAL GATE CMOS

LOGIC SYMBOL

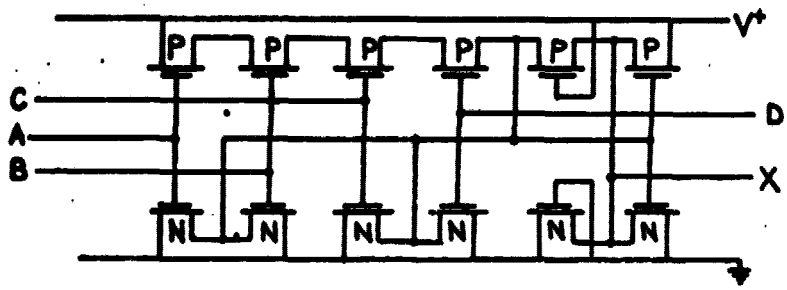


X = A+B+C+D

TRUTH TABLE

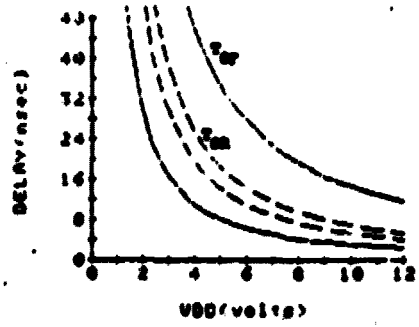
A	B	C	D	X
0	0	0	0	0
All other input combinations				1

SCHEMATIC

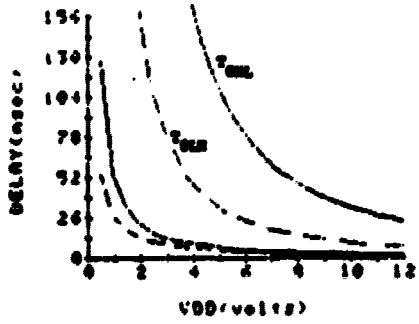


DYNAMIC DATA

RISE & FALL



PROP. DELAY



RELATIVE TO OUTPUT VOLTAGE

TRANSITION TIME

--- RISE
___ FALL

$T_R = T_{0R} + T_{1R}(F/O)$

$T_F = T_{0F} + T_{1F}(F/O)$

CAPACITANCE

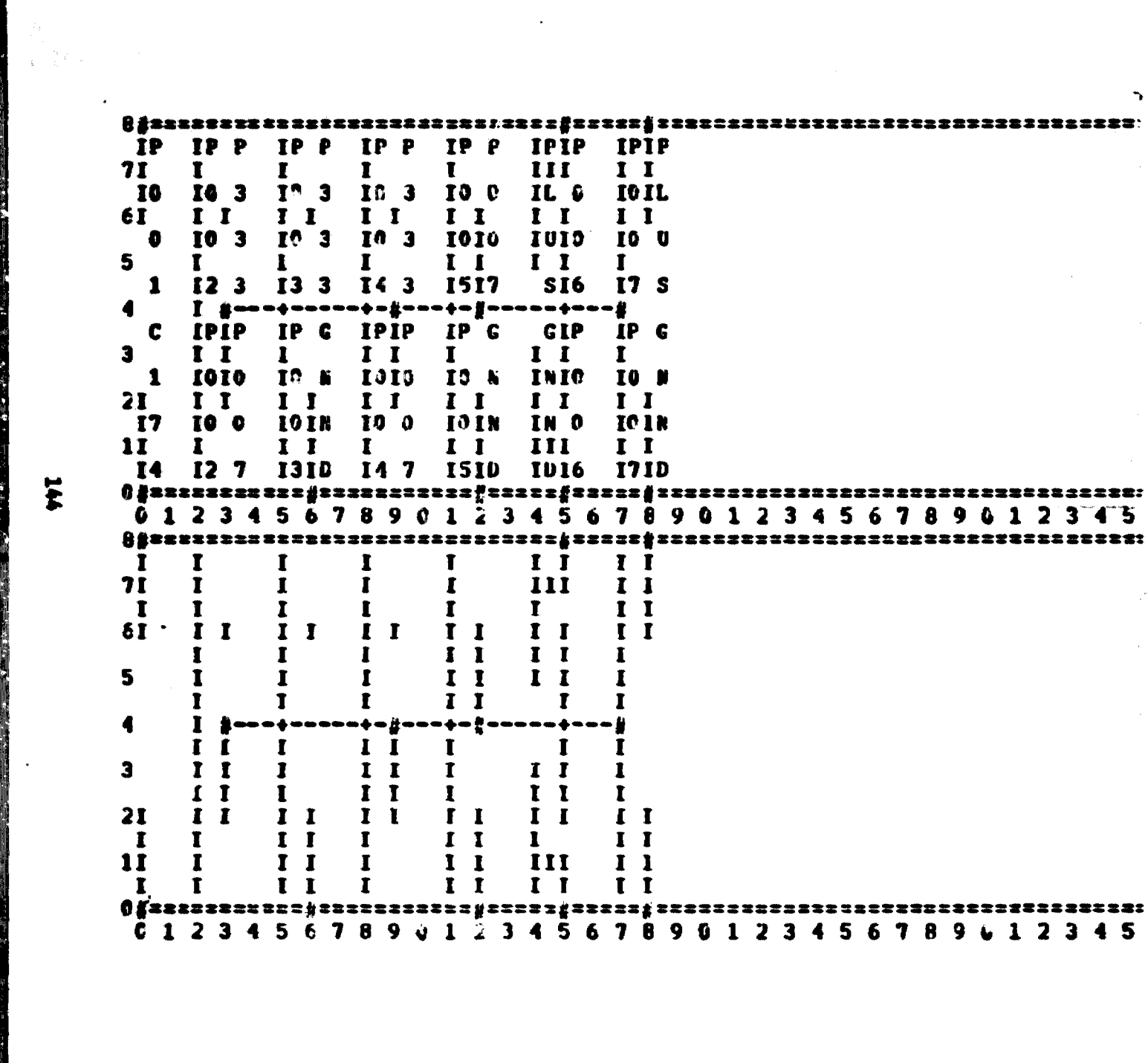
Pin No.	Absolute (pF)	Normalized
2	0.94	1.00
3	0.96	1.00
4	0.96	1.00
5	0.96	1.00

PROPAGATION DELAY

---- LOW TO HIGH
___ HIGH TO LOW

$T_{LH} = T_{0LH} + T_{1LH}(F/O)$

$T_{HL} = T_{0HL} + T_{1HL}(F/O)$



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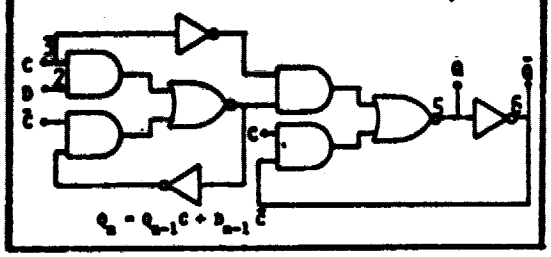
STAR STANDARD CELL NO. 1820

D-TYPE MASTER/SLAVE FLIP-FLOP

28 DEVICES
4 PINS CELL WIDTH = 14 GRIDS METAL GATE CMOS

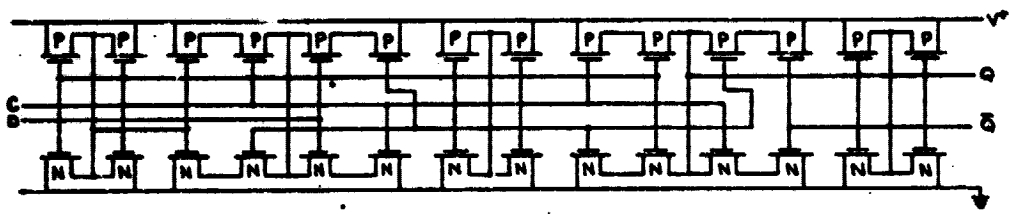
LOGIC SYMBOL



TRUTH TABLE

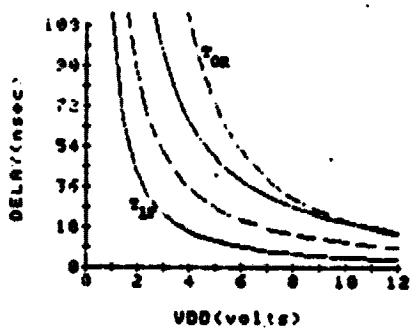
C	D	Q
↑	1	1
↑	0	0
↓	1	Q_{n-1}
↓	0	Q_{n-1}

SCHEMATIC

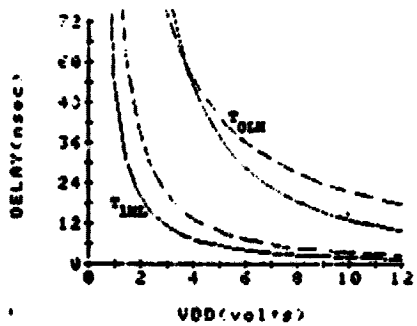


DYNAMIC DATA

RISE & FALL



PROP. DELAY



RELATIVE TO OUTPUT VOLTAGE

TRANSITION TIME

--- RISE
___ FALL

$T_R = T_{0R} + T_{1R}(F/O)$

$T_F = T_{0F} + T_{1F}(F/O)$

CAPACITANCE

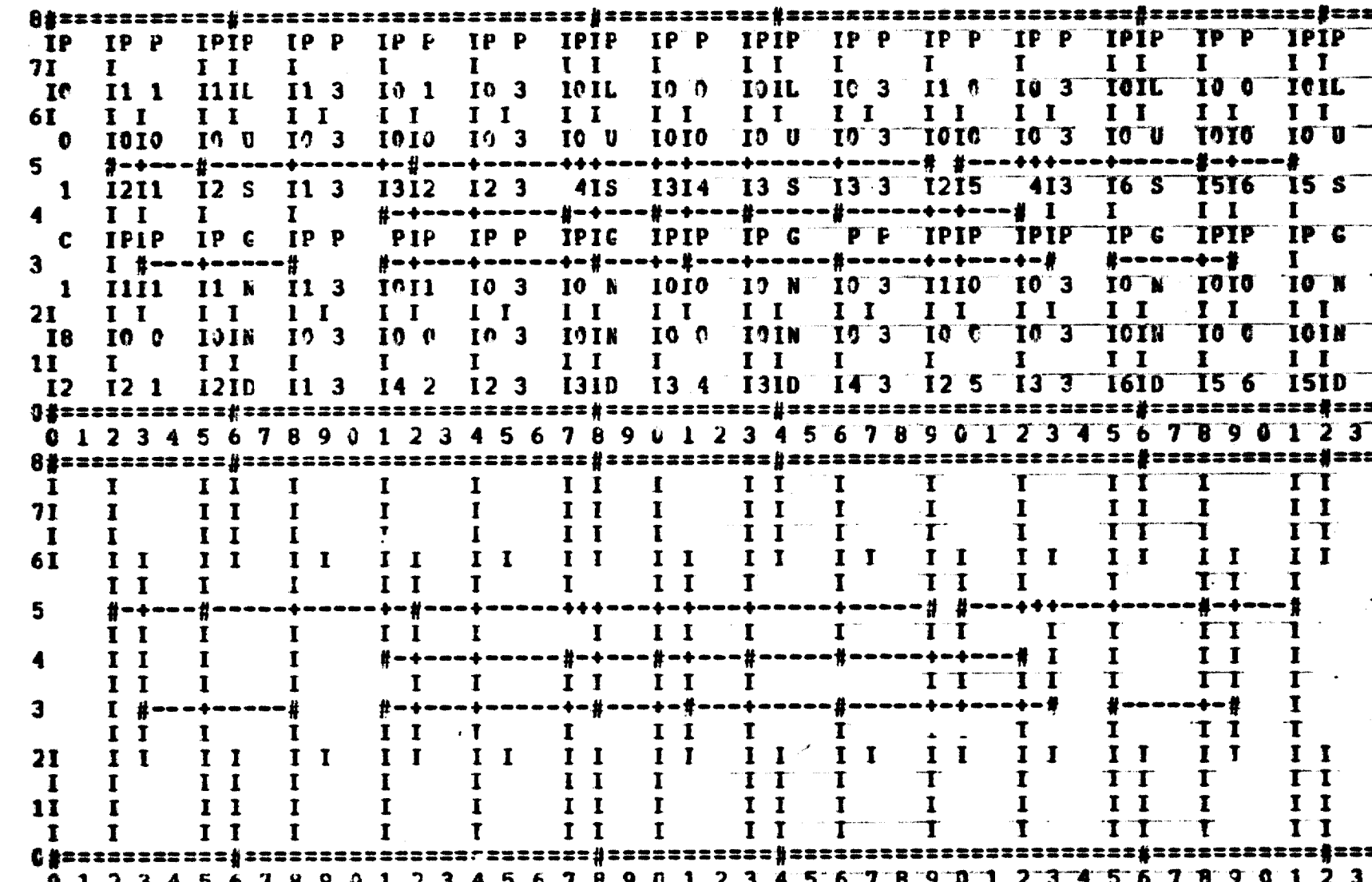
PIN NO.	ABSOLUTE (PF)	NORMALIZED
2	0.86	1.00
3	1.12	2.00

PROPAGATION DELAY

---- LOW TO HIGH
____ HIGH TO LOW

$T_{LH} = T_{0LH} + T_{1LH}(F/O)$

$T_{HL} = T_{0HL} + T_{1HL}(F/O)$



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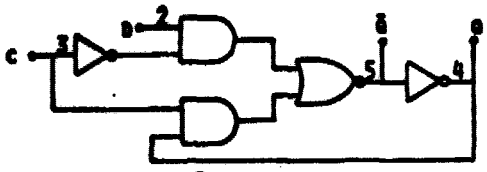
D-TYPE FLIP-FLOP

STAR STANDARD
CELL NO. 1830

16 DEVICES
4 PINS CELL WIDTH = 8 GRIDS METAL GATE CMOS

LOGIC SYMBOL

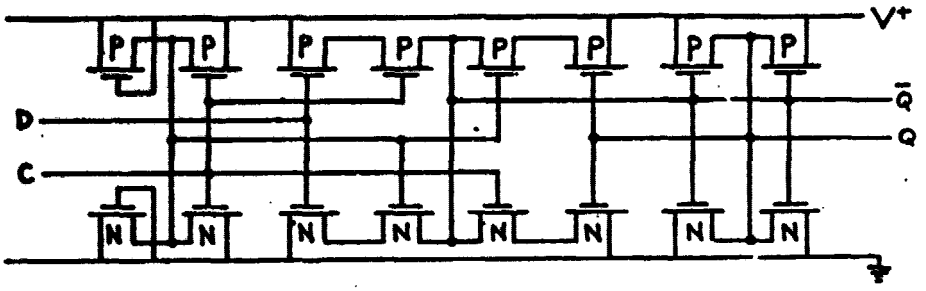


$A = D\bar{C} + Q_{n-1}C$

TRUTH TABLE

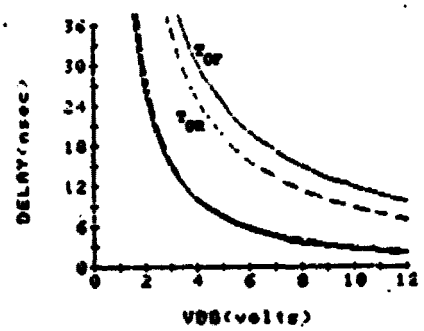
D	C	Q
0	1	Q_{n-1}
1	0	1
0	0	0

SCHEMATIC

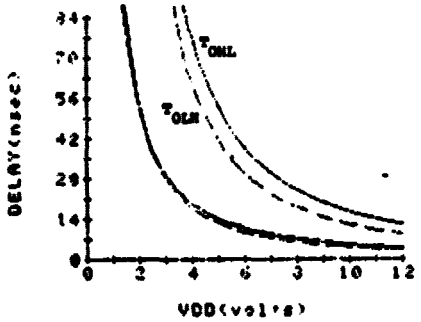


DYNAMIC DATA

RISE & FALL



PROP. DELAY



RELATIVE TO OUTPUT VOLTAGE

TRANSITION TIME

--- RISE
___ FALL

$T_R = T_{0R} + T_{1R}(F/O)$

$T_F = T_{0F} + T_{1F}(F/O)$

CAPACITANCE

PIN NO.	ABSOLUTE (PF)	NORMALIZED
2	0.56	1.00
3	1.12	2.00

PROPAGATION DELAY

----- LOW TO HIGH
_____ HIGH TO LOW

$T_{LH} = T_{0LH} + T_{1LH}(F/O)$

$T_{HL} = T_{0HL} + T_{1HL}(F/O)$

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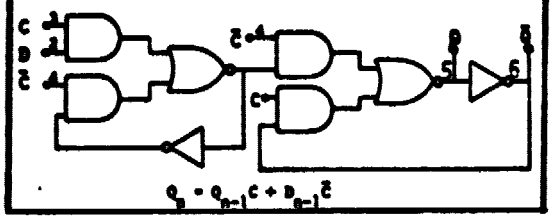
PROGRAMMABLE D-TYPE MASTER/SLAVE FLIP-FLOP

24 DEVICES
5 PINS CELL WIDTH = 12 GRIDS

STAR STANDARD CELL NO. 1900

METAL GATE CMOS

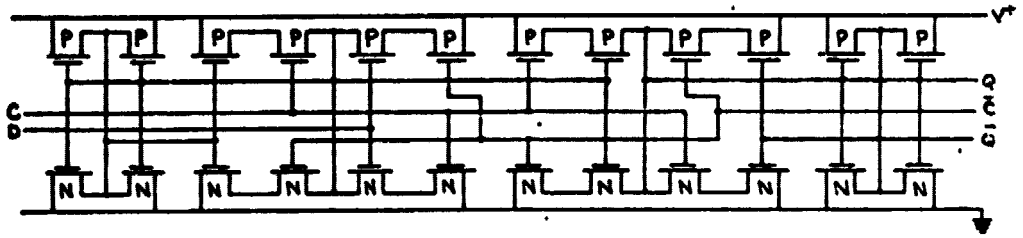
LOGIC SYMBOL



TRUTH TABLE

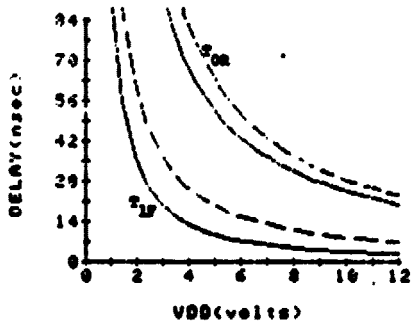
C	D	Q
↓	1	1
↓	0	0
↑	1	Q_{n-1}
↑	0	Q_{n-1}

SCHEMATIC

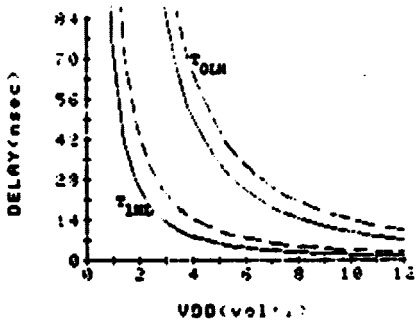


DYNAMIC DATA

RISE & FALL



PROP. DELAY



RELATIVE TO OUTPUT VOLTAGE

TRANSITION TIME

--- RISE
___ FALL

$T_R = T_{0R} + T_{1R}(F/O)$

$T_F = T_{0F} + T_{1F}(F/O)$

CAPACITANCE

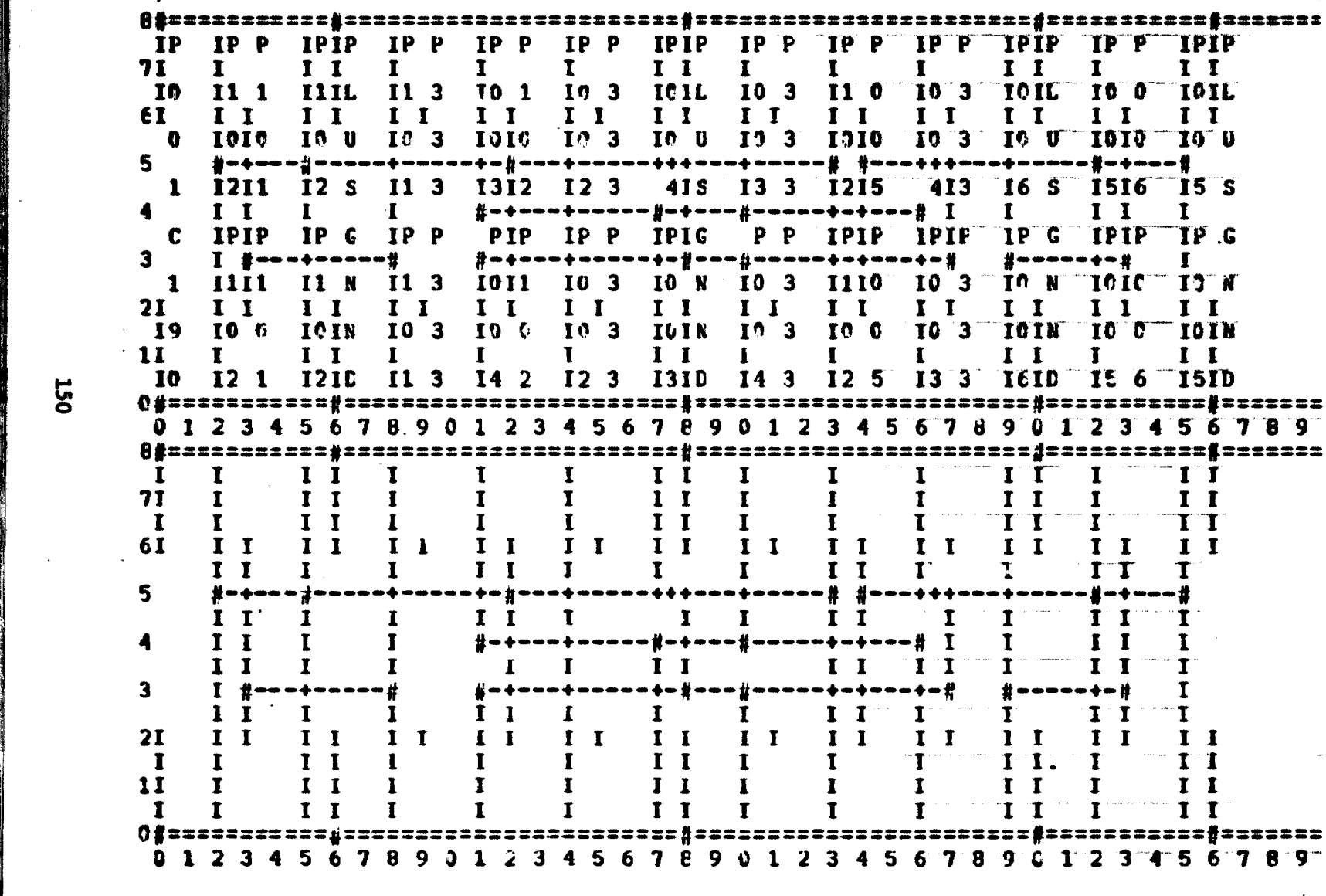
PIN NO.	ABSOLUTE (PF)	NORMALIZED
2	0.56	1.00
3	1.12	2.00
4	1.12	2.00

PROPAGATION DELAY

---- LOW TO HIGH
____ HIGH TO LOW

$T_{LH} = T_{0LH} + T_{1LH}(F/O)$

$T_{HL} = T_{0HL} + T_{1HL}(F/O)$



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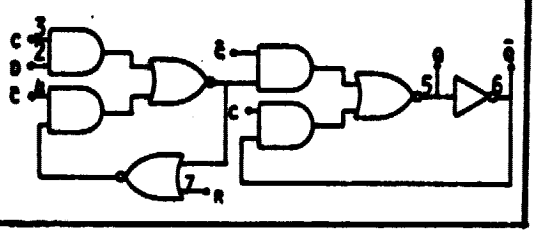
PROGRAMMABLE D-TYPE MASTER/SLAVE
FLIP-FLOP WITH RESET
26 DEVICES
6 PINS CELL WIDTH = 13 GRIDS

STAR STANDARD CELL NO. 1910

METAL GATE CMOS

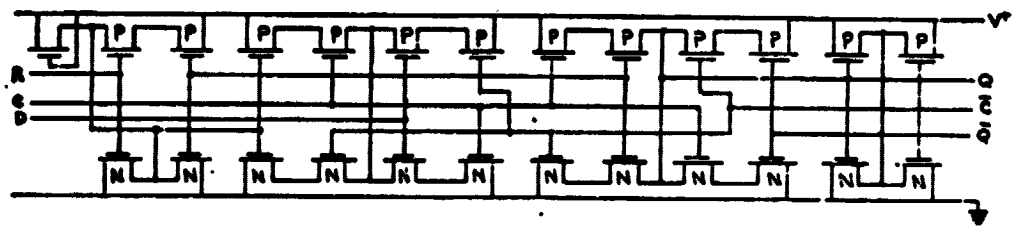
LOGIC SYMBOL



TRUTH TABLE

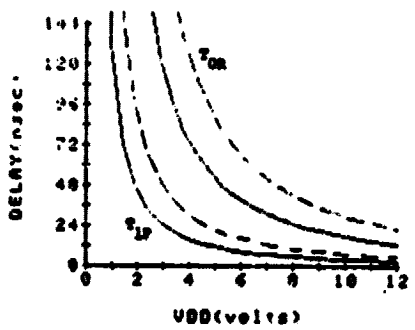
C	D	R	Q
↓	1	0	1
↓	0	0	0
↓	1	0	Q_{n-1}
↓	0	0	Q_{n-1}
1	*	*	Q_n
0	*	1	0
↓	1	1	↓

SCHEMATIC

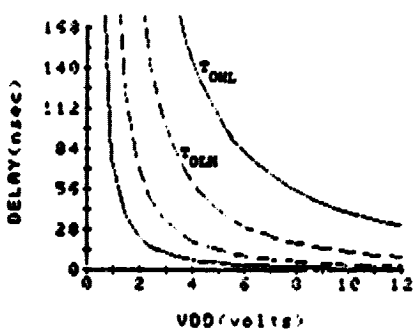


DYNAMIC DATA

RISE & FALL



PROP. DELAY



RELATIVE TO OUTPUT VOLTAGE

TRANSITION TIME

--- RISE
___ FALL

$T_R = T_{0R} + T_{1R}(F/O)$

$T_F = T_{0F} + T_{1F}(F/O)$

CAPACITANCE

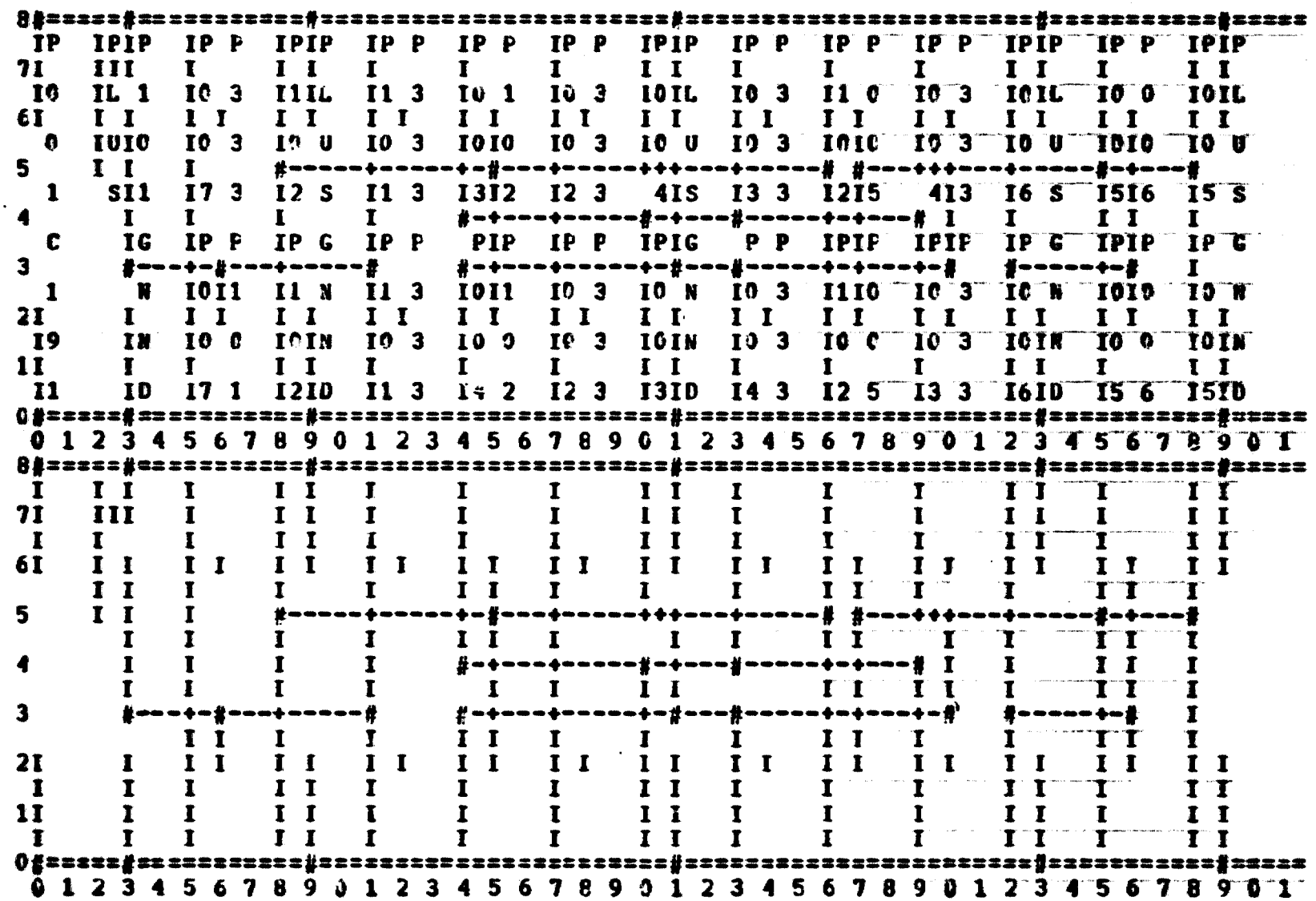
PIN No.	ABSOLUTE (PF)	NORMALIZED
2	0.86	1.00
3	1.12	2.00
4	1.12	2.00
7	0.86	1.00

PROPAGATION DELAY

---- LOW TO HIGH
___ HIGH TO LOW

$T_{LH} = T_{0LH} + T_{1LH}(F/O)$

$T_{HL} = T_{0HL} + T_{1HL}(F/O)$



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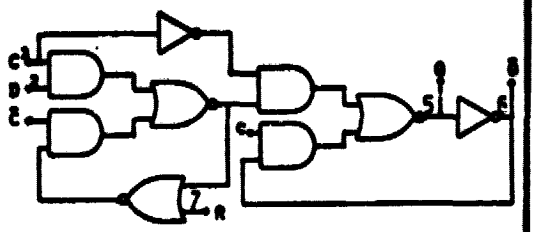
D-TYPE MASTER/SLAVE
FLIP-FLOP WITH RESET
30 DEVICES
5 PINS CELL WIDTH = 15 GRIDS

STAR STANDARD CELL NO. 1920

METAL GATE CMOS

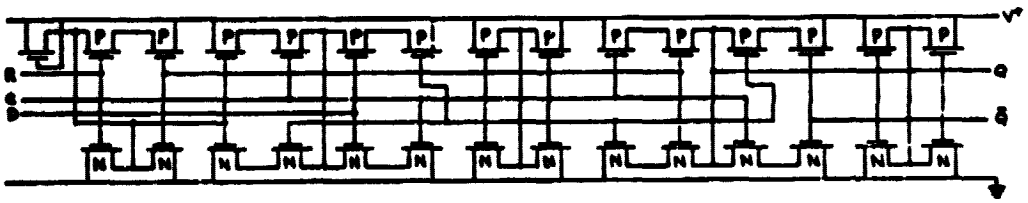
LOGIC SYMBOL



TRUTH TABLE

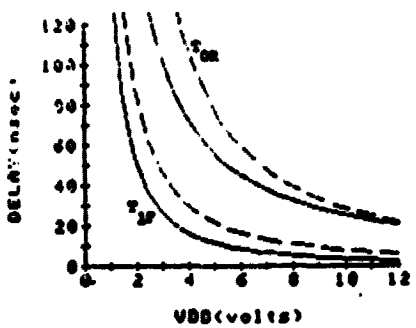
C	R	Q_n
↑	1	0	1
↑	0	0	0
↑	1	0	Q_{n-1}
↑	0	0	Q_{n-1}
1	*	*	Q_n
↓	*	*	Q_n

SCHEMATIC

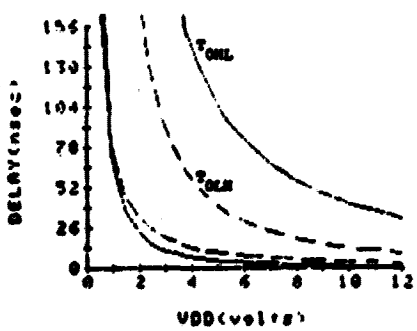


DYNAMIC DATA

RISE & FALL



PROP. DELAY



RELATIVE TO OUTPUT VOLTAGE

TRANSITION TIME

--- RISE
___ FALL

$T_R = T_{0R} + T_{1R}(F/O)$

$T_F = T_{0F} + T_{1F}(F/O)$

CAPACITANCE

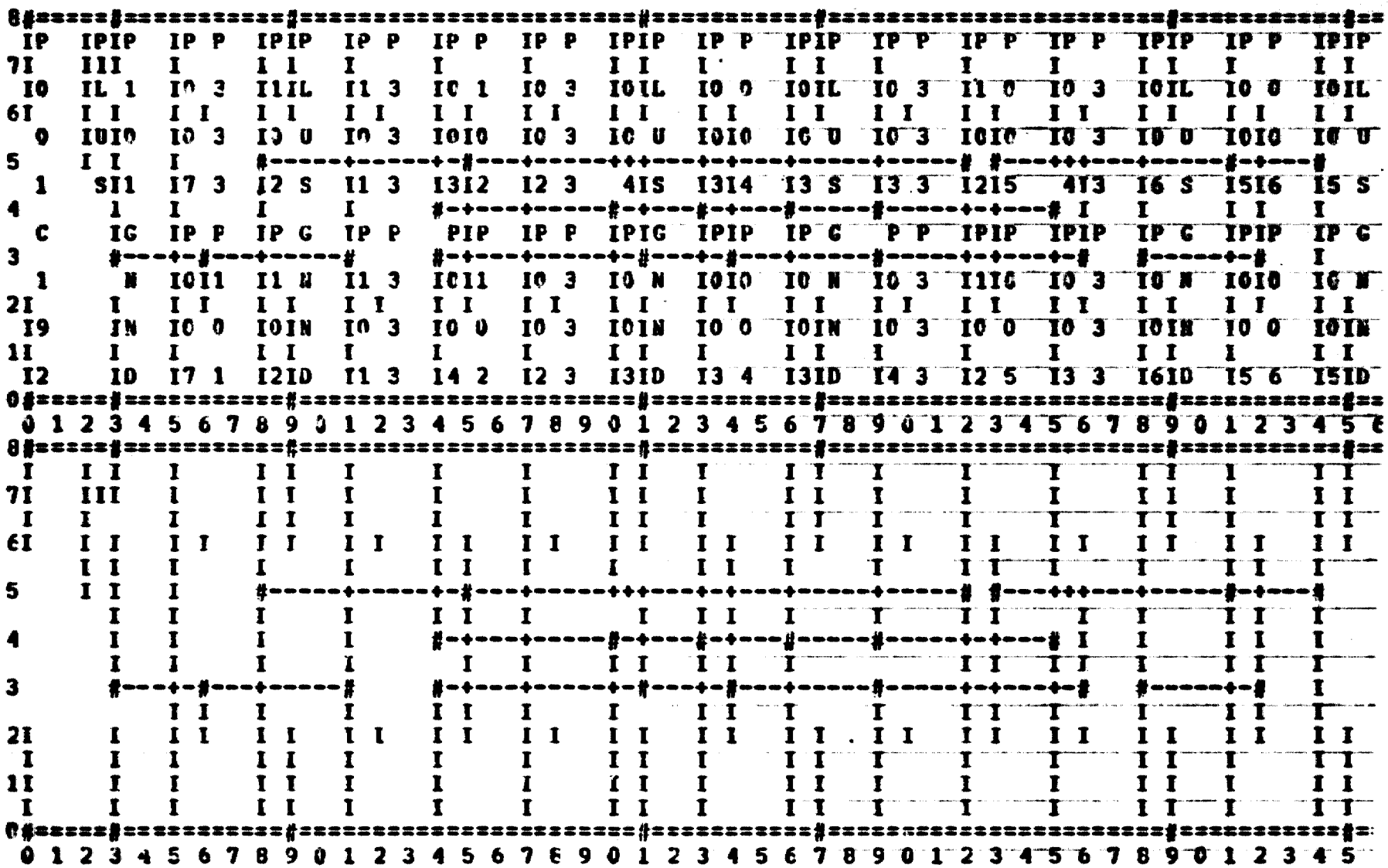
Pin No.	Absolute (pF)	Normalized
2	0.56	1.00
3	1.12	2.00
7	0.56	1.00

PROPAGATION DELAY

---- LOW TO HIGH
___ HIGH TO LOW

$T_{LH} = T_{0LH} + T_{1LH}(F/O)$

$T_{HL} = T_{0HL} + T_{1HL}(F/O)$



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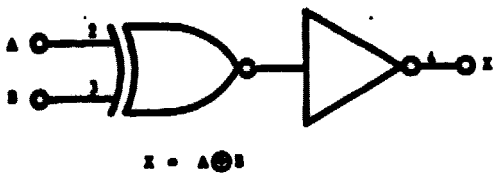
STAR STANDARD CELL NO. 2310

EXCLUSIVE-OR

10 DEVICES
3 PINS CELL WIDTH = 5 GRIDS METAL GATE CMOS

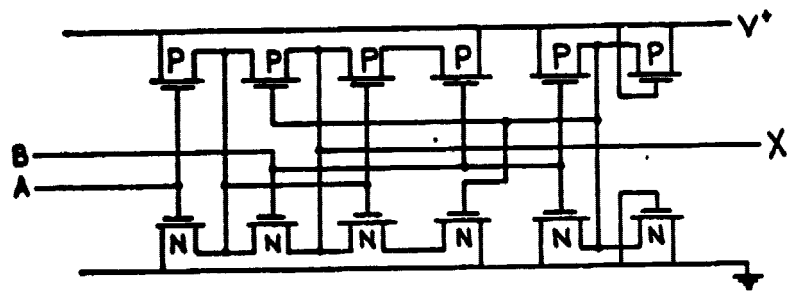
LOGIC SYMBOL



TRUTH TABLE

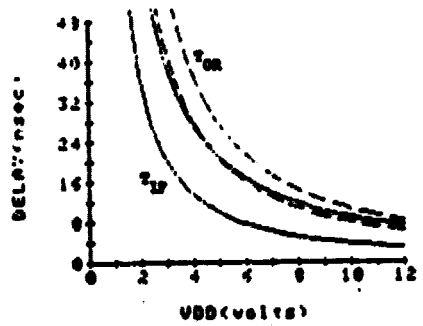
A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

SCHEMATIC

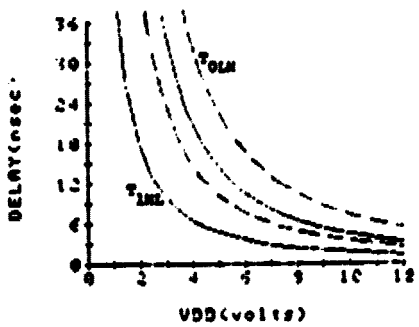


DYNAMIC DATA

RISE & FALL



PROP. DELAY



RELATIVE TO OUTPUT VOLTAGE

TRANSITION TIME

--- RISE
___ FALL

$T_R = T_{0R} + T_{1R}(F/O)$

$T_F = T_{0F} + T_{1F}(F/O)$

CAPACITANCE

PIN No.	ABSOLUTE (PF)	NORMALIZED
2	0.86	1.00
3	1.12	2.00

PROPAGATION DELAY

---- LOW TO HIGH
___ HIGH TO LOW

$T_{LH} = T_{0LH} + T_{1LH}(F/O)$

$T_{HL} = T_{0HL} + T_{1HL}(F/O)$

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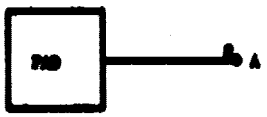
SIDE INPUT PAD

STAR STANDARD CELL NO. 2100

0 DEVICES
1 PIN: CELL WIDTH = 10 GRIDS METAL GATE CMOS

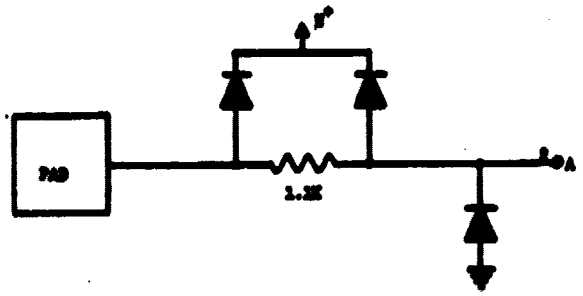
LOGIC SYMBOL



TRUTH TABLE

N/A

SCHEMATIC



DYNAMIC DATA

RISE & FALL

N/A

PROP. DELAY

N/A

RELATIVE TO OUTPUT VOLTAGE

TRANSITION TIME

--- RISE
___ FALL

$T_R = T_{0R} + T_{1R}(F/O)$

$T_F = T_{0F} + T_{1F}(F/O)$

CAPACITANCE

PIN No.	ABSOLUTE (PF)	NORMALIZED
2	2.2	2.34

PROPAGATION DELAY

----- LOW TO HIGH
_____ HIGH TO LOW

$T_{LH} = T_{0LH} + T_{1LH}(F/O)$

$T_{HL} = T_{0HL} + T_{1HL}(F/O)$

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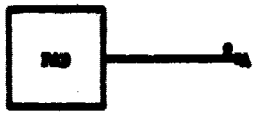
LEFT OUTPUT PAD

STAR STANDARD
CELL NO. 9130

0 DEVICES
1 PIN CELL WIDTH = 30 GRIDS METAL GATE CMOS

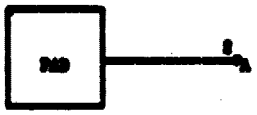
LOGIC SYMBOL



TRUTH TABLE

N/A

SCHEMATIC



DYNAMIC DATA

RISE & FALL

N/A

PROP. DELAY

N/A

RELATIVE TO OUTPUT VOLTAGE

TRANSITION TIME

--- RISE
___ FALL

$T_R = T_{OR} + T_{LR}(F/O)$

$T_F = T_{OF} + T_{LF}(F/O)$

CAPACITANCE

PIN NO.	ABSOLUTE (PF)	NORMALIZED
2	.05	1.04

PROPAGATION DELAY

----- LOW TO HIGH
_____ HIGH TO LOW

$T_{PLH} = T_{0PLH} + T_{LPLH}(F/O)$

$T_{PHL} = T_{0PHL} + T_{LPHL}(F/O)$

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RIGHT OUTPUT PAD

STAR STANDARD CELL NO. 9120

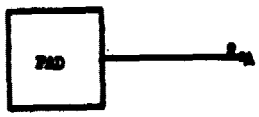
0 DEVICES
1 PIN CELL WIDTH = 10 GRIDS METAL GATE CMOS

LOGIC SYMBOL

TRUTH TABLE

N/A

SCHEMATIC



DYNAMIC DATA

RISE & FALL

N/A

PROP. DELAY

N/A

RELATIVE TO OUTPUT VOLTAGE

TRANSITION TIME

--- RISE
___ FALL

$T_R = T_{0R} + T_{1R}(F/O)$

$T_F = T_{0F} + T_{1F}(F/O)$

CAPACITANCE

Pin No.	Absolute (pF)	Normalized
2	.92	1.64

PROPAGATION DELAY

----- LOW TO HIGH
___ HIGH TO LOW

$T_{LH} = T_{0LH} + T_{1LH}(F/O)$

$T_{HL} = T_{0HL} + T_{1HL}(F/O)$

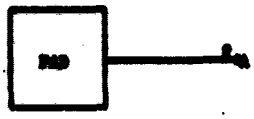
ORIGINAL PAGE IS
OF POOR QUALITY

TOP/BOTTOM INPUT PAD

STAR STANDARD CELL NO. 9200

0 DEVICES
1 PIN CELL WIDTH = 1 GRIDS METAL GATE CMOS

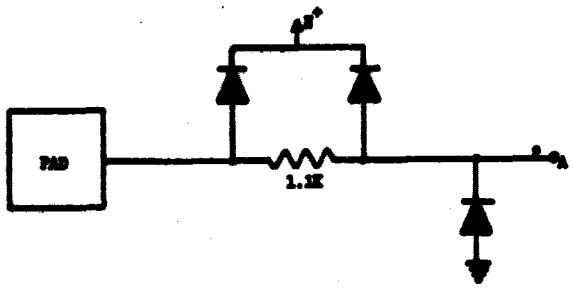
LOGIC SYMBOL



TRUTH TABLE

N/A

SCHEMATIC



DYNAMIC DATA

RISE & FALL	PROP. DELAY
N/A	N/A

RELATIVE TO OUTPUT VOLTAGE

TRANSITION TIME

--- RISE
___ FALL

$T_R = T_{0R} + T_{1R}(F/O)$

$T_F = T_{0F} + T_{1F}(F/O)$

CAPACITANCE

PIN NO.	ABSOLUTE (PF)	NORMALIZED
2	1.2	2.14

PROPAGATION DELAY

---- LOW TO HIGH
___ HIGH TO LOW

$T_{LH} = T_{0LH} + T_{1LH}(F/O)$

$T_{HL} = T_{0HL} + T_{1HL}(F/O)$

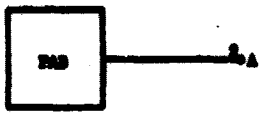
ORIGINAL PAGE IS
OF POOR QUALITY

TOP/BOTTOM OUTPUT PAD

STAR STANDARD CELL NO. 9210

0 DEVICES
1 PIN CELL WIDTH = 10 GRIDS METAL GATE CMOS

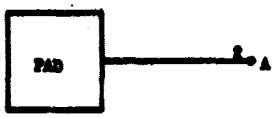
LOGIC SYMBOL



TRUTH TABLE

N/A

SCHEMATIC



DYNAMIC DATA

RISE & FALL

N/A

PROP. DELAY

N/A

RELATIVE TO OUTPUT VOLTAGE

TRANSITION TIME

--- RISE
___ FALL

$T_R = T_{0R} + T_{1R}(F/O)$

$T_F = T_{0F} + T_{1F}(F/O)$

CAPACITANCE

PIN NO.	ABSOLUTE (PF)	NORMALIZED
2	.92	1.64

PROPAGATION DELAY

----- LOW TO HIGH
___ HIGH TO LOW

$T_{LH} = T_{0LH} + T_{1LH}(F/O)$

$T_{HL} = T_{0HL} + T_{1HL}(F/O)$

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