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FINAL REPORT

60 GHz IMPATT DIODE DEVELOPMENT

PREPARED FOR

NASA—LEWIS RESEARCH CENTER
21000 BROOKPARK ROAD
CLEVELAND, OH 44135

W-45797

FINAL REPORT

60 GHz IMPATT DIODE DEVELOPMENT

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HUGHES AIRCRAFT COMPANY
MICROWAVE PRODUCTS DIVISION
3110 WEST LOMITA BOULEVARD
P.O. BOX 2940
TORRANCE, CA 90509-2940

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Project Managers: Edward J. Haugland, Robert R. Romanofsky
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16. Abstract

The objective of this program is to develop 60 GHz GaAs IMPATT Diodes suitable for communications applications. The performance goal of the 60 GHz IMPATT is 1W CW output power with a conversion efficiency of 15 percent and 10-year life time.

During the course of the program, we have developed double-drift (DD) GaAs IMPATT Diodes resulting in the state-of-the-art performance at V-band frequencies. We achieved 1W output power at 52.75 GHz with a conversion efficiency of 14.7 percent at a junction temperature of 228°C. A CW output power of 1.12 W was demonstrated at 51.9 GHz with 9.7 percent efficiency. The best conversion efficiency achieved was 15.3 percent.

We designed V-band DD GaAs IMPATTs using both small-signal and large-signal analyses. We grew GaAs wafers of DD flat, DD hybrid, and DD Read profiles using molecular beam epitaxy (MBE) with excellent doping profile control. Wafer evaluation was routinely made by the capacitance versus voltage (C-V) measurement. We also used secondary ion mass spectrometry (SIMS) analysis for more detailed profile evaluation.

The GaAs wafers were thinned to below 10 μm (by applying a thickness control pattern). This minimized the diode series resistance and provided a well-defined mesa configuration. We have successfully developed pill-type (Continued)

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16. Abstract (Continued)

diodes which enabled us to use diamond heatsinks, realizing substantial reduction in diode thermal resistance. The number of available diode chips from a same size wafer also increased by a factor of approximately 10 compared with that obtained in plated heatsink configuration.

The RF performance was evaluated through extensive circuit tuning in a coaxially coupled reduced-height waveguide cavity. This cavity provided a wide range of impedance at the device terminal. The diode RF performance was very sensitive to both bias and circuit conditions. The maximum output power appeared to be thermally limited.

The V-band GaAs IMPATTs failed over a wide temperature range in a step-stress test. The diode failure appeared to be process-related. The majority of diodes with Au-Zn metallization on the epi side failed around 350°C while diodes with Pt-Ti-Pt-Au metallization mostly failed between 400 and 425°C. The predominant failure mode was shorting.

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1.0 INTRODUCTION AND SUMMARY

The objectives of this program are to design, fabricate, test and deliver high performance, reliable 60 GHz GaAs IMPATT diodes suitable for communications applications. The performance goal of the diodes is 1W CW output power with a dc-to-RF conversion efficiency greater than 15 percent. The intended lifetime of the diodes is a minimum of ten years.

The program originally called for three iterations of diode design, fabrication, test and delivery, with a technology assessment study near the end of the program. During the course of the program, we submitted a proposal for the program modification in response to RFP No. RFP-504014, and were granted approval from the NASA-Lewis Research Center. The proposed program (with a 12-month add-on) is divided into nine major tasks, as required in the RFP. The program's technical tasks are basically four iterations of 60 GHz GaAs IMPATT design, fabrication, test and delivery in addition to a reliability test (dc step-stress test) and a technical assessment study.

We selected double-drift (DD) structures for the high-performance 60 GHz GaAs IMPATTs. However, we opted for a progressive approach to the diode design and fabrication, from single-drift (SD) Read structures through DD flat, to DD Read structures. Because of the uncertainties associated with material and physical parameters, several iterations were required for the optimization of the profile design and fabrication process.

At the beginning of the program, little information was available for the profile design of 60 GHz GaAs IMPATTs. In spite of the superior performance of GaAs IMPATT diodes in the microwave frequency range, development work in millimeter-wave GaAs IMPATTs has been limited in the past because of the large intrinsic response time of electrons in GaAs material. The initial design was basically based on the small-signal analysis and scaling of the design parameters for GaAs IMPATTs at lower frequencies. The large-signal analysis and the experimental evaluation data of the previous designs later provided more reliable information for the diode optimization.

Molecular beam epitaxy (MBE) was chosen for the baseline material growth approach to achieve the design profiles with submicrometer layer thicknesses. Recognizing the limited suppliers of the MBE technology, we also used vapor phase epitaxy (VPE) as a supplement. At the early stage, diode development was hampered by difficulties in growing quality materials on large substrates. However, operator experience, coupled with reactor modification and new-generation MBE machines, has gradually alleviated this problem and now allows growth of wafers as large as three inches in diameter with good profile control. Control of complex doping profiles of 60 GHz GaAs IMPATT diodes was difficult with the VPE technique. Because of the relatively fast growth rate in VPE, the transition between layers was graded, especially in the p-n junction region.

The doping profile has been evaluated routinely by capacitance versus voltage (C-V) measurement in step-etched GaAs wafers. Although we can obtain a complete profile by compositing the measured data, this technique fails to provide detailed information around the p-n junction because of the built-in depletion width. We conducted the secondary ion mass spectrometry (SIMS) analysis on some sample wafers to supplement the C-V measurement data. According to these evaluation data, many MBE wafers indicated uniform doping concentration in each layer, with abrupt transitions between layers.

To minimize diode series resistance, we thinned the GaAs wafer thickness below 10 μm. We gained precise control of wafer thickness by developing a control channel pattern. This thin wafer thickness also contributed to the fabrication of well-defined mesa diodes. The early diodes were fabricated in integrated (silver-plated) heatsink configuration with Ti-Au, Pt-Ti-Au or Au-Zn metallization on the epitaxial side, and Au-Ge-Ni metallization on the substrate side. Although we obtained reasonable RF performance from some plated heatsink diodes, their measured thermal resistance was too high to meet the program requirement.

The successful fabrication of pill-type diodes established a significant contribution for high performance V-band GaAs IMPATT development. The number of diode chips available from wafers of the same size increased by a factor of approximately ten, through elimination of the large area required for plated

heatsink diodes. By thermocompression-bonding the diodes to metallized diamond heatsinks, we reduced the thermal resistance of a pill diode by as much as 50 percent, compared to that of a plated heatsink diode. The pill diodes were mostly metallized either Au-Zn or Pt-Ti-Pt-Au on the epi side of the wafer. We mounted the diodes inside a miniature quartz-ring package using a one-mil diameter gold wire in cross-strap configuration.

Single-drift diodes with a Schottky contact made directly on n-type material often indicated poor breakdown and burned out prematurely in RF evaluation. Although growing a p-layer prior to metallization resulted in sharp breakdown, the RF performance of the SD diodes was limited to a couple hundred milliwatts.

We obtained about 500 mW output power in the frequency range between 45 and 55 GHz from the DD GaAs IMPATTs on plated heatsinks. Because of the high thermal resistance, the input power was restricted to a bias current of 9 to 12 kA/cm^2. We were able to increase the bias current density of the pill diodes on diamond heatsinks to about twice that of the plated heatsink diodes, resulting in state-of-the-art RF performances. We achieved 1W output power at 52.75 GHz with 14.7 percent efficiency at a junction temperature of 228°C. The highest output power measured at V-band was 1.12 W and the best efficiency was 15.3 percent from a DD hybrid diode.

The RF performance and noise characteristics of the V-band GaAs IMPATTs were sensitive to bias and circuit conditions. When mismatched, the diode burned out even at low bias current levels, often accompanied with significant noise degradation. The maximum output power appeared to be thermally limited, with the output power still increasing at the point of diode failure. The measured AM and FM noises of the V-band GaAs IMPATTs were slightly better than those of the silicon counterparts.

The step-stress test results of V-band DD GaAs IMPATTs seemed to indicate many process-related diode failures. The GaAs IMPATTs failed over a wide temperature range. The maximum failure temperature of the diodes with Au-Zn metallization on the epi side was 375°C, about 50° lower than that of the diodes with Pt-Ti-Pt-Au metallization. This was the direct consequence of higher thermal resistance of the diode with Pt-Ti-Pt-Au metallization.

According to the program schedule, a total of 40 V-band GaAs IMPATT diodes were delivered to the contract office at the end of four different phases. On each occasion, one diode was mounted inside the test circuit for the contract office to confirm the test data. The success of the program was manifested by the delivery of 25 high performance V-band GaAs IMPATT diodes at the end of the program. Typical output power of the delivery diodes was 1 W with about 13 percent efficiency with an average junction temperature rise of 236°C.

The sections below describe the technical approaches and efforts that led to successful completion of the program. Diode design of 60 GHz GaAs IMPATTs is discussed in Section 2. The material growth and evaluation, and diode fabrication are covered in Sections 3 and 4, respectively. Diode evaluation, and test circuits are described in Section 5 and the step-stress test and its results are discussed in Section 6. Section 7 describes the deliverables made during the course of the program and includes the test data. In Section 8, we draw a conclusion based on the work of this program and suggest some future work required to further improve the performance of GaAs IMPATT diodes.

2.0 IMPATT DIODE DESIGN

We have selected double-drift (DD) structures for the 60 GHz GaAs IMPATT development to meet the program goals of 1 W CW output power and 15 percent conversion efficiency. We designed DD flat, DD hybrid, and DD Read profiles. Both hi-lo and lo-hi-lo profiles were applied for DD hybrid and DD Read diodes. In Read structures, the avalanche region is well confined around the junction area and this provides better phase relationship between the voltage and current, resulting in improved efficiency.

We initially designed diode doping profiles based on small-signal analysis. During the course of the program, we developed a large-signal computer program and used it for profile optimization and refinement of the 60 GHz GaAs IMPATTs. The large-signal simulation data indicated that the program goals could be achieved using DD hybrid or DD Read diodes in optimum conditions.

2.1 DOPING PROFILES

The IMPATT profile structures can be generally divided into three types: the flat, the Read, and the hybrid. The flat and Read profiles can be subdivided into single-drift (SD) and double-drift (DD) structures. The Read-type profiles can be further divided into the true Read, the hi-lo and the lo-hi-lo structures according to their doping configurations. The hybrid profile is a DD structure with a flat profile in one side and a Read profile in the other side. Double-drift structures were selected for 60 GHz GaAs IMPATTs to meet the high power and high efficiency requirements. They have a single avalanche region and two drift regions, one for electrons and one for holes. Since the DD diode area can be twice as large as the SD diode for the same impedance, the RF output power can be increased by about a factor of 4. (More detailed calculations[1] indicate that this estimate is overly optimistic; the actual factor is around 2.7.) The efficiency of the DD diode shows about 30 percent increase over the SD case. Series action gives twice the RF output power per unit area but the dc voltage increases by only about 50 percent.

The p-side doping profile of the double-drift IMPATT diodes was designed to be slightly punchthrough at normal operating conditions. Because of the low hole mobility in GaAs, any undepleted region in the p-side may result in high series resistance. However, attention must be paid to the reported susceptibility of non-punchthrough IMPATT diodes to subharmonic oscillations and parametric instability.[2]

2.1.1 Double-Drift Flat Structure

The DD flat structure has flat profiles in both the n- and p-side of the device as shown in Figure 1. The p-side is designed to be slightly punchthrough to minimize the series resistance. Although the negative resistance of the flat structure diodes is lower than that of Read-type diodes, it is relatively flat over a wide frequency range. Therefore, performance of these diodes is less sensitive to operating frequency. In addition, fabrication of DD flat diodes is easier than that of Read-type diodes.

2.1.2 Double-Drift Hybrid Structure

The DD hybrid structure is a combination of SD flat and SD Read structures. The diode resembles a p-type SD flat structure in series with an n-type SD Read structure. Figure 2 shows the general doping and electric field profiles for a DD hybrid (hi-lo) structure. Since the electron mobility is much higher than the hole mobility in GaAs, the Read-type is always in the n-side, and the flat p region is designed to be punchthrough at operating current to reduce the series resistance.

While the lo-hi-lo structure can provide a more favorable electric field profile for high-performance IMPATTs, the hi-lo structure is easier in material growth. The advantage of easier growth is very important for high frequency devices in which the doping spikes for the Read profiles are so thin that they become extremely difficult to fabricate. The hi-lo structure has also shown lower power and frequency sensitivity over a wide temperature range in X-band GaAs IMPATTs developed at Hughes.

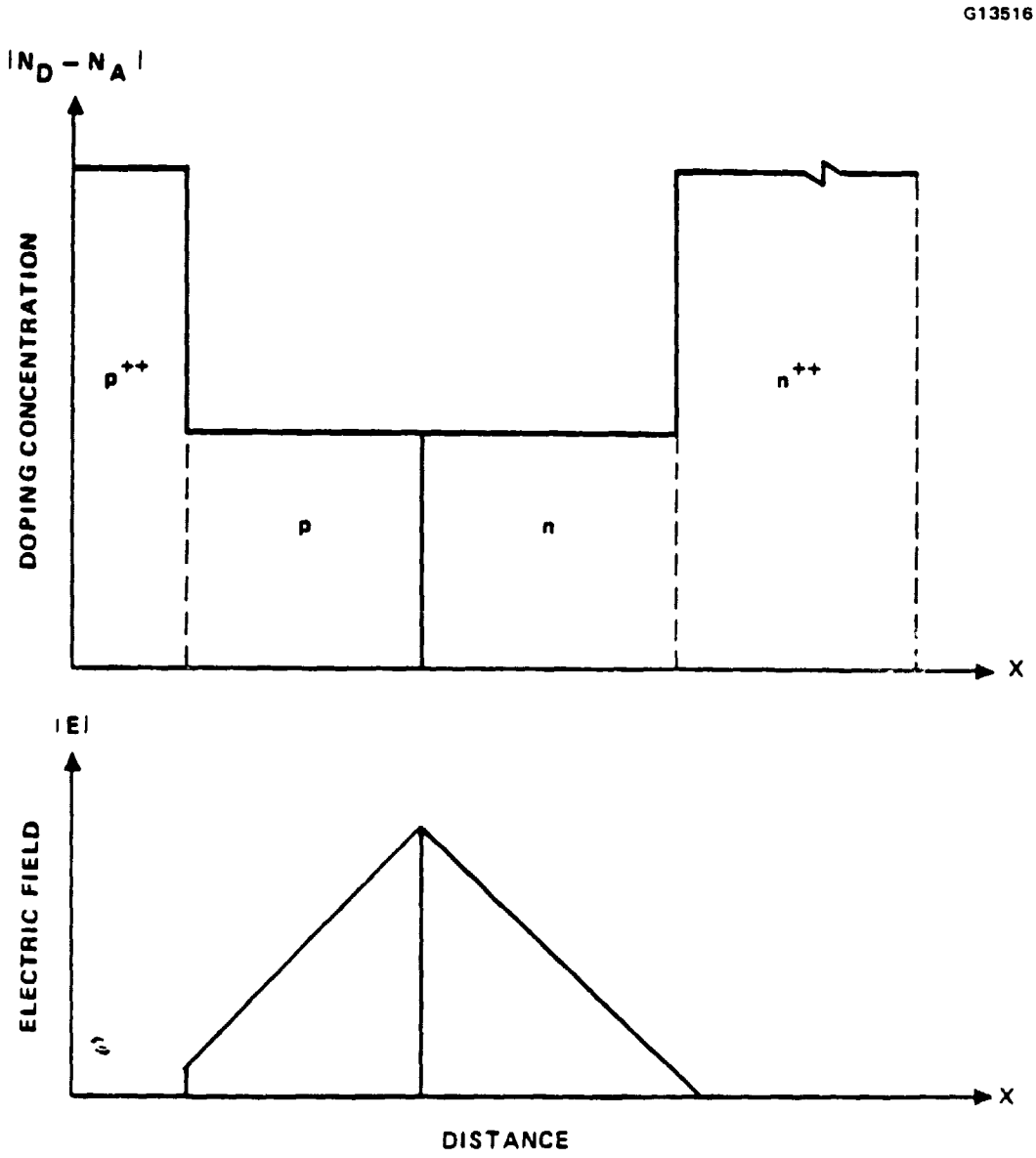


Figure 1 Doping and electric field profiles of DD flat structure.

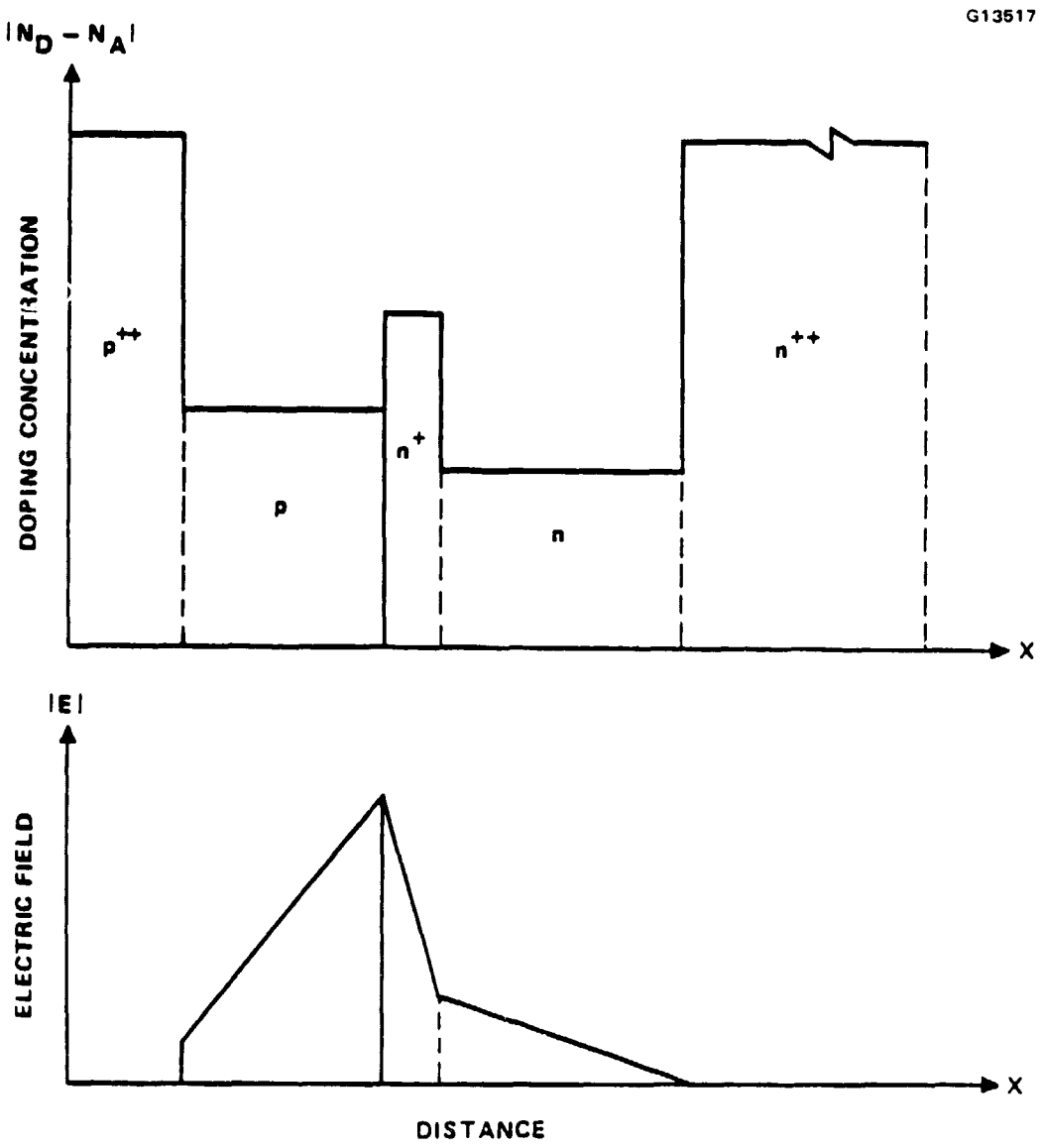


Figure 2 Doping and electric field profiles of DD hybrid structure.

2.1.3 Double-Drift Read Structure

The DD Read structure has Read profiles in both the n- and p-sides of the device as shown in Figure 3. Although the hi-lo profile is used both in n and p regions in this figure, the lo-hi-lo profile can also be used in either side or both sides of the structure, bearing in mind that the lo-hi-lo profile is more difficult to grow than the hi-lo profile.

The DD Read diode provides a more confined avalanche region than the DD hybrid diode. However, attention must be paid to keep the avalanche region wide enough for optimum IMPATT performance.

2.2 SMALL-SIGNAL ANALYSIS

Small-signal calculations[3] proved to be useful in the analysis of IMPATT diode operation. The basic equations governing the electron and hole currents and the electric fields are the current continuity equations for electrons and holes:

$$q\,\partial n/\partial t = G + \partial J_n/\partial x \tag{1}$$

$$q\,\partial p/\partial t = G + \partial J_p/\partial x \tag{2}$$

and Poisson's equation:

$$\varepsilon\,\partial E/\partial x = q(p - n + N_D - N_A) \tag{3}$$

where

$$G = \alpha J_n + \beta J_p \tag{4}$$

t = time (S)
x = distance (cm)
n = electron density (cm^{-3})
p = hole density (cm^{-3})

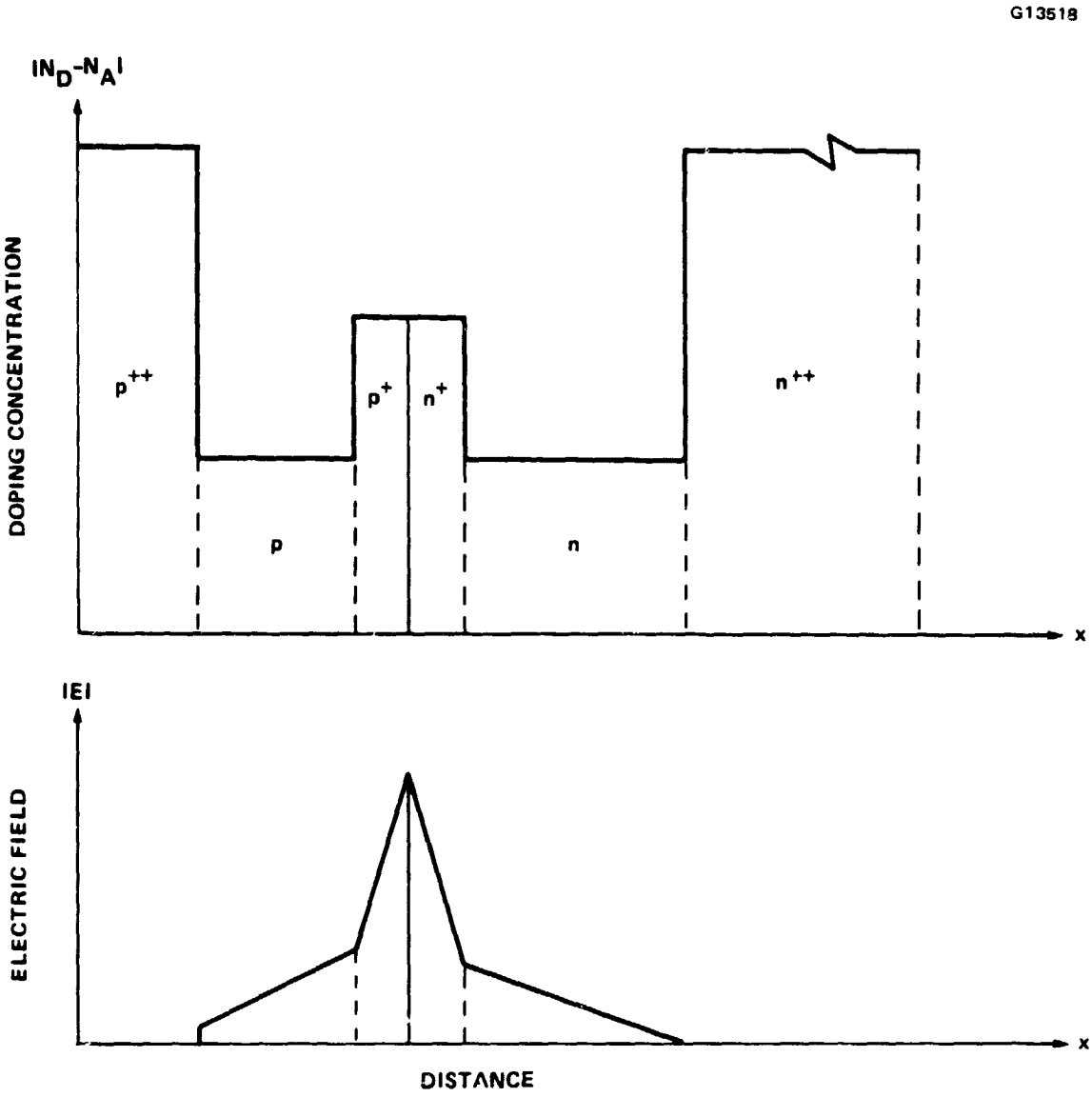


Figure 3 Doping and electric field profiles of DD Read structure.

J_n, J_p = electron and hole current densities (A cm^{-2})

G = impact avalanche generation rate (cm^{-3} S^{-1})

$\mathcal{E}$ = electric field intensity (V cm^{-1})

q = electronic charge (C)

ε = dielectric constant (F cm^{-1})

N_D, N_A = donor and acceptor impunity concentrations (cm^{-3})

v_n, v_p = electron and hole velocities (cm S^{-1})

α, β = electron and hole ionization coefficients (A cm^{-3})

The particle densities n and p are related to the current densities by:

$$J_n = q\, v_n\, n \tag{5}$$

$$J_p = q\, v_p\, p \tag{6}$$

We can linearize Equations (1), (2), and (3) by setting the electric field and particle current densities each equal to a dc part plus a small ac part:

$$E = E_o + E_1\, e^{j\omega t} \tag{7}$$

$$J_n = J_{no} + J_{n1}\, e^{j\omega t} \tag{8}$$

$$J_p = J_{po} + J_{p1}\, e^{j\omega t} \tag{9}$$

E_o, E_1, J_{no} J_{n1}, J_{po} and J_{p1} are all independent of time.

If Equations (7), (8), and (9) are substituted into Equations (1), (2), and (3), the latter equations separate into equations for the dc and ac solutions. The time derivatives vanish for the dc equations and the resulting dc equations are:

$$\frac{\partial E_o}{\partial x} = \frac{1}{\varepsilon}\left(\frac{1}{v_n} + \frac{1}{v_p}\right) J_{no} + \frac{q}{\varepsilon}\,(N_D - N_A) - \frac{J_o}{v_p} \tag{10}$$

$$\frac{\partial J_{no}}{\partial x} = (\alpha - \beta)\, J_{no} + \beta J_o \tag{11}$$

where $J_o = J_{no} + J_{po}$ is the total dc bias current density. The dc equations can be solved numerically, subject to a set of boundary conditions.

The ac equations are obtained by retaining the terms linear in the ac parts. Time derivatives with respect to t are replaced by $j\omega$. The ac equations are:

$$\frac{\partial E_1}{\partial x} = \frac{j\omega}{v_p} E_1 + \frac{1}{\varepsilon}\left(\frac{1}{v_n} + \frac{1}{v_p}\right) J_{n1} - \frac{J_1}{\varepsilon v_p} \tag{12}$$

$$\frac{\partial J_{n1}}{\partial x} = (\alpha' J_{no} + \beta' J_{po} - j\omega\varepsilon\beta)\, E_1 + \left(\alpha - \beta - \frac{j\omega}{v_{n1}}\right) J_{n1} + \beta J_1 \tag{13}$$

where $J_1 = J_{n1} + J_{p1} + j\omega E$, is the total ac current density. The primes indicate derivatives with respect to field. After obtaining the dc solutions, the ac equations can be solved for any desired frequency. The ac voltage V_1 across the depletion region is then given by:

$$V_1 = \int E_1 \, dx \tag{14}$$

where the integral is taken across the depletion region. The ac impedance Z and admittance Y are then found from:

$$Z = 1/Y = V_1/J_1 A \tag{15}$$

where A is the device area.

The diode can be modeled by specifying the doping profile. This profile can be any arbitrary function of x. The total bias current density must also be specified. We developed a computer program based on the above equations that calculates the small-signal IMPATT characteristics.

The initial design profiles of the 60 GHz GaAs IMPATT diodes were based on the results of the small-signal analysis and the scaling of the design parameters at lower frequencies. The accuracy of this analysis depends in large part on the input data of the ionization rates as a function of electric field, but the exact ionization rates in GaAs as a function of electric field and temperature are not well established. The small-signal program calculates the electric field profile and device admittance for a specified current density, operating junction temperature, and doping concentration. The program also determines the breakdown voltage, the operating voltage, and the required thickness of the drift region. The design is assumed to be optimized when the maximum negative conductance and the minimum negative Q occur near the desired frequency.

Figure 4 shows the doping profile and the dc electric field profile for a DD hybrid GaAs IMPATT diode that was produced by the small-signal analysis. The device small-signal admittance per unit area as a function of frequency is shown in Figure 5. The maximum negative conductance and the minimum negative Q are located near 60 GHz, the desired operating frequency for the diode. In this calculation we assumed an operating temperature of 250°C and an operating current density of 8 kA/cm^2.

We started our diode design with flat and hybrid profiles in both SD and DD structures. The flat and hi-lo Read profiles were chosen mainly because of their ease in material growth. The hi-lo structure, because of its slower electric field gradient, may also be less sensitive to the doping concentration of highly doped n^+ layer.

When the RF performance was evaluated, the diodes designed by small-signal analysis appeared to operate better at frequencies lower than the design frequency. This observation agreed with some recent publications[4,5] which reported good RF performance of EHF GaAs IMPATT diodes with active layer thicknesses shorter than the values predicted by conventional analysis. A possible reason is that the saturation velocity of electrons and holes in GaAs material, especially at high temperatures, is lower than previously thought.[6,7]

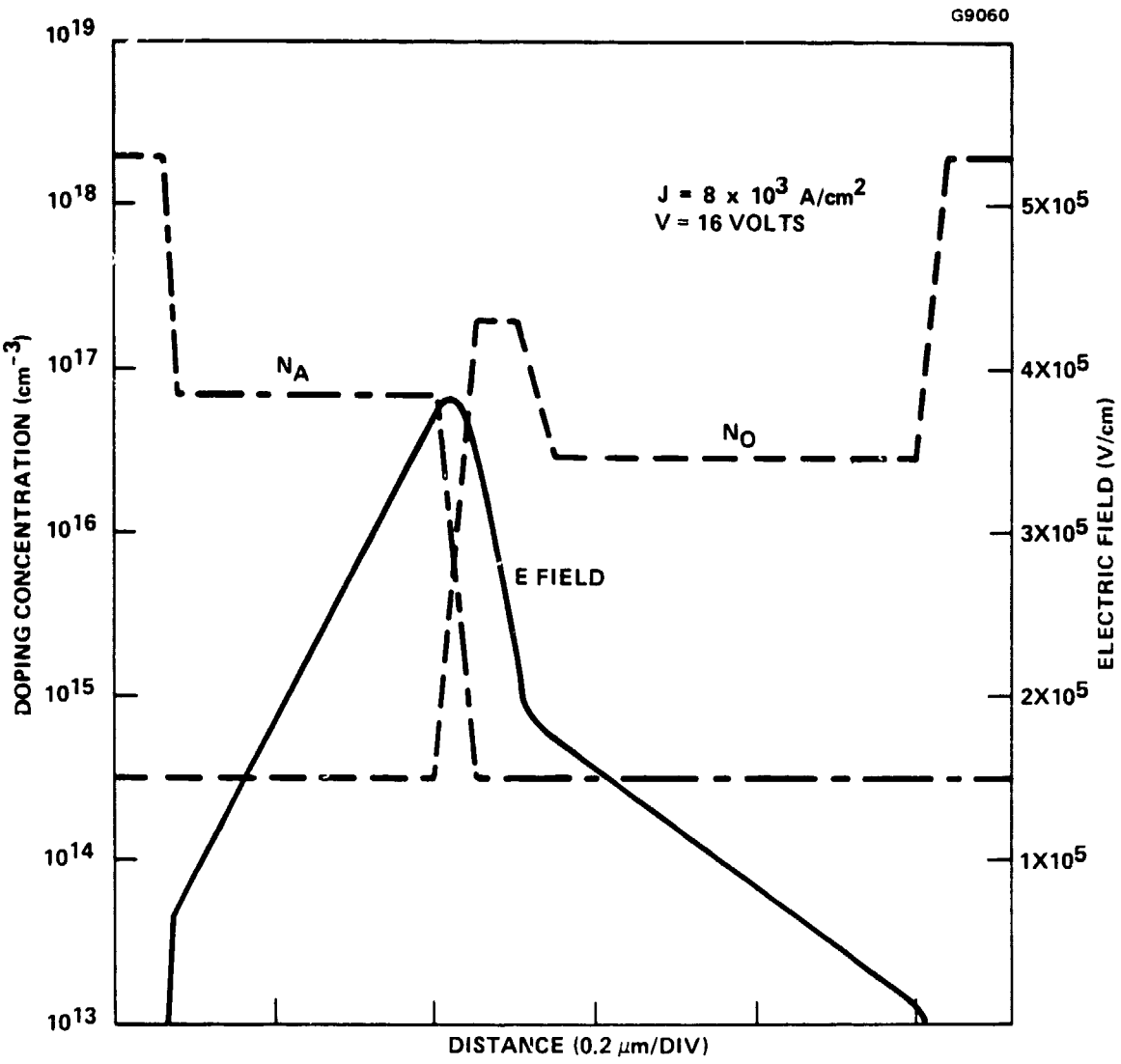


Figure 4 Doping and dc electric field profiles for a 60 GHz GaAs DD hybrid IMPATT.

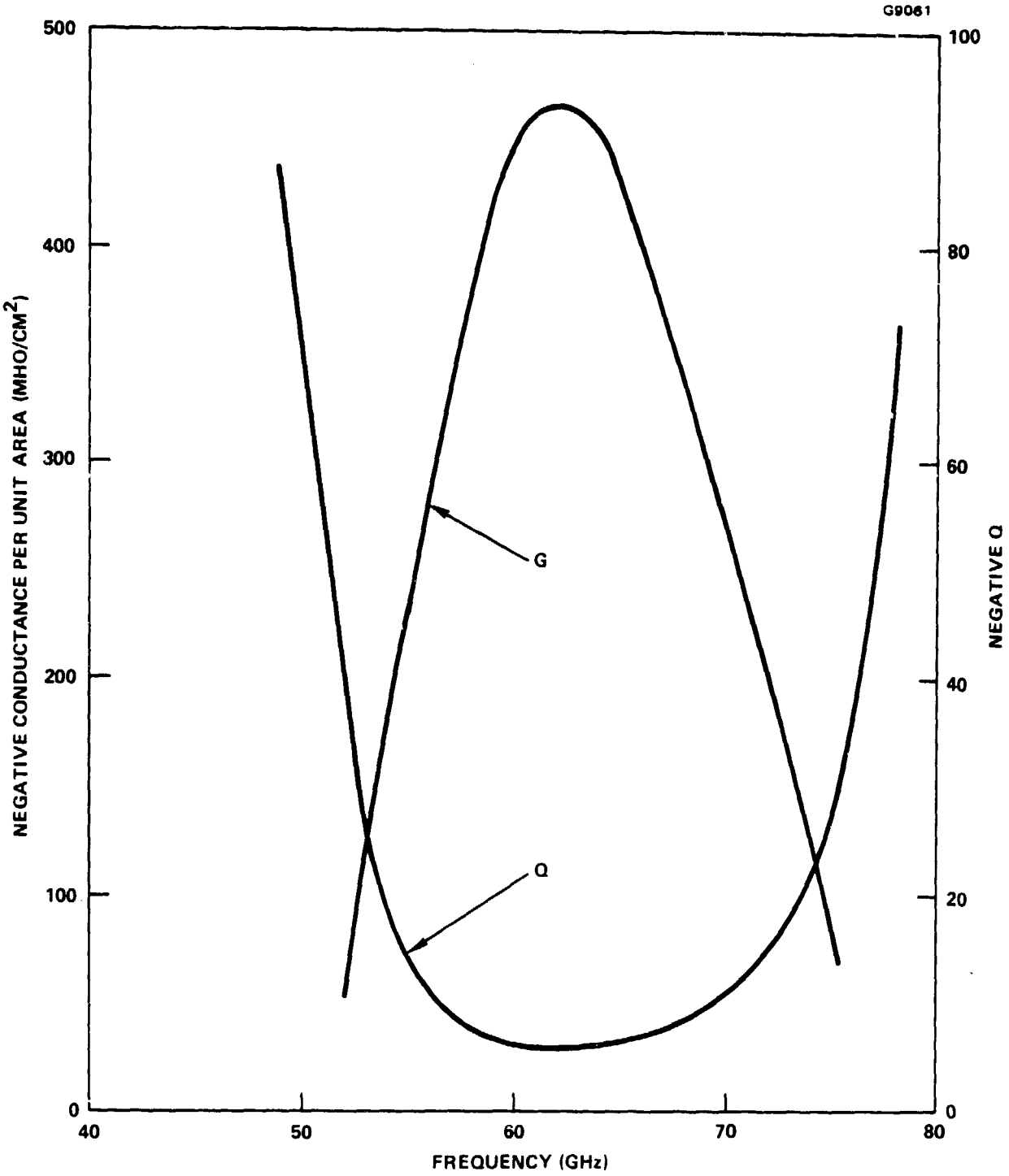


Figure 5 Small-signal negative conductance and Q per unit area for the GaAs IMPATT doping profile of Figure 4.

In response to this new information, we modified the design profiles, reducing the active layer thicknesses and increasing doping concentrations in drift regions accordingly. Figures 6 and 7 represent the modified design profiles of the DD flat and DD hybrid structures. Our symmetric DD flat structure design permits the electric field to punch through at the p^{++}-p and n-n^{++} interfaces under normal conditions.

The improved RF performance of these diodes indicated that our profile modification efforts were headed in the right direction. However, optimum profiles derived from these experimental data indicated some discrepancy when compared to the large-signal IMPATT simulation results. Because the large-signal analysis basically depends on assumed conditions and material parameters, some of which are ill-defined for GaAs material, the results must be experimentally verified. Applying a compromise approach for profile adjustment, we used existing profiles to slightly modify the design. We also designed a symmetrical DD Read structure, as shown in Figure 8.

The design profiles have been modified several times using the information obtained in RF evaluation of the diodes. Later, we also designed DD hybrid and DD Read diodes using the lo-hi-lo profile instead of the hi-lo profile.

2.3 LARGE-SIGNAL ANALYSIS

Although the small-signal analysis was useful in the IMPATT analysis, it does not provide an adequately detailed analysis of high performance IMPATT diodes. The optimum performance can be achieved through proper interaction of the diode with the external circuit. Sufficiently detailed information can be provided only by a large-signal analysis. We developed a numerical simulation program for large-signal IMPATT analysis because of the nonlinearity of the equations which describe the behavior of the particles in high electric fields, particularly at high-frequency operation.

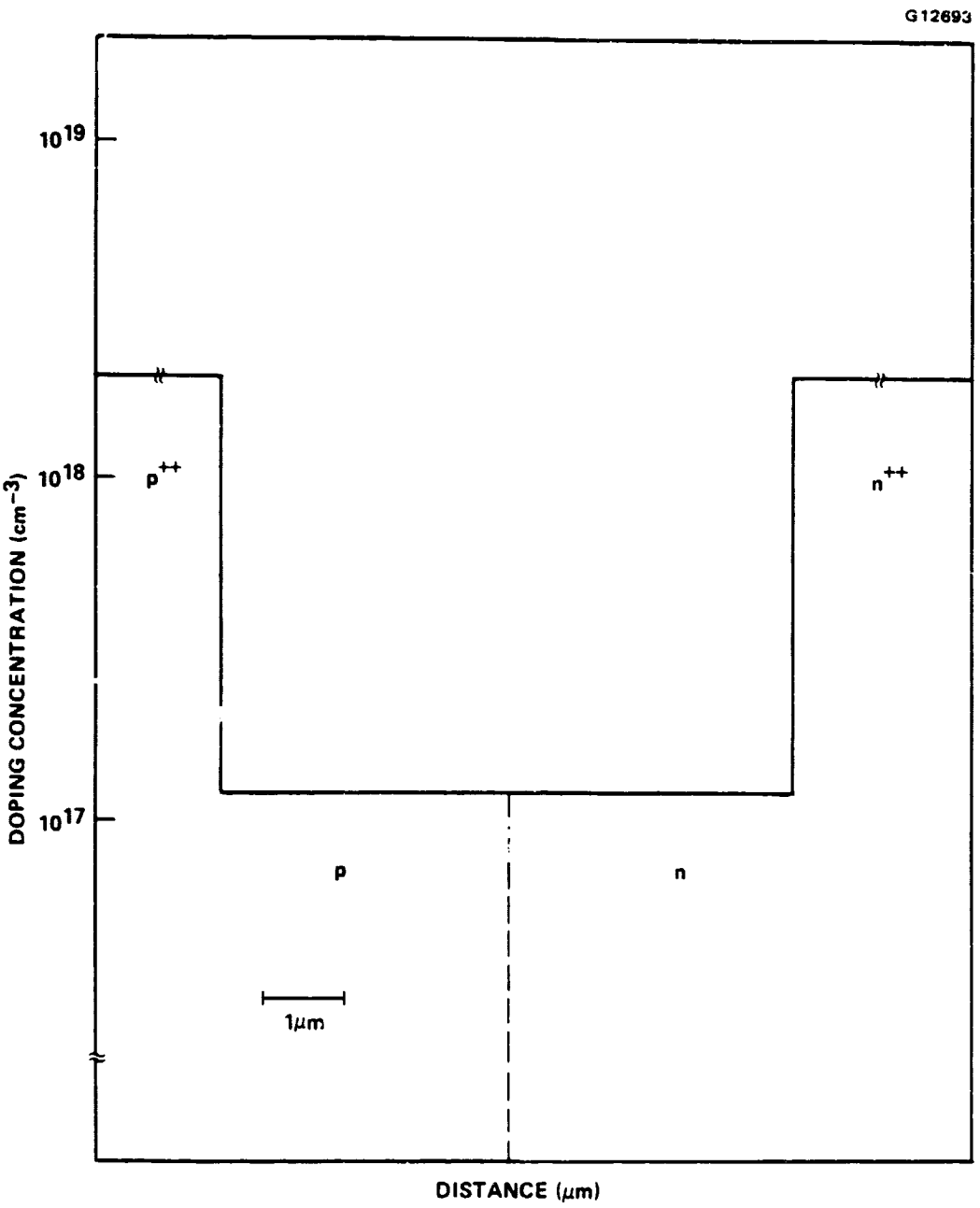


Figure 6 Design profile of 60 GHz DD flat GaAs IMPATT.

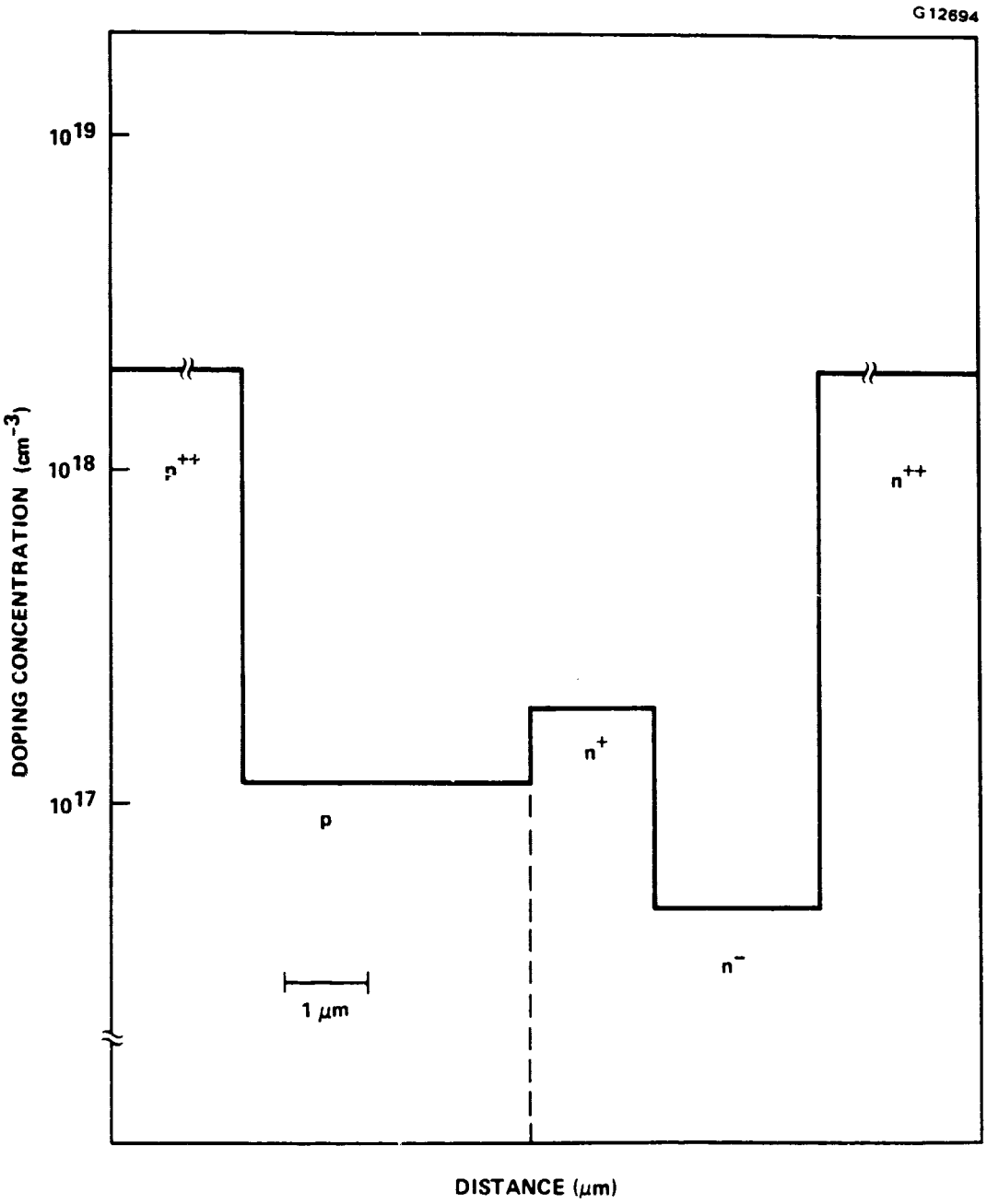


Figure 7 Design profile of 60 GHz DD hybrid Read GaAs IMPATT.

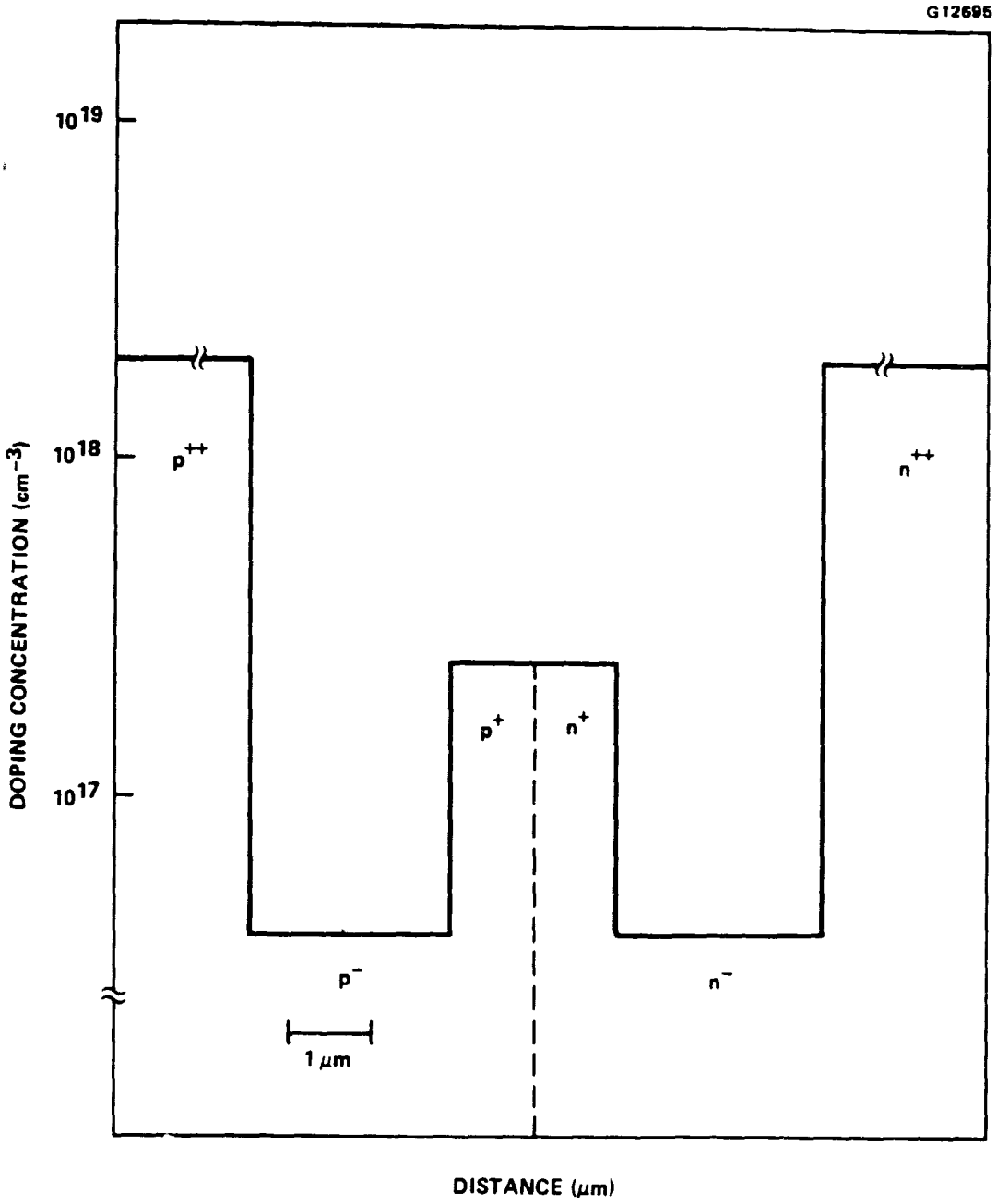


Figure 8 Design profile of 60 GHz DD Read GaAs IMPATT.

2.3.1 Computer Simulation

In our large-signal analysis of an IMPATT diode, the following relationships were used between the current densities and particle densities:

$$J_n = qnv_n - qD_n \, \partial n / \partial x \tag{16}$$

$$J_p = qpv_p - qD_p \, \partial p / \partial x \tag{17}$$

where D_n and D_p are the diffusion coefficients ($cm^2 \, S^{-1}$) for electrons and holes. The nonlinear partial differential equations for the current continuity equations, Poisson's equation, and the current density equations can now be approximated by a set of difference equations. These difference equations are then solved for a given set of initial and boundary conditions. The material parameters such as the velocities, diffusion coefficients, and ionization coefficients of electrons and holes are functions of electric field intensity and temperature and may be functionally approximated.

Although an implicit method[8] could provide accurate, stable solutions for the equations, it is too costly for extensive IMPATT analysis. The explicit methods[9,10] may introduce some small errors in the calculation, but they are economic and produce realistic results. We developed a large-signal simulation program using the explicit method.

A computer can store only values of variables at discrete points in space and time. These variables evolve by finite difference equations which relate the value of a variable at a particular point to the values at the other points. A time-space mesh (Figure 9) was chosen to derive the difference equations. The one-dimensional semiconductor is divided into N partitions J = 1,-----, N, N+1). The hole density, electron density, electric field, and the field-dependent material parameters are defined at these field points.

The difference equations for the particular current densities are:

$$J_{n_k}^{j} = q \cdot n_k^j \, v_{n_k}^{j} + q \cdot D_{n_k}^{j} \frac{\left(n_k^j - n_k^{j-1}\right)}{\Delta x} \tag{18}$$

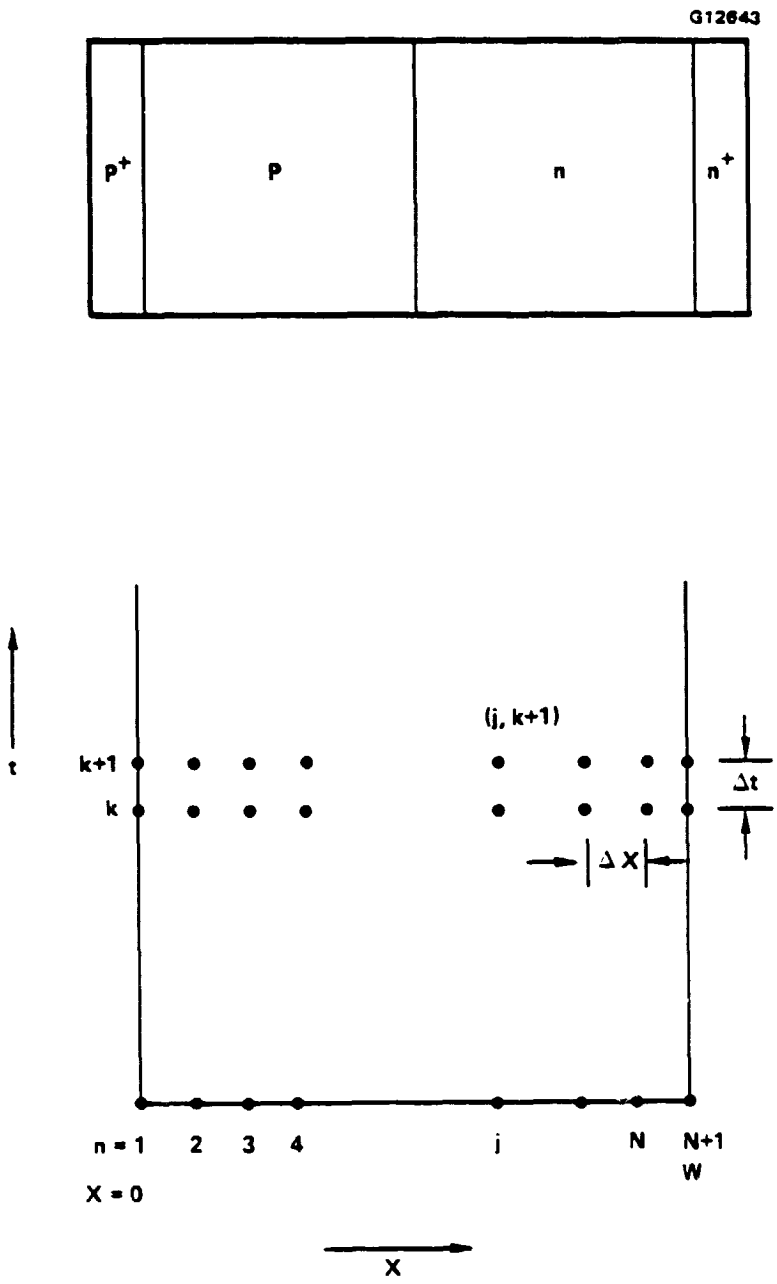


Figure 9 Time-space mesh used in the simulation.

and

$$J_{p_k}^{j} = q \cdot p_k^j v_{p_k}^j + q \cdot D_{p_k}^j \frac{\left(p_k^j - p_k^{j-1}\right)}{\Delta x} \quad (19)$$

The generation term at the j point is approximated by:

$$G_k^j = A_{p_k}^j \cdot \left|J_{p_k}^j\right| + A_{n_k}^j \cdot \left|J_{n_k}^j\right| \quad (20)$$

The continuity equations for electrons and holes and Poisson's equation can be rewritten as:

$$q\frac{\left(n_{k+1}^j - n_k^j\right)}{\Delta t} = G_k^j - \frac{\left(J_{n_k}^j - J_{n_k}^{j-1}\right)}{\Delta x} \quad (21)$$

$$q\frac{\left(p_{k+1}^j - p_k^j\right)}{\Delta t} = G_k^j - \frac{\left(J_{p_k}^j - J_{p_k}^{j-1}\right)}{\Delta x} \quad (22)$$

and

$$E_{k+1}^j = E_{k+1}^{j-1} + q/\epsilon\left(P_{k+1}^j - n_{k+1}^j + N_D - N_A\right) \cdot \Delta x \quad (23)$$

At the kth time step, the particle current densities $J_{n_k}^j$ and $J_{p_k}^j$ are calculated from Equations (18) and (19), and the generation term G_k^j is calculated from (20). Then, Equations (21) and (22) are used to calculate the particle densities n_{k+1}^j and p_{k+1}^j at the advanced (k+1)th time step. The electric field intensity E_{k+1}^j is calculated from (23) with the proper boundary conditions. This procedure can be repeated to advance the solution to k+2, k+3, ---, etc. The time step Δt was determined to satisfy certain numerical stability conditions to ensure that the numerical model does not result in oscillatory behavior and diverge.

To update the electric field at each time step, some relation between the terminal voltage and current is necessary. A simple way is to drive the diode by applying a sinusoidal voltage through a coupling capacitor (Figure 10). This method makes it possible to control the frequency and ac voltage amplitude

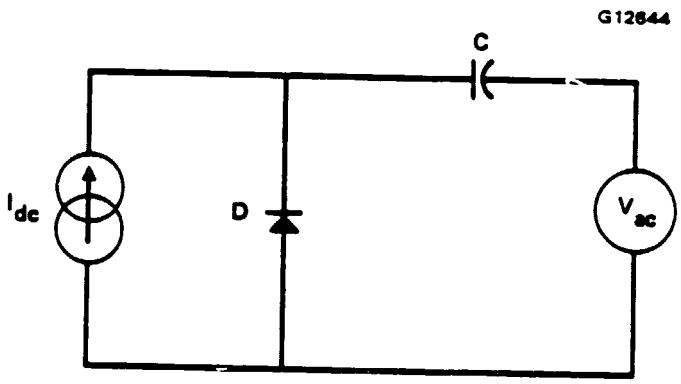


Figure 10 Diode-load configuration.

directly, economizing on the computer time. The coupling capacitor serves only to isolate dc and ac portions of the circuit so that dc current density can be controlled directly.

2.3.2 Material Parameters

The results of the IMPATT simulations depend strongly on the assumed material parameters, such as the velocity, diffusion coefficient and ionization rate of electrons and holes. These material parameters are functions of the electric field and temperature, and, unfortunately, some of the parameter values are uncertain, especially at the high electric fields and temperatures which are often encountered in millimeter-wave IMPATT operations. For the velocities of electrons and holes in GaAs, the following expressions were used in our simulation program:[11,12]

$$v_n(E) = \frac{\mu_n |E| + v_{nsat} \left[\frac{E}{E_v}\right]^4}{1 + \left[\frac{E}{E_v}\right]^4} \tag{24}$$

$$v_p(E) = v_{psat} \left[1 - \exp\left(1 - \frac{\mu_p |E|}{v_{psat}}\right)\right] \tag{25}$$

v_{nsat}, v_{psat}: saturation velocities of electrons and holes ($cm\ S^{-1}$)
μ_n, μ_p: low-field mobilities of electrons and holes ($cm^2\ V^{-1}S^{-1}$)

E_v is the electric field at which the peak electron velocity is obtained and the commonly used value is 4×10^3 V/cm. The assumed mobility expressions were:[13,14]

$$\mu_p = 400 \cdot \left[\frac{300}{T}\right]^{1.9} \tag{26}$$

and

$$\mu_n = \frac{(2.25 \times 10^6)}{T} \tag{27}$$

where T is the absolute temperature (^oK). Based on the recent measurements[15] and the assumption of a linear dependence on the temperature, the following relations are assumed for the saturation velocities for electrons and holes:

$$v_{nsat} = 6.0 \times 10^6 - 5.0 \times 10^3 \cdot (T-300) \tag{28}$$

$$v_{psat} = 6.8 \times 10^6 - 8.0 \times 10^3 \cdot (T-300) \tag{29}$$

The hole diffusion coefficient in GaAs was assumed to be 15 cm^2/S [16] while the electron diffusion coefficient was considered to be field-dependent and was approximated by[12]:

$$D_n(E) = \frac{\frac{kT}{q}\mu_n + 15 \times \left[-\frac{E}{5.8 \times 10^3}\right]^4}{1 + \left[\frac{E}{5.8 \times 10^3}\right]^4} \tag{30}$$

where k is the Boltzmann constant (J/K). The ionization rates of electrons and holes are assumed equal and is given by:[12,17]

$$\alpha(E) = \beta(E) = A \exp\left[-(b/E)^2\right] \tag{31}$$

A linear dependence of the parameters A and b on temperature is assumed, and the discrete values are represented by:

$$A = 1.614 \times 10^5 \times \left[1 + (T-300) \times 7.0 \times 10^{-4}\right] \tag{32}$$

and

$$b = 5.42 \times 10^5 \times \left[1 + (T-300) \times 9.69 \times 10^{-4}\right] \quad (33)$$

In this calculation, we have assumed perfect impedance match of the load to the diode. The computer results do not take into account the substrate resistance, contact resistance, and the circuit loss. The effect of these resistances degrades the diode RF performance and becomes more pronounced as the negative resistance decreases.

2.3.3 Computer Simulation

The diode operating characteristics were calculated for the diode imbedded in the circuit shown schematically in Figure 10. For a specified doping profile, current density, junction temperature, frequency and ac voltage, the program calculates the operating current and voltage, diode admittance, RF output power and efficiency.

The large-signal computer simulation was started with the values around the previous design profiles. Table 1 represents the diode admittance and RF performance for the DD flat structures. The RF performance was optimized by varying the ouput voltage amplitude. An example of diode RF performance versus output voltage amplitude is plotted in Figure 11. In all simulations, the diode was operated at 500°K with the current density of 18 kA/cm^2. The diode area was kept at 0.2×10^{-4} cm^2. The optimum doping concentration of symmetrical DD flat diodes was 8×10^{16} cm^{-3}. However, the change in efficiency with a factor of two variation in doping concentration from 6.0×10^{16} to 1.2×10^{17} was not significant, being less than 2 percent. The simulation data of flat diodes with various thicknesses is shown in Table 2.

Table 3 summarizes the large-signal simulation data of DD hybrid diodes with flat p and hi-lo n profiles. The diodes are again assumed to have an area of 0.2×10^{-4} cm^3 and to be operated at 500°K. The doping concentration of the high n^+ region was varied from 1.25×10^{17} to 2.25×10^{17}/cm^3. All the other parameters were considered to be fixed. The effects of the doping concentration of the flat p and low n regions are shown in Table 4. The epitaxial layer thicknesses were also changed slightly. According to these data, output

TABLE 1

COMPUTER SIMULATION DATA OF 60 GHz GaAs DD FLAT IMPATTS
WITH DIFFERENT DOPING CONCENTRATIONS

Epi-Layer Thickness (μm)	Doping Concentration (cm^{-3})	Conductance (m℧)	Susceptance (m℧)	Output Power (W)	Efficiency (%)
$\ell_p = \ell_n = 0.35$	$p = n = 0.6 \times 10^{17}$	-6.07	112.02	0.99	12.13
	$p = n = 0.7 \times 10^{17}$	-7.75	108.7	1.14	12.44
	$p = n = 0.8 \times 10^{17}$	-8.07	109.03	1.25	13.92
	$p = n = 0.9 \times 10^{17}$	-8.94	108.37	1.24	13.81
	$p = n = 1.0 \times 10^{17}$	-8.10	109.1	1.23	12.82
	$p = n = 1.1 \times 10^{17}$	-9.11	108.84	1.06	12.76
	$p = n = 1.2 \times 10^{17}$	-10.80	108.75	1.03	12.29
$\ell_p = \ell_n = 0.40$	$p = n = 0.6 \times 10^{17}$	-5.87	98.75	1.18	13.12
	$p = n = 0.7 \times 10^{17}$	-7.99	96.0	1.32	13.28
	$p = n = 0.8 \times 10^{17}$	-10.03	96.82	1.49	14.52
	$p = n = 0.9 \times 10^{17}$	-9.55	95.83	1.43	13.91

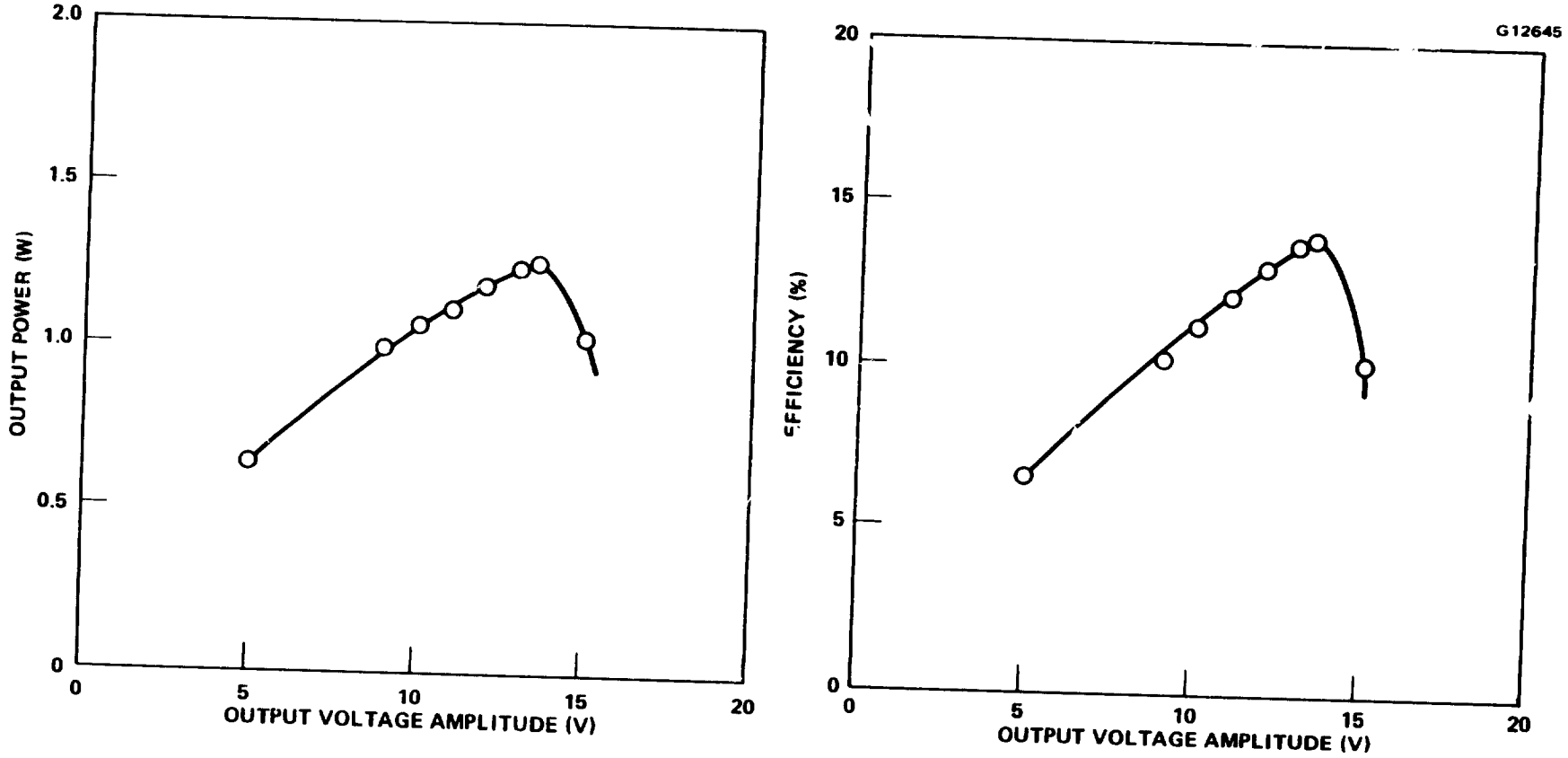


Figure 11 RF performance vs. output voltage amplitude of a 60 GHz DD flat GaAs IMPATT diode ($p = n = 8.0 \times 10^{16}$ cm^{-3}, $\ell_p = \ell_n = 0.35$ μm).

TABLE 2

COMPUTER SIMULATION DATA OF 60 GHz GaAs DD FLAT IMPATTS
WITH DIFFERENT LAYER THICKNESSES

Doping Concentration (cm^{-3})	Epi-Layer Thickness (μm)	Conductance (m℧)	Susceptance (m℧)	Output Power (W)	Efficiency (%)
0.8×10^{17}	$\ell_p = \ell_n = 0.30$	-9.66	125.33	1.11	13.43
	$\ell_p = \ell_n = 0.35$	-8.07	109.03	1.25	13.92
	$\ell_p = \ell_n = 0.40$	-10.03	96.82	1.49	14.52
	$\ell_p = \ell_n = 0.45$	-8.61	91.67	1.43	14.24
	$\ell_p = 0.4, \ell_n = 0.5$	-6.57	90.81	1.21	12.86
	$\ell_p = 0.4, \ell_n = 0.6$	-7.46	81.15	1.28	10.99

TABLE 3

SIMULATION RESULTS OF 60 GHz GaAs DD HYBRID IMPATTS
WITH 0.6 μm ACTIVE LAYER THICKNESS

Doping Concentration (cm^{-3})	Layer Thickness (μm)	Current Density (kA/cm^2)	Conductance (m℧)	Susceptance (m℧)	Output Power (W)	Efficiency (%)
$p = 1.0 \times 10^{17}$ $n^+ = 1.25 \times 10^{17}$ $n = 5.63 \times 10^{16}$	0.35 0.12 0.13	16	-7.67	129.5	0.82	11.82
$p = 1.0 \times 10^{17}$ $n^+ = 1.5 \times 10^{17}$ $n = 5.63 \times 10^{16}$	0.35 0.12 0.13	16	-7.68	129.9	0.85	12.41
$p = 1.0 \times 10^{17}$ $n^+ = 2.0 \times 10^{17}$ $n = 5.63 \times 10^{16}$	0.35 0.12 0.13	16	-9.08	126.9	0.86	12.40
$p = 1.0 \times 10^{71}$ $n^+ = 2.25 \times 10^{17}$ $n = 5.63 \times 10^{16}$	0.35 0.12 0.13	16	-8.75	128.5	0.82	12.38

TABLE 4

COMPUTER SIMULATION DATA OF 60 GHz GaAs
DD HYBRID (HI-LO) IMPATT DIODES

Doping Concentration (cm^{-3})	Epi-Layer Thickness (μm)	Current Density (kA/cm^3)	Conductance (m℧)	Susceptance (m℧)	Output Power (W)	Efficiency (%)
$p = 0.8 \times 10^{17}$ $n^+ = 2.0 \times 10^{17}$ $n = 5.0 \times 10^{16}$	$\ell_p = 0.35$ $\ell_{n^+} = 0.15$ $\ell_n = 0.25$	20	-8.9	100.6	1.47	14.16
0.9×10^{17} 2.0×10^{17} 5.0×10^{16}	0.35 0.15 0.25	20	-9.1	100.9	1.50	14.44
1.0×10^{17} 2.0×10^{17} 5.0×10^{16}	0.35 0.15 0.25	20	-9.0	101.5	1.48	14.40
1.1×10^{17} 2.0×10^{17} 5.0×10^{16}	0.35 0.15 0.25	20	-8.7	102.4	1.44	14.10
1.2×10^{17} 2.0×10^{17} 5.0×10^{16}	0.35 0.15 0.25	20	-8.2	103.8	1.35	13.47

TABLE 4 (CONTINUED)

COMPUTER SIMULATION DATA OF 60 GHz GaAs
DD HYBRID (HI-LO) IMPATT DIODES

Doping Concentration (cm^{-3})	Epi-Layer Thickness (μm)	Current Density (kA/cm^3)	Conductance (m℧)	Susceptance (m℧)	Output Power (W)	Efficiency (%)
$p = 1.1 \times 10^{17}$ $n^+ = 2.0 \times 10^{17}$ $n = 5.0 \times 10^{16}$	$\ell_p = 0.38$ $\ell_{n^+} = 0.14$ $\ell_n = 0.28$	20.0	-8.9	96.2	1.55	14.48
1.1×10^{17} 2.0×10^{17} 4.0×10^{16}	0.38 0.14 0.28	20.0	-9.4	95.6	1.55	14.80
9.7×10^{16} 1.95×10^{17} 3.5×10^{16}	0.4 0.14 0.32	20.0	-9.8	89.5	1.54	14.35
9.7×10^{16} 1.95×10^{17} 3.5×10^{16}	0.4 0.14 0.32	17.7	-9.25	92.3	1.43	15.51

power of 1.4 W can be achievable with 15.5 percent efficiency from a DD hybrid diode.

The RF performance of the best efficiency DD hybrid diode (p: 9.7×10^{16} cm^{-3}, 0.4 μm; n^+: 1.95×10^{17} cm^{-3}, 0.14 μm; n: 3.5×10^{15} cm^{-3}, 0.32 μm) was investigated as a function of operating frequency. The operating frequency and current density were kept at 500°K and 17.7 kA/cm^2, respectively, with a diode area of 0.2×10^{-4} cm^2. Figure 12 represents the normalized diode admittance (to the area) in the frequency range of 40 to 70 GHz. The variation of the negative conductance is only about 2 percent between 50 and 60 GHz. The diode RF performance vs frequency is plotted in Figure 13. The output power and efficiency peak at 60 GHz but are pretty much flat between 50 and 60 GHz.

Table 5 represents the RF performance of the hybrid diode as a function of operating current density. The operating voltage increases with the current density from 24.5 V at 10 kA/cm^2 to 26.8 V at 25 kA/cm^2. The optimum ac voltage changes slightly from 16.6 V to 17.6 V. While the output power increases with the operating current, the conversion efficiency peaks at the current density of 17.7 kA/cm^2. The diode RF performance was also simulated at different junction temperatures, since the temperature increases with input power. The results are shown in Table 6.

We have investigated the effect of the graded transitions on the diode RF performance using the large-signal simulation program. The simulation profiles were based on the present limitation of practical VPE-grown material; the compensated region around the p-n junction is about 0.2 μm and the transition slope between n and n^+ layers is 0.2 μm per decade change in doping concentration. According to simulation results, the RF performance of the diode with graded transitions was inferior (about 3 percent in conversion efficiency) to that of the diode with sharp transitions.

We also conducted the large-signal computer simulation for DD Read IMPATTs. We started the simulation with lo-hi-lo profiles in both p and n regions to compare the simulation results with the published data.[16] Table 7 represents the simulated profiles and computer output results. The total active layer of

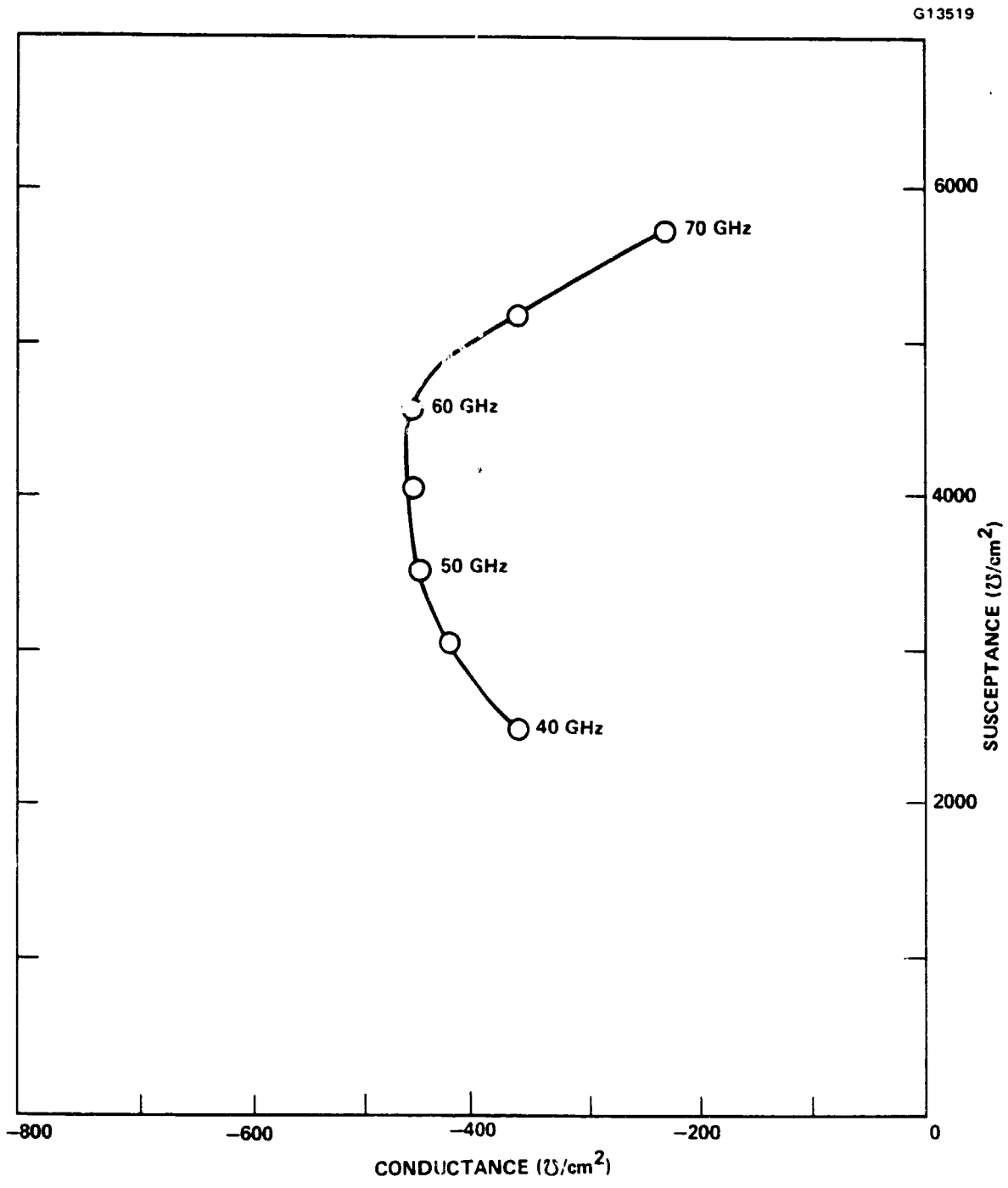


Figure 12 Normalized device admittance.

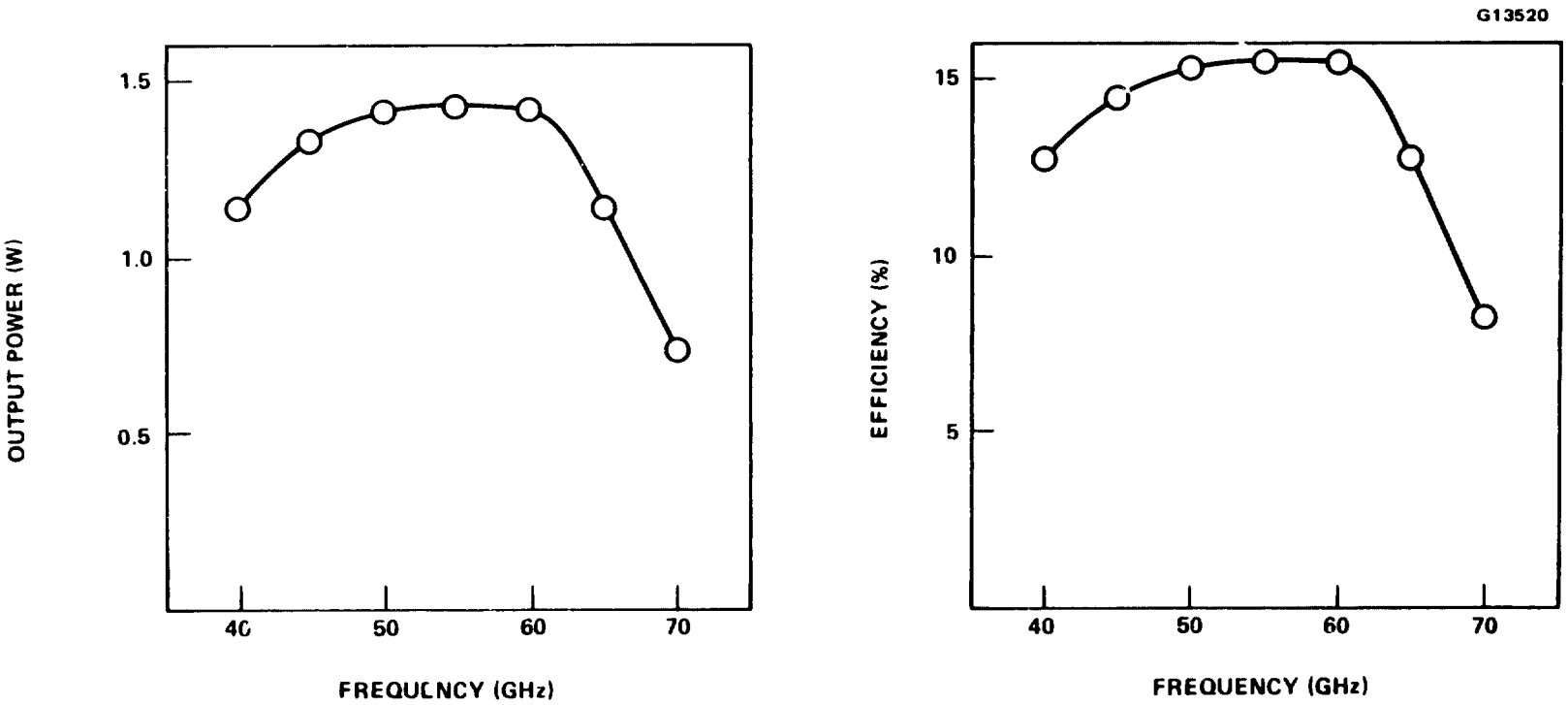


Figure 13 RF performance versus operation frequency.

TABLE 5

COMPUTER SIMULATION DATA OF A 60 GHz GaAs
DD HYBRID IMPATT

Doping Profile	Current Density (kA/cm^2)	Conductance (m℧)	Susceptance (m℧)	Output Power (W)	Efficiency (%)
$p = 9.7 \times 10^{16}\ cm^{-3}$	10.0	-2.8	100	0.39	7.55
0.4 μm	12.5	-4.1	98	0.60	9.52
$n^+ = 1.95 \times 10^{17}\ cm^{-3}$	15.0	-7.2	95	1.05	13.61
0.14 μm	17.7	-9.3	92	1.43	15.51
	20.0	-10.1	90	1.54	14.35
$n = 3.5 \times 10^{16}\ cm^{-3}$	22.5	-10.9	88	1.69	13.89
0.32 μm	25.0	-11.8	85	1.82	13.41

TABLE 6

COMPUTER SIMULATION DATA OF 60 GHz GaAs DD HYBRID IMPATTS
AT DIFFERENT JUNCTION TEMPERATURES

Doping Profile	Current Density (kA/cm^2)	Junction Temperature (°K)	Conductance (m℧)	Susceptance (m℧)	Output Power (W)	Efficiency (%)
$P = 9.7 \times 10^{16}\ cm^{-3}$ 0.4 μm	12.5	450	-5.2	98	0.64	10.67
		500	-5.4	98	0.74	11.70
		550	-5.5	97	0.85	12.59
$n^+ = 1.95 \times 10^{17}\ cm^{-3}$ 0.14 μm	17.7	450	-10	91	1.28	14.22
		500	-9	92	1.43	15.51
		550	-8	92	1.46	14.86
$n = 3.5 \times 10^{16}\ cm^{-3}$ 0.32 μm	22.5	450	-12	86	1.56	13.35
		500	-11	88	1.69	13.89
		550	-10	88	1.77	13.97

TABLE 7

SIMULATION RESULTS OF 60 GHz DD READ GaAs IMPATTS
WITH 0.84 μm ACTIVE LAYER THICKNESS

Doping Concentration (cm^{-3})	Layer Thickness (μm)	Current Density (kA/cm^2)	Conductance (m℧)	Susceptance (m℧)	Output Power (W)	Efficiency (%)
	l_p = 0.34 l_{p^+} = 0.04 l_{p^-} = 0.04	15.0	-7.16	96.8	1.17	14.58
	l_{n^-} = 0.04 l_{n^+} = 0.04 l_n = 0.34	17.7	-8.16	95.0	1.33	14.05
$p = 2.73\times10^{16}$ $p^+ = 5.4\times10^{17}$ $p^- = 5.0\times10^{15}$ $n^- = 5.0\times10^{15}$ $n^+ = 4.87\times10^{17}$ $n = 2.86\times10^{16}$	0.32 0.04 0.06	15.0	-8.62	96.8	0.86	11.88
	0.06 0.04 0.32	17.7	-9.72	94.85	1.04	12.01
	0.30 0.04 0.08	15.0	-8.03	97.0	0.75	10.67
	0.08 0.04 0.30	17.7	-9.95	94.4	0.93	10.99

these diodes was fixed at 0.84 μm. While the doping concentrations were kept to be constant, the distance between the p^+ and n^+ spikes was varied from 0.08 to 0.16 μm. Again, the diodes were assumed to have an area of 0.2×10^{-4} cm^2 and were operated at 500°K junction temperature. The best RF performance was obtained with a distance of 0.08 μm between the spikes.

Then, we performed large-signal simulation on the DD Read diodes with hi-lo profiles. The simulated profiles and computer output results are summarized in Table 8. The epitaxial layer thickness was kept constant (ℓ_p = 0.32 μm, ℓ_{p^+} = 0.1 μm, ℓ_{n^+} = 0.1 μm, ℓ_n = 0.32 μm) with a total thickness of 0.84 μm. The diode size and operating junction temperature were assumed to be same as the previous cases with a current density of 15 kA/cm^2. The best RF performance that could be achieved from a DD Read diode in the given conditions was about 1.3 W output power with 16.3 percent efficiency.

We studied the punch-through characteristic of the 60 GHz DD GaAs IMPATT diodes using a dc computer program. The electric fields at $p^{++}p$ and nn^{++} interfaces are important parameters in designing the high efficiency IMPATTs. High performance IMPATTs require large RF voltage across the diodes. During the negative portion of the RF cycle, IMPATT diodes are usually driven under-punch-through, and some undepleted material is left adjacent to the substrate contributing a series resistance. A heavy punch-through structure would be desirable to minimize the series resistance. However, this leads to a dispersed avalanche zone or causes partial breakdown and generation of minority current in the drift region, thus limiting the efficiency. The electric field at the interfaces should be designed to sustain high field modulation so that the gain due to the large signal offsets the loss due to the undepleted material.

Table 9 shows the electric fields at $p^{++}p$ and nn^{++} interfaces and the punch-through factors of some 60 GHz DD flat GaAs IMPATTs, along with the large-signal RF performances. The layer thicknesses were kept at 0.35 μm for both p and n regions. The electric fields at the interfaces and the punch-through factors of the DD hybrid and DD Read diodes are summarized in Tables 10 and 11. The total layer thickness of the DD hybrid diodes is

TABLE 8

SIMULATION RESULTS OF 60 GHz DD READ GaAs IMPATTS
WITH 0.84 μm ACTIVE LAYER THICKNESS

Doping Concentration (cm^{-3})				Conductance (mS)	Susceptance (mS)	Output Power (W)	Efficiency (%)
p	p^+	n^+	n				
$9.0x10^{16}$	$2.0x10^{17}$	$2.0x10^{17}$	$4.5x10^{16}$	-7.32	98.58	1.01	12.9
$8.0x10^{16}$	$2.0x10^{17}$	$2.0x10^{17}$	$4.5x10^{16}$	-7.11	98.00	1.10	13.9
$7.0x10^{16}$	$2.0x10^{17}$	$2.0x10^{17}$	$4.5x10^{16}$	-6.82	97.66	1.17	14.9
$6.0x10^{16}$	$2.0x10^{17}$	$2.0x10^{17}$	$4.5x10^{16}$	-7.27	96.72	1.25	15.6
$5.0x10^{16}$	$2.0x10^{17}$	$2.0x10^{17}$	$4.5x10^{16}$	-7.43	96.18	1.28	15.8
$4.5x10^{16}$	$2.0x10^{17}$	$2.0x10^{17}$	$4.5x10^{16}$	-7.41	96.02	1.27	15.7
$4.0x10^{16}$	$2.0x10^{17}$	$2.0x10^{17}$	$4.5x10^{16}$	-7.34	95.9	1.26	15.5
$5.0x10^{16}$	$2.0x10^{17}$	$2.0x10^{17}$	$4.0x10^{16}$	-7.33	96.22	1.26	15.5
$4.5x10^{16}$	$2.0x10^{17}$	$2.0x10^{17}$	$5.0x10^{16}$	-7.21	96.53	1.24	15.7
$5.0x10^{16}$	$1.5x10^{17}$	$1.5x10^{17}$	$4.5x10^{16}$	-6.35	96.21	1.21	14.8
$5.0x10^{16}$	$2.5x10^{17}$	$2.5x10^{17}$	$4.5x10^{16}$	-8.32	96.44	1.29	16.3
$5.0x10^{16}$	$3.0x10^{17}$	$3.0x10^{17}$	$4.5x10^{16}$	-9.64	96.41	1.17	15.4

TABLE 9

PUNCH-THROUGH CHARACTERISTICS OF 60 GHz DD FLAT GaAs IMPATTS

Doping Concentration (cm^{-3})	Output Power (W)	Efficiency (%)	Electric Field (10^5 V/cm)		Punch-Through Factor	
			At p^+p	At nn^+	P Side	n Side
$P = n = 0.8 \times 10^{17}$	1.25	13.92	2.40	2.00	1.74	1.69
$p = n = 0.9 \times 10^{17}$	1.24	13.82	1.75	1.68	1.57	1.49
$p = n = 1.0 \times 10^{17}$	1.23	13.81	1.40	1.35	1.43	1.37
$p = n = 1.1 \times 10^{17}$	1.06	12.76	1.10	1.05	1.31	1.26

TABLE 10

PUNCH-THROUGH CHARACTERISTICS OF 60 GHz DD HYBRID GaAs IMPATTS

Doping Concentration ($\times 10^{16}$ cm^{-3})			Output Power (W)	Efficiency (%)	Electric Field (10^5 V/cm)		Punch-Through Factor	
p	n	n^+			At $p^{++}p$	At nn^{++}	p side	n side
7.0	20.0	3.5	1.12	11.53	2.25	1.35	1.90	2.04
8.0	20.0	3.5	1.19	12.60	1.85	1.52	1.65	2.13
9.0	20.0	3.5	1.29	13.82	1.55	1.66	1.45	2.20
9.7	20.0	3.5	1.43	15.51	1.32	1.80	1.39	2.50
11.0	20.0	3.5	1.32	14.61	0.78	1.92	1.19	2.68
9.7	20.0	2.5	1.27	12.89	1.32	2.00	1.37	3.80
9.7	20.0	4.5	1.15	12.40	1.32	1.20	1.37	1.63
9.7	20.0	5.5	0.65	7.35	1.32	0.80	1.37	1.30
9.7	15.0	3.5	1.50	14.54	1.22	2.20	1.26	2.84
9.7	25.0	3.5	0.75	8.54	1.37	1.10	1.42	1.86
9.7	30.0	3.5	0.23	2.83	1.41	0.33	1.46	1.26

TABLE 11

PUNCH-THROUGH CHARACTERISTICS OF 60 GHz
DD READ GaAs IMPATTS

Doping Concentration (cm^{-3})	Output Power (W)	Efficiency (%)	Electric Field (10^5 V/cm)		Punch-Through Factor	
			At p^+p	At nn^+	p side	n side
$p_+ = 5.0X10^{16}$ $p_+ = 1.5X10^{17}$ $n^+ = 1.5X10^{16}$ $n = 4.5X10^{16}$	1.21	14.8	2.3	2.4	2.36	2.48
$p_+ = 5.0X10^{16}$ $p_+ = 2.0X10^{17}$ $n^+ = 2.0X10^{17}$ $n = 4.5X10^{16}$	1.28	15.8	2.15	2.3	2.29	2.33
$p_+ = 5.0X10^{16}$ $p_+ = 2.5X10^{17}$ $n^+ = 2.5X10^{16}$ $n = 4.5X10^{16}$	1.29	16.3	2.0	2.1	2.05	2.14
$p_+ = 5.0X10^{16}$ $p_+ = 3.0X10^{17}$ $n^+ = 3.0X10^{17}$ $n = 4.5X10^{16}$	1.17	15.4	1.85	1.95	1.90	1.90

0.86 μm (ℓ_p = 0.4 μm, ℓ_{n+} = 0.14 μm, ℓ_n = 0.32 μm) and that of the DD Read diodes is 0.8 μm (ℓ_p = 0.32 μm, ℓ_{p+} = 0.1 μm, ℓ_{n+} = 0.1 μm, ℓ_n = 0.32 μm), respectively. According to these data, the optimum RF performance was achieved from the diodes with the electric field between 1.5 and 2.5 x 10^5 V/cm at the $p^{++}p$ and nn^{++} interfaces. The corresponding punch-through factor was around 1.5 for flat profiles and 2.0 to 2.5 for Read profiles.

2.4 THERMAL CONSIDERATION

Careful attention to the thermal properties is critical in the development of high performance GaAs IMPATT diodes. When a maximum safe junction temperature, which determines the average lifetime of the device, is specified for the operating conditions of an IMPATT diode, the maximum RF power output attainable from the device is determined by the efficiency and the thermal resistance of the device according to the expression:

$$P = \frac{T_M - T_A}{\theta_T} \frac{\eta}{1 - \eta} \tag{34}$$

T_M is the specified maximum temperature, T_A is the ambient temperature, which for most applications is around 25° C, θ_T is the device thermal resistance, and η is the device efficiency which here is assumed constant for a given device. Therefore, maximum device output power is achieved by maximizing the diode efficiency and minimizing its thermal resistance, although it must be realized that the two parameters are not completely independent. It should be noted that the ouput power of an IMPATT can be increased by increasing its area up to some point because the thermal resistance decreases. But beyond that point the efficiency will drop because of difficulty in impedance matching and eventually the output power itself will decrease.

The thermal resistance of an IMPATT depends upon a number of factors, and each should be given consideration in the overall design of the IMPATT. These factors are: The device area and geometry, the type and quality of the metallization of the diode and its bonding to the heatsink, the heatsink material and its metallization, and the doping profile of the epitaxial material, particularly the thickness of the GaAs material between the junction

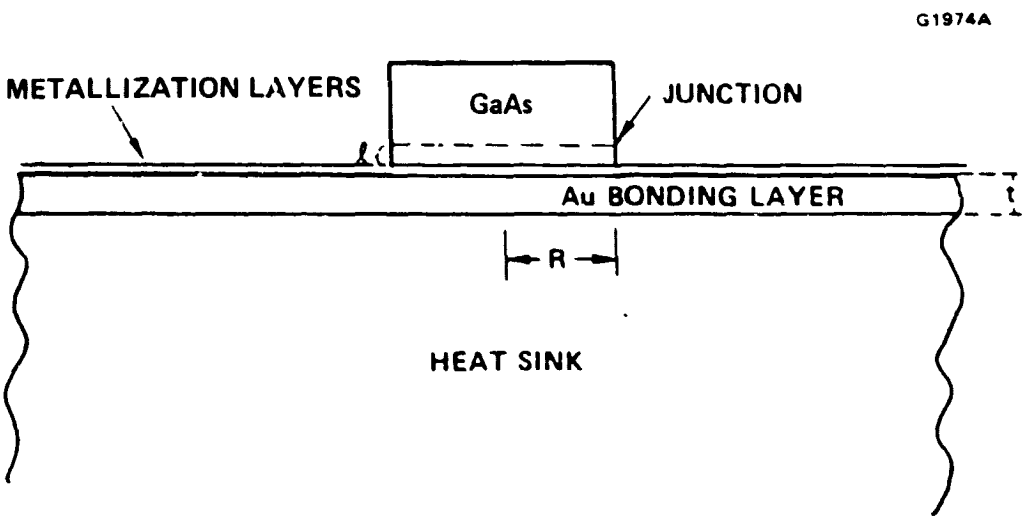
central plane and the metallized surface which lies against the heatsink. For CW devices this thickness is especially significant and should be kept to a minimum because GaAs is a relatively poor conductor of heat.

A calculation of the steady-state thermal resistance can be performed using a model shown in Figure 14. This model consists of a diode disc of radius R mounted on a two-layer heatsink consisting of a gold bonding layer followed by a semi-infinite heatsink. This disc geometry is the simplest and most commonly used one for IMPATTs. The semi-infinite heatsink consists of a layer of gold metallization which acts as a bonding layer. The total thermal resistance, θ_T, is the series combination of the contribution for the GaAs, θ_D, and the contribution due to two-layer heatsink, θ_{HS}. Since the thickness of the deposited metallization layers is small compared to the diode radius, the contribution of these layers on diode thermal resistance has been neglected. The electrical analog for the total thermal resistance is shown in Figure 14(b).

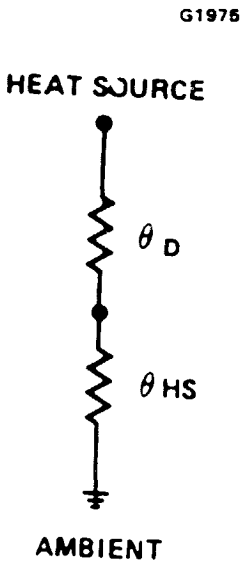
The generation of heat within the actual IMPATT is distributed throughout the junction of the GaAs material according to the joule heating term $\vec{E} \cdot \vec{J}$ where $\vec{E}$ is the local electric field and $\vec{J}$ is the local current density. However, in this model the heat source is confined to a disc of zero thickness located at the junction center in order to simplify the analysis. Also, this heat source is taken as one of uniform downward heat flux. In the actual case, because the temperature profile is radially dependent, the nonuniform temperature distribution within the junction brings about a nonuniform current density distribution. These nonuniformities in junction temperature and current density result in nonuniform heat flux. These effects have been included in published analyses of heat flow in IMPATT diodes.[18,19] However, these effects are small and are neglected in the present analysis. With this assumption, a solution of a one-dimensional linear heat flow equation in the GaAs leads simply to:

$$\theta_D = \ell / k_D A \tag{35}$$

where ℓ is the distance from the junction to the heatsink, A is the device area and k_D is the thermal conductivity of GaAs.



(a) Cross Section



(b) Electrical Analogue

Figure 14 Thermal model of IMPATT diode.

The solution for the thermal spreading resistance for a two-layer heatsink has been obtained where the thermal conductivity of the material in each layer is essentially independent of temperature.[20] The result is:

$$\theta_{HS} = \frac{1}{\pi R k_1} \int_0^\infty \frac{1 + pe^{-2UH}}{1 - pe^{-2UH}} J_1(U) \frac{dU}{U} \qquad (36)$$

where $H = t/R$, R is the diode radius and t is the thickness of heatsink top layer, $p = (k_1 - k_2)/(k_1 + k_2)$, and where k_1 and k_2 are respectively, the thermal conductivities of the gold layer and of the semi-infinite heatsink which is generally either copper or diamond. The actual thermal conductivity of diamond has a significant inverse temperature dependence. However, a conservative estimate of thermal impedance can be obtained by assuming a constant conductivity of 9.0 watts/cm$^{\circ}$K.

The expression in equation (36) has been evaluated numerically and the addition of the thermal impedances of the GaAs and gold layers between the junction and the heatsink has been made for the thicknesses shown in Figure 4 which apply to the initial design of the 60 GHz IMPATT device. The layers of metallization on the IMPATT have been neglected because they are so thin. The results of this calculation are plotted in Figure 15 for the thermal resistance versus diode radius for copper, silver, and diamond heatsinks.

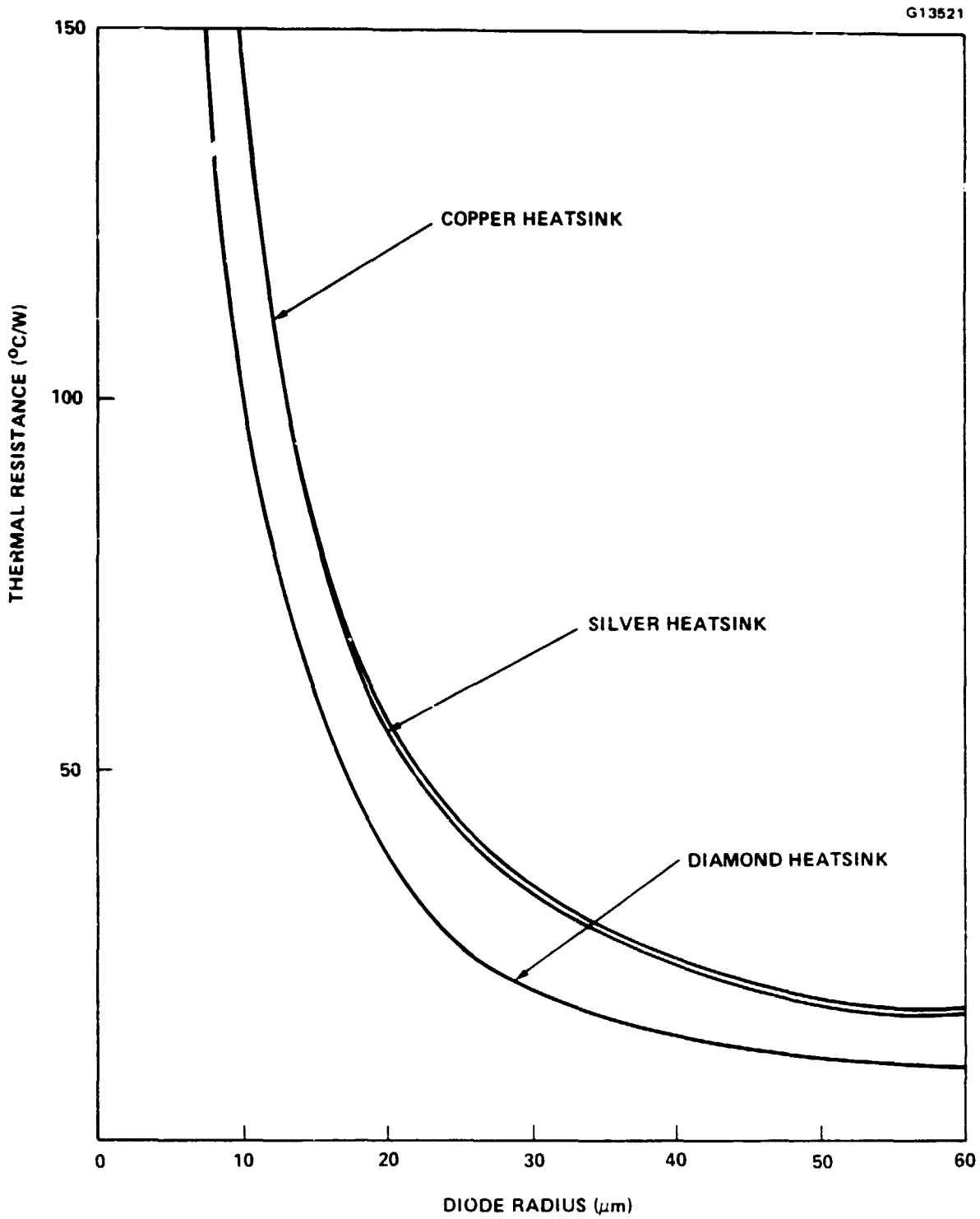


Figure 15 Thermal resistance versus radius of 60 GaAs IMPATTs with different heatsinks.

3.0 MATERIAL GROWTH AND EVALUATION

The design of 60 GHz GaAs IMPATTs requires complex doping profiles with extremely small dimensions. The performance of the IMPATT diodes depends on how well the profile parameters are controlled. Material growth of these doping configurations is a challenging task even with the most advanced equipment. We used molecular beam epitaxy (MBE) as the primary material growth approach, with vapor phase epitaxy (VPE) as a supplement.

Accurate material evaluation is as important as material growth in diode optimization. We routinely used the capacitance versus voltage (C-V) measurement on step-etched wafers for material evaluation. The secondary ion mass spectrometry (SIMS) analysis has also been utilized on selected wafers.

3.1 EPITAXIAL MATERIAL GROWTH

In the fabrication of high performance 60 GHz GaAs IMPATT diodes, precise doping profile control is essential. This imposes a stringent requirement in controlling the uniformity of doping concentration and layer thickness during the growth of the specific epitaxial layer structure. In order to meet this stringent material requirement, we selected MBE as the primary approach for the GaAs material growth. We have contacted three outside suppliers for MBE material growth; Perkin-Elmer (Physical Electronics Division), University of Southern California (MBE Laboratory) and Cornell University. Several MBE wafers were also grown at Hughes Research Laboratory (HRL) at Malibu, California. Although Hughes Microwave Products Division (MPD) in Torrance, California installed an MBE machine at the later stage of the program, no materials were grown for this program due to lengthy calibration required for the machine.

Because the MBE wafers were grown by outside suppliers, turnaround time for material growth was very slow. To overcome this limitation, GaAs materials also were grown using VPE at Hughes MPD.

3.1.1 Molecular Beam Epitaxial Growth

Molecular beam epitaxy provides the means for GaAs material growth, allowing excellent control over both the carrier concentration and the layer thickness. MBE material growth is performed in an ultra-high-vacuum environment, where the growth rate can be controlled accurately by regulating the temperature of the effusion cells. Also, the ultra-high-vacuum environment makes the MBE system ideal for the study of epitaxial growth and in-situ monitoring of film quality during growth, using such methods as quadrupole mass spectrometry, reflection electron diffraction, Auger electron spectrosocpy and secondary ion mass spectrometry.

Under an equilibirum condition, the beam flux from an effusion cell in an MBE system can be written as:

$$F = C\ P\ (MT)^{-1/2} \text{ molecule/cm-sec} \qquad (3?)$$

where

C = constant

P = equilibrium vapor pressure (Torr)

M = molecular weight of the vapor constituents

T = absolute temperature (^{o}K)

In actual film growth, the condensation of the vapor at the substrate is a function of the directivity of the source emission, the geometry factor determining the fraction of emission intercepted by the substrate and the condensation coefficient of the species. Oven temperatures must be carefully regulated if reproducible growth rates are to be obtained. Other important deposition parameters for achieving reproducible controlled growth are the substrate temperature, the vacuum quality, and the outgassing of the system hardware. Typically, the deposition rates of MBE range from 0.003 to 5 μm/hr for good quality film growth.

The MBE system at both Perkin-Elmer and USC is a Perkin-Elmer model. As shown schematically in Figure 16, this system consists of three chambers; a load chamber, an analytical chamber and a growth chamber, pumped respectively by a turbomolecular pump, a combination of ion pump - titanium sublimation pump with cryopanels, and a closed cycle helium cryopump. The analytical chamber and the growth chamber normally need not be exposed to atmospheric pressure when samples are introduced or removed. Base working pressures in these two chambers are better than 10^{-10} Torr. The substrate is held on a molybdenum block by a film of indium. The block, containing a substrate heater capable of reaching 900°C and a thermocouple, is mounted on the end of a support rod for insertion into the analytical and growth chambers. Eight boron nitride (BN) effusion crucibles (four 2 cc, four 20 cc capacities) are mounted inside individual resistive wound tantalum furnaces capable of reaching 1200°C. Each circuit is radiatively shielded and surrounded by a liquid nitrogen cryoshroud. The cells are arranged concentrically about a center line at an angle to the horizontal and pointing towards the substrate. The fluxes are controlled by pneumatically operated shutters, one for each cell. In the growth position, the sample is partly surrounded by a large liquid nitrogen cooled cryoshroud. A quadrupole mass spectrometer is positioned just above the sample, serving as a residual gas analyzer as well as a beam flux monitor. Below the sample, a nude ion gauge is installed as an absolute flux gauge. Here the flux from each cell can be measured individually both before and after growth. A high energy (10 kV) grazing incidence electron beam and phosphor screen complete the basic instrumentation in the growth chamber. The analytic chamber contains a scanning Auger microprobe and an argon ion gun for Auger depth profiling.

The proposed Cornell University system is a Varian Generation II MBE machine. This machine provides substrate rotation during growth for wafer uniformity. Both Hughes' machines are Riber systems. The HRL machine is a Riber 1000 MBE system and the MPD machine is a Riber 2300P MBE system. The Riber 2300P machine is a modular system which allows batch handling of up to ten 2-inch diameter wafers. The system has provision for substate rotation during growth.

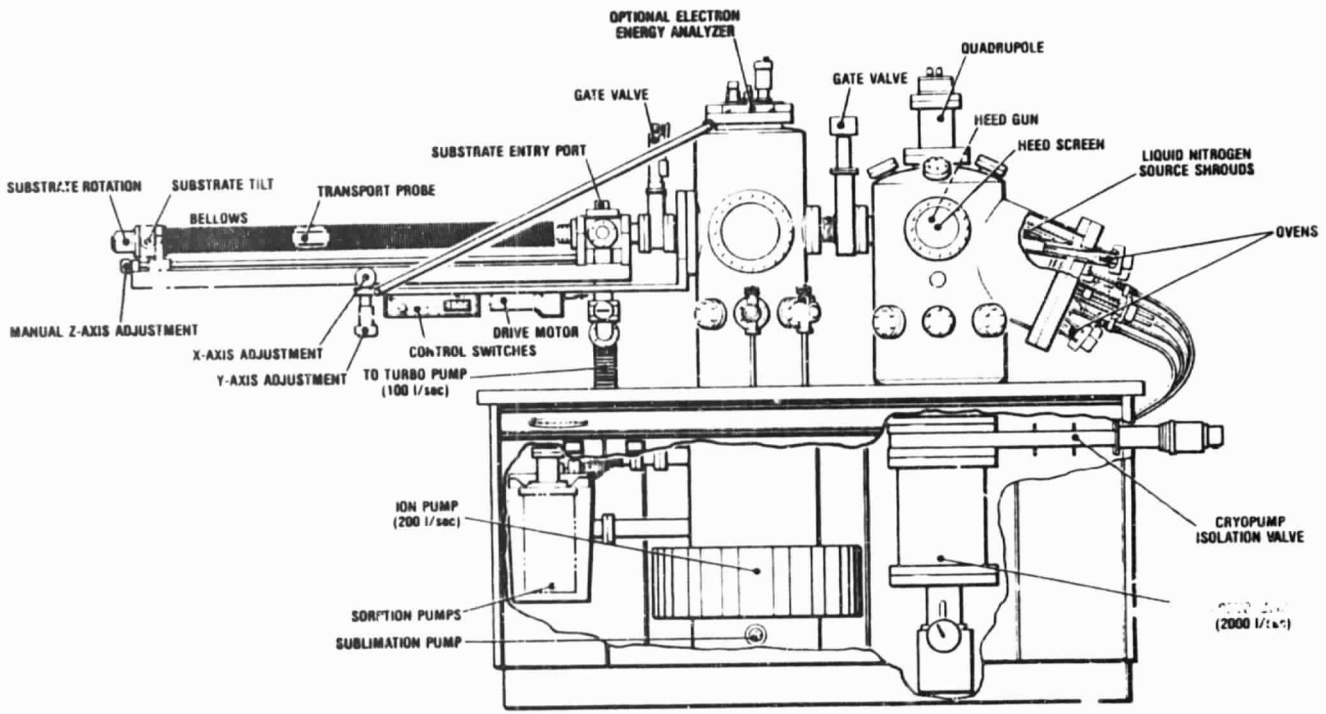


Figure 16 Schematic diagram of Perkins-Elmer MBE Model 400 system.

Perkin-Elmer has been the most consistent MBE wafer supplier for us. The doping profiles of Perkin-Elmer grown MBE wafers were reasonably close to the design values. Yet, only a few iterations of material growth were made during the course of the program, partly due to reactor modifications, installation of a new machine and some personnel reorganization at Perkin-Elmer. The old MBE reactor was modified to grow wafers as large as three inches in diameter. However, all of the materia were grown on 1.5-inch substrates.

The epitaxial layers were grown on [100] n^+ GaAs substrates doped with Si at $\sim 2 \times 10^{18}$ cm^{-3}. After cleaning, the substrates were mounted with indium on molybdenum sample holders and outgassed at 400°C for one hour in the MBE systems analysis/preparation chamber.

In the MBE growth chamber, the surface oxides were desorbed thermally in an arsenic flux, and the epitaxial layers were grown at a substrate temperature of 600°C with a growth rate of 1 μm/hour. The double-drift structures were grown using Si and Be as the n- and p-type dopants, respectively. The dopant temperature and sputter changes were controlled automatically by a preprogrammed, microprocessor-based MBE oven controller. During growth, each substrate was rotated continuously at approximately 10 rpm. After growth, the substrate and mounting block were cooled at 250°C in an arsenic flux and then returned to the analysis/preparation chamber for further cooling to enable removal from the MBE system.

The first three batches of Perkin-Elmer MBE wafers consisted of five DD hybrid structures with flat p and hi-lo n profiles. Then, five MBE wafers were grown according to the first design modification in May and fourteen wafers according to the second design modification in November 1983. The May wafers consisted of three DD flat and two DD hybrid (hi-lo) structures and the November wafers included three DD flat, eight DD hybrid, and three DD Read structures. Two of the DD hybrid structures had lo-hi-lo profiles while all other Read structures had hi-lo profiles. Seven more MBE wafers were grown at Perkin-Elmer in July 1984, based on the final design profiles. These wafers comprised two DD flat, three DD hybrid and two DD Read structures. All Read structures were hi-lo profiles.

Only a few MBE wafers were received from USC. Some of these were SD hi-lo Read and the others were DD flat structures. Except for several wafers, USC was unable to provide qualified GaAs MBE wafers due to continuing problems with the MBE reactor and personnel change. The contract with USC for the MBE wafer growth was discontinued after one year. A new contract was made with Cornell University, Electrical Engineering department to grow GaAs MBE material. After a long calibration period, they were able to provide six qualified wafers in late April 1984. Since that time no more MBE wafers have been grown at Cornell University. Availability of the MBE machine at HRL also has been limited because of commitment of the machine to other projects. Attempts were made to grow some materials whenever the machine was available, and several SD hi-lo and DD flat structures were grown at HRL. Hughes MPD installed a Riber 2300 P MBE system in late 1983. However, because of lengthy, time-consuming check-up and calibration procedures for the machine, no materials were grown for this program.

3.1.2 Vapor Phase Epitaxial Growth

To supplement the MBE wafers grown by outside suppliers, GaAs wafers were also grown in house using VPE. The VPE method has been used at Hughes MPD for growing epitaxial GaAs material for microwave and millimeter-wave IMPATT fabrication. This system produces high quality epitaxial layers, ranging in thickness from 0.2 to 20 μm and dopant concentrations from 10^{14} to 10^{18} cm^{-3} for n-type epilayers and 10^{15} to 10^{18} cm^{-3} for p-type epilayers. One of the VPE reactors is capable of in-situ growth of n-type and p-type epitaxial layers.

Figure 17 illustrates a schematic diagram of our VPE system. Hydrogen gas and $AsCl_3$ vapor are introduced into the reactor tube from the upstream side of the Ga source boat which is held at 850°C. As the gas mixture passes over the Ga melt, the Ga source is being saturated with As to form GaAs crust. When the Ga melt is fully saturated (about 8 percent As at 850°C), additional $AsCl_3$ passing over the melt starts the following reactions:

$$4\ AsCl_3 + 6\ H_2 \xrightarrow{500^{\circ}C} 12\ HCl + As_4 \qquad (38)$$

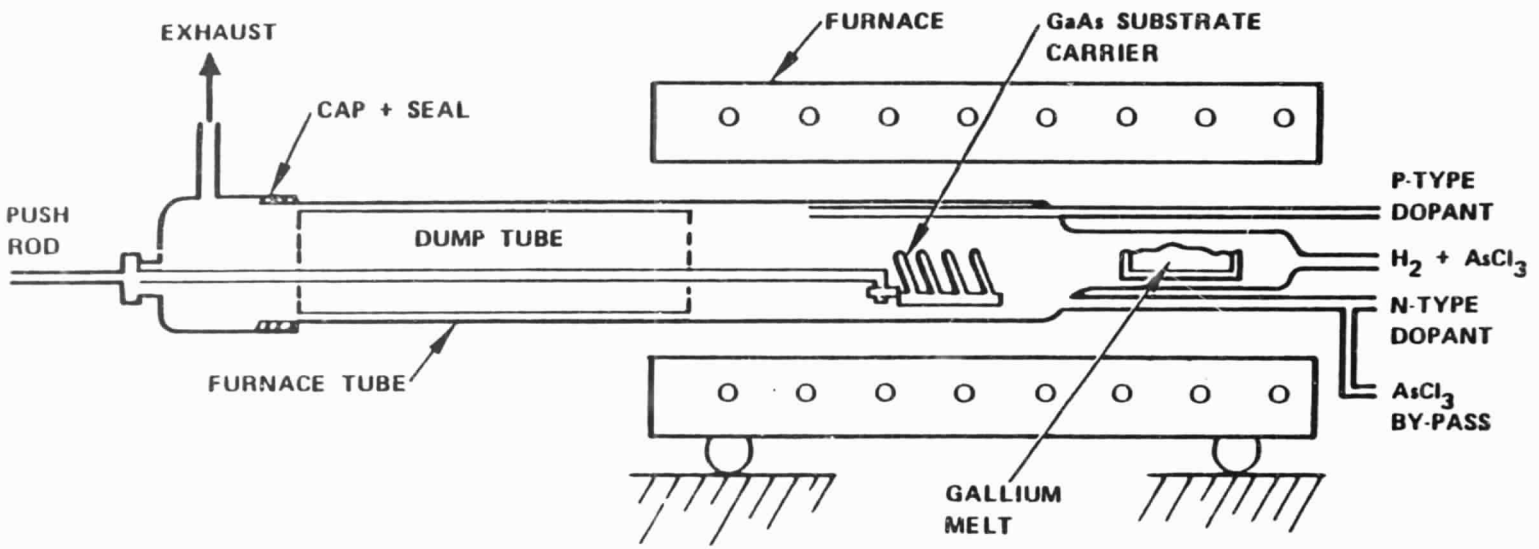


Figure 17 Schematic diagram of vapor phase epitaxy system.

$$12\ HCl + 12\ GaAs \xrightarrow{350^{\circ}C} 12\ GaCl + 6\ H_2 + 3\ As_4 \qquad (39)$$

This vapor, consisting of GaCl and As_4, proceeds to the deposition zone which is held between 730° to 760°C. Epitaxial layers of GaAs are then deposited on the substrate through the disproportionation reaction:

$$6\ GaCl + As_4 \xrightarrow{740^{\circ}C} 4\ GaAs + 2\ GaCl_3 \qquad (40)$$

These reactions are dependent on the $AsCl_3$ mole ratio (moles $AsCl_3$/moles H_2). For normal operation, a mole ratio is kept between 10^{-3} and 10^{-2}. This mole ratio is controlled by introducing additional $AsCl_3$ vapor to the reactor tube at the downstream side of the Ga melt thus bypassing the Ga boat. This is shown in Figure 17 as the $AsCl_3$ bypass line. This line is also used to change the reactor condition from growth to etching by modifying the $AsCl_3$ mole ratio for in-situ etching.

Doping is introduced to the reactor tube at two different locations. The p-type dopant is injected further downstream from the n-type dopant to minimize cross contamination of the dopants. The GaAs substrate carrier is placed on the upstream side of the p-type doping line during the n-type epitaxial layer growth. At the completion of n-type layer growth, the operator moves the substrate holder by retracting the push rod to the downstream side of the p-type doping line for in-situ growth of p-type epitaxial layers.

A microprocessor based controller is coupled with solenoid valves and automatic mass flow controllers for all gas handling in our VPE system. Figure 18 is a photograph of the VPE reactor and control system. This arrangement allows us to preprogram the epitaxial growth conditions for the whole growth cycle and enables the VPE reactor to repeat exactly the same gas flow conditions from run to run.

The reactor is capable of growing both n-type, Si-doped and p-type, Cd-doped layers in situ. The n-type layers were grown on n^+ substrate prior to the p-type layers. P-doping is accomplished by passing hydrogen through dimethyl cadmium contained in a bubbler held at a constant temperature of 20°C. This

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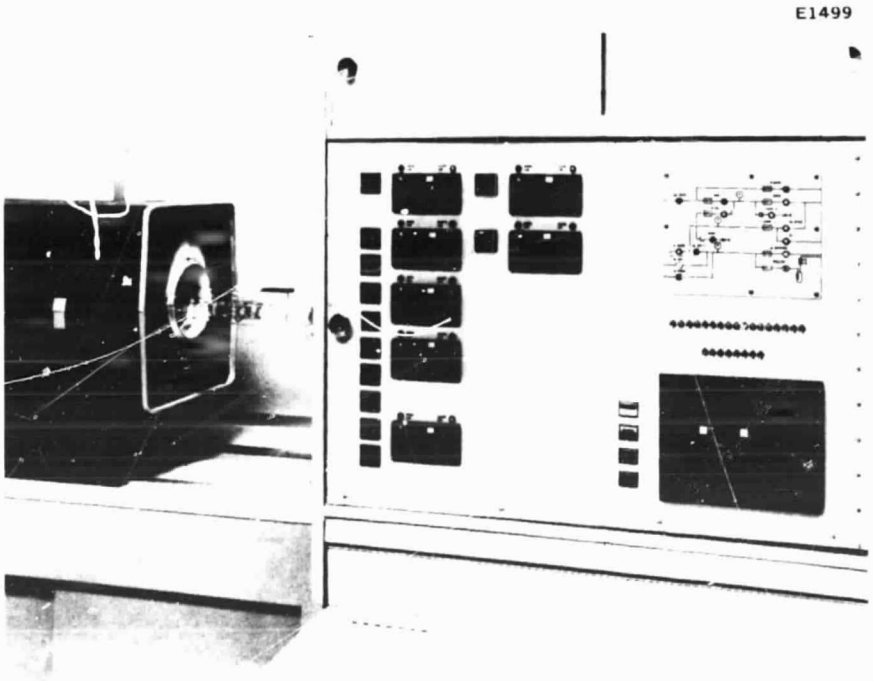

Figure 18 VPE reactor GaAs control system.

gas is further diluted with hydrogen in a mixing chamber and then metered into the reactor vapor stream. All flows are controlled by mass flow controllers. The doping densities are varied from run to run by varying the flows of the hydrogen dilution gas and final mixture entering the reactor. The only exception to this procedure is when the p^{++} contact layer is grown. In this instance the dilution gas is shut off and the flows through the bubbler and into the reactor are increased. We have been able to vary doping densities from 2×10^{15} cm^{-3} to 10^{17} cm^{-3} in p-type layers.

We had assigned a VPE reactor for this program. The growth rate of the reactor was initially about 0.2 μm/min. We started VPE material growth with the n-type SD flat structure. The target doping profile was same as that in the n-type portion of the DD flat structure to investigate the validity of our initial IMPATT design. Due to the scarcity of GaAs IMPATT data beyond 40 GHz and the uncertainty of material parameters at high temperatures and at high electric fields, the initial design parameters might be different from the optimum values. Any information obtained from the SD structures could be utilized for DD IMPATT optimization.

Several n-type SD flat structures were grown using VPE. For thicker epitaxial layers than the design value, the extra thickness was removed by etching. The surface of these wafers was slightly hazy, and a large leakage current was observed in the initial evaluation.

Following the growth of flat structures, SD hi-lo structures were grown. Because of the relatively high growth rate of VPE, the transitions between layers were somewhat graded. A sharp transition between the substrate and the epitaxial layer was achieved by etching back the buffer layer before growing the low-density n layer. However, a hump was observed close to the transition and was eliminated by introducing a purging step after etching the buffer layer.

Control of double-drift doping profiles was difficult in VPE growth. Nonuniformity in doping density within a layer also was observed, especially in the p-layer. The most prominent problem associated with VPE growth appeared to be the poorly defined p-n junction. The compensated region around the p-n junction was

estimated to be 0.2 to 0.3 μm in thickness, too wide for 60 GHz GaAs IMPATTs. The p-n junction area of the DD structures could not be evaluated accurately by C-V measurement because of the built-in depletion width. The p-dopant (Cd) of our VPE wafers could not be evaluated by SIMS analysis, because the background level of Cd was comparable to profile doping concentration. The problem associated with the poorly defined p-n junction appeared more acute with DD hybrid structures, which require a narrow, high-concentration n-layer at the p-n junction.

The many parameters which can affect the sharpness of the p-n junction interface include: (1) the flow pattern of the gases in the reactor; (2) the technique of dopant gas introduction into the reactor; and (3) the procedure of switching from n-type to p-type epitaxial layer growth. Modifying the flow pattern of the gas in the VPE reactor or changing the technique of dopant gas introduction into the reactor requires costly, time-consuming major modifications of the design and construction of the VPE reactor system, which is beyond the scope of this program. Therefore, we decided to improve the p-n junction sharpness by modifying the procedure of switching between n- and p-type layer growth.

We made a series of epitaxial growth runs to form a p-n junction. While the doping levels of the n- and p-layer remained constant, we experimented with various procedures for switching the dopant gases, e.g.: (1) we continued n-dopant gas flow after the completion of n-layer growth; (2) we introduced p-dopant gas before the n-dopant gas was turned off; (3) we introduced p-dopant gas before p-type layer growth started, etc. No significant improvement in the p-n junction transition was observed from these dopant purging steps, compared to the standard growth procedure of switching directly from n- to p-type dopant gases. We concluded that it is impractical to sharpen the p-n junction by changing the growth procedure using our existing VPE reactor.

We tried to fabricate DD flat structures by implanting p-dopant on the VPE-grown n-type wafers. First, the n-layer was grown on the n^{++} substrate for the specified doping specification and was followed by an undoped epitaxial

layer. Beryllium ions were then implanted on this undoped layer to form the p-drift region. After implantation, these wafers were annealed at 800°C for 30 minutes.

Our effort to fabricate DD IMPATTs by an epitaxial growth and ion implantation combination achieved limited success. To obtain a well defined p-n junction, thickness control and evaluation of the undoped and implanted layer must be precise, because the n- and p-layer doping concentrations of the DD flat diodes are about the same. This was a difficult task; we often encountered either undoped or compensated regions near the p-n junction.

We conducted a similar experiment to obtain a sharp buffer/n-layer interface. We achieved the best transition by etching back the buffer layer and growing the n-layer without purge.

Based on above experiments, we concluded that the complex doping profiles of the 60 GHz GaAs IMPATT diodes taxed the limit of our present VPE reactor. The material growth using VPE was, therefore, discontinued around the end of the second year and emphasis has been placed on MBE growth.

3.2 MATERIAL EVALUATION

In the fabrication of high performance IMPATT diodes, the most important factor is the control of doping profiles and material quality of a specific diode structure. It is therefore of paramount importance that the epitaxial materials must be thoroughly evaluated prior to device fabrication. The key parameters to be evaluated are the thickness and doping concentration of each individual layer, uniformity across each layer, and the transitions between layers.

3.2.1 Capacitance Versus Voltage (C-V) Measurement

The capacitance per unit area at zero bias is a function of the background impurity concentration; as the reverse bias is increased, the depletion layer width increases while the capacitance decreases. The doping concentration

N(x), as a function of distance x from a junction or a Schottky barrier contact, can be expressed as follows:

$$N(x) = \frac{C^3}{q\varepsilon A^2} (dC/dV)^{-1} \tag{41}$$

and

$$C = \frac{\varepsilon A}{x} \tag{42}$$

where

- C = depletion layer capacitance
- q = electron charge
- ε = permittivity of the semiconductor material
- A = the diode junction area

An automatic profiler provides a direct plot of N versus x by slowly sweeping capacitance versus voltage.

For DD profile measurement, the resulting profile plot gives information on the effective doping density (N_{eff}) and an effective depletion width (x_{eff}).

$$\frac{1}{N_{eff}} = \frac{1}{N} + \frac{1}{P} \tag{43}$$

and

$$x_{eff} = x_n + x_p \tag{44}$$

where

- P = p-type doping concentration
- N = n-type doping concentration
- x_n = depletion width on the n-type side
- x_p = depletion width on the p-type side.

For measuring the doping profiles of a DD IMPATT diode, it is necessary to perform the C-V measurements on both mesa and Schottky barrier diodes on a precisely step-etched wafer. Because the avalanche breakdown voltage is a strong function of carrier concentration, the penetration depth to which the depletion layer can be extended into the epi layer is limited. The step-etch procedure extends the range of profiling to cover the total layer thickness. Although Schottky barrier diodes can be made on p-type GaAs, the information provided by the Schottky barrier data is erroneous near the p-n junction. This is because near the junction, the reverse-biased Schottky barrier diode is in series with a forward-biased p-n junction. Minority carriers are therefore injected into the junction, causing the diffusion capacitance to dominate the true capacitance measurement. Therefore, the Schottky barrier data can only be used to check the p-side reconstruction data. It cannot be used for direct profiling.

C-V measurement was routinely conducted for every wafer. A section of each wafer was precisely step-etched with different step thicknesses, and the mesa and Schottky barrier diodes were delineated on the surface. The mesa diodes were used to measure the effective doping concentration versus total depletion width, while Schottky barrier diodes were used to evaluate the n-side doping profile. By reconstructing the p-side profile using the known n-side profile, a composite profile of a DD structure can be obtained. The step-etching also was used, even for SD wafers to extend the range of profiling for the total layer thickness.

We have often observed poor surface morphology on early VPE wafers. This problem later disappeared while experimenting with modifications of growth process. Figure 19 illustrates the C-V profile of an SD hi-lo structure grown by VPE. This wafer, which is one of the better-looking VPE wafers, shows good uniformity in doping concentration with reasonably sharp transitions. However, it was very difficult to control the doping profile using VPE to the degree required for 60 GHz GaAs IMPATTs. Significant nonuniformity was also observed within a wafer.

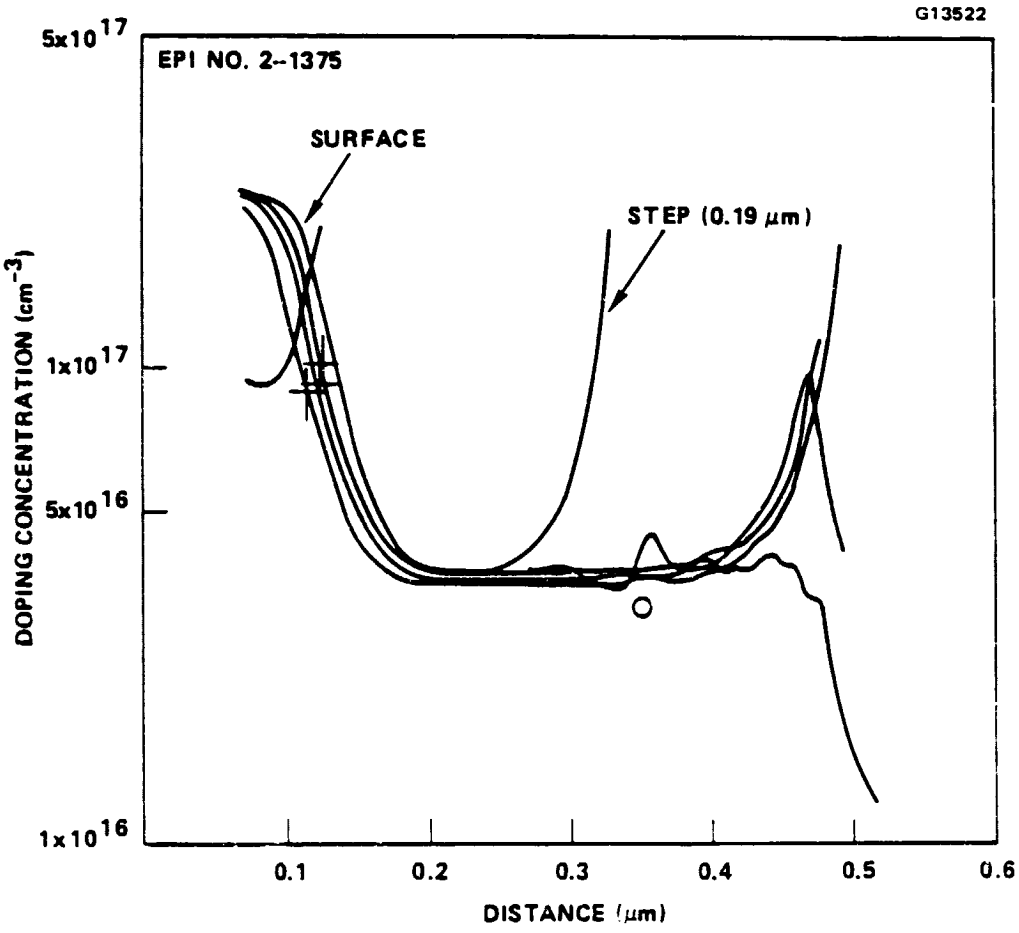

Figure 19 Doping profile of a VPE-grown single-drift hi-lo structure (with puring step).

Although MBE technology has a potential of precise doping control, the actual profile of many MBE wafers indicated deviation from the design profiles. Some of the USC and HRL-grown MBE wafers showed poor surface morphology, while most of the MBE wafers grown at Perkin-Elmer and Cornell University indicated good surface morphology. The doping profile of a USC-grown MBE wafer is shown in Figure 20. Each line indicates the doping profile of different diode chips within a wafer. A slight nonuniformity of the doping concentration within a wafer can be seen in this figure.

Figure 21 represents a composite profile of an MBE DD flat structure grown at Perkin-Elmer. Each discontinued line indicates the C-V profile data taken at the surface and each different step. A composite doping profile of a MBE DD hybrid structure is shown in Figure 22. A cluster of lines in the hi-lo region indicates the profile data obtained from different diode chips at the same step.

The C-V measurement has a limitation in providing accurate information near the junction. The actual doping profile within the depletion width cannot be evaluated. This problem becomes more acute for DD structures (especially for DD hybrid and DD Read profiles) which possess a p-n junction. Evaluation of nonuniform p-doping concentration of a DD structure is also difficult with the C-V profiling technique, since it measures the effective doping concentration.

3.2.2 The Secondary Ion Mass Spectrometry (SIMS) Analysis

In SIMS analysis, a section of the semiconductor wafer is mounted in a sample holder which is placed in the SIMS sample vacuum chamber. An incident ion beam of either cesium or oxygen impinges on the semiconductor target in a 20 x 20 mil square raster which bombards a square hole slowly and at a constant rate into the sample wafer. The secondary ions which are driven off from the central region of this square crater are analyzed by a computer controlled mass spectrometer system. This equipment can produce relative concentration profiles of the dopant elements, as well as of almost any other desired elements such as possible contaminants within the sample. Absolute doping concentration profiles can be obtained by calibrating the system with a sample

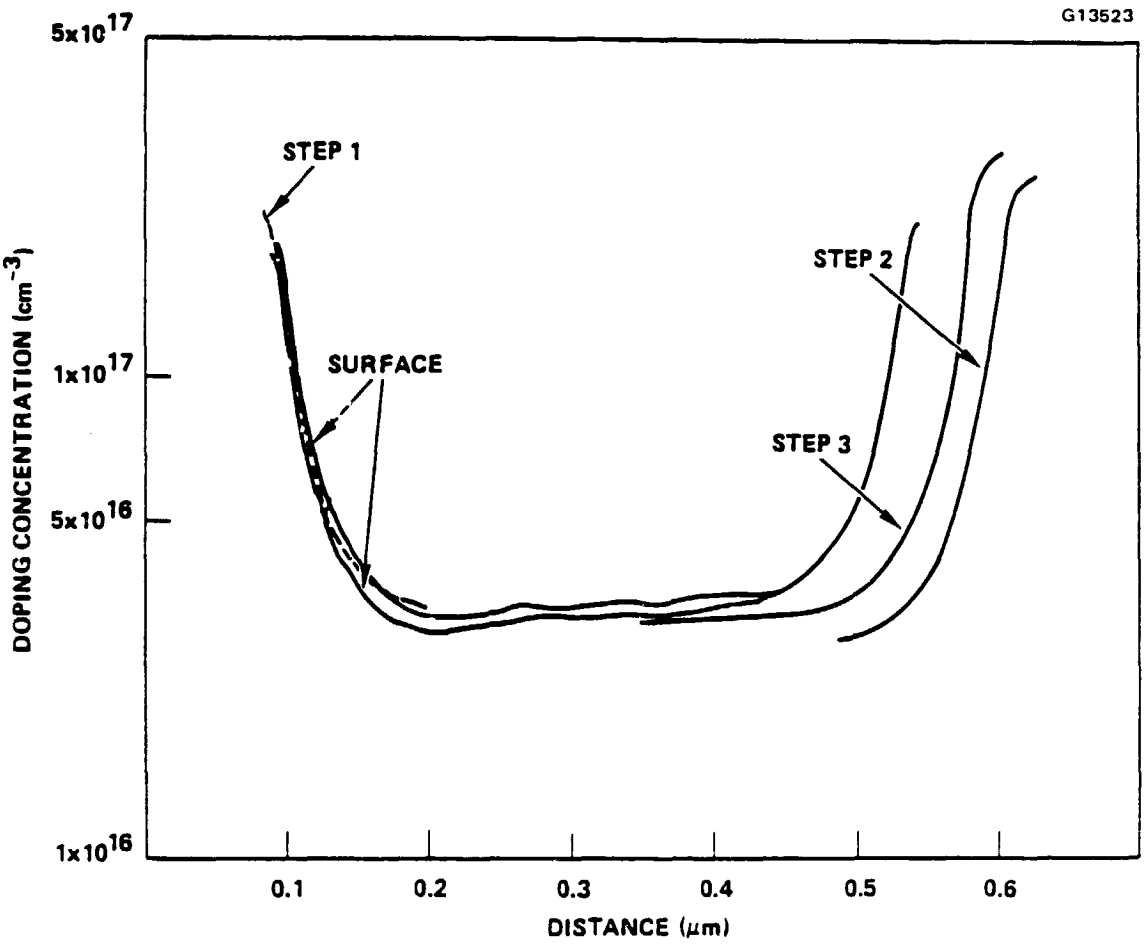

Figure 20 Doping profile of a MBE-grown single-drift hi-lo structure (USC).

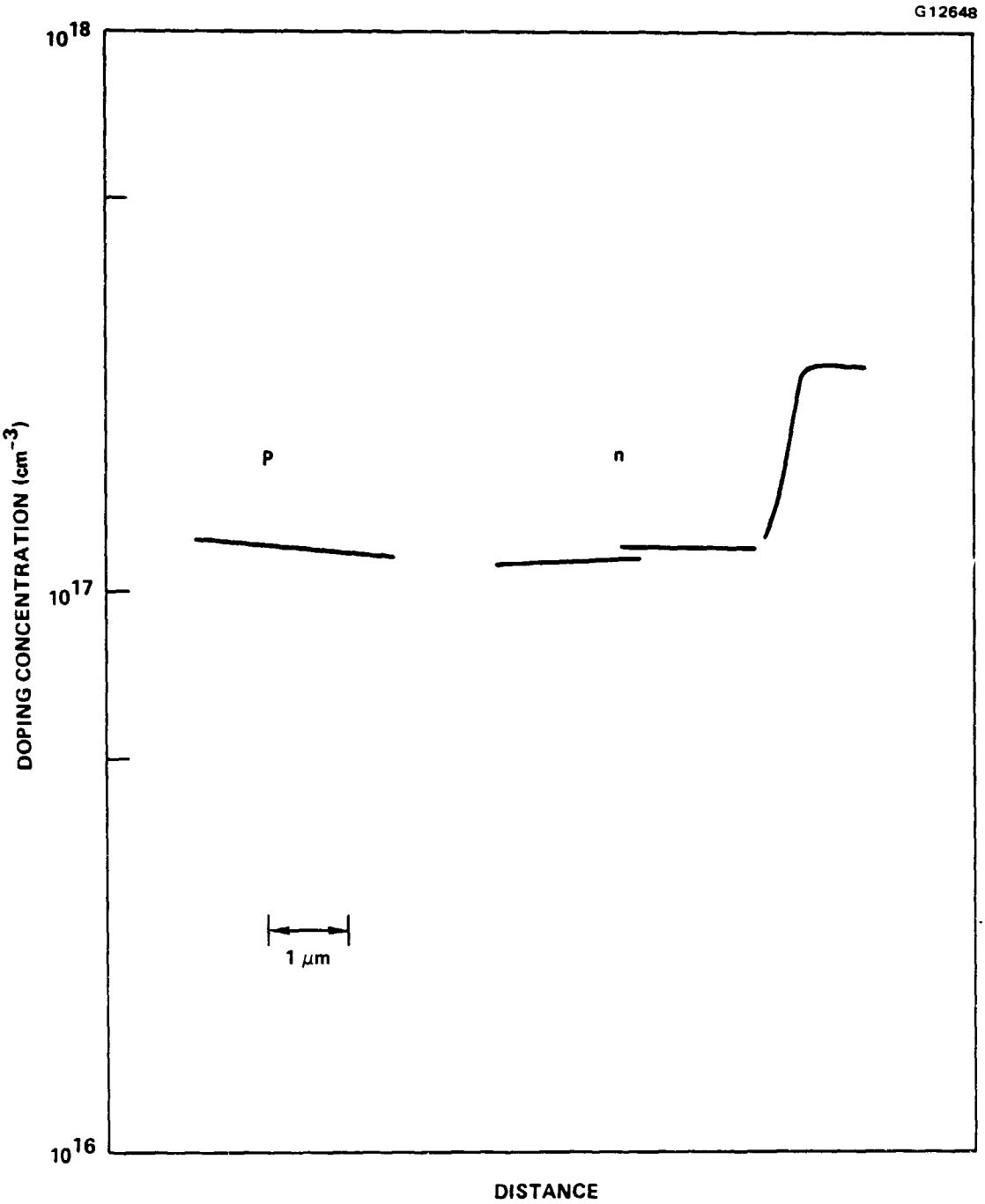

Figure 21 Composite doping profile of a MBE DD flat structure (Perkin-Elmer).

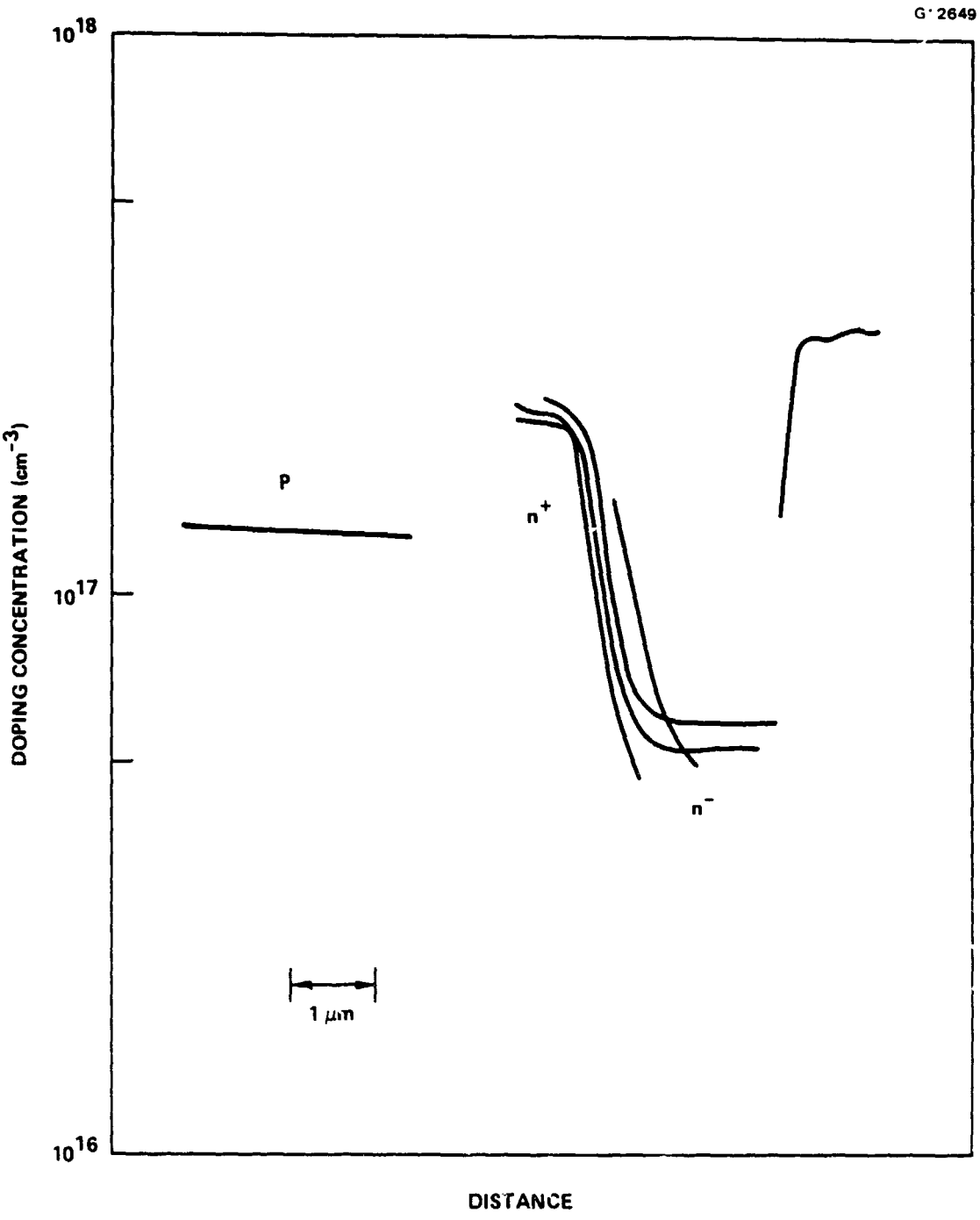

Figure 22 Composite doping profile of a MBE DD hybrid structure (Perkin-Elmer).

containing the desired element of known concentration. The absolute accuracy of the result then depends upon the accuracy to which the concentrations of the elements are known in the calibration sample.

SIMS analysis was conducted at Charles Evans & Associates, San Mateo, California. Beryllium and cadmium were monitored by a O_2/SIMS machine and silicon was monitored by a Cs/SIMS machine. The doping concentration was calibrated by using ion-implanted standards. This was done by setting the integrated counts under the implant curve equal to the implant fluence, after corrections were made for spurious surface and background counts. The uncertainty in the measure of the implanted species is estimated to be a factor of two. The depth scales were calibrated by measuring the depth of each analytical sputter-crater. The error in the depth scale is estimated to be about 10 percent. In Figures 23 and 24, the SIMS profiles of the MBE DD structures grown at Perkin Elmer are compared with the design profiles (represented by the dotted lines). The C-V profiles of the same structures were shown previously in Figures 21 and 22. Note that the SIMS profiles provide more detailed information than the C-V profiles. The doping concentrations evaluated by the two different methods show a slight discrepancy, probably because of the uncertainties associated with each evaluation technique. However, SIMS data indicate that the MBE wafers have excellent doping uniformity in each layer, with sharp transitions between layers.

SIMS profiles of a DD hybrid structure with a lo-hi-lo profile in n side and a DD Read structure with hi-lo profiles in both p and n sides are shown in Figures 25 and 26. An n^{++} spike between the GaAs substrate and the first epitaxial layer can be seen in these figures. This spike was also noticed on some other wafers grown at the same time. These spikes appeared real since they were observed in both cesium and oxygen analyses. The cause and possible effect on diode performance of these spikes were unknown. However, many diodes fabricated from these wafers indicated a poor breakdown characteristic and burned out at low bias levels.

The SIMS profile of a DD flat MBE sample grown at Cornell University is shown in Figure 27. For this particular wafer, the doping concentrations in active

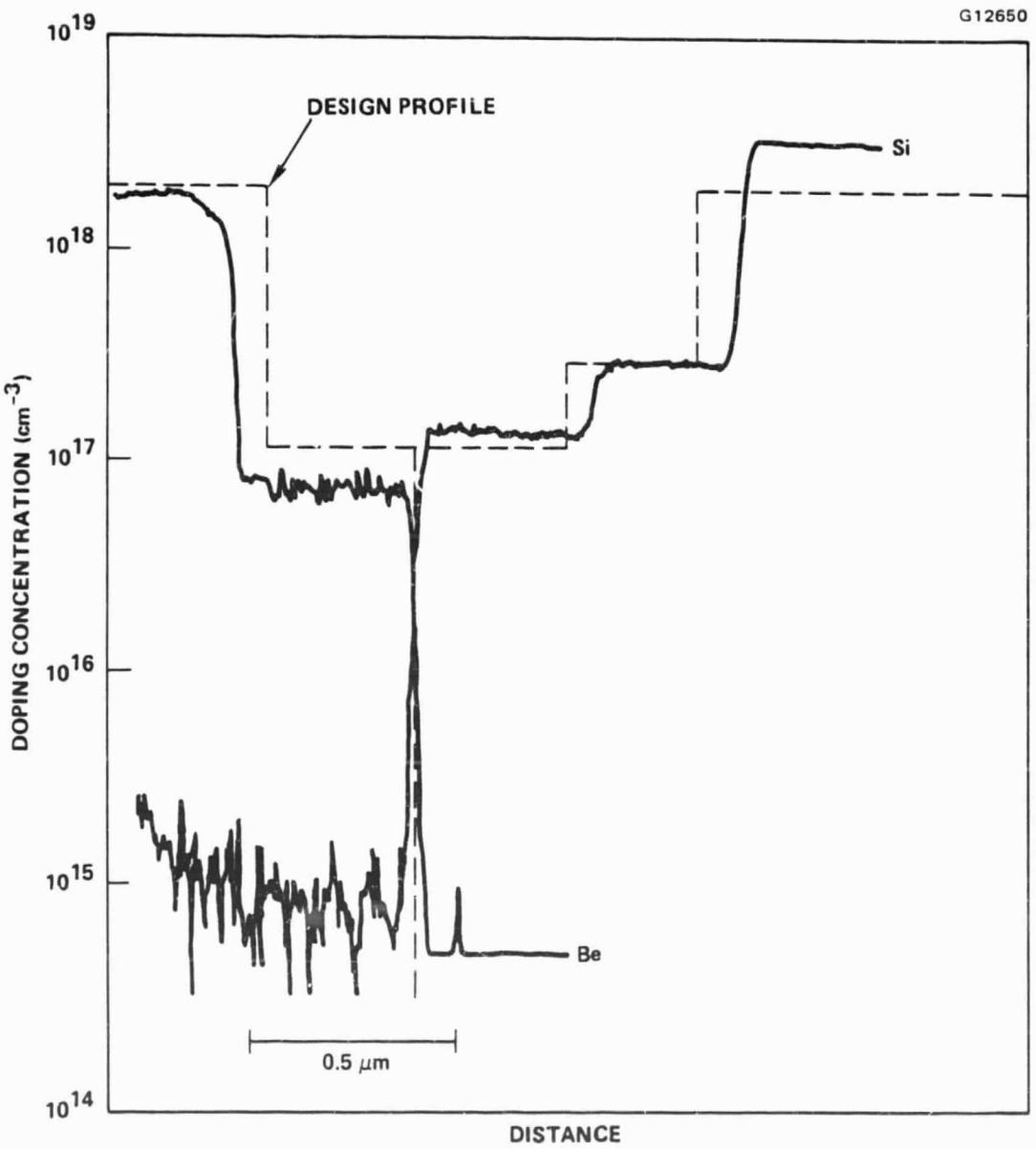

Figure 23 SIMS profile of a DD flat MBE wafer grown at Perkin-Elmer.

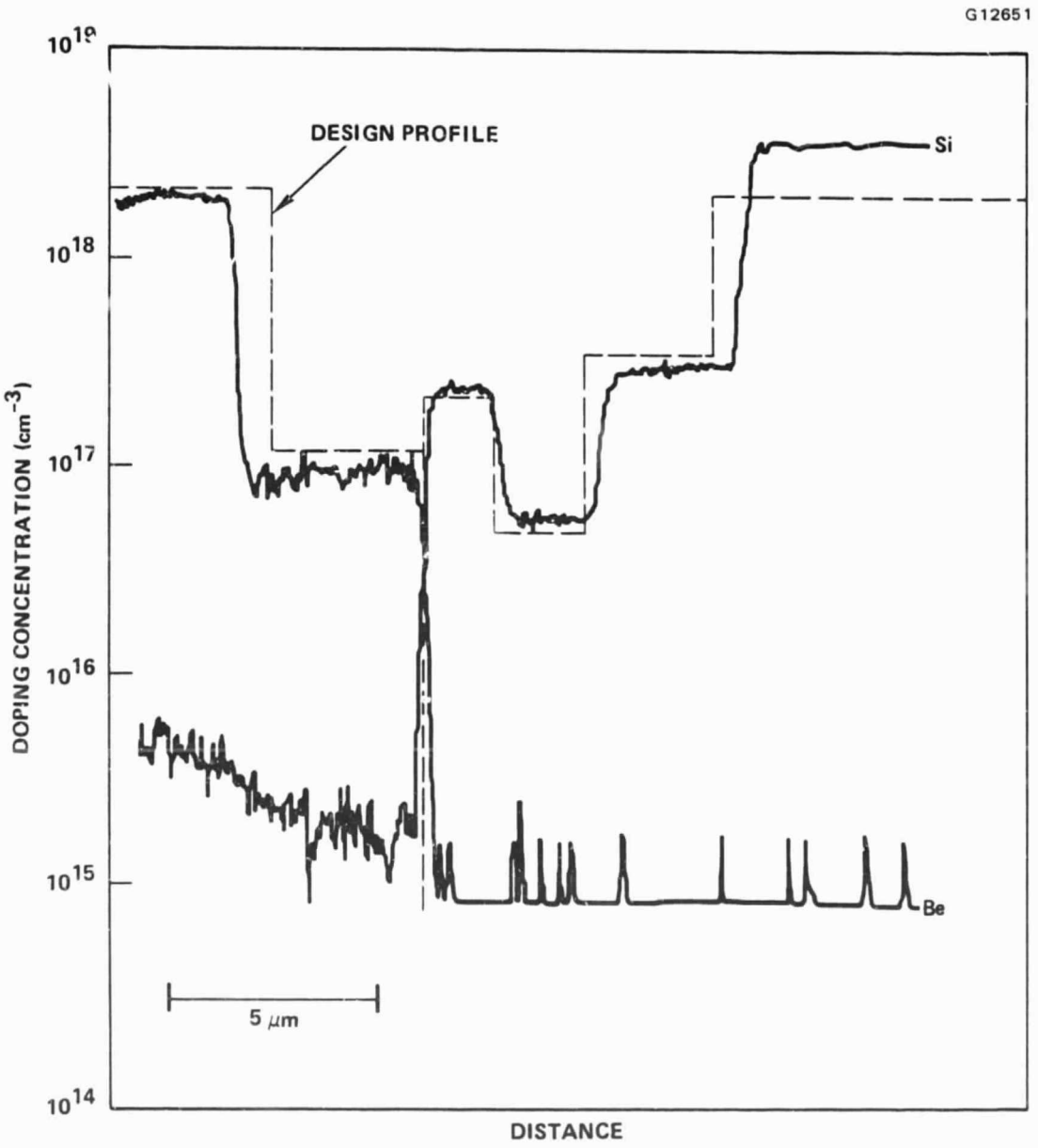

Figure 24 SIMS profile of a DD hybrid (hi-lo) MBE wafer grown at Perkin-Elmer.

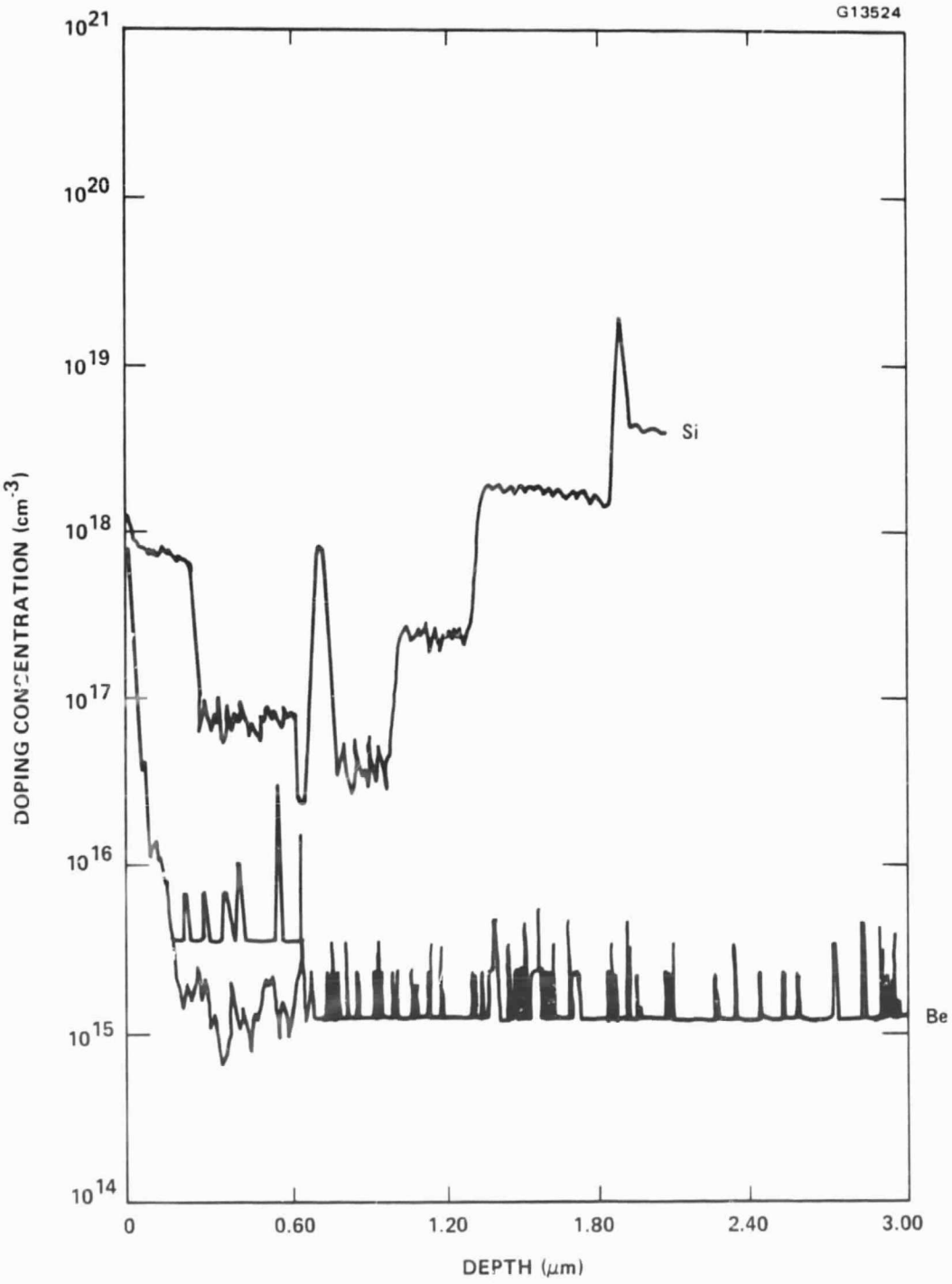

Figure 25 SIMS profile of a DD hybrid (lo-hi-lo) MBE wafer grown at Perkin-Elmer.

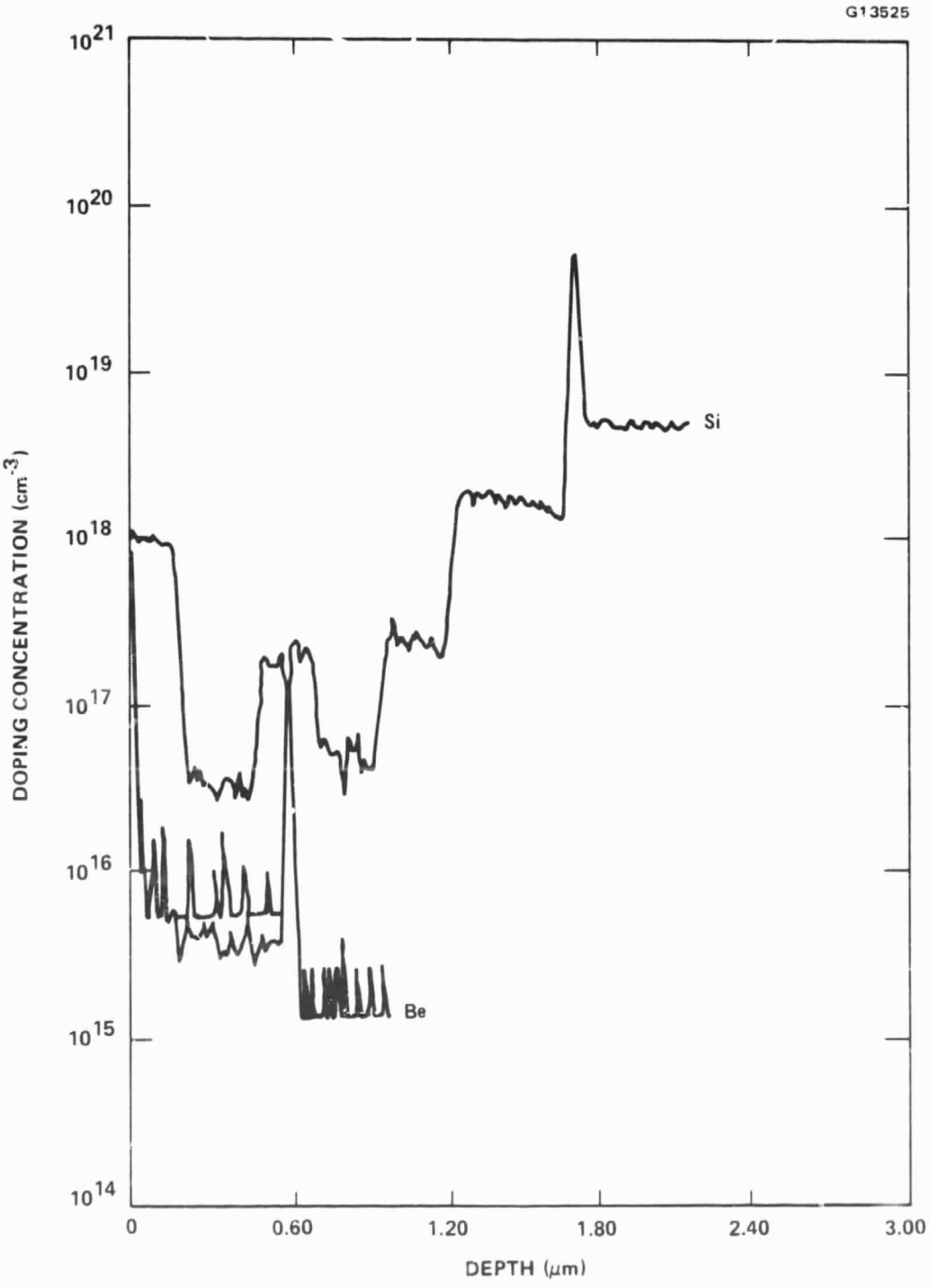

Figure 26 SIMS profile of a DD Read (hi-lo) MBE wafer grown at Perkin-Elmer.

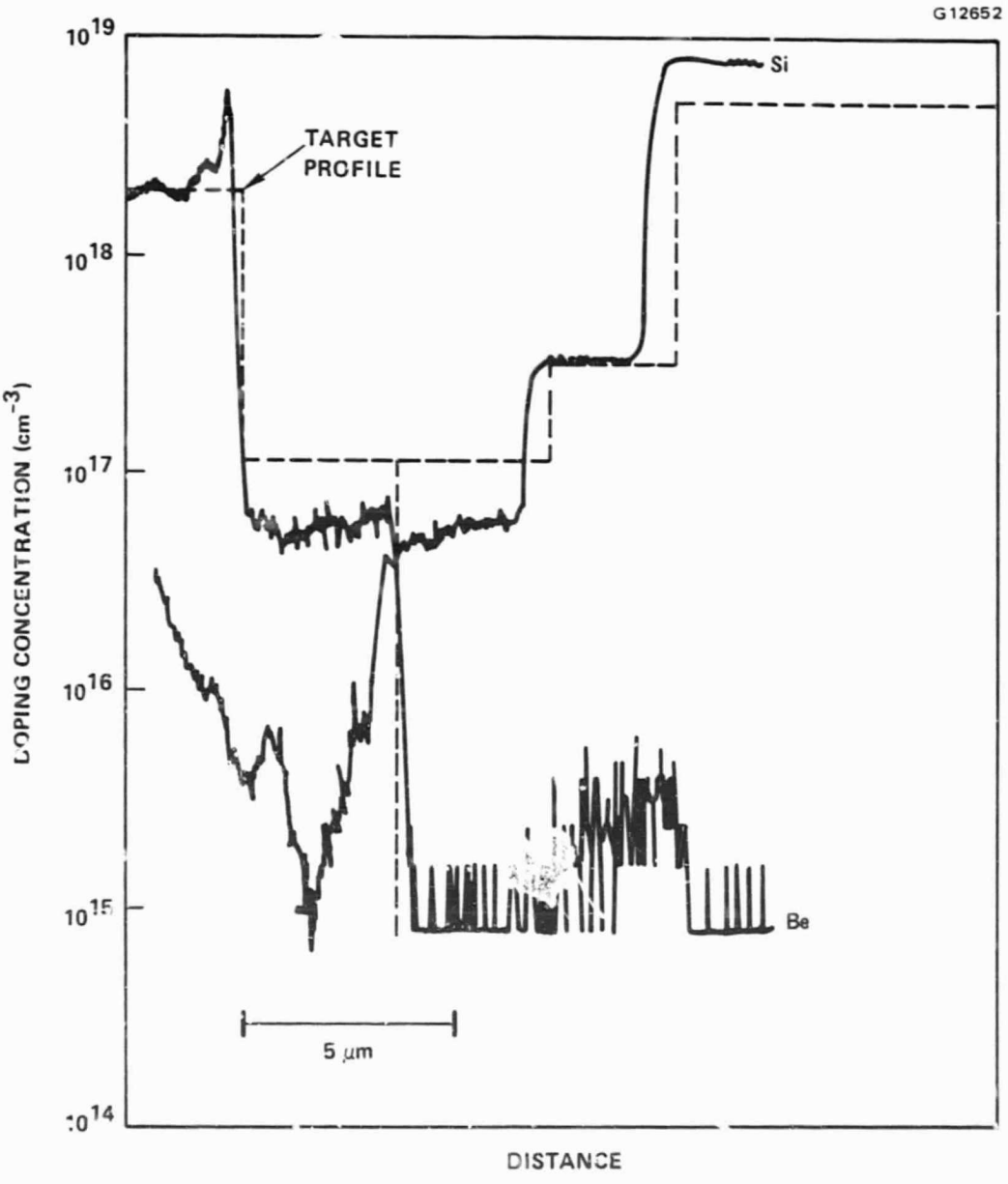

Figure 27 SIMS profile of a DD flat MBE sample grown at Cornell University.

layers are lower than target values. The high Si counts on the left-hand side appeared to be due to surface contamination of the wafer. A spike at the transition between p and p^{++} layers also was observed in other Cornell-grown samples. Figure 28 shows the n-side doping profile of a VPE wafer grown at Hughes MPD. The p-side profile of the Hughes VPE wafers could not be evaluated because the detection limit of cadmium, which was used as p-dopant, was as high as the accual doping concentrations. An n^{++} spike was observed at the transition between the substrate and first epitaxial layer in many Hughes-grown VPE wafers. The SIMS profile of an n-doped VPE wafer followed by p-implantation is shown in Figure 29. As expected, the implanted p-region indicates Gaussian distribution, resulting in a more graded p-n junction. Doping density uniformity and transition sharpness of the VPE wafers were not so good as those of MBE wafers.

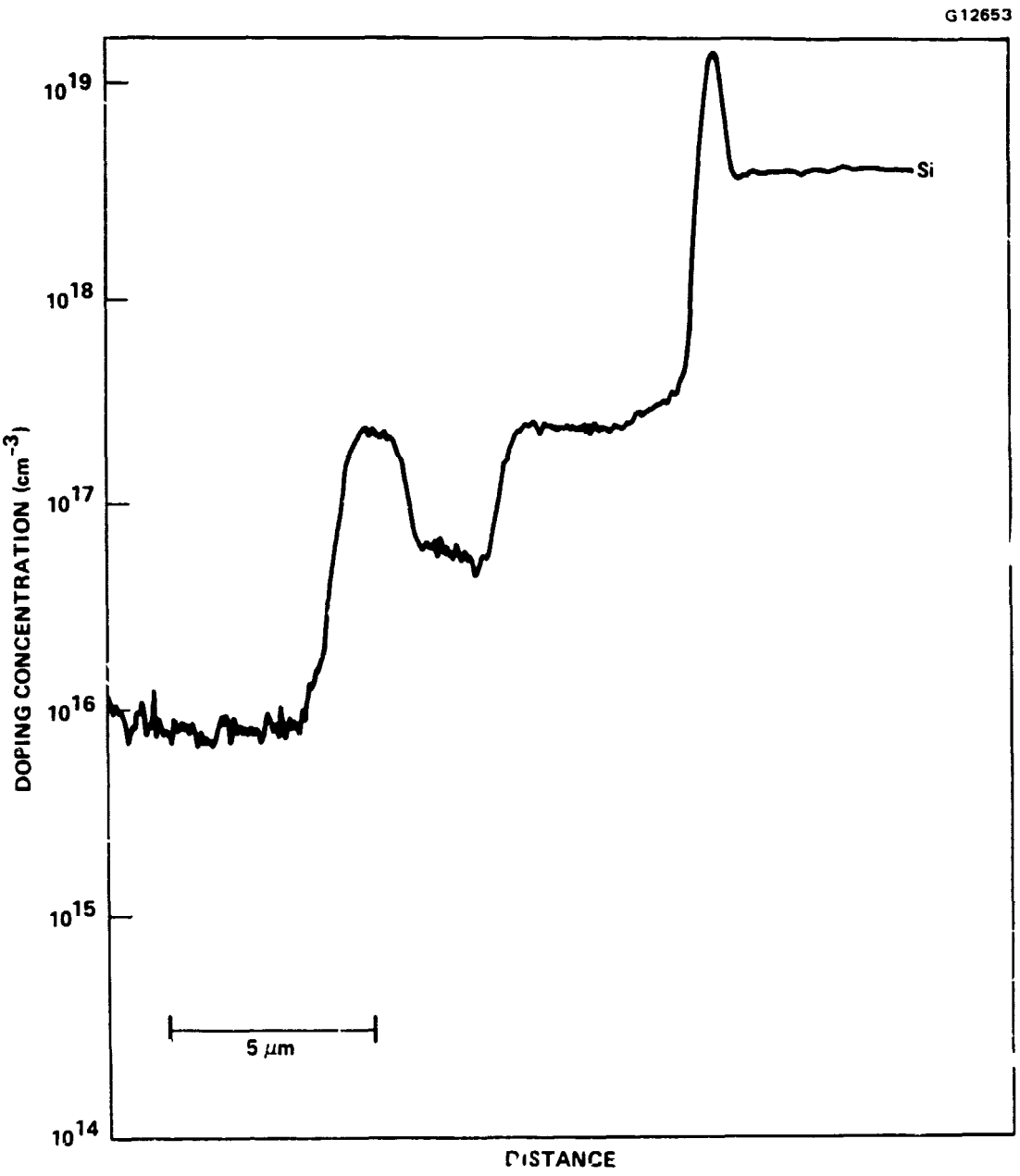

Figure 28 SIMS profile of Si(n)-doped layers of a VPE wafer grown at Hughes MPD.

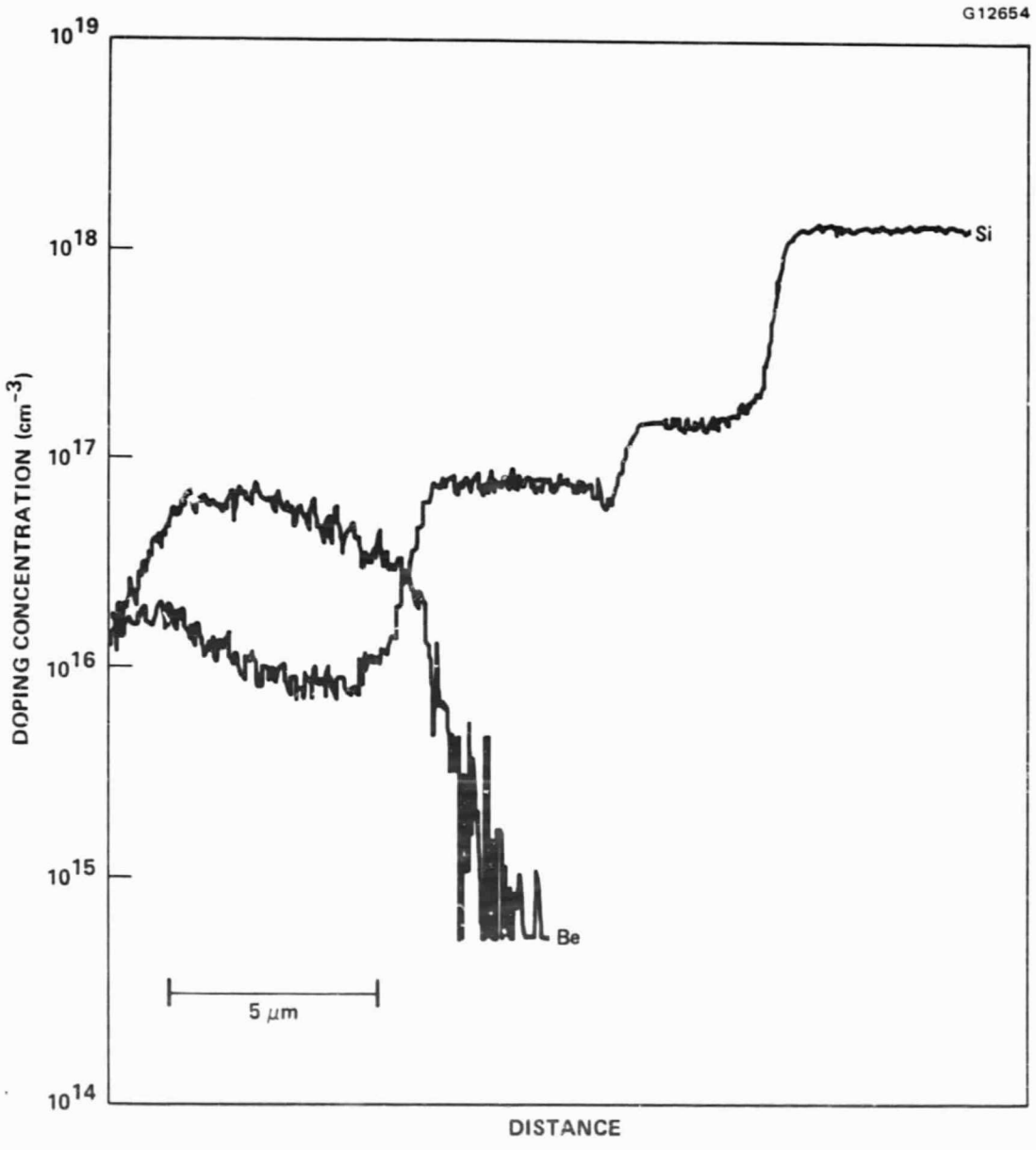

Figure 29 SIMS profile of a n-doped VPE wafer followed by p-implantation.

4.0 DIODE FABRICATION

During the course of the program, we have successfully fabricated pill-type diodes. By applying this technique, we were able to increase the number of available diode chips from a wafer by a factor of approximately ten. By thermocompression (TC)-bonding the pill diodes on diamond heatsinks, we reduced thermal resistance as much as 50 percent. Until the successful development of pill diode processing, the V-band GaAs IMPATT diodes had been fabricated in plated heatsink configuration.

The diode was mounted inside a miniature quartz-ring package. In most cases, a one-mil diameter gold wire was used for electrical connection in cross-strap configuratio .

4.1 WAFER PROCESSING

Many of the MBE wafers were small in size. The wafer size for diode fabrication was further reduced, since sections of the wafer were used for profile evaluation. Because of the large area required for a plated heatsink diode, the number of diode chips processed using this technique was often not enough for sufficient diode evaluation. Considering the difficulty encountered in attaining adequate uniformity within a wafer and repeatability among wafers, this problem imposed a serious limitation on diode optimization that was based on the evaluation data.

High frequency GaAs IMPATT diodes require a high level of current density which in turn requires small dimensional geometries; therefore, good thermal conduction is essential for optimum diode performance. The V-band GaAs IMPATTs clearly indicated a thermal limitation, with output power still increasing at the point of diode failure. Diamond is known to have the best heat conduction characteristic. Utilization of a diamond as a heatsink will, therefore, reduce thermal resistance and, consequently, improve diode performance. To overcome these limitations, we developed a processing technique for pill-diode fabrication. In this diode configuration, the plated heatsink was eliminated, increasing

the number of diode chips significantly. The diodes were then bonded directly to diamonds, thus reducing the thermal resistance.

The height of the GaAs mesa (i.e., the thickness of the wafer) must be minimized to reduce series resistance resulting from skin-effect loss for diodes operating at high frequencies. Thinner wafers also produce better defined mesa configuration with minimum area differential between a diode's top and bottom surfaces.

Hughes used a unique process procedure to control the mesa height of the finished diode. This was accomplished using a thickness control channel pattern to manipulate the wafer thickness (hence the GaAs mesa height) during the wafer thinning process. The process procedure is illustrated in the schematic drawing shown in Figure 30. Figure 30(a) shows that photoresist is used to define the control channel patterns. The GaAs material is etched away from those exposed channel patterns to the channel depth that is equal to the desired mesa height of the finished diode. The photoresist layer is then removed and a metallization layer is placed on the wafer, as shown in Figure 30(b). It is important to note that the bottoms of the channel patterns are covered with metal. The wafer is thinned from the substrate side and the etch action is stopped when the bottom of the control channel pattern is exposed, as shown in Figure 30(c). At this stage, the wafer thickness is equal to the desired mesa height of the finished IMPATT diodes. Using this processing technique, we reduced wafer thickness from about 15 mils down to 1.0 to 1.5 mils. Later, this thickness was further reduced to less than half a mil.

The quality of the metallization has a direct bearing on diode performance, failure and reliability. A proper metallization provides a minimum electrical contact resistance for the metal contacts to GaAs. These metal contacts should also have lower thermal resistance and must be stable for high diode reliability. We have used several different metallization systems on the epi side of the wafer. Ti-Au or Pt-Ti-Au metallization was used for Schottky contact on n-type SD structures. For SD structures with a p-n junction and DD structures, Ti-Au, Pt-Ti-Au, Pt-Ti-Pt-Au, or Au-Zn metallization was used. We controlled the p^{++} layer thickness somewhat using different metallization

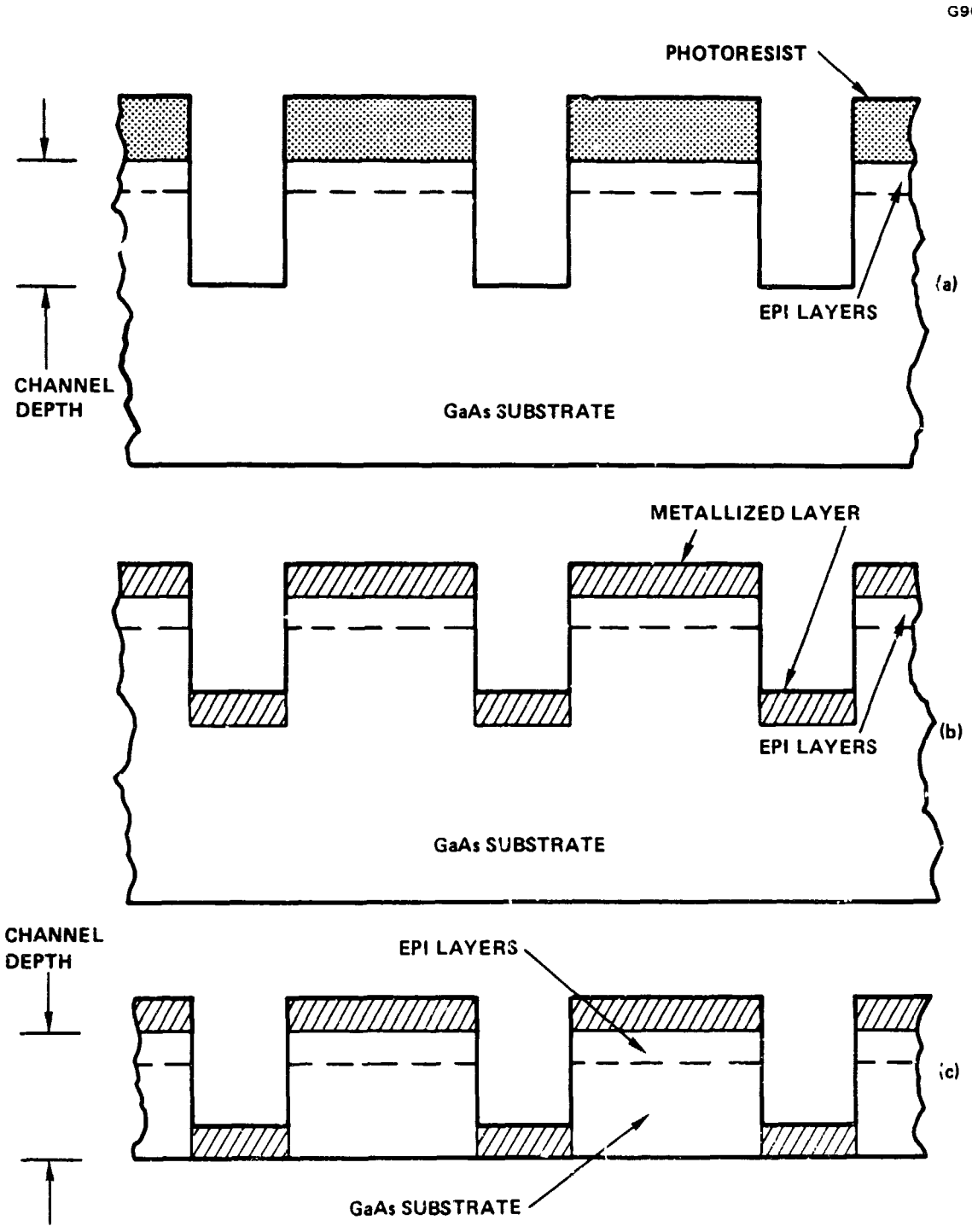

Figure 30 Schematic diagram of wafer thinning process.

systems. Ti-Au metallization forms a contact right at the surface, while Pt-Ti-Au penetrates 500 to 1000 Å. About 2000 Å extra thickness is required for Au-Zn metallization to account for the metal penetration into the wafer. For good ohmic contact, Ti-Au metallization requires high p^{++} concentration, while Au-Zn is not sensitive to p concentration. The Pt-Ti-Au metallization stands somewhere between these two metallizations. We used Ti-Au, Pt-Ti-Au or Au-Zn metallization for plated heatsink diodes and Pt-Ti-Pt-Au or Au-Zn metallization for pill diodes.

An Au-Ge-Ni metallization system has been used on the n substrate side of the wafer. Most Au-Ge-Ni based ohmic metallization systems require a subsequent 450°C alloying step to form a good lower resistance contact. At Hughes, we have applied a proprietary Au-Ge-Ni based ohmic contact metallization alloying step which requires only 350°C for one minute to form a low resistance contact. The lower alloying temperature subjects the wafer to less thermal shock during the ohmic contact alloying process. The reduced thermal shock to the wafer eliminates thermally induced damage found in a high temperature procedure.

4.1.1 Integrated Heatsink Diodes

The silver-plated heatsink technique is well established at Hughes and has been widely used for pulsed GaAs IMPATT diodes at microwave frequencies. Although the detailed processing procedure is slightly different for each metallization system on the epi side of the wafer, the general procedure for plated heatsink diodes can be outlined as follows:

1. Clean wafer. The cleaning procedure includes solvent clean plus diluted HCl and buffered HF etching to remove oxides from wafer surface.

2. Define metallized pattern on epi side.

3. Sinter metal contact (this step is omitted for Ti-Au metallization).

4. Etch channel grid from the epi surface into the substrate to define GaAs mesa height in final device configuration.

5. Electrical check: measure breakdown voltage (V_B) and diode capacitance as a function of voltage (C-V) to screen wafers for futher processing.

6. Sputter gold and then electroplate silver on epi side to form heatsink.

7. Thin wafer from substrate side by chemical etching until channels prepared in step 4 are exposed.

8. Evaporate Au-Ge-Ni based ohmic contact metal layers onto substrate side of wafer.

9. Electroplate gold over ohmic contact metallization.

10. Define photoresist dot patterns on gold metal surface by using photolithography.

11. Etch excess gold away outside the photoresist patterns defined in last step.

12. Etch the exposed GaAs surface to form a mesa under each photoresist dot pattern.

13. Strip photoresist; clean wafer.

14. Alloy Au-Ge-Ni ohmic contact.

15. Define photoresist circle patterns on the heatsink side of the wafer. These circle patterns are lined up with the mesa formation on the other side of the wafer.

16. Etch away excess metal layers outside the photoresist circle patterns defined in last step to separate the diode heatsinks.

17. Strip photoresist and solvent clean.

18. Sort diode chips.

4.1.2 Pill-Type Diodes

Pill diode fabrication is important for V-band GaAs IMPATT development to utilize the diamond heatsink and to increase available diode chips from a wafer. Our principal approach to pill diode fabrication was the modification of the established processing procedure for the plated heatsink diodes. We replaced the thick metal (silver) layer with a thin gold layer, and we fabricated mesa diodes using photolithography and chemical etching. We have experienced several problems associated with GaAs material in diode bonding to diamond. One hindrance was the brittleness of GaAs. Only a small amount of pressure could be applied to diode bonding to diamond without causing fractures. We needed a soft metal, such as pure gold, at the interface surfaces of the diode and diamond to secure a strong bond using minimal pressure. A small amount of impurities could harden the gold significantly. We relied on evaporation from a very pure source to produce the soft gold.

Another stumbling block was the required high temperature for metal alloying or sintering. For good ohmic contact, properly deposited gold must be alloyed or sintered to both p- and n-type GaAs. The high temperature caused the gold to harden, and it became difficult to bond. This hardening could be overcome by depositing soft gold over the contact after the alloy. This was performed readily on one surface of a wafer (p-side). The skin depth on GaAs at 60 GHz is about 15 μm, and diode thickness should be thinner. Since GaAs is brittle and cracks easily, we needed a thick metal backing for handling the GaAs during wafer thinning. This metal backing on the p-side inhibited deposition of fresh gold over this surface after thinning the wafer, alloying the ohmic contact, and depositing the soft gold on the other surface of the wafer.

We developed a process to overcome these limitations. After high-temperature sintering of Au-Zn metallization on the p-side surface of the wafer, tungsten was sputtered over the gold. To aid wafer handling, we plated a thick silver layer over the tungsten. The wafer was thinned, and we evaporated and alloyed ohmic contact metals on the n-substrate side of the diode. Next, pure gold was evaporated over the alloyed ohmic contact. The tungsten-gold interface is relatively inert at the second alloy temperature, and the underlying pure gold surface should not become excessively hardened. We etched circular diodes from the n-side. The silver backing metal and the tungsten layer were removed to expose gold. We subjected the gold to a cleanup etch in preparation for bonding.

The fabrication procedure for the pill structure is outlined below:

1. Clean wafer.

2. Deposit Au-Zn layers on epi side of the wafer and alloy.

3. Form pill thickness control channel patterns and etch to the specified depth. (Figure 31)

4. Sputter and evaporate gold.

5. Sputter tungsten and gold.

6. Plate silver.

7. Thin wafer from substrate side by chemical etching until channel patterns prepared in Step 3 appear. (Figure 31)

8. Evaporate Au-Ge-Ni-Au on substrate side of the wafer and alloy.

9. Sputter and evaporate gold.

10. Define dot patterns.

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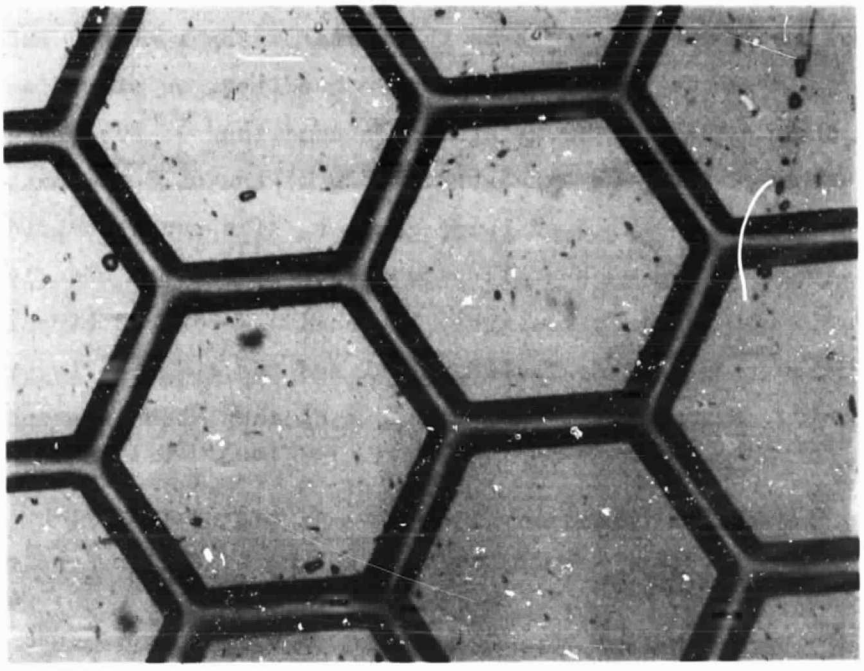
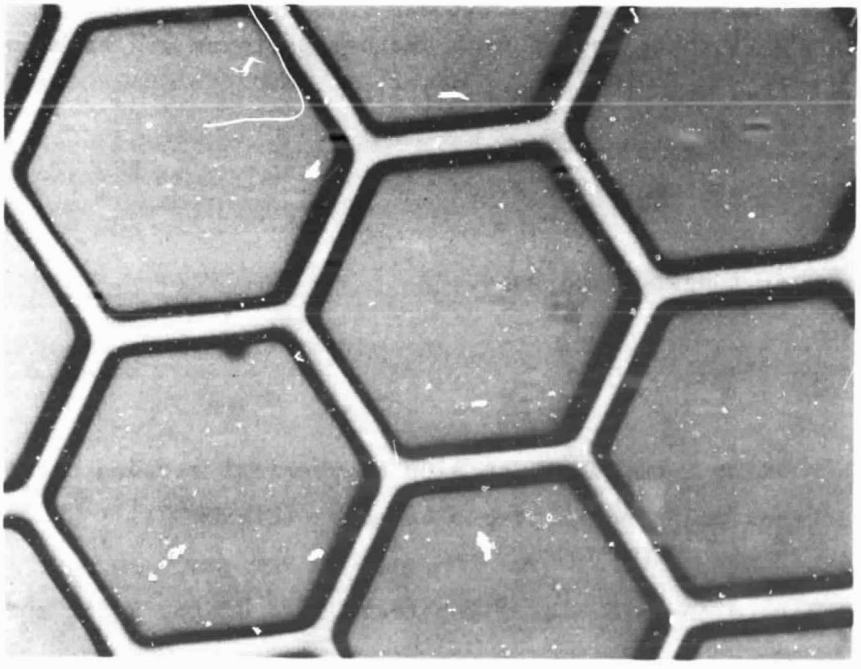


(a) FROM EPI SIDE (PILL DIODE PROCESS STEP 3)



(b) FROM SUBSTRATE SIDE (PILL DIODE PROCESS STEP 7)

Figure 31 Channel patterns.

11. Etch excess metal off.

12. Etch through the exposed GaAs to form mesa. (Figure 32)

13. Define another photo-resist pattern.

14. Etch metal layers to expose tungsten.

15. Mount the wafer in wax with silver side up.

16. Etch silver and tungsten layers.

17. Clean-up etch. (Figure 33)

18. Sort pill diode chips.

Figure 33 shows pill diode chips after the clean-up etch. The final pill configuration has a different diameter of gold on each side, making it possible to discern the top and bottom surfaces of the wafer.

At the early stages of pill diode development, we observed considerable cracking when the pills were TC-bonded to diamond heatsinks. We identified two possible causes for this cracking problem. The first was the relatively large area difference between the diode's top and bottom surfaces. We reduced this difference by minimizing the wafer thickness. The second possible cause was the plated gold we used initially. It might have been too hard to apply adequate pressure on brittle GaAs material. The plated gold was later replaced by evaporated gold to produce soft gold.

We sputtered a tungsten layer between the evaporated gold and thick plated silver introduced for wafer handling. The tungsten-silver interface would be relatively inert during the Au-Ge-Ni metal alloying on the substrate side, keeping the underlaying gold layer soft. However, tungsten formed ..ensive stresses in films when subjected to high temperature and caused the wafer to bow. On large wafers, this bowing caused cracking in the GaAs; thus, only a portion of the wafers has been processed in pill diode fabrication.

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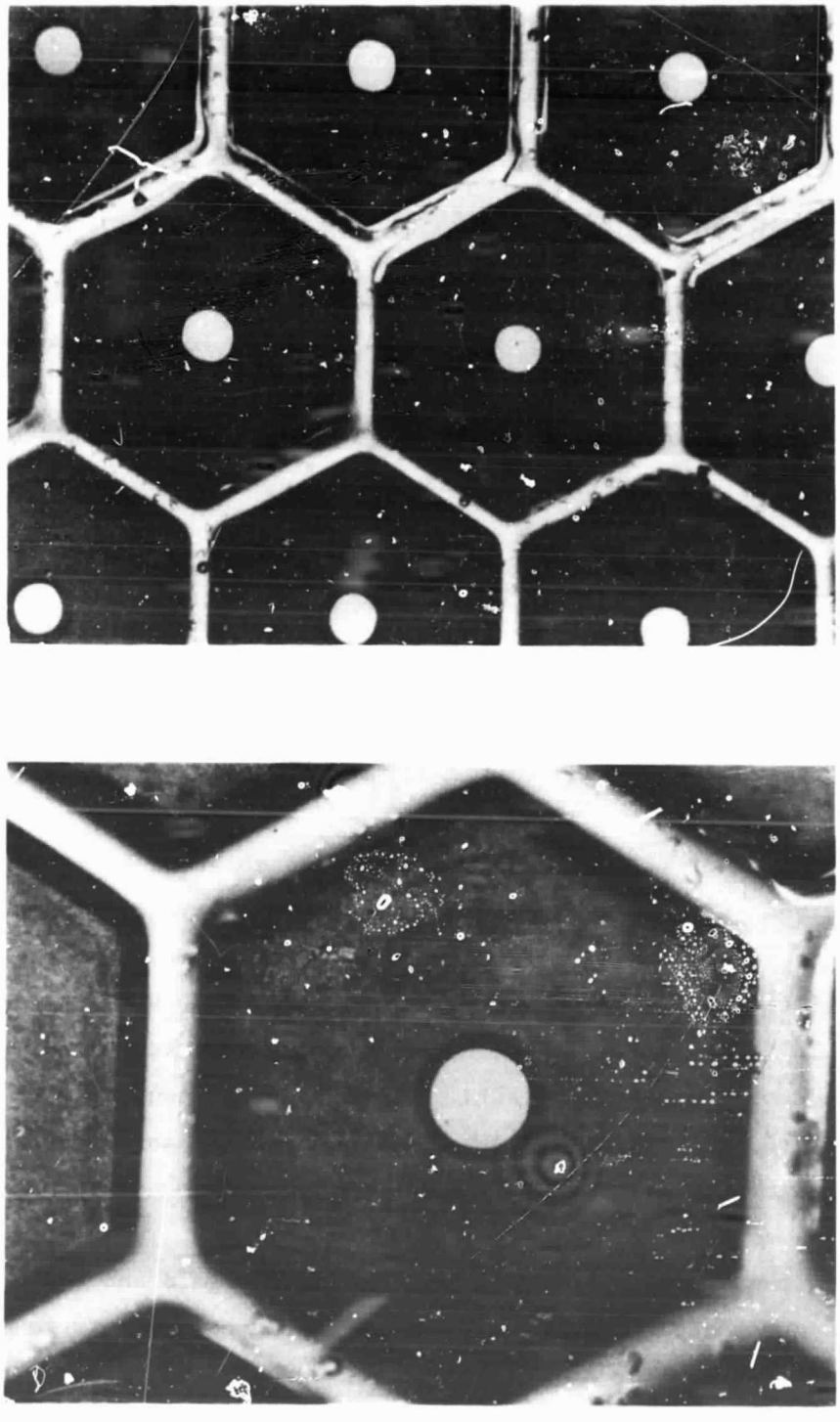

Figure 32 Diode and channel patterns after mesa etch.

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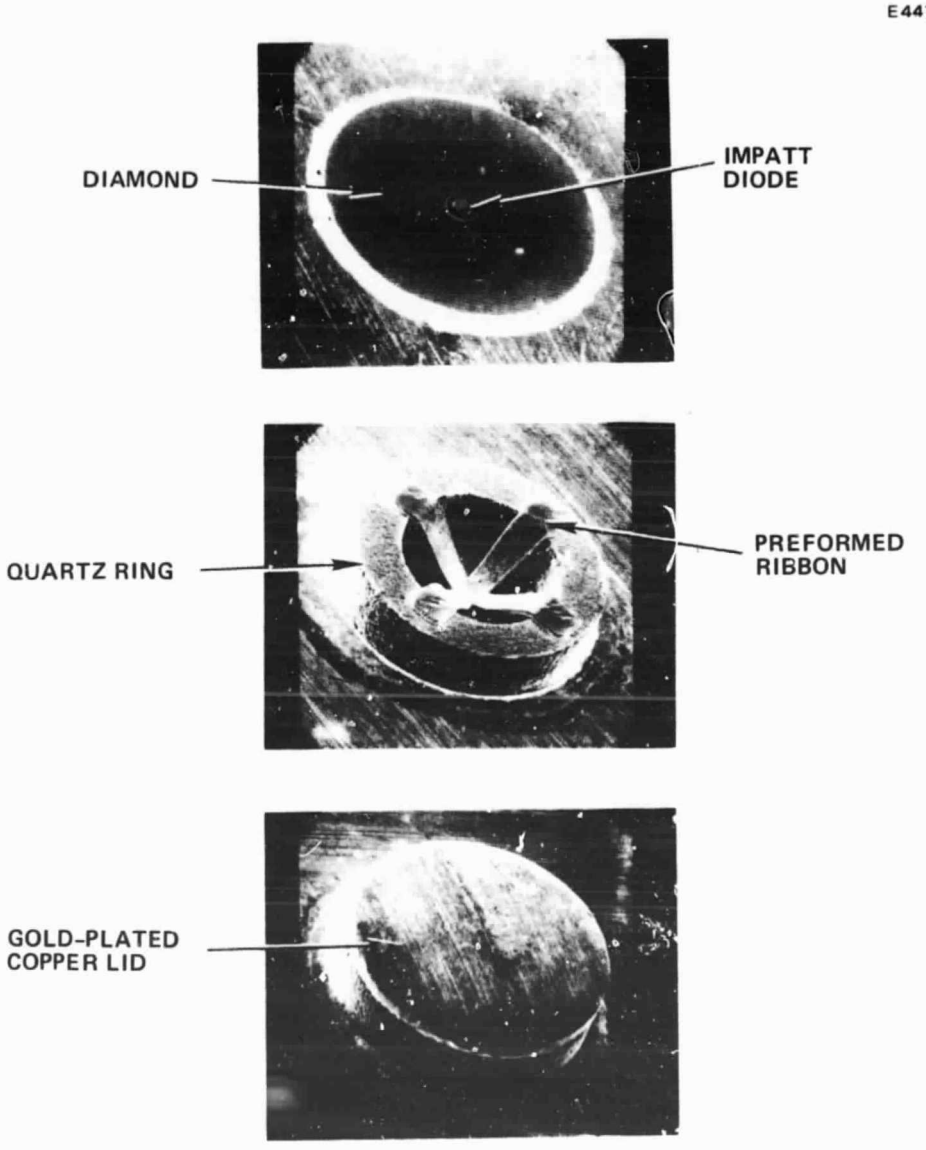

Figure 37 Fabrication sequence of quartz-ring package on diamond heatsink.

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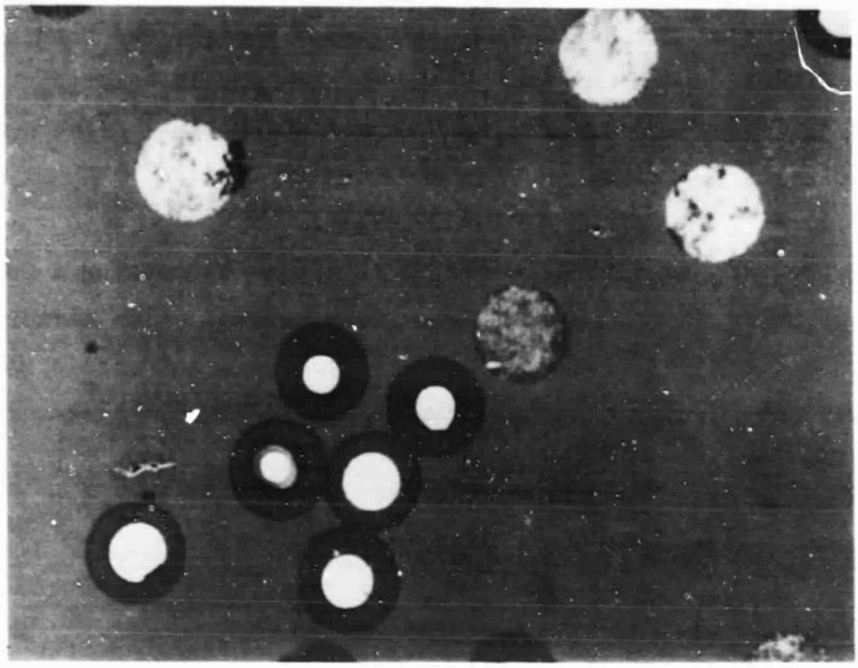

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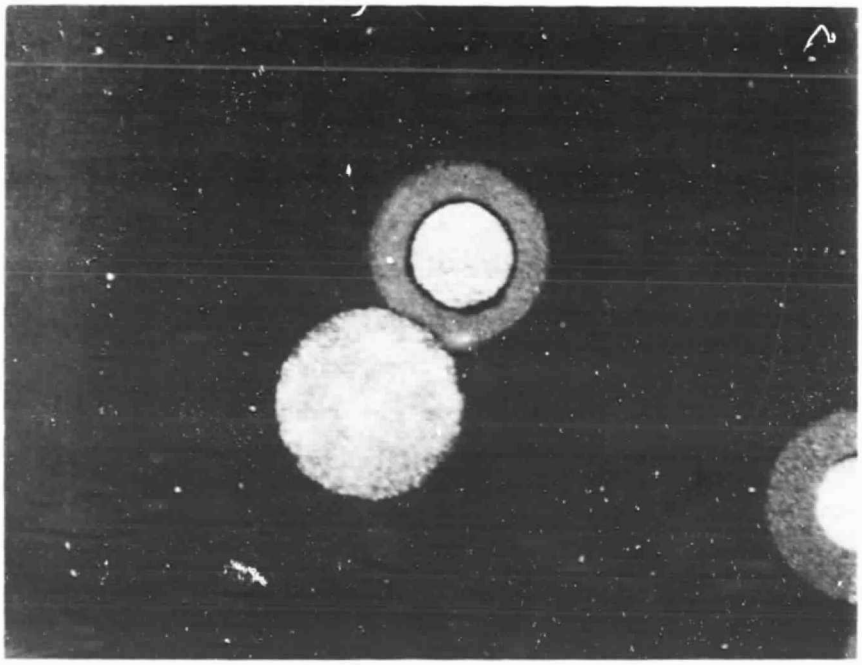

(b)

Figure 33 Pill diode chips after clean-up etch.

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We experimented with diode bonding to a diamond heatsink at different bonding pressures. Because of the brittleness of GaAs material, the bonding pressure of GaAs pill diodes on diamond heatsinks, without surface damage, was lower than that of silicone diodes. Figure 34 shows a GaAs pill diode successfully bonded to a diamond heatsink.

We had also attempted to fabricate GaAs pill diodes by cutting a GaAs wafer with a diamond saw. Experiments on dummy GaAs wafers, using different thicknesses of blades with different speeds, resulted in considerable saw damage. The damage was severe enough to be noticeable even after a clean etch. Consequently, this approach was abandoned.

4.1.3 Diamond Heatsink

Diamond heatsink was essential for the development of high performance V-band GaAs IMPATTs. We have performed a considerable amount of development work on diamond heatsink in recent years and have established optimum metallization and diode bonding. We obtained a factor of nearly two improvement with a diamond heatsink compared with a copper heatsink.

The key to achieving low thermal resistance with diamond heatsinks lies in the diamond metallization. With considerable effort, we have developed a metallization system compatible with diamond. A high temperature sputtering process has also been developed using a Cr-Pt-Au metallization. This involves the use of a high temperature sputtering procedure prior to heating the diamond in a vacuum. A sputter cleaning process is then done, and is followed immediately by a sputtered Cr-Pt-Au metallization in the same vacuum system. The Cr is used as a contact metal due to its good match in lattice constant with diamond. The close match in lattice constant results in a metallic interface layer with optimal thermal transfer properties. With the high temperature Cr-Pt-Au metallization technique, consistently low thermal resistances have been measured.

We have developed procedures for checking the integrity of the metallization process that is critical to the thermal resistance of diamond heatsink diodes.

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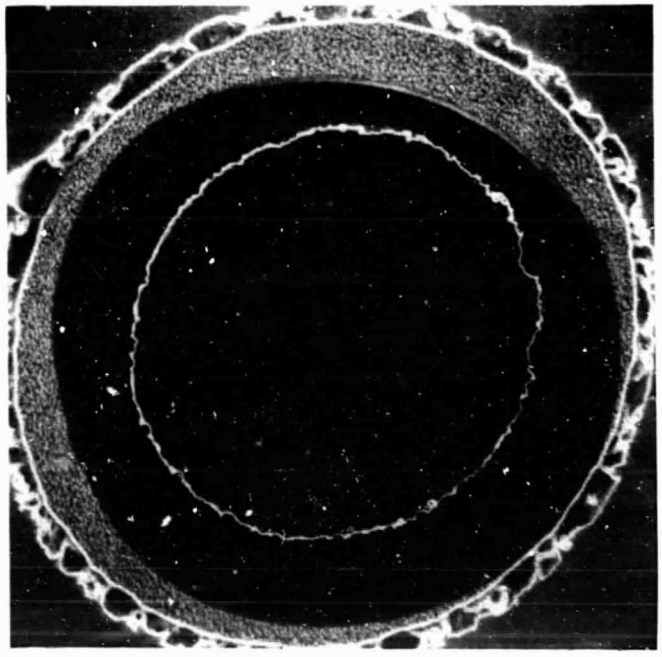

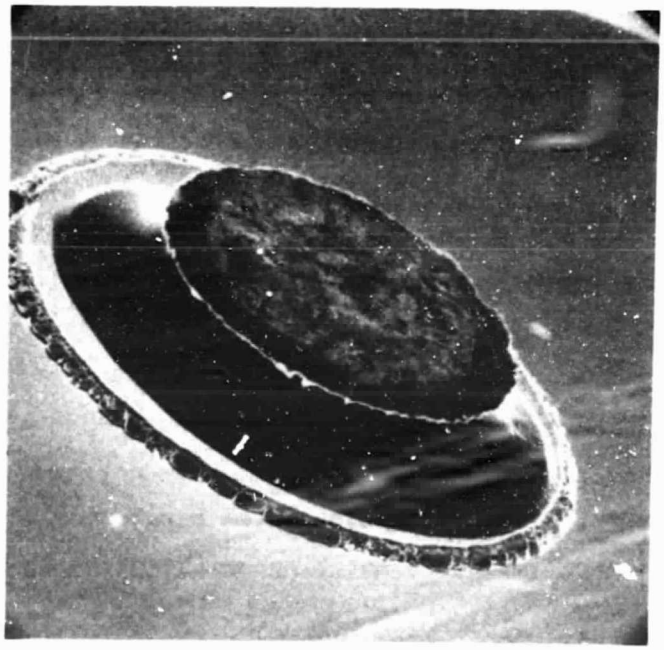

Figure 34 GaAs pill diode bonded to diamond heatsink.

We used sample metallized diamonds in packaging a set of IMPATT diodes from a previous test lot specifically set aside for this purpose. The IMPATTs were accurately trim-etched to a given zero-bias capacitance to ensure that all the diodes were of the same area. We then measured the thermal resistances. For the diamond lot to be qualified, the measured value must be lower than an established value from a previous measurement on similar diodes. All the data were then stored in a data bank for future reference.

4.2 DIODE PACKAGING

The device package must be designed to meet both the electrical and thermal requirements. It should also provide reliable operation and easy handling for the device. Miniature quartz-ring packages have been used at Hughes for millimeter-wave IMPATT diodes operating up to 150 GHz.

4.2.1 Package Design Considerations

The package associated with a millimeter-wave diode is a critical element to the overall diode performance. An empirically designed diode package can degrade the performance of a diode by: 1) introducing high RF loss from the packaging materials, 2) having high parasitic capacitances and inductances that essentially force the diode to operate at lower than the optimum design frequency, and 3) having a high thermal resistance that leads to a high junction temperature resulting in poor device reliability. Therefore, the features necessary in a good millimeter-wave device package are:

1. Low RF loss from the packaging material.

2. Low electrical parasitics or controlled parasitics which are beneficial to the impedance matching of the diode to the external circuit.

3. Low thermal resistance between the diode chip and the remainder of the circuit.

In addition, other desirable physical features for the package are:

1. Mechanical ruggedness
2. Hermetic sealability
3. Reproducibility

Minimum package parasitics do not always yield the optimum package design. It is desirable to minimize resistive loss associated with the chip and its mounting connections. It is also desirable to minimize capacitance that shunts the chip in order to reduce circulating RF currents that are dissipated in the resistive parasitics. However, the inductance of the connecting lead often has an optimum non-minimum value. A package, or mount, should be designed to have a shunt capacitance value that is a small fraction of the operating diode capacitance and to have means for varying the inductance of the connecting leads.

The parasitics associated with the package can be used to provide part of the required impedance transformation from the low impedance level of the device to high circuit impedance level. A qualitative understanding of this impedance transformation can be obtained using a simplified equivalent circuit shown in Figure 35. It can be shown that at the frequency determined by:

$$\omega^2 L_p \left(\frac{C_p C_d}{C_p + C_d} \right) = 1, \tag{45}$$

the transformed impedance at the package terminal is:

$$Z_{in} = - \frac{R_d}{(\omega C_p R_d)^2} - j \frac{\omega^2 L_p C_d - 1}{(\omega C_p R_d)^2 \omega C_d} \tag{46}$$

For $C_p R_d < 1$, the negative resistance of the device is transformed to a higher value.

A qualitative illustration of the transformed impedance as a function of frequency is shown in Figure 36. To transform the low negative resistance of the diode chip to a higher value, it will be necessary to operate the diode

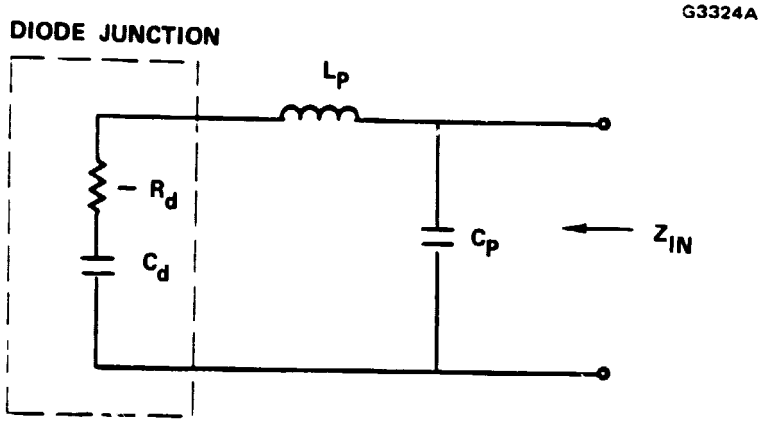

Figure 35 Equivalent circuit of IMPATT diode and package.

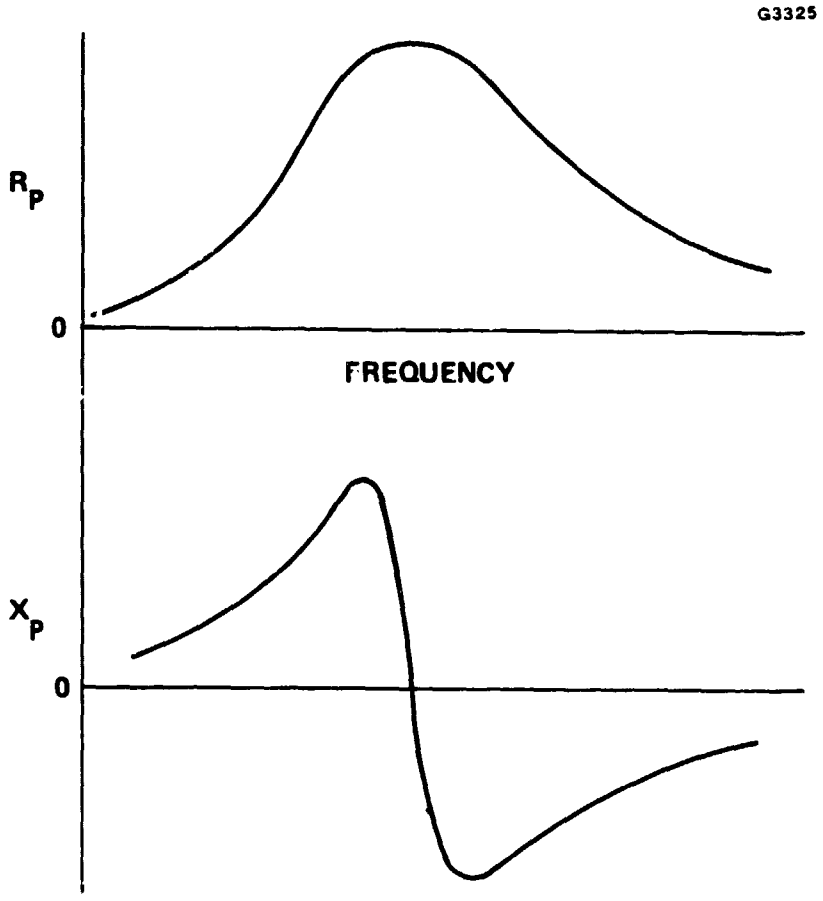

Figure 36 Qualitative representation of transformed diode impedance at the package terminal as a function of frequency.

close to the package resonant frequency. For this reason, the element value L_p from the ribbon and C_p from the insulator must be properly designed as will be discussed below.

4.2.2 Quartz-Ring Package Fabrication

We have used miniature quartz-ring packages for 60 GHz GaAs IMPATT diodes. The low package parasitics realized by these packages are necessary for operation at millimeter-wave frequencies. The fabrication procedure of a quartz-ring package around a plated heatsink diode is as follows:

1. A single crystal quartz ring metallized top and bottom is soldered to the integrated heatsink base concentric to the diode diameter.

2. A gold ribbon is thermosonic-bonded from the top of the diode to the top of the quartz insulator ring.

3. The diode is chemically trim-etched to a preselected junction area. This process is monitored by measuring the zero-bias capacitance of the diode which is a function of the diode cross-sectional area.

4. The assembly is baked and a gold-plated copper lid is soldered onto the top of the quartz insulator ring.

The fabrication procedure of a quartz-ring packaged pill diode on a diamond heatsink is illustrated in Figure 37 and is outlined below:

1. A metallized diamond is hot-pressed into a gold-plated copper heatsink.

2. A GaAs pill diode is TC-bonded to the diamond.

3. A single crystal quartz ring metallized on top and bottom is soldered to the heatsink base concentric to the diode diameter.

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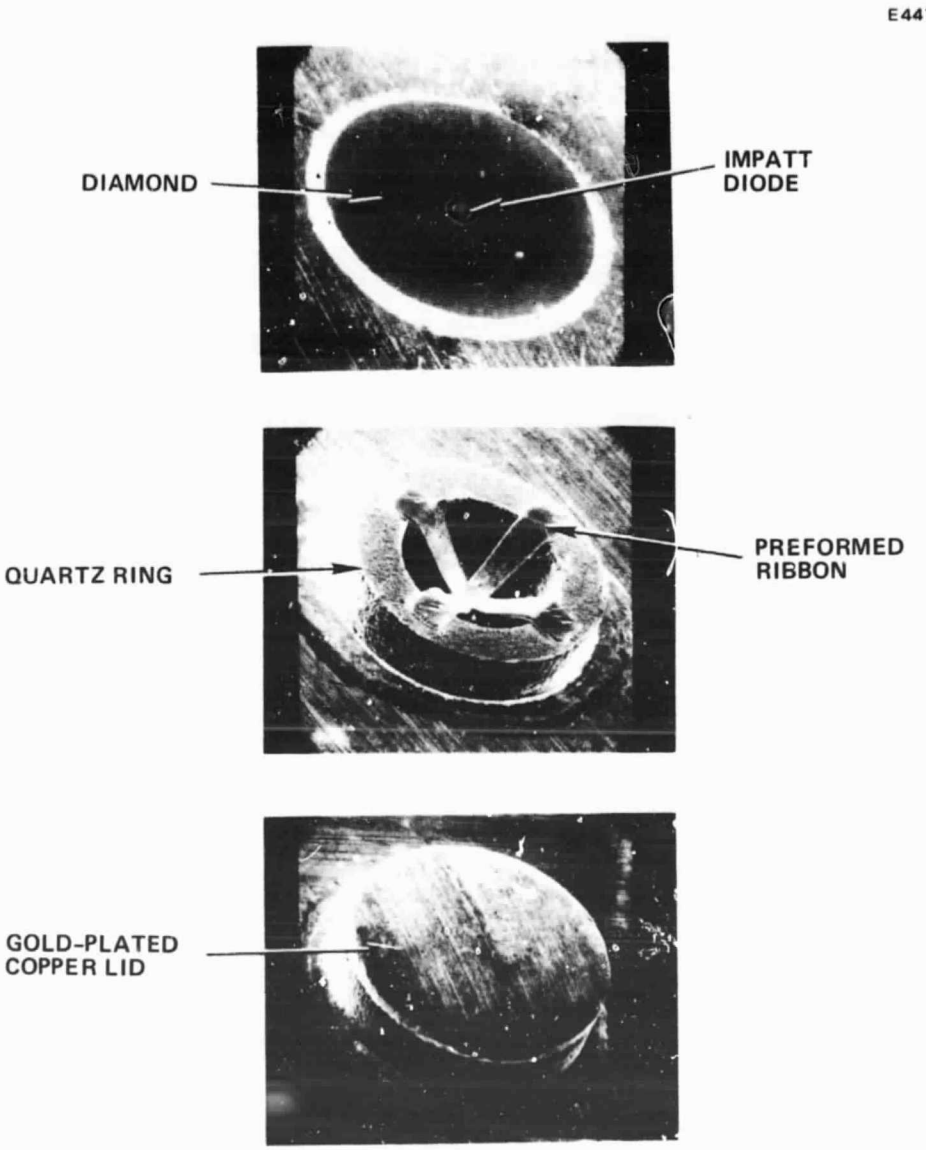

Figure 37 Fabrication sequence of quartz-ring package on diamond heatsink.

4. A gold ribbon is TC-bonded from the top of the diode to the top of the quartz ring.

5. The diode is chemically trim-etched to a pre-selected junction capacitance. This process is monitored by measuring the zero-bias capacitance, which is a function of the diode cross-sectional area.

6. The assembly is baked and a gold-plated copper lid is soldered onto the top of the quartz ring.

The predominant element for package inductance is the connecting ribbon(s) between the diode chip and the surrounding quartz ring. The package inductance was varied by changing the ribbon configuration, as shown in Figure 38. The package capacitance was changed by using different sizes of quartz rings. Figure 39 illustrates the mini- and micro-pill quartz-ring packages used for V-band GaAs IMPATT diodes. Since the 60 GHz GaAs IMPATT diodes in two different packages did not indicate any significant difference in RF evaluation, we extensively used the mini-pill quartz-ring packages in a cross-strap ribbon configuration.

4.2.3 Ribbon Configuration

At early stages of the program, we packaged GaAs sample diodes using preformed ribbons of three-mil width and one-mil thickness. The preformed ribbons are well defined and have uniform inductance values. When these diodes were tested, however, we experienced many premature diode failures. Subsequent investigation revealed significant undercuts in the mesa configuration of these diodes. The small diode size of 40 to 50 μm in diameter, required for millimeter-wave GaAs IMPATTs, could not be adequately trim-etched under the three-mil width ribbon(s). To minimize the undercut, we have used a one-mil diameter gold wire instead of the preformed ribbons. In most cases, the wire was used in cross-strap configuration. Figure 40 represents the mini-pill quartz-ring packages with one-mil diameter gold wire and with preformed ribbons.

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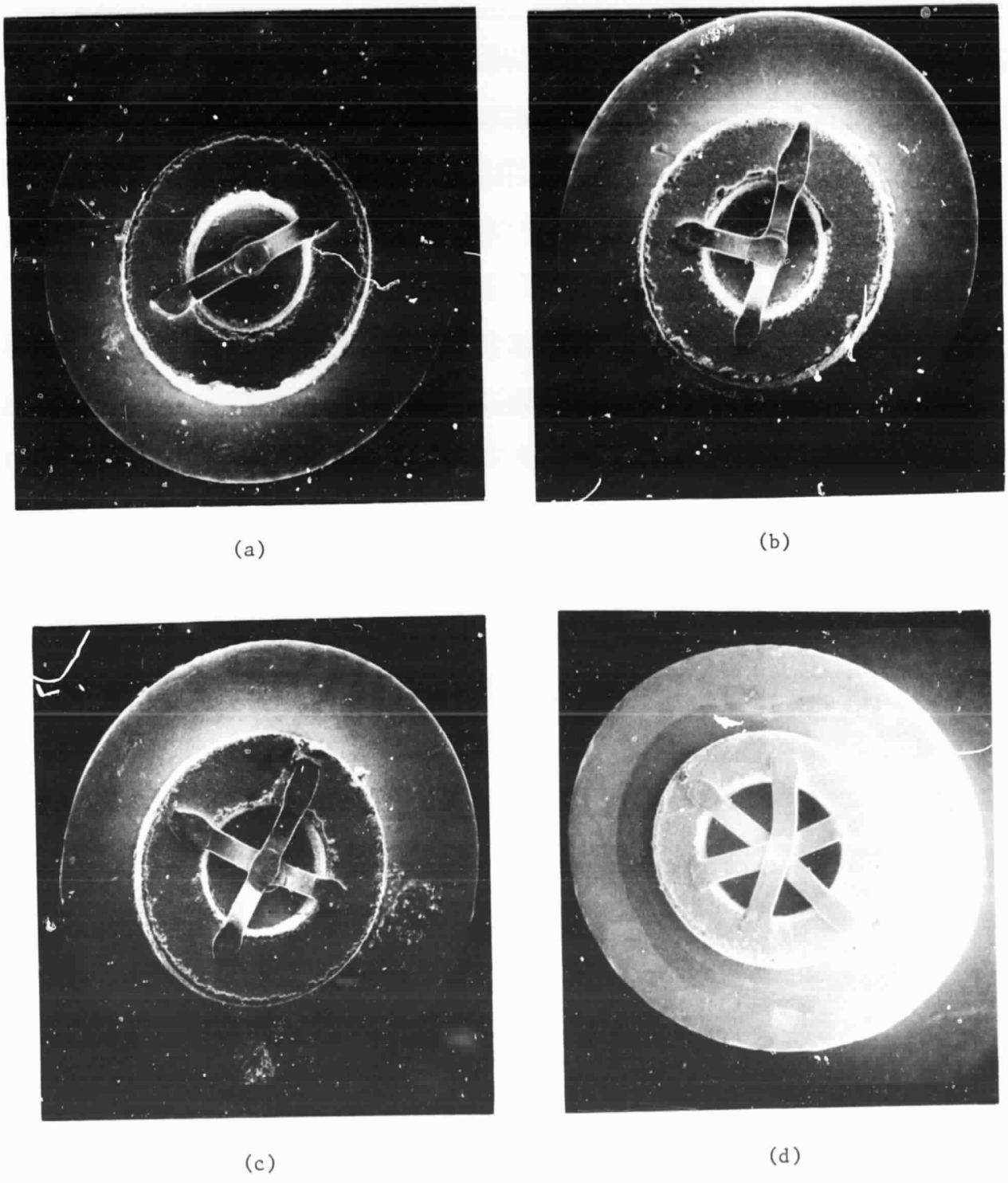

(a) (b)

(c) (d)

Figure 38 Photographs of ribbon configurations for quartz-ring package. (a) Full strap, (b) 1.5 strap, (c) cross strap, (d) triple strap.

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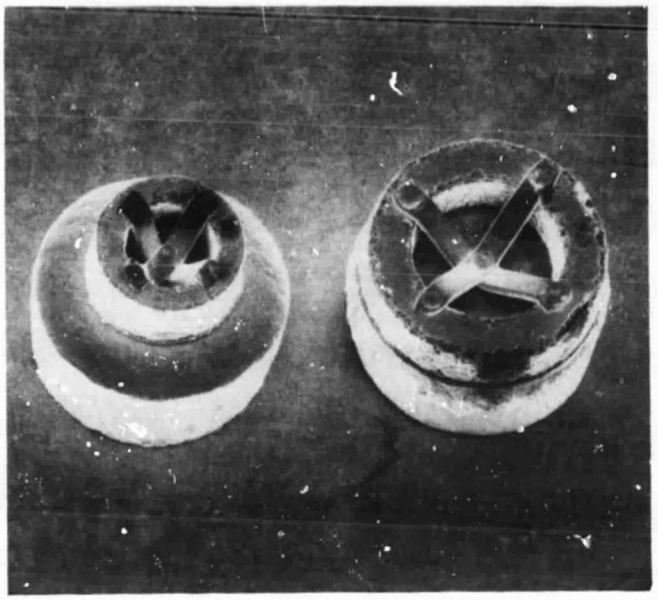
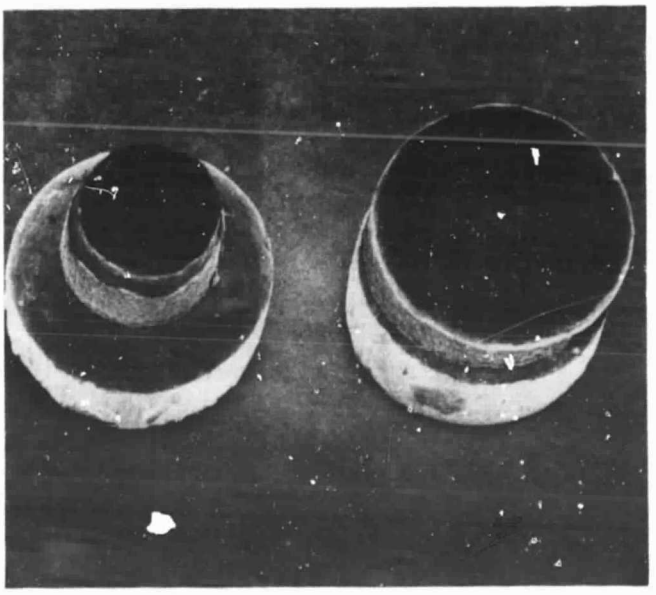


(a) WITHOUT CAP



(b) WITH CAP

Figure 39 Size comparisons between minipill and micropill quartz-ring packages.

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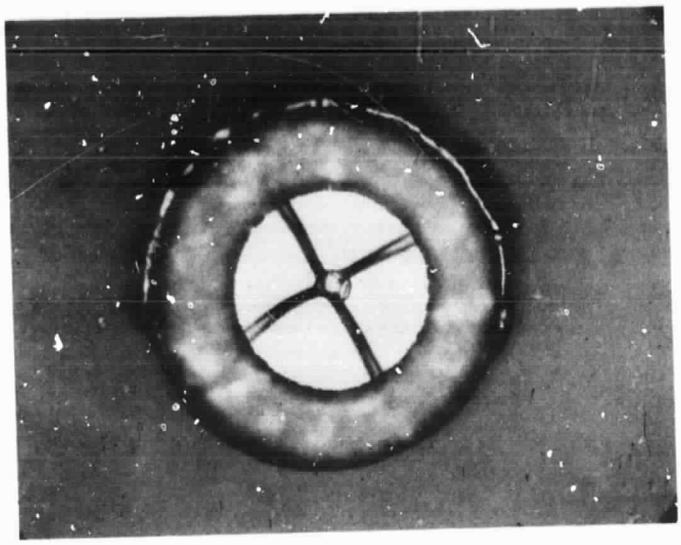
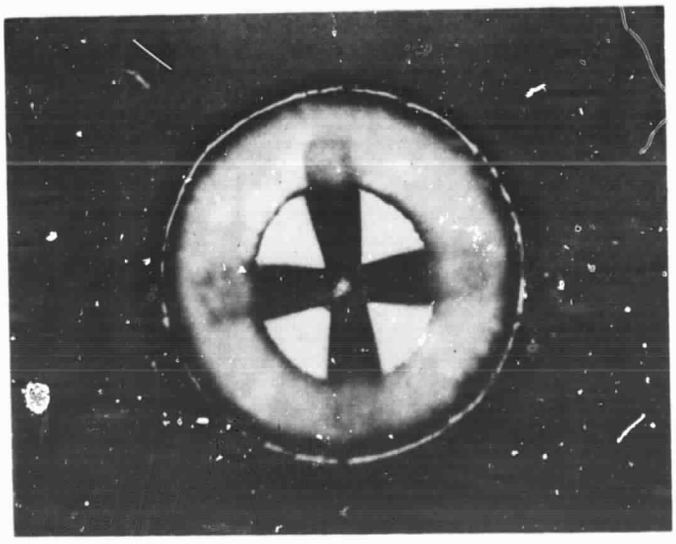


(a) 1 MIL GOLD WIRE



(b) 3 MIL WIDTH PREFORMED RIBBON.

Figure 40 Quartz-ring with gold wire and preformed ribbon.

5.0 DIODE EVALUATION AND TEST

Electrical evaluation has been conducted at various stages of diode fabrication to characterize the diode. The dc evaluation data at each stage provided valuable information on diode RF performance and was used to determine whether to continue the processing. Then, routine RF evaluation was performed on sample diodes of each diode lot. More elaborate RF test and thermal resistance measurement were conducted on samples from the diode lots which indicated good RF performance in the preliminary test. All evaluation data were then implemented as inputs for next diode designs.

To realize the full potential of an IMPATT diode, an oscillator cavity must have low loss and provide a proper impedance matching. A less than optimum test circuit could give misleading information on the quality of the IMPATT by yielding less than maximum diode output power. Impedance mismatch could also lead to easy device burnout. The coaxially coupled reduced-height waveguide cavity was used extensively for diode RF test. The full-height waveguide resonator cavity was used only occasionally for further circuit optimization.

5.1 DC CHARACTERIZATION

The most important dc parameters of IMPATT diodes regarding diode RF performance are the doping profile, reverse breakdown voltage, forward voltage, reverse leakage current, and the junction capacitance. As discussed in Section 2.0, the doping profile basically establishes diode RF performance. The breakdown voltage is directly related to the doping profile. A sharp reverse breakdown free from microplasma and excess leakage current is important for reliable operation of an IMPATT diode. From the data on breakdown voltage and the junction capacitance, the diode junction diameter and area can be determined. The differential resistance from the forward I-V characteristic reveals the quality of metallization (ohmic contact) of the diode. Excessive voltage drop or resistance indicates poor ohmic contacts which, in turn, yield short device life.

The doping profile was measured three times during GaAs IMPATT fabrication; first after material growth, next after formation of channel grid on the epi side of a wafer, and finally at the completion of mesa diodes. Breakdown voltage and leakage current were also checked during these profile measurements. The latter two measurements were used to investigate the quality of wafer metallization as well as to confirm the previously measured doping profile. Upon formation of the mesa diode, breakdown voltage and junction capacitance were often mapped to investigate wafer uniformity.

As discussed before, the doping profile was obtained by capacitance-voltage (C-V) measurement. Measurement of other dc parameters is straightforward. The junction capacitance was measured using a capacitance meter normally at zero-bias voltage. The C-V characteristic of the diode was measured using digital meters or a curve tracer. Breakdown voltages and reverse leakage currents were measured at several different points.

The first profile evaluation was conducted on a step-etched wafer. Ti-Au metallization was used to prevent any metal penetration into the wafer. However, doping concentrations of the double-drift structures (measured at the surface and at the first step) often indicated different values, because the contact quality depended on the p-concentration. The Ti-Au metallization requires high p-doping concentration for good ohmic contact. The diode breakdown characteristics depend not only on the GaAs epi material, but also on the wafer metallization.

Most of the SD GaAs IMPATT diodes with a Schottky contact directly on an n-type epitaxial material showed poor breakdown characteristic with wide variation in breakdown voltage. This was true for both VPE and MBE grown diodes. The soft breakdown characteristic of a Schottky contact IMPATT diode, which has also been reported in other laboratories,[21,22] became more acute for Read-type diodes in which the Schottky contact was made on high concentration n-type material. The breakdown characteristic was improved when a p-layer was introduced over the n-layer(s) prior to metallization. In general, MBE-grown DD diodes indicated sharp breakdown but sample diodes from some MBE wafers still showed poor breakdown. In Figure 41, the breakdown characteristic of a

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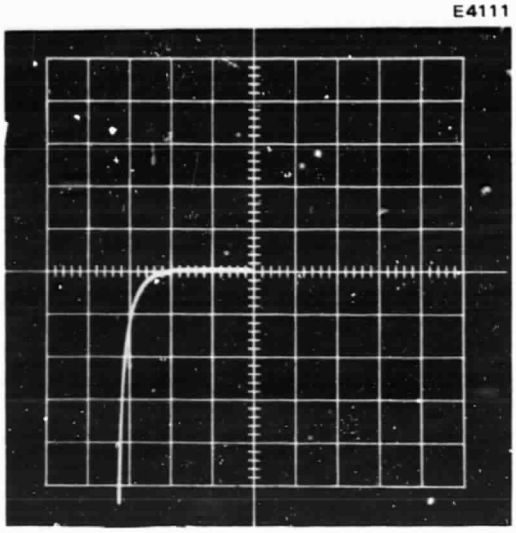
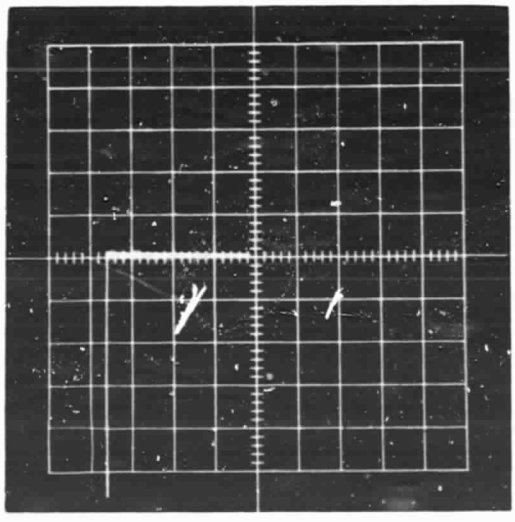


(a) Schottky Contact



(b) Ohmic Contact

Figure 41 Breakdown characteristics of GaAs IMPATT diodes (Vertical 0.2 mA/Div., Horizontal 5 V/Div.)

VPE-grown SD GaAs IMPATT diode is compared with that of a MBE-grown DD diode. The breakdown characteristic was a good indication for diode RF performance and was often used for diode screening.

5.2 THERMAL RESISTANCE MEASUREMENT

At Hughes MPD, thermal resistance of millimeter-wave silicon IMPATT diodes has been measured routinely using a technique similar to that described by Haitz, et al.[23] The measurement technique is based on the current-voltage (I-V) characteristic of an IMPATT diode in avalanche breakdown and on the temperature dependence of the reverse breakdown voltage. Measured thermal characteristics of the V-band GaAs IMPATTs were similar to those of silicon diodes; hence, the same technique was applied to measuring thermal resistance of GaAs IMPATTs without any modifications.

One major difference between our measurement technique and that of Haitz is a negative pulse of several volts amplitude, rather than a small perturbation signal, was used to determine the slope of I-V characteristic (i.e., the space-charge resistance) of the diode under isothermal conditions. Based on the temperature dependence of the diode reverse breakdown voltage, the I-V characteristic in avalanche breakdown at two different junction temperatures can be written as:

$$V_2 = V_1\left[1 + \beta\,(T_2 - T_1)\right] + (I_2 - I_1)\,R_1\left[1 + \gamma\,(T_2 - T_1)\right] \qquad (47)$$

Here the subscripts 1 and 2 represent two points on the I-V curve, and

V_1, V_2 = Diode voltage at Points 1 and 2,

I_1, I_2 = Diode currents at Points 1 and 2,

T_2, T_2 = Diode junction temperature at Points 1 and 2,

R_1 = Diode electrical resistance at point 1, which consists primarily of the depletion region space-change resistance as well as any additional series resistance,

$\beta = 1/V_1 \, \partial V/\partial T =$ Temperature coefficient of reverse voltage,

and

$\gamma = 1/R_1 \, \partial R/\partial T =$ Temperatue coefficient of electrical resistance.

For convenience we let:

$$\Delta V = V_2 - V_1$$
$$\Delta T = T_2 - T_1$$
$$\Delta I = I_2 - I_1$$
$$\Delta V_p = R \, \Delta I$$

Then, solving Equation (47) for the temperature rise T gives:

$$\Delta T = \frac{\Delta V - \Delta V_p}{V_1 \beta + \gamma(\Delta V_p)} \tag{48}$$

The thermal resistance R_T is then given by the temperature rise divided by the power increment;

$$R_T = \frac{\Delta T}{\Delta P} = \frac{\Delta V - \Delta V_p}{[V_1\beta + \gamma(\Delta V_p)] \; (V_2 I_2 - V_1 I_1)} \tag{49}$$

Thus, the determination of R_T involves the evaluation of the quantities appearing on the right side of Equation (49). Two points on the I-V characteristic were selected first. Typically, the values 5 mA and 55 mA were chosen for I_1 and I_2, respectively. The quantities I_1, I_2, V_1, V_2 and ΔV were determined with digital meters. ΔV_p is the electrical contribution to the voltage rise (i.e., that part of the rise not due to heating). To determine the magnitude of this rise, a fast pulse measurement was used to minimize diode heating. The diode current was pulsed between I_1 and I_2 and the voltage rise was noted on an oscilloscope. The pulse applied was 100 nsec

in length and the voltage was read as early in the pulse as possible (20 to 50 nsec). The temperature coefficients β and γ were determined for each diode from voltage and resistance measurements with the diode mounted on a hot plate so that known temperatures could be established.

Special care must be taken for the measurement of ΔV_p. Even for a pulse length as short as 20 nsec there was still noticeable diode heating during the pulse. Thus, the thermal resistance determined from Equation (49) tends to underestimate the true value. If ΔV_p could be measured directly at t = 0 of the applied pulse, then no correction due to heating would be necessary. Since this was difficult to accomplish, the ΔV_p at t = 0 was determined by extrapolation. The voltages were measured at three points on the voltage-pulse curve spaced equally from t = 0. Typically, the points were taken at 20, 40 and 60 nsec. With these three measured values and the application of the LaGrange Three Point Interpolation Formula, the ΔV_p value at t = 0 was determined. The corrected value of thermal resistance, R_T, was then calculated by inserting the ΔV_p at t = 0 into Equation (49). The block diagram of the equipment setup, used for the measurement of pulse paramters, is shown in Figure 42.

The thermal resistance was measured only for selected sample diodes. Table 12 represents the measured thermal resistance of early V-band GaAs DD IMPATT diodes. The diodes were fabricated from the same wafers for different heatsink configurations. Because of the narrower depletion width, the size of the DD hybrid diodes is slightly smaller than that of the DD flat diodes for the same junction capacitance. Zero-bias capacitance of 1.25 pF corresponds to the junction area of 1.45×10^{-5} cm^2 for DD hybrid diodes and 1.78×10^{-5} cm^2 for DD flat diodes, respectively. Obviously, the thermal resistance of the silver-plated heatsink diodes was too high to meet the program requirement at a reasonable junction temperature of 250°C. Thermal resistance of the pill diodes was about 30 percent lower than that of the plated heatsink diodes. In our early measurements of diode thermal resistance we had neglected the term, $\gamma (\Delta V_p)$, in Equation (49). However, we later realized that when this term was included, the thermal resistance reduced by about 10 percent. In Figure 43, the measured thermal resistances of the pill diodes from three

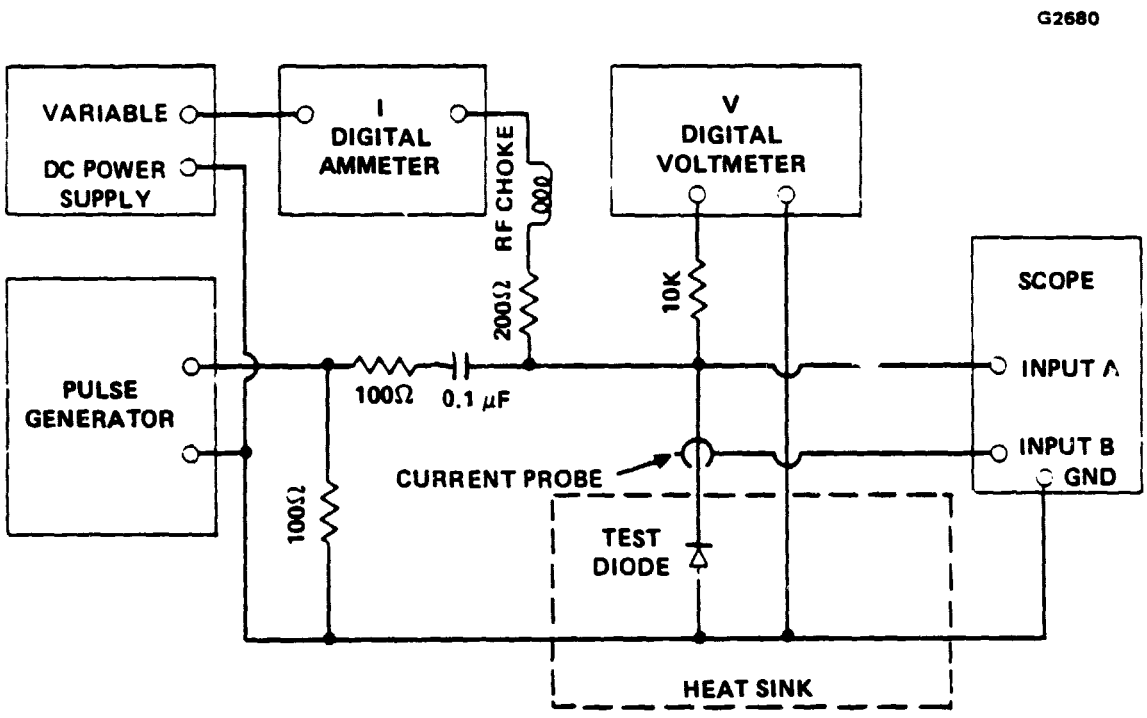


Figure 42 Test setup for pulse parameters required for the measurement of thermal resistance of an IMPATT diode.

TABLE 12

MEASURED THERMAL RESISTANCE OF
V-BAND DD IMPATT DIODES ON DIFFERENT HEATSINKS

Doping Profile	Heatsink	Zero-Bias Capacitance (pF)	Thermal Resistance (°C/W)
DD Flat	Silver-Plated	1.24	79.0
		1.39	74.5
	Diamond	1.25	55.7
		1.40	48.6
DD Hybrid	Silver-Plated	1.12	91.6
		1.24	84.9
	Diamond	1.12	66.2
		1.27	60.3

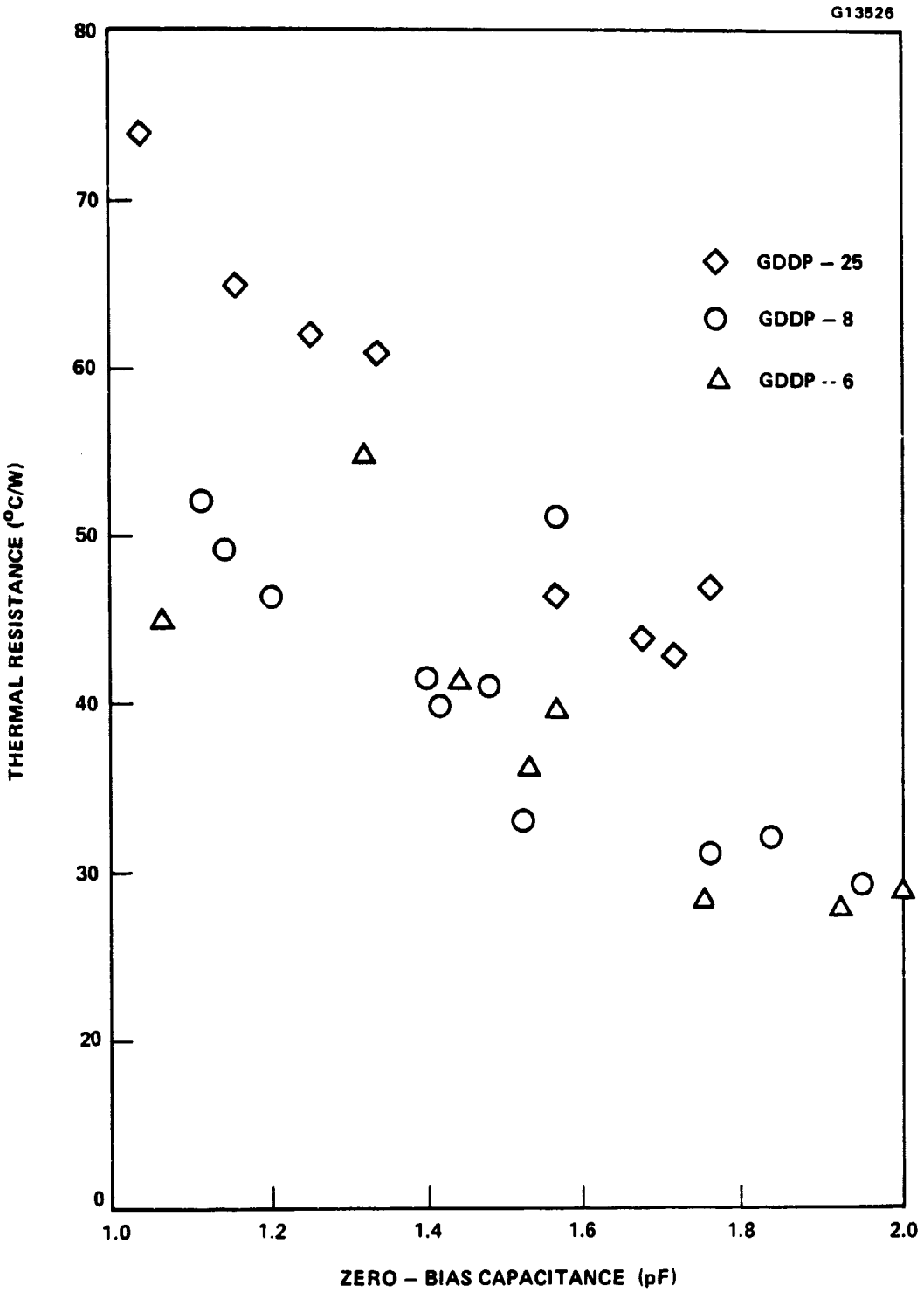


Figure 43 Measured thermal resistance of V-band GaAs IMPATTs.

different lots are plotted as a function of zero-bias capacitance. The GDDP-6 diodes are DD flat structures and the GDDP-8 diodes are DD hybrid structures. Both diode lots were fabricated from MBE wafers grown at Perkin-Elmer and metallized by Au-Zn on the p side and by Au-Ge-Ni on the n side. The GDDP-25 diodes were fabricated from a DD hybrid MBE wafer grown at Cornell University with Pt-Ti-Pt-Au metallization on the p side and Au-Ge-Ni on the n side. The measured thermal resistance of GDDP-25 diodes is clearly higher than those of other diodes.

The measured thermal resistances of V-band GaAs IMPATT diodes with different metallizations are compared in Table 13. The three diode lots were fabricated from the same DD hybrid (flat p and lo-hi-lo n regions) MBE wafers grown at Perkin-Elmer. The GDDP-12 diodes were metallized by Au-Zn on the p side and Au-Ge-Ni on the n side, the GDDP-23A diodes by Pt-Ti-Pt-Au on the p side and Au-Ge-Ni on the n side, and the GDDP-23B diodes by Pt-Ti-Pt-Au on both p and n sides. The breakdown voltages of all three lot diodes were similar: from 14.5 V to 15.3 V. However, the measured thermal resistance of the diodes with Au-Zn metallization on the p side was lower than those of the two remaining lots.

5.3 TEST CIRCUIT AND RF EVALUATION

We have routinely conducted the RF test of an IMPATT diode in a coaxially coupled reduced-height waveguide cavity. We used full-height waveguide resonator cavities only in limited cases. We expected higher output power in the resonator cavities because of the high Q nature. However, the diode RF performance achieved in these cavities was comparable to that measured in reduced-height waveguide cavity. We often used a current regulator in the bias circuit to minimize the transient effect of the power supply.

5.3.1 Oscillator Cavities

The oscillator performance of an IMPATT diode depends not only on the device itself but also on the circuit conditions. In order to obtain optimum RF

TABLE 13

MEASURED THERMAL RESISTANCES OF V-BAND DD GaAs IMPATTS WITH DIFFERENT METALLIZATIONS

Lot No.	GDDP-12			GDDP-23A			GDDP-23B		
Diode No.	C_o (pF)	V_{BR} (V)	θ_T (°C/W)	C_o (pF)	V_{BR} (V)	θ_T (°C/W)	C_o (pF)	V_{BR} (V)	θ_T (°C/W)
1	1.48	14.8	34.0	1.54	14.4	51.8	1.50	15.1	46.6
2	1.53	14.8	31.7	1.56	14.4	41.9	1.54	15.2	43.4
3	1.54	14.6	37.6	1.56	15.0	42.9	1.55	15.3	53.1
4	1.54	14.7	31.4	1.57	14.2	45.0	1.56	15.3	42.3
5	1.55	14.6	35.3	1.57	14.6	42.0	1.57	15.3	40.0
6	1.57	14.7	33.0	1.57	14.3	45.9	1.58	15.3	47.9
7	1.59	14.8	31.9	1.60	14.4	42.4	1.58	15.2	41.6
8	1.59	14.8	27.5	1.60	14.5	44.7	1.59	15.1	39.1

C_o ; Zero-bias capacitance
V_{BR}; Breakdown voltage
θ_T ; Thermal resistance

performance consistent with high reliability from an IMPATT diode, the oscillator cavity must provide the following characteristics.

1. Low circuit loss to minimize power loss in the cavity.

2. Proper RF impedance matching to both real and imaginary parts of the diode impedance to efficiently extract power output at the desired frequency.

3. Low thermal resistance to remove the heat generated in the diode.

5.3.1.1 Coaxially Coupled Reduced-Height Waveguide Cavity - A rectangular waveguide cavity cross-coupled by a short coaxial section of which one end is terminated by an IMPATT diode has been used for IMPATT oscillators. This configuration has great versatility in impedance matching. The waveguide height is reduced to lower the characteristic impedance of the waveguide and the reduced-height waveguide is coupled to the full-height waveguide through a step transformer. Figure 44 shows a V-band coaxially coupled reduced-height waveguide cavity.

The diode is contacted by a bias pin which also serves as a coupling post in the waveguide as well as the center conductor of the coaxial line. The bias line is introduced through the top wall of the waveguide and is insulated from the cavity. The two coaxial sections at the top and bottom of the waveguide provide a wide range of impedance matching. Final tuning of the cavity is obtained by the sliding short in the waveguide.

This circuit has a great deal of flexibility because it is readily disassembled and parts can be interchanged with others of varied dimensions to vary the impedance presented to the IMPATT. For example, the coaxial line section around the bias pin at the IMPATT diode end can be varied in outer diameter and length merely by replacing a shim with another of different hole diameter and thickness, respectively. Multiple coaxial sections were realized by stacking such shims.

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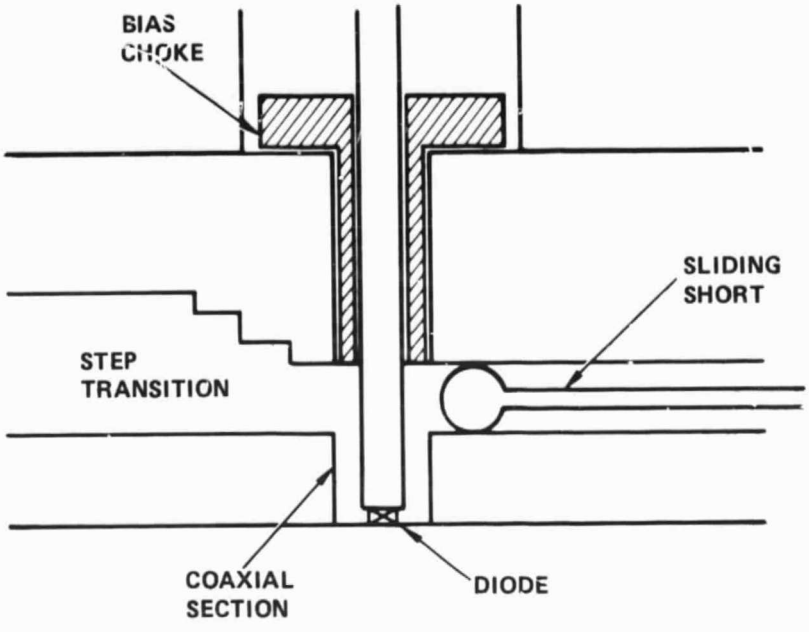

(a) SCHEMATIC DIAGRAM

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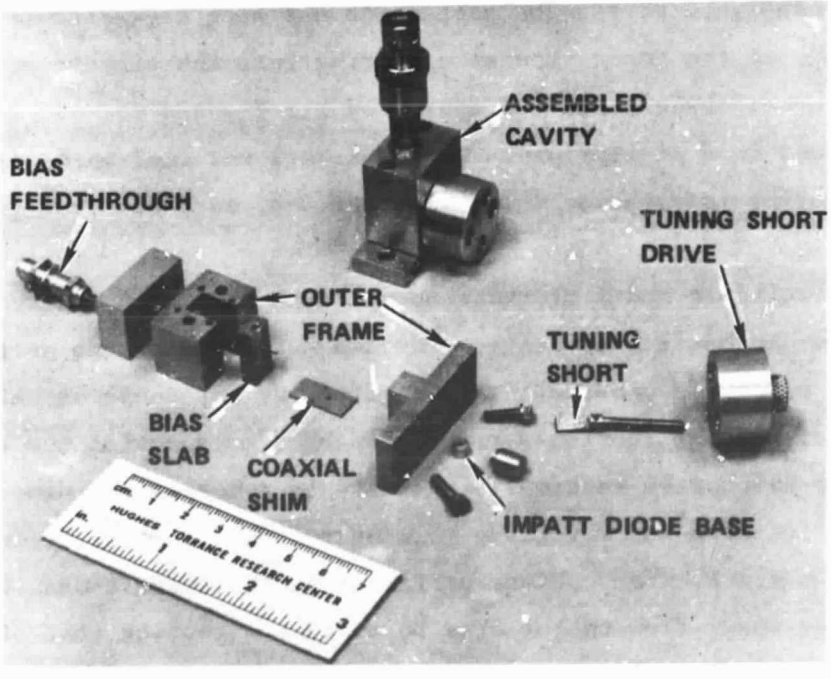


(b) ASSEMBLY PHOTO

Figure 44 Coaxially coupled reduced-height waveguide cavity.

Another important feature of this IMPATT test fixture is the means for inserting and removing the IMPATT diodes. A packaged IMPATT diode is mounted on a gold-plated copper cylinder, shown in Figure 44(b), which can be readily inserted into the test fixture and removed without disturbing the overall circuit assembly. This is important because slight changes in mechanical positioning can present a large electrical change at millimeter-wave frequencies. The diode mount cylinder is held firmly in position by means of a threaded plug which is easily inserted and removed with a screwdriver. This method minimizes changes in the RF circuit load seen by an IMPATT which may be brought about by inserting or removing a diode from the test fixture.

We made extensive investigation for the coaxially coupled waveguide circuit. The equivalent circuit shown in Figure 45 is based on the analysis of Lewin[14] with some modifications. Z_0 is the characteristic impedance of the waveguide and Z_{01} and Z_{02} are those of the coaxial lines. Z_{op} is an inductive component due to the post in waveguide excited by TE_{n0} modes. Y and Y_{1p}, Y_{2p} account for the effects of waveguide-coaxial junctions and X_b[15] is due to the phase variation of the field across the post which has been neglected in Lewin's analysis. Z_{IN1} is the input impedance looking into the circuit at the coaxial end with the other three ports terminated by Z_2, Z_3, and Z_4. Z_{IN2}, Z_{IN3} and Z_{IN4} are defined in a similar way. R_1 and R_3 are the real parts of the impedances looking into the port 1-1 and port 3-3, as shown in Figure 45.

The equivalent circuit model provides useful information on the design of an IMPATT cavity. In oscillator design, the two coaxial sections at the top and bottom of the waveguide provide the most effective impedance matching to the diode. The top coaxial section was adjusted by simply moving the bias filter position while the bottom section is adjusted by mounting the diode in a recessed position from the waveguide wall using spacers of different thicknesses and hole sizes. For optimum performance, the circuit must be designed to minimize the power flow to the bias port, thus directing most of the power to the waveguide load.

5.3.1.2 Full-Height Waveguide Resonator Cavity - An alternative approach to the coaxially coupled waveguide circuit is the radial line waveguide circuit

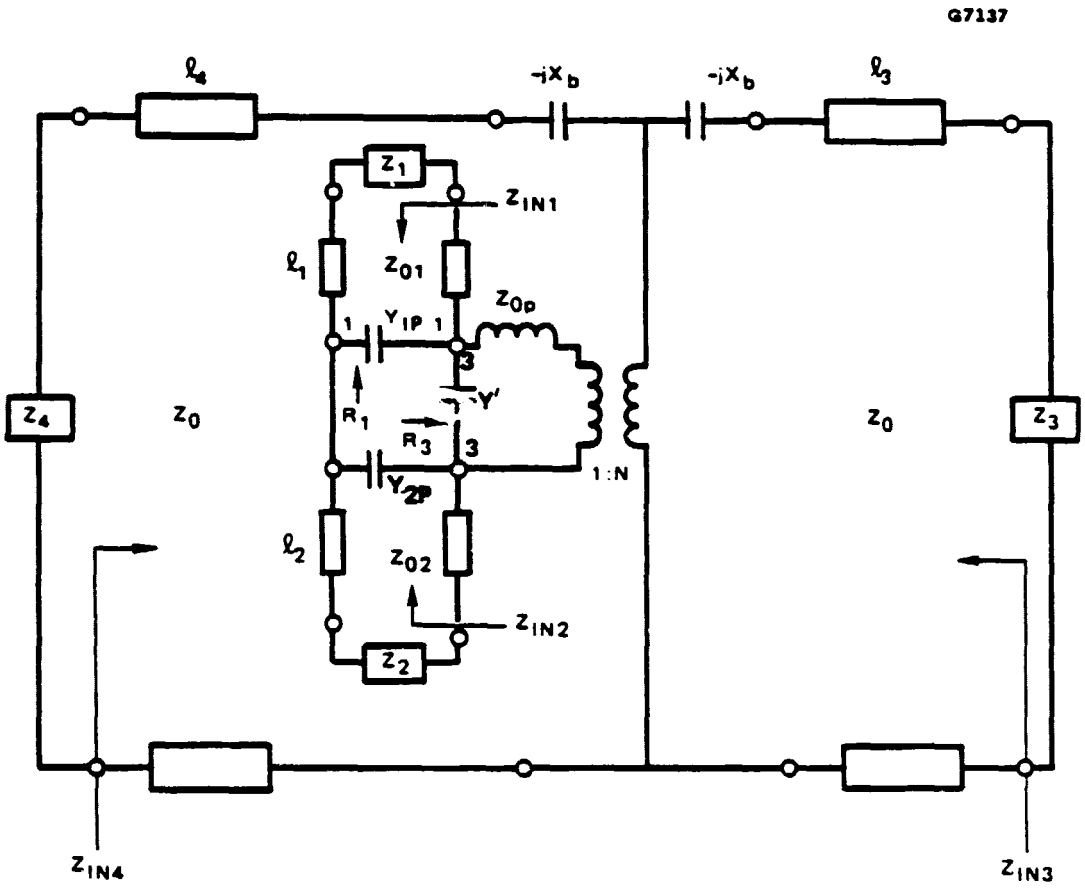


Figure 45 Equivalent circuit of coaxially coupled waveguide mounting structure.

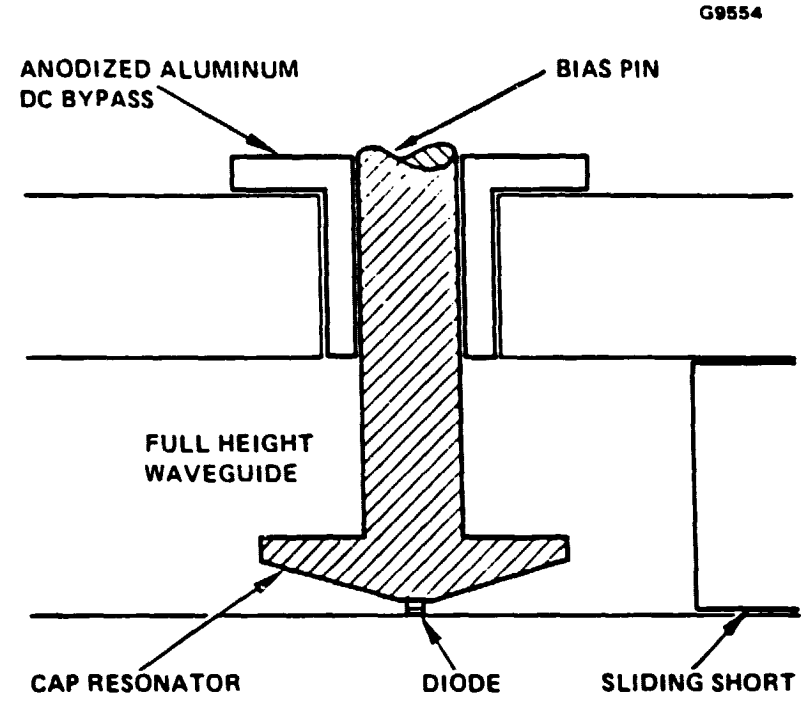
schematically shown in Figure 46. In a cap resonator circuit, a metal "cap", through which dc bias is supplied is brought down to make pressure contact to the diode, forming a localized cavity around the diode. The required high impedance transformation between the circuit and the device is provided by a radial line formed by the cap directly above the diode. The height of the radial line between the cap and the waveguide floor has predominant influence on the matching of the real part of the impedance while the diameter of the cap affects the matching of the imaginary part, thus determining the center frequency of the IMPATT oscillator. The cap thickness and the post diameter has secondary effect on overall impedance matching because of the reflected wave from the sliding short. Increase of the cap thickness reduces the transformation ratio of impedance.

A tapered cap as shown in Figure 46(a) is often used for smooth impedance transformation instead of a flat cap. In the former case, impedance matching can also be controlled by varying the taper angle. The final tuning of the cavity is usually conducted by the sliding short. To obtain optimum RF performance, a proper combination of circuit parameters must be found. Although better oscillator performance has been reported in this cavity, the cap resonator circuit is known to have narrower bandwidth than that of the coaxially coupled reduced-height waveguide circuit.

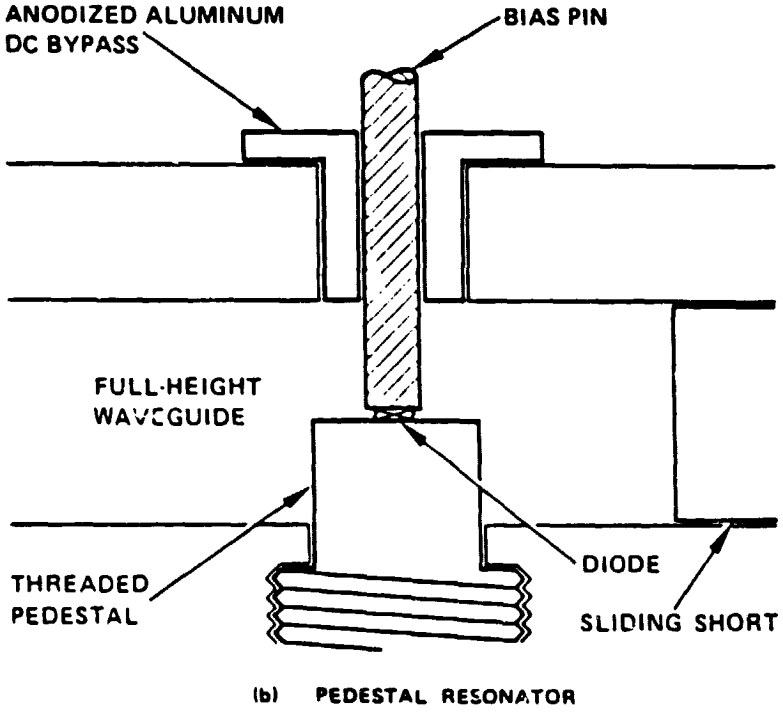
A radial line can also be realized by extending the pedestal into the waveguide as shown in Figure 46(b). The height of the radial line can be controlled continuously by moving the threaded pedestal up and down parallel to the E-plane of the waveguide for tuning purposes. This continuous adjustment simplifies circuit tuning for optimum diode performance.

5.3.2 Current Regulator

The oscillator characteristics of an IMPATT diode are strongly influenced by the bias current. Therefore, an adjustable current regulator has been utilized to stabilize the bias current applied to the diode. Figure 47 represents the schematic diagram of the adjustable current regulator. The LM 117 is an adjustable 3-terminal positive voltage regulator capable of supplying in



(a) CAP RESONATOR



(b) PEDESTAL RESONATOR

Figure 46 Radial line waveguide cavity.

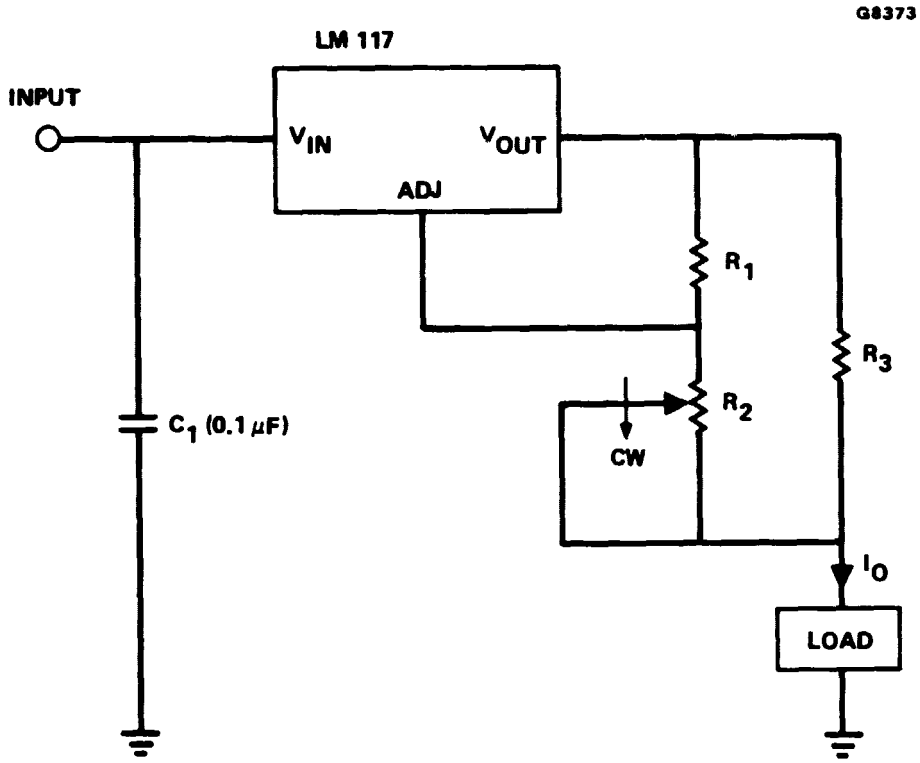


Figure 47 Schematic diagram of current regulator.

excess of 1.5 A over 1.2 to 37 V output voltage range with excellent line and load regulation. It also offers full overload protection under most conditions. The dropout voltage is less than 2.5 V over the temperature range from -55°C to 150°C.

In operation the LM 117 develops a nominal 1.25 V reference voltage between the output and adjustable terminals. By connecting a resistor between those terminals, the LM 117 is used as a precision current regulator. The adjustable current range is determined by the value of the resistor, which is actually a combination of three resistors. The fine control of the current level is provided by a potentiometer, which is represented by a variable resistor R_2 in the figure.

In general, resistor R_3 determines the minimum current level. The maximum current can be obtained by proper combination of R_1 and R_2. The selection of R_2 depends on the availability of a potentiometer as long as the corresponding R_1 values fall in the range which yields the current flow within the program current between 1 and 10 mA. R_3 must be a high-power resistor since most of the current flows through it. In Figure 48, design curves are plotted for different combination of these resistors.

5.3.3 RF Test

5.3.3.1 RF Test Setup - A block diagram of a general millimeter-wave CW oscillator measurement setup is shown in Figure 49. The setup is for the output power, frequency, efficiency and tuning characteristics. Since oscillator performance of an IMPATT diode is sensitive to load VSWR, it is important that the output port of the oscillator under test is terminated properly. It should be pointed out that high VSWR outside the band of specific interest is often the cause of adverse effects. For this reason, an isolator with broadband capability covering the full waveguide band is often used as a broadband termination for the diode under test.

Each measurement system was carefully calibrated as a unit. At millimeter-wave frequencies, the wavelength is so small that small discontinuities

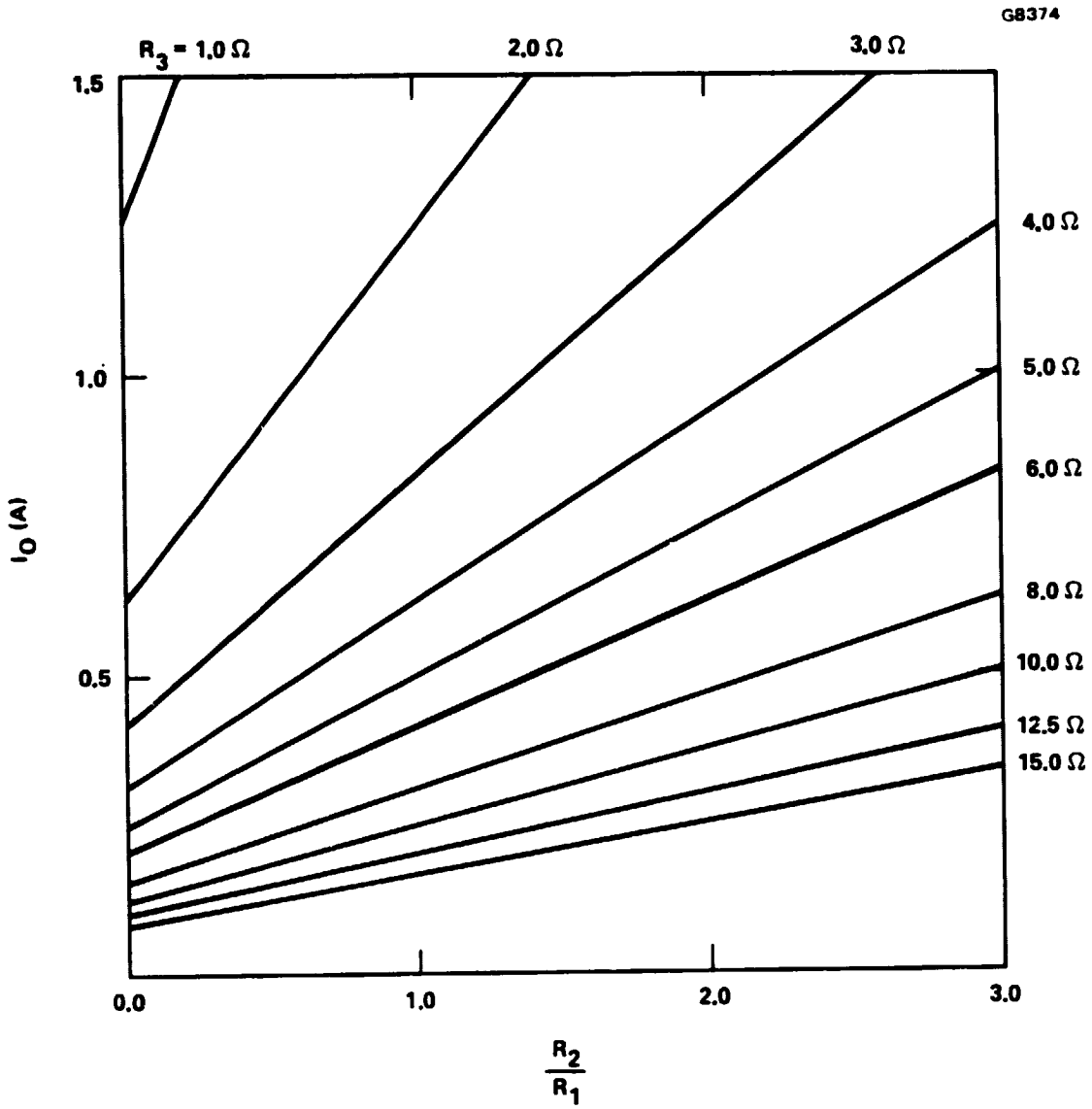


Figure 48 Design curves for current regulator.

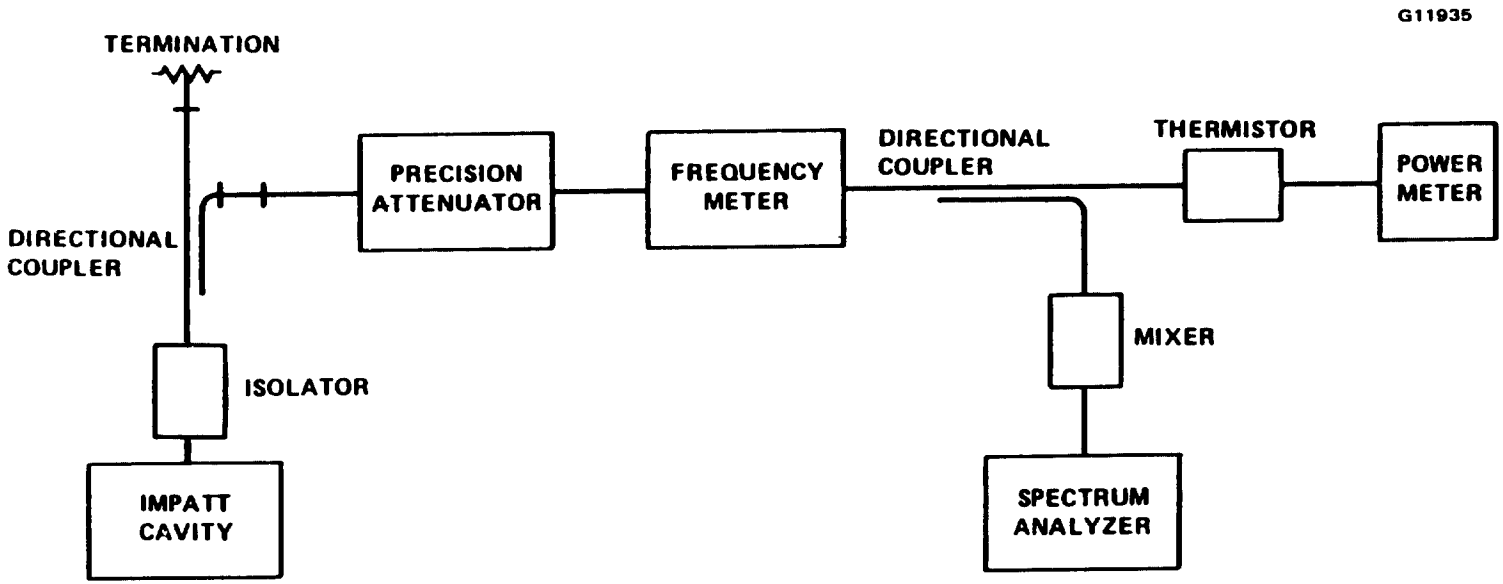


Figure 49 Test setup for CW IMPATT oscillator.

between components can change the insertion loss for the system significantly. The possible inconsistency of the system insertion loss that might be caused by periodic calibration of each individual component was eliminated by calibrating the whole measurement system as a unit.

The oscillator output power was read directly from the power meter considering system calibration and the oscillation frequency was measured using the frequency meter by observing the dip on the power meter. The mixer-spectrum analyzer branch was used to investigate the frequency spectrum and bandwidth. The operating voltage and current were monitored using digital multimeters and these readings were used to calculate input power and dc-to-RF conversion efficiency.

5.3.3.2 RF Performance - RF evaluation of an IMPATT diode has routinely been performed in a coaxially coupled reduced-height waveguide cavity. Since the approximate device/circuit models described previously could not provide the required accuracy of element values to the degree conducted by fine adjustment, the final oscillator performance was optimized through experimental circuit adjustment. Systematic circuit optimization has been carried out to improve oscillator performance for each diode lot. Among the various parameters, the bias choke position, and the spacer hole size and thickness were found to be most effective for circuit optimization. The spacer effectively controls the line length and the characteristic impedance of the coaxial line. The final tuning of the cavity was usually conducted by the sliding short.

A full-height waveguide resonator cavity was also used as a test circuit for some diode lots which had indicated reasonable RF performance in the reduced-height waveguide cavity. The bias pin which has a different cap size at one end was used as a basic optimizing element in this cavity. In general, the best RF performance that could be achieved in one cavity was comparable to that measured in the other cavity.

As described previously, Schottky contact VPE SD IMPATT diodes (both flat and hi-lo structures) indicated poor breakdown characteristics and wide variation

in breakdown voltage. Most of these diodes failed at low bias current level. Many of the failed diodes still showed similar V/I characteristics, but at lower forward and reverse voltages. The best output power obtained from these diodes was limited to 100 mW at low 50 GHz range. Although some of the ohmic contact MBE SD hi-lo diodes (grown at USC) showed fairly sharp breakdowns, they also failed at low bias currents when tested in an oscillator cavity without generating any significant RF power. All the SD diodes were fabricated on plated heatsinks in the early stage of the program.

Although not quite close to the design values in doping profile, many VPE DD flat wafers have been processed for plated heatsink diodes. Because of the rather wide variation in doping profile, the breakdown voltage of these diodes ranged from 13.0 to 28.0 V. Most of these diodes were prone to burn-out at low bias currents and generated output power less than 100 mW. Only a few VPE diode lots generated output power more than 100 mW in the lower end of V-band frequency between 50 and 55 GHz. The maximum output power achieved from a VPE DD flat diode was 300 mW with 5.2 percent efficiency at 51.3 GHz. The current density at this operating point was 16.5 kA/cm^2. However, most of these diodes operated at far lower current densities (< 10 kA/cm^2) and failed when the bias current was increased. Diodes which generated output power over 100 mW generally operated at current density higher than 10 kA/cm^2.

The VPE pill diodes mounted on diamond heatsinks were able to operate at higher bias currents. The maximum output power obtained from a VPE pill diode was 560 mW with 5.25 percent efficiency at 51.2 GHz. The current density at this point was 17.1 kA/cm^2.

The DD diodes fabricated from the MBE wafers grown at Perkin-Elmer have produced more consistent results. From an initial design MBE diode, output power of 260 mW was obtained with 5.2 percent efficiency at 55.1 GHz. Conversion efficiency of 7.65 percent was also obtained with 220 mW output power at 51.6 GHz. These performances were achieved at the current density of 6 to 8 kA/cm^2. All of these diodes were in plated heatsink configuration and the current density was limited to about 8 kA/cm^2, because of the high thermal

resistance. These diodes performed better at Q-band frequencies generating as high as 750 mW with over 10 percent efficiency.

Improved RF performance was realized from the second design MBE IMPATTs. First, silver-plated heatsink diodes were fabricated from a section of each MBE wafer. Although the three DD flat and two DD hybrid wafers were grown with the same reactor settings, some discrepancy in doping profile occurred among these wafers. When processed, sample diodes from different lots also indicated somewhat different RF performance. The plated heatsink diodes appeared to operate better at lower frequencies than the designed value of 60 GHz. We obtained about 500 mW output power around 45 GHz. The attainable output power decreased with increasing oscillation frequency. The highest 15.1 percent from a DD hybrid diode. The highest oscillation frequency was 67.1 GHz with 300 mW output power. Because of the high thermal resistance of plated heatsink diodes, the input power was limited to a bias current of about 10 kA/cm^2 and 12 kA/cm^2 for DD flat and DD hybrid diodes, respectively. RF performance results of these diodes are summarized in Tables 14 and 15.

Second, the remaining portions of the second design MBE wafers were processed into pills and these diodes were TC-bonded on diamond heatsinks. For the same junction capacitance, the pill diodes were able to take much higher bias current than the plated heatsink diodes due to the reduced thermal resistance. The operating bias voltage of the pill diodes was lower than that of the plated heatsink diodes at the same bias current levels. Output power greater than 1 W was achieved from both DD flat and DD hybrid pill diodes on diamond heatsinks. The highest output power was 1.12 W at 51.9 GHz from a DD hybrid diode. The best efficiency obtained at V-band was 11.1 percent from a DD flat diode, and 15.3 percent from a DD hybride diode. Tables 14 and 15 also include the RF performance summary of the pill diodes on diamond heatsinks. The RF performance versus bias current of a DD flat and DD hybrid are shown in Figures 50 and 51, respectively. The oscillation frequency increased slowly with increasing bias current.

The next generation MBE wafers grown at Perkin-Elmer included DD flat, DD hybrid (with flat p and either hi-lo or lo-hi-lo profile in n side), and DD Read (with

TABLE 14

RF PERFORMANCE OF DD FLAT GaAs IMPATTS

Heatsink	Zero-Bias Capacitance (pF)	Current Density (kA/cm^2)	Oscillation Frequency (GHz)	Output Power (mW)	Efficiency (%)
Silver-Plated	1.52	9.2	43.9	480	9.9
	1.1	8.2	46.1	400	13.0
	0.88	9.2	48.6	270	9.7
	1.52	9.7	53.5	250	6.5
Diamond	1.58	17.0	51.7	1025	10.5
	1.48	14.5	53.5	800	9.5
	1.11	13.7	55.9	630	11.1
	1.2	15.2	58.2	740	10.5
	1.06	13.9	67.1	300	6.9

TABLE 15

RF PERFORMANCE OF DD HYBRID GaAs IMPATTS

Heatsink	Zero-Bias Capacitance (pF)	Current Density (kA/cm^2)	Oscillation Frequency (GHz)	Output Power (mW)	Efficiency (%)
Silver-Plated	1.05	9.5	47.2	450	15.1
	1.04	11.9	53.8	435	13.0
	1.02	11.0	55.2	290	9.7
	0.94	10.5	59.3	200	7.9
Diamond	1.79	19.2	45.0	1350	14.0
	1.83	18.8	48.7	1260	13.4
	1.15	15.5	51.7	725	15.3
	2.21	18.5	51.9	1120	9.7
	1.60	12.0	52.75	1050	14.7
	1.57	17.7	55.5	1025	13.3
	1.02	13.1	62.0	325	9.6

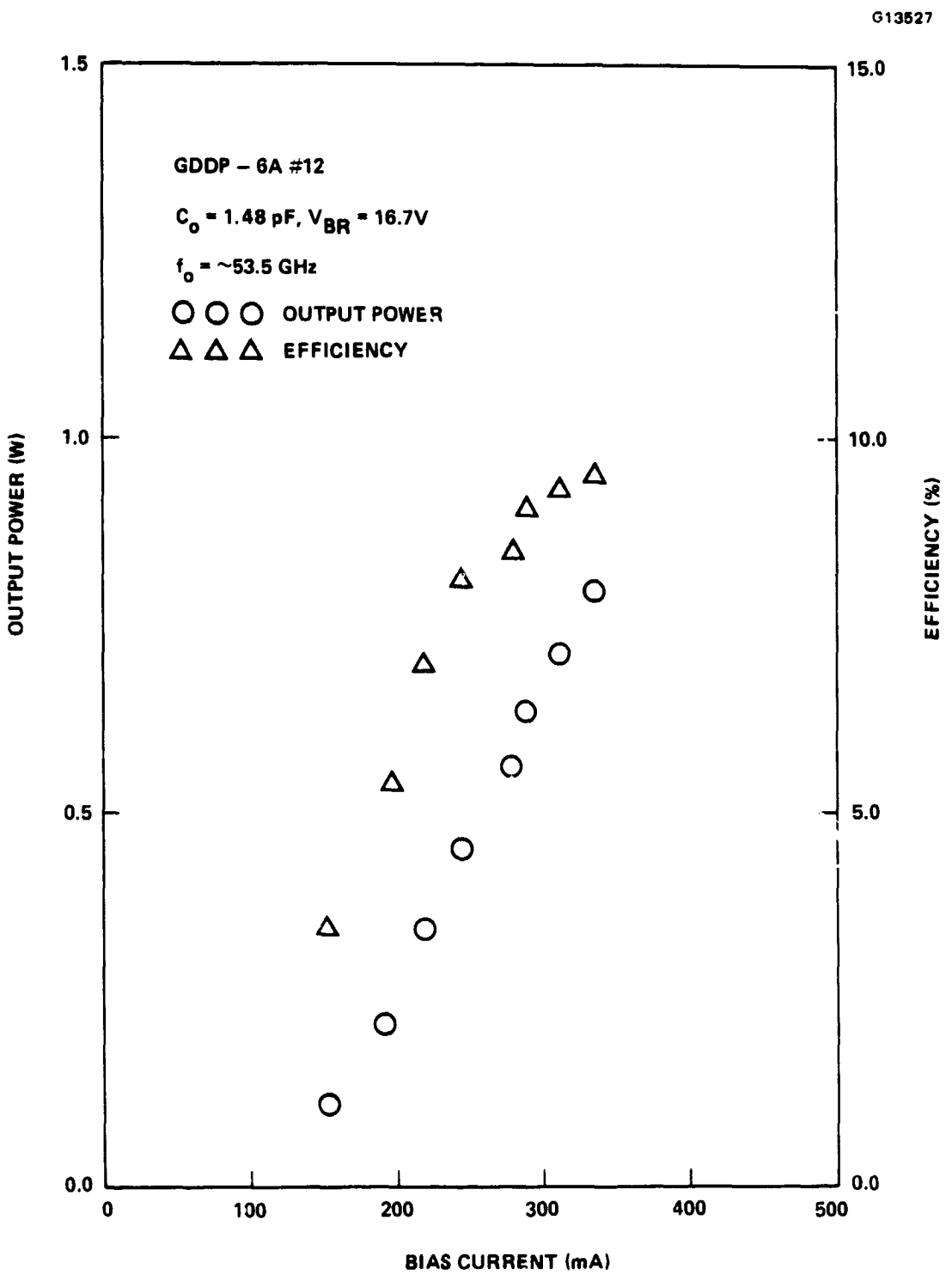


Figure 50 RF performance of a V-band GaAs DD flat IMPATT diode.

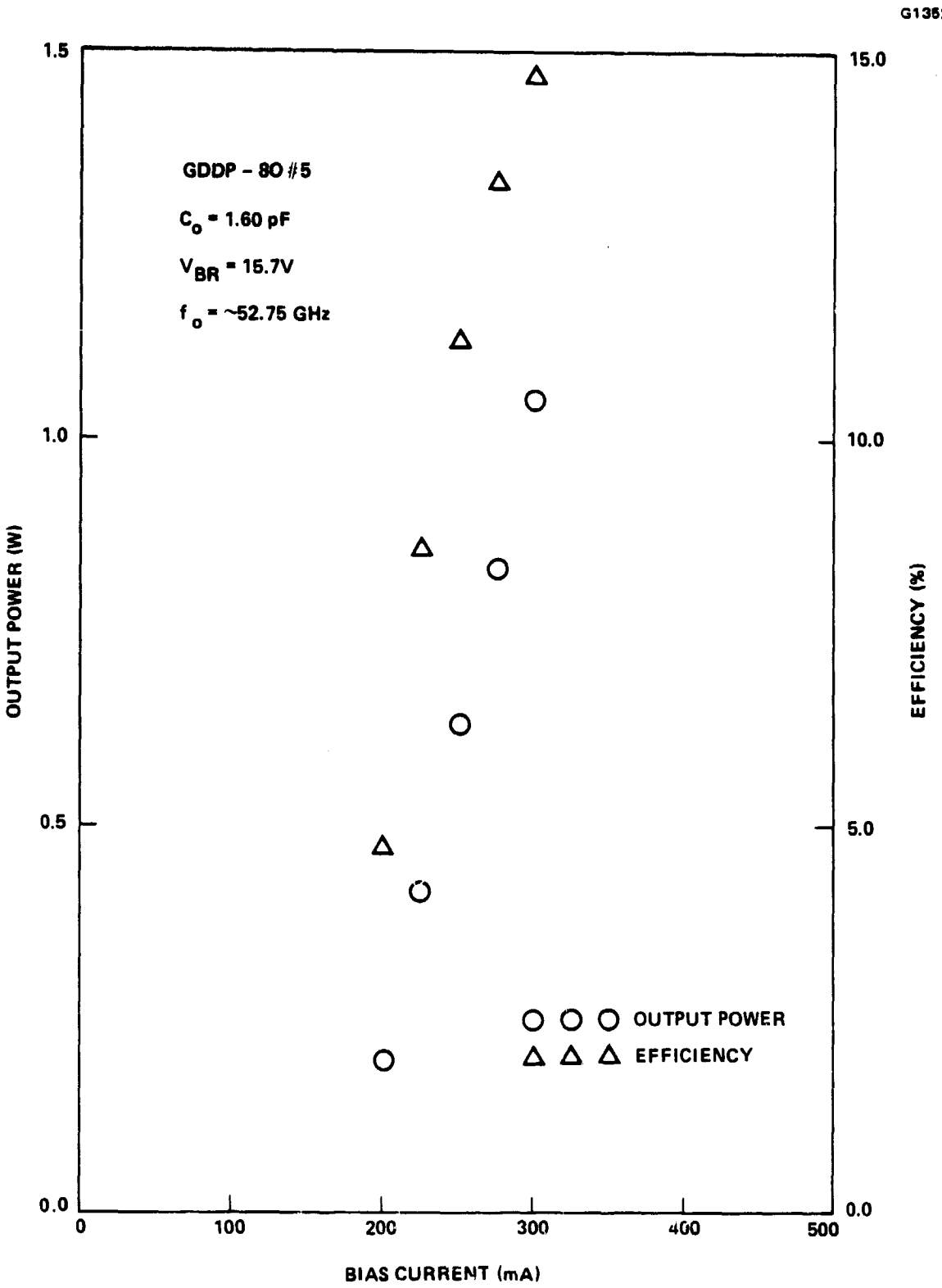


Figure 51 RF performance of a V-band GaAs DD hybrid IMPATT diode.

hi-lo profiles in both p and n sides) structures. Many diodes fabricated from these wafers (many of which showed a n^{++} spike between substrate and the buffer layers) showed poor breakdown characteristics and burned out prematurely in RF test. The diodes from three DD hybrid wafers (with flat p and lo-hi-lo n profiles), however, showed sharp breakdown characteristic and generated output power up to 1 W with 10 to 12 percent conversion efficiency. The highest output power obtained from a DD Read diode was 500 mW with 8.6 conversion efficiency.

The last batch of Perkin-Elmer MBE wafers were grown around the end of the program and only a couple of the wafers were processed. We obtained 750 mW around 55 GHz with 12 percent efficiency in the preliminary evaluation of these diodes.

Several MBE wafers grown at the University of Southern California and Hughes Research Laboratories (HRL) in Malibu in the early stage of the program were processed for plated heatsink diodes. The measured doping profiles of these wafers were not quite as close to the design values. These diodes generated no significant output power in RF evaluation. We obtained maximum 500 mW with 6 percent efficiency from a pill diode on a diamond heatsink fabricated from a MBE wafer grown at HRL. Three DD flat and three DD hybrid (with the hi-lo profile) MBE wafers were grown at Cornell University. When processed into pill diodes, most samples showed sharp breakdown characteristic except the ones fabricated from a DD flat structure. The best RF performance from a DD flat diode was 630 mW output power at 54 GHz with 8.1 percent efficiency. The DD hybrid diodes performed better than the DD flat dlodes. Some of the test results of the DD hybrid diodes are represented in Table 16. The oscillation frequency ranged from 51 GHz to 66 GHz and generally decreased with increasing diode junction capacitance. A conversion efficiency of 14.9 percent was achieved at 60 GHz with 645 mW output power. Output power of 1W was also achieved near 57 GHz with a conversion efficiency of 12.5 percent. The highest oscillation frequency was 66.1 GHz with an output power of 410 mW. These RF performances were obtained at a current density between 13 and 19.3 kA/cm^2. In most cases, the maximum power was thermally limited.

TABLE 16

RF PERFORMANCE OF GaAs DD HYBRID IMPATTS (GDDP-25)

ZERO-BIAS CAPACITANCE (pF)	BREAKDOWN VOLTAGE (V)	BIAS CURRENT (mA)	BIAS VOLTAGE (V)	CURRENT DENSITY (kA/cm^2)	OSCILLATION FREQUENCY (GHz)	OUTPUT POWER (mW)	EFFICIENCY (%)
1.0	14.3	209	22.2	15.9	62.0	630	13.6
1.02	14.4	197	22.1	14.7	60.5	630	14.45
1.07	14.6	214	22.4	15.2	66.1	410	8.5
1.16	14.4	232	22.2	15.2	56.9	760	14.8
1.17	14.4	200	21.7	13.0	60.0	645	14.9
1.22	14.4	284	23.1	17.7	60.2	850	12.9
		310	24.0	19.3	57.4	930	12.5
1.54	14.4	350	22.9	17.3	56.9	1000	12.5
1.55	14.5	347	22.3	17.0	59.5	980	12.7

The RF performance of V-band GaAs IMPATT diodes was very sensitive to circuit tuning, resulting in frequent diode burn-out at low bias currents. The output signal was very clean when the circuit was properly tuned and the diode failure often occurred with signal degradation. The cause of this circuit-related burn-out is not clearly known at this time.

The maximum output power of the diodes appeared to be thermally limited. The diode burn-out temperature is estimated to be 300 to 350°C. As the bias current increased, the output power, at first, increased rapidly and then slowed down. However, in most cases, the output power was still increasing at the diode burn-out point indicating thermal limitation.

5.4 NOISE MEASUREMENT

The AM and FM noise properties of CW oscillation are important parameters for communication systems applications. These noise characteristics can be obtained from the power spectral densities of an oscillator in the neighborhood of the carrier frequency. The noise characteristics of an IMPATT oscillator were very sensitive to bias and circuit conditions.

5.4.1 AM Noise

The experimental setup used for the AM noise measurement of an IMPATT oscillator is shown in Figure 52. In this system, the oscillator output is directly detected by means of a low-noise balanced mixer. The AM noise sidebands are thus translated to video frequencies and the power spectrum of this video signal is amplified by a low noise amplifier and then measured by a selective voltmeter (or wave analyzer). The main function is to build a symmetrical circuit to minimize the differential delay between the two branches of the balanced mixer. The two splitted signals arrived at the mixer with a negligible or no phase difference. Therefore, the noise generated by random phase fluctuation in the two splitted arms will cancel each other. Only the noise generated from the amplitude fluctuation will be detected by the balanced mixer.

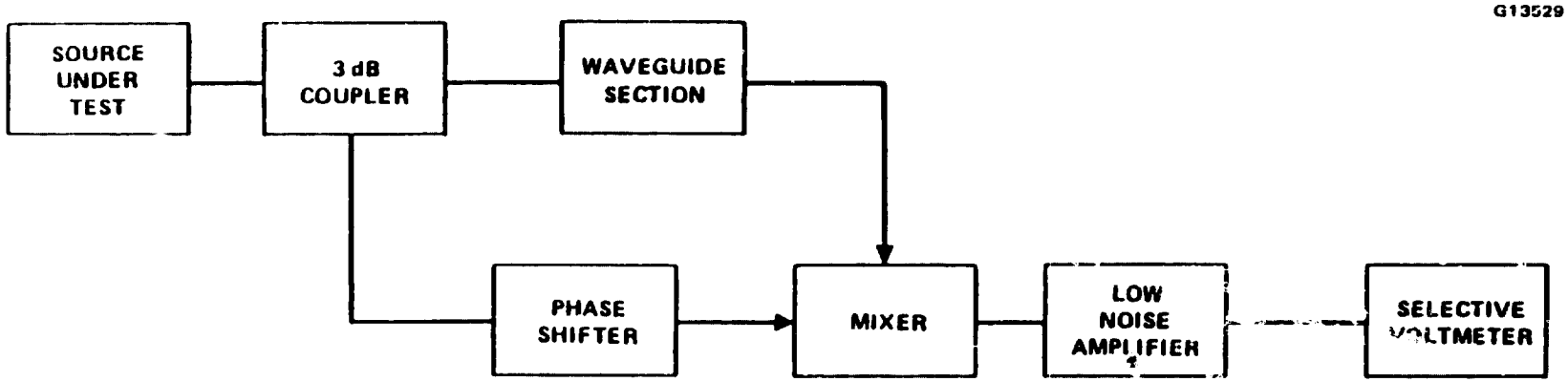


Figure 52 Test setup for IMPATT AM noise measurement.

Figures 53 and 54 show the measured AM noise as a function of frequency from carrier for a V-band GaAs DD flat (GDDP-4) and DD hybrid (GDDP-5) diodes, respectively. In Figure 53, the diode was operated at a bias level of 238 mA with output power of 150 mW. The oscillator cavity was adjusted to get the cleanest signal on a spectrum analyzer at this bias level. The double side band (DBS) signal-to-noise (S/N) ratio of this IMPATT source was about -120 dBc/Hz at 300 Hz from carrier, decreased slowly to -147 dBc/Hz around 100 kHz from carrier and flattened out beyond this point. Figure 54 shows the DSB S/N ratio of a DD hybrid diode with 1 Hz bandwidth under three different bias levels. The oscillator cavity was tuned to get the cleanest signal at the bias current of 250 mA with an output power of 500 mW. The bias level was then reduced to 230 mA and 206 mA without disturbing the cavity. As shown in this figure, the cleanest signal was observed at higher output power level of 500 mW since the cavity was adjusted at this particular bias level. The noise characteristics of the oscillator was sensitive to either bias or circuit condition and could change drastically with a slight tuning.

5.4.2 FM Noise

FM noise is generated from random fluctuations in phase. The test setup for measuring oscillator FM noise is shown in Figure 55. The system is similar to that used for measuring AM noise except for the introduction of a circulator with a section of waveguide and the sliding short. They form a waveguide delay line bridge discriminator which can convert the frequency deviation into a noise voltage. As the two splitted signals arrive at the balanced mixer with 90° out of phase, the amplitude fluctuation of these signals cancel each other. The noise generated by random phase fluctuation is detected by the balanced mixer, amplified by the low noise amplifier and then measured by the selective voltmeter. The measured DSB FM S/N ratios of a DD flat (GDDP-4) and a DD hybrid (GDDP-5) diode are shown in Figures 56 and 57. The diode bias and output power levels were the same as those in AM measurements.

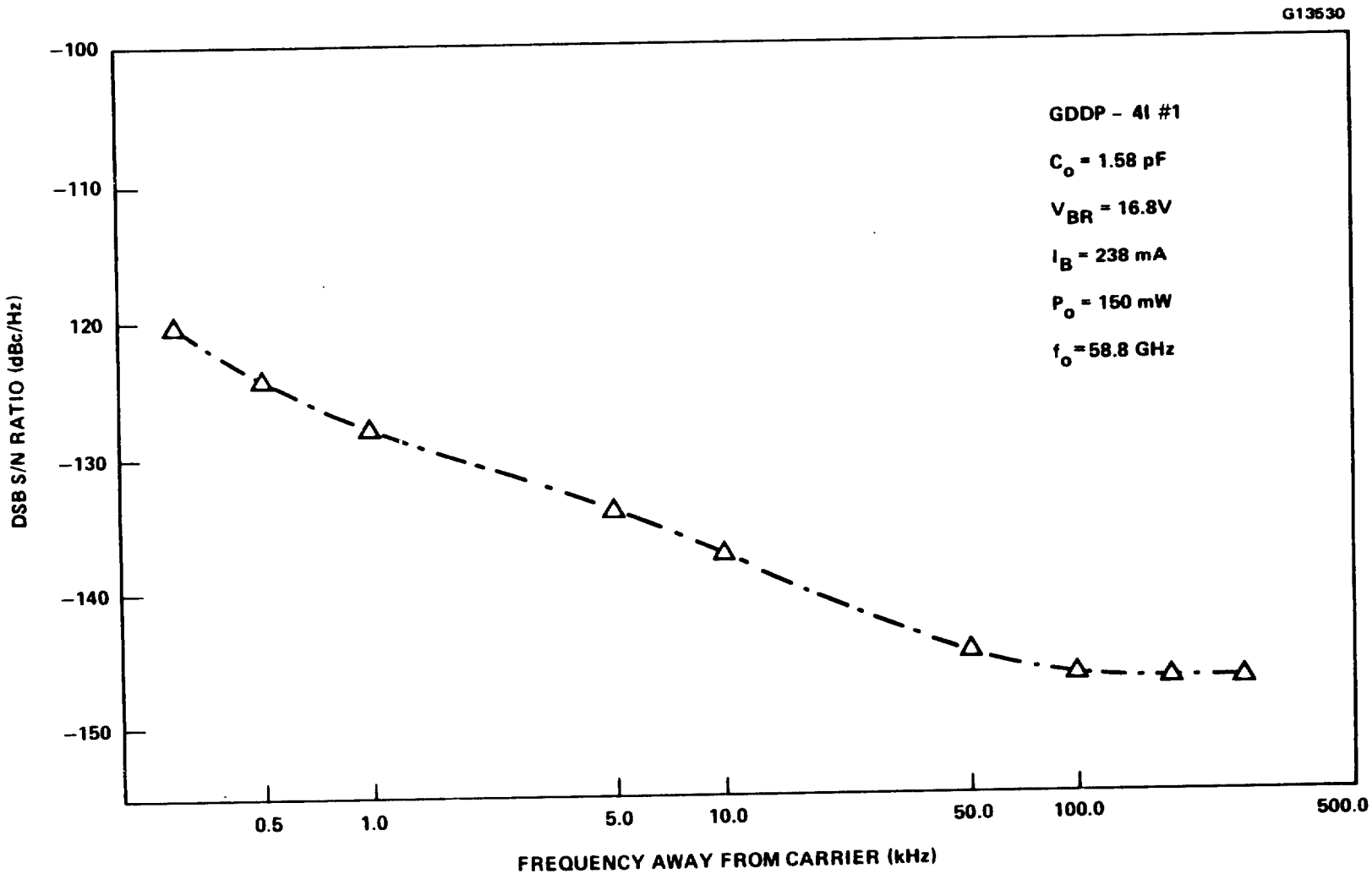


Figure 53 Measured AM noise of a V-band DD flat GaAs IMPATT diode.

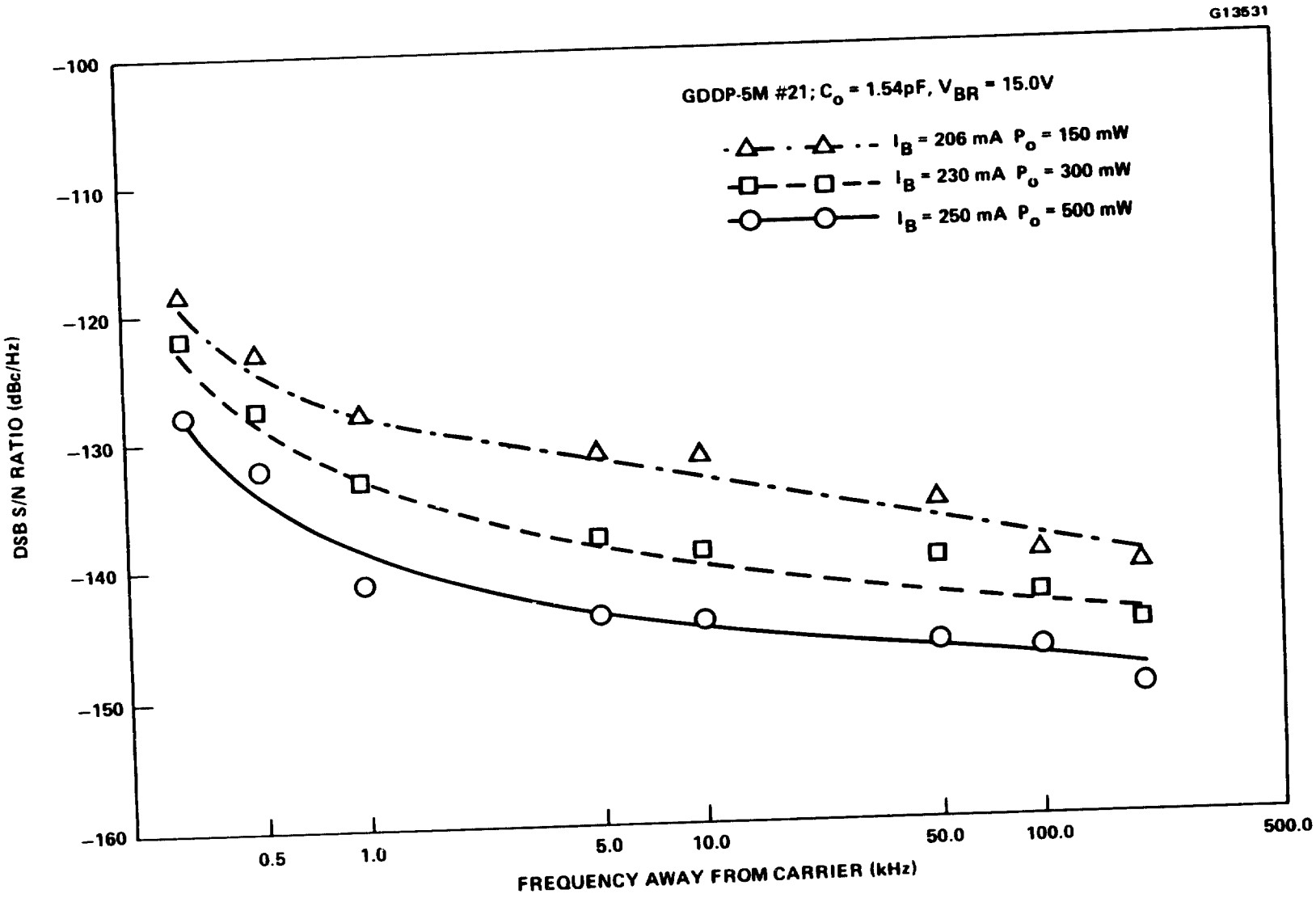


Figure 54 Measured AM noise of a V-band DD hybrid GaAs IMPATT diode.

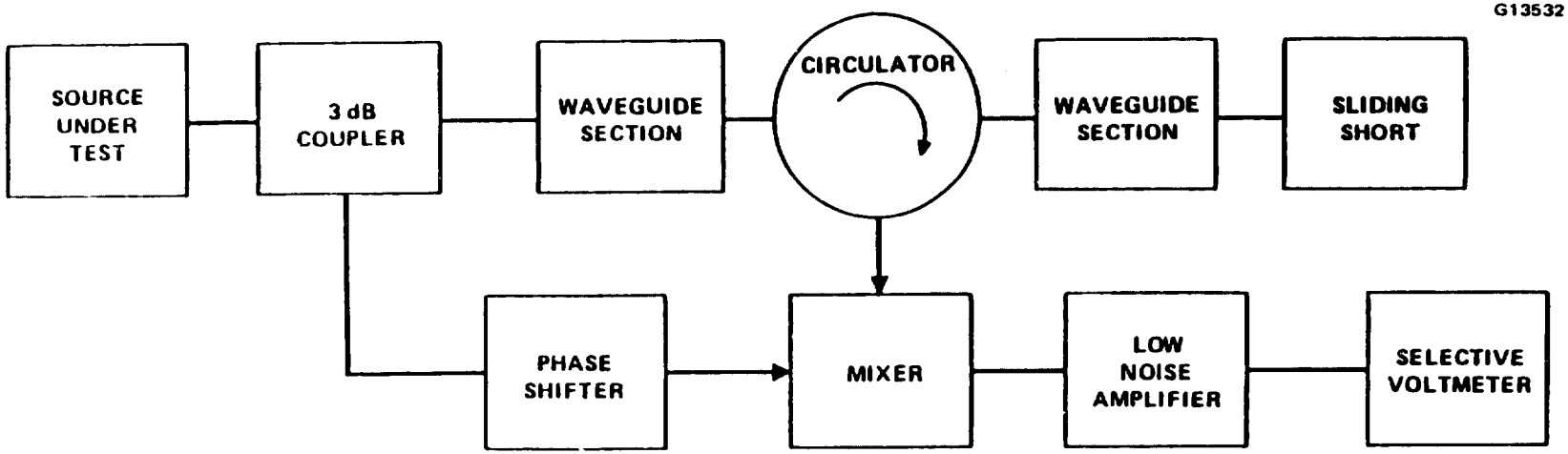


Figure 55 Test setup for IMPATT FM noise measurement.

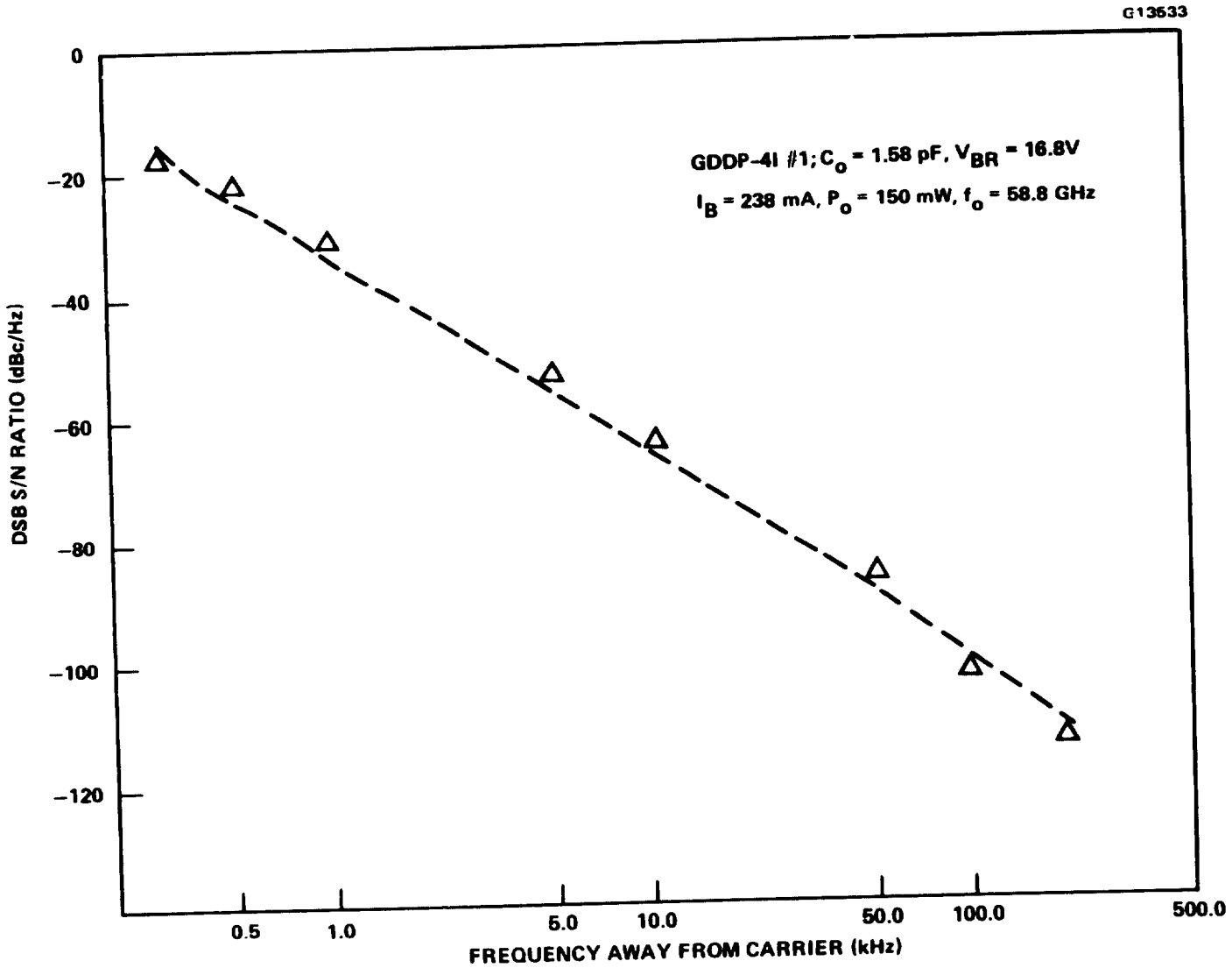


Figure 56 Measured FM noise of a V-band DD flat GaAs IMPATT diode.

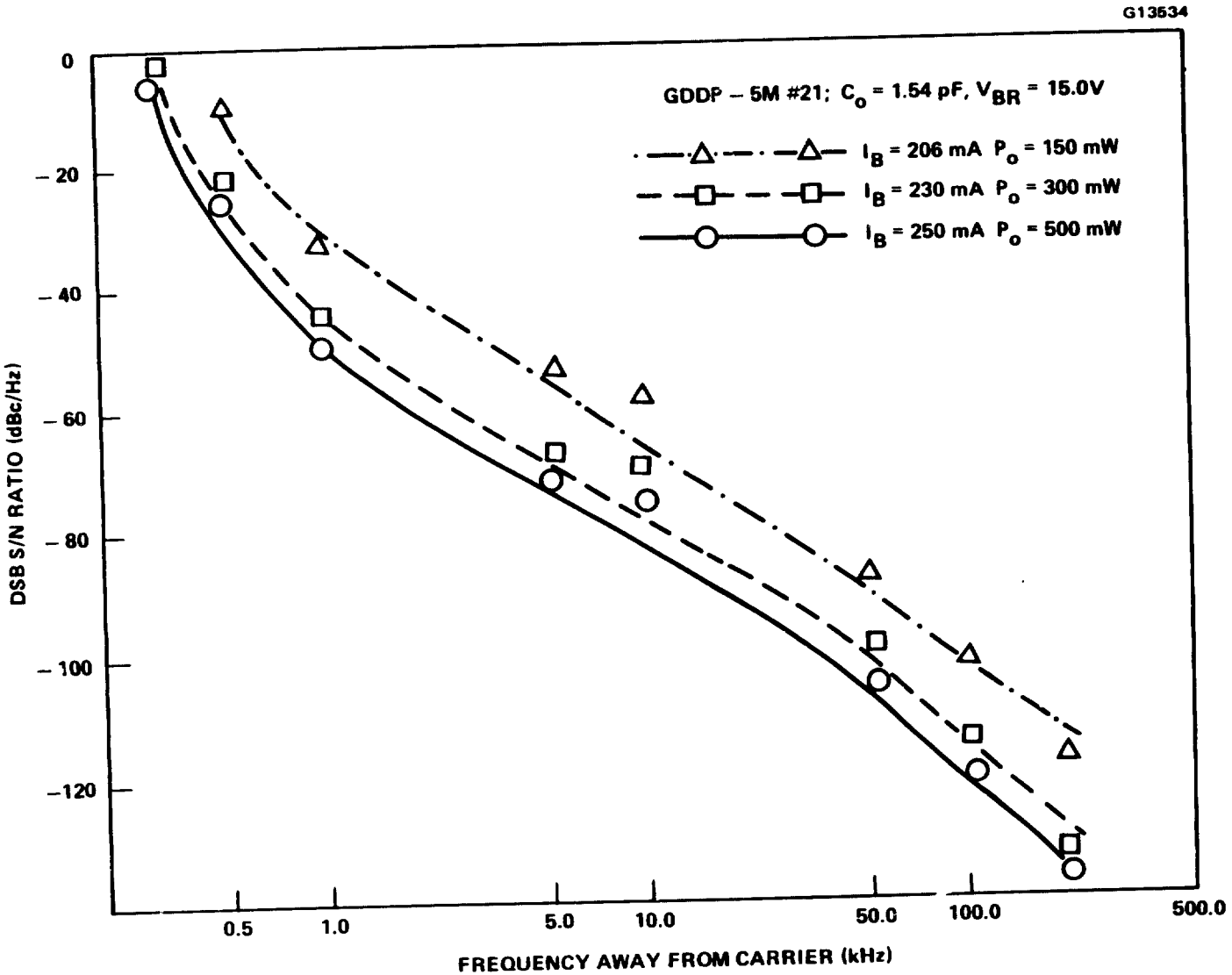


Figure 57 Measured FM noise of a V-band DD hybrid GaAs IMPATT diode.

6.0 RELIABILITY TEST

To obtain adequate information on diode reliability in a reasonable amount of time, accelerated life test methods are used. These techniques can be organized into two general categories: the step-stress test and the constant- stress test.

Under this program, we conducted only the step-stress test for one DD flat (GDDP-6) and two DD hybrid lots (GDDP-8 and GDDP-25). The test was under dc condition with the diodes mounted in a test stand and biased with no RF power generated. This method is much less expensive than testing under RF conditions and proved to be very useful.

In a step-stress test, devices were operated for a fixed period of time at each of a series of increasing stress levels until failure. The specific stress mechanism chosen for IMPATT diodes, as well as most semiconductor devices, was temperature. The purpose is to establish operating stress levels that will accelerate the formation of failure mechanism so that meaningful failures can be generated in a relatively short period of time. The procedure is also useful in determining operational limits and in establishing device screening procedures to eliminate early failures.

6.1 TEST STATION

The test station, which is shown in Figure 58, is designed to permit periodic dc testing without physically removing the diodes from the mounting stand. Each position on the test panel is numbered so that the identity of each diode can be maintained. Figure 59 presents the main components of the station: the dc power supply, individual coarse and fine current-adjust controls, current-limiting resistors, individual V_R/I_R readout jacks, and test diode mounting stand in a dry nitrogen atmosphere. A strip chart recorder continuously monitors the total bias current to the test stations. Changes in the current level indicate a diode's exact failure time.

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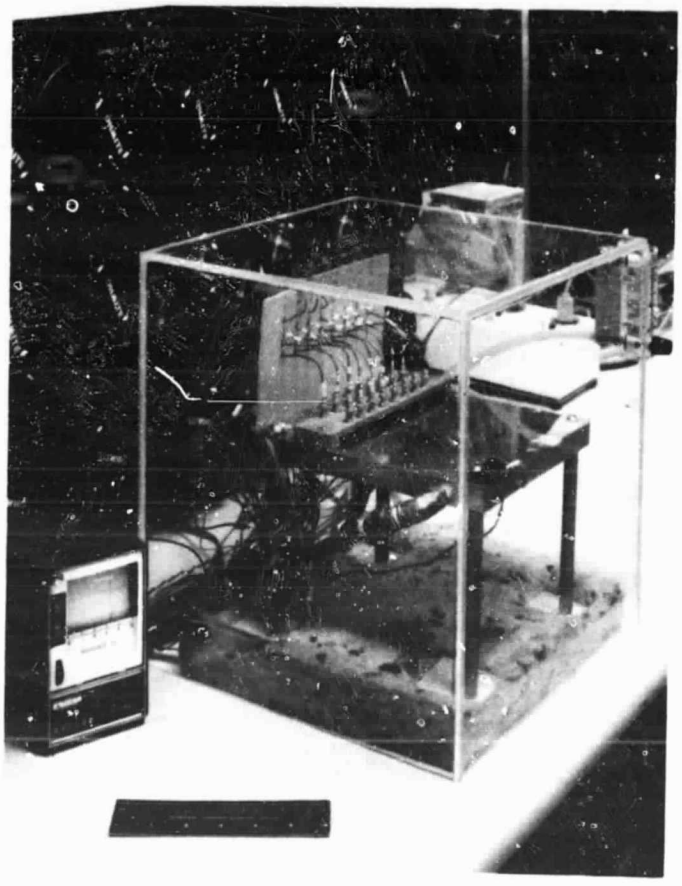

Figure 58 Life test stand with control panel in background.

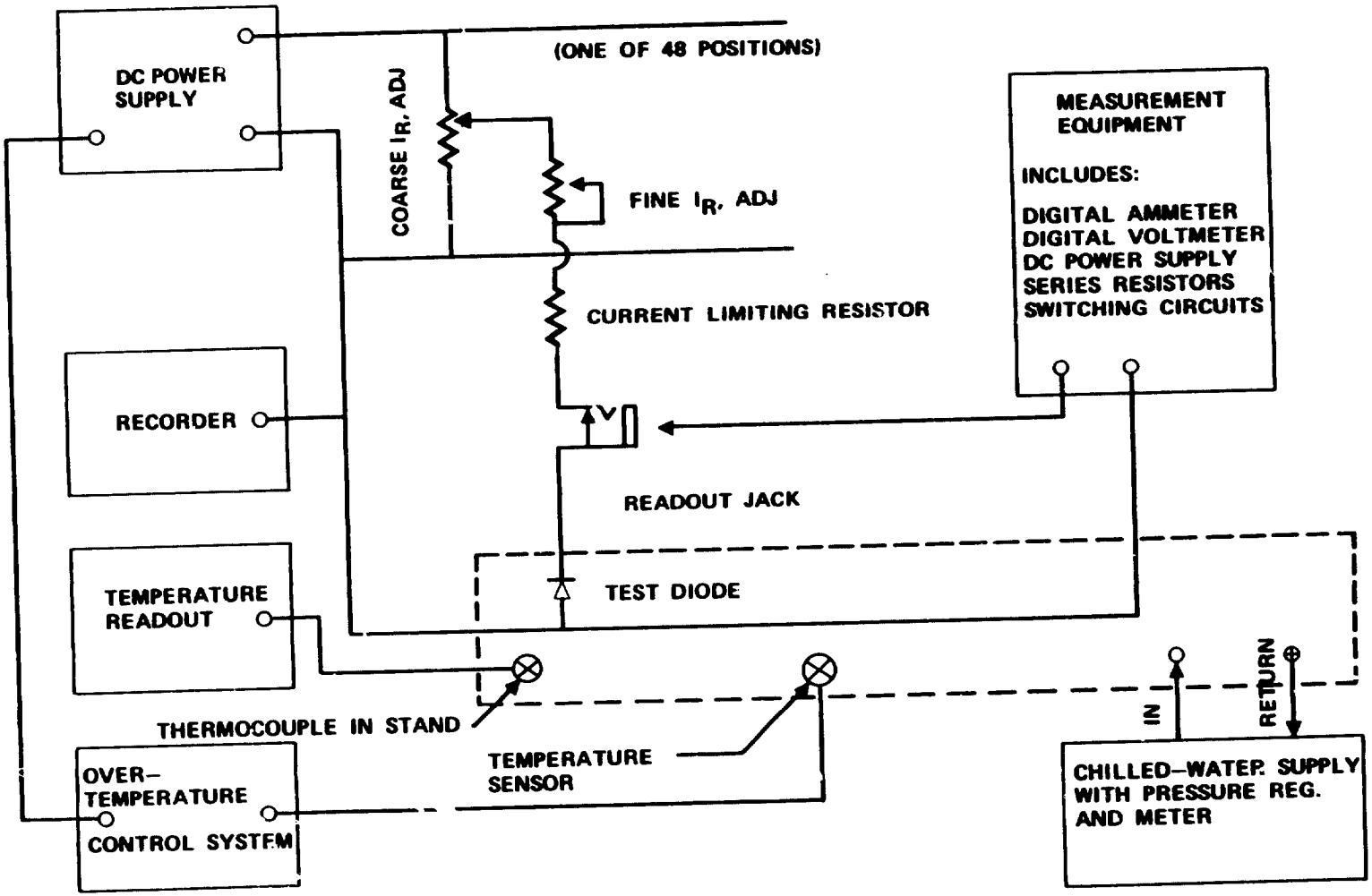

Figure 59 IMPATT diode life test station. Broken lines represent mounting stand (in dry nitrogen atmosphere).

The temperature of the diode test stand is controlled by pressure-regulated chilled water flowing continuously through the channels inside the stand and maintained within $\pm 2^{\circ}C$ from the stabilized temperature. This is measured with a thermocouple embedded into the stand.

To prevent unnecessary damage, the following protective measures were taken: the use of current-limiting resistors which prevent excessive current when a diode shorts, the selection of a dc power supply that has excellent voltage regulation and negligible voltage overshoot in the event of a power outage, installation of an over-temperature control system that reduces power supply voltage to a value less than the breakdown voltage when the temperature of the diode stand exceeds a preset limit, and the use of an alarm and automatic emergency dry nitrogen supply system when the house nitrogen supply is interrupted.

6.2 TEST DESCRIPTION

Before being subjected to a life test, the diodes were screened to eliminate units which would otherwise fail prematurely and distort the normal failure rate. The screening procedure consists of visual mechanical examination and measurement of electrical parameters.

The electrical parameters used to screen diodes include thermal resistance, reverse leakage currents, reverse voltages, and forward voltages. In the past, anomalies in these quantities were correlated with premature diode failure. High thermal resistance can be indicative of a poor thermocompression bond between the diode and heatsink, resulting in excessive localized heating. High leakage current can signify either surface contamination or bulk defects. A high forward voltage drop is associated with a degraded electrical contact at the metal-substrate interface.

The actual life testing of the IMPATT diodes is straightforward. The thermal resistance of each diode was measured and recorded. The diodes were then mounted onto the life test fixtures, where initial electrical data were measured. They were then reverse-biased into avalanche breakdown. The bias

current was adjusted so that the product of the dc power dissipated with the measured thermal resistance equalled the desired operating junction temperature rise above ambient. Once all the diodes in a group were operating, the test was underway and the operating time accumulated. The diodes were then operated continuously for 72 hours. During this time, the operating conditions were monitored and recorded. If a diode opened or shorted, the time-to-failure was recorded. After 72 hours, the power was removed and the initial electrical measurements were repeated and recorded. The surviving diodes were then brought up to the next step junction temperature with 25° increment and the operating test was continued. This 72-hour cycle was repeated until all the diodes failed.

The data measured and recorded during each life test were as follows:

1. Recorded initially and periodically after each 72-hour step.

    a. Reverse voltages (V_R) at 1, 10 and 100 mA.
    b. Reverse current (I_R) at 1 V less than V_{BR} at 1 mA.
    c Forward voltages (V_F) at 1, 10 and 100 mA.

2. Monitored daily.

    a. Date, time and total test hours.
    b. Test stand temperature.
    c. V_R and I_R of each diode at the life test power level.

3. Time of failure.

The time of diode failure was recorded by the strip chart recorder monitoring the total test fixture current with a resolution of 15 minutes. The identity (serial number) of the failed diode was obtained during the next daily monitor of each diode.

6.3 STEP-STRESS TEST

The step-stress test was performed on a total of 38 diodes, 13 diodes each from GDDP-6 and GDDP-8 lots and 12 diodes from GDDP-25 lot. (One of the GDDP-25 diodes was mistakenly recorded as shorted during the test and discounted.) The GDDP-6 diodes have DD flat structure and the GDDP-8 and GDDP-25 diodes possess DD hybrid structure with flat P and hi-lo n profiles. The GDDP-6 and GDDP-8 diodes were metallized by Au-Zn on the epi (P^{++}) side while the GDDP-25 diodes by Pt-Ti-Pt-Au. The metallization of substrate (n^{++} side of all diodes was Au-Ge-Ni-Au. All the diodes were mounted on diamond heatsinks inside quartz-ring packages with cross-strap ribbon configuration. The zero-bias capacitance was chosen around 1.5 pF at which value the optimum RF performance of the diode was achieved. We started the step-stress test at 200°C. The junction temperature was raised by 25° increment until all diodes failed. The test duration at each step was 72 hours.

The test results are shown in Figures 60 through 62 for diode lots GDDP-6, GDDP-8, and GDDP-25, using histograms indicating the failed diodes at each temperature. Failures for these tests were taken to be catastrophic, i.e., either short- or open-circuited diodes. All the test diodes failed by shorting. The V-band GaAs IMPATTs failed over wide range of junction temperature. However, majority of the failures for GDDP-6 (DD flat) and GDDP-8 (DD hybrid) diodes with Au-Zn metallization on the epi side occurred around 350°C while the majority of GDDP-25 diodes (DD hybrid) with Pt-Ti-Pt-Au metallizat on failed between 400 and 425°C. The main reason for this discrepancy was the difference in thermal resistance. The measured thermal resistance of the diodes with Pt-Ti-Pt-Au metallization was higher by about 50 percent compared to the same size diodes with Au-Zn metallization as described in Section 5.2. The maximum failure temperature corresponded to the input power of 7.5 to 8.0 W for all diodes from three different lots. According to the results of the step-stress tests, the failure of V-band GaAs IMPATTs appeared to be pretty much process-related and strongly depended on diode fabrication process.

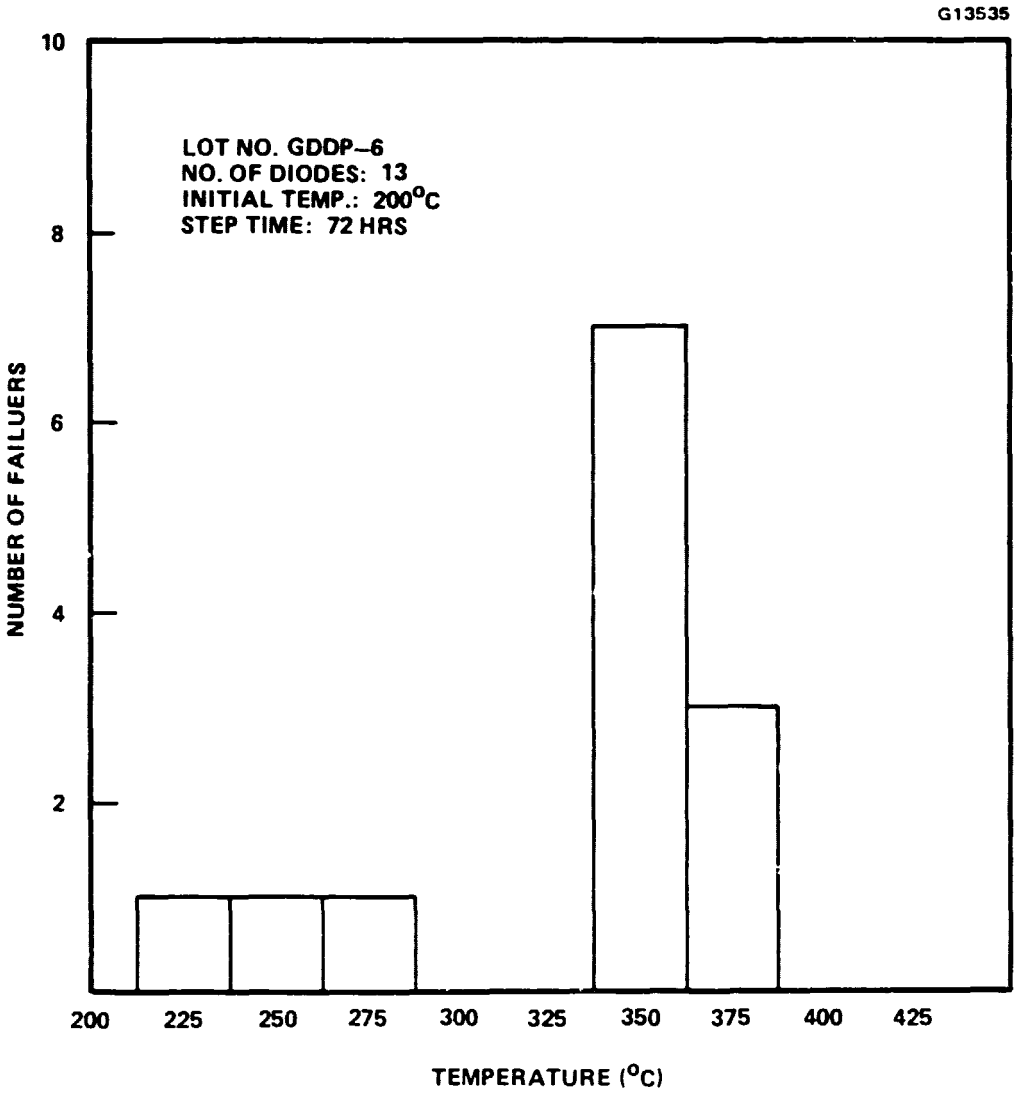

Figure 60 Step-stress test histogram for lot GDDP-6.

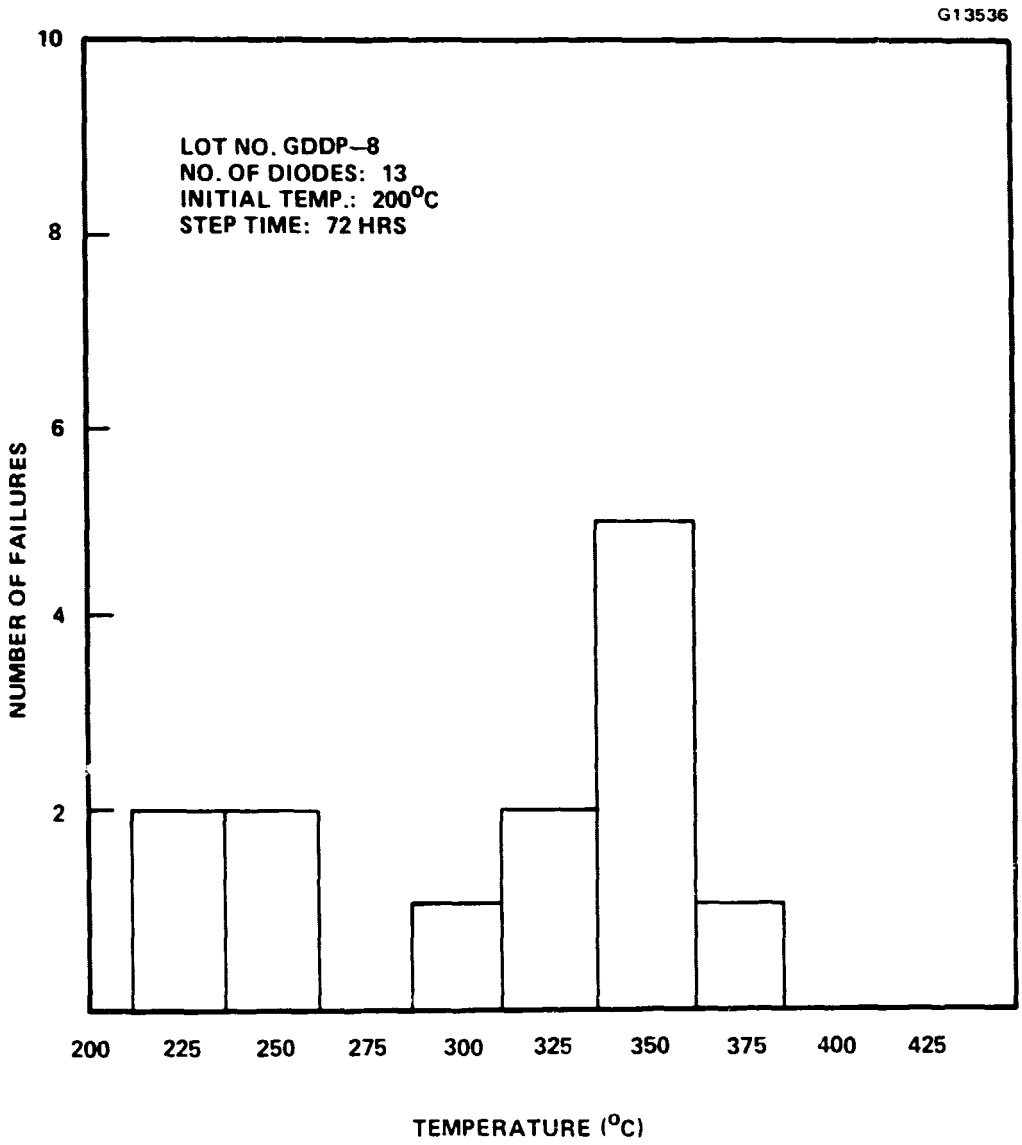

Figure 61 Step-stress histogram for lot GDDP-8.

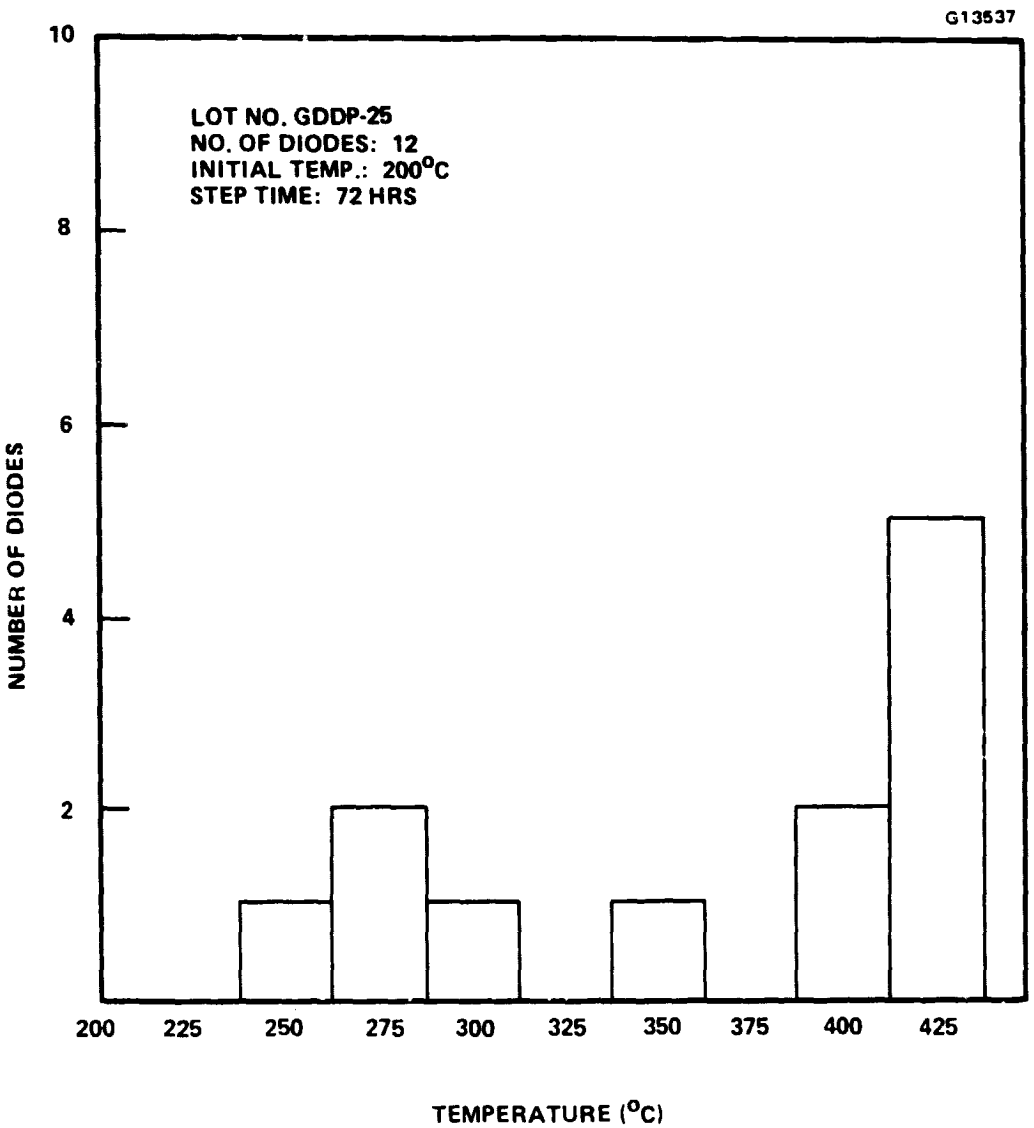

Figure 62 Step-stress histogram for lot GDDP-25.

6.4 FAILURE ANALYSIS

Whether circuit-related or thermally limited, the failure mode of V-band GaAs IMPATTs occurred in RF evaluation was predominantly shorting. The rare diode failures by opening seemed mostly related with power transient in the bias circult. Several failed diodes in RF evaluation were subjected to failure analysis. The cap of the package was removed and the diode was examined under a scanning electron microscope (SEM). In general, diodes with initial sharp breakdown characteristic showed a small melted area on the perimeter of the diode. Figure 63 shows SEM photographs of a shorted diode with a preformed ribbon. A melted spot that caused the diode failure can be seen at the perimeter of the diode. The failure mechanism seemed to be similar among the failed diodes at different bias levels. An interesting note is that the diode chip has a rectangular shape rather than a circular shape due to uneven diode etching beneath the preformed ribbon. The SEM photographs of a shorted diode with a gold wire (1 mil diameter) ribbon are shown in Figure 64. A melted spot is shown in the lower left corner of Figure 64(a). Enlargement of this region is shown in Figure 64(b). Diodes with poor breakdown characteristic often showed a melted spot in an area other than the perimeter. In Figure 65(a), the shorted area appears to be a melted gold protrusion near the center of the diode. Figure 65(b) shows the enlargement of this area. SEM photographs of an opened diode are shown in Figure 66. As shown in these photographs, both the diode and ribbons were melted away in most cases. According to SEM photographs, the actual junction diameter of the diodes was about 10 percent smaller than obtained by optical measurement.

To investigate the diode failure, a couple of the failed diodes from three different lots subjected to step-stress tests were examined under a microscope. Although many diodes showed a cracked quartz ring, nothing was unusual on the surface in our visual inspection. Next, we carefully removed the metal cap, contact ribbon and quartz ring and examined each portion under a SEM to investigate any anomaly the in diode package. Figure 67 shows the SEM pictures taken at this stage. When being checked at this stage, two of the six diodes revealed normal breakdown characteristics while the remaining four diodes indicated shorting. The cause of the shorting of the two diodes appeared to be the excess

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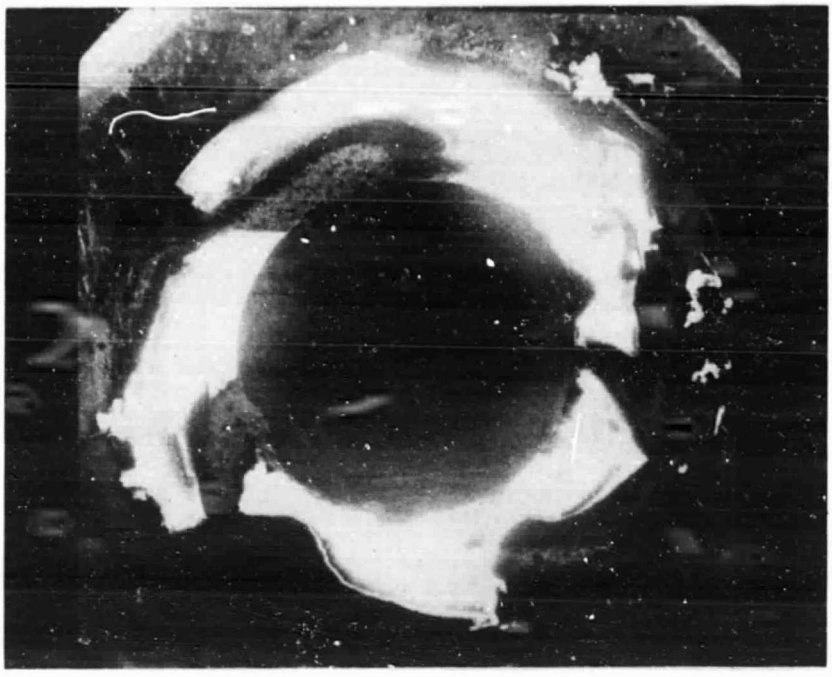
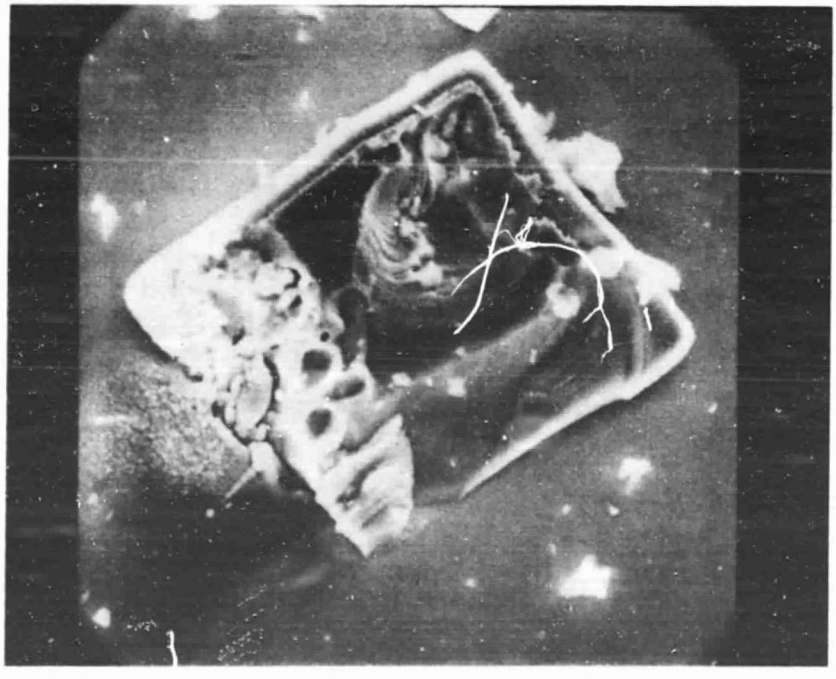


(a)



(b)

Figure 63 SEM photographs of a shorted GaAs IMPATT diode with a preformed ribbon.

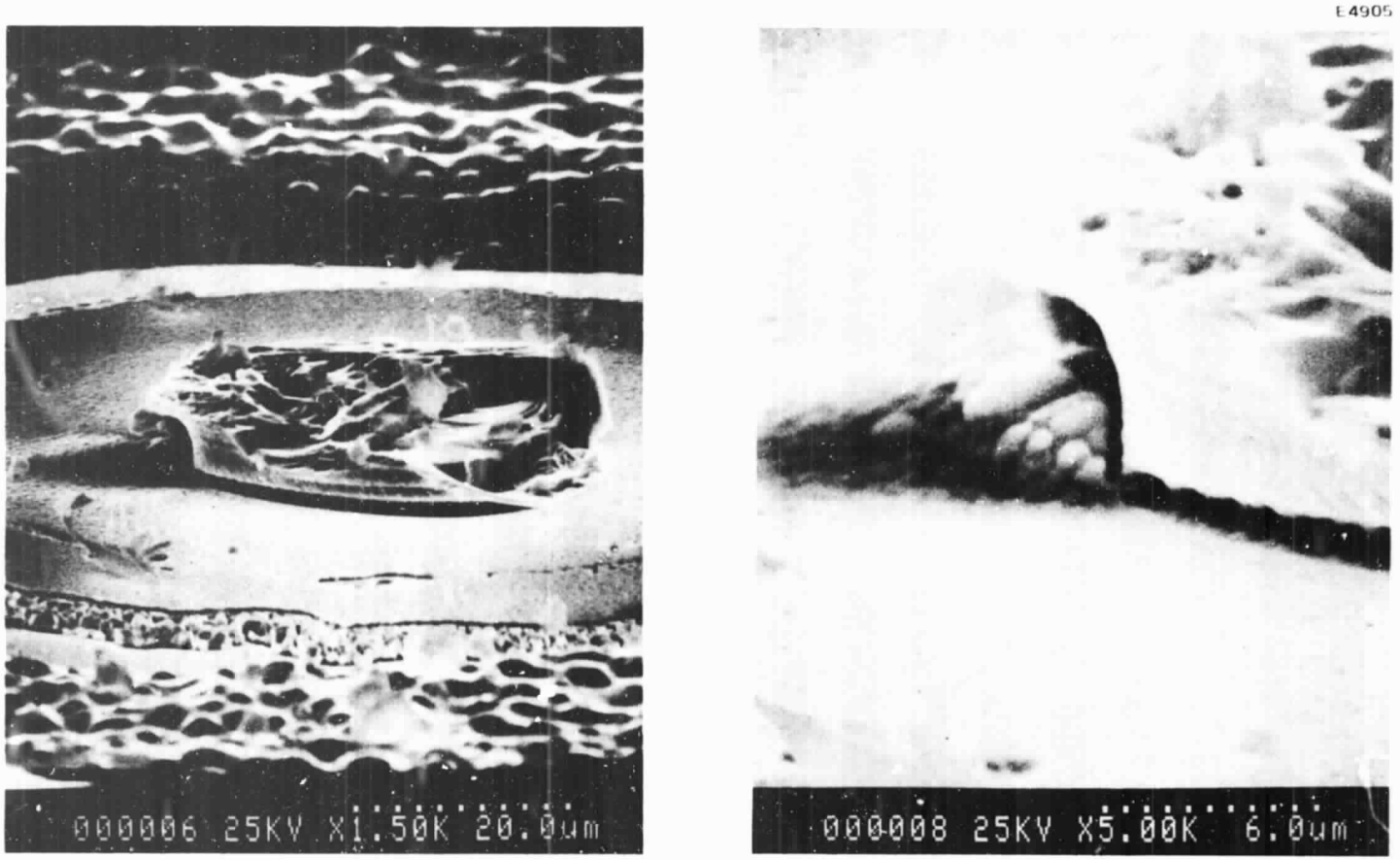


Figure 64 SEM photographs of a shorted GaAs IMPATT diode with a gold wire ribbon.

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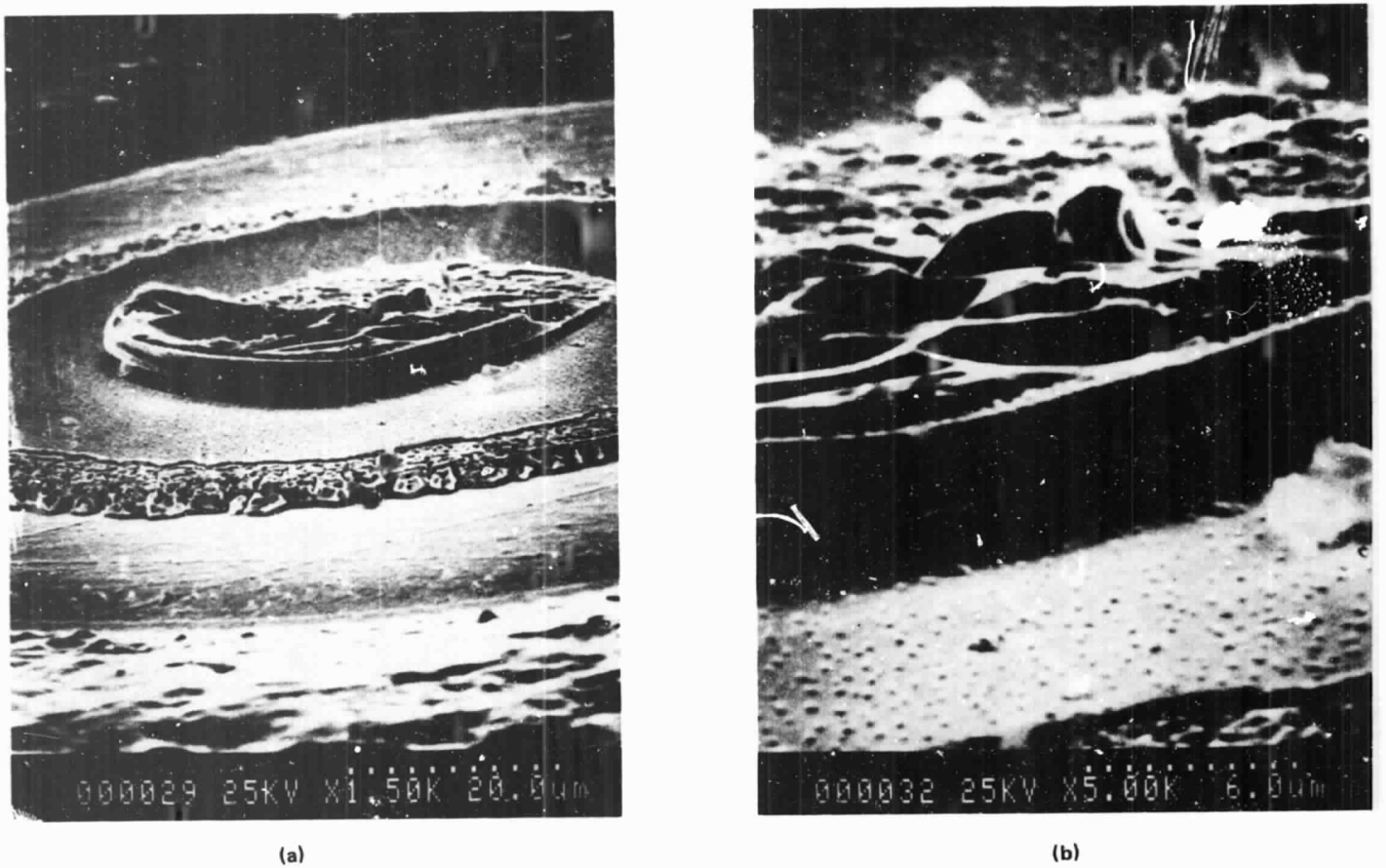
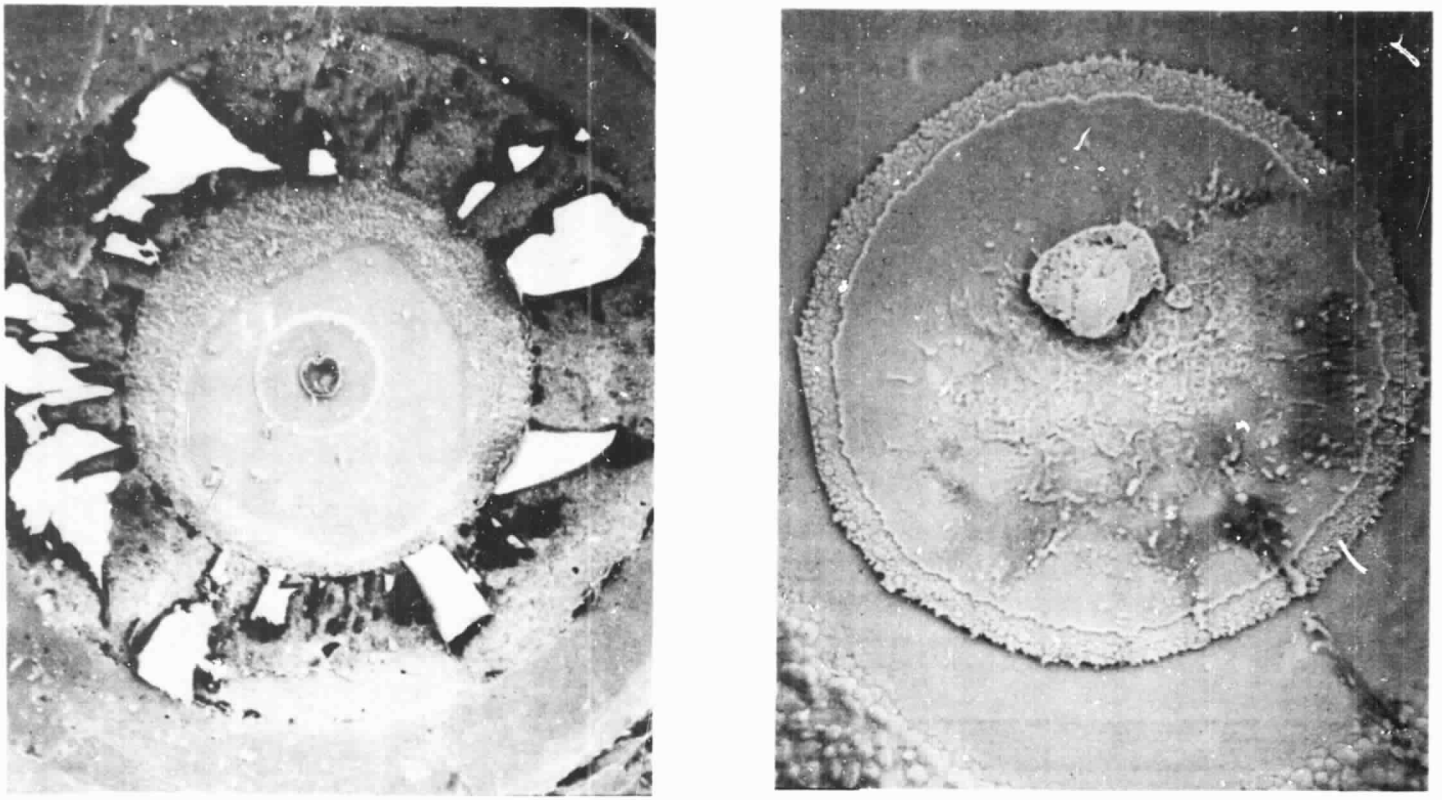


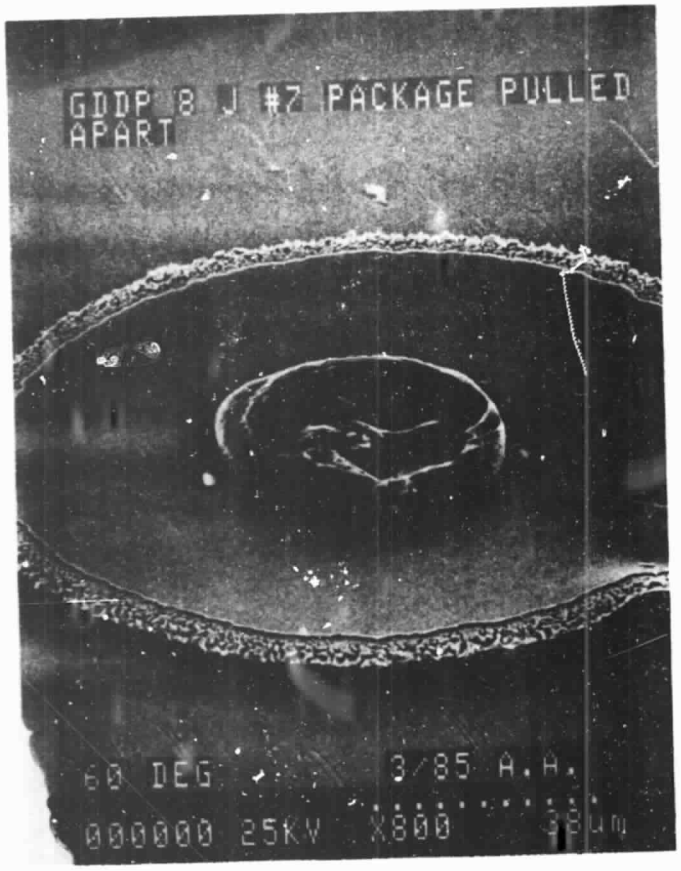
(a) (b)

Figure 65 SEM photographs of a shorted GaAs IMPATT diode with poor breakdown characteristic.

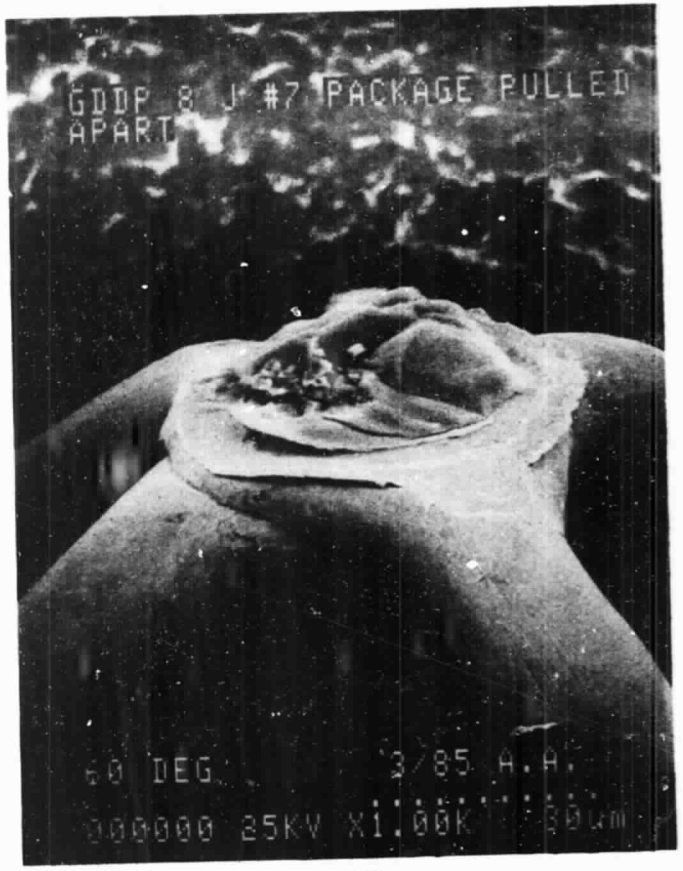


(a) (b)

Figure 66 SEM photographs of an opened GaAs IMPATT diode.



(a)



(b)

Figure 67 SEM photographs after the metal cap, contact ribbon, and quartz ring are removed.

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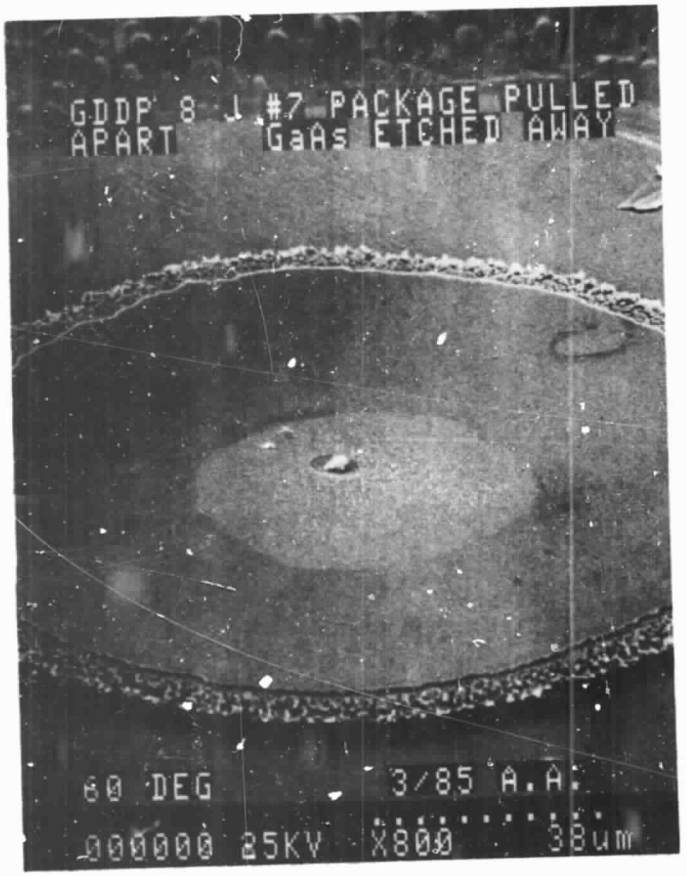
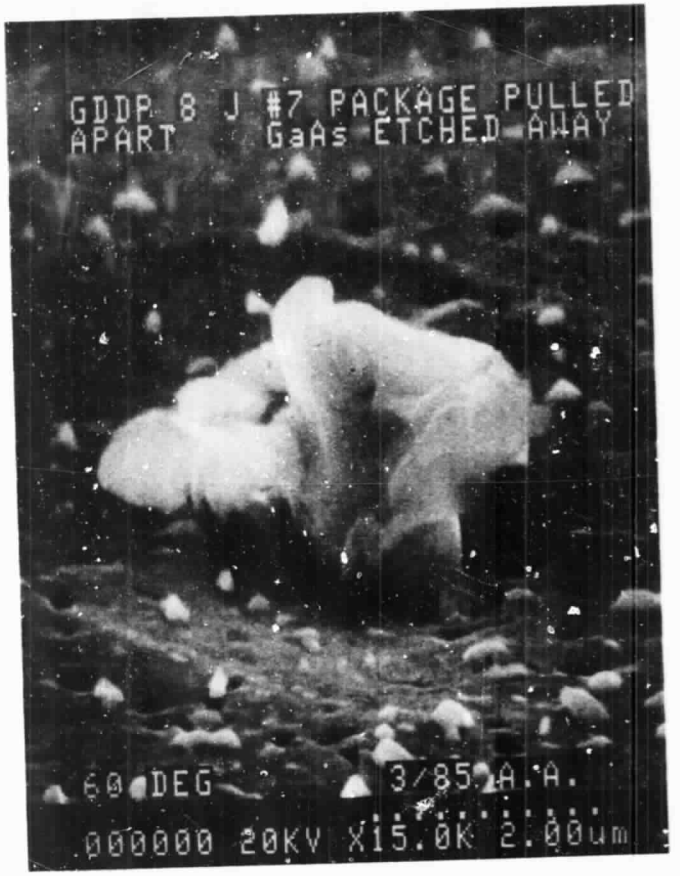
metal overhang on top of the diode chip. Then we etched away the GaAs chip. We found no suspicious areas on the two diodes which showed normal breakdown characteristics. The remaining four diodes showed melted spot(s) between the diode and heatsink which caused the diode failure. An example is shown in Figure 68. The bright gold spike causing the diode to short is clearly visible.



(a)



(b)

Figure 68 SEM photographs of a failed GaAs IMPATT diode subjected to failure analysis in which the GaAs material was etched away.

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7.0 PROGRAM DELIVERABLES

According to the program schedule, a total of 40 V-band GaAs IMPATT diodes have been delivered to the contract office along with the test data of each diode. A test circuit was also delivered with the related documents at each delivery.

7.1 IMPATT DIODES

The first delivery diodes were developed based on our initial design. These diodes were fabricated from double-drift hybrid MBE wafers in plated heatsink configuration. Table 17 represents test data of the five GaAs IMPATT diodes. One of the IMPATT diodes was mounted in the oscillator cavity. The best output power was 100 mW with 2.5 percent conversion efficiency. The oscillation frquency was just above 50 GHz.

The second delivery diodes were pill diodes on diamond heatsinks. All five diodes were selected from a DD hybrid MBE lot. The RF performance data of these diodes are shown in Table 18. Minimum output power of 500 mW was achieved with a conversion efficiency greater than 10 percent. By comparing Table 18 with Table 17, substantial performance improvement can be seen. The diode data were obtained using the same test cavity with only the sliding short adjusted for tuning purpose.

The third delivery diodes were selected from the GDDP-5 lot, same as the second delivery diodes. However, by increasing bias current beyond 300 mA, output power around 1 W was achieved with a conversion efficiency greater than 12 percent as shown in Table 19.

At the end of the program, 25 V-band GaAs IMPATTs were delivered to the contract office. All the diodes were selected from a DD hybrid lot, GDDP-8. The dc and RF characteristics of these diodes are shown in Tables 20 and 21. These diodes have zero-bias capacitance from 1.51 to 1.64 pF with an average thermal resistance of 35°C/W. Typical output power was 1.0 W with a 12.9 percent effieciency with an average junction temperature rize of 236°C.

TABLE 17

TEST DATA OF FIRST DELIVERY V-BAND GaAs IMPATTS

Diode Ser. No.	Diode Lot No.	Zero-Bias Capacitance (pF)	Breakdown Voltage (V)	Bias Current (mA)	Bias Voltage (V)	Oscillation Frequency (GHz)	Output Power (mW)	Efficiency (%)
1	MBED-8	1.34	18.8	233	25.6	53.0	75	1.3
2*	MBED-9	1.10	18.9	152	26.3	52.6	100	2.5
3	MBED-9	1.50	19.8	155	25.5	50.4	90	2.3
4	MBED-10	1.28	19.6	160	27.2	50.1	90	2.1
5	MBED-11	1.31	18.6	192	25.6	50.4	75	1.5

*Mounted in the cavity

TABLE 18

TEST DATA OF SECOND DELIVERY V-BAND GaAs IMPATTS

Diode Ser. No.	Diode Lot No.	Zero-Bias Capacitance (pF)	Breakdown Voltage (V)	Bias Current (mA)	Bias Voltage (V)	Oscillation Frequency (GHz)	Output Power (mW)	Efficiency (%)
6*	GDDP-5	1.51	15.0	240	22.0	56.1	575	10.9
7	GDDP-5	1.46	15.0	212	21.2	55.4	500	11.1
8	GDDP-5	1.43	15.0	216	21.7	55.9	525	11.2
9	GDDP-5	1.56	15.2	217	21.7	55.6	500	10.6
10	GDDP-5	1.56	15.0	230	21.6	56.0	510	10.3

*Mounted in the cavity

TABLE 19

TEST DATA OF THIRD DELIVERY V-BAND GaAs IMPATTS

Diode Ser. No.	Diode Lot No.	Zero-Bias Capacitance (pF)	Breakdown Voltage (V)	Bias Current (mA)	Bias Voltage (V)	Oscillation Frequency (GHz)	Output Power (mW)	Efficiency (%)
11	GDDP-5	1.50	15.0	329	24.45	54.8	1000	12.5
12*	GDDP-5	1.50	15.1	309	23.7	53.4	900	12.3
13	GDDP-5	1.50	15.1	327	24.5	54.7	960	12.0
14	GDDP-5	1.55	14.9	339	24.75	53.1	1025	12.2
15	GDDP-5	1.56	15.0	327	24.2	54.9	1000	12.6

*Mounted in the cavity.

TABLE 20

DC CHARACTERISTICS OF FINAL DELIVERY V-BAND GaAs IMPATT DIODES

IMPATT Diode		Zero-Bias Capacitance (pF)	Breakdown Voltage (V)		Forward Voltage (V)		Reverse Leakage Current (μA)	Thermal Resistance (°C/W)
Ser. No.	Lot No.		at 1 mA	at 10 mA	at 1 mA	at 10 mA		
16	GDDP-8	1.52	15.750	16.033	1.285	1.609	<1.0	35.3
17	GDDP-8	1.57	15.794	16.145	1.169	1.358	<1.0	41.6
18	GDDP-8	1.58	15.761	16.044	1.138	1.241	<1.0	35.0
19	GDDP-8	1.58	15.826	16.163	1.152	1.333	<1.0	36.6
20	GDDP-8	1.59	15.601	15.835	1.287	1.631	<1.0	32.5
21	GDDP-8	1.59	15.552	15.843	1.184	1.370	<1.0	33.5
22	GDDP-8	1.60	15.826	16.093	1.215	1.509	<1.0	34.1
23	GDDP-8	1.60	15.826	16.146	1.167	1.356	<1.0	36.1
24	GDDP-8	1.60	15.839	16.146	1.162	1.331	<1.0	33.5
25	GDDP-8	1.60	15.965	16.246	1.251	1.556	<1.0	33.4
26	GDDP-8	1.60	15.890	16.248	1.161	1.361	<1.0	38.6
27	GDDP-8	1.60	15.720	16.012	1.186	1.411	<1.0	33.4
28*	GDDP-8	1.60	15.459	15.731	1.142	1.250	<1.0	32.6
29	GDDP-8	1.61	15.642	15.875	1.331	1.668	<1.0	33.1
30	GDDP-8	1.61	15.883	16.185	1.205	1.471	<1.0	33.4

*Mounted in the cavity.

TABLE 20 (Continue)

DC CHARACTERISTICS OF FINAL DELIVERY V-BAND GaAs IMPATT DIODES

IMPATT Diode		Zero-Bias Capacitance (pF)	Breakdown Voltage (V)		Forward Voltage (V)		Reverse Leakage Current (μA)	Thermal Resistance (°C/W)
Ser. No.	Lot No.		at 1 mA	at 10 mA	at 1 mA	at 10 mA		
31	GDDP-8	1.61	15.841	16.168	1.155	1.305	<1.0	34.3
32	GDDP-8	1.62	15.852	16.108	1.362	1.699	<1.0	34.4
33	GDDP-8	1.62	15.606	15.829	1.459	1.769	<1.0	33.3
34	GDDP-8	1.62	16.030	16.377	1.142	1.297	<1.0	35.5
35	GDDP-8	1.62	15.702	15.990	1.175	1.370	<1.0	33.9
36	GDDP-8	1.62	15.900	16.229	1.156	1.303	<1.0	35.6
37	GDDP-8	1.63	15.798	16.127	1.153	1.287	<1.0	37.4
38	GDDP-8	1.63	15.796	16.042	1.363	1.684	<1.0	33.6
39	GDDP-8	1.63	16.079	16.409	1.145	1.291	<1.0	35.2
40	GDDP-8	1.64	15.639	15.906	1.210	1.495	<1.0	34.0

TABLE 21

RF CHARACTERISTICS OF FINAL DELIVERY V-BAND GaAs IMPATT DIODES

IMPATT Diode		Bias		Oscillation Frequency (GHz)	Output Power (mW)	Efficiency (%)	Junction Temperature Rise (°C)
Ser. No.	Lot No.	Current (mA)	Voltage (V)				
16	GDDP-8	0.304	24.18	53.4	1000	13.6	224
17	GDDP-8	0.293	24.67	52.8	1000	13.8	259
18	GDDP-8	0.315	24.67	53.0	1000	12.8	237
19	GDDP-8	0.306	24.60	52.7	1000	13.3	239
20	GDDP-8	0.320	23.37	51.7	960	12.8	212
21	GDDP-8	0.321	24.11	53.4	1000	12.9	226
22	GDDP-8	0.316	24.35	52.7	1000	13.0	228
23	GDDP-8	0.318	24.85	50.7	1000	12.7	249
24	GDDP-8	0.325	24.53	52.8	1000	12.5	234
25	GDDP-8	0.312	24.16	51.4	1000	13.3	218
26	GDDP-8	0.307	24.98	52.8	1000	13.0	257
27	GDDP-8	0.297	23.74	52.8	1000	14.2	202
28*	GDDP-8	0.320	23.49	52.0	1000	13.3	212
29	GDDP-8	0.335	22.77	51.2	1000	12.6	230
30	GDDP-8	0.317	24.60	53.0	1000	12.8	227

*Mounted in the cavity.

TABLE 21 (Continued)

RF CHARACTERISTICS OF FINAL DELIVERY V-BAND GaAs IMPATT DIODES

IMPATT Diode		Bias		Oscillation Frequency (GHz)	Output Power (mW)	Efficiency (%)	Junction Temperature Rise (°C)
Ser. No.	Lot No.	Current (mA)	Voltage (V)				
31	GDDP-8	0.312	24.30	52.5	1000	13.2	226
32	GDDP-8	0.325	24.35	52.1	1000	12.6	238
33	GDDP-8	0.330	23.28	51.1	1000	13.0	223
34	GDDP-8	0.311	24.79	51.2	1000	13.0	238
35	GDDP-8	0.328	24.40	52.7	1000	12.5	237
36	GDDP-8	0.333	25.04	51.?	1000	12.0	261
37	GDDP-8	0.350	25.69	56.2	1025	11.4	298
38	GDDP-8	0.335	24.63	53.0	1000	12.1	244
39	GDDP-8	0.330	24.95	51.2	1050	12.8	253
40	GDDP-8	0.325	24.05	52.8	1000	12.8	232

7.2 IMPATT OSCILLATOR

The test circuit for the delivery diodes was the coaxially coupled reduced-height waveguide cavity shown in Figure 44. The test data of delivery IMPATTs was obtained by tuning the test circuit for optimum RF performance for each diode. At each delivery, at least one diode was shipped as mounted in the cavity for an easy check of the test data. The IMPATT oscillator was pretuned for optimum RF performance inside the cavity. (The bias choke was glued to the bias slab and the tuning short was locked using a set screw.) An isolator was connected at the output port of the cavity to minimize the loading effect. An air-cooling system is recommended for operation of the socillator.

7.2.1 Operation of IMPATT Oscillator

Using a test setup shown in Figure 49, the diode RF performance can be measured as follows:

1. Set the current and voltage control knobs of a power supply at zero position before connecting the power supply to an IMPATT oscillator. An ammeter between the power supply and the oscillator and a voltmeter across the oscillator can be connected to monitor the operating bias current and voltage of the IMPATT oscillator.

2. Connect the power supply to the IMPATT oscillator for right polarity (positive to the center conductor). A crowbar box may also be introduced in parallel with the IMPATT oscillator.

3. Turn on the power supply.

4. Set the voltage control knob of the power supply beyond the operating bias voltage by 2 to 3 volts.

5. Turn slowly the current control knob of the power supply to increase the bias current to the specified value.

The oscillator must generate the RF performance specified in the data sheet. If the oscillator does not generate the specified RF performance.

6. Unlock the set screw and adjust slightly the tuning short for optimum performance.

7.2.2 Diode Replacement and Optimization

The IMPATT diode in the delivery oscillator can be replaced through the hole at the bottom of the cavity. This can be done by removing the threaded plug without disassembling the cavity. The replacement steps are outlined below:

1. Remove the threaded plug at the bottom of the cavity.

2. Remove the diode to be replaced. (If the diode does not drop with the plug, it may be taken out with a tweezer.)

3. Insert a new diode to be tested.

4. Tighten the threaded plug. Do not overtighten.

After replacement, the new diode can be optimized through the following procedure:

1. Set the current and voltage control knobs of a power supply at zero position before connecting the power supply to the oscillator.

2. Connect the power supply to the IMPATT oscillator for right polarity (positive to the center conductor).

3. Turn on the power supply.

4. Set the voltage control knob of the power supply beyond the operating bias voltage by 2 to 3 volts.

5. Turn slowly the current control knob of the power supply to increase the bias current to around 160 mA.

6. Adjust the tuning short for maximum output power.

7. Increase the bias current of the oscillator until the output power saturates.

8. Adjust the tuning short very slowly for maximum output power. Care must be taken to avoid any sudden drop of the output power which may cause diode failure. Move the sliding short in slightly until the output power drops about a couple tenth of a dB.

9. Repeat Steps 7 and 8 until the bias current of the oscillator reaches to the specified value. At this current level, adjust the tuning short for maximum output power.

8.0 CONCLUSIONS AND RECOMMENDATIONS

We have made significant advance in V-band GaAs IMPATT technology. Progresses have been made in diode design, material growth and wafer processing areas. As a result, we achieved state-of-the-art performance from double-drift (DD) GaAs IMPATTs at V-band frequencies. CW output power of 1W was obtained at 52.75 GHz with 14.7 percent conversion efficiency at a junction temperature of 228°C. The highest output power demonstrated at V-band was 1.12 W and the best conversion efficiency was 15.3 percent.

We have designed DD flat, DD hybrid, and DD Read structures. Initial doping profiles of the V-band GaAs IMPATTs were based on the small-signal analysis and the scaling of the IMPATT profiles designed for operation at lower frequencies. These profiles were modified later with the results of large-signal analysis as well as the feedback information gained in RF evaluation of the previously designed IMPATT diodes.

We grew GaAs materials using molecular beam epitaxy (MBE) as a primary approach and vapor phase epitaxy (VPE) as a back-up. MBE provided excellent doping control. According to secondary ion mass spectrometry (SIMS) analysis, MBE wafers revealed good doping density uniformity in each layer with sharp transitions between layers. Despite our intensive efforts, we were not able to grow qualified wafers using VPE. The growth rate of VPE was too fast to grow the complicated doping profiles with submicrometer layer thicknesses. VPE wafers indicated graded transitions with less uniform doping concentration in each layer.

We believe that two techniques we applied in wafer processing were particularly instrumental for the successful development of the V-band GaAs IMPATTs. One was the reduction of the GaAs wafer thickness to less than 10 μm. This reduced the diode series resistance and produced well-defined mesa configuration, which permitted higher bonding pressure during thermocompression (TC)-bonding a diode to a heatsink. The number of diode chips available from a wafer in pill configuration was substantially higher than the number in plated heatsink configuration. By TC-bonding the diodes on diamond heatsinks, the thermal

resistance of the pill diodes was reduced by as much as 50 percent compared to that of the plated heatsink diodes.

We have experimented different metallizations including Ti-Au, Pt-Ti-Au, Pt-Ti-Pt-Au, and Au-Zn for the contact on the epitaxial side of the wafer. For the ohmic contact on the substrate side we relied on Au-Ge-Ni-Au metallization. When a Schottky contact was made directly on n-type material of single-drift (SD) structure, the diodes often indicated poor breakdown characteristic and burned out prematurely in RF evaluation. Although sharp breakdown was achieved by depositing a p-layer before metallization, the RF performance of the SD diodes was limited to a couple hundred milliwatts output power.

The measured thermal resistance of the diodes with Au-Zn metallization was lower than that of the diodes with Pt-Ti-Pt-Au on the epi side. However, the diodes with Au-Zn metallization were also burned out at lower junction temperatures. It appeared that the metallization of the wafer has direct bearing on the thermal resistance and reliability of the diodes.

The RF evaluation of the diodes was conducted in a coaxially coupled reduced-height waveguide cavity. Over a half watt output power was obtained at V-band from DD GaAs IMPATT diodes of different profiles; DD flat, DD hybrid, and DD Read diodes. However, DD hybrid diodes thus far have produced the best RF performance. Typical performance of a diode from a good diode lot was 0.8 to 1.0 W output power with 12 to 13 percent efficiency at a junction temperature around 260°C. The RF performance and the noise characteristics of the V-band GaAs IMPATTs were sensitive to bias and circuit condtions. We experienced frequent diode failure while tuning the circuit even at low bias current levels. The diode failure was often accompanied with significant noise degradation. However, the maximum output power of the diode appeared to be thermally limited. When properly tuned, the measured double side-band (DSB) AM signal to noise (S/N) ratio was about -120 dBc/Hz at 300 Hz from carrier and reduced to about -140 dBc/Hz at 200 kHz from carrier. The DSB FM S/N ratio reduced from about -10 dBc/Hz at 300 Hz from carrier to about -115 dBc/Hz at 300 kHz from carrier.

We performed dc step-stress test on sample V-band GaAs IMPATTs selected from one DD flat and two DD hybrid diode lots. Unlike silicon IMPATTs, GaAs diodes failed over a wide temperature range. This may indicate more process-related diode failure of GaAs IMPATTs. The maximum failure temperature of the diodes with Au-Zn metallization on the epi side was 375°C while that of the diodes with Pt-Ti-Pt-Au metallization was 425°C.

We anticipate further improvement in RF performance of the V-band GaAs IMPATTs. Double-drift GaAs IMPATTs with lo-hi-lo profiles could generate better performance since the lo-hi-lo profile can provide a more confined avalanche region than the hi-lo profile. Large-signal analysis with well defined material parameters will be useful in determining the optimum profiles of these structures. According to a recent study, 1.5 W CW output power can be achieved at 60 GHz with 22 percent efficiency, and close to 1.0 W CW output power at 94 GHz with 18 percent efficiency from DD Read GaAs IMPATT diodes in ideal conditions.

Material growth of the V-band GaAs IMPATTs was singled out as one of the most critical area for successful development of V-band GaAs IMPATTs. The complicated doping profiles with submicrometer layer thicknesses of 60 GHz GaAs IMPATTs were taxing even for the most advanced material growth techniques. Although MBE has demonstrated the capability of excellent doping profile control, more work has to be done to improve the uniformity within a wafer and the repeatability among wafers.

Scanning electron microscope (SEM) examination of the V-band GaAs IMPATT diodes revealed non-uniform surfaces on the periphery after trim-etch, which may be the cause of many diode failures. Techniques to eliminate this non-uniformity can be investigated to provide more uniform current density across the diode. The quality of the metallization has a direct bearing on diode thermal resistance and its RF performance.

Different metallizations can be investigated to provide good thermal conduction with minimum electrical contact resistance. Optimum metallization and bonding conditions can also be examined. Because of tensive stresses in films, pill diodes have been made from a small section of wafers. The present pill process

must be refined to reduce tensitive stress, thus allowing pill diode fabrication from larger size wafers.

The diode reliability is directly related to the operating junction temperature and the maximum output power of a V-band GaAs IMPATT diode is thermally limited. The thermal resistance of the diode can be further reduced by using a ring geometry structure rather than the conventional solid circular structure. However, process modification may be required to achieve a well defined ring structure with such dimensions as those required in V-band frequency operation. The reliability of the diodes must be well established to be eligible for systems applications. Preliminary results of the step-stress test indicate that many diode failures of GaAs IMPATTs are process-related. We strongly recommend more systematic reliability test on V-band GaAs IMPATT diodes to identify the failure mechanism and to establish the life expectancy of the diodes.

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