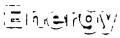
DOE/CS/54209-27(Vol.1) (DE85017586)

NASA-CR-176118 19850026022



EVALUATION OF SEMICONDUCTOR DEVICES FOR ELECTRIC AND Final Report

HYBRID VEHICLES (EHV) AC-DRIVE APPLICATIONS

By F. C. Lee D. Y. Chen M. Jovanovic D. C. Hopkins

March 25, 1985

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EVALUATION OF SEMICONDUCTOR DEVICES FOR ELECTRIC AND HYBRID VEHICLE (EHV) AC-DRIVE APPLICATIONS Final Report

Volume I March 25, 1985

Prepared for

JET Propulsion Laboratory California Institute of Technology Pasadena, CA. 91109

> Contract No. 956684 RE- 1521170

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7.3	Conclusions and Recommendations

1.0 INTRODUCTION

This report summarizes the results of evaluation of power semiconductor devices for electric hybrid vehicle AC drive applications. Three types of power devices were evaluated in the effort: high power bipolar or Darlington transistors, power MOSFETs and asymmetric silicon control rectifiers (ASCR). In the past five years, the advancement made in these three device technology is truly remarkable. Not only the performances of the devices are improved significantly but also the prices are reduced substantially. The Bipolar transistors, including discrete device and Darlington devices, ranges from 100 A to 400 A in current rating and from 400 V to 900 V in voltage rating. These devices are currently used by many equipment manufacturers as key switching elements inverters for AC motor drive applications. Power MOSFETs, on the other hand, are much smaller in current rating as compared to BJT. For the 400 V device, the current rating is limited to 25 A. For the main drive of an electric vehicle, device paralleling is normally needed to achieve practical power level. For other EV related applications such as battery charger circuit, however, MOSFET is advantagous to other devices because of drive circuit simplicity and high frequency capability. Asymmetrical SCR is basically a SCR device and needs commutation circuit for turn-off. However, the device poses several advantages. Those are low conduction drop and low cost.

The primary objectives of the evaluation are threefold:

- 1. To evaluate these devices from the point of view of electric car applications.
- 2. To provide important data that are normally not available or not

complete from the manufacturer's data sheet.

To present the result in user-oriented format so that proper choice
of devices and selection of drive conditions can be easily
achieved.

Because of various tests involved and large amounts of data generated in this report, a description of the organization of the report will be given below for readers' convenience. The report is divided into two volumes. Volume I describes the major tasks, test method and conclusions. Volume II summarizes the mass data generated, including the oscillograms, plots etc. Volume I consists of seven chapters. To provide those readers who are only interested in the project overview, key results are summarized in Chapter 2. Chapters 3 to 5 deal with bipolar transistors. In Chapter 3, six sets of device parameters are evaluated: Switching time, power losses, static characteristics, reverse recovery of diodes, device paralleling etc. In Chapter 4, reverse-biassecond breakdown capabilities of power transistors are evaluated. A unique nondestructive secon-breakdown tester, constructed and tested at Virginia Polytechnic Institute & State University (VPI&SU) was used to evaluate these devices. In Chapter 5, several base-drive circuit hardwares were evaluated, including a "smart" proportional current drive circuit developed at VPISSU. The results of MOSFET evaluation are presented in Chapter 6, and ASCR results are presented in Chapter 7.

In Volume II, the data are presented according to the chapter sequence of Volume I. The figures and tables in this volume are often referred in the text of Volume I.

2.0 SUMMARY OF KEY RESULTS

A large volume of test results have been generated during this phase of investigation. For the benefit of the readers perspective before belaboring with the details, some key results were extracted and summarized here to provide a quick overview. The summary presented here are based on detailed test results and/or investigators observations. In some cases it is rather difficult to quantize the device properties and rank them in the order of preference as many readers wish to see. As you know each device often has its own strength and weakness. It is difficult to draw a line in a subjective manner. The choice of device is often done based on the users familiarity with the device and often is dictated by the particular application and circumstance. For these reasons, and observations are given in general statements. If the reader is interested in finding out some specific details, one should refer to the main text in Volume I and the supporting test results in Volume II.

The summary will be presented according to the following subjects.

- 1. Bipolar Transistors
- 2. Base Drive Circuit
- 3. Power FETs
- 4. Asymmetrical SCRs

2.1 BIPOLAR TRANSISTOR EVALUATION

Table 2.1 summarizes the features of the devices evaluated. A total of 11 devices were evaluated.

2.1-1. Switching Time

Table 2.2 gives a rough classification of the switching speed of the devices evaluated. Except for one device (Westinghouse DAl1503008), the measured data agree well with the spec. provided by the manufacturers.

2.1-2. Effect of Second Base Drive on the Turn-Off Time

Among the eleven devices evaluated, seven devices have the option of second base drive. Table 2.3 summarizes the effect of the second base drive on the reduction of turn-off time.

Significant reduction of storage time and fall time can be achieved by the use of the second base. This is especially true for devices without speed-up diode. A 30% reduction in both the storage time and the fall time has been observed. The increase of switching speed, in both the storage time and the fall time, however, must be accompanied by the increase of base drive circuit complexity.

2.1-3. Switching Energy Losses

Table 2.4 gives a relative comparison of switching energy losses of all the device evaluated.

2.1-4. Saturation Voltage

Table 2.5 summarizes the saturation voltage of the devices.

2.1-5. Current Gain

Table 2.6 summarizes the curren gain of the devices.

2.1-6. Power Losses

Table 2.7 summarizes the power losses

2.1-7. Effect of Collector-Emitter dv/dt and the Reverse Recovery of the Anti-Parallel Diode

In the operation of a three phase bridge inverter for AC drives, a destructively large turn-on current spike of transistor may occur. This is caused by two possible sources. One is the slow reverse recovery time of the anti-parallel diode of the totem pole device and the other is dv/dt stress that momentarily turns on the opposing transistor in the totem pole. It is concluded that in all the transistors been evaluated, dv/dt effect is dominant in determining the turn-on surge current. It was observed that turn-on surge current could be 10 times as high as the steady state current if the base is not kept reverse biased. This accounts for one of the failure modes of the transistor operation. By properly reverse biasing the transistor that is subjected to high dv/dt, the turn on surge current can be reduced 5 times. This finding has a direct ramification on base circuit design.

High Power Transistors Evaluated

	No.	Device Type	Configuration	Second Base Drive Feature	Speed-Up Diode	Package	Voltage&Current Rating
	1	Westinghouse KD324510	Double Darlington	Yes	No	Dual Tottem-Pole	100A/450V
	2	Westinghouse DA11503008	Discrete Darlington	Yes	No	Single	300A/400V
ļ	3	Fuji ETN81-055	Double Darlington	Yes	Yes	Single	200A/550V
	4	Fuji EVM31-050	Double Darlington	No	Yes	Dual	150A/500V
	5	Mitsubishi QM150DY-H	Double Darlington	Yes	Yes	Dual Tottem-Pole	150A/450V
	6	Mitsubishi QM300HA-H	Double Darlington	Yes	Yes	Single	300A/450V
	7	Mitsubishi QM300HA-2H	Triple Darlington	Yes	Yes	Single	300A/1000V
	8	Toshiba ST200M-R2G41	Double Darlington	Yes	Yes	Dual Tottem-Pole	200A/900V
	9	Toshiba ST300M21	Double Darlington	No	No	Single	300A/900V
	10	Toshiba ST400G21	Double Darlington	No	No	Single	400A/450V
	11	Toshiba ST400G-R2G41	Double Darlington	Yes	Yes	Dual Tottem-Pole	400A/450V

Generalized evaluation of the switching times for each tested device

No.	characteristic Device type	to n	ts	t _f	agreement with the specified data
		I	GROU	JP	
1.	Westinghouse KD324510	M	F	F	good
2.	Fuji EVM 31-050	M	F	M	good
3.	Mitsubishi QM1500DY-H	M	F	M	good
4.	Fuji ETN81-055	F	М	F	good
5.	Toshiba ST200M	s	S	S	good
		II	GROU	JP	•
6.	Mitsubishi QM300HA-H	М	F	F	good
7.	Mitsubishi QM300HA-2H	s	М	М	moderate
8.	Toshiba ST300M21	F	s	s	moderate
9.	Westinghouse DA 11503008	s	М	s	poor
10.	Toshiba ST400G	s	F	s	no data
11.	Toshiba ST400G21	F	М	М	moderate

F - fast

M - moderate S - slow

The Second base drive effect on the storage and fall time

No.	Characteristic Device Type	t _{s.} [%]	t _f [%]
1.	Westinghouse KD324510	10-20	10-25
2.	Westinghouse DA11503008	25-45	45-60
3.	Fuji ETN81-055	30-35	10-20
4.	Mitsubishi QM150DY-H	20-25	10-20
5.	Mitsubishi QM300HA-H	NOT ME	ASURED *
6.	Mitsubishi QM300HA-2H	5-10	10-20
7.	Toshiba ST400G	20-25	40-50

^{*2}nd base drive introduces large collector spikes, therefore, measurements were not performed (all measurements were performed w/o clamp or snubber circuit)

TABLE 2.4 Switching energy losses generalized data

No.	Characteristic Device Type	Q _{on}	Q _{on(qsat)}	Q _{on(tot)}	Q _{off}	Q _{tot}
			I	GROUP		
1.	Westinghouse KD324510*	L	L	L	М	M
2.	Fuji EVM31-050	M	M	M	L	L
3.	Mitsubishi QM150DY-H	M	М	M	L	L
4.	Fuji ETN81-055	М	М	M	M	М
5.	Toshiba ST200M	н	Н	Н	Н	н
			II (GROUP		
6.	Mitsubishi QM300HA-H *	L	L	L	L	L
7.	Mitsubishi QM300HA-2H	M	M	M	M	М
8.	Toshiba ST300M21	М	м	M	H	н
9.	Westinghouse DA11503008	М	М	М	M	М
10.	Toshiba ST400G	н	н	н	н	н
11.	Toshiba ST400G21	L	L	L	м	М

^{*} extrapolated to $V_{CC} = 300V$

L - low M - medium H - high

TABLE 2.5 The Saturation voltage range for the forward forced gain in the range of 25 to 75 ($G_{
m f}$ = 25-75) at collector current levels greater than 50% of rated current

No.	Characteristics Device Type	V _{Ecat} [v]	agreement with the specified data
		I GRO	DUP
1.	Westinghouse KD324510	1-1.3	good
2.	Fuji EVM31-050	1.4-2.3	good
3.	Mitsubishi QM150DY-H	1-1,2	good
4.	Fuji ETN81-055	1-2.25	good
5.	Toshiba ST200M	1 4-5	good
		II (ROUP
6.	Mıtsubishi QM300HA-H	1-1.3	good
7.	Mitsubishi QM300HA-2H	1.9-2.2	good
8.	Toshiba ST300M21	0.9-1.2	good
9.	Westinghouse DA11503008	2-2.25	good
10.	Toshiba ST400G	1.1-2.2	no data
11.	Toshiba ST400G21	1.35-1.5	good

Current Gain Value at Maximum Rated Collector Current Level at V_{CE} = 3V

No.	Characteristic Device Type	${ m h_{FE}}$	agreement with the specified data*
		I GR	OUP
1.	Westinghouse KD324510	125	good
2.	Fuji EVM31-050	80	good
3.	Mitsubishi QM150DY-H	190	good
4.	Fuji ETN81-055	100	good
5.	Toshiba ST200M	60	good
		II G	ROUP
6.	Mitsubishi QM300HA-H	230	good
7.	Mıtsubishi QM300HA-2H	120	good
8.	Toshiba ST300M21	160	good
9.	Westinghouse DA11503008	65	moderate
10	Toshiba ST400G	95	no data
11.	Toshiba ST400G21	200	good

^{*} extrapolated

Table 2.7 The Approximate Calculated Maximum Operating Frequency for the Duty Cycle 50% at the Maximum Rated Collector Current and $V_{\rm CC}^{=300V}$ with $G_{\rm f}^{=6} = G_{\rm rl}^{=50}$

No.	Characteristic	Specified P _D [W]	Conduction loss [%]	Switching loss [%]	Maximum frequency
	Device Type				<kh></kh>
1.	Westinghouse KD324510 *	620	10	90	15
2.	Westinghouse DA11503008	3000	10	90	10
3.	Fuji ETN81-055	1000	13	87	6
4.	Fuji EVM31-050	600	20	80	5
5.	Mıtsubıshı QM150DY-H	690	15	85	11
6.	Mıtsubıshı QM300HA-H *	1380	15	85	11
7	Mıtsubıshı QM300HA-2H	1980	15	85	8
8.	Toshiba ST200M **	400	251	75	1
9.	Toshiba ST300M21	1500***	10	90	4.5
10.	Toshiba ST400G	400***	901	10	<<1
11.	Toshiba ST400G21	1500***	20	80	3.5

^{*}extrapolated for V_{cc} =300V

 $^{**}G_{f} = 25$

^{***} estimated using thermal resistance data because $\mathbf{P}_{\widehat{\mathbf{D}}}$ data are not given

2.1-8. Package Type

- 1. For AC motor drive application in which a bridge inverter configuration is needed, the totem-pole power module (two transistors in series), each with and anti-parallel drode, is desirable for two reasons. The first reason is the convenience of inverter package which ultimately translates to a lower cost. The second reason is that the snubbering requirement can be much reduced because of a smaller parasitic inductance associated with the much shorter conductor length between the two transistors within the module. In fact, a snubber across the bus, instead of six separate snubbers across each transistor of the 3 phase inverter, is often adequate if totem-pole power modules are used.
- 2. In some applications where device paralleling is required, power module (two separate transistor chips mounted on the same package) is also desirable. Current sharing between the two devices are improved by a better thermal coupling of the devices and by the geometric symmetry of the package.

2.1-9. Reverse Bias Safe Operating Area

1. The RBSB behavior of a Darlington transistor depends on the magnitude of the reverse-base current. For a strong reverse-base drive, breakdown usually occurs before $V_{\rm CE}$

reaches $V_{\text{CE(SUS)}}$. The breakdown voltage may be greater than or less than $V_{\text{CE(SUS)}}$ and may increase with or decrease with the reverse base current depending on devices. For a weak drive, the breakdown could occur several microseconds after the Darlington transistor reaches the sustaining mode.

2. It has been observed that the RBSB voltage of a Darlington transistor may vary significantly with the magnitude of forward base current. This suggests that a new parameter, forward base current, should be included in the characterization of RBSOA of a Darlington transistor which has never been done in any manufacturers.

Among the devices evaluated, only several are provided with RBSOA Specifications. from the manufacturers. Those are

Westinghouse KD32450

Fuji ETN81-055

Fuji EVM31-050

Mıtsubishi OM300HA-H

The RBSOA data, for all the four devices mentioned above, is given for only one fixed reverse-bias current value. In all the RBSOA data provided through this report, both forward current and reverse base current are varied to fully characterize the devices. It has been observed that 200 V difference (in 600 V devices) could results from different yet practical driving conditions.

3. The manufacturers' estimate for RBSOA is in general quite

conservative. Yet, certain drive conditions were observed to cause device breakdown within the manufacturers specified RBSOA.

- 4. The turn-off speed-up diode plays an important role in the RBSB behavior of a Darlington transistor. Using the same base drive circuit, a transistor may exhibit different breakdown voltage levels, depending upon whether a speed-up diode is present. If a diode is not present, the breakdown voltage varies with the value of R₂ (the resistor in parallel with the emitter and base of the driver transistor).
- 5. RBSOA of a device is significantly altered by temperature. In some devices, at high collector current level, RBSOA increases with temperature. An increase of 100 V (for 600 V device) has been observed from 25°C to 90°C. On the other hand, at low collector current level, RBSOA decreases with temperature. A reduction of 20 V from 25°C to 90°C was observed. In other devices, RBSOA increases with temperature regardless of collector current level.

Comments for each Transistor Evaluated

Westinghouse KD324510

Fuji ETN81-055

Fuji EVM 31-050

Mıtsubishi QM150DV-H

Generally speaking, these devices can be reliably operated

up to rated curent without snubber or clamp circuit provided that supply voltage is below 300 V for Fuji and Mitsubishi devices and 200 V for Westinghouse device.

Mıtsubishi QM300HA-H

- The fastest device among all devices tested.
- Large turn-off voltage spike
- Needs claim circuit for supply voltages greater than 150 V
 and the reverse current greater than 8 A
- Demands careful design (lay-out) of collector circuit to minimize lead inductance

Mıtsubishi QM300HA-2H

- Very fast device
- Large turn-off voltage spike
- Because of high breakdown voltage (900V) it can be operated with 300 V power supply without using clamp or snubber circuit.
- A very rugged device in our opinions

Toshiba ST200M

- Relatively slow device (compared with the similar device ETN81-055)
- No high voltage spike during turn-off

- Do not need snubber or clamp circuit even for operation from 300 V supply
- Under the same considerations, this device is getting hotter than other switching devices because poor thermal resistance $(R_{th(j-c)} = 0.25 \, ^{\circ}C/_{W}$ is specified).

Toshiba ST400G

- Slow device (turn-on and off)
- Relatively low voltage spike
- Snubber and clamp circuit is not necessary (except with high reverse base current operation)
- Poor thermal resistance, the device usually gets very hot even at low duty cycle operation

Westinghouse DA11503008

 Driver transistor reliability (especially for high reverse base current) is less than expected (two driver devices are lost during testing under the conditions within specified ratings)

Toshiba ST300M21 and ST400G21 (press pack)

- Low thermal resistance, this is interesting because ST400G21 and ST400G probably have the same chip and ST400G has problems with the thermal resistance
- ST300M21 doesn't need snubber or clamp. For ST400G21 the same conclusion holds as for ST400G regarding clamp circuit.

2.2. BASE DRIVE CIRCUIT COMPARISONS

Three base drive circuits have been evaluated including the Fuji base-drive module, the Mitsubishi base-drive module and the PERG base drive. The third base drive circuit, designed by the Power Electronics Research Group (PERG), VPI&SU, uses a collector voltage feedback method that does not allow for direct comparison with the first two base drives. Therefore, direct comparison are made of the first two drive circuits and the preferred circuit is compared to the PERG base drive based on projected performance.

The Fuji circuits exhibited two undesirable characteristics:

- High levels of interference susceptibility required very careful construction techniques to achieve a suitably working circuit.
- 2. During the turn-off base drive cycle when applied to the power switch, a "notching" in the base drive circuits output occurred that could force the power switch into an undesired operating mode.

The Mitsubishi circuit provided two desirable characteristics:

- a. Since using only one input photocoupler an easier system interface is provided.
- b. The total electrical performance of the drive is superior to that of the Fuji except for a 25% faster turn-off time exhibited by the Fuji drive.

It is concluded that the Mitsubishi base drive should be preferred when compared to the Fuji drive.

When comparing the electrical performance of the Mitsubishi base drive and PERG base drive there are equally weighted pros and cons. However, when comparing the drives from a functional systems point of view, the PERG drive offers many advantages with respect to monitoring and controlling the operating parameters of a power electronic switch.

In conclusion, for a "simple" base drive circuit application the Mitsubishi base drive is preferred over the Fuji circuit. If the storage time of a power

electronic switch is unimportant in the system design then the Mitsubishi base drive is comparable in <u>electrical</u> <u>performance</u> to the PERG base drive. However, if comparing the functionality of the base drive circuits at a systems level, the PERG drive excels. The PERG drive provides the following features:

- A self regulated positive base current,
- A negative base current in-suring fast power switch turn-off at a constant current level,
- Adjustable output current,
- A selectable minimum conducting time to allow for discharge of any snubber networks,
- Protection against deep saturation of the power switch,
- Immediate limitation of the collector current to avoid overcurrent operation of the power switch,
- Monitoring of the positive and negative base drive circuit power supplies and programmable maximum on-time.

Only the device manufactured by Siemens of West Germany was tested. By all indications these devices are not Asymmetrical SCRs (ASCR). Neither the data sheets, test and characterizations indicate that these are ASCRs. As such their performance compared with typical ASCR's performances is poor. Further, in the most critical parameter for inverter operation, that of commutated turn-off time, t_q , the Siemens devices did not meet the

manufacturer's specification. It is concluded that in typical motor drive inverter applications these devices will provide inferior performance compared with generally accepted, state-of-the-art alternatives.

2 3. POWER FETS

Table 2.10 summarizes the rating of the FET devices evaluated

2.3.1 Conduction Resistance

Table 2.11 & 2.12 summarizes the comparison of the conduction resistance for different devices.

Comments

- $^{R}_{DS(on)}$ is increasing with drain current I_{D} for the constant gate drive (V_{GS}) ;
- $R_{DS(on)}$ depends on gate-source voltage V_{GS} . That dependence is very weak for all devices and $R_{DS(on)}$ is slightly reduced with increasing of V_{GS} . Moreover, the influence of V_{GS} on $R_{DS(on)}$ is more pronounced at higher current levels, above the rated DC level, i.e., at the levels allowed only in pulsed mode operation. The strongest influence of V_{GS} on $R_{DS(on)}$ was observed for IRF 441, where at the maximum pulsed drain current, change of V_{GS} from 10V to 15V causes 10% decrease of $R_{DS(on)}$ from 2.20 to 2.0

TABLE 2.10

Power FET Ratings

No	Тур	I _D [A]	I _{DM} [A]	BV _{Dss} [V]	R _{DS(on)} [Ω]	P _O [W]	PACKAGE
1	IRF 441	8	32	500	0.85	125	TO-3
2	RFK 15N45 (RCA)	15	40*	450	0.85	х	то-3
3	RFK 15N50 (RCA)	15	40*	500	0.85	х	TO-3
4	2SK 356 (Toshiba)	12	30	250	0.25	120	TO-3
5	2SK 386 (Toshiba)	10	15	450	0.7	150	PLASTIC not standard

^{*} supposed x unknown

 $^{\rm R}_{
m DS(on)}$ increases with a increase of the case temperature $^{\rm R}_{
m C}$ for a given $^{\rm V}_{
m GS}$. The change of resistance value with $^{\rm T}_{
m C}$, also, depends on the drain current level. Its is observed that the temperature coefficient of $^{\rm R}_{
m DS(on)}$ is greater at higher current levels. Positive temperature coefficient of $^{\rm R}_{
m DS(on)}$ is very desirable for parallel operation of MOSFETs because it tends to balance current sharing through each device.

In Table 2.11, the intervals of the on-resistance values in the full range of drain current at three different temperatures are given. In fact, Table 2.12 generalizes the data given in Appendix E.

2.3.2 Switching Time

Table 2.13 summarizes the switching times for the devices evaluated.

Comments

A. Turn-on delay time td(on)

The main conclusions about $t_{d(on)}$ can be summarized as follows:

- t_(on) is almost independent of drain curren I_D;
- $t_{d(on)}$ depends on the gate drive conditions (V_{GS} and R_{GS}) strongly;
- t_{d(on)} decreases with a increase of V_{GS};
- t_{d(on)} depends on the device type;

TABLE 2.11

On-resistance values in the full range* of drain current at three different case temperatures $T_C = .30$; 75; 100°C for $V_{GS} = 10$ V

No.	Characteristic Device Type	R _{DS(on)} [Ω] at T _C =30°C	R _{DS(on)} [Ω] at T _C =75°C	R _{DS(on)} [Ω] at T _C =100°C
1.	IRF 441	0.8 - 2	1.3 - 2.6	1.4 - 3.6
2.	RCA RFK 15N45	0.45 - 1	0.7 - 1.1	0.8 - 1.5
3.	RCA RFK 15N50	0.55 - 1	0.7 - 1.1	0.9 - 1.4
4.	Toshiba 2SK 356	0.25 - 0.27	0.3 - 0.35	0.35 - 0.45
5.	Toshiba 2SK 386	0.55 - 0.65	0.8 - 1.1	0.9 - 1.35

^{*} Full range means from low current up to maximum pulsed current allowed. At higher T_C then 30°C derated maximum pulsed current values were taken.

TABLE 2.12

Devices Relative Categorization Regarding the On-Resistance Values

LOW RDS(on)	2SK 356
MEDIUM R _{DS(on)}	RFK 15N45, RFK 15N50, 2SK 386
HIGH ^R DS(on)	RF 441

• for all give device $t_{d(on)}$ is in the range from 80 ns to 60 ns. The upper range values correspond to smaller V_{GS} ; i.e., $V_{GS} = 10V$.

B. Rise Time tr

From the data obtained for the rise time we can draw the following conclusions:

- t_r depends strongly on both drain current (I_D) and gate drive conditions (V_{GS}, R_{GS}) ;
- t_r is increasing function of I_D ;
- t_r is decreasing function of V_{GS} ;
- The influence of V_{GS} on t_r is stronger at the higher current levels (the range over D.C. current rating);
- the range of t_r measured for two different $V_{\rm GS}$ = 10 and 15V is 5-30 ns at low currents and 300-400 ns at maximum pulsed current.

C. Turn-On Time ton

Turn-on time (t_{on}) is given as a sum of turn-on delay time $t_{d(on)}$ and rise time (t_r) i.e.

$$t_{on} = t_{d(on)} + t_{r}$$

The general conclusions about t_{on} can be summarized as follows:

TABLE 2.13

Typical Ranges of the Switching Times for each Device Tested for $V_{GS} = \{10; 15V\}$ and Full Range of I_D (up to maximum pulsed rated)*

No	Characteristics DEVICE TYPE	td(on) (ns)	t _r (ns)	ton (ns)	t _{d(off)} (ns)	t _f (ns)	^t off (ns)
ļ	DEVIOR III				·		
1.	IRF 441	60-80	35-370	100-440	10-20	40-80	20-100
2.	RCA RFK 15N45	60-80	35-370	100-440	30-50	120-240	150-290
3.	RCA RFK 15N50	60-80	35-370	100-440	30-50	90-170	120-220
4.	Toshiba 25K 356	60-80	30-420	90-500	15-30	30-140	45-170
5.	Toshiba 25K 386	60-70	5-120	65-190	10-20	30-40	40-60

*devices have different $I_{\mbox{\footnotesize{DM}}}$ rating see Table 2.10

- t_{on} depends on both I_D and V_{GS};
- t_{on} depends on I_{D} in the very same manner as t_{r} because $t_{d(on)}$ is virtually independent of I_{D} ;

D. Fall Time tf

The main observations regarding fall time (t_f) are:

- t_f depends on the drain current I_D for constant gate drive so that t_f increases as I_D increases;
- t_f is virtually independent of the gate voltage $V_{\mbox{\footnotesize GS}}$ condition at all current levels;
- the range of t_f obtained for measured device in full current range is 15 ns-220 ns;

E. Turn-Off Time toff

Turn-off ($t_{(off)}$) time is given as a sum of turn-off delay time ($t_{d(off)}$) and fall time (t_f) i.e.,

The general conclusions about $t_{\mbox{off}}$ can be summarized as follows:

• $t_{\rm off}$ depends on both drain current $I_{\rm D}$ and gate voltage $V_{\rm GS}$. It should be noted that $t_{\rm f}$ depends on $I_{\rm D}$ and $t_{\rm d(off)}$ is independent of $I_{\rm D}$.

2.3.3 Parallel Operation Consideration

All five device types were tested for two-device parallel operation. The main concern in parallel operation is the static and dynamic load current sharing properties among devices in parallel as well as the thermal stability of that operation. The analyses of parallel operation was carried out by monitoring the load current sharing at different currents levels for different gate-source voltages and duty cycles.

From data obtained (presented in the Appendix H using format explained in section 6.5.4) we can draw the following conclusions:

- For all devices under consideration, static sharing of load current at all drain current levels are relatively good. Generally speaking the static sharing is within 5A difference in the individual drain currents. The difference in current is caused either by the spread of on-resistance value or the effect of parasitic resistance of the test circuit which was not identical for both devices, the second effect is perhaps prevalent.
- Dynamic sharing during the turn-on phase is good for all devices and at all drain current levels. Slight differences were observed primarily because of non-equalized parasitic inductances in individual circuit, in spite of all precaution taken to avoid that
- Dynamic sharing during the turn-off phase is also good for all devices and at all drain current levels

 The stable parallel operation were observed for all devices at all drain current levels except for Toshiba 2SK 386 device.

2.4. ASYMMETRIC SCR

Only the device manufactured by Siemens of West Germany was tested. By all indications these devices are not Asymmetrical SCRs (ASCR). Neither the data sheets, test and characterizations indicate that these are ASCRs. As such their performance compared with typical ASCR's performances is poor. Further, in the most critical parameter for inverter operation, that of commutated turn-off time, $\mathbf{t_q}$, the Siemens devices did not meet the manufacturer's specification. It is concluded that in typical motor drive inverter applications these devices will provide inferior performance compared with generally accepted, state-of-the-art alternatives.

3.0 EVALUATION OF HIGH POWER BIPOLAR JUNCTION TRANSISTORS

In the past three years, dramatic advancement has been made in high power bipolar transistor industry. Devices of various ratings are commercially available at much reduced prices. In this chapter, results of evaluatin of 11 different transistor types from various companies will be presented. Devices rating ranges from 100 A to 400 A in current and from 450 V to 1000 V in voltage. Table 3.1 summarizes the devices ratings, the package types, availability of the second base terminal etc.

In the presentation, test equipment will be described first, and definition of various device parameters will be given. A summary of test results will then be presented. In the concluding section, test results will be evaluated and key observations and remarks will be summarized. Detailed test data are presented in Volume II of the report.

3.1 TEST TASKS

Six sets of device parameters will be evaluated in this task.

- A. Switching Times

 Turn-on time t_{on} Storage time t_{s} Fall time t_{f}
- B. Switching Power Losses
 Turn-on Power Loss Pon

Table 3.1. High Power Transistors to be Evaluated

No.	Device Type	Configuration	Second Base Drive Feature	Speed-Up Diode	Package	Voltage&Current Rating
1	Westinghouse KD324510	Double Darlington	Yes	No	Dual Tottem-Pole	100A/450V
2	Westinghouse DA11503008	Discrete Darlington	Yes	No	Single	300A/400V
3	Fuji ETN81-055	Double Darlington	Yes	Yes	Single	200A/550V
4	Fuji EVM31-050	Double Darlington	No	Yes	Dua1	150A/500V
5	Mitsubishi QM150DY-H	Double Darlington	Yes	Yes	Dual Tottem-Pole	150A/450V
6	Mitsubishi QM300HA-H	Double Darlington	Yes	Yes	Single	300A/450V
7	Mitsubishi QM300HA-2H	Triple Darlington	Yes	Yes	Single	300A/1000V
8	Toshiba ST200M-R2G41	Double Darlington	Yes	Yes	Dual Tottem-Pole	200A/900V
9	Toshiba ST300M21	Double Darlington	No	No	Single	300A/900V
10	Toshiba ST400G21	Double Darlington	No	No	Single	400A/450V
11	Toshiba ST400G-R2G41	Double Darlington	Yes	Yes	Dual Tottem-Pole	400A/450V

Quasi-Saturation Loss $P_{on(qsat)}$ Turn-off Power Loss P_{off}

C. Static Characteristics

Saturation Voltage V_{CE}, sat

Current Gain h

- D. Reverse Recovery Characteristics of Anti-Parallel

 Diode and dv/dt Effect
- E. Device Paralleling
- F. Effect of Second Base Drive
- G. RBSB Characterization

3.2 TEST EQUIPMENT

The test equipment consists of:

Base Drive Module

Load Circuit

Power Supply (EMHP 300 V/100 A)

Tektronix Current Probes

Tektronix Digital Processing Oscilloscope 7854 (DPO)

Tektronix 4052 Graphic Computing System and Hard Copy Unit

The block diagram of the test equipment interconnection is given in Figure 3.1.

Detailed schematic of power transistor test circuit is given in Figure 3.2.

The base drive module has the following features.

Forward Drive Selection (max 15 A)

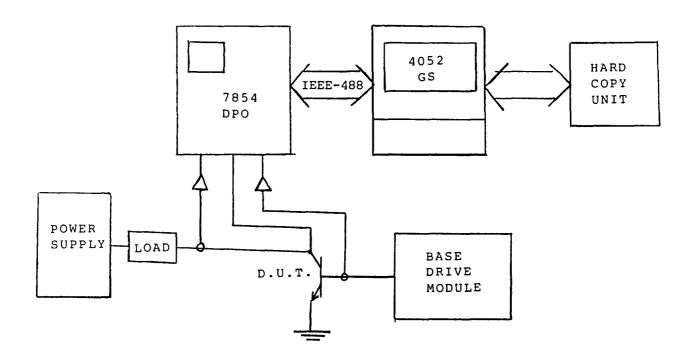


Fig. 3.1 Test Set-Up

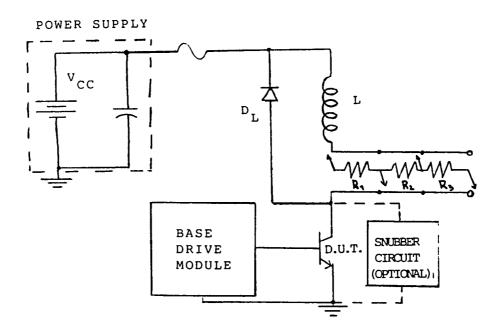


Fig. 3 .2. Power Transistor Tester Circuit

Single Base Reverse Drive Selection (max 20 A)

Base Drive Envelope Control for Average Supply

Current

Duty Cycle PWM Control

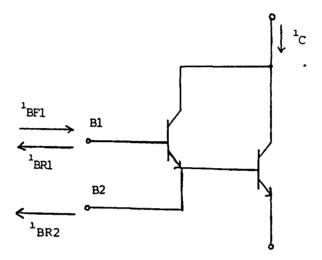
The digital processing oscilloscope is used for acquiring and processing relevant transistors waveforms for the switching times and power losses calculations while the graphical computer terminal is used for permanent data storage (magnetic tape) and graphics representation of the measured data.

3.3 TEST METHOD

All data are generated as a function of the collector current for various values of the forward $(G_{\mathbf{f}})$ and reverse $(G_{\mathbf{r}1} \text{ and } G_{\mathbf{r}2})$ forced current gains. Definitions of $G_{\mathbf{f}}$, $G_{\mathbf{r}1}$ and $G_{\mathbf{r}2}$ are given in Fig. 3.3.

Depending on the measured characteristic data are generated with the following parameters:

- Turn-on time ton-f(Ic); varying Gf
- Storage time t_s=f(I_c); varying G_{r1}
- Fall time $t_f = I(I_c)$; varying G_{r1}
- Storage time with second base,
 t_s=f(I_c); varying G_{r2}
- Fall time with second base
 t_f-f(I_c); varying G_{r2}



$$G_{f} = \frac{{}^{1}_{c}}{{}^{1}_{BF1}}$$

$$G_{r1} = \frac{{}^{1}_{c}}{{}^{1}_{BR1}}$$

$$G_{r2} = \frac{{}^{1}_{c}}{{}^{1}_{BR2}}$$

Fig. 3.3. The Forced Gains Definitions

- Turn-on loss (crossover)
 Q_{on}=f(I_c); varying G_f
- Turn-on loss (quasisaturation)

- Turn-on loss (total) Q_{on(tot)}=f(I_C); varying G_f
- Turn-off loss Q_{off}=f(I_c); varying G_{r1}
- Switching loss (total) $Q_{tot} = f(I_C); \text{ varying } G_{r1} \text{ and } G_f$
- Saturation voltage V_{CE,sat}=f(I_C); varying G_f
- Current gain $h_{FE} = f(I_C)$.

Conventional definition of switching times is used. Fig. 3.4 shows such a definition. Switching power losses definition is also given in the same figure, as well as in Fig. 3.5 for turn-on loss in more details.

3.4 TEST RESULTS

The devices were tested under the following conditions.

- Supply voltage is approximately 300 V for all devices except the Westinghouse KD324510 $(V_{CC}=200\ V) \ \text{and the Fuji QM300HA-H } (V_{CC}=175\ V).$
- Case temperature is 30° C
- · No snubber circuit was used

The test results are presented in Appendices A to C.

In Appendix A, measurements of switching characteristics are given for each device type. The devices are presented in

Horz. Dimension: 4.353E-6 sec/div.

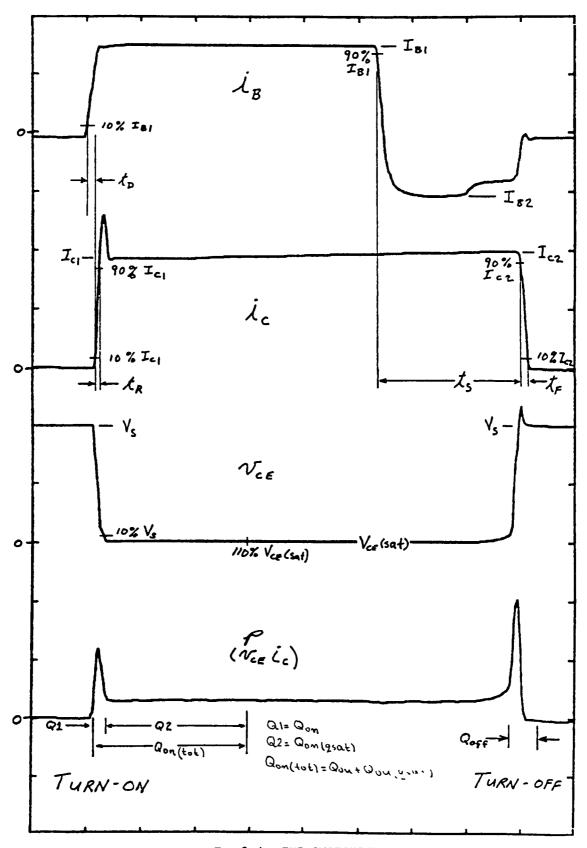


Fig.3.4 TUT SWITCHING CYCLE

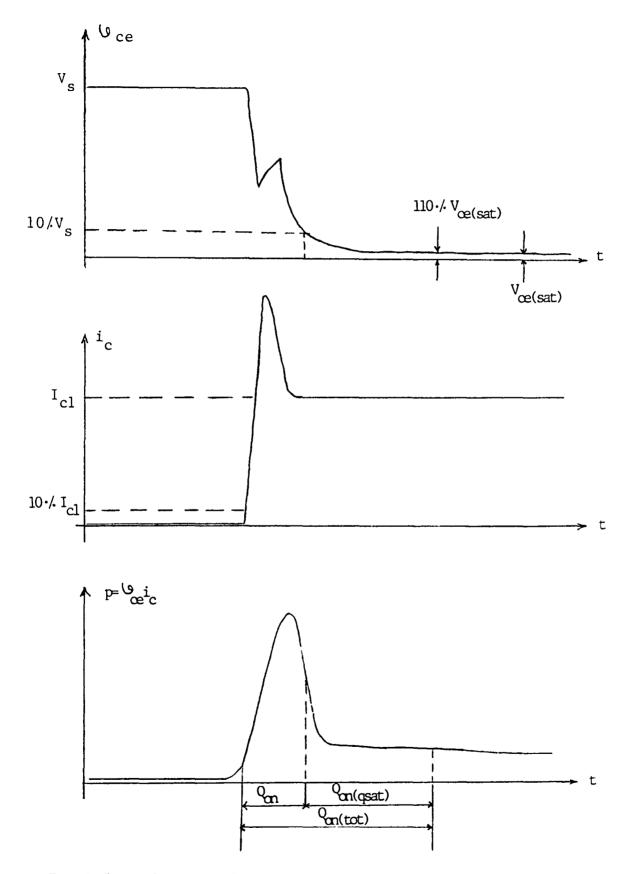


Fig. 3.5. Definition of turn-on power losses.

the same order as listed in Table 3.1 earlier. In Appendix B, the bulk data presented in Appendix A are reorganized in a fashion that one can readily make comparison among devices of comparable rating. Finally, in Appendix C, the test data of parallel operation of power transistors are presented.

3.4.1 Test Results for Each Device (Appendix A)

The test results are given in Appendix A from Fig. A.1.1 to Fig. A.11.13. There are several graphics given for each device type. A description of the graphics and the illustration how to use them are given below, using the data for Westinghouse's KD324510 as an example.

Rise-Time ton (Fig. A.1.1)

This plot presents transistor rise time versus collector current magnitude using forward gain ($G_f = I_C / I_{BF1}$) as the running parameter. For example, at 100 A, and forward gain of 50 (i.e. $I_{BF} = 2$ A), the rise time is approximately 0.6 s.

Storage Time t_s (Fig. A.1.2 and Fig. A.1.3)

Since the storage time is affected by both the forward gain and the reverse gain, two graphs are given for each device. In one graph, the reverse gain is fixed, but forward gain is a running parameter and in the other graph, the forward gain is fixed and the reverse gain is a running

parameter. In both graphs, storage time is plotted versus collector current. This set of data provides the designers more complete data in choosing the desirable base drive conditions.

Fall Time t_f (Fig. A.1.4)

Fall time is mainly a function of collector current level and reverse gain. As can be seen from the data, reverse gain affects the fall time much more dramatically than collector current.

Effect of Second Base Drive on Storage Time and Fall Time (Fig. A.1.5 and A.1.6)

Fig. A.1.5 is a plot of storage time vs. collector current for fixed forward gain and fixed the first base forced reverse gain (G_{r1}) by varying the second base forced reverse gain (G_{r2}) . Notice that reverse gain of "infinity" refers to the case when the second base is not used. As it can be seen from the figure, a significant reduction of storage time can be achieved by the use of the second base. The same thing applies to the fall time data shown in Fig. A.1.6. This increase in switching speed, however, must be accompanied by the increase of base drive complexity.

Turn-On Switching Energy Losses (Qon', Qon(qsat) on(tot) (Figs. A.1.7, A.1.8 and A.1.9)

Graphs 7, 8 and 9 are all related to turn-on energy losses. Turn-on losses can be divided into two periods, the cross-over period and the "tailing" period. The exact definition of both periods is shown in Fig. 3.5. Fig. A.1.7 is a plot of turn-on loss during cross-over period. Fig. A.1.8 is a plot of turn-on loss during the "tailing" period and Fig. A.1.9 is a plot of total turn-on energy losses. The voltage waveform "tailing" phenomenon is due to the quasi-saturation region of a power transistor. The loss during the "tailing" period is also called quasi-saturation turn-on loss $Q_{\rm on(qsat)}$. It can be seen from both Fig. A.1.7 and A.1.8 that the energy loss during the "tailing" period is significantly higher than during the cross-over period. To find out the average turn-on power loss, energy loss must be timed by operating frequency.

Turn-Off Energy Loss Qoff (Fig. A.1.10)

This graph is a plot of turn-off energy loss as a function of collector current using reverse gain $(G_{r1}=I_{C}/I_{BR1})$ as running parameter. Using this number, one can find out turn-off power dissipation at certain switching frequency by multiplying energy loss per turn-off by frequency.

Total Switching Energy Loss Qtot (Fig. A.11)

This graph gives a plot of the sum of the turn-on losses and turn-off losses $(Q_{tot}=Q_{on(tot)} + Q_{off}(tot))$ under

the different base drive conditions.

Switching Loci (Figs. A.1.12 and A.1.13)

Fig. A.1.12 is for turn-on switching locus and Fig. A 1 13 is for turn-off. Both are for switching an inductive load.

Collector-Emitter Saturation Voltage V_{CE} sat (Fig. A.1.14)

In this graph, the transistor conduction drop is plotted against collector current for different forward gains.

Current Gain h FE (Fig. A.1.15)

In this graph, the transistor current gain is plotted against collector current. Current gain data available in commercial catalogs are normally given under the condition of 5 V conduction drop. In the present graph, however, current gain is measured under the conditions of 3 V conduction drop. This voltage level is chosen because in electrical vehicle applications, conduction loss is of great concern and data available at 3 V conduction drop should help the circuit designers to choose proper base drive level to optimize the power loss.

Reverse Recovery Characteristics of Anti-Parallel Diodes and dv/dt Effect (Fig. A.1.16)

For each transistor, the dv/dt test was conducted for

two drive conditions. In the first drive condition, the DUT was held off by open circuit base and in the other condition the DUT's base was reverse biased by 4 V. These tests were conducted only for devices with intergrated diodes. Those devices which do not have an intergrated diode were not tested because the results would be affected by the choice of the particular descrete diode.

3.4.2 Comparison of Device Switching Characteristics (Appendix B)

Comparative test data plots generated for the devices with similar current rating are given in Fig. B.1.1 to B.4.6 in Appendix B. Four groups of transistors are formed as follows:

150 A devices

Fuji EVM31-050

Mıtsubishi QM150DY-H

200 A devices

Fuji ETN81-055

Toshiba ST200M

300 A devices

Westinghouse DA11503008

Mıtsubishi QM300HA-H

Mıtsubishi QM300HA-2H

Toshiba ST300M21

400 A device

Toshiba ST400G

Toshiba ST400G21

The Westinghouse KD324510 is the only device with 100 A collector current rating. The Comparative data for the four groups of devices include the following characteristics.

- 1. Turn-on time
- 2. Storage time
- 3. Fall time
- 4. Turn-on total energy loss
- 5. Turn-off energy loss
- 6. Total switching energy loss
- 7. Collector-emitter saturation voltage
- 8. Current gain

For example, both ST400G and ST400G21 are 400 A, 450 V devices. From the comparative data, it can be seen that ST400G21 is faster in current fall time, and rise time and consequently has less turn-off power loss but slower in storage time, and also smaller in conduction drop. Since the storage time is measured under the same forward gain, the longer storage time of ST400G21 is due to higher current gain of the device. In other words, the device (ST400G21) is more heavily saturated under the same forward current gain condition.

Comparison of other devices are given in the same format. This information enables the designer to make an intelligent decision based on overall device performances.

3.4.3 Devices in Parallel (Appendix C)

Because only one device type, the Fuji EVM31-050 has two separate transistors in the same package, test data are generated for the Fuji device, only. The test data are generated at the different collector current levels, base drive conditions, and case temperatures ($T_{\rm C}$ =30°C and $T_{\rm C}$ =100°C). At each collector current level and a given base drive, several oscillograms are taken to provide information of load current sharing through each device.

3.5 TEST RESULTS INTERPRETATION

Because of the enormous amount of data generated in this report, it is rather difficult and inefficient to have the readers interpret these results. In this section, the authors attempt to sort out these results, interpret them and draw conclusions concerning the following bipolar transistor characteristics.

switching times

effect of second base drive

energy losses

saturation voltage

current gain

switching load time

anti-parallel diode

parallel operation

3.5.1 Switching Times Consideration

As ıt was stated earlier the switching times measurements were performed for each device under the different base drive conditions and collector current However, because of the broad range of devices levels. current ratings, comparison of the switching performances for all devices which were tested is not practical. Therefore, the eleven devices being tested are divided into two groups according to their current ratings. group contains the devices with collector current rating up to 200 A, while the second group contains the devices with current rating in excess of 200 A.

Comparisons of switching performances is given in Table 3.2.

The last column in the table describes the degree of agreement between measured data and the manufacturer's specified data based on the limited information provided in the manufacturer's specification sheets.

As it can be seen from Table 3.2, there is a good agreement between the measured and specified data for most devices being tested. Only apparent disagreement between measured and specified data has been found for Westinghouse DA11503008 device, and that discrepancy is primarily in storage time values.

Table 3.2 Generalized evaluation of the switching times for each tested device

No.	characteristic Device type	ton	ts	t _f	agreement with the specified data
		I GROUP			
1.	Westinghouse KD324510	M	F	F	good
2.	Fuji EVM 31-050	M	F	М	good
3.	Mıtsubishı QM1500Y-H	M	F	М	good
4.	Fuji ETN81-055	F	M	F	good
5.	Toshiba ST200M	s	s	s	good
		ΙΙ	GROU	JP	
6.	Mitsubishi QM300HA-H	M	F	F	good
7.	Mıtsubıshi QM300HA-2H	s	M	M	moderate
8.	Toshiba ST300M21	F	s	s	moderate
9.	Westinghouse DA 11503008	s	М	s	poor
10.	Toshiba ST400G	s	F	s	no data
11.	Toshiba ST400G21	F	М	М	moderate

F - fast M - moderate

S - slow

3.5.2 Effect of the Second Base Drive

For these devices with the accessible second base, improvement of turn-off switching characteristics is possible. The amount of improvement of the storage time and the fall time with the second base drive relative to no second base drive case depends on forced gain of the second base drive (G_{r2}) . In Table 3.3, the percentage of improvement of the storage time and the fall time is shown for the forced gain in the range of G_{r2} =25-100. For the higher G_{r2} , G_{r2} and G_{r3} are expected to be shorter.

From Table 3.3 it can be seen that for the most devices the improvement is about 20-30% in storage time and 10-20% in fall time. Maximum improvement in storage time was observed for Westinghouse DA11503008 (approximately 45% for $G_{r2}=25$), and the fall time (approximately 60% for $G_{r2}=25$).

3.5.3 Switching Energy Losses Consideration

Comparisons of switching energy losses is given in Table 3.4 Comparison has been made for two groups of devices depending on their current ratings as it has been done previously.

Besides the total switching energy losses per switching period, Table 3.4 also contains separate data for switching losses during the turn-on and the turn-off phase, i.e., $Q_{on(tot)} + Q_{off}$. Moreover, during the turn-on phase,

Table 3.3

The Second base drive effect on the storage and fall time

No.	Characteristic	t _s [%]	t _f [%]
	Device Type		
1.	Westinghouse KD324510	10-20	10-25
2.	Westinghouse DA11503008	25-45	45-60
3.	Fuji ETN81-055	30-35	10-20
4.	Mitsubishi QM150DY-H	20-25	10-20
5.	Mitsubishi QM300HA-H	NOT ME	ASURED *
6.	Mitsubishi QM300HA-2H	5-10	10-20
7.	Toshiba ST400G	20-25	40-50

^{* 2}nd base drive introduces large collector spikes, therefore, measurements were not performed (all measurements were performed w/o clamp or snubber circuit)

Table 3.4 Switching energy losses generalized data

No.	Characteristic Device Type	Q _{on}	^Q on(qsat)	Q _{on(tot)}	Q _{off}	Q _{tot}
			I GRO			
1.	Westinghouse KD324510	L	L	L	М	М
2.	Fuji EVM31-050	М	М	М	L	L
3.	Mıtsubıshı QM150DY-H	М	М	M	L	L
4.	Fiji ETN81-055	M	M	M	М	М
5.	Toshiba ST200G	н	н	Н	Н	Н
			II GROUP			
6.	Mitsubishi QM300HA-H	L	L	L	L	L
7.	Mıtsubıshi QM300HA-2H	М	М	M	М	М
8.	Toshiba ST300M21	М	М	M	Н	н
9.	Westinghous DA11503008	M	М	M	M	м
10.	Toshiba ST400G	Н	н	н	Н	н
11.	Toshiba ST400G21	L	L	L	М	М

extrapolated to $V_{cc} = 300V$

L - low M - medium H - high

separate loss data are provided for the crossover (Q_{on}) and quasisaturation phases $(Q_{on(qsat)})$ where $Q_{on(tot)} = Q_{on} + Q_{on(qsat)}$.

If one studies the loss data presented in Appendix A and B he can concede that the turn-off loss contributes to a large portion of the total switching energy loss. This implies that the devices with longer fall time have a greater total switching energy loss. In addition from the test data one can see that during turn-on phase the contribution of the quasisaturation energy loss to the total turn-on energy loss is most significant.

3.5.4 Saturation Voltage Consideration

The saturation voltage level for a given collector current depends strongly on the forward base current, i.e., forward forced gain $G_{\mathbf{f}}$. For lower $G_{\mathbf{f}}$, the device is more saturated than for higher $G_{\mathbf{f}}$. Furthermore, saturation voltage depends on collector current level and is smaller at lower currents.

In Table 3.5 the range of the saturation voltage for each device, with the forward forced gain $G_{\rm f}$ varying from 25 to 75, are given. The test results show good agreement with the specified data. It can be seen that the saturation voltages for almost all devices are in the range of 1 to 2.2 V, except for the Toshiba ST200M device which has $V_{\rm CE, sat} = 5$ V at $I_{\rm C} = 200$ A and $G_{\rm f} = 75$. If we examine the current gain of

Table 3.5 The Saturation voltage ranges for the forward forced gain in the range of 25 to 75 (G_f = 25-75) at collector current levels greater than 50% of rated values.

No.	Characteristics Device Type	V _{CE,sat} [v]	agreement with the specified data
		I GRO	UP
1.	Westinghouse KD324510	1-1.3	good
2.	Fuji EVM31-050	1.4-2.3	good
3.	Mıtsubıshı QM150DY-H	1-1.2	good
4.	Fuji ETN81-055	1-2.25	good
5.	Toshiba ST200M	1.4-5	good
		II GROUP	
6.	Mıtsubıshı QM300HA-H	1-1.3	good
7.	Mıtsubıshı QM300HA-2H	1.9-2.2	good
8.	Toshiba ST30021	0.9-1.2	good
9.	Westinghouse DA11503008	2-2.25	good
10.	Toshiba ST400G	1.1-2.2	no data
11.	Toshiba ST400G21	1.35-1.5	good

the Toshiba ST200M at I_C =200 A (Appendix A Fig. A.8.15) we can conclude that for G_f =75 the device is out of saturation.

3.5.5 Current Gain Consideration

In most cases, the current data given by manufacturers are sufficiently detailed. For the majority of the eleven devices tested, current gain specification is given at V_{CE} =5 V or V_{CE} =2 V. In order to avoid repetition, we have tested the current gain of the devices at V_{CE} =3 V, i.e. in the quasisaturation region.

The current gain values at the maximum rated collector current levels at $V_{\rm CE}=3$ V are given in Table 3.6.

From Table 3.6 one can see that Toshiba ST400G21, Mitsubishi QM300HA-H and Mitsubishi QM150DY-H are higher gain devices, while Toshiba ST200M and Westinghouse DA11503008 are lower current gain devices.

3.5.6 Switching Load Line Consideration

The switching load line characteristics during turn-on and turn-off are presented in Appendix A. The primary concern is the voltage stress during turn-off phase. The spike voltage (overtshoot) value is related to the circuit layout (parasitic inductance) and device turn-off speed which is dependent upon reverse forced gains G_{r1} and G_{r2} .

In Table 3.7 the voltage spike magnitudes, as the

Table 3.6
Current Gain Value at Maximum Rated Collector Current Level at $V_{\rm CE}$ = 3V

No.	Characteristic Device Type	h _{FE}	agreement with the specified data*
		I GR	OUP
1.	Westinghouse KD324510	125	good
2.	Fuji EVM31-050	80	good
3.	Mıtsubıshı QM150DY-H	190	good
4.	Fuji ETN81-055	100	good
5.	Toshiba ST200M	60	good
		II GROUP	
6.	Mıtsubıshı QM300HA-H	230	good
7.	Mıtsubishı QM300HA-2H	120	good
8.	Toshiba ST300M21	160	good
9.	Westinghouse DA11503008	65	moderate
10.	Toshiba ST400G	95	no data
11.	Toshiba ST400G21	200	good

^{*} extrapolated

Table 3.7 The Voltage Spike Magnitude as the Percentage of D.C. Level during Turn-Off Phase at Maximum Collector Current and $G_f = G_{rl} = 50$

No.	Characteristic Device Type		
1.	Westinghouse KD324510	30	yes
2.	Westinghouse DA11503008	25	Recommended
3.	Fuji ETN81-055	35	Recommended
4.	Fuji EVM31-050	25	Recommended
5.	Mıtsubishi QM150DY-H	25	Recommended
6.	Mıtsubishi QM300HA-H	75	yes
7.	Mitsubishi QM300HA-2H	35	not necessary
8.	Toshiba ST200M	10	not necessary
9.	Toshiba ST300M21	15	not necessary
10.	Toshiba ST400G	20	Recommended
11.	Toshiba ST400G21	25	Recommended

percentage of DC level for G_{r1} =50, are given. The percentage of voltage overshoot is determined from the turn-off switching load line as the difference of the maximum collector voltage and steady-state blocking voltage.

The table summarizes the severeness of voltage overshoot during turn-off. It is observed that some devices require a clamp circuit or a snubber circuit while other may not require snubber circuit at all. The conclusion is based on test results performed at the supply voltage of 300 V and with minimum parasitic lead length possible with our test circuit layout.

3.5.7 Antiparallel Diode and dv/dt Consideration

The reverse recovery characteristics of the antiparallel diode and the dv/dt turn-on characteristics of the
Darlington transistor are critical to the reliability of
motor drive power circuts. These two characteristics are
different in nature but the effect is the same. A
dangerously large turn-on transistor current spike may occur
if the diode characteristics or the dv/dt characteristics of
the transistor is improper. It will be explained in the
next paragraph how these characteristics affect the turn-on
current spike.

In a power circuit with a loop consisting of two serially connected power Darlingtons and a voltage source, the problem mentioned above may occur. Commonly-used two-

quadrant chopper for DC motor drive and bridge inverter for AC motor drive are two examples. The two-quadrant chopper will be used as an example to explain the effect of the two characteristics mentioned above:

- (1) Reverse recovery of the anti-parallel diode and,
- (2) dv/dt turn-on of the Darlington.

Fig. 3.6 shows a two-quadrant DC chopper circuit in which two Darlington modules are needed. When $\mathbf{Q}_{\mathbf{T}}$ conducts, current flows through $\textbf{Q}_{\textbf{T}}\text{, }\textbf{L}$ and the motor. When $\textbf{Q}_{\textbf{T}}$ cuts off, inductive current flows through \mathbf{D}_2 and transistor \mathbf{Q}_2 in reverse direction. The problem arises when $\mathbf{Q}_{\mathbf{T}}$ turns on again. A short circuit loop is formed by (V_s, Q_T, D_2) or (V_s, Q_T, Q_2) . D_2 is temporarily conducting in reverse direction because of stored charge. Q_2 is falsed turn-on because of dv/dt. The fact that a reverse current flows through Q_2 prior to Q_T conducting makes Q_2 more susceptible to false dv/dt turn-on. The severeness of the short circuit depends on the magnitude of source voltage, the parasitic impedance of the loop, the magnitude of free-wheeling current through the diode D_2 , and the transistor Q_2 . In this section, the Darlington transistors were evaluated in this respect. The test set-up and the results will be presented.

Test Set-Up

Fig. 3.6 shows the test set-up for evaluating the diode

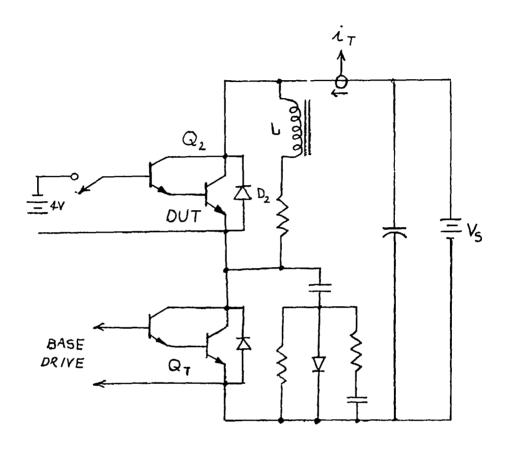


Fig. 3.6. Test set-up for dv/dt measurements

recovery and dv/dt turn-on characteristics of a Darlington transistor. When $\mathbf{Q}_{\mathbf{T}}$ conducts, current flows from source through the load and $\textbf{Q}_{\textbf{T}}.$ When $\textbf{Q}_{\textbf{T}}$ cuts off, inductive current freewheels through DUT (both the diode D_2 and the transistor Q_2) in reverse direction. When $Q_{\mathbf{T}}$ begins to conduct again, a large current spike may occur depending on the DUT characteristics. Collector current of DUT is measured at the instant of $\mathbf{Q}_{\mathbf{m}}$ turn-on. Because both the transistor and the anti-parallel diode are in modular package, it is not possible to distinguish the current spike caused by diode and by the transistor dv/dt. However, it has been proven earlier that both the diode and the transistor contributes to the turn-on spike. [Ref. 1] The measurement result is, therefore, a combined effect. In fact, from the user's point of view, the combined effect is of the most important concern.

Several conclusions are drawn from this evaluation:

The current spike caused by the combined effect of diode and transistor can be destructive. In some cases, the current spike is 5 or 6 times of the switched current level.

A drastic reduction of turn-on current spike can be accomplished by maintaining a reverse-bias drive on the DUT transistor when a high dv/dt is applied. The conclusion has ramifications on the design of base drive circuit.

From the manufacturer's specifications, all the anti-parallel diodes used in the Darlington modules are of fast recovery type. This is confirmed in the evaluation. The main cause for large current spike is false dv/dt triggering. As mentioned above, it is possible to minimize such triggering by proper design of base drive circuit.

3.5.8 Parallel Operation Consideration

Several devices out of the total eleven devices being tested have two devices in the same package. However, only Fuji EVM31-050 device has two devices separated, while for all others, the two devices are connected in totem pole configuration (see Table 3.1). Therefore, parallel operation of two devices in the same package is only possible for Fuji EVM31-050. The main concern in parallel operation of bipolar devices is the load-current sharing because of the positive current temperature coefficient and device characteristics (static and dynamic) spread. parallel operation characterization of the Fuji EVM31-050 was carried out by monitoring the current sharing of the two devices at different collector current levels, base drive conditions and case temperatures. Data are generated at case temperatures $T_c = 30^{\circ}C$ and $T_c = 100^{\circ}C$. The elevated tests were performed using controlled temperature temperature hot-plate.

At both case temperatures, current sharing was

monitored at three different load current levels, i.e., at 100 A; 100 A and 300 A. As the Fuji EVM31-050 is rated for the maximum current of 150 A, the maximum load current of 300 A is allowed for the two devices in parallel. In order to examine the effect of base drives on the collector current sharing the tests at $T_c=30^{\circ}\text{C}$ were performed for two different base drives, that is, $I_{B(tot)}=5$ A and 10 A.

From the data presented in Appendix C we can conclude that:

- very good static current sharing among the two paralleled devices exist at both case temperatures and at all collector current levels up to the maximum rated value.
- very good dynamic collector current sharing among the two paralleled devices exist at both case temperatures and at all collector current levels up to the maximum rated value.
- very good static and dynamic base current sharing exist for all base current drives employed in both forward and reverse directions and at both temperature levels.
- the only noticeable difference in base curent sharing was observed at the very end of the turn-on phase. One device carries more current than the othe. i.e., one waveform has current overshoot and the other undershoot. This causes some unbalance in the collector currents. After some time both base

currents become almost equal.

 at higher collector current levels, static current sharing is not quite equal. This is mainly caused by differences in current gains.

3.6 COMMENTS ON THE TEST RESULTS

Each of the devices were evaluated under various base drive conditions. Unlike the data provided by the manufacturer, which are normally obtained under a fixed drive condition, the results presented in this report enable the users to readily perform trade-off analysis.

- Good agreement was found between specific measurement point and the limited manufacturers data except for one device. A large discrepancy (2 to 1) of storage time (measured time is longer) was observed in Westinghouse's DA11503008 device.
- Significant reduction of storage time and fall time can be achieved by the use of the second base. 30% reduction was observed. The increase of switching speed, however, must be accompanied by the increase of base drive circuit complexity.
- Among the devices evaluated, Mitsubishi devices
 QM300HA-H and QM300HA-2H have the fastest current
 fall time, which may not be desirable as explained

in the following comment.

For electric car motor drive application, the transistor operating switching frequency is normally below 2 KHz. A very fast device is not necessary. In fact, a very fast turn-off device often requires large snubber to reduce the collector turn-off voltage spike to save level. Generally speaking, the device ruggedness reduces and conduction drop increases when the switching speed is increased.

For battery-charger application, however, higher switching frequency is desirable because of reduction in charging current ripple and inductor size. 20 KHz operation is often desirable.

The maximum operating frequency of the devices can be determined from the switching loss data and the conduction loss information. The following criteria are employed for the calculation of the maximum operating frequency:

- •• Maximum collector current
- •• Supply voltage V_{CC}=300V
- •• 50% duty cycle drive
- •• forward and reverse forced gain of 50

•• The devices can be operated at the maximum power dissipation level specified by the device manufacturer.

The value of the calculated maximum operating frequency along with switching and conduction power losses and the maximum possible device power dissipation are presented in Table 3.8.

 Transistor package plays an important role in getting user's acceptance.

Most of the devices have a discrete fast reverse recovery diode in the same power module except Westinghouse DA11503008.

For AC motor drive application in which a bridge inverter configuration is needed, the totem-pole power module (two transistors in series) is desirable for two reasons. First of the reasons is the convenience of inverter package. The second reason is that the snubbering requirement can be much reduced because of smaller parasitic inductance associated with the module. In fact, a snubber across the bus, instead of six separate snubbers across each transistor of the 3 phase inverter, is often adequate if totem-pole power modules are used.

Darlington in one package reduces not only the

Table 3.8 The Approximate Calculated Maximum Operating Frequency for the Duty Cycle 50% at the Maximum Rated Collector Current and $V_{\rm cc}$ =300V with $G_{\rm f}$ = $G_{\rm rl}$ = 50

No	Characteristic	Specified P _D [W]	Conduction loss [%]	Switching loss [%]	Maxımum frequency
	Device Type				<kh></kh>
1.	Westinghouse KD324510 *	620	10	90	15
2.	Westinghouse DA11503008	3000	10	90	10
3.	Fuji ETN81-055	1000	13	87	6
4.	Fuji EVM31-050	600	20	80	5
5.	Mıtsubıshı QM150DY-H	690	15	85	11
6.	Mitsubishi QM300HA-H *	1380	15	85	11
7.	Mitsubishi QM300HA-2H	1980	15	85	8
8.	Toshiba ST200M **	400	251	75	1
9.	Toshiba ST300M21	1500***	10	90	4.5
10.	Toshiba ST400G	400***	901	10	<<1
11.	Toshiba ST400G21	1500***	20	80	3.5

^{*}extrapolated for V_{cc} =300V

*** estimated using thermal resistance data because $\mathbf{P}_{\mathbf{D}}$ data are not given

 $^{**}G_{f} = 25$

problems with parasitic elements but also easier to assemble. Weestinghouse transistor DA11503008 is the only one with discrete device. A separate drive transistor is needed to form a Darlington. This is a distinct disadvantage.

Reverse recovery time of the anti-paralleled diode plays an important role in determining the overall reliability of the power transistor operating in the circuit. A very large turn-on current spike of the transistor may result from a slow reverse recovery of the anti-parallel diode of the opposite device in the totem-pole configuration such as a three-phase bridge inverter for AC drive or a two-quadrant chopper for DC drive. The large surge current may cause device failure due to forward- bias second breakdown or outright burnout of the bonding wire.

In a totem-pole connection, the transistor may be subjected to a sudden voltage rise. This dv/dt stress may cause the Darlington transistor to momentarily turn on and results in a large vurn-on spike current. It is essentially to apply a the device reverse blas to even when transistor is not conducting but its anti-parallel diode conducts. It is observed experimentally that by properly reverse bias the transistor, as

indicated above, the current spike can be reduced by 5 times.

• The current sharing (both collector current sharing and base current sharing) of two devices in one package under all conditions tested exhibits very good characteristics. Currents are fairly equally shared by the two paralleled devices at both 30° and 100°C. Bipolar transistor paralleling, in general, presents more problems than what was encountered in this investigation. It is suspected that the two chips in the same package are better matched. The good thermal coupling also helps the situation.

4.0 REVERSE BIAS SECOND BREAKDOWN TESTING OF BIPOLAR TRANSISTOR

4.1 INTRODUCTION

Reverse Bias Second Breakdown (RBSB) is a primary failure mode of power transistor when it is switched off under an inductive load. The ability of a transistor to withstand RBSB is directly related to safe operating area (SOA) of the transistor. However, the data provided by device manufacturers are, in general, very conservative estimates based upon certain destructive tests. The reason for such an inadequacy is that nondestructive testing is difficult, especially for large devices.

VPI&SU has initiated an effort, sponsored by NASA/DOE, to construct a nondestructive tester for such purposes in 1982. Nondestructive testing of RBSB is essential for two reasons. Firstly, a high power device is too expensive to perform a destructive test, and such a test can only provide a data point. Secondly, nondestructive testing enables one to obtain repetitively data points for the very same device under different driving conditions. The tester can be used effectively to perform parametric study of a device. The tester which was designed and fabricated at VPI&SU has been successfully tester at the rated capability 1000 V, 120 A.

In this chapter, RBSB test results will be given for the transistor types given in Table 3.1. For each transistor tested,

the results are documented by a set of oscillograms obtained under various drive conditions, and the data from each set of oscillograms are summarized by a Reverse Bias Safe Operating Area plot.

4.2 RBSOA CHARACTERIZATION

RBSOA characterization of a device can be established by repeatly performing the RBSB testing of the same devices under different operating conditions and drives. The RBSB testing has been performed on all devices listed in Table 3.1. devices the RBSB testing can be conducted successfully up to 120 A, the maximum capability of the tester, while for other devices the non-destructive RBSB testing can only be performed at a lower current levels. In general, the device RBSOA can be characterized after accumulating sufficient RBSB test data which are performed at various collector current levels and different forward and reverse base currents. For four-terminal devices an addition reverse drive for the second base, also, has been applied and conditions for RBSB has been determined. In addition, some devices have been tested at the room temperature as well as elevated temperature.

4.3 TEST RESULTS PRESENTATION FORMAT

A large amount of data was acquired during the nondestructive second breakdown characterization of the devices listed in the Table 3.1. All test results are presented in the form of oscillograms as shown in Appendix D. For reader's convenience these results are also presented in a graphical form, i.e., RBSOA plots which, in essense, summarizes the test results presented in the Appendix D.

4.3.1. INTERPRETATION OF OSCILLOGRAMS

Figures D.1.1 to D.13.6 show the oscillograms of the test results for DUT under various circuit conditions. Take Fig. D.1.1 as an example. A family of three V_{CE} waveforms is recorded in this figure. Each waveform corresponds to a different forward base current. As can be seen from the figure, V_{CE} waveforms start at nearly zero voltage, corresponding to the turn-on of the device. When the base drive turn-off signal is applied, the voltage V_{CE} rises to a peak magnitude at which second breakdown occurs and V_{CE} drops sharply. The fast dv/dt reduction of the V_{CE} waveform triggers the shunt circuit. The shunt circuit quickly diverts the collector current from the device and saves the device from permanent damage. From the figure, it can be seen that the breakdown voltage is 760 V when forward base current I_{BF} is 2 A. All the three tests were conducted at collector current of 20 A.

4.3.2 RBSOA PLOTS

Fig. 4.1 is a typical RBSOA plot obtained from data point documented in the oscillograms (Fig. D.1.1 to Fig. D.1.15). This is a plot of breakdown voltage and collector current levels for different forward and reverse base current levels. The collector current levels at which the device were tested are 20 A, 40 A, 60 A, 80 A, and 100 A. For example, point [1] at the upper right corner in Fig. 4.1 refers to forward base current $I_{\rm BF}=2$ A and reverse base current of $I_{\rm BR}=4$ A. The transistor second breakdown occurs at 100 A and 730 V. The dotted line indicates the data given by manufacturer. Although the given data is conservative compared with most of the measured data, there is a data point inside the RBSOA.

4.4 TEST DATA ANALYSIS

In this section, discussion of the RBSOA data for each device are presented. Prior to the discussion, it is important to note that the non-destructive second breakdown testing performed on these devices, in some cases, is not fully non-destructive. In fact after certain number of RBs3 testings, one can observe some degree of degradation on certain devices, particularly at high collector current level. On the other hand, for some devices the repetitive non-destructive testing can be performed at the maximum rated tester current (120 A). It would be desirable to relate the difference in the RBSOA properties to the internal structure of the devices. This is, however, not

within the present scope of investigation.

Because the limited number of data points can be obtained before a discernable degradation can occur, the most complete RBSOA characterization are obtained using more than one device. For example in Fig. 4.1 a most complete RBSOA data of the Westinghouse KD324510 are presented. However, these data are obtained from three devices. The specific test data obtained in each device are listed in Fig. 4.2 to 4.4.

4.4.1 THE RBSOA TEST DATA AT ROOM TEMPERATURE

In the following sections, the interpretation of the measured RBSOA characteristics of each device is presented. All RBSOA test results were obtained at the case temperature $T_C=30\,^{\circ}\text{C}$. Only the first base was used for turning off all power devices except, for the Westinghouse DA 11503008.

• Westinghouse KD 324510

The complete RBSOA characterization of the device was performed using three devices for the collector current up to 100 A. The plots of the tests results are given in the plots Fig. 4.1 to Fig. 4.4. Fig. 4.1 represents the combined measured RBSOA for all three devices, while fig. 4.2 to 4.4 represent the RBSOA of individual devices. From the plots, it can be seen that, in general, the manufacture specified RBSOA is conservative. However, some measurement data are well within the specified RBSOA. In fact, the measured point for the reverse base current $I_{\rm RB}$ =2A are all outside the specified

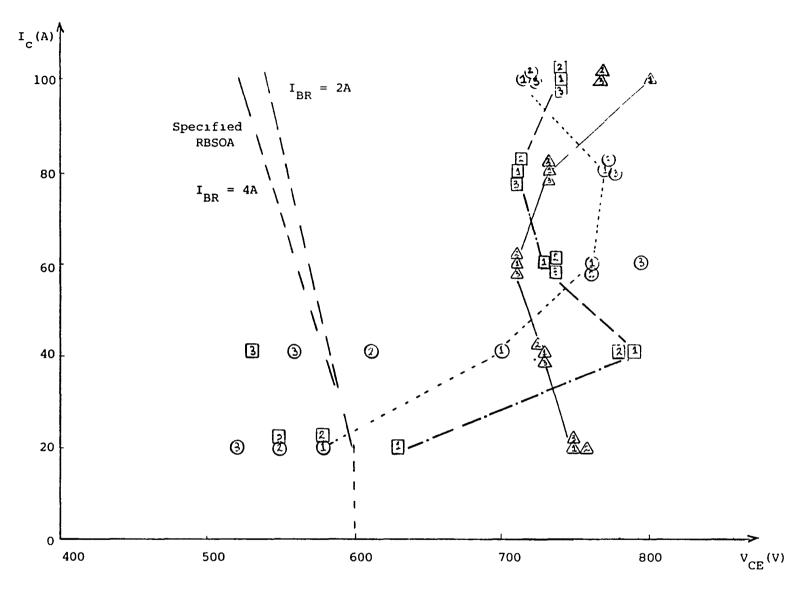


Fig. 4.1. Measured RBSOA for the Westinghouse KD324510 for $I_{BF} = 2 \text{ A(1)}$; $I_{BF} = 4 \text{A(2)}$; $I_{BF} = 8 \text{A(3)}$ and $I_{BR} = 2 \text{ A(\triangle)}$; 4A(\bigcirc) ; 8A(\bigcirc) . Measured points obtained using three devices, i.e., plot represents combined RBSOA for three devices. Individual RBSOA plots for each device are given in Figs. 4.2 to 4.4.

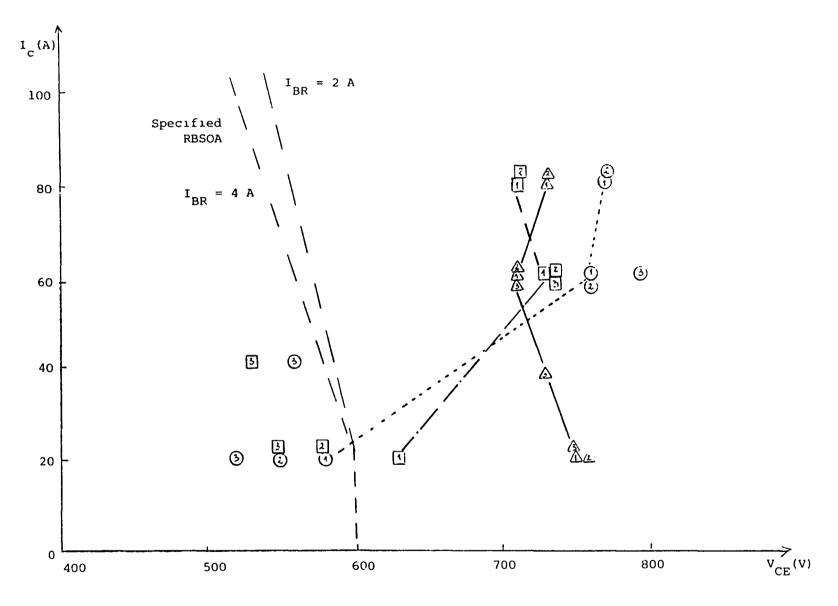


Fig. 4.2. Measured RBSOA for the Westinghouse KD324510 for $I_{BF}=2$ A(1); $I_{BF}=4$ A(2); $I_{BF}=8$ A(3) and $I_{BR}=2$ A(\triangle); 4 A (\square); 8 A (\bigcirc). All points measured on the same device.

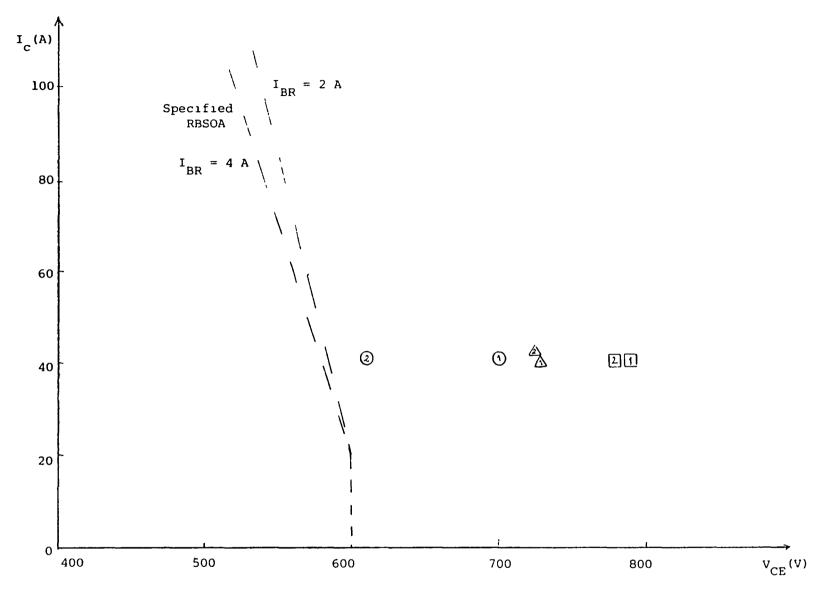


Fig. 4.3 . Measured RBSOA for the Westinghouse KD324510 for $I_{BF}=2$ A(1); $I_{BF}=4$ A(2); $I_{BF}=8$ A(3) and $I_{BR}=2$ A(\triangle); 4 A (\square); 8 A (\bigcirc). All points measured on the same device.

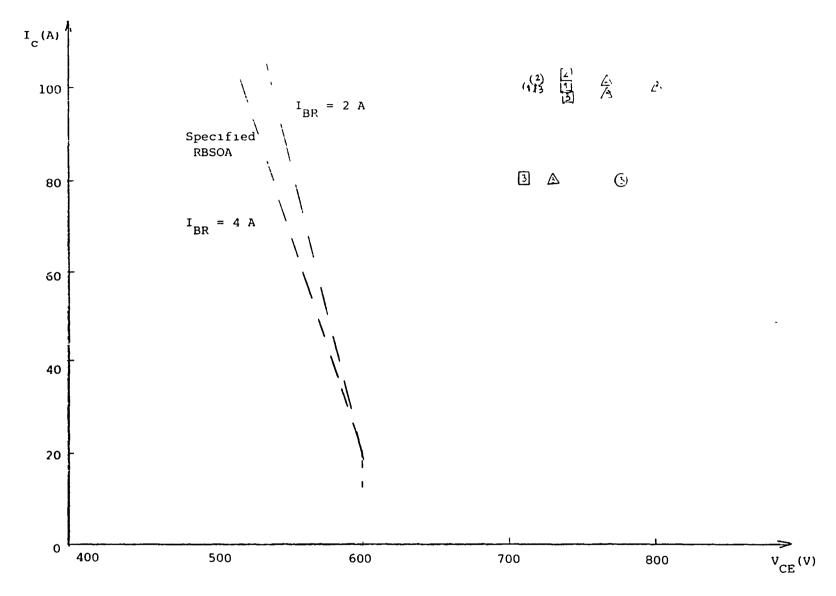


Fig. 4.4. Measured RBSOA for the Westinghouse KD324510 for I_{BF} = 2 A(1); I_{BF} = 4 A(2); I_{BF} = 3 A(3) and I_{BR} = 2 A(\triangle); 4 A (\square); 8 A (\bigcirc). All points measured on the same device.

RBSOA. For I_{BR} =4A some measurement data at lower collector current range are inside the specified RBSOA.

Moreover, it can be seen that the RBSOA are affected by the forward and reverse base drive conditions. Increase of the reverse drive or forward drive may decrease or increase the RBSBA voltage depending on the collector current level. In general one can state that the influence of the reverse drive on the RBSOA characteristic is usually stronger then the forward base drive.

• Westinghouse DA 11503008

The plot of measured points of RBSOA for Westinghouse DA 11503008 is given in Fig. 4.5. It is interesting to note that the measured RBSOA points are obtained using the second base drive. If one merely use only first base drive in RBSOA testing of DA 11503008, a second breakdown could not be induced at all current levels even for a very strong base drives.

As an example, in Appendix D fig. D. 2.2 represents an attempt to breakdown DA 11503008 at 100 A collector current with I_{BR}=16A trough first base. Oscillogram shows no occurance of second breakdown event. To explain such behavior of the Westinghouse DA 11503008 we have to recall that DA 11503008 is descrete Darlington and that it was tested without using any resistor across the base-emitter junction of the input device. During the turnoff the stored charge in the input device is removed with the reverse current and input device (smaller device) turns-off first. Consequently the stored charge in the output device can not be removed through base, but rather must

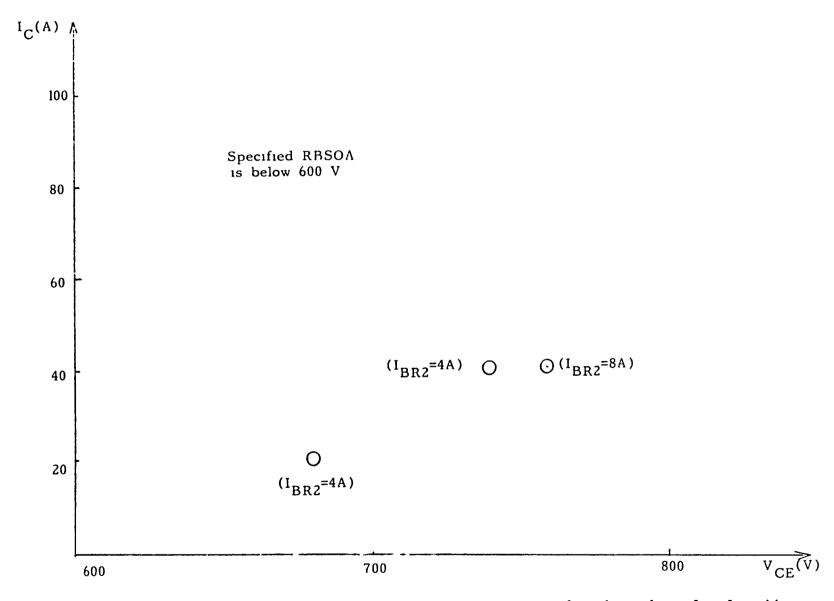


Fig. 4.5. Measured RBSOA for the Westinghouse DAll53008 for the constant first base drive $I_{\rm BF} = I_{\rm BR} = 4\Lambda$ and different second base drive conditions as it is shown on the plot. Using only the first base drive second breakdown could not be induced at all tested collector current levels up to 120A.

recombine. Since during turn-off phase the base of the output device is essencially, open, no severe non-uniform collector current flow is possible and SB does not occur. In fact, the device turns off in sustaining mode of operation, i.e., the collector voltage stays at primary breakdown voltage during the inductor discharge.

When the second drive is employed device goes to SB because the second base current causes current constriction of the collector current of the output device. In fig. D.2.3 (Appendix D) the two tests with and without second base drive, when other conditions are the same, are shown.

Few measured data of RBSOA are shown to be outside of the specified RBSOA. Specified RBSOA lies below the 600V line. High curent RBSB testing was not successful in the discrete Darlington case, i.e., for the DAll503008 device.

• Fuji ETN81-055

The RBSOA for Fuji ETN81-055 were measured using two devices up to 100A collector current. The measured data are presented the figs 4.6-4.8. In fig. 4.6 the combined RBSOA for both devices are given, while in fig. 4.7 and fig. 4.8 the RBSOA for the individual transistors are shown. Again, as in the case of the Westinghouse KD324510, the RBSOA depends strongly on the reverse base current as well as forward base current. All measured points, except two points, are outside of the specified RBSOA for $I_{RR}=6$ A at $T_{C}=125$ °C.

The two measured data inside the specified RBSOA region were obtained immediately before device failure although no apparent

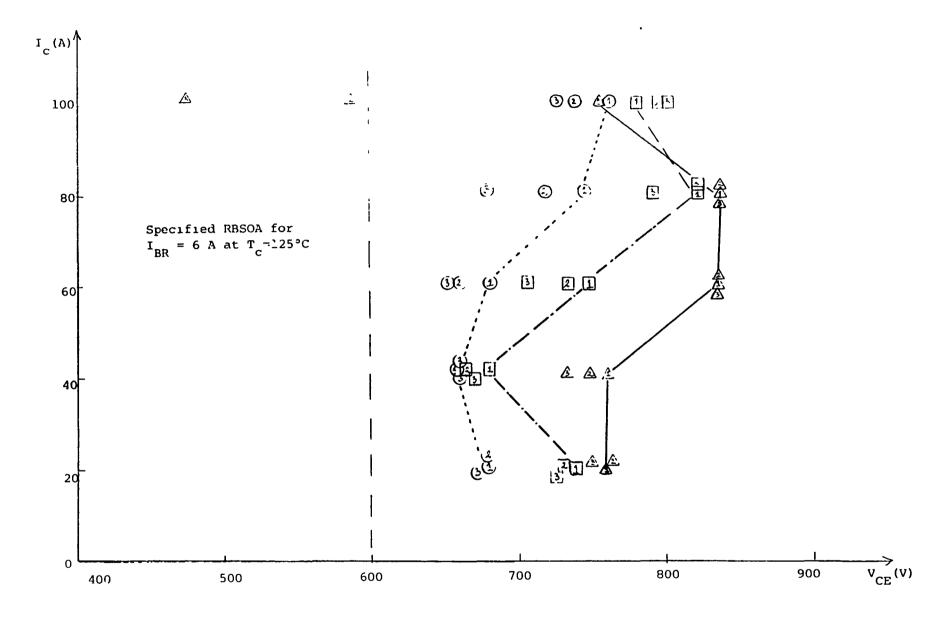


Fig. 4.6 . Measured RBSOA for the Fuji ETN81-055 for $I_{BF}=2$ A (1); $I_{BF}=4$ A (2); $I_{BF}=8$ A (3) and $I_{BR}=2$ A(\triangle); 4 A (\square); 8 A (\bigcirc). Measured points obtained using two devices, i.e. plot represents combined PBSOA for two devices.

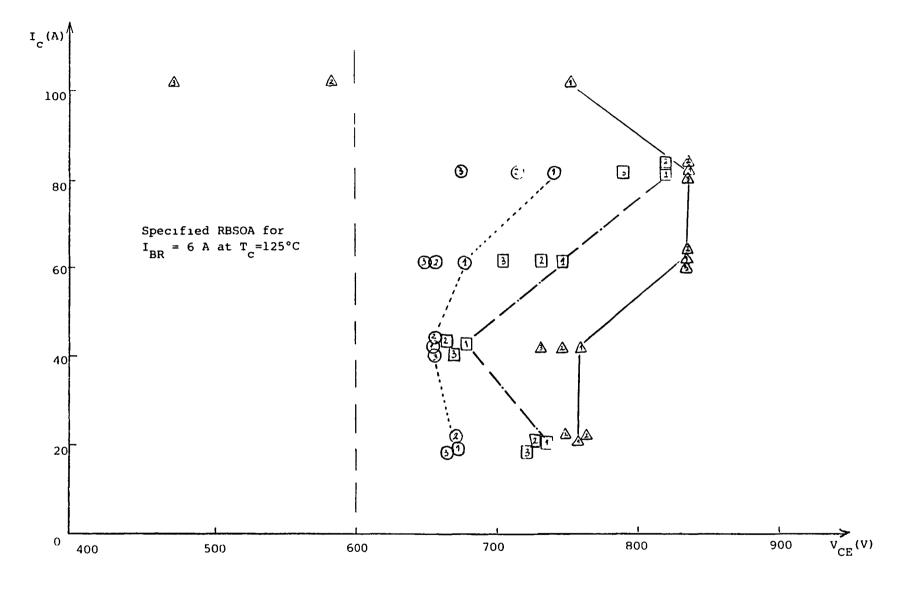


Fig. 4.7. Measured RBSOA for the Fuji ETN81-055 for $I_{BF} = 2 \text{ A(1)}$; $I_{BF} = 4 \text{ A (2)}$; $I_{BF} = 8 \text{ A (3)}$ and $I_{BR} = 2 \text{ A ($\triangle$)}$; $4 \text{ A ($\square$)}$; $8 \text{ A ($\square$)}$. All points measured on the same device.

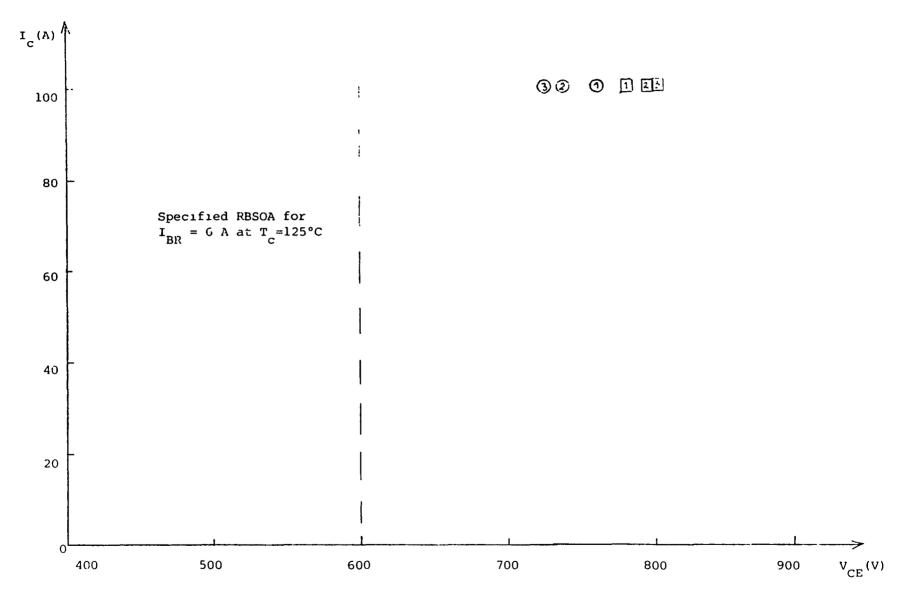


Fig. 4.8 . Measured RBSOA for the Fuji ETN81-055 for I_{BF} = 4 A (2); I_{BF} = 8 A (3) and I_{BR} = 2 A(\triangle); 4 A (\square); 8 A (\bigcirc). All points measured on the same device.

degradation of the device characteristics were observed.

• Fuji EVM 31-050

In RBSOA characterization of the Fuji EVM 31-050 only one device were used for the entire current range up to 120 A. The measured RBSOA plot is shown in Fig. 4.9 along with the specified RBSOA for $I_{\rm RD}$ =4A.

From the plot in Fig. 4.9 it can be clearly seen that all measured points, except three at the collector current of 20 A, are outside the specified RBSOA. However, all three points inside the specified RBSOA correspond to the reverse base drive of I_{BR} =2A. All measured point for I_{BR} =4A are outside the specified RBSOA. In addition, the measured points at higher current levels (>60A) are shown to be substantially outside the specified RBSOA.

Mitsubishi QM150DY-H

The RBSOA measured for the Mitsubishi QM150DY-H under different base drive conditions is given in Fig. 4.10. For each collector current level a different device was used because of device failure after several tests. Since the Mitsubishi QM150DY-H was tested up to 60A collector current the RBSOA in fig. 4.10 represents combined RBSOA area for three devices. As no manufacturer's specification concerning RBSOA are given comparison can not be made.

However, for al! measured points the second breakdown voltage is higher then 550V.

• Mitsubishi QM300HA-H

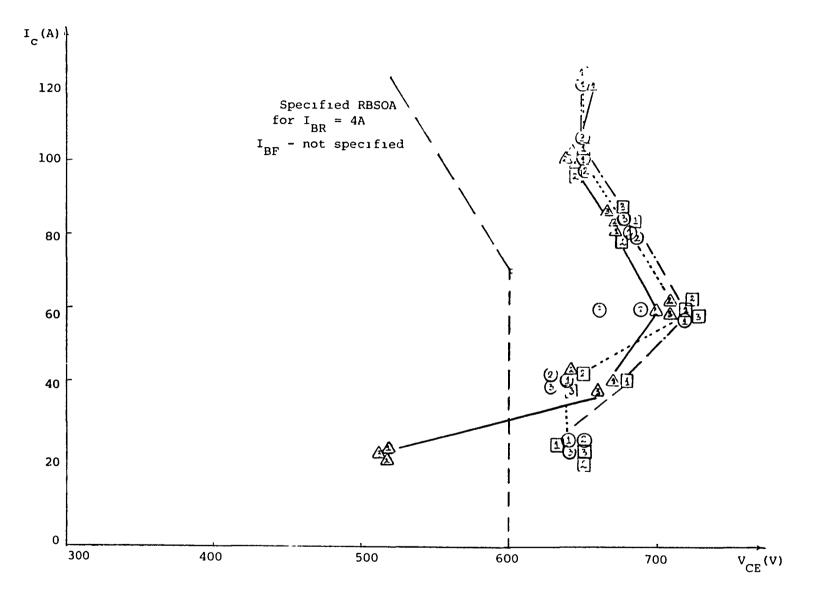


Fig. 4.9 Measured RBSOA for the Fuji EVM31-050 for I_{BF} = 2A(1); I_{BF} = 4A(2); I_{BF} = 3A(3); and I_{BR} = 2A (\triangle); 4A (\bigcirc); 8A (\bigcirc). All points belong to the same device.

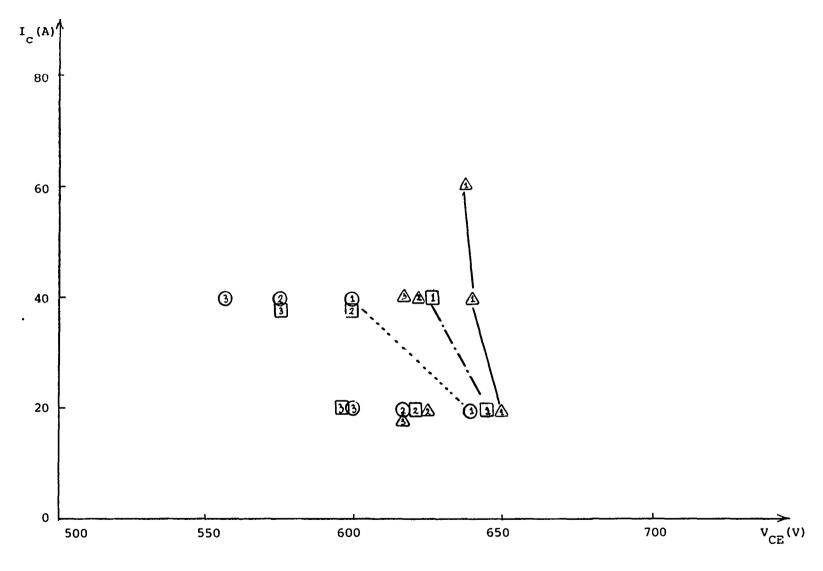


Fig. 4.0. Measured RBSOA for the Mitsubishi QM150DY-H for $I_{BF} = 2$ A (1); $I_{BF} = 4$ A (2); $I_{BF} = 8$ A (3) and $I_{BF} = 2$ A (\triangle); 4 A (\square); 8 A (\bigcirc). For each collector current level measured points belong to different devices, i.e. the plot represents combined RBSOA for three devices.

For this device only few successful tests could be performed and those scattered points are shown in fig. 4.11. Along with manufacturer specified RBSOA for I_{BR} =4A. As the matter of fact, the RBSB tester was capable to perform non-descriptive testing only at limited cases. From Fig. 4.11 one can observe that at the collector current of 80 A the second breakdown voltage is between 500V and 600V depending on the forward base current.

• Mitsubishi QM300HA-H-2H

The Mitsubishi QM300HA-H device is a high-voltage high-current device rated at $V_{\rm CEO}=1000{\rm V}$. Because the clamp voltage limitation of the second breakdown tester (max. clamp voltage around 1100V), the second breakdown phenomenon could not take place even at the maximum tester current $I_{\rm C}=120{\rm A}$ and high current base drive $I_{\rm BR}=16{\rm A}$ as it is illustrated in Fig. D.7.1 in Appendix D. As we see from fig. D.7.1 device voltage during turn-off reaches a present clamp voltage and stays at that voltage while the inductor energy discharges.

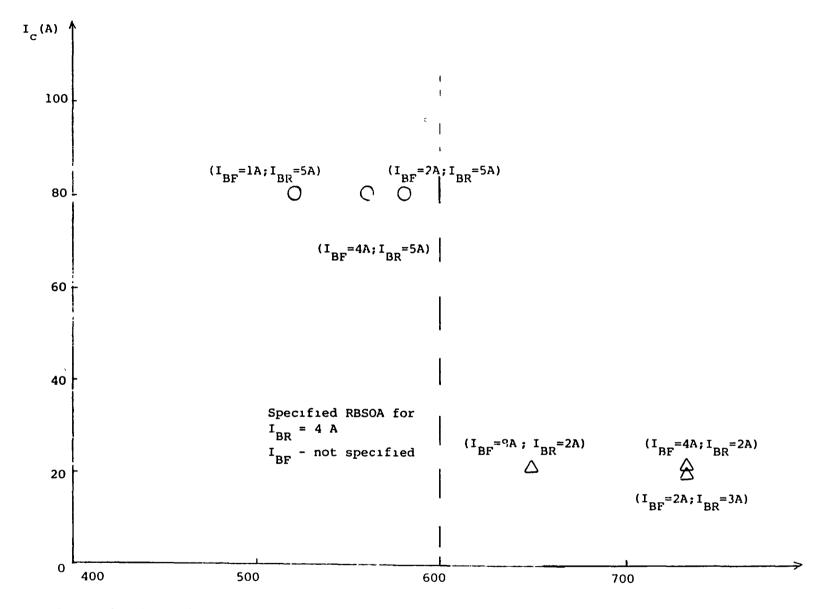


Fig. 4.11. Measured points of RBSOA for the Mitsubishi QM300HA-H for $I_{BR} = 2$ A (!) and $I_{BR} = 5$ A (?); and different forward base drives as it is designated in the plot. For each collector current level measured points belong to the different devices, i.e., plot represents combined RBSOA for two devices.

• Toshiba ST200M

The RBSOA characterization of the Toshiba ST200M device was done using only one device for the entire collector current range, i.e., from 20A up to 120A. The obtained results are shown in fig. 4.12. From fig. 4.12 We can see that at the lower collector currents (<40A) the RBSOA extends to higher collector voltages (>700V), while at the higher collector current (>60) the breakdown voltage is considerably smaller, (<600V). In fact, from fig. 4.12 it is clear that the measured points are grouped in two distinctive groups depending on the collector current level with transitional collector current level around 60A. To verify the measured results, i.e., to verify that the second breakdown testing hasn't altered the RBSB characteristics of the DUT, we had performed two additional tests. Naimly, after full RBSOA characterization we tested the device again in the lower current range ($I_c=20A$ and 40A) under the same base conditions as we had done before. results are shown in figs. D.8.16 and D.8.17 and from those we can conclude that SB characeristic didn't change even after fifty four repeatative tests. In addition, we also didn't observe any change in collector leakage current. manufacture data concerning RBSOA characteristic are available for this devices.

• Toshiba ST300M21

The measured RBSOA for the Toshiba ST300M21 is given in fig. 4.13. In the RBSB testing three devices were used, i.e., the collector current levels of 20A and 40A were characterized

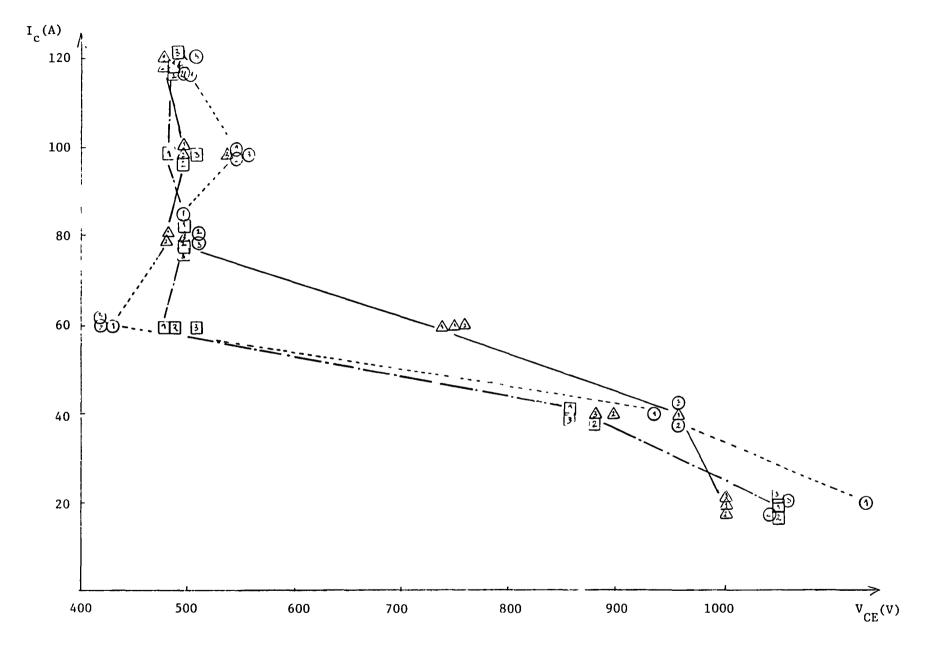


Fig. 4.12. Measured RBSOA for the Toshiba ST200M for I_{BF} =2A(1); I_{BF} =4A(2); I_{BF} =8A(3) and I_{BR} =2A(\triangle); 4A(\square); 8A(O). All points belong to the same device.

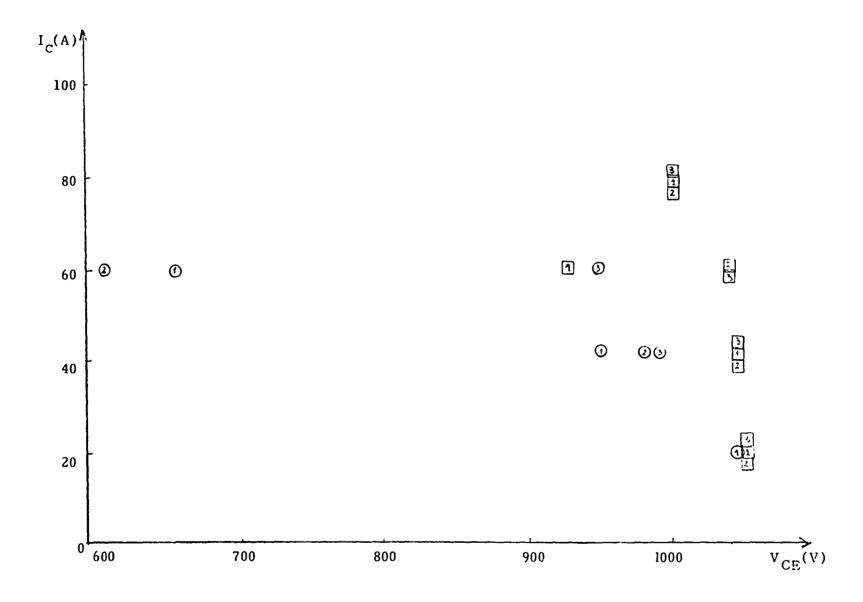


Fig. 4.13 . Measured RBSOA for the Toshiba ST300M21 for I_{BF} =2A(); I_{BF} =4A(2); I_{BF} =8A(3) and I_{BR} =2A(\triangle); 4A(\square); 8A(\bigcirc). Measured points belong to three different devices, i.e. points for 20 A and 40 A belong to one, for 60 A to another and 80 A to a third device.

using one device, while for the collector current levels of 60A and 80A one device for each level was used for RBSOA characterization. The Toshiba ST300M21 device is rated at $V_{\rm CEO}^{=900V}$. As we see, except two point at $I_{\rm C}^{=60A}$ all measured points have the second breakdown voltage in excess of 900V.

Somewhat surprising results were obtained at I_C =60A where two points belonging to I_{BR} =8A have considerably lower second breakdown voltage (in the range of 600V to 700V). Also, from the oscillograms in Appendix D, it can be seen that second breakdown can not be initiated for some base drive conditions (for example Fig. D.9.1) In fact, no second breakdown mode of operation can be observed at all collector current levels for the reverse base drive of I_{BR} =2A.

• Toshiba ST400G21

The RBSOA characterization for the Toshiba ST400G21 device were performed up to 60A using two devices.

At the collector current levels above 60A no non-destructive test was possible, i.e., only one test was performed at that level successfully. From limited number of data shown in Fig. 4.14 it can be seen that the range of second breakdown voltage for this device, up to 60A collector current, is around 500V to 600V. No manufacturer's data for this device is available.

• Toshiba ST400G

No RBSOA measurement result of these devices is available because all four devices were destroyed during other dynamic

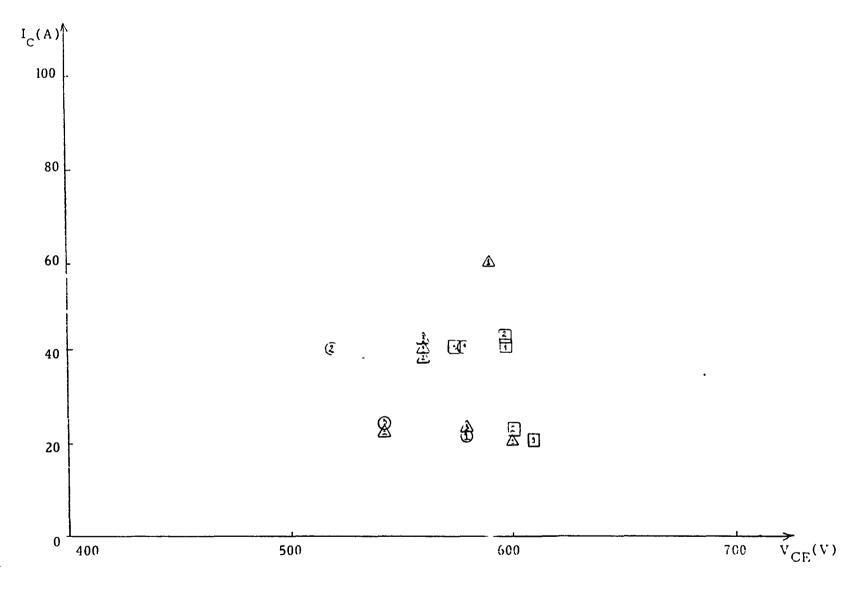


Fig. 4.14. Measured RBSOA for the Toshiba ST400G21 for I_{BF} =2A(1); I_{BF} =4A(2); I_{BF} =8A(3) and I_{BR} =2A(\triangle); 4A(\square); 8A(\bigcirc). Measured points belong to two different devices, i.e. points for 20 A and 40 A level belong to one and the point at 60 A to another device.

testings.

4.4.2 THE RBSOA TEST DATA AT ELEVATED TEMPERATURE

The Westinghouse KD324510 device was characterized for RBSOA at the elevated case temperature $T_C=100^{\circ}C$. The test results are summarized in nine plots, i.e., in figs 4.15 to 4.23 using the oscillograms from Appendix D (section D.12). The plots present simultaneously the RBSOA characteristics at $T_C=30^{\circ}C$ and $T_C=100^{\circ}C$ under different base drive conditions. From the given plots we can conclude that the temperature influence on RBSOA strongly depends on base drive conditions and collector current level. These effects can be summarized as follows:

- For the same collector current level, the RBSB voltage at the elevated temperature can be higher or lower than that at the room temperature, depending on the base drive conditions (see figs. 4.15 and 4.16 for $I_C=40A$, for example)
- For the same base drive the temperature effect on the RBSB voltage depends on the collector current level. At low current level (I_C =20A) and high current level (I_C =80A), the RBSB voltage increases with the temperature. However, at the current range, I_C =40 60A, no clear relation can be observed between the breakdown voltage and the case temperature.
- It appears that for a weak reverse drive, the RBSB voltage increases with the case temperature, while for a stronger reverse base drive, the breakdown voltage can be either increased or decreased as the case temperature rises.

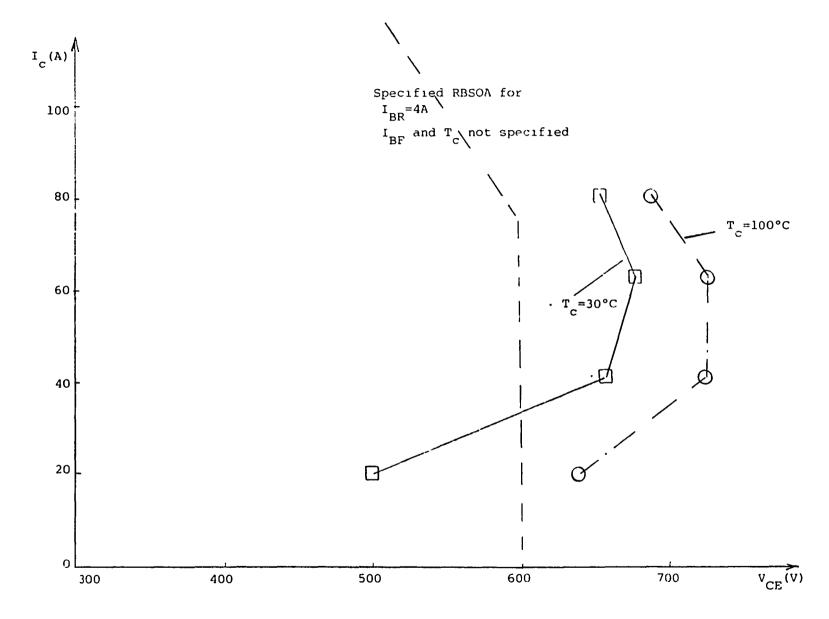


Fig. 4.15. Measured RBSOA for the Fuji EVM31-050 for I_{BF} = 2 A and I_{BR} = 2 A for two different case temperatures. (\Box - case temperature T_{C} = 30°C; \bigcirc - case temperature T_{C} = 100 °C)

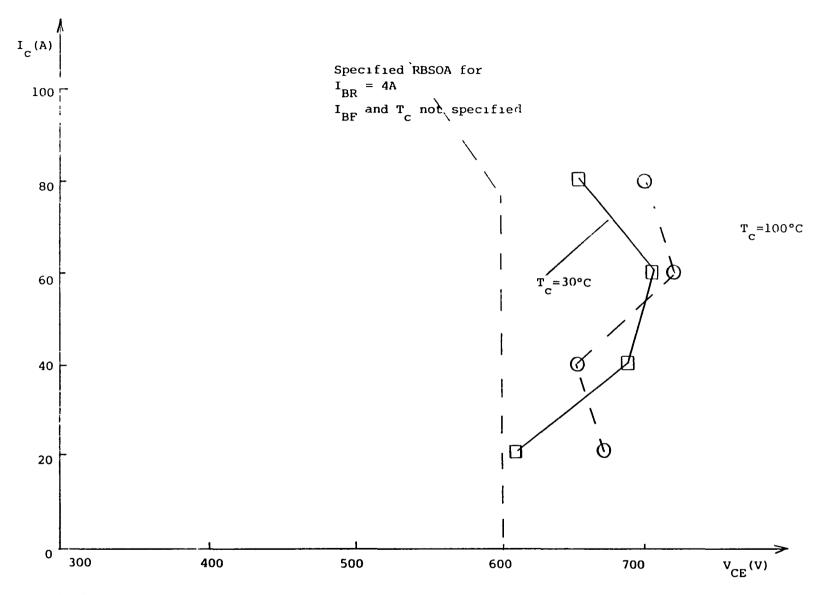


Fig. 4.16. Measured RBSOA for the Fuji EVM31-050 for $I_{BF} = 2A$ and $I_{BR} = 4A$ for two different case temperatures. (\Box - case temperature $T_{C} = 30$ °C; $\dot{\Box}$ - case temperature $T_{C} = 100$ °C)

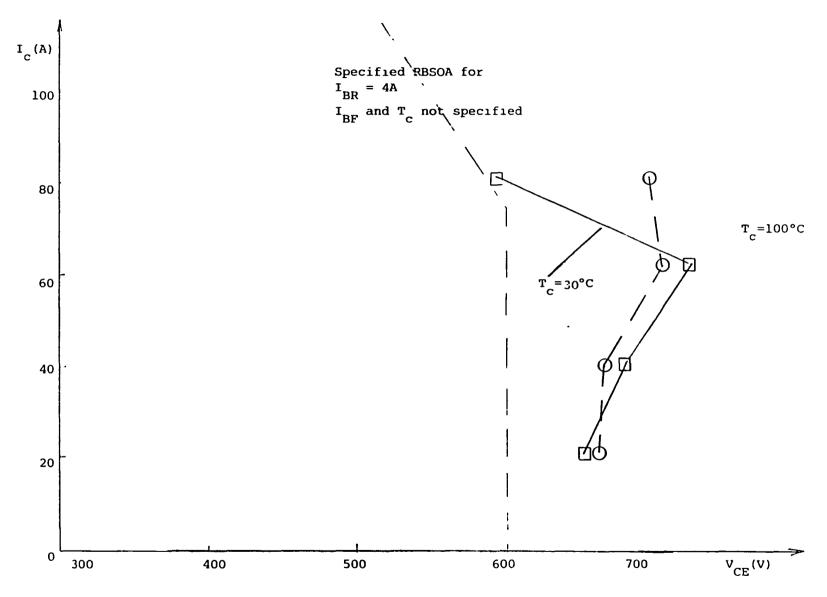


Fig. 4.17. Measured RBSOA for the Fuji EVM31-050 for I_{BF} = 2 A and I_{BR} = 8A for two different case temperatures. (— case temperature T_{c} = 30°C; — case temperature T_{c} = 100°C)

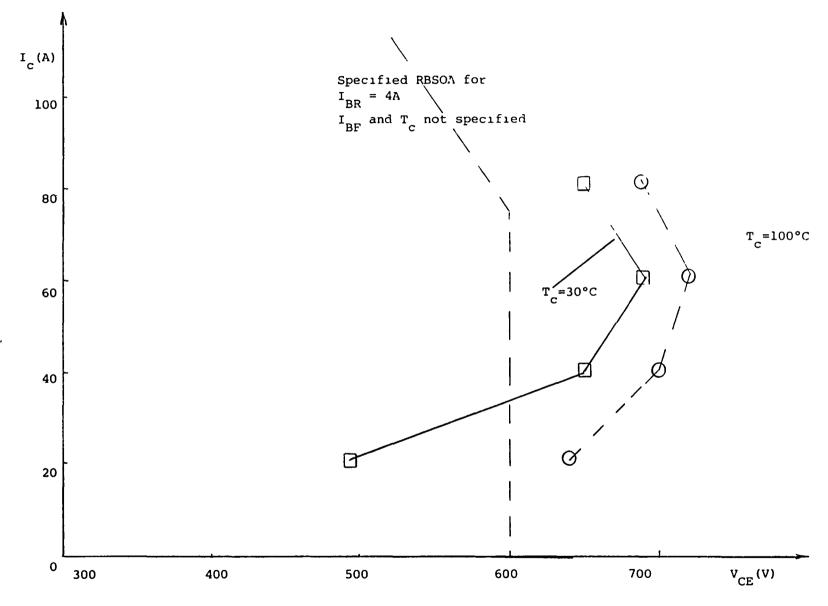
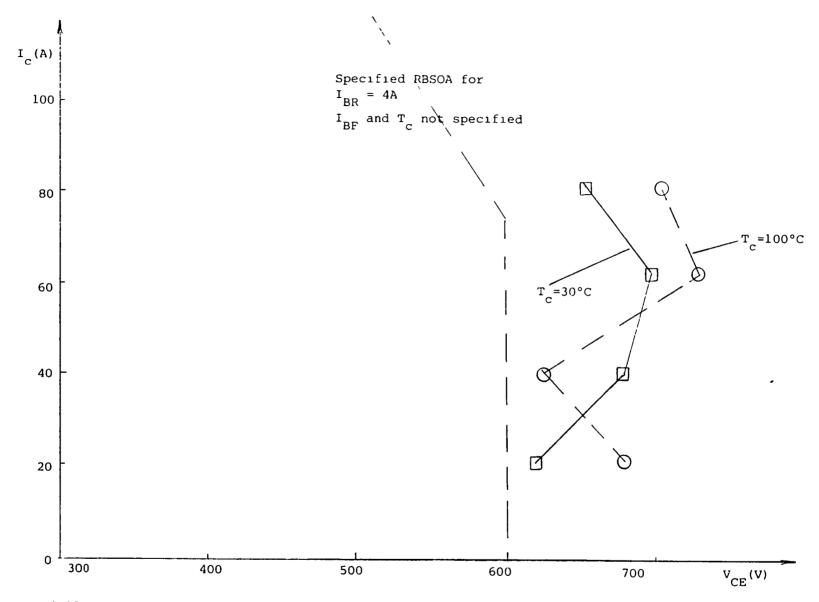


Fig. 4.18. Measured RBSOA for the Fuji EVM31-050 for $I_{BF} = 4$ A and $I_{BR} = 2$ A for two different case temperatures. (- case temperature $T_{c} = 30$ °C; - case temperature $T_{c} = 100$ °C)



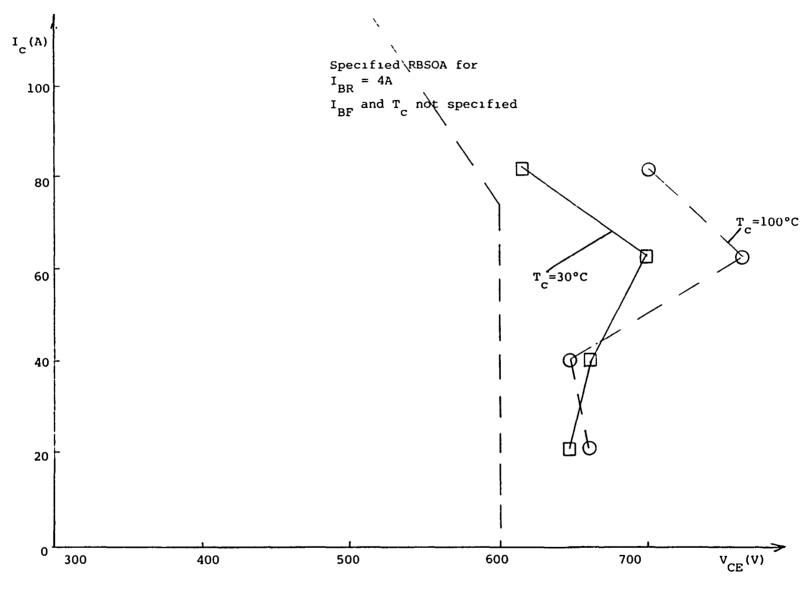


Fig. 4.20. Measured RBSOA for the Fuji EVM31-050 for $I_{BF} = 4$ A and $I_{BR} = 8$ A for two different case temperatures. (\Box - case temperature $T_{C} = 30$ °C; \bigcirc - case temperature $T_{C} = 100$ °C)

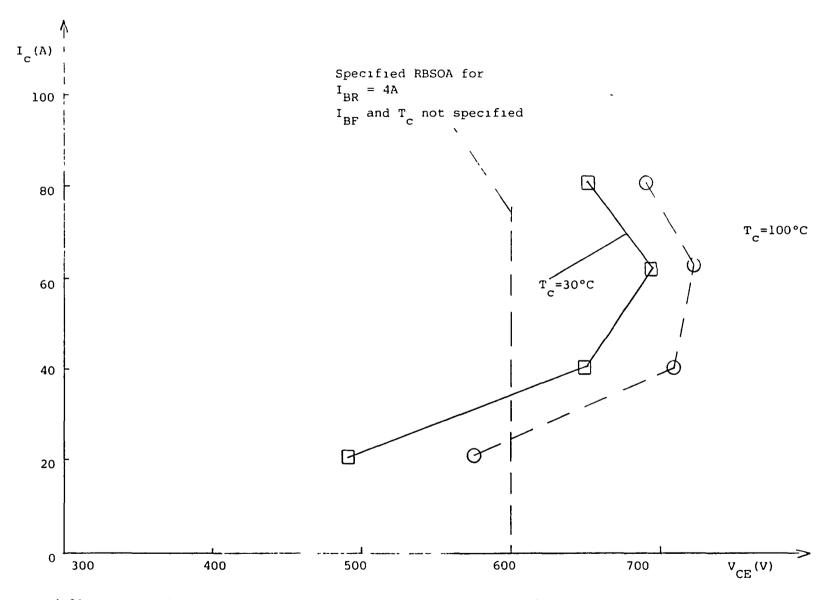


Fig. 4.21. Measured RBSOA for the Fuji EVM31-050 for $I_{BF} = 8$ A and $I_{BR} = 2$ A for two different case temperatures. ([]- case temperature $T_{C} = 30$ °C; () - case temperature $T_{C} = 100$ °C)

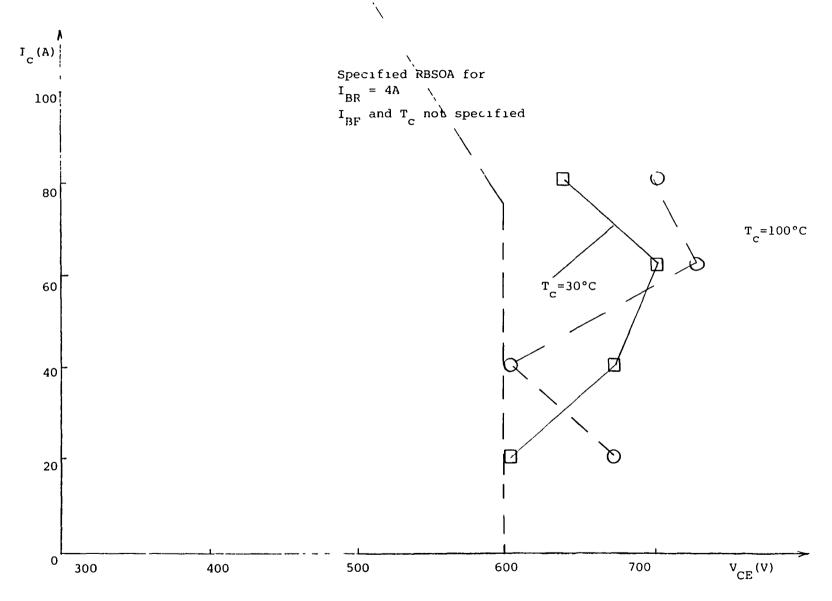


Fig. 4.22. Measured RBSOA for the Fuji EVM31-050 for $I_{BF} = 8$ A and $I_{BR} = 4$ A for two different case temperatures. (\Box - case temperature $T_{C} = 30$ °C; \Box - case temperature $T_{C} = 100$ °C)

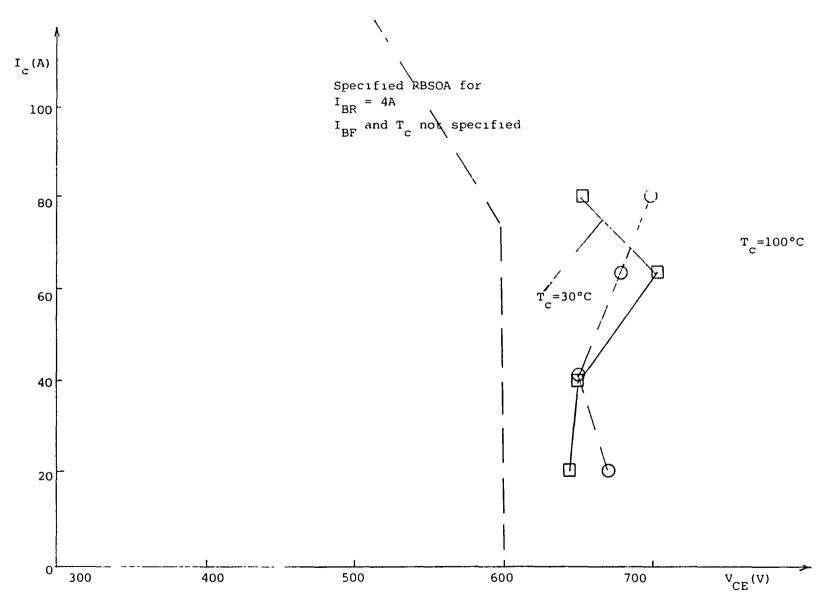


Fig. 4.23. Measured RBSOA for the Fuji EVM31-050 for I_{BF} = 8 A and I_{BR} = 8A for two different case temperatures. (\Box - case temperature T_{C} = 30°C; \bigcirc - case temperature T_{C} = 100°C)

• The breakdown voltage under the same base drive and at the same collector current level can vary as much as 150V as the case temperature is varied from 30°C to 100°C. (see Fig. 4.18, for example).

4.4.3 THE RBSOA CHARACTERISTICS WITH A SECOND BASE DRIVE

Influence of the second base drive on RBSOA was investigated using the Westinghouse KD324510 device. The test results, i.e., the RBSOA plots with and without the second base drive employed are shown in fig. 4.24 to 4.26 for three different base drive conditions. In fact, for all three plots the forward base current and the second base reverse current were held constant ($I_{\rm BF}$ =4A, $I_{\rm BR2}$ =4A). Only the first reverse base current was varied ($I_{\rm BR}$ =2,4,8A). Each plot presents the RBSOA with and without the second base drive employed so that influence of the second drive can be clearly seen.

As we can observe from figs. 4.24 to 4.26, the influence of the second base drive on RBSOA is very complex. However, it appears that the second base drive has a stronger effect at lower collector current levels, at which the second base drive tends to reduce the RBSOA.

4.5 CONCLUSION

From the tests results obtained we can draw the following conclusions concerning RBSOA characteristics of the high power

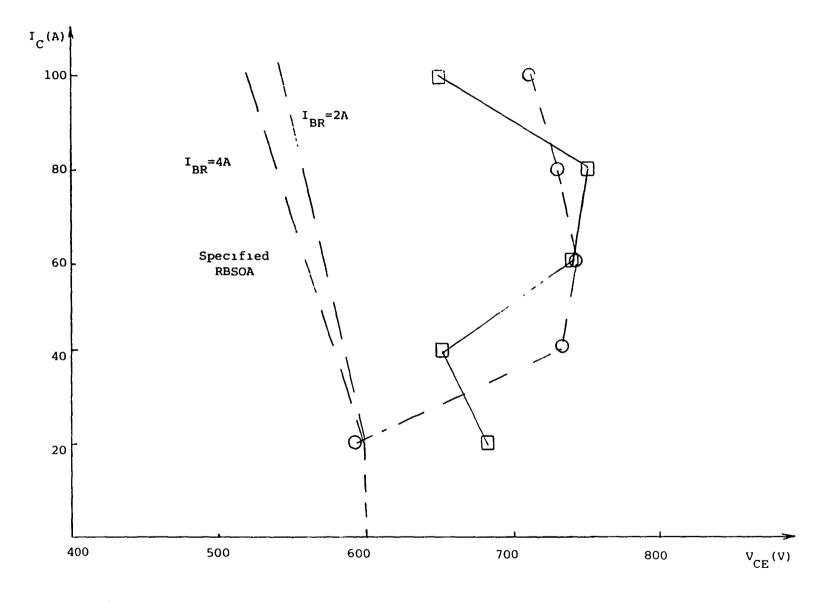


Fig. 4.24. Measured RBSOA for the Westinghouse KD324510 without the second base drive (\bigcirc) and with the second base drive (\bigcirc) for $I_{BF}^{=4A}$; $I_{BR}^{=2A}$; $I_{BR2}^{=4A}$. (\bigcirc - no 2nd base drive; \bigcirc - with 2nd base drive)

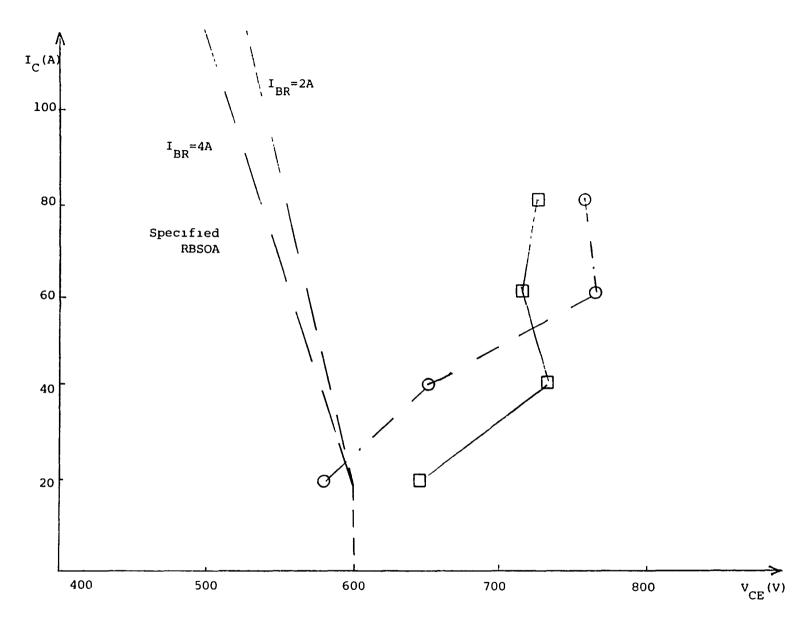


Fig. 4.25. Measured RBSOA for the Westinghouse KD324510 without the second base drive (\bigcirc) and with the second base drive (\bigcirc) for T_{BF}=4A; I_{BR}=4A; I_{BR2}=4A (\bigcirc - no 2nd base drive; \bigcirc - with 2nd base drive)

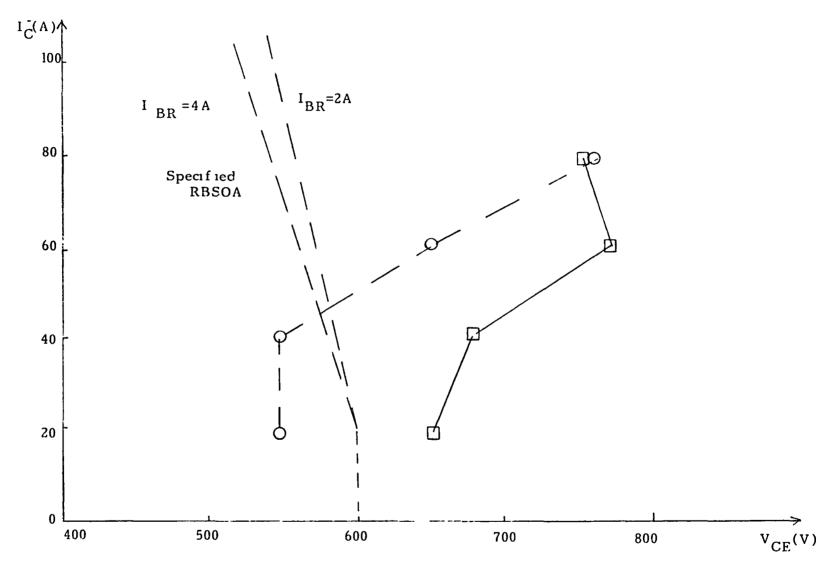


Fig. 4.26. Measured RBSOA for the Westinghouse KD324510 without the second base drive ([]) and with the second base drive ([)) for $I_{BF}=4\Lambda$; $I_{BR}=8\Lambda$ and $I_{BR2}=8\Lambda$. ([] - no 2nd base drive; [] - with 2nd base drive)

bipolar devices:

- 1. The RBSB behavior of a Darlington transistor depends on the magnitude of the reverse-base current. For a strong reverse-base drive, breakdown usually occurs before V_{CE} reaches $V_{CE(SUS)}$ The breakdown voltage may be greater than or lower than $V_{CE(SUS)}$ and may either increase or decrease with the reverse base current depending on devices. For a weak drive, the breakdown could occur several microseconds after the Darlington transistor reaches the sustaining mode. As with the single BJT device, this mode is not well understood.
- 2. It has been observed that the RBSB voltage of a Darlington transistor may vary significantly with the magnitude of foward base current. This behavior has not been observed for single BJT devices. It suggests that perhaps a new parameter, forward base current, should be included in the characterization of RBSOA of a Darlington transistor.
- 3. The turn-off speed-up diode plays an important role in the RBSB behavior of a Darlington transistor.

 Using the same base drive circuit, a transistor may exhibit different breakdown voltage levels, depending upon whether a seed-up diode is present.

If a diode is not present, the breakdown voltage varies with the value of R_2 , the resistor in parallel with the emitter and base terminals of the driver transistors.

- 4. RBSOA of a device is significantly altered by temperature. At high collector current level, RBSOA increases with temperature. An increase of 100 V (for 600V device) has been observed from 25°C to 100°C. On the other hand, at low collector current level, RBSOA may decreases or increases with temperature.
- 5. The second base drive may either increase or decrease the RBSOA or a device. At lower collector current levels, the RBSOA generally decreases as the second reverse drive is applied.
- 6. It has been observed that most manufacture specified RBSOA data tend to be conservative as compared to our measurement data. Nevertheless, there exist a few measurement data at low collector current levels well within the specified RBSCA.

5.0 DESIGN, EVALUATION AND TESTING OF INTEGRATED BASE DRIVE MODULES

Reducing the weight and volume of electronic systems in electric vehicle drives is of primary importance. One potential area for reductions is the base drive circuitry which must be included with each electronic power switch. Present methods employ hybridized or integrated circuit modules which are offered by many manufacturers of power electronic switches. These modules may offer better operational characteristics, more functions and certain levels of protection. Their offering varies from simple primitive switching amplifiers to more sophisticated base drive and monitoring systems.

This project will evaluate three different base drive modules or circuits of which two are hybridized and the third constructed around an integrated circuit. These are:

Mitsubishi M57215L

Fuji EXB-356

PERG Base Drive

<u>5.1</u> <u>TASKS</u>

The following are tasks involved with evaluating the base drive modules listed above.

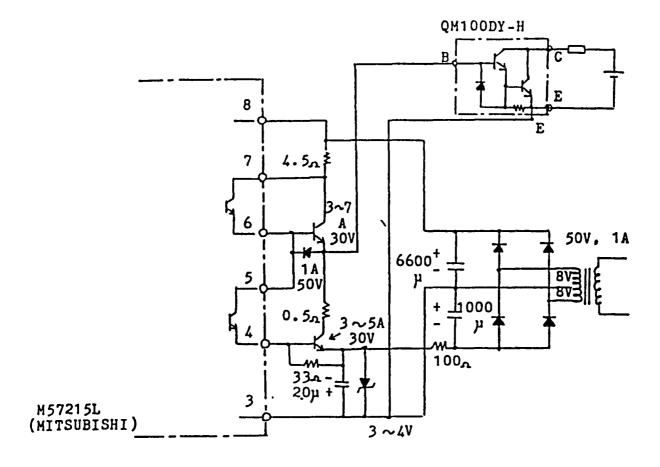
5.1.1 CONSTRUCTION

The Mitsubishi base drive is constructed similar to that in the application note shown in Fig. 5.1.1. This circuit uses the Mitsubishi hybrid module and associated components (for increased power output). The addition of the associated components causes some decoupling of any protection circuitry offered by the modules and increases the overall size. However, the electrical isolation, TTL compatibility, etc. are maintained.

The Fuji base drive circuitry is a replication of the application circuit shown in Fig. 5.1.2a and b. No circuit modifications have been made. However, the central hybrid base drive module from Fuji does require external transistors to increase its output power capability to drive the larger power switching devices proposed for testing in this program.

Two Fuji base drive circuits needed to be constructed. The first construction, Fuji Base Drive Board No. 1 (FBDB-1), developed a repetitive false triggering condition during operation. The source of false triggering was isolated to the photo coupler stage internal to the hybrid base drive module. After all external sources of possible conducted noise, etc. were eliminated or discounted the false triggering prevailed. A second Fuji Base Drive Board No. 2 (FBDB-2) was constructed with the same design rules as the first, such as, symmetry, minimum spacing, twisted leads, ground planes, etc. The second board, FBDB-2, was

2. BASE AMPLIFIER OUTPUT TYPE



3. NECESSARY DRIVE CONDITION OF QM100DY-H

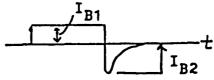


Fig. 5.1.1 Mitsubishi Base Drive Circuit

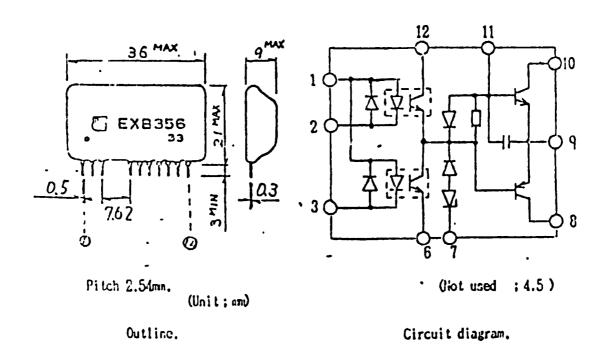


Fig. 5.1.2a.
Fuji Module Outline and Circuit Diagram

d) Application circuit.

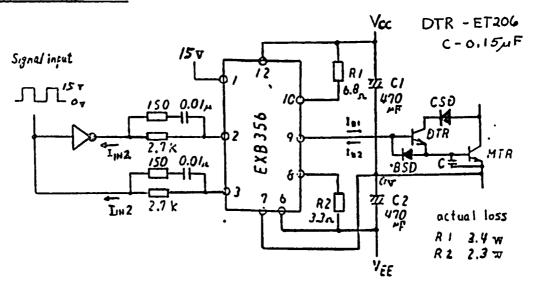


Fig. 5.1.2b.
Fuji Application Circuit

free of this false triggering regardless of the hybrid Fuji base drive module used. The present testing uses the FBDB-2 circuit.

The PERG base drive circuit is designed around the Thomson-CSF Components Corporation's UAA4002 - "Control Circuit for Fast Switching Transistor". This device was selected because of its many protective features as listed in Figure 5.1.3a and because of the internal current source and base current diversion circuitry which provides a closed loop adaptive base drive control scheme (shown in Figure 5.1.3b). The basic PERG base drive circuit is shown in Figure 5.1.3c. No monitoring options have been implemented in the development but will be at the developments conclusion.

All base drive circuits use dual power supplies, onboard filter capacitors and conform to medium frequency construction rules such as ground planes, minimum spacing, twisted pair wiring, etc.

5.1.2 STATIC TESTS

The Mitsubishi and Fuji base drive circuits require no feedback information from the power device. Therefore, these two-port systems can be statically tested using the base-to-emitter junctions of the actual power transistors (DUT, Device Under Test) which they will drive without having the DUT energized. The static tests consist of

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Integrated Circuits

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D. C. HOPKINS

UAA4002

ADVANCE INFORMATION

CONTROL CIRCUIT FOR FAST SWITCHING TRANSISTOR

- Direct drive of the switching transistor
- Self regulated positive base current (max 0 5 A)
- Negative base current ensuring fast turn-off (max 3 A)
- The output current can be increased by means of one (or more) external transistor.
- Minimum conducting time (or no conduction) to allow the discharge of a RDC network
- Protection against a saturation failure of the power transistor during a conducting period, with an ajustable detection threshold.
- Immediate limitation of the collector current
- Watching of the positive supply of the chip (VCC).
- Watching of the negative supply with adjustable threshold
- On-chip thermal protection
- Programmable maximum ON time
- TTL and CMOS compatible.
- Can be drived with alternate pulses
- Adjustable delay between the rising edge of the input signal and the beginning of the positive base drive.

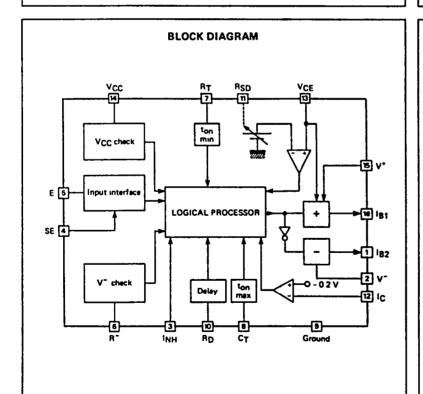
CONTROL CIRCUIT FOR FAST SWITCHING TRANSISTOR

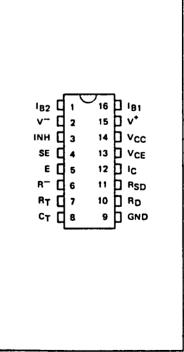
CASE CB-79



DP SUFFIX
PLASTIC PACKAGE

PIN ASSIGNMENT





SP8201A 1/8

THOMSON-CSF Components Corp. Semiconductor Division
P O Box 1454 - 6660 Variel Avenue
CANOGA PARK, CA 91303
Tel (213) 887 10 10 Telex 698481

Fig. 5.1.3a.

ion-csf ಬ್ರಾಗಿಡ್ಡಿಕ

OUTPUT STAGE "ON STATE"

ON state

The positive stage achieves a very efficient drive of the switching transistor. Its features are essentially

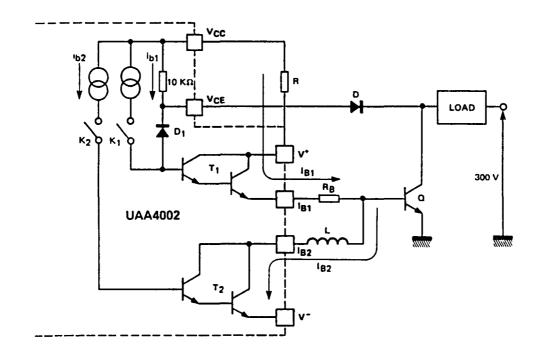
- Direct drive (no transformer)
- The transistor stays in a quasi saturation mode, and thus has a reduced storage time.
- The drive energy is strictly limited to what is necessary.
- Easy implementation

K₁ is closed to turn the positive stage on

The maxim im value of the positive base current is settled by the limitation resistor R (Ig₁ < 0.5 A)

A regulation loop is used to keep Q in a quasi saturation mode—the more Q gets saturated,—the more diode D will shunt an important part of the drive current 161, through diode D₁

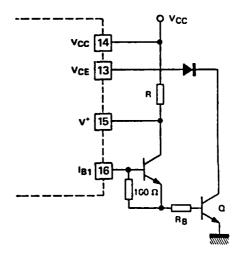
Rg is a low resistor (about 1 Ω) which helps to stabilize the regulation loop



Voltage VCE across transistor Q is .

If the required drive current is greater than 0.5 A, one external NPN transistor may be added

In this case



6/8

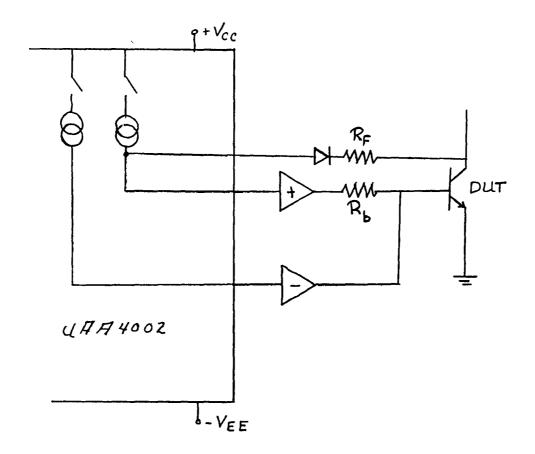


Fig. 5.1.3c. PERG Base Drive

measuring the current levels for sourcing current to the base of the DUT, sink current levels for extracting charge from the base of the DUT, rise time, fall time, and propagation delays for these base drive circuits. These tests are performed at room temperature and at increased temperatures.

Because the PERG circuitry requires active feedback for development the static and active test is incorporated along with the circuit development.

5.1.3 ACTIVE TESTING

Although the static testing provides much information about the base drive circuit's own characteristics, the operation of the main power switching transistor (DUT) when driven by this base drive module is paramount. Therefore, the performance of the base drive circuitry will be evaluated in light of the performance of the power switch.

Variations in base drive performance between the static testing and active testing should be minor with most contributions from the parasitic feedback capacitances (such as Miller capacitance during the active versus non-active operation).

5.1.4 DATA SHEET COMPARISONS

Manufacturer's data sheets provide specific data for specific operating points of their products. Conversely, designers are interested in the information across a wide operating region. From the user's point of view, this necessitates the testing as described in the above two sections.

In the Test Results section, the manufacturers data is compared with the measured data.

5.2 TEST EQUIPMENT

5.2.1 STATIC TESTS

Basic electronic equipment was used for the static testing as reported in this interim report. The equipment included an oscilloscope, power supplies, signal generators, etc. The equipment used for the active testing is described in section 3.2, Characterization of High Power BJT.

5.3 TEST METHOD

Because the base drive circuits are constructed primarily around a base drive module or integrated circuit, little can be done by the designer to change the circuit's characteristics. Therefore, tests of the base drive

circuits will only be terminal characterizations.

5.3.1 STATIC TESTING

The test circuit of Fig. 5.3 is used to test the Mitsubishi and Fuji base drive circuits. The base drive circuit is operated at the manufacturer's required supply voltages and within the manufacturer's suggested limits. The base-to-emitter junction of a DUT is used as a load for the base drive circuit. Under this load condition, the switching wave forms of the base-to-emitter voltage and base-to-emitter current are recorded. Of particular importance is the rise and fall times (t_{br}, t_{bf}) of the current and the magnitude of the forward and reverse base currents (I_{b1}, I_{b2}). Current levels are checked for adequacy and the integrity of the output wave form from the base drive circuit is observed for any abrupt changes in in which may cause the DUT to operate outside the safe operating area (such as momentary inadequate drive of the DUT during assumed forward conduction or severe oscillations in base current during turn-off). Finally, the propagation delay between the rise of the input signal and subsequent output activation of the base current to the DUT is documented.

High temperature effects at approximately 100°C are also qualitatively recorded.

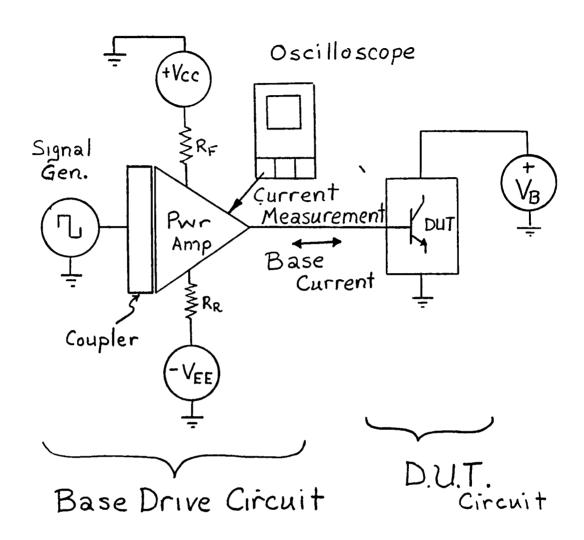


Fig. 5.3.
Test Circuit

5.3.2 ACTIVE TESTS

Active testing of the devices will be used as the primary basis of comparison. Therefore, the critical operating characteristics as outlined below will be acquired and the needed parameters extracted.

Since reliable comparative data are needed the maximum operating current ratings of the DUTs at 100 to 150 A have To test at higher current levels would been selected. require a change in the output current amplification stage of the base drive circuits. This amplification stage somewhat isolates the load (DUT) from the base drive modules. Hence, such testing at higher currents (i.e. 400 A) would then make the tests and comparison of the base drive circuits more dependent on the electromagnetic environment, topological construction and designer experience, all of which can have considerable variation. Only after the base drive comparison and selection is made can the effect of these generic variables be quantified and possibly minimized.

The Active Tests' test plan is: Three BJT devices will be used for DUTs:

Mitsubishi QM150DY-H

Fuji EVM 31-050

Westinghouse KD 324510-10

The DUTs will be operated at 50% and 100% of maximum collector current and applied $\rm V_{CF}$ of approximately 200V.

Under these conditions the DUT's collector current characteristics for rise time, $t_{\rm r}$; fall time, $t_{\rm f}$; and storage time, $t_{\rm s}$ will be recorded. The DUT's base current characteristics (base drive circuits output) for magnitude and transition time will be recorded. Also, the phase difference (propagation delay) between the input current signal (or voltage signal) and the DUT's base current and collector current will be recorded for both turn-on and turn-off. For this low voltage test the DUT's base-to-emitter voltage will be recorded for completeness but only at 100% collector current.

Base drive circut tests include operating the DUTs at high voltage where base current, base-to-emitter voltage and collector current transition characteristics will be recorded at the highest collector current available. Of particular importance is the measurement of the input voltage and/or current signals to the base drive modules. At higher voltages the interelectrode capacitance could have an appreciable effect.

5.4 TEST RESULTS

This section contains the resulting test data from the Static and Active Tests. Upon this data the "Evaluation of Test Results" in section 5.6 is concluded.

5.4.1 STATIC TESTING

5.4.1.1 MITSUBISHI BASE DRIVE MODULE (M57215L)

The base drive module circuits were connected as previously outlined and the Mitsubishi transistor, QM300-HA-H was connected as the static load. The tests were conducted and results are shown in Table 5.1, Static Tests of Mitsubishi Base Drive Circuit. The recorded measurements are well within keeping of the published data by the manufacturer. All these tests were run at room temperature. Higher temperatures were introduced to observe the change in propagation delay. At approximately 100°C the propagation delay between the input signal and the output excursion at the base of the device under test was less than the manufacturer's guaranteed rating, as desired.

The wave forms of the base current delivered to the DUT are shown in Figures 5.4.1a and 5.4.1b. In Figure 5.4.1a, the current flowing into the DUT reached its steady state value of 5.6 A in less than 1 microsecond. The reverse current applied to turn the DUT off reached the peak value of 2 A in less than 0.5 microseconds and delivered this current for approximately 6.5 microseconds.

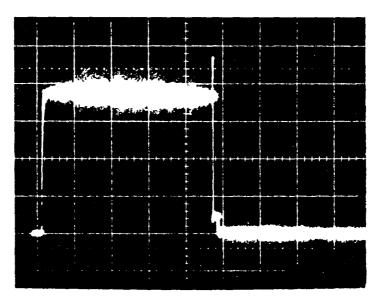
The Figures 5.4.1a and 5.4.1b are the voltages across the series resistors $R_{\rm F}$ and $R_{\rm R}$, respectively. Small excursions such as the turn-off peak current shown in Fig. 5.4.1a during the negative transition is an internal current

Table 5.1

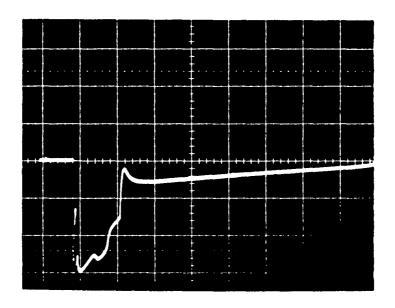
Static Tests of Mitsubishi Base

Drive Circuit

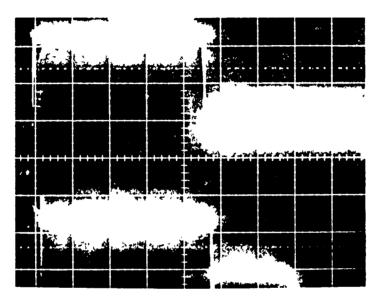
	Forward Base Current of DUT	Reverse Base Current of DUT
I peak	3.6 A	2.10 A
I Steady State	3.6 A	0.42 A
Rise Time (t _r)	0.84 µs	<0.5 µs
Fall Time (t _f)	0.3 µs	3.5 µs
Pulse Width		6.5 µs
Propagation Delay	4.4 μs	4.4 µs



Forward Base Current of DUT vert. 1 A/div horiz. 20 µs/div. Fig. 5.4.1a.



Reverse Base Current of DUT Vert. 0.71 A/div. Horiz 5 µs/div Fig. 5.4.1b.



Propagation delay vert. 2 V/div. Input Signal 1 V/div. V of DUT 20 µs/div. Fig. 5.4.1c.

passed between the source and sink transistors of the base drive circuit as indicated in Fig. 5.5.

Figure 5.4.1c shows the input voltage waveform across the optal coupler and the voltage across the base to emitter of the DUT. These two synchronized waves display the propagation delay at room temperature between the input signal and the final activation of the DUT. Through a repetition of these tests, the measurements did not change and their expected wave shapes were in keeping with the published manufacturers information.

5.4.1.2 FUJI (EXB-356)

The given application circuit shown in Fig. 5.1.2b requires a base-to-emitter capacitor externally connected to the DUT. From preliminary test measurements this capacitor provides a deceptive base drive circuit switching performance. Further investigation into the capacitors usefulness has been undertaken. From a qualitative assessment of the base drive circuit operation with the suggested 0.15 F, it is easily seen that the added capacitance retards the turn-off of the DUT. (This investigative test used an activated DUT.) Rather than discount this capacitance completely, a lower value, C = 0.015 F is used to partly maintain any effects known to the manufacturer and that have escaped this author.

As noted in section 5.1.1, two Fuji Base Drive Boards

(FBDB-1 & 2) had to be constructed due to the described false triggering problem (see section 5.1.1). The second construction, FBDB-2, displayed no problem from false triggering. Therefore, the Fuji tests are conducted using this second board.

The test results are summarized in table 5.2 consistent with the manufacturer's data. Since the output current amplification stage of the base drive circuit is simply an open collector transistor no meaningful measurement of forward base current can be made unless the DUT is connected and energized as shown in Figure 5 1.2b. For these tests the DUT was energized with 5 V and a maximum of 8 A collector current.

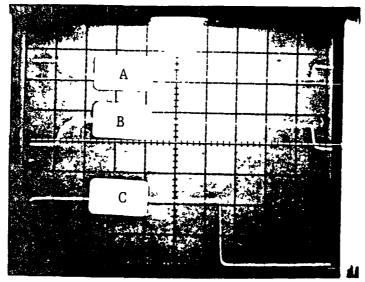
Shown in Figures 5 4.2a and b are the Fuji base drive circuit test results. The base characteristics of the DUT in Figures 5.4.2a shows in the center trace the drive current available from the base drive circuit. Forward drive, I_b , is delivered from a Darlington connected transistor (Fuji ET206 connected between collector and base of the DUT) and not directly from the base drive circuit. There is a Schottky diode connected in series with the collector of the ET206. At low DUT collector currents when the DUT gain is high the Schottky diode prevents Darlington action by the ET206. Current delivered from the base drive circuit passes through the base-to-emitter junction of the ET206 and directly drives the DUT allowing for a $V_{\text{CE}(\text{sat})}$ to be achieved. At higher load (DUT) currents the ET206

Table 5.2

Static Tests of Fuji Base Drive Circuit

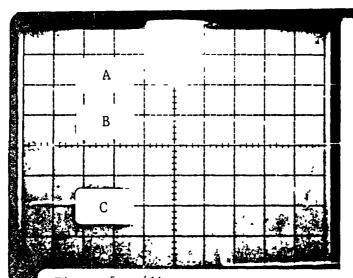
	Forward Base Current of DUT	Reverse Base Current of DUT			
I peak	(note 1)	2 A			
I Steady State	(note 1)	0.05 A			
Rise Time (t _r)	1.0 μs	l.l µs			
dI _{b2} /dt		2.1 A/2 μs			
Pulse Width		7.5 µs			
Propogation Delay	√ 6 µs	7 μs			

Note 1: The current amplification stage at the base drive output forms the Darlington drive configuration. The forward $\bf I_b$ is dependent on the $\bf V_{cb}$ of the DUT.



Time 5 μ s/div V_{be} : 5 V/div (A) I_{b} : 1 A/div (B) I_{in} : 5 ma/div (C)

(Base Drive Module)
Fig. 5.4.2a. Base Characteristics of DUT



Time: 5 μs/div V_{ce}: 5 V/div (A) I_c: 10 A/div (B) I_{in}: 5 mA/div (C)

Fig. 5.4.2b. Collector Characteristics of DUT

provides more of the drive current as the collector-to-base voltage, $V_{\rm cb}$, of the DUT increases. There is no variation in the base-to-emitter current of the ET-206. This circuit configuration does not provide a meaningful measurement of the forward DUT base current during static testing.

Since the reverse (turn-off) base drive to the DUT is supplied directly from the base drive circuitry bypassing the ET206 through a diode, the negative going waveshape of the center trace in Figure 5.4.2a accurately depicts the reverse base drive current to the DUT. The high rate-of-change of reverse curent ($\mathrm{dI}_{\mathrm{b2}}/\mathrm{d_{t}}$) and the effect of the base-to-emitter capacitor are seen in the initial negative transition of the current. Upon further increases in DUT operating voltage (and current) the "notching" decreased. This effect will be of particular interest during active testing.

From Figures 5.4.2a and b, the propagation delay between the input signal to the base drive module and outputs of the base drive circuit and DUT can be seen. These were well within specifications. However, the Fuji modules were observed to operate at significantly elevated temperatures. This also, precluded any high temperature tests.

5.4.1.3 PERG BASE DRIVE

The PERG circuit incorporates a single chip control

circuit for sensing, active feedback control and monitoring:

Supply voltage

On chip temperature

Minimum and maximum on time of DUT

Saturation voltage

Emitter current

Additional curcuitry enables the base drive circuit to provide proportional base current to the DUT along with sufficient reverse base current and holding current. The circuitry is TTL and CMOS compatible.

Since the base drive provides proportional base current dependent on the DUT's collector-base voltage, static testing cannot be performed. Refer to the "Active Testing" results for comparative data.

5.4.2 ACTIVE TESTING

The following information is critical for comparisons of base drives. We compare the characteristics of the DUTs during switching rather than the actual base drives characteristics since the end result is what is required.

Listed in table 5.3 is the summary data of the Active Testing. The table is divided into three columns according to the base drive module or base drive circuit used. The horizontal divisions list the different switching times for the on and off transitions of current flowing through the

Table 5.3
Summary Data of Active Testing

	;	Mitsubishi Base Drive			Fuji Base Drive		PERG Base Drive			
		<u> </u>	EVM31-050	KD324510	QM150DY-H	EVN31-050	KD324510	QM15CDY-H	EVM31-050	KD324510
Turn-on	t _r	0.17	0.14	0.12	2.0	1.3	0.54	0.8	1.03	1.0
0.5 I (μs)	t _{d1}	3.1	2.9	3.1	11	12	12	3.8	4.2	3.2
Turn-on	t r	0.30	0.34	0.24	2.2	1.9	0.73	1.35	2.3	1.6
I cmax (μs)	t _{dl}	3.0	2.9	3.0	11	12	12	5	3.2	3.2
Turn-off	^t f	1.4	0.99	1.3	0.64	0.52	0.59	0.21	1.0	0.25
0.5 Ι _{cmax} (μs)	ts	20	13	19	14	13	14	1.9	1.4	1.7
136	t _{d2}	33	20	30	22	21	22	3.3	2.8	2.4
Turn-off	t	1.1	1.0	1.2	0.75	0.91	0.73	1.3	2.5	.79
I (μs) cmax	t _s	11	5.8	11	11	10	11	2.0	2.2	1.39
	t _{d2}	18	11	19	19	20	19	3.3	3.6	2.7
I _{cmax} (A)		150	150	100	150	150	100	150	150	100
DUT Mfgr.		Mıtsu.	Fuji	West.	Mitsu.	Fuji	West.	Mitsu.	Fuji	West.
Figures		3.4.3	3.4.4	3.4.5	3.4.6	3.4.7	3.4.8	3.4.9	3.4.10	3.4.11

DUTs. The data is taken at half load (one half of the maximum collector current allowed) and at full load. At the very bottom of the chart is listed the maximum current for each device and the manufacturer of the device.

The terms listed within the table and the critical information on the following oscillograms are defined below. A graphical description of these terms is also found in Figure 1.4.

t_r: rise time of the collector current of the DUT

 t_{D1} : delay time between the initiation of input to the base drive and the rise time of the collector current

 t_f : fall time of the collector current of the DUT

 t_s : storage time of the DUT during turn-off t_{D2} : Delay time between the initiation of the signal to the base drive and the final fall of the current in the DUT.

There are two test circuits used in this evaluation. If the DUT is driven by the Mitsubishi or Fuji base drives, then the circuit in Figure 1.2 is used with a source voltage of approximately 200 V. If the DUTs were driven by the PERG base drive then the circuit in Figure 5.1.3c was used with a source voltage of approximately 100 V.

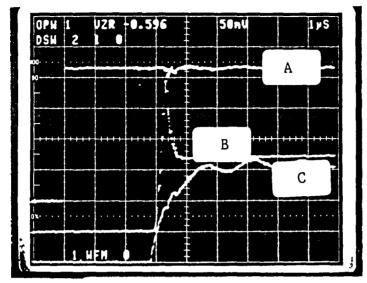
5.4.2.1 Mitsubishi Base Drive Module (M57215L)

The information in Table 5.3 is extracted from oscillograms shown in the following figures. The information regarding switching times for the Mitsubishi

base drive driving the Mitsubishi transistor is shown in the sequence of Figures 5.4.3a-e. As shown in Fig. 5.4.3a, this base drive provides a 5A peak turn-on base current to the DUT. It then settles out to an increasing 2.5-5.0 A constant current. The propagation delay measured between the initiation of the signal to the base drive and the final rise time of current at the collector is approximately 5.1 microseconds. In Fig. b, the reverse current exceeds 2 A for turn-off and is sustained at a reverse bias voltage of 7 V which provides aporiximately .5 A of continual reverse base current after the initial peak. Since these DUTs are Darlingtons, the reverse current will reach zero before the collector current begins to fall since the main clearing current provided by the base drive is to turn off the saturated drive transistor within the Darlington. DUT is operating at full load, a larger amount of clearing charge required from base drive. However, the base drive uses a fixed capacitance for charged storage. Therefore, the time interval for reverse current from the base drive is shortened when turning off the device under full load conditions. At full load, a peak current for turn-on is reached at approximately 4.5 A and settles out to a full 3 A maintaining current. There is some oscillation in the collector current due to the inductance within the load circuitry.

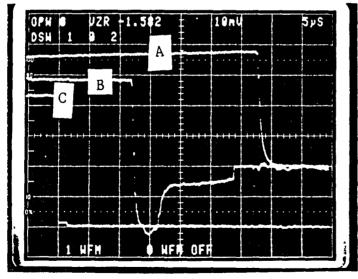
Shown in Figure 5.4.3e is the output characteristics of the base drive circuitry. Shown is the voltage of the base-

DUT OM150DY-H

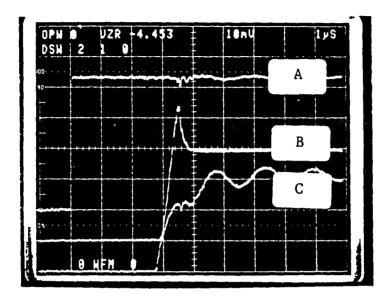


Turn-on @ 75A
Input = 1 V/div (A)
I_b = 1 A/div (B)
I_c = 20 A/div (C)
Time = 1µs
Fig. 5.4.3a.

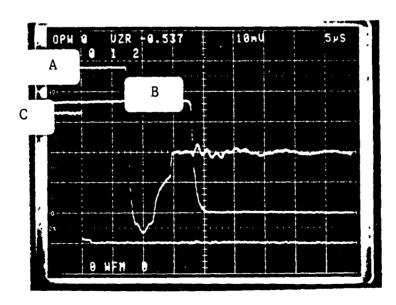
F



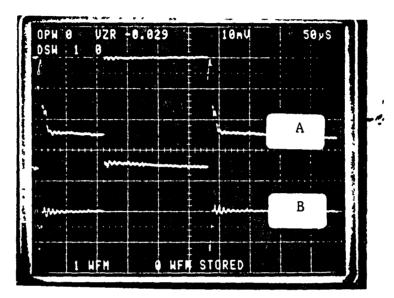
Turn-off @ 75 A $I_c = 20 \text{ A/div (A)}$ $I_b = 1 \text{ A/div (B)}$ Input = 1 V/div (C) $Time = 5\mu s$ Figure 5.4.3b.



Turn-on @ 150 A
Input = 1 V/div (A)
I_b = 1 A/div (B)
I_c = 40 A/div (C)
Time = 1µs
Fig. 5.4.3c.



Turn-off @ 150A I_b = 1 A/div (A) I_c = 40 A/div (B) Input = 1 V/div (C) Time = 5µs Fig. 5.4.3d. DUT: QM150DY-H



DUT Base Characteristic at 150 A

$$V_{be} = 1 \text{ V/div}$$
 (A)

$$I_b = 2 A/div$$
 (B)

Time = $50\mu s$

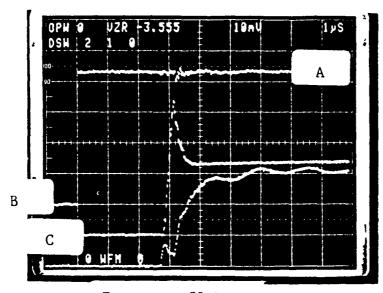
Figure 5.4.3e

to-emitter (output of the base drive of the DUT). Revealed is the constantly applied reverse voltage (approximately 7 V) to the DUT. The source of this voltage should be of high impedance since the transistor could be operated in a reverse conducting mode with an exceptionally low gain. This occurs quite often in full-bridge circuitry.

In Figures 5.4.4a-e show the switching results for the Mitsubishi base drive driving the Fuji DUT. Shown in Figure is the half-load characteristics. Again Mitsubishi base drive offers a peak current pulse during turn-on which is very advantageous. At turn-off the reverse pulse again exceeds 2 A. The Fuji device responds with a slowly rising turn-on and a slowly falling turn-off. seen in Figure 5.4.4c, at full load the turn-on pulse is quite small and unfortunately, inadequate for the turn-on of the Full transistor. At the rising current edge, the driver transistor starts to turn-on, however, the total Darlington gain is too low and the major transistor does not have sufficient charge to begin its turn-on process. In Figure 5.4.4d, the turn-off characteristic is very suitable. With the reverse current in excess of 3 A, the Fuji DUT turns off quickly, as indicated in Table 3 with a 1.0 microsecond fall time.

As shown in Figure 5.4.4e, there is some inductance within the leads of the base drive circuit going to the DUT. This is evident by the overshoot voltage on the top trace during turn-on. During turn-off the inductance has

DUT: EVM31-050



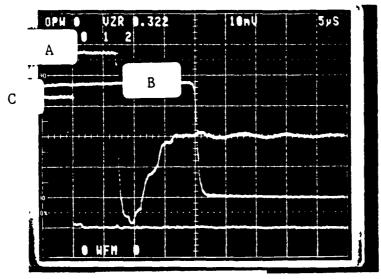
Turn-on at 75 A Input = 1 V/div (A)

 $I_b = 1 \text{ A/div} \qquad (B)$

 $I_c = 20 \text{ A/div}$ (C)

Time = lµs

Figure 5.4.4a



Turn-off at 75 A

 $I_b = 1 \text{ A/div (A)}$

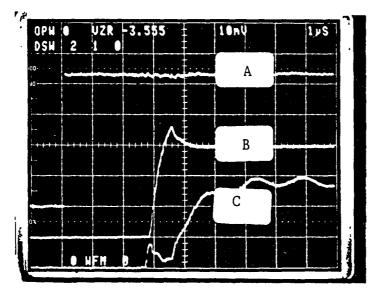
 $I_c = 20 \text{ A/div (B)}$

Input = 1 V/div (C)

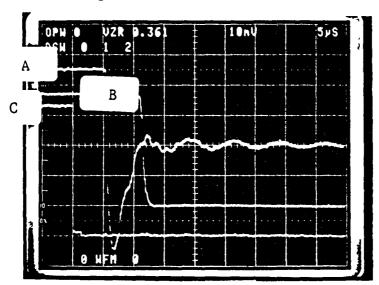
Time = $5\mu s$

Figure 5.4.4b

TUT EVM 31-050



Turn-on at 150A Input = 1 V/div (A) I_b = 1 A/div (B) I_c = 40 A/div (C) Time = 1µs Figure 5.4.4c



Turn-off at 150 A

I_b = 1 A/div (A)

I_c = 40 A/div (B)

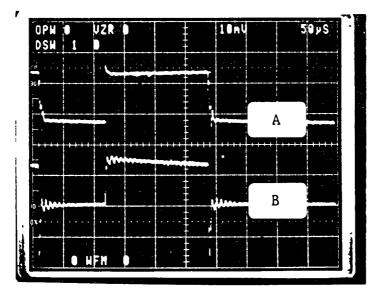
Input = 1 V/div (C)

Time = 5µs

Figure 5.4.4d

Mitsubishi Base Drive

DUT: EVM 31-050



DUT Base Characteristics at 150 A $V_{be} = 2 V/div (A)$

 $I_b = 2 \text{ A/div (B)}$

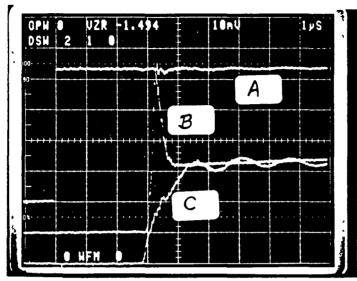
Time = $50 \mu s$ Figure 5.4.4e minimized effect and the current source characteristic of the drive provides the high reverse current.

Shown in Figure 5.4.5a is the turn-on characteristics of the Westnghouse DUT driven by the Mitsubishi base drive. The overshoot current from the base drive is significant and helps the Westinghouse DUT turn on abruptly. The reverse current shown in Figure b is similar to the Mitsubishi base drive circuit driving its own Mitsubishi device (Figure turn-off the same characteristics 5.4.3b). Αt observations can be made as in the previous Figures 5.4.5. Again Figure 5.4.5e shows the same characteristics as in the earlier Figure 5.4.3e and the same conclusions can be made. It should be noted that the Mitsubishi company packages the Westinghouse device in Japan for Westinghouse. interesting to note that the Westinghouse and Mitsubishi DUTs have many identical characteristics. As will be seen later, the Westinghouse DUT appears to have better switching characteristics than the Mitsubishi device from all three base drive circuits.

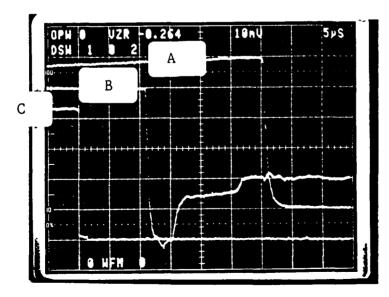
5.4.2.2 FUJI BASE DRIVE MODULE (EXB-356)

The following three sets of oscillograms are the result of the Fuji base drive circuit driving the three devices under test. Shown in Figure 5.4.6a is the turn-on characteristic for the Fuji base drive driving the Mitsubishi power Darlington transistor (DUT). Shown is a

CLT KD324510



Turn-on at 50 A
Input = 1 V/div (A)
I_b = 1 A/div (B)
I_c = 10 A/div (C)
Time = 1µs
Figure 5.4.5a



Turn-off at 50 A

I_c = 10 A/div (A)

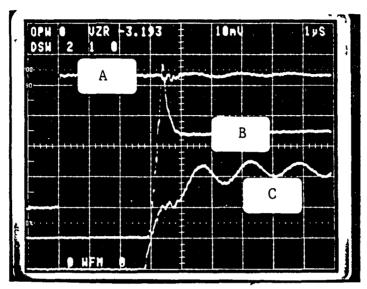
I_b = 1 A/div (B)

Input = 1 V/div (C)

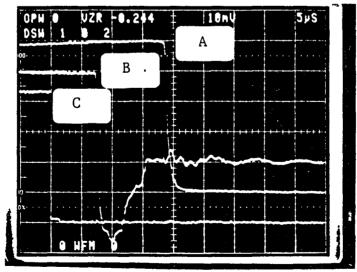
Time = 5µs

Figure 5.4.5b.

KD 324510



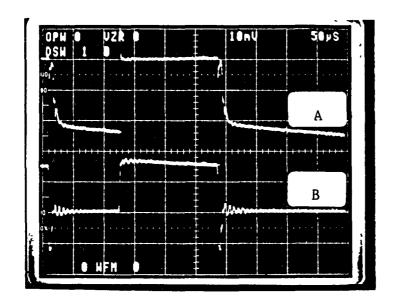
Turn-on at 100 A
Input = 1 V/div (A)
I_b = 1 A/div (B)
I_c = 20 A/div (C)
Time = 1µs
Figure 5.4.5c



Turn-off at 100 A $I_c = 20 \text{ A/div (A)}$ $I_b = 1 \text{ A/div (B)}$ Input = 1 V/div (C) Time = 5µs Figure 5.4.5d

Mitsubishi Base Drive

DUT: KD324510



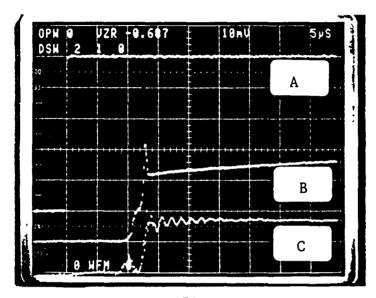
DUT base characteristic at 100A $V_{be} = 1 \text{ V/div (A)}$

 $I_b = 2 \text{ A/div (B)}$

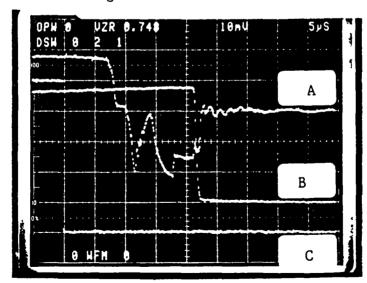
Time = $50\mu s$

Figure 5.4.5e

slight peak current overshoot from the base drive which helps to rapidly turn the device on. The rise time for the collector current is measured at 2 microseconds with a propagation delay (between the initiation of a signal to the base drive and final rise collector current in the DUT) of approximately 11 microseconds. During turn-off there is a peak reverse current that has an unusual characteristic. Reverse current reaches a peak value of approximately one amp, then reduces to zero current in approximately 4 microseconds and then will peak again for an interval of approximatly 7 microseconds to clear the transistor. should be noted in the Fuji base drive configuration that a third transistor is used as a driver forming a triple darlington configuration. Unlike the typical turn-off of a Darlington transistor, the reverse base current continues after the clearing of the main power transistor. Further investigation of this is given in the following section evaluating the test results. At full load, shown in Figure 5.4.6c, the overshoot current again helps to turn on the transistor. During turn-off, the characteristic of reverse current notching exceeds the zero level (positive I_h) followed by a reverse current pulse in the reverse direction for approximately 6 microseconds. Again this will be investigated in the following section. Figure 5.4.6e shows the combined base characteristics of base to emitter voltage and base current (output from the base driver).



Turn-on at 75 A Input = 2 V/div (A) I_b = 0.5 A/div (B) I_c = 20 A/div (C) Time 5 μ s Figure 5.4.6a



Turn-off at 75 A

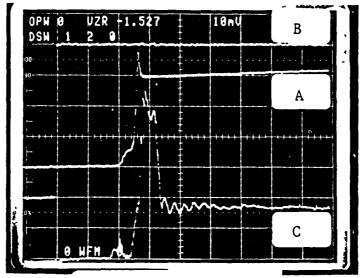
I_b = 0.5 A/div (A)

Input = 2 V/div (B)

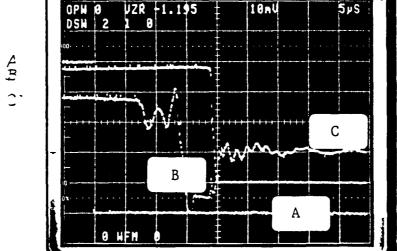
I_c = 20 A/div (C)

Time = 5µs

Figure 5.4.6b



Turn-on at 150 A $I_b = 0.5 \text{ A/div (A)}$ Input = 2 V/div (B) $I_c = 40 \text{ A/div (C)}$ Time = $5\mu s$ Figure 5.4.6c



Turn-off at 150 A Input = 2 V/div (A)

 $I_c = 40 \text{ A/div}$ (B)

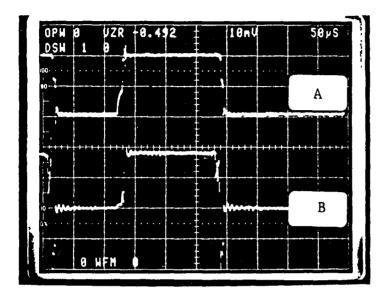
 $I_b = 0.5 \text{ A/div (C)}$

Time = $5\mu s$

Figure 5.4.6d

Fuji Base Drive

DITT: QM 150DY-H



DUT Base Characteristics at 150 A $V_{be} = 2 \text{ V/div (A)}$

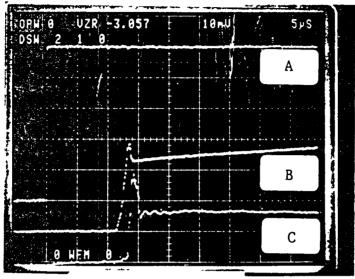
 $I_b = 0.5 \text{ A/div (B)}$

Time = 50µs Figure 5.4.6e

The Figure set 5.4.7 shows oscillograms resulting from the Fuji base drive circuit driving a Fuji transistor (this combination is recommended in the application literature). As seen in Figure 5.4.7a, there is, due to a test set-up malfunction, a significant overshoot in the collector current. However, the base current does provide adequate drive for the transistor. In the turn-off shown in Figure b the same characteristic as previously noted appears. turn-off drive current in the base continues collector current drops. Again, this will be explained in the following section. Shown in Figure 5.4.7c is the turnon of the DUT under full load (150 A). Again, there is sufficient drive from the base drive to provide a high rate of rise of current in the DUT. The reverse turn-off shown in Figure 5.4.7d does not display the severe notching in the turn-off base current as seen previously. The slope of the base turn-off current going from forward to reverse rather slow with a peak turn-off current of 1.25 Considerable oscillations show up on the reverse turn-off which is attributed to a large lead inductance. To further show the base drive characteristic, Figure 5.4.7e shows the base to emitter voltage and base current (output from the base drive circuit) at the input (base) of the DUT. As can be seen, a large overshoot current in the base is available.

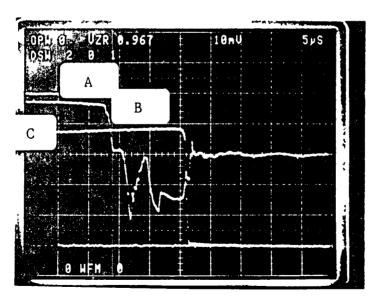
The following set of oscillograms shows the response of the Westinghouse transistor to the Fuji base drive circuit. Fuji Base Drive

DUT: EVM 31-050

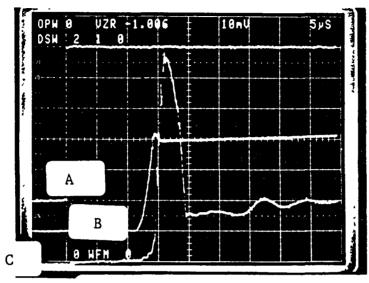


Turn-on at 75 A
Input = 2 V/div (A)
I_c = 40 A/div (B)
I_b = 0.5 A/div (C)
Time = 5µs

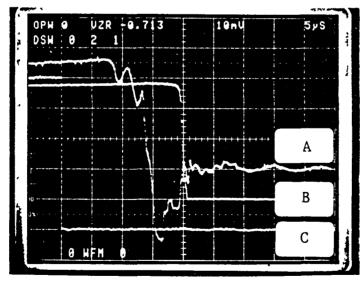
Time = 5μ s Figure 5.4.7a



Turn-off at 75 A Input = 2 V/div (A) $I_b = 0.5 \text{ A/div (B)}$ $I_c = 20 \text{ A/div (C)}$ Time = 5 μ s Figure 5.4.7b DUT: E /M31-050



Turn-on at 150 A Input = 2 V/div (A) $I_b = 0.5$ A/div (B) $I_c = 20$ A/div (C) Time = $5\mu s$ Figure 5.4.7c

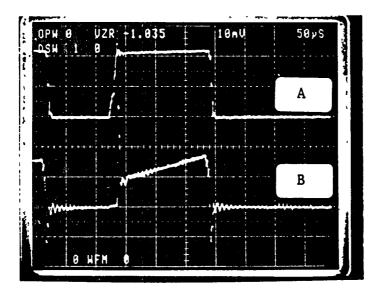


Turn-off at 150 A $I_b = 0.5 \text{ A/div (A)}$ Input - 2 V/div (B) $I_c = 40 \text{ A/div (C)}$ Time = 5µs

Figure 5.4.7d

Fujı Base Drive

DUT: EVM 31-050



DUT Base Characteristics at 150 A V_{be} = 2 V/div (A)

 $I_b = 1 \text{ A/div (B)}$

Time = $50\mu s$ Figure 5.4.7e

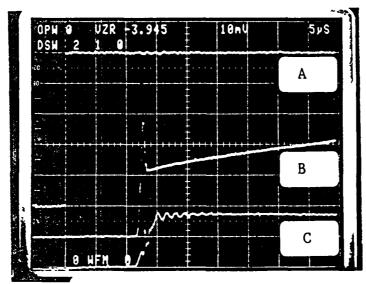
Figure 5.4.8a the overshoot current turns In the Westinghouse device on abruptly. The current then builds slowly to the full current provided by the base drive. The reverse base drive current is similar to that shown in the oscillograms 5.4.6a&b depicting the Mitsubishi response from being driven by the Fuji base drive module. Shown in Figure 5.4.8c is the turn-on of the Westinghouse transistor at full load. The overshoot base drive current from the Fuji drive circuit does assist in the turn-on of the Westinghouse device. An unusual response is shown at turn-off, Figure 5.4.8d. The reverse base current begins to reach a peak value of 1 A, then, reverses direction providing almost a 1 A forward drive into the DUT for a short 2 microseconds. It then reverses direction again to provide the reverse current flow required to clear charge in the DUT. This activity occurred with a collector current of Figure 5.4.8f In shows more acceptable characteristics when the collector current is only 95 A. It appears the small threshold of 5 A aggravates this turn-off characteristic in the base drive circuitry.

5.4.2.3 PERG BASE DRIVE

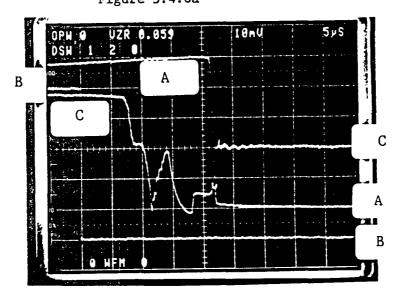
The following set of oscillograms use a different circuit for evaluating the base drive performance with the DUTs. Shown in Figure 5.4.9a is the turn-on and turn-off characteristics of the PERG base drive and the Mitsubishi

Fuji Base Drive

DLT: DK324510



Turn-on at 50 A
Input = 2 V/div (A)
I_c = 10 A/div (B)
I_b = 0.5 A/div (C)
Time - 5µs
Figure 5.4.8a



Turn-off at 50 A

I c = 10 A/div (A)

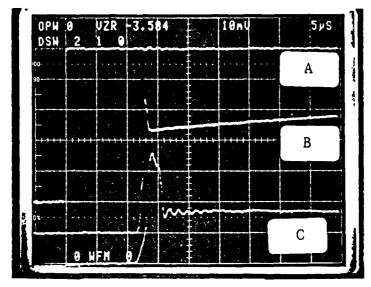
Input = 2 V/div (B)

I b = 0.5 A/div (C)

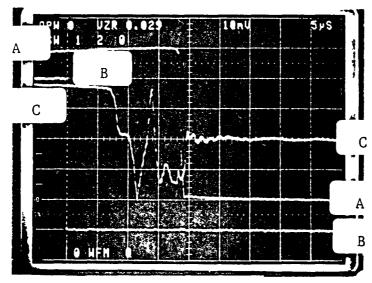
Time = 5µs

Figure 5.4.8b

K2 324510



Turn-on at 100 A
Input = 2 V/div (A)
I c = 20 A/div (B)
I b = 0.5 A/div (C)
Time = 5µs
Figure 5.4.8c



Turn-off at 100 A

I_C = 20 A/div (A)

Input = 0.5 A/div (B)

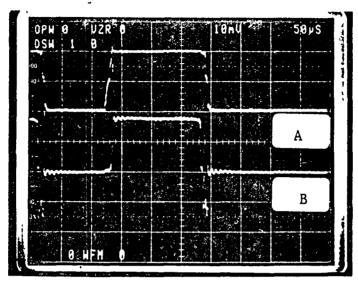
I_b = 2 V/div (C)

Time = 5µs

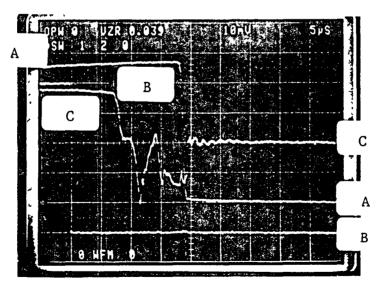
Figure 5.4.8d

Ti. Dase Drive

₽U7. DK324510



DUT Base Characteristics at 100 A V_{be} = 2 V/div (A) I_{b} = 0.5 A/div (B) Time = 50 μ s Figure 5.4.8e

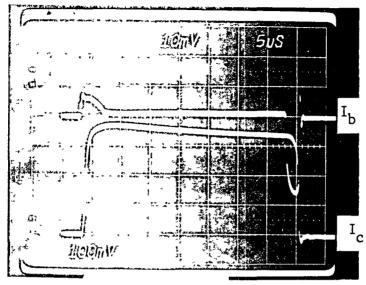


Turn-off at 95 A $I_c = 20 \text{ A/div (A)}$ Input = 2 V/div (B) $I_b = 0.5 \text{ A/div (C)}$ Time = 5 µs Figure 5.4.8f

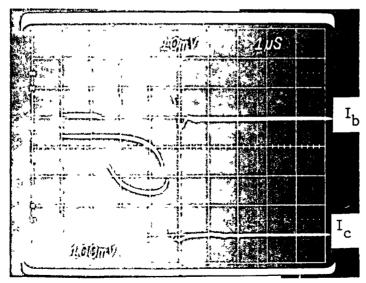
Remember that this drive circuit uses DUT. feedback information from the collector to base voltage of the DUT providing proportional base drive. At turn-on there is a minimum on time for the base drive circuitry which also provides a maximum input current to the DUT. approximately 1.75 A. After initial turn-on the base current is adjusted accordingly to maintain the appropriate operating conditions for the DUT. At turn-off there is no feedback mechanism incorporated and a maximum reverse current is applied, shown in Figure 5.4.9b. In this oscillogram we see a very strong turn-off current approximately 10 A into the DUT. The DUT accordingly. At full load the turn-on characteristic, shown in Figure 5.4.9c again provides a minimum turn-on current of approximately 3 A and the DUT has an abrupt turn-on. turn-off under full load the same current characteristic as previously is provided to the DUT. In these oscillograms, the collector current of the DUT and the base drive are all well behaved. In Figure 5.4.9e is a composite photo showing the base drive voltage and current (input to the DUT). From these oscillograms come the results that are entered into Table 5.5.

The following set of oscillograms show the response of the Fuji DUT to the PERG base drive. In Figure 5.4.10a the turn-on response of the DUT at half load is indicated. The collector current of the DUT briefly rises abruptly, then there is a slow transition to full current. This may be due

QM150DY-н



Turn-on at 75 A $I_b = 2 \text{ A/div}$ $I_c = 20 \text{ A/div}$ Time = 5 μ s Figure 5.4.9a



Turn-off at 75 A

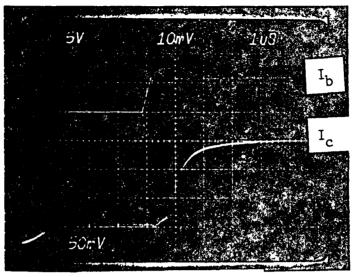
I_b = 5 A/div

I_c = 20 A/div

Time = 1µs
Figure 5.4.9b

PERG Base Drive

DUT: QM150DY-H

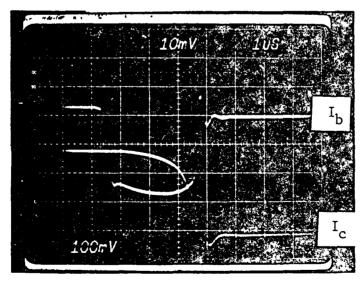


Turn-on at 150 A

I_b = 2 A/div

I_c = 50 A/div

Time 1µs
Figure 5.4.9c



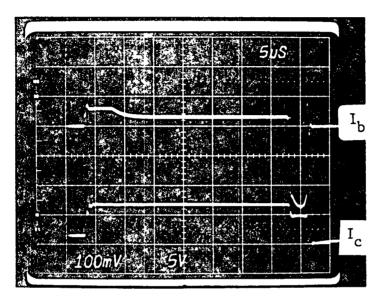
Turn-off at 150 A

I_b = 2 A/div

I_c = 50 A/ div

Time = lµs
Figure 5.4.9d

DUT: QM150DY-H



DUT Base Characteristics at $I_c = 150$ A

$$I_b = 2 A/div$$

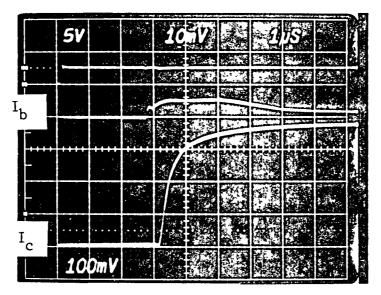
$$V_{be} = 5 \text{ V/div}$$

$$Time = 5us$$

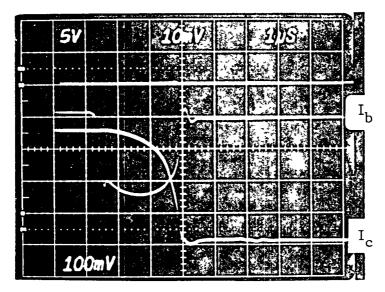
Time = 5µs Figure 5.4.9e

to a lack of sufficient base drive of the early turn-on stage. In Figure b is the turn-off characteristic. the 10 A is applied for a minimum 2.5 microseconds while the DUT turns off. The turn-off, like the turn-on, is rather sluggish except for the final transition. During the off time of the transistor, a constant 5 V is applied to the device. At full load turn-on, shown in Figure 5.4.10c, the PERG base drive supplies a turn-on current of approximately 2 A (due to a change of the series base resistance to 1.3 ohms and the use of a bypass capacitor across this series base resistor of 35 F). Some difficulty of the turn-on at full load was encountered since the automatic shut-down mechanism of the base drive integrated circuit was activated at the 140 A level. The difficulty encountered was that the current buildup of the collector current was slow compared the required time limitation in the reduction of collector to base voltage sensed by the integrated circuit. Since the collector current did not build sufficiently in time and the collector base voltage had not dropped to a low enough level, the integrated circuit would command the turn off of the transistor. By providing a slight increase in the initial turn-on base current to the Fuji DUT the collector base voltage dropped to a sufficient level to allow the integrated circuit to continue its base drive function at the 150 A full load current rating for the DUT. The turn-off curve shown in Figure 5 4.10d shows the initial current surge from the base drive circuitry and the well

D EVM31-050

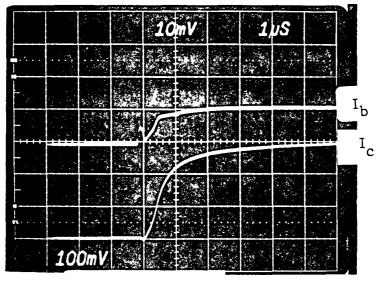


Turn-on at 75 A
I_b = 2 A/div (A)
I_c = 20 A/div (B)
Time = 1µs
Figure 5.4.10a



Turn-off at 75 A
Input = 5 V/div (A)
I_b = 2 A/div (B)
I_c = 20 A/div (C)
Time = 1µs
Figure 5.4.10b

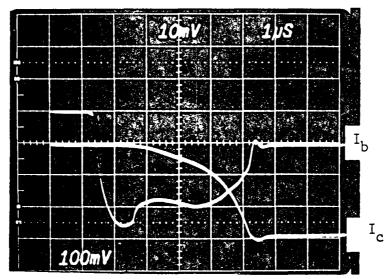
חויד EVM31-050



Turn-on at 150 A $I_b = 2 \text{ A/div}$ $I_c = 50 \text{ A/div}$

 $R_{b} = 1.3$ $C_b = 35\mu F$

Time = $1\mu s$



Turn-off at 150 A $I_b = 2 \text{ A/div}$

 $I_c = 50 \text{ A/div}$

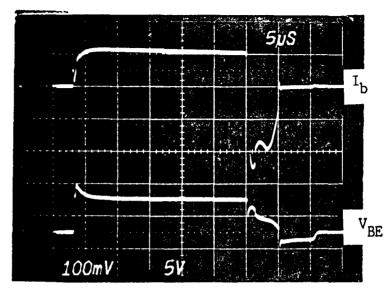
 $R_b = 1.3$

 $C_b = 35\mu F$

Time = 1μ s Figure 5.4.10d

PERG Base Drive

CUT: "VM 31-050



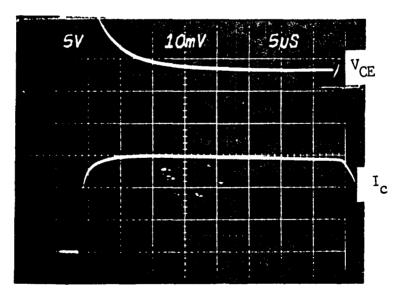
DUT Base Characteristics at $I_c = 150 \text{ A}$

$$I_B = 2 A/div$$

$$V_{BE} = 5 \text{ V/div}$$

Time =
$$5\mu s$$

Figure 5.4.10e



DUT Collector Characteristic V_{CE} = 5 V/div

$$V_{CE} = 5 V/div$$

 $I_c = 50 \text{ A/div}$

 $R_B = 1.3$

 $C_B = 35\mu F$

Time = $5\mu s$

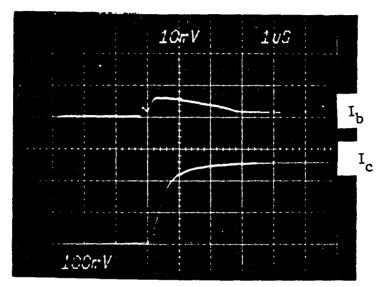
Figure 5.4.10f

behaved turn-off of the DUT. There appears to be a slight problem with the DUT rather than the base drive and the rapid turn-off of its collector current. In Figure 5.4.10e, the base drive current from the circuitry to the DUT and the base-emitter voltage of the DUT is shown. The abrupt rise of base current and the abrupt transition to reverse current is well documented. Shown in Figure f is the collector to emitter voltage of the DUT. As previously mentioned, the V_{Ce} of the device was slow to drop at turn-on. It was this voltage that caused the integrated circuit to cease its drive operation detecting a "fault" condition.

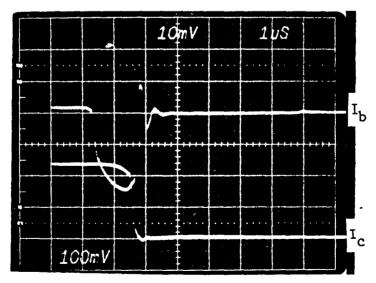
In Figures 5.4.11a-e are shown the response of the Westinghouse transistor to the PERG base drive. 5.4.11a&b are the turn-on and turn-off characteristics similar to those of the Mitsubishi device in Figure 5.4.9. The same comments apply. In Figures 5.4.11c&d the turn-on and turn-off characteristics of the DUT at full load (100 A) are shown. They are well behaved and within acceptable operating limits. The last oscillogram is Figure 5.4.11e which shows a composite base characteristic of the DUT (output of the PERG base drive). As indicated by the top minimum turn-off current is provided approximately 5 microseconds. The base drive then, goes into a proportional current drive mode providing the minimum current necessary to keep the collector base voltage within a predetermined amount. The lower trace shows the base-toemitter voltage in the forward and reverse (turn-off) mode.

Fir Sase Drive

['T KD 32-4510-10



Turn-on at 50 A $I_B = 2 \text{ A/div}$ $I_C = 20 \text{ A/div}$ Time = 1 μ s Figure 5.4.11a



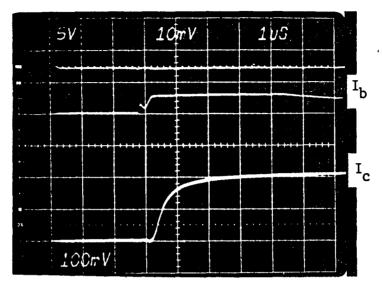
Turn-off at 50 A

I_B = 2 A/div

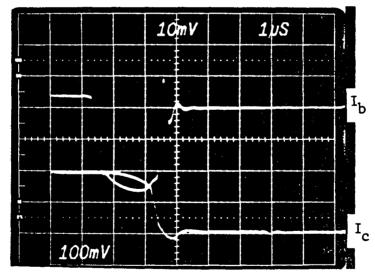
I_c = 20 A/div

Time - 1µs
Figure 5.4.11b

DUT: KD 32-4510-10



Turn-on at 100 A I_B = 2 A/div I_C = 50 A/div Time = 1µs Figure 5.4.11c



Turn-off at 100 A

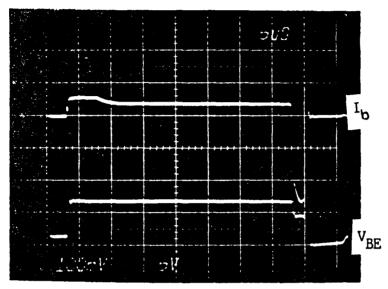
I_B = 2 A/div

I_C = 50 A/div

Time = 1µs

Figure 5.4.11d

DUT: KD32-4510-10



DUT Base Characteristics at $I_c = 100 \text{ A}$

 $I_B = 2 A/div$

 $V_{BE} = 5 \text{ V/div}$

Time = 5µs Figure 5.4.11e

5.5 EVALUATION OF TEST RESULTS

5.5.1 STATIC TESTS

5.5.1.1 MITSUBISHI BASE DRIVE MODULE (M57215L)

Reviewing the wave forms of Figure 5.4.1a for the forward base drive current to the DUT, we see a very fast rising current pulse to the base. For such high-current power switches as tested in this project it is important that the base drive current rise to its maximum value as quickly as possible. The given 0.84 microsecond rise time current pulse is very suitable to get the main power device (DUT) conducting as quickly as possible within its safe operating area. The turn-off portion of Figure 5.4.1a is indicative of the current flow through the base module and the reverse current through the DUT. The amount of overshoot indicates that a small overlap period exists when the source and sink transistors of the drive module may be This does not hinder the turn-off on at one time. properties of the base drive circuit. As shown in Figure 5.4.1b a very fast rising reverse current flows from the the DUT. A significantly long time of microseconds) is given for the device for the DUT to turn A holding current with a peak value of 0.5 A is available to maintain the DUT in the off state during the non-conduction part of the cycle. This current is supplied through the series resistor and the negative supply.

In summary, the DUT will see a very stiff current source for turn on and turn off base current pulses. This is indicated by the very fast rise time of the forward base current and reverse base current from the base drive module circuits.

5.5.1.2 FUJI BASE DRIVE CIRCUIT (EXB-356)

Reviewing the waveforms of Figures 5.4.2a and b it can be seen that the Fuji drives operated marginally within the manufacturer's specifications. The propagation delay as measured between input to the base drive circuit and activation of the DUT was slightly larger than the specification. However, an extra output stage was added between the Fuji base drive module and the DUT which can account for the increased delay. At elevated temperatures this propagation delay will increase due to the opto-coupler stage internal to the hybrid module. This delay increase most probably will remain within 15 s which is the delay allowable for the Mitsubishi drive.

Without active testing it is difficult to exactly measure the foward rise time but within the constraints of a DUT activated at low voltage and low current the rise time equalled the specification of 1 s. The rise time of reverse current was also approximately 1 s.

The reverse current drive is characterized by the

manufacturer by a rate of change of current from forward to reverse. Considering the first abrupt transition from forward to reverse base current flow the base drive circuit operated well within specification. This should be verified during the active test.

5.5.1.3 PERG BASE DRIVE

Since the PERG Base Drive uses active collector voltage feedback no static testing can be performed. Refer to Section 5.5.2.3 for active test results.

5.5.2 ACTIVE TESTS

This section will evaluate the Active Results from above section 5.4 and will be the basis for the Evaluation Summary in Secton 5.5.5.

5.5.2.1 MITSUBISHI BASE DRIVE CIRCUITS

This section will compare the operation of the three DUTs: Mitsubishi, Fuji and Westinghouse, when driven by the Mitsubishi base drive circuit.

From the Figure Sets 5.4.3, 5.4.4, and 5.4.5 we see that at full load the turn-on base current overshoot provided by the Mitsubishi base drive circuit assists in turning the DUT on rapidly for two of the three devices. In the Fuji device, the collector current does not rise

immediately. This appears to be due to the base drive circuit configuration and can be corrected if the base drive circuit parameters are modified.

With a storage time of 5.8 microseconds, which is half that of the other two DUTs, the Fuji device appears to be the more suitable DUT to be driven by this Mitsubishi base drive circuit. This lower storage time is a result of lower internal shunt resistance between base and emitter in the main transistor within the Fuji Darlington DUT. This lower shunt resistance allows a higher reverse current flow in the driver transistor to sweep out charge more quickly. This low resistance also explains why the base drive circuit finds difficulty turning on this Fuji DUT. The Mitsubishi and Westinghouse DUTs have comparable parameters at full load. To reduce their storage time, an increase in reverse base current would be needed.

CONCLUSION. The three devices appear to be suitably driven by this Mitsubishi base drive circuit provided some based drive parameters are changed, i.e. for the Fuji device, a higher turn-on base current is necessary whereas for the Mitsubishi or Westinghouse a higher turn-off base current is required. These changes can be implemented by changing the values of $R_{\rm F}$ and $R_{\rm R}$ (Fig. 5.3) respectively.

5.5.2.2 FUJI BASE DRIVE CIRCUIT

This section compares the performance of the three DUTs when driven by the Fuji base drive circuit. As shown in Figures 5.4.5, 5.4.6, and 5.4.7.

A significant difference can be seen between the three DUTs during turn-on. The best performer is the Westinghouse device when driven by this base drive. It is assumed that the high gain of the Westinghouse device contributes to This ıs explained by viewing the circuit configuration of the Fuji base drive given in Figure 5.1.2 and its operation as described in Figure 5.1. The Fuji base drive circuit uses a third transistor in a triple darlington configuration to drive the DUTs. However, the third transistor is not activated for very high gain DUTs but rather acts as a series diode between the base drive circuit and the DUT's input (base). The high gain Westinghouse DUT responds as if it were directly driven from the Fuji Base Drive Module.

At turn-off the Fuji base drive circuit is acceptable when driving the Fuji transistor at full load. Even at part load this base drive circuit performance is unacceptable. At turn-off the base drive current begins to flow out of the DUT then at the peak reverses direction and begins flowing back into the device or, at least, reaches a minimum turn-off current. The reverse current then continues to peak again and turn off the device in a natural manner. This action can be explained by viewing carefully the interaction

of the three transistors composing and the output transistor of the Fuji base drive and the DUT. When the current (Ib1) flowing from the base drive MODULE reverses direction (Ip2) a portion of the current, I_{b2} , is drawn through the base to emitter junctions of all three transistors and the remainder bypassing in the shunt base to emitter resistances in the This reverse current begins to turn off the internal drive transistor of the darlington DUT before the base drive circuit output transistor (DTR, Fig. 5.1.2b) begins to turn off. When the voltage across the emitter to collector of the Darlington drive transistor builds, the DTR's forward collector current begins to increase, thus reducing or stopping the reverse current flow out of the base of the The recovery of the DTR and DTU continues until the eventual forward biasing of the 'base to emitter bypass diode' of the DTR. Then, the Darlington DUT recovers as normal. The drive transistor of the Darlington is no longer seen as a saturated transistor and this condition during turn-off accounts for the collector current and base current reaching zero at the same time. This same turn off characteristic is observed in the results of the PERG base drive when the drive transistor of the darlington is not saturated. There will be a coincident zeroing of the base and collector currents.

It can be concluded that none of the three DUTs is acceptable with this base drive. For acceptable operation the output transistor of the base drive circuit (DTR) must

be sized such that it will be minimal in size compared with the drive transistor of the Darlington. This makes the circuit highly dependent upon the characteristics of the DUT such as temperature, gain, etc.

5.5 2.3 PERG BASE DRIVE

This section compares the three DUTs performance when driven by the PERG Base Drive as previously outlined.

The turn-on characteristics indicate the DUT's are adequately driven. However, the Fuji DUT is the least desirable due to the low effective gain exhibited. For this drive circuit to accommodate the Fuji device a change in the series base resistance, $R_{\rm B}{=}1.3$ ohms (refer to Figure 5.1.3c) was required along with a bypass capacitor across this resistor of value 35 F. An alternative solution would be to use a higher speed, lower $V_{\rm ce(sat)}$ device for the current sourcing transistor (Figure 5.1.3b). A good candidate for this transistor would be the recently reintroduced germanium transistors by companies i.e. Germanium Power Devices Corp., since they have a low $V_{\rm ce}$ which is desirable. Also the temperature dependence of the germanium transistor is not critical in this application.

The best performing DUT at turn-off is the Westinghouse device with the 790 nanosecond fall time and a 1 39 microsecond storage time. All devices, however, are acceptable.

To conclude, the Mitsubishi and Westinghouse devices are the preferred devices to be driven by this drive circuit, since the Fuji requires the higher quality output drive stage which translates into a higher cost.

5.6 EVALUATION SUMMARY

This section compares the three base drive circuits highlighting each of their advantages. Fortunately, there is sufficient commonality to allow for two concluding summaries as given in the last subsection 5.5.5.2.

5.6.1 BASE DRIVE CIRCUIT COMPARISONS

Since the PERG base drive uses a feedback mechanism for regulating the amount of base current to the DUT and the Mitsubishi base drive circuit and Fuji base drive circuit does not, the latter two circuits will be evaluated first and then the choice will be compared with the PERG base drive.

Independent of performance comparisons, the Fuji base drive had two undesirable characteristics. As outlined in section 5.1.1, two Fuji base drive circuit boards had to be constructed because of the high level of interference susceptibility exhibited by the Fuji circuit whereas the Mitsubishi board exhibited little if any interference susceptibility. In fact, the Mitsubishi board was more

"loosely" laid out than the Fuji's circuit and yet, outperformed the Fuji circuit. Another undesirable characteristic of the Fuji base drive circuit is the base drive "notching" explained in section 5.4.2.2 where the reverse base current is not steadily applied to sweep out charge from the main DUT. Other than performance characteristics The Mitsubishi circuit has an advantage compared to the Fuji in the input drive circuitry required. Since the Mitsubishi uses only one input photocoupler it is easier to interface with and appears to be more dependable.

Comparing the electrical performance characteristics of the two base drive circuits, refer to table 5.4, the Mitsubishi circuit drives the DUT sufficiently to cause a faster rise time of the collector current and a shorter delay time (from initiation by the input signal to the actual activation of collector current of the DUT). However, the fall time of the collector current of the DUT is faster by approximately 25% for the Fuji base drive circuit. The storage time and turn-off delay time of the two base drives are comparable.

Because of the undesirable action of the reverse current from the Fuji base drive circuit, the interference susceptibility and the small margin of performance improvement of the Fuji drive, the Mitsubishi base drive circuit is the preferred circuit of the two.

Next a comparison is made between the Mitsubishi base drive circuit and the PERG base drive. From a functional

systems point of view, the PERG base drive offers a number of advantages when monitoring and controlling the DUT's, operating parameters, such as, overvoltage, overcurrent, minimum on-time, etc. as described in section 5.1.5. The Mitsubishi drive would require many discrete external components to provide the same functions. The PERG base drive also, provides for fewer components, smaller size, lighter weight, higher reliability and easier assembly. Unfortunately, the PERG drive has no galvonic isolation.

Again using Table 5.4, a comparison between the Mitsubishi and PERG drives can be made. The Mitsubishi circuit provides a faster collector current rise time of approximately 0.3 microseconds which is five times faster than that provided by the PERG drive (averaged). The PERG drive, however, provides a 0.23 microsecond fall time at half load and a storage time of only 1.7 microseconds which is an order of magnitude lower than that provided by the Mitsubishi drive. Surprisingly, at full load the fall time of the DUT's collector current is comparable for either drive. Finally, the delay time of the drives at turn-on (approximately 5.5 microseconds) is comparable but the PERG excells at turn-off with only a 2.9 microsecond delay time which is approximately one order of magnitude faster than the Mitsubishi device.

5.6.2 CONCLUSIONS AND RECOMMENDATIONS

For a "simple" base drive circuit the Mitsubishi base drive is preferred over the Fuji. Surprisingly, if the storage time of the DUT is unimportant in the system design, the Mitsubishi base drive is also comparable to the PERG drive. If considering the base drive circuits at a systems level, then the PERG base drive excels. The PERG drive provides a self-regulated positive base current, a negative base current insuring fast turn-off at a constant current level, adjustable output current which can be increased by means of one or more external transistors, a selectable minimum conducting time to allow for discharge of any snubber networks, protection against saturation of the DUT, immediate limitation of the collector current to avoid overcurrent operation of the DUT, monitoring of the positive and negative base drive circuit power supplies and programmable maximum on-time.

Because the PERG base drive uses a dual resistor feedback scheme to determine the proportional base drive to the DUT, the base drive circuit must be optimized for the device under test. Also, the output driver stage for the Thompson-CSF Integrated Circuit (as outlined in Section 5.1.1) should be optimized for the current range that it is to be used in.

5.7 PERG Base Drive Development

The term "optimum base drive" has many different meanings to users of power transistors. There are some common desired functions within each meaning and these are incorporated in the PERG Drive. There are four major preferred functions as discussed below.

Many power electronic circuits incorporate small resistor-capacitor circuits to soften the harsh switching transients that appear across the power switching devices. These "snubber circuits" store energy during the period when transostor is cut-off. However, during the period when the transistor is turned on these snubbers must be discharged. Such a requirement may necessitate a "minimum on-time" operation of a power switch. The PERG Base Drive incorporates a "minimum on-time" function.

As a precaution in inductive switching circuits, a "maximum on-time" limit may be needed as a precaution against system malfunctions or power switching device overloads. The PERG Drive incorporates a "maximum on-time" limit for the power switching devices.

Almost all high power bipolar switching devices use a "bilateral base current" as a drive requirement. The PERG Drive provides such a drive condition. The forward turn-on current for the power device is controlled by feedback whereas the reverse base current for turn-off is at a preset level.

The most important feature of the base drive is to provide proportional base current. This assists the transistor in many ways such as, fast switching and more rugged operation. The PERG drive provides this function by monitoring the power switching device's collector base voltage and adjusts the base current to keep the voltage within a preset bound. This method inherently provides a means for over-current protection by turning-off the transistor when the bounding parameter is exceeded.

In summary the PERG Drive provides the following functions for power switch operation:

- Minimum on-time for power switch operation:
- Maximum on-time
- Bipolar base current
- Proportional base drive
- Current limiting

The following subsections will detail the theory involved in the proportional base drive along with the conceptual evolution of such a circuit. The last subsection documents the laboratory development and testing of the PERG Drive.

5.7.1 Theory of Operation for Proportional Base Drive

Nearly all high power transistors fabricated today are of a Darlington configuration [1] as shown schematically in Figure 5.7.1. From this configuration it can be shown that the transistor, T_2 , never operates in the steady state saturation region where the collector-base junction is forward biased. This is desirable, as will be discussed later, for fast switching transistors. However, the transistor, T_1 , can operate well into saturation unless its base drive circuit controls its region of operation. It is then the intent of a proportional drive circuit to control the "level of saturation" of transistor T_1 by varying the amount of base current, T_1 , delivered to T_1 in proportion to the collector (load) current of transistor T_2 .

How might this proportional current drive be accomplished? It can be shown from device physics that the current through a transistor device causes changes in the collector to base voltage drop, $V_{\rm cb}$. A preferred region of operation, as depicted on the simplified terminal characteristics in Figure 5.7.2, identifies this relationship. This preferred region is known as quasi-saturation. If a transistor operates to the right of this region a excessive amount of power can be dissipated due to the high $V_{\rm cb}$. If the transistor operates to the left in deep saturation then minimum power is dissipated. However, very high storage times are observed during switching that limits the transistor's maximum operating frequency and greatly increases the switching loss. Ideally, operation in the mid-region is

preferred to minimize \mathbf{V}_{cb} and the switching loss.

To provide a more quantitative approach to the control problem a small derivation of the physical parameters comprising the collector-base voltage is now undertaken. Figure 5.7.3 shows a one dimensional view of a high voltage bipolar power transistor. The area of most interest is the n-region and its interface at p-n-. In this area the collector-base voltage is due to: 1) the electric field due in the depletion region of the base-collector junction, 2) the electric field created in the space charge region due to high level injection of minority carriers, and 3) the electric field caused by the spacial current-resistance product in the bulk n- material. The expressions for these voltages can be readily derived from the Basic Current-Density equations. The currents due to the flow of positive change (holes) and negative charge (electrons) per unit area are:

$$J_{p} = q\mu_{p} p E - q D_{p} \nabla p \tag{1}$$

$$J_{n} = q\mu_{n} \quad n \quad E + q \quad D_{n} \nabla_{n} \tag{2}$$

where

q = magnitude of electronic charge (1.6x10⁻¹⁹C)

 μ = hole and electron mobility (450 cm²/v-s and 1500 cm²/v-s respectively)

p,n = hole and electron concentration, respectively

E = electric field

 Δ = diffusion coefficient equal to (0.059 /v)

V = gradient of charge concentration.

The major flow of current through this high gain transistor is due to electron flow. The hole current density can be considered negligible, therefore, from equation (1)

$$0.0 = q \mu_p p E - q D_p(dp/dx)$$

which implies that

$$E(x) = (KT/q) p^{-1}(x) (dp(x)/dx)$$
(3)

This represets the electric field in the n region (The depletion layer effect is not included.) Combining (3) and (2) and realizing that for high level injection the gradients dp/dx and dn/dx are equal

$$Jn = -2qDn (1+N_d/2p) dp/dx$$
 (4)

where n=p(x)+Nd from charge neutrality constraints. Since Jp = 0, the collector current

$$J_c = -Jn$$

and the solution to equation (4) is

$$p(x) = p(0) - (J_c x/2qDn) + (N_d/2) ln (p(0)/p(x)).$$
 (5)

Now we can view any part of the n region and find the voltage drops.

Referring back to Figure 5.7.2, the two extremes of the quasi-saturation region are labeled at A and A'. To the right of

A' the collector-base junction is reversed biased and the transistor operates in the active mode. At point A' the electric field caused by the collector-base junction's depletion layer is countered by an applied base-collector voltage, hence, there is no space charge region since there is no forward injection. The only voltage drop occurring across the collector-base terminals is due to the electric field caused by the collector current flowing thru the bulk n^- material. From equation (2) where $\nabla n=0$, n=3c and n=Nd, the voltage drop in the bulk material is

$$V_{b} = -\int_{0}^{x} E dx = JcW/q\mu_{n}N_{d}$$
 (6)

this equation shows the general results [2] that the slope of the line delineating active and quasi-sat is given by

$$m = R_{q}^{-1} = (q \mu_{n} N_{d} A / W)$$
 (7)

where A is effective cross sectional area

W is the width of the n region.

(Note: W can be obtained by applying equation

(6) at low current levels)

At the other extreme of quasi-saturation, point A, the transistor is nearing entry into hard saturation. This can be characterized in Figure 5.7.2 by a complete saturation of the negion with minority hole carriers injected from the p-n interface and extending to the n-n+ interface with the constraint that the concentration of holes reaches a nominal amount at the interface. This is depicted by the dotted line. These injected carriers avail themselves for charge transport and

consequently, modulates (reduces) the resistance of this n region. Two electric fields provide this effect. The first is caused by a junction voltage, V_j , due to the depletion layer at the metallurgical junction which must be overcome to provide charge injection. The second field from voltage, V_s , is due to the charge gradient of the space charge layer in the modulated region. Since the entire operating region from A to A' in Figure 5.7.2 is of interest, the voltages V_j and V_s will be expressed as a function of the amount of quasi-saturation and related thru the distance x that the injected charge passes within the n region. The space charge region produces an electric field (hence, voltage) as expressed in equation (3). Using equation (5) as the limits

$$Vs = -\int_{0}^{x} Edx = \int_{p(0)}^{p(x)} 0.0259/p(x) dp(x)$$
 (8)

$$= 0.0259 \ln (p(o) Nd/2.1x10^{20})$$

where
$$p(o) = p_o + p_{no}$$
, $p_x = p_{no} = n_1^2/N_d$,
 $n_1 = 1.45 \times 10^{10} \text{ cm}^{-3}$

The amount of injected charge at the p-n interface can be expressed as

$$p(o) = p_{no}(exp (38.6 v_1) -1)$$
 (9)

However, p_{no} is the uniform background charge concentration found throughout the n^{-} region. From equation (5) for $p(x) = p_{no}$ at some corresponding value x_{C}

$$p_{po}/p(0) = 1 + J_c \times (2qD_pp(0))$$
 (10)

Solving equation (9) and substituting equation (10) we have an expression for the junction voltage:

$$V_j = 0.0259 \ln \{1 + J_c x_c / 2q D_n p(o)\}$$

Finally, the voltage from collector to base of a power transistor in quasi-saturation can be calculated from [3]

$$Vcb = -\frac{J_{c}(W-x_{c})}{q \mu_{n} N_{d}} - \frac{KT}{q} \frac{p(0) N_{d}}{n_{i}^{2}}$$

$$-\frac{KT}{q} \ln \left(1 + -\frac{J_c x_c}{2qD_n p(0)}\right)$$
 (11)

for p(o) >> p_{no}

To ease the analysis the last term can be assumed to have a negligible effect.

To operate the transistor at point A in Figure 5.7.2 the entire n region is modulated, i.e. $x_{\rm C} = w$ and the major voltage drop from collector to base is due to the second term in equation (11). This indicates that $V_{\rm cb} = f(\ln p(o))$ and from equation (5) $p(o)\alpha J_{\rm C}$. However, our interest lies nearer to operation at the A' point of Figure 5.7.2. As can be seen from equation (11) for $x_{\rm C} = 0$, the first term dominates while the second term makes a minor contribution. This is the key that shows the direct dependence of $V_{\rm cb}$ on collector current and that which has been

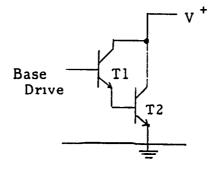


Figure 5.7.1

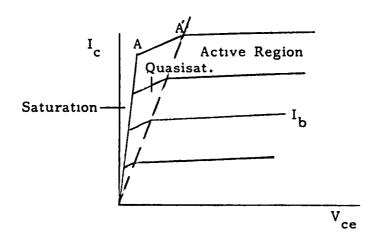
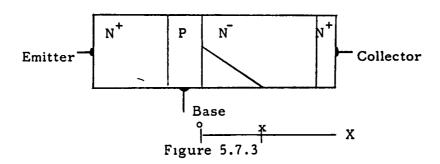


Figure 5.7.2



successfully used [4] to derive a proportional base drive. The PERG drive deviates little in theory from previous designs.

5.7.2 Proportional Drive Circuit Evolution

One method of proportional base drive control is the variation of base current to maintain constant V_{ch} voltage. has been done, historically, in the "Baker Clamp" topology for driving transistors shown in Figure 5.7.4. To prevent the transistor from saturating excess base current is diverted through the upper diode. When assuming equal forward drops across the forward conducting diodes, the \mathbf{V}_{ch} equals zero. Relating this to equation (11) it can be seen that the conduction drop in the collector is approximately equal to the voltage drop in the modulated and unmodulated n region countered by the voltage drop of the forward biased p-n injecting junction. Two drawbacks to this approach are: 1) The amount of modulation varies with temperature (due to gain change) and causes varying switching times; 2) though the base current to the transistor is proportional, the base drive supply current does not change. This later drawback is considerable since one main advantage to a proportional drive is the energy savings in the base drive supplies. A simple remedy suggested by D.C. Hopkins at VPI SU is shown in Figure 5.7.5. The middle diode of the circuit in Figure 5.7.4 is replaced by the base-emitter junction diode of the drive transistor in Figure 5.7.5. Now, the amount of excess current bypassing the main transistor's base (through the upper diode) is

reduced by the gain of the drive transistor. Ideally, the $v_{\rm cb}$ of the main transistor is still zero volts.

Unfortunately, maintaining a constant $V_{\rm Cb}$ is not desirable. As shown by equation (7) the $V_{\rm Ce}$ vs $I_{\rm C}$ characteristic gives a preferred straight line relation to the threshold edge of quasi-saturation. We have assumed $V_{\rm be}$ is constant and $V_{\rm ce} = V_{\rm be} + V_{\rm cb}$. Therefore, we must vary $V_{\rm cb}$ with changes of $I_{\rm c}$. This would be simple to implement in Figure 5.7.5's circuit if the transistor gain, $h_{\rm fe}$, was constant. This last assumtion about constant gain is not a serious limitation since a base drive cicuit design can be optimized for full load operation that would provide maximum performance and energy savings. At low loads any error, though possibly large in percent would have a minor effect because of the small magnitude of load curent.

To provide a larger V_{cb} at higher collector currents which requires higher base currents, a series base resistor, $R_{\rm b}$, can be connected as shown in Figure 5.7.6. This resistor provides the linear relation between V_{cb} and I_{c} . There still needs to be incorporated and offset term indicated in equation (11) and accurately identified by Mr. Rippel (reference 4). The additional resistor, $R_{\rm f}$, in Figure 5.7.6 allows the base drive circuit to control the V_{cb} in magnitude and degree of variation as a function of I_{c} . Again, refer to reference 4 for a practical step by step procedure for choosing the resistor values $R_{\rm b}$ and $R_{\rm f}$. This entire development assumes a fixed current supply, $I_{\rm B1}$ as shown in Figure 5.7.6.

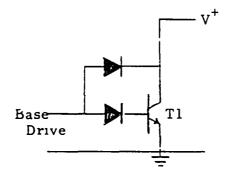


Figure 5.7.4

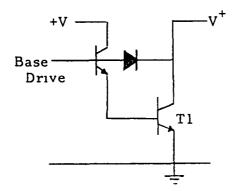


Figure 5.7.5

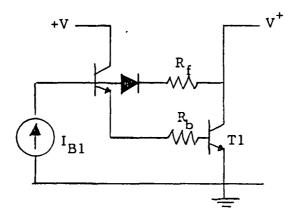


Figure 5.7.6

5.7.3 Circuit Development

The main component the PERG Base Drive Circuit is the Thomson-CSF Components Corporation's integrated circuit (IC) UAA 4002 "Control Circuit For Fast Switching Transistor" shown in Figure 5.1.3a. Besides providing many monitoring functions the IC has an ouput driver stage that replicates the desired circuit in Figure 5.7.6 (excluding the resistors and transistor) and is shown in Figure 5.1.3b. The output stage of the final circuit incorporating the UA 4002 IC is shown in Figure 5.7.7. selection of output Drive Transistors, T_1 and T_2 , was based on switching speed and availability and may not represet the optimum choice. All resistor values exept R_h and R_F were selected in the manufacturer's suggested accordance with application procedure. It should be noted that the manufacturer's the internal circuit arrangement description of 18 functionally descriptive. This was born out by many frustrating attempts to alter the external component arrangement to something different than what the application notes specifically suggested. One criticism of this IC is the inadequate description about the internal workings. However, when the manufacturer's suggestions were implemented the results were very gratifying.

Since the circuit uses a feedback loop for operation the circuit development and "Active Device Testing" were performed simultaneously. For this development the Mitsubishi power transistor was used as the Device Under Test (DUT). An example

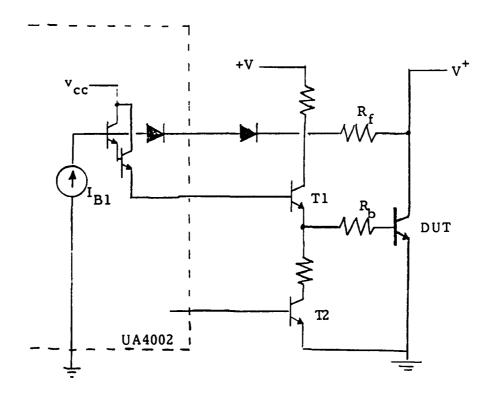


Figure 5.7.7

of the resulting waveforms of the PERG Base Drive output for base current, Ib, DUT's collector current, Ic, and collector-emitter, voltage, V_{ce} are shown in Figure 5.7.8. The important parameter to view is the V_{ce} of the DUT (top trace) as a decrease in I_{c} (middle trace) occurs. As can be seen, I_c reduces from 100 A initially to a 50% value while the base current, I, (lower race), reduces significantly (since this is the main function of a proportional base drive circuit). As noted in the previous section, we regulate I_b to regulate V_{cb} , however, with some variation in V_{ch} so that a somewhat constant portion of the n region is maintained in conductivity modulation within the transistor structure. The remaining part of the n region acts as a bulk resistor and its voltage varies proportionally with current. The base drive, also, provides an initially large base current pulse to get the DUT turned on quickly with minimum switching loss.

To demonstrate the controlability of the operating parameters of the base drive, Figures 5.7.9a and b are given as plots of V_{bc} (vertical axis) versus I_b (horizonal axis). The origin for both axes is denoted by the circle in the lower left. One should take a moment to fully understand the significance of these traces. Figure 5.7.10 gives the complete trace of a probable operating line. The two resistors R_b and R_F (in the PERG Base Drive circuit (Figure 5.7.7) control the slope and I_b intercept of the operating trajectory in Figures 5.7.9a and 5.7.9b. For both figures the base resistor, $R_b = 5.6\Omega$. For Figure 5.7.9a the feedback resistor, R_F is nearly twice that of

Figure 5.7.9b. For a larger feedback resistance value more current is diverted into the base current resulting in higher $I_{b'}$ for the same V_{bc} . A more informative view may be to consider $I_{b'}$ i.e., a higher V_{bc} (- V_{cb}) means the transistor is operating deeper into quasi-saturation (approaching full saturation). As I_{b} varies, as in Fgiures 5.7.8., the V_{bc} varies. Since R_{b} and R_{F} control the trajectory their values can be adjusted to provide optimum base drive to the DUT. Again refer to Reference 4 for a practical detailed method of selecting R_{b} and R_{F} .

The final results of the PERG Base Drive development are given in Section 5.5. The values for $R_{\mbox{\scriptsize b}}$ and $R_{\mbox{\scriptsize F}}$ were selectd empirically for these results.

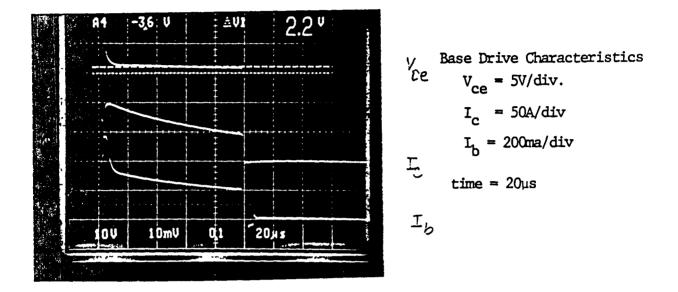
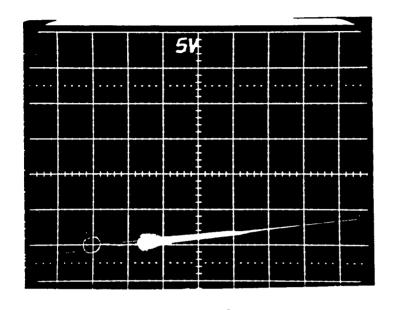


Figure 5.7.8

PERG Base Drive and DUT Outputs



 V_{bc} vs. I_{b} (vert.) $V_{bc} = 5V/\text{div}$ (horiz) $I_{b} = 125\text{mA/div}$ $R_{F} = 970\Omega$ $R_{b} = 3.6 \Omega$

Figure 5.7.9a Collector-Base Characteristic

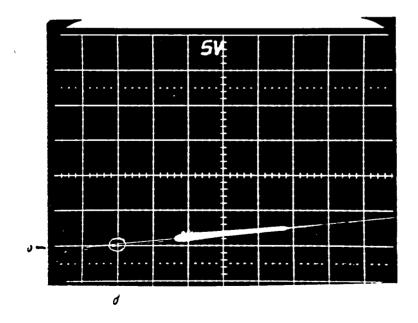


Figure 5.7.9b
Collector-Base Characteristic

Section 5.7 References

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6.0 CHARACTERIZATION OF POWER FETS

In this chapter, five different power FETs are evaluated. The ratings of these devices are given in Table 6.1.

Table 6.1
Ratings of Power FETs

No	Тур	I _D [A]	I _{DM} [A]	BV _{DSS} [V]	$R_{DS(on)}[\Omega]$	P _O [W]	PACKAGE
1	IRF 441	8	32	500	0.85	125	TO-3
2	RFK 15N45 (RCA)	15	40*	450	0.85	x	то-3
3	RFK 15N50 (RCA)	15	40*	50 0	0.85	x	TO-3
4	2SK 356 (Toshiba)	12	30	250	0.25	120	TO-3
5	2SK 386 (Toshiba)	10	15	450	0.7	150	PLASTIC

^{*} supposed

6.1 Test Tasks

Three sets of device parameters will be evaluated as described in the following:

A. Switching Times

- turn-on delay time td(on)
- rise time tr
- turn-on time ton = td(on) + tr
- turn-off delay time td(off).
- fall time t_f
- turn-off time toff = td(off) + tf

B. Conduction Resistance RDS(on)

x unknown

- R_{DS(on)} dependance on gate-source voltage (V_{GS})
- R_{DS(on)} dependance on case temperature

C. Device paralleling

6.2 Test Equipment

In general, the test equipment used for the power FET characterization is the same as that used for the bipolar transistors. The base drive circuit used in bipolar transistor testing is used here as a gate drive for the FETs. In order to avoid the effect of parasitics on the switching times of the FETs the power circuit of the tester was arranged as tight as possible, so that very fast switching times can be measured. The simple test circuit for the FET devices is shown in Fig. 6.1.

6.3 Test Method

All data are generated as a function of the drain current up to the maximum rated pulse drain current.

All data were measured using the gate-source voltage as the running parameter. In addition, the data were generated at different case temperatures. The switching times definitions are given in Fig. 6.2.

6.4 Test Conditions

All FET devices were tested under the following circuit conditions:

- Supply voltage was approximately one half of the rated maximum (breakdown) device voltage.
- gate-source resistance $R_{GS} = 4\Omega$
- Duty cycle < 1%

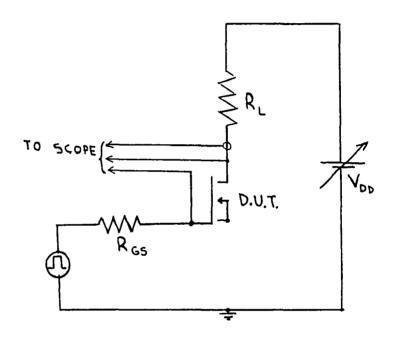


Fig.6.1. Test circuit for MOSFET characterization.

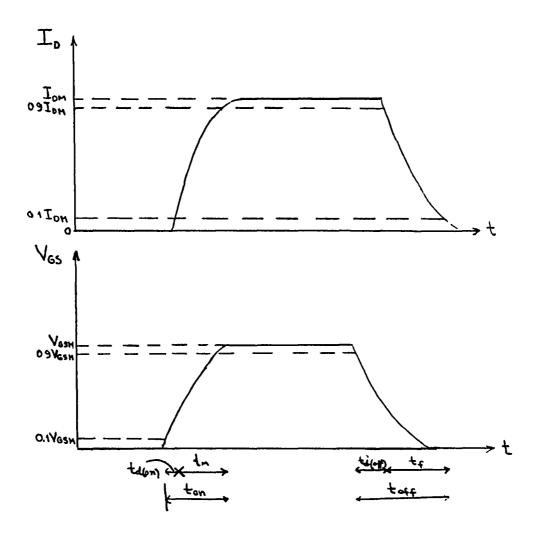


Fig.6.2. MOSFET switching times definition.

- gate-source voltage $V_{GS} = 10$ and 15V
- case temperature $T_C = 30$; 75; 100 °C

6.5 Test Results Presentation

The test results concerning various power FETs' characterizations are given in Appendices E to H.

In Appendix E, the test results of power FET on-resistance values are given, while in Appendix F the test results the of switching-times are presented. In appendix G, comparisons are made among the FETs. Finally, in Appendix H, the results of parallel operation of FETs are given.

6.5.1 On-Resistance Characteristics

The test results of the FETs' on-resistance values are given in Appendix E from Fig. E.1.1 to E.5.2. There are two graphs for each of the five devices. A description of the two graphs are given below using the data measured for the IRF 441 device.

on-resistance at
$$T_C = 30^{\circ} C$$
 (plot 1 in Fig. E.1.1)

This graph is a plot of on-resistance values as a function of drain current at two different gate voltages $V_{\rm CS}=10$ and 15V. The data were obtained at 30° C case temperature.

on-resistance at
$$T_C = 30^{\circ}$$
 75° 100° C (plot 2 in Fig. E.1.2)

For this graph, the gate-source voltage $V_{\rm GS}$ was constant at $V_{\rm GS}$ = 10V. At three different case temperatures, $T_{\rm C}$ = 30°; 75° and 100° C, the on-resistance values were measured as a function of drain current. This graph provides the information of on-resistance as a function of the case temperature.

6.5.2 Switching Characteristics

The test results are given in Appendix F, from Fig. F.1.1 to Fig. F.5.6. There are six graphs for each of the five devices. Switching characteristics were plotted as a function of drain current at two different gate drives ($V_{\rm GS}$ = 10V and 15V), while the drain-to-source voltage and case temperature were held constant at $V_{\rm DS}$ = 200V and $T_{\rm C}$ = 30 C, respectively.

Taking the IRF 441 device as an example those plots are as follows:

- turn-on delay time t_{d(on)} (plot 1 in Fig. F.1.1)
- rise time t_r (plot 2 in Fig. F.1.2)
- turn-on time $t_{on} = t_{d(on)} + t_{r}$ (plot 3 in Fig. F.1.3)
- turn-off delay time t_{d(off)} (plot 4 in Fig. F.1.4)
- fall time t_f (plot 5 in Fig. F.1.5)
- turn-off time toff = td(off) + tf (plot 6 in Fig. F.1.6)

6.5.3 Comparative test data

The comparative tests data plots are presented in Appendix G. The comparative test data were generated for on-resistance data as well as switching times data. From these plots relative comparison among five tested devices in terms of on-resistance and switching times is possible.

For on-resistance comparison three graphs are generated (Fig. G.1.1-G.1.3) with the comparative data for all devices at constant gate drive voltage $V_{\rm GS}$ = 10V and three different case temperatures $T_{\rm C}$ = 30°; 75° C; 100° C.

The switching times comparison can be made using two sets of graphs generated for two different gate drives $V_{\rm GS}$ = 10V (Fig.

G.2.1-G.2.6) and $V_{GS} = 15V$ (Fig. G.3.1-G.3.6).

Each set of graphs contains six graphs for six switching times characteristics ($t_{d(on)}$, t_r , t_{on} , $t_{d(off)}$, t_f , t_{off}).

6.5.4 Test Data of Parallel Operation Characterization

All test data of parallel operation characterization, given in Appendix H, are presented by oscilograms. The oscilograms were taken at different drain current levels, and for each current level three oscilograms are taken showing the load current sharing among devices. First oscilogram for each current level shows static current sharing while rest two show dynamic current sharing during turn-on and turn-off phases.

6.6 Test Data Interpretation

In this section the test results given in Appendices E to H, are discussed. However, because of a large number of data generated this discussion will be carried out in terms of a little bit more generalized form. The goal is to draw the clear conclusions about the power FETs' behavior regarding the measured performances, and that is:

- on-resistance characteristic
- switching characteristics
- parallel operation behavior

6.6.1 On-resistance Consideration

Using the plots given in Appendix E it is obvious that the following conclusions concerning on-resistance $R_{\mbox{DS}(\mbox{on})}$ of MOSFETs can be drawn:

• $R_{DS(on)}$ is increasing function of drain current I_D for the

constant gate drive (V_{CS});

- $m R_{DS(on)}$ depends on gate-source voltage V_{GS} . That dependence is for all devices very weak and tendency of higher V_{GS} is to reduce $m R_{DS(on)}$. Moreover, the influence of V_{GS} on $m R_{DS(on)}$ is more pronounced at higher currents, above the rated DC current, i.e., at the currents allowed only in pulsed mode operation. The strongest influence of V_{GS} on $m R_{DS(on)}$ was observed for the IRF 441, where at the maximum pulsed drain current, change of V_{GS} for 5V. (from 10V to 15V) causes the decrease of $m R_{DS(on)}$ approximately for 10% (2.20 to 20).
- $R_{\mathrm{DS(on)}}$ increases with a increase of the case temperature T_{C} for given V_{GS} . The change of resistance value with T_{C} , also, depends on the drain current level and it was observed that the temperature coefficient of $R_{\mathrm{DS(on)}}$ is greater at higher current levels. Positive temperature coefficient of $R_{\mathrm{DS(on)}}$ is very desirable for parallel operation of MOSFETs because it automatically tends to keep current sharing balanced.

In the Table 6.2 the intervals of the on-resistance values in the full range of drain current, at three different temperatures, are given. In fact, the Table 6.2 generalizes the data given in Appendix E.

Table 6.2 On-resistance values in the full range* of drain current at three different case temperatures $T_C = 30^\circ$; 75° ; 100° C for $V_{CS} = 100^\circ$

No.	Characteristic Device Type	R _{DS(on)} [Ω] at T _C =30°C	R _{DS(on)} [Ω] at T _C =75°C	R _{DS(on)} [Ω] at T _C =100°C
1.	IRF 441	0.8 - 2	1.3 - 2.6	1.4 - 3.6
2.	RCA RFK 15N45	0.45 - 1	0.7 - 1.1	0.8 - 1.5
3.	RCA RFK 15N50	0.55 - 1	0.7 - 1.1	0.9 - 1.4
4.	Toshiba 2SK 356	0.25 - 0.27	0.3 - 0.35	0.35 - 0.45
5.	Toshiba 2SK 386	0.55 - 0.65	0.8 - 1.1	0.9 - 1.35

^{*} Full range means from low current up to maximum pulsed current allowed. At higher T_C then 30°C derated maximum pulsed current values were taken.

According to the values of on-resistance $R_{\mathrm{DS(on)}}$, tested devices may be categorized as Table 6.3.

Table 6.3

Devices Relative Categorization Regarding the On-Resistance Values

LOW RDS(on)	2SK 356
MEDIUM R _{DS(on)}	RFK 15N45, RFK 15N50, 2SK 386
HIGH R _{DS(on)}	IRF 441

6.6.2 Switching Times Consideration

From the experimental data presented in Appendix F we can draw some general conclusions concerning switching characteristics of MOSFETs. The obtained results for each measured characteristic

 $(t_{d(on)}, t_r, t_{on}, t_{d(off)}, t_f, t_{off})$ are discussed separately.

A. turn-on delay time td(on)

The main conclusions about $t_{d(on)}$ can be summarized as follows:

- t_{d(on)} is almost independent of drain current I_D;
- $t_{d(on)}$ depends strongly on the gate drive conditions (V_{GS} and R_{GS});
- t_{d(on)} decreases with a increase of V_{GS};
- t_{d(on)} depends on the device type;
- for all five devices $t_{d(on)}$ is in the range from 80 ns to 60 ns. The upper range values correspond to smaller V_{GS} ; i.e., $V_{GS} = 10V$.

Such behavior of $t_{d(on)}$ can be explained recalling that $t_{d(on)}$ exists because some finite time is needed to charge up the gate capacitance to the threshold voltage value. That time depends on the gate drive conditions (V_{GG} ; R_{GS}) and the value of the gate capacitance, i.e., on the device type. It is clear that higher V_{GS} or smaller R_{GS} give smaller $t_{d(on)}$ and, therefore, for a constant drive (V_{GS} , R_{GS} = const), $t_{d(on)}$ depends solely on device typ. Since all measured devices are of the similar ratings (except 2SK 386), it should be expected that they have the similar areas and, therefore, the gate capacitances so the turn-on delay time is very similar, too.

B. Rise Time tr

From the data obtained for the rise time we can draw the following conclusions:

- t_r depends strongly on both drain current (I_D) and gate drive conditions (V_{CS}, R_{CS}) ;
- t_r is increasing function of I_D ;
- t_r is decreasing function of V_{GS} ;
- V_{GS} relative influence on t_r is stronger at the higher current levels (the range over D.C. current rating);
- the range of t_r measured for two different $V_{\rm GS}$ = 10; 15V is 5-30 ns at low currents and 300-400 ns at maximum pulsed current.

The observed behavior of t_r is very easily understandable since for the constant gate drive (V_{GS} , R_{GS} = const) higher current I_D requires longer time to be reached, while for the higher V_{GS} transistor sweeps faster through linear region because of the faster rate of the gate voltage increase (the faster gate capacitance charging) and, therefore, t_r is reduced.

C. Turn-On Time ton

Turn-on time (t_{on}) is given as a sum of turn-on delay time $t_{d(on)}$ and rise time (t_{n}) i.e.

$$t_{on} = t_{d(on)} + t_{r}$$

The general conclusions about ton can be summarized as follows:

- t_{on} depends on both I_{D} and V_{GS} ;
- t_{on} depends on I_{D} in the very same manner as t_{r} depends on I_{D} because $t_{d(on)}$ is virtually independent of $I_{D'}$
- t_{on} dependence on V_{GS} is because both $t_{d(on)}$ and t_r depend on

VGS;

- At the higher current levels (pulsed mode) t_{on} is virtually determined by t_{r} since $t_{d(on)}$ is relatively small;
- the range of t_{on} for two different V_{GS} and broad range of I_{D} , for all five measured devices, is 60-500 ns.

D. Turn-Off Delay Time td(off)

Concerning turn-on delay time $(t_{d(off)})$ from the data obtained we can draw the following conclusions:

- t_{d(off)} is virtually independent of drain current I_D;
- $t_{d(off)}$ depends on the gate drive conditions (V_{GS} , R_{GS});
- for the higher V_{GS} the value of $t_{d(off)}$ is greater;
- t_{d(off)} depends on transistor type;
- $t_{d(off)}$ range is 10-50 ns for device tested at two different $v_{GS} = 10;15V$.

For explanation of described behavior of $t_{d(off)}$ we have to recall that $t_{d(off)}$ exists because input gate capacitance needs some time to discharge from oversaturated gate voltage to the voltage which corresponds to active region gate voltage. Therefore, $t_{d(off)}$ primarily depends on gate capacitance in conjunction with gate drive conditions (V_{GS} , R_{GS}) and is independent of I_D for a given device typ. For higher V_{GS} the transistor gate voltage is more oversaturated so $t_{d(off)}$ is longer.

E. Fall Time tf

The main observations regarding the fall time (t_f) are:

• t_f depends on the drain current I_D for a constant gate drive and t_f increases as I_D increases;

- t_f is virtually independent of the gate voltage V_{GS} at all current levels;
- the range of $t_{\rm f}$ obtained for the measured devices in full current range is 15 ns-220 ns;

Because t_f represents the time which device spends sweeping through the active region in turn-off phase and, since off-gate voltage is zero (not negative gate drive was used), then for the given current level time needed for the gate capacitance to discharge from the voltage at the beginning of the active region to threshold voltage does not depend on a positive value of V_{GS} used to turn the device on. However, t_f depends on R_{GS} because it determines the gate time constant in conjunction with the input gate capacitance. For a higher I_D longer time t_f is needed for a discharge of gate capacitance because the voltage at the beginning of active region is higher.

F. Turn-Off Time toff

Turn-off ($t_{(off)}$) time is given as a sum of turn-off delay time ($t_{d(off)}$) and fall time (t_f) i.e.,

The general conclusions about toff can be summarized as follows:

- t_{off} depends on both the drain current I_{D} and gate voltage v_{GS} ;
- t_{off} dependence on I_D is because t_f depends on I_D , since $t_{d(off)}$ does not depend on I_D ;
- t_{off} dependence on V_{GS} is due to $t_{d(off)}$ dependence on V_{GS} , since t_f virtually is independent of V_{GS} ;
- at the higher current range (pulsed mode) t_{off} is virtually determined by t_f since $t_{d(off)}$ is relatively small;

• the range of $t_{\rm off}$ for two different $V_{\rm GS}$ = 10;15V in the full range of $I_{\rm D}$, for all five measured devices, is 25-270 ns.

Some important conclusions explained earlier are summarized in the Table 6.4.

Table 6.4

Summary regarding switching characterization of MOSFETs

No.	behavior	Depe	nds on		Influence of	the Increase of
	characteristic	I _D	V _{GS}		I _D for V _{GS} = const	V _{CS} for I _D = const
1.	td(on)	No	Yes		No	Decrease
2.	t _r	Yes	Yes	-	Increase	Decrease
3.	ton	Yes	Yes	-	Increase	Decrease
4.	^t d(off)	No	Yes		No	Increase
5.	^t f	Yes	No	_	Increase	No
6.	t _{off}	Yes	Yes	-	Increase	Increase

In addition to Table 6.4 we have to point out that gate circuit series resistance R_{GS} also influences the swithcing characteristics. Its influence is always to improve the switching performances as it becomes smaller and smaller. In our investigation it was kept at constant value $R_{GS} = 4\Omega$. However, the minimum value of R_{GS} is limited by possible gate circuit oscillations.

From Table 6.4 we can conclude that higher $V_{\mbox{\footnotesize GS}}$ improves turn-on characteristics and degrades turn-off performances, therefore, there is trade-off between those two.

Finally, in Tables 6.5 and 6.6 we have shown typical switching

time values for five tested devices and relative comparison among them.

Table 6.5 Typical Switching Time Ranges for $V_{GS} = [10; 15V]$ and in Full Range of I_D (up to maximum pulsed rated)*

No.	Characteristic DEVICE TYPE	td(on)	t _r (ns)	t _{on}	^t d(off) (ns)	^t f (ns)	t _{off} (ns)
1.	IRF 441	60-680	35-370	100-440	10-20	40-80	10-100
2.	RCA RFK 15N45	60-80	35-370	100-440	30-50	120-240	150-290
3.	RCA RFK 15N50	60-80	35-370	100-440	30-50	90-170	120-120
4.	Toshiba 25K 356	60-80	30-420	90-500	15-30	30-140	45-170
5.	Toshiba 25K 386	60-70	5-120	65-190	10-20	30-40	40-60

^{*} devices have different $\boldsymbol{I}_{\boldsymbol{MD}}$ rating see Table 6.1

Table 6.6
Relative comparison of tested devices regarding switching performance

fast	IRF 441, Toshiba 2SK 386
medium	RCA RFK 15N50, Toshiba 2SK 356
slow	RCA RFK 15N45

6.6.3 Parallel Operation Consideration

All five device types were tested for two-device parallel operation behavior. The main concern in parallel operation is about static and dynamic load current sharing among devices as well as the stability of that operation. The analysis of parallel operation was carried out by monitoring the load current sharing at different current levels for different gate-source voltages and duty cycles. Because all results qualitatively were identical as for $V_{\rm GS}=10{\rm V}$ and duty cycle d = 1%, only oscillograms for those conditions are presented in Appendix H. An impact of higher duty cycle is to increase a case temperature and decrease steady-state current level (for constant drain supply voltage) due to increase in on-resistance value at higher temperatures.

From the obtained data (presented in Appendix H using format explained in section 6.5.4) we can draw the following conclusions:

• for all devices under consideration static sharing of load current at all drain current levels are relatively good.

Generally speaking' the static sharing is within 5A difference of the individual drain currents. It can be caused either because of the spread of on-resistance values or because of

nonequal parasitic resistance of the test circuit for each device, although, all were done to make it equal. Our belief is that the second reason is prevalent.

- dynamic sharing during the turn-on phase is good for all devices and at all drain current levels and slight differences were caused primarily because of non-equalized parasitic inductances in individual circuits, in spite of all precaution taken to avoid that
- dyanmic sharing during the turn-off phase is, also, good for all devices and at all drain current levels
- the stable parallel operation were observed for all devices at all drain current levels except for Toshiba 2SK 386 device.

To elaborate on the last observation we will use the Fig. H.5.4 and H.5.7 (or fig. H.5.8 and fig. H.5.11) which were taken under the same test conditions but in two different times after the test beginning. Namely, the oscillogram in Fig. H.5.4 (or H.5.8) was taken immediately after the application of the gate drive (several seconds after), while the oscillogram in Fig. H.5.7 (or fig. H.5.11) was taken after 3 minutes of parallel operation. As it can be seen the current sharing in the beginning of parallel operation is good but after some time (3 minutes) we observe the current robbing where one device takes more current then another one (sum of those two currents in both figures are the same due to the constant load current). This tendency is such that eventually one device takes the full load current Of course, when load current is higher then rated current of the device which tends to take over the load current the device fails and immediately after fails the another device because of the same reason.

In other words Toshiba 2SK 386 device exhibits positive drain current temperature coefficient (like bipolars) and can not be used in direct (without some additional network) parallel operation.

All other devices were tested for stability but neither has shown instable (current robbing) mode of operation.

6.7 Some Comments on the MOSFETs Characterization

In addition to the discussion presented in the previous section here we want to point out some important facts concerning the MOSFET characterization and application which are not mentioned or, only, briefly discussed earlier.

First, a comparison between the test data and specified manufacturer's data can be carried out only approximately because the test data are generated under somewhat different conditions and are much more detailed than specified. Nevertheless, it has been found the reasonable agreement between the test and specified data for conditions which are similar, for all device and for all resistance and switching characteristics. However, the data generated for parallel opertion of two devices are quite new regarding that they are not given in data specifications.

Second, in order to ultize the full advantage of fast switching speed of power MOSFETs the layout design of power circuit must be carefully done. In fact, due to very fast switching speed, i.e., the fast turn-on and turn-off time (generally $t_{\rm on}$ < 500 ns; $t_{\rm f}$ < 300 ns) the parasitics of the circuit must be kept as small as possible. Otherwise the current switching times are determined not by device but the parasitic components. It means that MOSFET circuit must be very tight. In addition, for operation with an inductive load turn-on tire

is determined by load circuit while turn-off time is affected by free-wheeling diode. To obtain fast $t_{\rm off}$ the diode must be faster than device. Also, in this case MOSFET circuit must be free of parasitic inductance as much as possible to achieve the fast response and low drain voltage spike.

Third, as we have explained the switching performances of MOSFETs are strongly affected by the gate drive conditions (see Table 6.4). In fact, the switching performances depend on how fast we are able to charge and discharge nonlinear gate capacitance. Practically, it means that the gate circuit time constant $\tau = R_{GS}^{x} C_{gate}^{x}$ conjunction with the value of gate supply voltage $(V_{GG} = V_{GS})$ controls switching speed. However, turn-on characteristic can be improved by using higher V_{CS} and smaller R_{CS} , while turn-off characteristic is slightly affected by V_{GS} (only through $t_{d(off)}$) and getting worse with higher V_{GS} , but can be improved by reducing R_{GS} (reducing t_f). Unfortunately, R_{GS} minimal value is limited by oscillations of gate circuit because the input gate capacitance along with the parasitic inductance of gate circuit for sufficiently low $\mathbf{R}_{\mathbf{GS}}$ form poor damped resonant circuit. In addition, smaller R_{CS} increases the power dissipation of drive circuit. Therefore, the choice of \mathbf{R}_{dS} is up to designer depending of concrete situation. The upper value of V_{CS} is limited by the gate breakdown voltage (usually 20V). The higher the ${\rm V}_{\rm GS}$ the smaller parasitic inductance is allowed in gate circuit, due to possible gate spike voltage which can cause the failure of device.

Finally, in parallel mode of operation in order to achieve the good static and dynamic load current sharing the circuit design should be symmetrical so that the both devices see the same circuit

parameters. It means that all connections must be of equal length as well as all contacts should be with the same resistance. Also, the thermal coupling of devices should be good; although that is not essential as in the case of bipolar devices. Only devices with the negative drain current temperature coefficient may be paralleled directly.

7.0 ASCR Testing

An alternate power switch to the transistor is the thyristor. It has advantages of high current capability at low cost but has a disadvantage of not being a self-commutating device (except the Gate-turn-off type). The Asymmetrical Silicon Controlled Rectifier (ASCR) is of this thyristor family and enjoys the advantage of having the highest switching speed. To accomplish the higher speed the device is fabricated to have different forward and reverse blocking voltage ratings ("asymmetric" ratings).

The testing of the Siemens company's BStH6140f device is reported in this section. The summary information is given in the last subsection. The test procedures followed are standard for Thysistors and test parameters are similar to those in the devices specification sheets, Figures 7.1a and b.

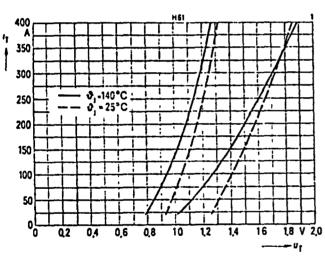
7.1 Test Results

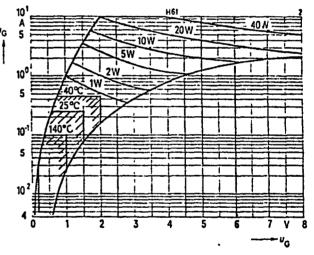
The significant test results can be divided into two areas; results from testing the input gate to cathode characteristics (V_{GT} , I_{GT}), and results from the output switching time (tq) and conduction drop (V_{F}).

The test results are summarized in Table 7.1. In early testing two of the four Siemens device samples were destroyed due to operator/hardware error. Therefore, data for only two devices are available. The testing was performed in a straight forward manner using semi-automated test equipment and using test

Sperr- und Blockierrichtung Hochster positiver bzw negativer Sperrstrom	I _O , I _R	_ 10 mA	Nebenbedingungen $S_i = 140$ C, bei 0,67 $U_{DR^{11}}$, 0,67 U_{RRM} = 140° C, bei U_{DRM} , U_{RRM}
Durchlaßrichtung Grenzeffektivstrom	Itanis(i)	250 A	
Stoßstrom	I _{TSM(i)}	1850 A 1650 A	θ_i = 25°C Sinushalbwelle = 140°C \int 50 Hz, U_R = 0 V
Grenzlastintegral	∫i²dt	17 200 A ² s 13 700 A ² s 10 000 A ² s 8 000 A ² s	$\theta_{i} = 25^{\circ}C$ $t = 10 \text{ ms}, U_{R} = 0 \text{ V}$ = 140°C $t = 2 \text{ bis 5 ms}$ = 140°C $t = 2 \text{ bis 5 ms}$
Schleusenspannung Differentieller Widerstand	<i>и</i> (то)	1,03V 1,65 mΩ	Ersatzgerade für 3; = 140°C
Dynamische Werte, Ein- und Aussc Einraststrom	chaltverhalten I _{LAT}	0,5 A 1,0 A -	$S_i = 140^{\circ}\text{C}$ $U_D = 18\text{V}$, = 25°C $I_G = 1\text{ A}$, $d_{IG}/dt = 1\text{ A}/\mu\text{s}$, = -40°C $t_{gt} = 15\mu\text{s}$
Zundverzug	t _{gd}	2,2μs 1,5μs	$I_G = 1 \text{ A} \ d_{IG}/dt = 1 \text{ A}/\mu \text{ s}, \ \vartheta_I = 25^{\circ}\text{ C}$ $I_G = 3 \text{ A} \ U_O = 0,5 \ U_{ORIM}, \ L/R = 2 \ t_{gd}$ $I_{TM} = 16 \text{ A}$
Kritische periodische Laststromsteilheit bei zusätzlicher Beanspruchung aus einer RC-Beschaltung	(d://dt) _{cr}	150 A/μs	$I_{TM} = 16 A$ $S_1 = 140^{\circ} C$, $f = 50 Hz$, $U_D = 0.67 U_{DRM}$ Langimpuls mit linearem Stromanstieg auf $I_{TM} = 480 A$ Zusatzlich zulassige Einschaltstromspitze aus RC-Entladung, $I_{TM(RC)} = 100 A$ notwendige Ansteuerung $I_G \ge 1 A$, $d_G/dt \ge 1 A/\mu s$
Periodischer Einschaltstrom aus RC-Beschaltung	<i>I</i> тм(RC)	100 A 50 A	$di/dt \Rightarrow (di/dt)_{cr}$ notwendige Ansteuerung $I_G \ge 1 \text{ A, } di_G/dt \ge 1 \text{ A/μs}$ $di/dt \le 10 \text{ A/μs}$ notwendige Ansteuerung $I_G \approx I_{GT}$ $di/dt = \frac{10 \text{ A/μs}}{10 \text{ A/μs}}$ $0,67 \text{ U}_{ORM}$
Kritische Spannungssteilheit (Typ BSt H61) (Typ BSt H61S9)	(du/dt)cr	200 V/μs 1000 V/μs 100 V/μs 500 V/μs 2000 V/μs	0,67 UDRM O,33 UDRM Linearer 1,0 UDRM O,67 UDRM O,33 UDRM O,33 UDRM Offen.
Freiwerdezeit (Typ BSt H61 _f) (Typ BSt H61 g)	t _q	15μs 18μs	$S_{\rm i}=140^{\circ}{\rm C}, -{\rm d}/{\rm d}t=-10{\rm A/\mu s}$ $U_{\rm R}=0.67U_{\rm RRM},U_{\rm D}=0.67U_{\rm DRM}$ ${\rm d}u/{\rm d}t=50{\rm V/\mu s},I_{\rm TM}=160{\rm A}$ Tablette vor Kommutierung voll durchgeschaltet
Steuerkreiswerte Oberer Zündstrom	/ _{GT}	100 mA 250 mA 450 mA	$S_{i} = 140^{\circ}C$ = 25°C = -40°C $U_{0} \ge 2V$
Obere Zundspannung -	<i>U</i> _{GT}	1,0 V 1,5 V 2,0 V	S_i = 140°C = 25°C = -40°C U_0 ≥ 2V
Nichtzundender Steuerstrom	IGO	 5 mA	$S_1 = 140^{\circ} \text{C}, U_0 = 2 \text{V}$ = 140° C, $U_0 \le 0.5 U_{\text{DRM}}$
Nichtzündende Steuerspannung	U _{GD}	0,2 V	$S_1 = 140^{\circ} \text{ C}, U_0 \le 0.5 U_{ORM}$
Hochster zulassiger Steuerstrom	IGM IGest	10 A 3 A	Scheitelwert Figure 7.1a Effektivwert Siemen's Device Data
Hochste zufassine Stellerverfliste	P~	20 W	Grenzwert 225

Thermische Werte Nebenbedingungen Hochste, dauernd zulassige Sperrschichttemperatur 140°C 9(1) Betriebstemperaturbereich S, -40 bis +140°C Lagertemperaturbereich 9. -40 bis +150°C Warmewiderstand für Konstantstrom RthJC 0,17 K/W doppelseitige Kühlung 0,30 K/W (ohne Übergang) anodenseitige Kühlung 0,40 K/W kathodenseitige Kühlung doppelseitige Kuhlung \siehe Montage-Warmeübergangswiderstand 0.015 K/W RthCK 0,030 K/W einseitige Kuhlung } anleitung Mechanische Werte 2000 N ± 11% Sollwert Anpreßkraft Anode - Gitter Kriechstrecke 5_{mm} Anode - Gitter Luftstrecke 5_{mm} Gewicht 60 g 50 m/s² Rüttelfestigkeit bei 50 Hz, ohne Kühlkörper C nach DIN 40 040 **Feuchteklasse** Kennlinien Durchlaßkennlinien (Streubander) Eingangskennlinien (Streuband) Parameter. Sperrschichttemperatur & mit Zündbereichen und Verlüstleistungshyperbein H61 20W ¹G





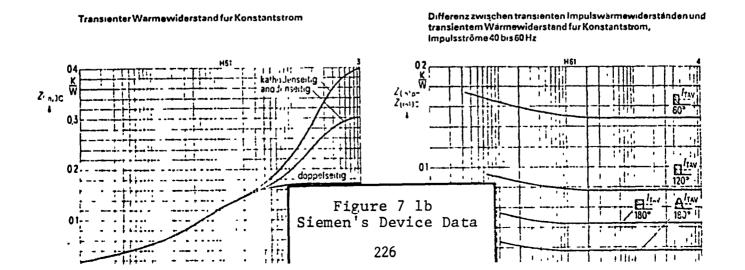


TABLE 7.1 SIEMENS - BStH6140f

UNIT	V _G r	I _{GT}	DRM	IRRM ₁	v _F	t * q	IH	L
	(V)	(MA)	(400V) μΑ	(400V) μΑ	(400A) (V)	(10A/µs) µs	(MA)	(MA)
1	0.94	72	5	6	1.5	22.6	44	260
2	0.94	72	6	7	1.7	24.7	51	260

*t_q tests at $\approx 140^{\circ}$ C

TABLE 7.2

GENERAL ELECTRIC - CA 358
(Manufacture's Data)

UNIT	V _{GT}	I _{GT}	IDRM	IRRM ₂	$v_{_{\mathbf{F}}}$	t _q *	IH	IL
	(V)	(MA)	(400V) μA	(400V) μΑ	(400A) (V)	(10A/μs) μs	(MA)	(MA)
15	1.57	57	15	30	2.39	8.6	41	395
26	1.50	54	15	32	2.57	6.6	55	705
28	2.53	64	14	84	2.47	7.8	63	480

 $t_{
m q}$ at $140^{
m 0}$ C

parameters from the device data sheets (Figures 7.1 a and b.)

Since only one manufacturer's device (Siemens) is being tested a set of another manufacturer's test results are included in Table 7.2 for comparison. The data in Table 7.2 are for three samples of a General Electric CA358 Asymmetrical SCR. For further information refer to Figures 7.2a and b.

Referring to Table 7.1., the trigger voltage and trigger current, V_{CT} , I_{CT} , for the Siemens device are given. From the low values of the gate to cathode, voltage $\mathbf{V}_{\mathbf{CT}},$ and the large gate current, I_{CT} , it appears these devices do not have an amplifying gate. This can provide some speed up in switching but consequently, requires a large gate drive. The next two parameters are the forward and reverse off-state leakage currents, respectively. It should be noted that these measurements for $\mathbf{I}_{\mbox{\footnotesize{DRM}}}$ and $\mathbf{I}_{\mbox{\footnotesize{RRM}}}$ are taken at 400V. It appears the Siemens device is not asymmetrical as originally believed. This shown better in Figure 7.3 oscillograph (with a negative horizonal voltage scale). A true asummetric would have a reverse breakdown at less than 60V. Also, the very low (leakage) current values indicate a smaller than expected amount of "deep level" dopants within the silicon thyristor structure. For very fast thyristor switch characteristics the silicon structure might be gold to help facilitate doped with materials such as recombination of minority charge carriers and hence, speed up the switch's turn-off. These curents indicate that the Siemens device can be a fast switched thyristor or "Inverter Grade"



ASYMMETRIC

Silicon Controlled Rectifier

1400 Volts

260A RMS ¹

20 5 5 0 04
Supersedes 20 9 7/81
ENERGY SAVER SERIES

CA358



The General Electric CA358 Asymmetrical SCR's are designed specifically to meet the demanding requirements of high power inverter and chopper circuits. The CA358 is rated at 260A RMS at 1000 Hz and fully characterized for operation up to 10 KHz... Its high off-state voltage combined with its low on-state voltage and short turn off time makes this innovative thyristor ideal for today's changing technology.

Equipment designers can use the CA358 ASCR in such applications as DC choppers, PWM inverters, UPS systems, and variable speed AC motor controls - wherever the SCR does not require reverse blocking capability.

DC choppers, wherever the

Companion anti-parallel diodes to be used with ASCR's are also available.

FEATURES

- Faster turn off times than inverter grade SCR's with lower forward voltage drop at comparable current.
- Higher surge current capability than inverter grade SCR's.
- Directly replaces conventional inverter grade SCR's in most applications where an anti-parallel diode is present and also utilizes existing gate drive circuitry.

BENEFITS

- Improved overall system efficiency due to dramatically reduced conduction and switching losses
- Improved system overload capability
- Simplified and less costly circuit design

MAXIMUM ALLOWABLE RATINGS

TYPES	REPETITIVE PEAK OFF-STATE VOLTAGE, V _{DRM} ² T _J = -40°C to +125°C	REPETITIVE PEAK REVERSE VOLTAGE, V _{RRM} T _J = -40°C to +125°C		
CA358PD	1400 Volts	10 Volts		
CA358PC	1300	10		
CA358PB	1200	10		
CA358PA	1100	10		
CA358P	1000	10		
CA358T	900	10		
CA358N	800	10		
CA358N	800	10		

NOTES

1 65°C, 1,000 Hz, 50% duty cycle, sine wave, 800 lbs pressure

2 Half sine wave waveform, 10 ms max pulse width

Figure 7.2a. ASCP-CA358

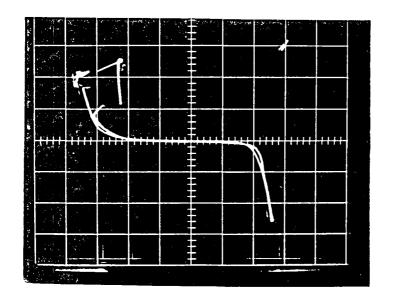


CHARACTERISTICS AND RATINGS

TEST	SYMBOL	MIN.	TYP	MAX.	UNITS	TEST CONDITIONS
Repetitive Peak Off-State Current	IDRM	-	12	20	mA	T _C = +125°C, = V _{DRM}
Repetitive Peak Reverse Off-State Current	IRRM	1	_	1	A	T _C = +125°C V = V _{RRM} =10V
Peak On-State Voltage (For incoming test correlation only)	VTM	ı	19	26 3.1	Volts	TC=125°C, IF=500 Amps (See fix 7)
Conventional Circuit Commutated Turn-Off Time -1 -2	£q.	1	1 1	15 20	µsec µsec	(1) I _T = 2000A (2) T _J = 425 C / 25 C (3) dv/dt = 400 V/µsec (4) dt/dt = 100 A/µsec (5) Pulse Width = 500 µsec (6) V _R = 5 V _{MAX} Use LEM with Divide (7) V _{REAPPLY} = 0 67 V _{DRM}
DC Gate Trigger Current	IGT	_	70	250	mAdc	$T_J = +25^{\circ}C$, $V_D = 6 \text{ Vdc}$, $R_L = 3 \text{ Ohms}$
(For incoming test correlation only Recommended gate supply for optimum performance is 20V,		_	100	400		T _J = -40°C, V _D = 6 Vdc, R _L = 3 Ohms
20Ω with pulse rise time < 0.2 microsecond.)		+	25	175		T _J = +125°C, V _D = 6 Vdc, R _L = 3 Ohms
DC Gate Trigger Voltage	V _{GT}		3	5	Vdc	T _j = -40°C to 0°C, V _D = 6 Vdc, R _L = 3 Ohms
(For incoming test correlation only Recommended gate supply for optimum performance is 20V,		_	1 25	30		T _J = 0°C to +125°C, V _D = 6 Vdc, R _L = 3 Ohms
20Ω, with pulse rise time <0 2 microsecond)		0 15	-	_		T _J = 125°C, V _{DRM} , R _L = 1000 Ohms
DC Gate Current not to Trigger	IGNT	3		_	mAdc	T _C = +125°C, 50% V _{DRM}
DC Gate Voltage not to Trigger	V _{GNT}	4	_	-	V	T _C = +125°C, 50% V _{DRM}
Critical Exponential Rate-of-Rise of Forward Blocking Voltage (Higher values may cause device switching)	dv/dt	400	600	_	V/µsec	T _C = +125°C, Gate Open 08 V _{DRM}
Critical Exponential Rate-of-Rise of On-State Current Non-Repetitive	dı/dt (1)	_	_	800	A/µsec	See Curve 10, Note #2.
Repetitive			<u> </u>	500		
Peak One Cycle Surge (Non-Rep) On-State Current (\bar{x} = MEAN VALUE) (σ = STANDARD DEVIATION)	ITSM	π π-σ π-3σ		2,200 2,000 1,500	A A A'	60 Hz, 800 lb Mounting
		x̄ x̄-σ x̄-3σ		2,100 1,900 1,500	A A A	50 Hz, 800 lb Mounting
I't for Fusing (X = MEAN VALUE	I²t	x x - 3σ	•	2.0 x 10 ⁴ 1 04 x 10 ⁴	A ² sec	t≥83 Milliseconds, 800 lb Mounting
(σ=STANDARD DEVIATION)	1	x x - 3σ		1 x 10 ⁴ 6 6 x 10 ³	A ² sec	t ≥ 2.0 Milliseconds, 800 lb Mounting
Thermal Resistance	$R_{\theta JC}$	-	12	135	°C/Watt	Junction-to-Case (Double-Side Cooled) , 800 lbr
Mounting Force		800 3.56	-	_	LBS KN	

⁽¹⁾ di/dt Ratings Established in Accordance with EIA NEMA Standard RS397, SEC 5 2.2 6 for Conditions of Maximum Rated VDRM, 20V, 20 Ω Gate Trigger Source with 2 μ second Short Circuit Current Rise Time

Figure 7.2b. ASCR-CA358



Blocking Voltage (vert.) $I_A = 10$ ma/div (horiz) $V_{AK} = -300$ v/div

Figure 7.3 Breakover Voltage

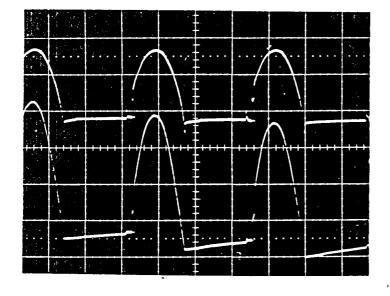


Figure 7.4
Forward Voltage Drop

Forward Voltage Measurement

(top) Anode Current $I_A = 100A/div$

(bot) Anode to Cathode Voltage $V_{AK} = 0.2V/div$

 $t = 5 \, \text{mg/div}$

thyristor but does not appear to be optimized as a true ASCR might be. This becomes obvious by comparing Table 7.1 with Table 7.2. (See last subsection)

The next table listing is the forward voltage drop, from anode to cathode, when 400A is past through the thyristor (see Figure 7.4 for an example test waveform at 200A). These are very good values for low on-state loss and again, indicate the probable use of low levels of "deep level" dopants. The turn-off time, t_{σ} , is listed next. This value indicates the amount of time needed to clear sufficient charge from the thyristor so that the thyristor can immediately block a reapplied forward voltage. The testing was performed at an elevated temperature with test parameters given in Figure 7.1a. These values undesirably exceed the data sheet values by a significant amount. This is a direct result of the fabrication processes referred to earlier when discussing the low values of $I_{\mbox{\footnotesize{DRM}}}$ and $I_{\mbox{\footnotesize{RRM}}}.$ The last two quantities in the table are the "holding" current and "latching" curent usually not found in manufacturer's data sheets. give the lower limit of allowable current during steady-state and turn-on, respectively, to guarantee the device will self-commutate off. These are of little consequence to our immediate evaluation of these devices.

Because of the very poor test results thus far and as concluded below, further testing requiring elaborate set-up, such as, dv/dt was not persued.

7.3 Conclusions and Recommendations.

By all indications these Siemens devices are not Asymmetrical SCRs. Neither the data sheets, Figures 7.1; the test data for I_{DRM} and I_{RRM} , or the oscillograph, Figure 7.3, indicate that these are ASCR's. Also, from Siemens general product catalog these devices are listed for use in both phase control and inverter type application and not optimized for only one application. This is supported by the measurements in Table 7.1 for low V_{GT} , suggesting a non-amplifying gate and low V_{F} suggesting a very low resistivity silicon material composition unlike that found in thyristors optimized for fast switching applications. Of greatest importance is the commutated turn-off time, t_{q} , which far exceeds the data sheet specification of 15 μ s (under the same test conditions).

As a point of comparison, Table 7.2 lists the manufacturer's measurements of an ASCR optimized for fast switching and employing on amplifying gate. The, t_q , rating for this device is the same 15 μ s as the Siemen's device. However, it has a measured value near half, of its rating as to be expected. What suffers in this second device type if the forward on-state voltage drop, V_F , which is approximately 60% higher than the Siemens' device.

To conclude, in inverter drives of substantially high switching frequencies, the switching loss and energy lost to commutation significantly exceeds the on-state conduction loss. Hence, the value, t_{σ} , is most important and Siemens' BStH6140f is

inadequate compared with other types of Asymmetrical SCRs optimized for fast switching such as General Electric's CA358. If, however, a very low switching frequency is to be used, then, the low forward drop of Siemens' BStH6140f is advantageous and should dominate in device selection.

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