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Test Results for 20-GHz GaAs FET Spacecraft Power Amplifier

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TEST RESULTS FOR 20-GHz GaAs FET SPACECRAFT POWER AMPLIFIER

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SUMMARY

Tests were conducted at the NASA Lewis Research Center to measure the performance of the 20-GHz solid-state, proof-of-concept amplifier developed under contract NAS3-22504. The amplifier operates over the 17.7- to 20.2-GHz frequency range and uses high-power gallium arsenide field-effect transistors. This report includes contract performance goals, contractor test results, and NASA test results. The amplifier design and test methods are briefly described. NASA and contractor performance data are compared.

INTRODUCTION

Because of large increases in satellite communications traffic, lower frequency bands allocated to communications use have become saturated with users. To alleviate this problem, NASA is conducting the 30/20-GHz Technology Development program. The program promotes the use of the 27.5- to 30.0-GHz uplink and 17.7- to 20.2-GHz downlink frequency ranges. As a continuation of this project a transponder will be constructed at NASA Lewis to serve as an advanced-technology test base for future satellite communications systems. Certain high-risk system components have been identified and selected for a proof-of-concept (POC) test program. One test component is a high-power, solid-state spacecraft amplifier to operate over the 17.7- to 20.2-GHz frequency range. The successful development of such a device would create an alternative to the free-electron devices that currently dominate spacecraft transmission systems. Critical performance parameters of the amplifier are radiofrequency (rf) output power, power gain, efficiency, voltage standing wave ratio (VSWR), and reliability.

Two parallel contracts were awarded for the development of these amplifiers. This report gives the results of the contract awarded to Texas Instruments, Inc. (TI) of Dallas, Texas. The amplifier was subjected to a series of tests at NASA Lewis, and its performance was recorded and analyzed. Test methods and results are described and discussed herein. Tests include measurement of rf output power, rf gain, 1-dB compression point, VSWR, noise figure, third-order intermodulation, amplitude-modulation-to-phase-modulation (AM/PM) conversion, direct-current-to-rf efficiency, and spurious responses. POC model performance goals are summarized in table I. The TI amplifier and its functional block diagram are shown in figures 1 and 2.

During final testing at the TI facility a major breakdown occurred in the amplifier. Repair of the amplifier required that many of the field-effect transistors (FET's) be replaced and a biasing protection network be added. These modifications returned the amplifier to a working state but significantly altered the rf characteristics. This report will occasionally reference the amplifier rf performance recorded by TI prior to breakdown but will concentrate

on the test results obtained by NASA with the amplifier in its present condition.

DESIGN

The TI amplifier is constructed in a modular design. Radiofrequency signals are amplified by using 16 parallel amplifier modules, each designed for 30 dB of rf gain with a 1/2-W output power level. Each module uses six cascaded gallium arsenide (GaAs) FET's with gate widths ranging from 150 to 1350 μm. The 16 modules are arranged in parallel to guarantee a graceful degradation in output power should failure occur in any module.

Radiofrequency signals are supplied to the modules through a four-stage, 16-way power divider. Four-port waveguide hybrid tees are used in each divider stage to avoid insertion losses normally encountered in microstrip divider circuits. By terminating the E-plane arm of each tee, balanced 16-way power division is obtained from the single input port. All waveguide tees and interconnects are dimensioned as WR-51 for the 15- to 22-GHz frequency range. The contractor estimates insertion losses near 0.6 dB from the divider input port to any output port (in addition to 10 log 16 dividing factor). The output power of the 16 amplifier modules is combined by using a similar structure. This combiner is a duplicate of the input divider and serves the reverse function electrically (i.e., offers balanced, in-phase, 16-way power combination to a single output port). Both manifolds are manufactured from precision aluminum subassemblies.

Each amplifier module consists of three components: the module housing, the waveguide-to-microstrip transitions, and the FET's. The structural component (the module housing) is a machined copper mainframe into which microstrip circuit elements are mounted. The housing includes WR-51 mounting flanges and FET biasing feedthroughs. Each carrier housing is 14 cm (5.6 in) in overall length. A module is shown in figure 3 and its block diagram in figure 4. The second component, the waveguide-to-miscrostrip transitions, are fin-line tapers with a 50-Ω matching balun. Mechanical pressure holds a transition parallel to the E-plane in the housing waveguide channel. Contractor measurements during construction indicated a 0.6-dB loss for back-to-back transitions over the 17.7- to 20.2-GHz range. The active elements contained in each module housing are the six GaAs FET's. Each FET amplifier was first designed and tested individually as a single stage. For this project TI designed and tested a new device (the π-gate FET). This device exhibited significantly better rf performance than the previous multiple-parallel-gate device. A typical π-gate FET is shown in figure 5. Similar FET's, in this design, were fabricated with gate widths of 150, 300, 600, and 1350 μm. Gate lengths ranged from 0.5 to 0.8 μm. Six FET's were then selected on the basis of their power and gain performance and mounted in the waveguide mainframe in a series configuration. The original design used a 2- by 1350-μm parallel FET balanced configuration for the final (sixth) gain stage. This design was later changed to a single 1350 μm FET in all 16 modules. This modification improved each module's resistance to oscillation but sacrificed the output power capability. The present design uses a 150- to 150- to 300- to 600- to 1350- to 1350-μm-gate-width cascaded FET approach. Total gain per module is more than 30 dB with output power typically 150 mW.

After the amplifier failure, voltage regulators were added to each assembly to isolate the FET biasing circuits. This addition reduced the possibility of a damaging transient signal propagating through the entire amplifier. Individual bias control was then available to tune each FET for optimum performance.

The reader is referred to figure 1 for a view of the assembled proof-of-concept amplifier. The 16 amplifier modules, the power divider, the power combiner, and the baseplate are shown. Four voltage regulator cards (one card for each four modules) are mounted on top of the input manifold. WR-51 to WR-42 waveguide transitions are attached at input and output ports to adapt the amplifier to existing laboratory equipment.

The amplifier is cooled conductively through the baseplate or convectively with the aid of a single forced-air cooling fan. The amplifier was designed for complete conductive cooling when it was fastened into its protective steel enclosure. This enclosure, however, severely restricted access to the amplifier and was removed. A steel module support framework conducts thermal energy away from each module. Each thermal path is designed for minimum thermal resistivity between the modules and a thermal reservoir. A single 13-cm (5-in) cooling fan was used to force air past the amplifier for benchtop cooling. A water-cooled heat sink is also a potential cooling method for laboratory conditions.

TEST RESULTS

Output Power and Gain

The rf output power and gain of the assembled amplifier were measured with test equipment configured as shown in figure 6. Automation of the test system permitted rapid, calibrated data acquisition every 50 MHz across the 17.7- to 20.2-GHz band. The amplifier was allowed to thermally stabilize approximately 10 min before any measurements were made (baseplate temperature, 77±1 °F). NASA Lewis tests were performed with a leveled Hewlett-Packard (HP) model 8350 sweep oscillator as the signal source with HP 436A power meters at the amplifier input and output ports. Radiofrequency power was measured through directional couplers. Data were collected by and displayed on a Perkin-Elmer model 3240 computer.

NASA Lewis measured a maximum rf output power of 2.6 W at 18.2 GHz and a minimum of 1 W at the upper edge of the 17.7- to 20.2-GHz band. TI measured a maximum power output of 3 W over the same frequency range. The maximum-output-power-versus-frequency curves of the POC amplifier obtained by NASA and TI are compared in figure 7. A strong similarity of measured values and performance trends is apparent.

NASA Lewis measured an rf power gain of 30.5±1.5 dB at the 1-dB compression point over the full passband. TI measured a gain of 30 dB at the 1-dB compression point. The gain-versus-frequency-response curve measured at NASA Lewis at the 1-dB compression point is shown in figure 8. A maximum gain variation goal of ±0.5 dB over 17.7 to 20.2 GHz was set by NASA. Both NASA Lewis and TI (fig. 7(b)) test results indicated a 3-dB variation. Prior to amplifier breakdown TI recorded a saturated output power level of 8.95 W at

18.6 GHz with a 30-dB gain. These data more closely parallel the design goals of the contract.

1-dB Compression Point

Physically realizable amplifiers characteristically produce a nonlinear gain relation near their maximum rf input drive level. The 1-dB compression point is defined as that point where the amplifier output power level drops 1 dB from the linear relation of input and output powers. Figure 9 displays the compression curve for the 18.2-GHz frequency at which maximum output power was obtained. Input power required for 1-dB compression ranged from -2.5 dBm to 1.2 dBm over the full 2.5-GHz passband. Contractor data gave the 1-dB compression point at 3 dBm across the passband. Representative NASA Lewis data are given in table II. Gain degradation and 1-dB compression point fluctuations (~1 dB) occurred until the amplifier reached nominal operating temperature.

Third-Order Intermodulation Distortion

When the rf drive level to the amplifier was increased beyond the linear gain region (into the saturation region), a distortion of the input signal resulted. If two rf input signals (f_1 and f_2) were used to drive the amplifier, the amplifier nonlinearity produced a set of intermodulation products. The third-order products (IMD_3) had the largest magnitude of the intermodulation output spectrum. The suppression of the third-order products relative to the input signals is a measure of the signal distortion due to the amplifier nonlinearity.

A block diagram of the third-order intermodulation measurement configuration is shown in figure 10. Two signal generators were used to produce the input signals. The two continuous-wave (cw) input signals were summed with a WR-42 waveguide, 3-dB directional coupler. Signal separation of 200 MHz was used to avoid any effects caused by dissimilar gain. The signals were located near the center of the passband. Output signals were measured with a Hewlett-Packard model 8566A spectrum analyzer. Output intermodulation spectra for two input drive levels are shown in figure 11.

As the rf drive level increased into the amplifier saturation region, the intermodulation products increased in amplitude. All input power above that required for saturation was delivered to the intermodulation product signals. At the 1-dB compression point P_0 the IMD_3 signals were more than 14 decibels below the carriers (dBc). At 3 dB below P_0 the IMD_3 suppression was more than 18 dBc. Target performance values were 20 dBc at P_0 and 30 dBc at $P_0/2$.

TI provided no data on third-order intermodulation distortion.

Amplitude-Modulation-to-Phase-Modulation Conversion

In nonideal amplifiers the input signal level as well as the operating frequency will affect the phase relationship of the signal. These level-dependent phase variations are commonly addressed as amplitude-modulation-to-phase-modulation (AM/PM) conversion. For an AM signal demodulated by a phase-insensitive detector, AM/PM conversion is not a problem. For many other modulation schemes, however, phase linearity is important. In a static measurement the signal level into the amplifier is increased in steps, and the difference in phase resulting from the change in input level is measured. The AM/PM conversion coefficient is then expressed in degrees of phase shift per decibel of change in signal level.

The test configuration for AM/PM conversion measurements is shown in figure 12. An HP 8409 automatic network analyzer (ANA) was used for all phase measurements. Calibrated amplitude and phase angle data were collected and stored for 28 frequencies across the amplifier passband. An Avantek model 8352 preamplifier was used to supply the large input power range needed for amplitude modulation. Attenuators were placed in the system to keep signal strengths within amplifier and preamplifier damage and ANA sensitivity limits. An HP K382A rotary-vane attenuator served as the input amplitude modulator for the test. Input signal amplitude was varied from -9.5 to 2.5 dBm in 2-dB increments. Output power and phase were recorded automatically for each frequency. Contract goals specified a 3-deg/dB phase shift above the 1-dB compression point P_0 and 2 deg/dB below. NASA Lewis tests indicated the amplifier produced a maximum shift of 3.5 deg/dB at P_0 and 2.6 deg/dB at P_0 - 2 dB. Worst-case AM/PM conversion factors are presented in table III.

The mechanical design of the amplifier precluded the measurement of the AM/PM characteristics of the individual amplifier modules. Had such testing been convenient, the data would have been used to assess the overall performance of the amplifier. TI provided no data on AM/PM conversion.

Group Delay

The group delay of an amplifier is an equivalent way of describing the amplifier's deviation from linear phase. Group delay is defined as the derivative of the phase response with respect to frequency,

$$t_g = -\frac{d\varphi}{d\omega} \tag{1}$$

In this way the group delay is calculated as the slope of the phase response curve. A linear phase response would have a constant slope and thus a constant group delay. Amplifier design goals would then tend toward minimum group delay variation (in addition to a minimum absolute value). Group delay is also commonly thought of as the time required for the input signal to propagate through the amplifier from input to output (ref. 1).

The group delay performance of the amplifier is shown in figure 13. Data were recorded with the automatic network analyzer configured for the AM/PM test. Standard ANA software enabled the group delay values to be calculated from measured phase data. The performance goal for this test was a variation of less than 0.5-ns delay over any 500-MHz band. NASA Lewis measured a maximum

of 1.4-ns variation over 500 MHz. Peak delays occurred at 17.70 and 20.14 GHz with maximum deviations occurring between 17.70 and 17.98 GHz. TI provided no data on group delay.

Voltage Standing Wave Ratio

The input VSWR of the TI amplifier was measured by using the reflectometer configuration shown in figure 14. This test determined the quality of the impedance match of the amplifier to other devices in the system. The method records the incident and reflected power levels from a given test port. The return loss of the device is then used to make a direct translation to VSWR. A perfect impedance match allows all incident power to be delivered to the device and corresponds to a VSWR of 1. A waveguide short was used at the test port (reference plane) during calibration to force a zero return-loss condition. A precision rotary-vane attenuator was then used to impose a calibrated return loss.

Input VSWR data are presented in table IV for several frequencies at the 1-dB compression point. Contract goals list a maximum ratio of 1.4. NASA recorded VSWR's exceeding 2.50 at the lower band edge. Varying the input power had minimal effect on return loss. Similar data were obtained during ANA tests. TI supplied no VSWR data for the rebuilt amplifier. Return-loss data recorded by TI prior to amplifier breakdown yielded a maximum input VSWR of 2.45 near 18.2 and 18.9 GHz.

Noise Figure

The noise figure of a component is defined as the ratio of the signal-to-noise ratio at the input port to the signal-to-noise ratio at the output port. Ideally the noise figure of the component equals 1, indicating that 0 dB of noise is added to the system. In this way the noise figure serves as a figure of merit for a device such as an amplifier.

The noise figure test configuration is shown in the block diagram in figure 15. The measurement is made with an HP 8970A noise figure meter. The meter is limited by a 1500-MHz maximum input frequency. Therefore a mixer and a local oscillator (LO) were used to translate the amplifier output to frequencies within the noise meter limits. An HP 8350 sweep oscillator served as an adjustable LO. An HP 9845 desktop computer was used to control all testing. An Ailtech model 07053 gas tube noise source (excess noise ratio (ENR) = 16.15±0.25 dB) was used to inject excess noise into the amplifier input. The Y-factor measurement technique is described in figure 16 (ref. 3).

Table V lists NASA Lewis noise figures measured at several points within the 2.5-GHz band. Results ranged from a maximum of 19.3 dB at the upper band edge to a minimum of 14.8 dB near 18.8 GHz. These measurements clearly met the 25-dB maximum noise figure performance requirement. TI provided no data for the noise figure of the amplifier.

Spurious Responses

The output spectrum of the TI amplifier was monitored with an HP model 8566A spectrum analyzer. A typical plot of the saturated output generated by an 18.9-GHz cw signal is shown in figure 17. A single cw rf input signal (+0 dBm) was swept across the passband of the amplifier. No spurious signals were generated by the amplifier above the -60-dBm spectrum analyzer noise floor. The step in the trace resulted from a filter change within the analyzer and is not a function of the device under test. The spurious response of the amplifier is therefore above the 60-dBc performance requirement.

Removing the carrier input did not affect the generation of spurious signals. No spurious responses were visible across the 2.5-GHz band. This test confirmed that FET oscillations, if any, have been suppressed sufficiently to provide a clean amplification environment.

dc-to-rf Efficiency

The power-added efficiency of the amplifier was measured by using the configuration shown in figure 18. Standard digital multimeters were used to measure voltages and currents supplied to the gate and drain bias ports. The overall power-added efficiency η (in percent) was calculated as

$$\eta = \frac{(\text{rf power out}) - (\text{rf power in})}{(\text{dc power in})} \times 100 \qquad (2)$$

The bias values are listed in table VI for the thermally stabilized amplifier. The overall efficiency was calculated to be 2.5 percent. The overall efficiency goal was 20 percent.

Power losses in the bias voltage regulators are included in the 2.5 percent efficiency figure. Ideally a set of test points would be located between the regulators and the FET's. This would permit the determination of FET module power consumption alone and would be a more accurate measure of performance. Regulator losses cannot be accurately estimated at this time. TI recorded module efficiencies of the order of 15 percent for the original amplifier.

CONCLUDING REMARKS

Analysis of test data has demonstrated the feasibility of a high-performance, solid-state 20-GHz power amplifier. State-of-the-art technology indicates that gallium arsenide field effect transistors (FET's) are moving closer to meeting the requirements of a space-qualifiable amplifier. Contract performance goals for radiofrequency (rf), gain, noise figure, amplitude-modulation-to-phase-modulation conversion, and spurious response were realized. Other parameters, such as power output, voltage standing wave ratio and direct-current-to-rf efficiency, did not meet contract specifications. One of the intents of proof-of-concept contracts is to assess the level of present-day technologies. This contract has helped to accomplish that task. It is expected that continued effort will enhance the TI amplifier significantly. Data are summarized in table VII.

Many of the poor performance characteristics of the amplifier are a result of the failure that occurred during contractor testing. Monetary and scheduling constraints forced TI to perform rapid repair and reassembly. To accomplish this, a variety of devices from several different yields were mixed. Phase variations and impedance mismatches in these devices undoubtedly contributed to the degradation in rf performance, particularly output power.

Many problems plaguing the TI amplifier could be resolved through continued effort. The amplifier output power level could be raised significantly through the use of higher-power FET's in either single stage or balanced configurations. Ongoing efforts in the design and fabrication of FET's have already demonstrated device enhancements. Devices fabricated more recently, both commercially and under similar contracts, have consistently yielded a 1-W output power level, 4-dB rf power gain, and a 22-percent power-added efficiency. The increase in rf output could improve several amplifier performance characteristics, including third-order intermodulation distortion, harmonic suppression, spurious response suppression, and dc-to-rf efficiency.

The dc-to-rf efficiency is routinely low in solid-state amplifiers. Continued efforts in this area are yielding major improvements as GaAs FET technologies develop. A second-generation amplifier should exhibit vastly improved performance characteristics.

RECOMMENDATIONS

Day-to-day improvements in manufacturing techniques will undoubtedly enhance FET performance. Data suggest the need for continued effort in this area in order to obtain more powerful and efficient FET's.

It is recommended that future proof-of-concept amplifiers incorporate a set of test points between the voltage regulators and the FET's. This would permit accurate measurement of the power consumption and other parameters of the amplifier modules. This modification would also assist the test engineer in troubleshooting the amplifier through the ability to isolate damaged FET's.

Improvements in impedance matching would augment the dc-to-rf efficiency performance of the amplifier. This would then optimize the power transfer to the amplifier input and from the amplifier output to other system components.

The 16-way power combiner/divider manifolds serve as a strong mainframe for the mechanical support of the amplifier modules. The precision machining of the manifolds also ensures that waveguide flanges are properly mated. This design does, however, eliminate the possibility of phase matching all 16 of the modules through the use of shims. A common shimming technique places shims of calculated thickness in the waveguide segments of a typical amplifier branch. This action increases the electrical length of that branch and causes an additional phase delay. Careful selection of shims allows all modules to be phase matched to maximize the power output capability of the overall amplifier. An alternative matching technique uses microstrip delay lines. Each delay line must then be custom fitted to the phase mismatch of each module. This amplifier does not use either technique.

It is recommended that a radial power combiner/divider structure be used. A radial orientation would facilitate phase matching of the modules by permitting a given branch to be shimmed outward in a radial direction. The radial combiner/divider technique also makes each module more accessible for individual repair or testing.

REFERENCES

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2. Saunier, P.; and Nelson, S.: 30/20 GHz Spacecraft GaAs FET Solid State Transmitter for Trunking and Customer-Premise-Service Application. (TI-08-83-42, Texas Instruments; NASA Contract NAS3-22504), NASA CR-168276, 1983.

3. Adam, Stephen F: Microwave Theory and Applications. Prentice-Hall, 1969, pp. 490-499.

TABLE I. - PERFORMANCE GOALS

Radiofrequency output power, W	6.0-.7.5
Operating frequency range, GHz	17.7-20.2
Radiofrequency power gain, dB	30
Third-data intermodulation distortion, dBc:	
At P_0[a]	20
At $P_0/2$	30
AM/PM conversion, deg/dB:	
Above P_0	3
Below P_0	2
Group delay variation per 0.5 GHz, ns	0.5
Input voltage standing wave ratio	1.4
Noise figure, dB	25
Harmonic suppression, dBc	30
Spurious signal suppression, dBc	60
Direction-current-to-radiofrequency efficiency, percent	20

[a] P_0 refers to input power required for 1-dB compression.

TABLE II. - INPUT POWER AT 1-dB COMPRESSION POINT (NASA)

Frequency, GHz	Compression-point input power, dBm
18.0	0
18.5	1.2
19.0	.4
19.5	-2.5
20.0	-1.4

TABLE III. - MAXIMUM AM/PM CONVERSION FACTORS (NASA)

Input power level, dBm	Maximum AM/PM conversion factor, deg/dB
-9.5 to -7.5	-2.0
-7.5 to -5.5	-2.5
-5.5 to -3.5	-2.0
-3.5 to -1.5	-2.6
[a]-1.5 to 0.5	-3.5
0.5 to 1.5	-2.2
1.5 to 2.5	-2.2

[a]1-dB compression point.

TABLE IV. - INPUT VOLTAGE STANDING WAVE RATIOS (NASA)

Frequency, GHz	Voltage standing wave ratio
17.7	2.50
18.0	1.98
18.5	1.94
19.0	1.10
19.5	1.54
20.0	1.34
20.2	1.37

TABLE V. - NOISE FIGURES

(NASA)

Frequency, GHz	Noise figure, dB
17.7	15.9
18.0	15.2
18.5	14.8
19.0	15.5
19.5	15.7
20.0	17.2
20.2	19.3

TABLE VI. - AMPLIFIER BIAS VALUES (NASA)

	Voltage, V dc	Current, A
Gate	-5.5	1.07
Drain	10.5	9.1

TABLE VII. - PERFORMANCE SUMMARY

Parameter	Goal	NASA results	TI results
Radiofrequency output power, W	6.0-7.5	2	3
Operating frequency, GHz	17.7-20.2	17.7-20.2	17.5-20.2
Radiofrequency power gain, dB	30	31	30
Third-order intermodulation distortion, dBc:			
At P_0	20	14	----------
At $P_0/2$	30	18	----------
AM/PM conversion, deg/dB:			
Above P_0	3	3.5	----------
Below P_0	2	2.6	----------
Group delay variation per 0.5 GHz, ns	0.5	1.4	----------
Input voltage standing wave ratio	1.4	2.5	2.45
Noise figure, dB	25	19.3	----------
Harmonic suppression, dBc	30	>60	----------
Spurious signal suppression, dBc	60	>60	----------
Direct-current-to-radiofrequency efficiency, percent	20	2.5	----------

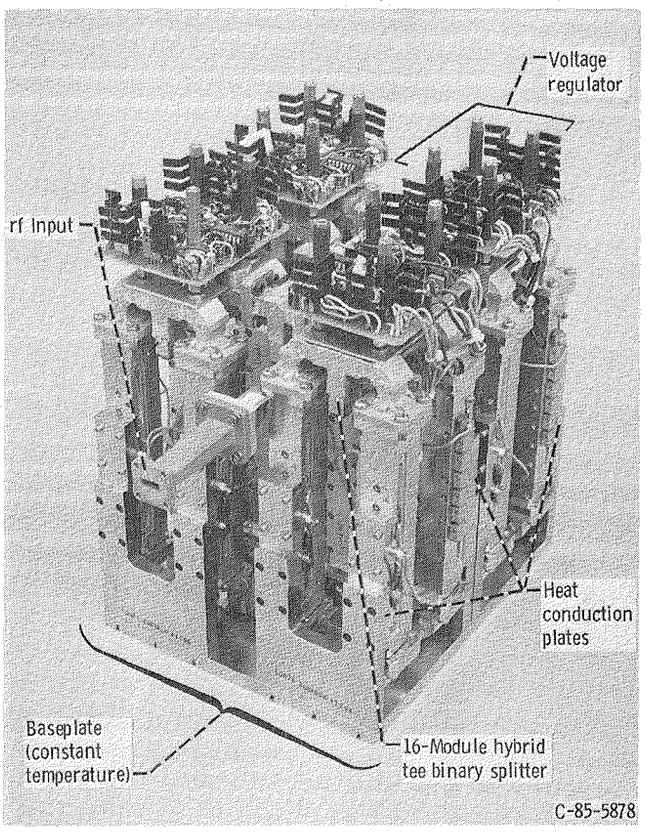


Figure 1. - 20-GHz GaAs FET amplifier - proof-of-concept model.

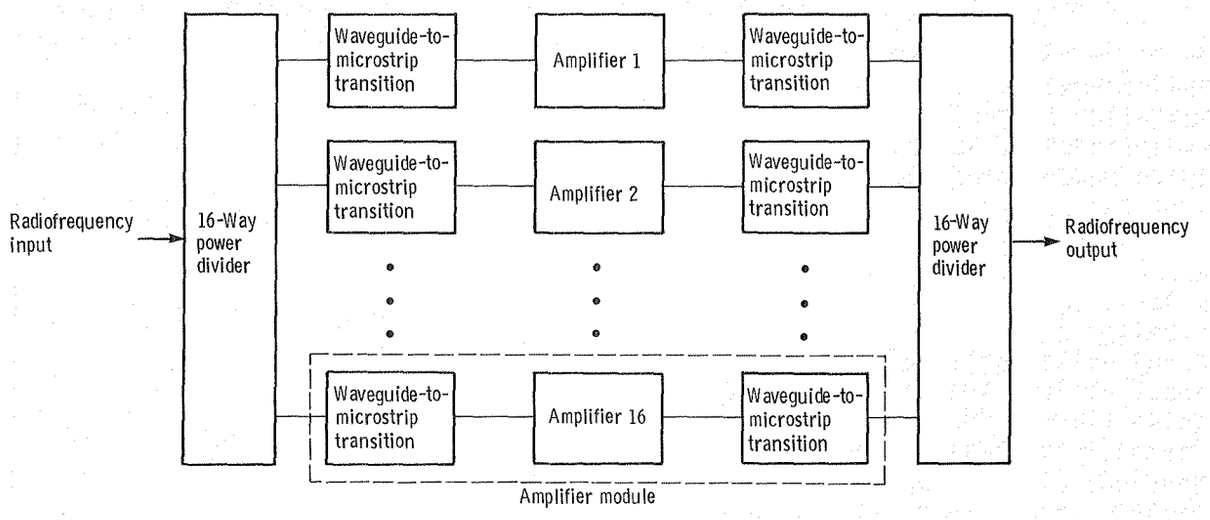


Figure 2. - Functional block diagram of amplifier.

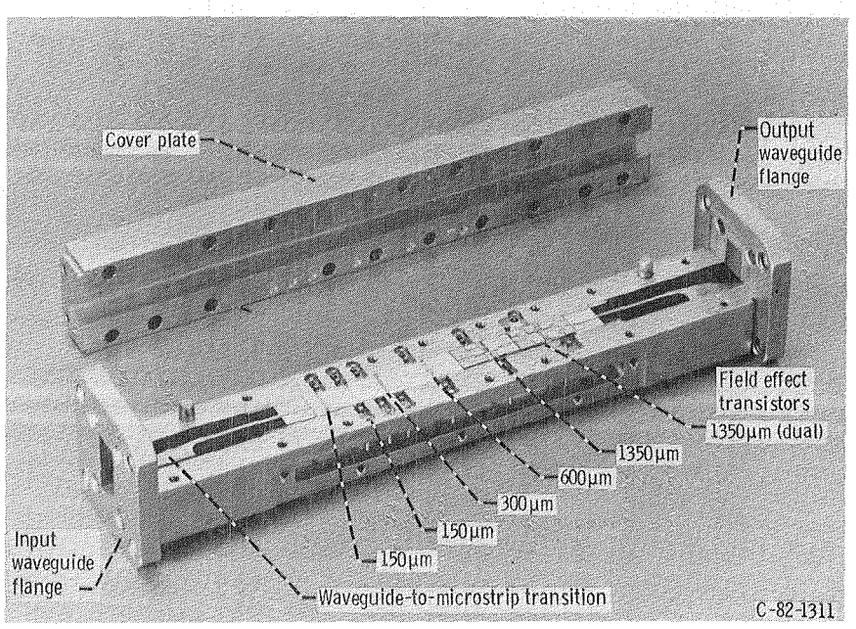


Figure 3. - Six-stage gain module for 20-GHz GaAs FET amplifier.

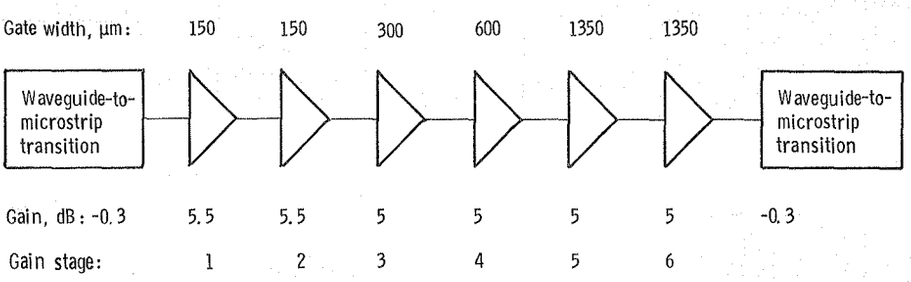


Figure 4. - Functional block diagram and gain budget for amplifier module.

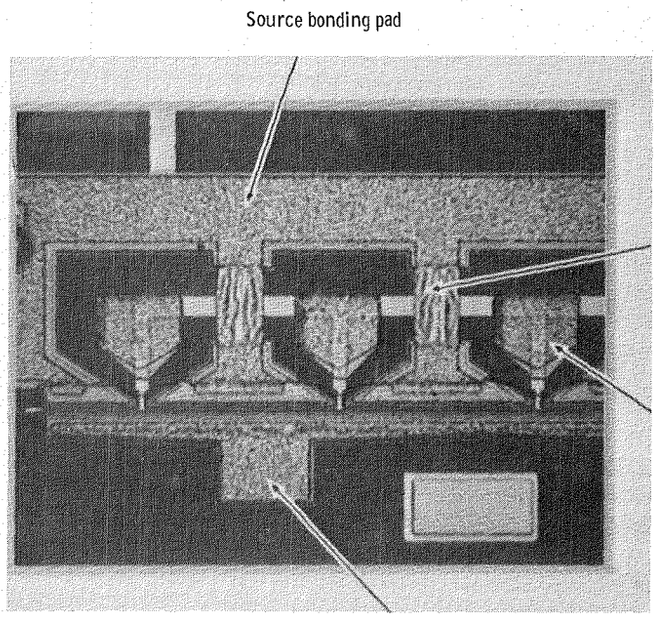


Figure 5. - GaAs π-gate power FET.

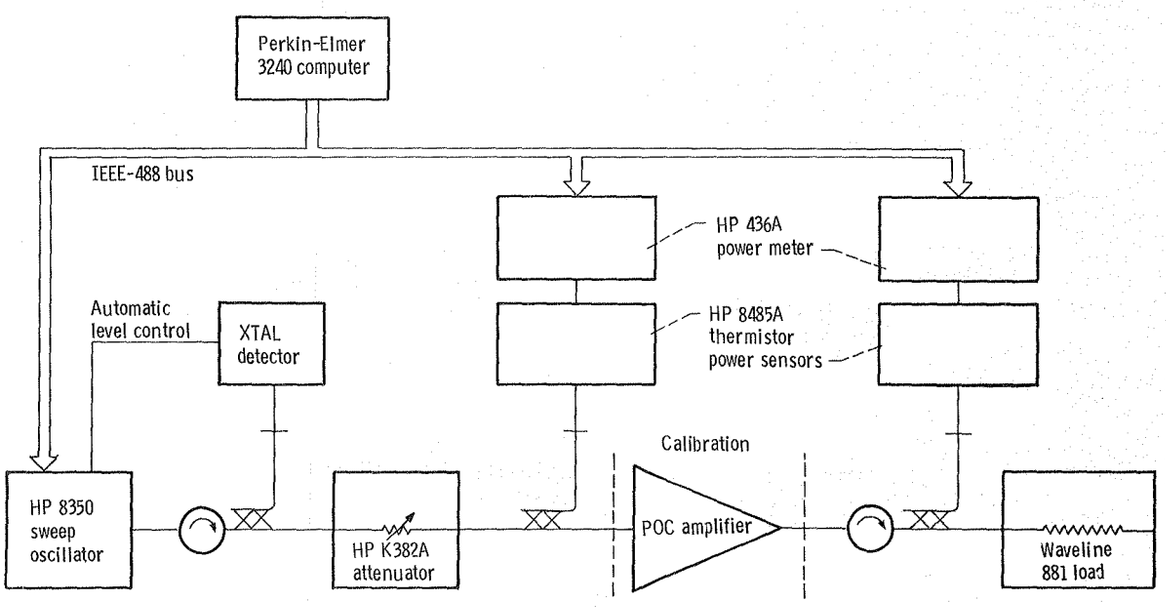
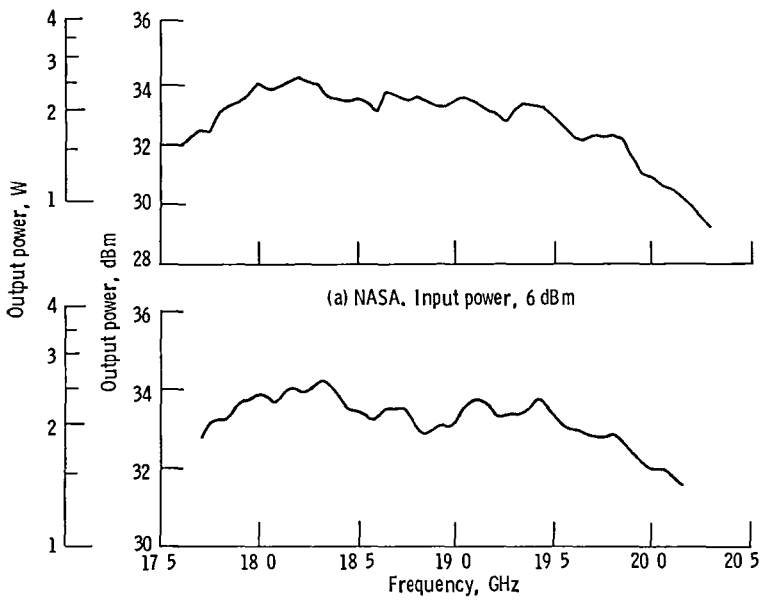


Figure 6. - Radiofrequency power and gain measurement configuration.



(a) NASA. Input power, 6 dBm

(b) Texas Instruments Input power, 5 dBm

Figure 7. - Output power characteristics

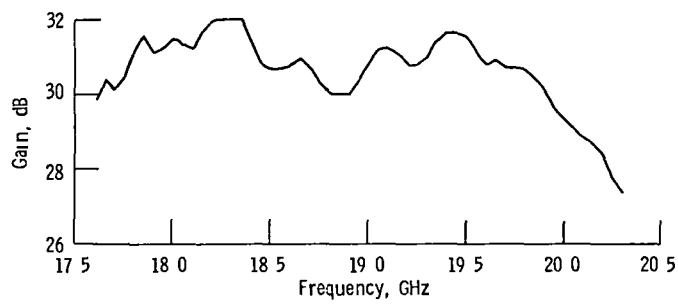


Figure 8 - Gain characteristic at 1-dB compression point (NASA)

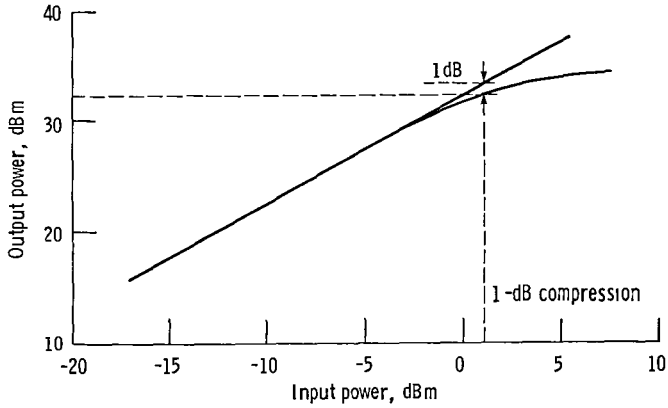


Figure 9 - Compression characteristic at 18 2 GHz (NASA)

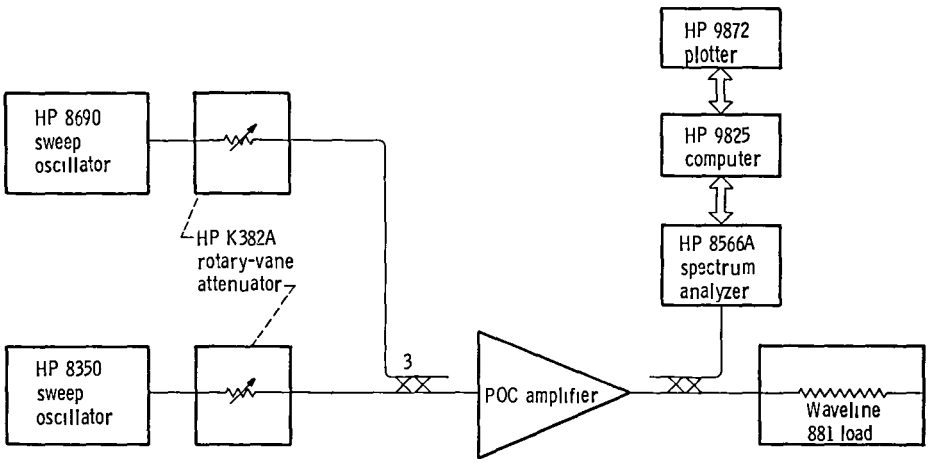
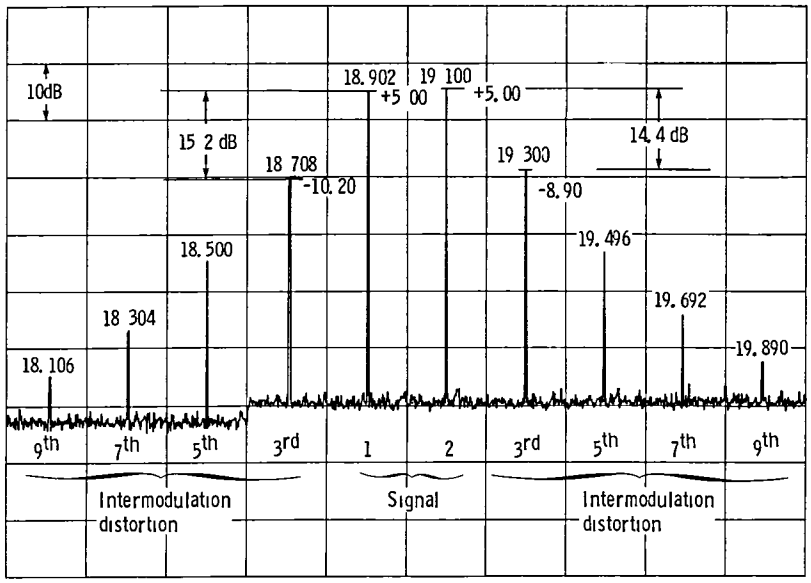
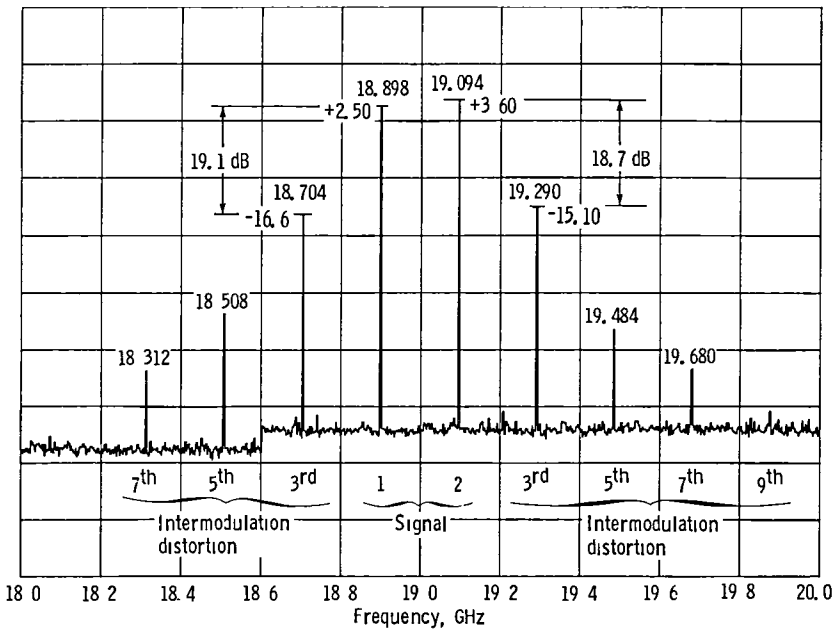


Figure 10. - Third-order intermodulation test configuration



(a) 1-dB compression point. Resolution bandwidth, 30 kHz, video bandwidth, 100 kHz, sweep time, 6 sec



(b) 3-dB below 1-dB compression point. Resolution bandwidth, 10 kHz, video bandwidth, 30 kHz, sweep time, 60 sec.

Figure 11 - Third-order intermodulation distortion spectra (NASA).

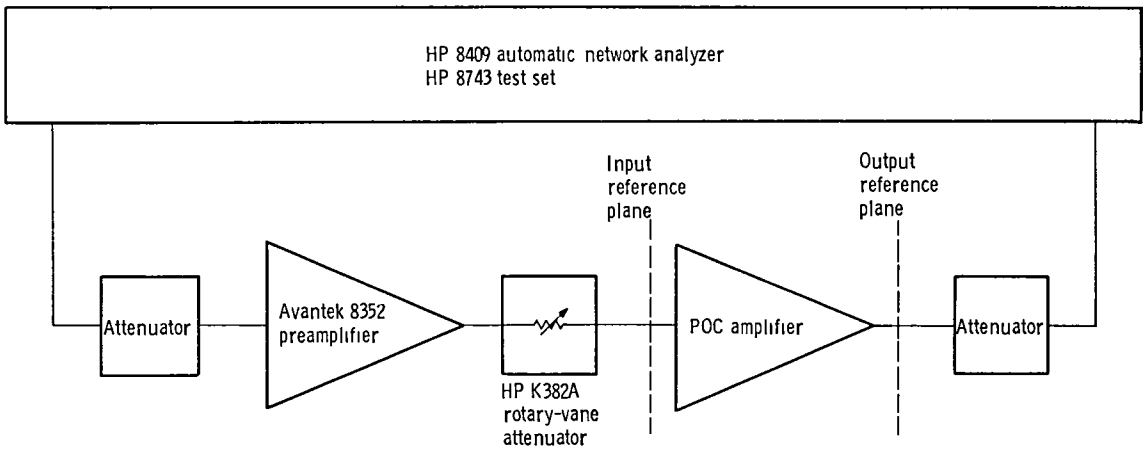


Figure 12 - AM/PM conversion test configuration

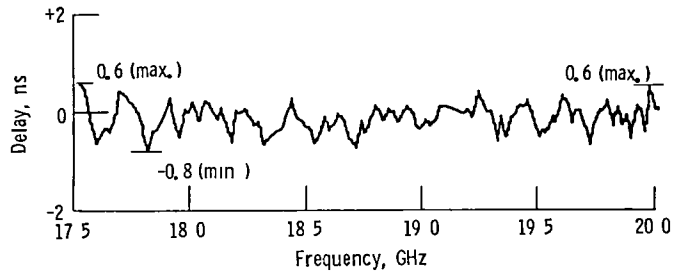


Figure 13 - Group delay variation (NASA)

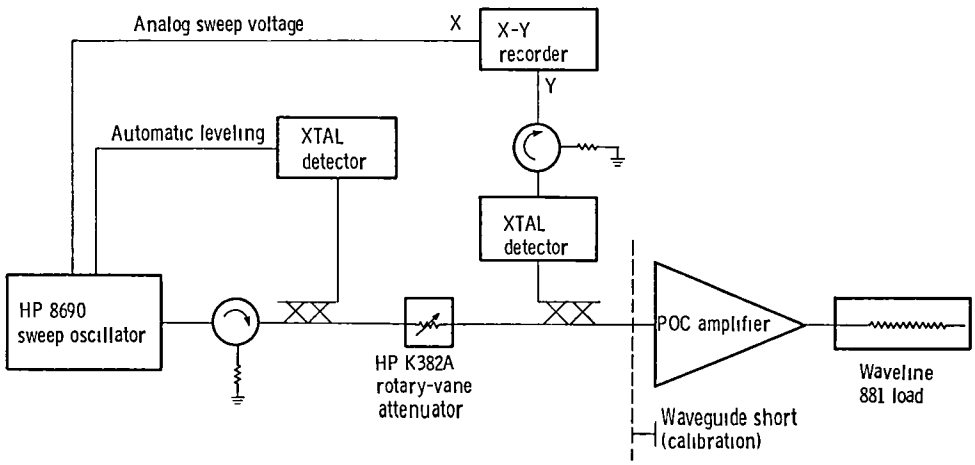


Figure 14 - Reflectometer configuration

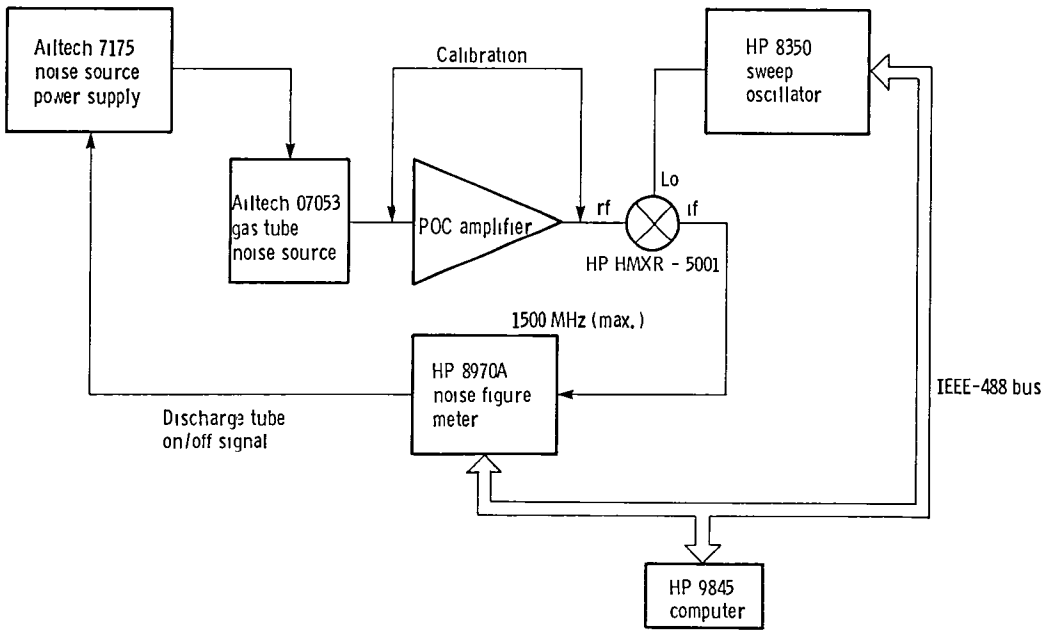


Figure 15 - Noise figure test configuration

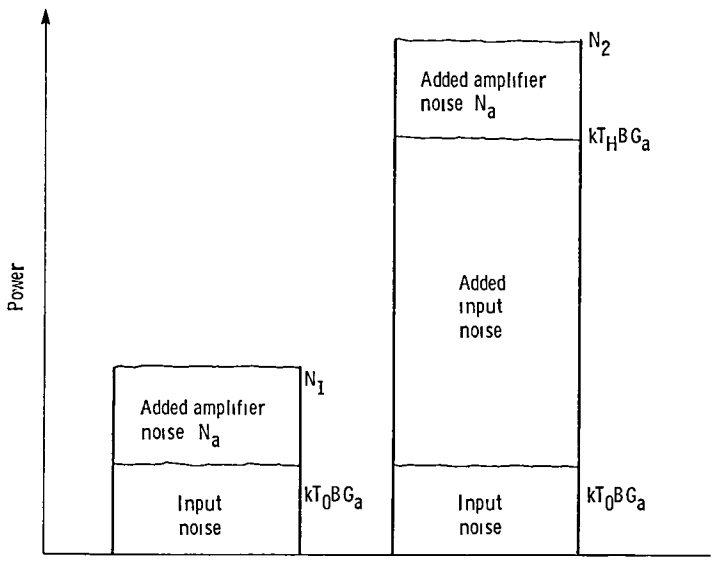


Figure 16 - Y-factor measurement technique. NF = ENR - 10 log (Y - 1), $Y = N_2/N_1$, ENR = 10 log $(T_H - T_0)/T_0$ where K = Boltzmann's constant (1.38×10^{-23} J/K), B = bandwidth, G_a = amplifier gain, and T_H, T_0 = temperature of source resistance (on, off).

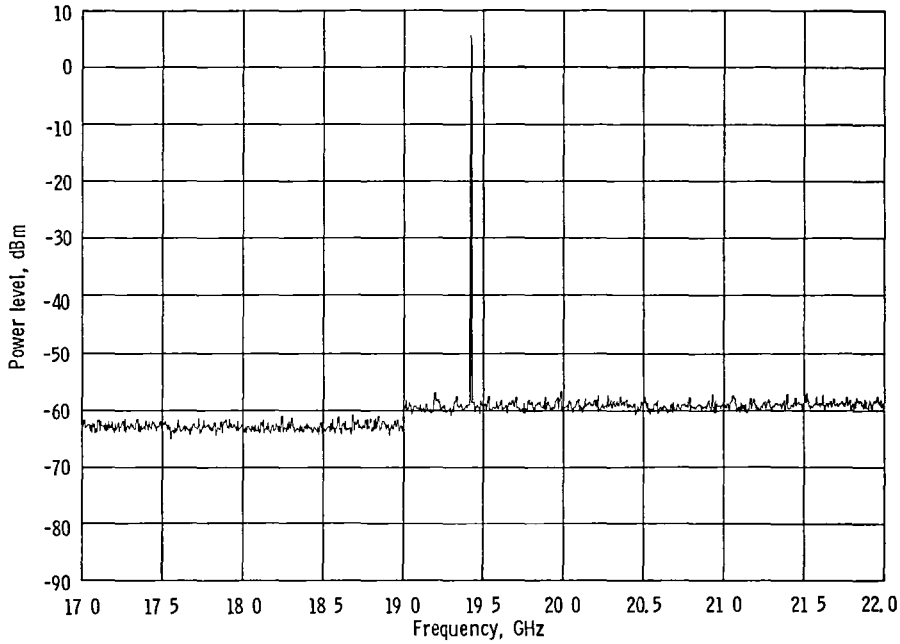


Figure 17 - Spurious signal suppression (NASA) Input attenuation, 20 dB, resolution bandwidth, 30 kHz, video bandwidth, 100 kHz, sweep time, 12 sec

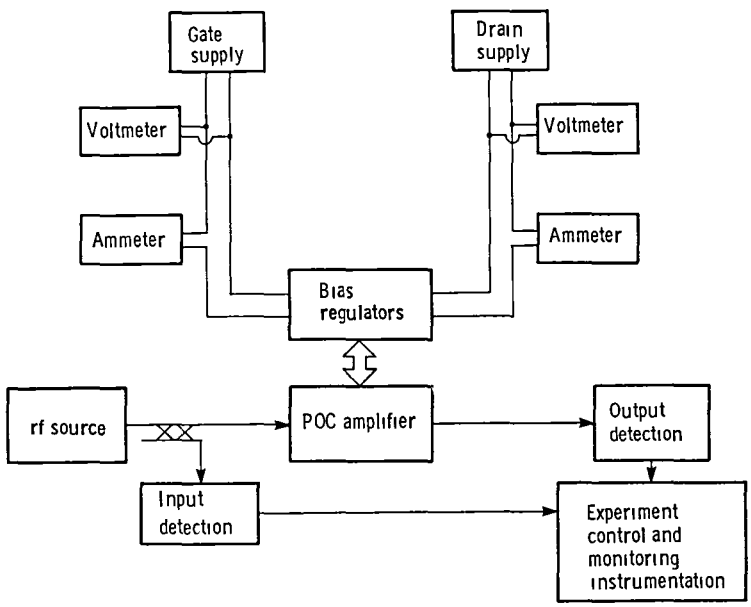


Figure 18 - Block diagram of direct-current-to-radiofrequency efficiency measurement.

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15 Supplementary Notes

16 Abstract

Tests were conducted at the NASA Lewis Research Center to measure the performance of the 20-GHz solid-state, proof-of-concept amplifier developed under contract NAS3-22504. The amplifier operates over the 17.7- to 20.2-GHz frequency range and uses high-power gallium arsenide field-effect transistors. This report includes contract performance goals, contractor test results, and NASA test results. The amplifier design and test methods are briefly described. NASA and contractor performance data are compared.

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