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# Reliability and Engineering of Thin-Film Photovoltaic Modules

## Research Forum Proceedings

Edited by:

R.G. Ross
E.L. Royal




October 1 1985

Prepared for
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Jet Propulsion Laboratory
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Pasadena, California

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16. Abstract

A Research Forum on Reliability and Engineering of Thin-Film Photovoltaic Modules, under sponsorship of the Jet Propulsion Laboratory's Flat-Plate Solar Array (FSA) Project and the U.S. Department of Energy, was held in Washington, D.C., on March 20, 1985. Reliability-attribute investigations of amorphous-silicon cells, submodules, and modules were the subjects addressed by most of the Forum presentations. Included among the reliability research investigations reported were: Arrhenius-modeled accelerated stress tests on a-Si cells, electrochemical corrosion, light-induced effects and their potential effects on stability and reliability measurement methods, laser-scribing considerations, and determination of degradation rates and mechanisms from both laboratory and outdoor exposure tests.

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## ABSTRACT

A Research Forum on Reliability and Engineering of Thin-Film Photovoltaic Modules, under sponsorship of the Jet Propulsion Laboratory's Flat-Plate Solar Array (FSA) Project and the U.S. Department of Energy, was held in Washington, D.C., on March 20, 1985. Reliability-attribute investigations of amorphous-silicon cells, submodules, and modules were the subjects addressed by most of the Forum presentations. Included among the reliability research investigations reported were: Arrhenius-modeled accelerated stress tests on a-Si cells, electrochemical corrosion, light-induced effects and their potential effects on stability and reliability measurement methods, laser-scribing considerations, and determination of degradation rates and mechanisms from both laboratory and outdoor exposure tests.

## KEY WORDS

Activation energy, annealing, Arrnenius, degradation mechanisms, electrochemical corrosion, reference cells, Staebler-Wronski Effect, step-stress testing, stability, tandem cells, Tedlar, transparent conductive oxide, and voltage isolation.

## FOREWORD

As part of the U.S. Department of Energy (DOE) National Photovoltaics Program, the Jet Propulsion Laboratory (JPL) Flat-Plate Solar Array Project (FSA) manages research that includes developing the technology base required to achieve 30-year life for flat-plate photovoltaic (PV) modules. In coordination with the Solar Energy Research Institute (SERI), a portion of this JPL activity is focused on achieving the technology base required for thin-film modules, specifically amorphous silicon (a-Si) modules, which has attained a high level of maturity under SERI's cognizance.

The purpose of the Research Forum was to: (1) examine critically the attributes of thin-film cells that influence module performance and reliability, (2) explore the lessons and applicability of crystalline-Si module technology to thin-film modules, (3) review the current status of thin-film module technologies, and (4) identify problem areas and needed research. Another important objective was to accelerate the sharing of technical experience between solid-state device researchers and engineering reliability researchers. Forum arrangements were designed to encourage interaction and exchange of information among the wide range of researchers who attended.

The keynote address, presented by Dr. Charles Gay, Vice President, Reasearch and Development, ARCO Solar, Inc., was titled "The Need for Thin-Film Reliability Research." In this address, Dr. Gay praised the work of JPL for its reliability research support as a key factor in the success of crystalline-silicon technology. He urged that a similar type and level of support be committed for thin-film cell and module reliability research. Dr. Gay gave equal praise to SERI as a developing center of excellence in basic research studies and measurements. In addition to papers presented, two domestic private-industry photovoltaic companies used the Research Forum to announce new a-Si mudule designs. Both modules were shown and each was described in considerable technical detail.

These Proceedings contain the papers presented and visual materials used by Reasearch Forum participants. In addition, much of the informal discussions, questions, and answers which followed each presentation are included, edited for clarity and brevity.

R. G. Ross, Chairman
E. L. Royal, Cochairman

PROGRAM

RESEARCH FORUM: RELIABILITY AND ENGINEERING OF THIN-FILM PHOTOVOLTAIC MODULES

DATE: March 20, 1985
Washington, D.C.

KEYNOTE ADDRESS: The Need for Thin-Film Reliability Research
Speaker, C. Gay, Vice President, ARCO Solar, Inc

TECHNICAL SESSIONS

SESSION I CELL AND SYSTEM CHARACTERISTICS AFFECTING MODULE DESIGN (L. Herwig, U.S. Department of Energy Headquarters, Chairman)

SESSION II THIN-FILM MODULE DEVELOPMENTS WITHIN U.S. COMPANIES (E. Royal, Jet Propulsion Laboratory, Chairman)

SESSION III RELIABILITY RESEARCH AND PERFORMANCE INVESTIGATIONS (R. Ross, Jet Propulsion Laboratory, Chairman)

Attendees: 68

Papers: 15

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THIN-FILM MODULE DESIGN DEVELOPMENTS
(E. L. Royal, Jet Propulsion Laboratory, Chairman)



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RELIABILITY RESEARCH AND PERFORMANCE INVESTIGATIONS
(R. G. Ross, Jet Propulsion Laboratory, Chairman)

# FORUM INTRODUCTION ADDRESS

R. Ross
(Jet Propulsion Laboratory)

N86-12760

# CRYSTALLINE-SILICON RELIABILITY LESSONS FOR THIN-FILM MODULES

Ronald G. Ross, Jr.
Jet Propulsion Laboratory
Pasadena, California 91109

## Introduction

During the past 10 years the reliability of crystalline-silicon modules has been brought to a high level with lifetimes approaching 20 years, and excellent industry credibility and user satisfaction. With the emergence of thin-film power modules it is important to review the lessons learned from the crystalline-Si product development history and apply the technology base, where applicable, to enhance the development of thin-film modules.

The transition from crystalline modules to thin-film modules is comparable to the transition from discrete transistors to integrated circuits. New cell materials and monolithic structures will require new device processing techniques, but the package function and design will evolve to a lesser extent. Although there will be new encapsulants optimized to take advantage of the mechanical flexibility and low-temperature processing features of thin-films, the reliability and life-degradation stresses and mechanisms will remain mostly unchanged. Key reliability technologies in common between crystalline and thin-film modules include hot-spot heating, galvanic and electrochemical corrosion, hail-impact stresses, glass breakage, mechanical fatigue, photothermal degradation of encapsulants, operating temperature, moisture sorption, circuit design strategies, product safety issues, and the process required to achieve a reliable product from a laboratory prototype.

## Crystalline-Si Research Objective and Approach

Before examining the lessons learned from the crystalline-Si module development effort it is instructive to review briefly its objective and approach.

Increased array life and reliability directly influence the economic viability of photovoltaics as an energy source by controlling the total number and size of revenue payments received from future sales of electricity. After considerations of present value discounting and escalation of the worth of electricity in future years, a 30-year PV plant, for example, is worth 25 to 30 percent more than a 20-year-life plant. Based on this economic sensitivity to plant life, a 30-year life was chosen as the target of the crystalline-Si module development effort (Fig. 1) (1).

To achieve this high level of reliability a systematic reliability program (Fig. 2) was undertaken in 1975 by the Jet Propulsion Laboratory Flat-Plate Solar Array Project to develop the technology base required (2). Figure 3 lists the principal failure mechanisms for crystalline-Si modules and notes the economic importance of each and the target allocation level for each which is consistant with achieving a 30-year life (3). The next three figures illustrate the history of occurance of crystalline-Si field reliability problems and the research developments over the past 10 years which have led to the present high reliability of crystalline-Si modules.

## Lessons Learned

The remainder of the figures systematically summarize the key reliability lessons learned from the 10-year crystalline-Si module development effort. For convenience the lessons are subdivided into five topic areas:

- o Module Reliability Lessons
- o Reliability Research Lessons
- o Module Qualification Experience
- o Qualification Test Experience
- o Field Test Experience

## Conclusions

An important lesson from the crystalline program (and the nuclear program) is that honest conscientious working of reliability and safety issues can significantly affect the economic viability and public acceptance of the product. Resolving the issues is not cheap, and cannot be accomplished overnight. For example, it still takes approximately 2 years from initial product design to successful passing of product qualification specifications for a crystalline-Si module.

As with your family car, initial cost and efficiency are directly measurable; lifetime and reliability are the greatest areas of user risk and play a key role in purchase decisions.

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Figure 1. Crystalline-Silicon Reliability Objective

**To achieve the technology base for 30-year array life**

- **Acceptable power degradation rates**
- **Acceptable component failure rates**
- **Acceptable maintenance costs**

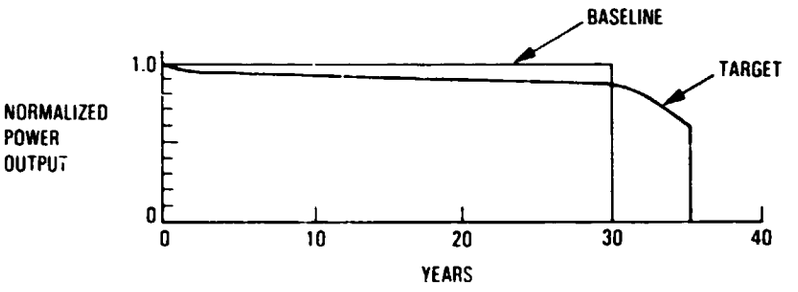


Figure 2. Reliability Research Elements

- **Establishment of mechanism-specific reliability goals**
  - **Identification of key degradation mechanisms**
  - **Determination of system energy-cost impacts**
  - **Allocation of system-level reliability**
- **Quantification of mechanism parameter dependencies**
  - **Governing materials parameters**
  - **Governing environmental-stress parameters**
  - **Qualitative understanding of mechanism physics**
- **Development of degradation prediction methods**
  - **Quantitative accelerated tests**
  - **Life-prediction models**
- **Identification of cost-effective solutions**
  - **Component design features**
  - **Circuit redundancy and reliability features**
- **Testing and failure analysis of trial solutions**

Figure 3. Life-Cycle Cost Impacts and Allowable Degradation Levels

| Type of Degradation | Failure Mechanism | Units of Degrad. | Level for 10% Energy Cost Increase* | | Allocation for 30-Year Life Module | Economic Penalty |
|---|---|---|---|---|---|---|
| | | | k = 0 | k = 10 | | |
| Component failures | Open-circuit cracked cells | %/yr | 0.08 | 0.13 | 0.005 | Energy |
| | Short-circuit cells | %/yr | 0.24 | 0.40 | 0.050 | Energy |
| | Interconnect open circuits | $\%/yr^2$ | 0.05 | 0.25 | 0.001 | Energy |
| Power degradation | Cell gradual power loss | %/yr | 0.67 | 1.15 | 0.20 | Energy |
| | Module optical degradation | %/yr | 0.67 | 1.15 | 0.20 | Energy |
| | Front surface soiling | % | 10 | 10 | 3 | Energy |
| Module failures | Module glass breakage | %/yr | 0.33 | 1.18 | 0.1 | O&M |
| | Module open circuits | %/yr | 0.33 | 1.18 | 0.1 | O&M |
| | Module hot-spot failures | %/yr | 0.33 | 1.18 | 0.1 | O&M |
| | Bypass diode failures | %/yr | 0.70 | 2.40 | 0.05 | O&M |
| | Module shorts to ground | $\%/yr^2$ | 0.022 | 0.122 | 0.01 | O&M |
| | Module delamination | $\%/yr^2$ | 0.022 | 0.122 | 0.01 | O&M |
| Life-limiting wearout | Encapsulant failure due to loss of stabilizers | Years of life | 27 | 20 | 35 | End of life |

*k = Discount rate

Figure 4. Module Reliability Lessons

- Most module reliability problems are related to the encapsulant system
  - Soiling
  - Cracking
  - Yellowing
  - Delaminating
  - Accelerated corrosion
  - Voltage breakdown
  - Laminating (processing) stresses
  - Differential expansion stresses
- Primary function of encapsulant is structural support and electrical isolation for safety reasons. The secret is to perform these functions while not degrading the intrinsic reliability of the cells themselves
- Second most frequent module reliability problems are related to circuit integrity
  - Fatigue due to differential expansion stresses
  - Poor solder joints
- Crystalline-Si cell reliability problems are most often related to cell cracking, metallization adherence/series resistance and durability of anti-reflective coatings

## Figure 5. Reliability Research Lessons

- **Failure mechanisms fall into two broad classes: generic and statistical. Generic problems must be solved by design or process changes; statistical failures are effectively solved through redundancy and quality control**
- **The physics of most failure mechanisms is poorly understood. This requires a high reliance on emperical characterization and testing**
- **Increased temperature is an excellent universal accelerator of chemical degradation mechanisms. Typical acceleration is Arrhenius with a factor of 2 increase per 10°C**

## Figure 6. Module Qualification Experience

- **Qualification testing is a cost-effective way to identify obvious reliability problems; should be used during development as well as for design verification**
- **New designs almost never pass the Qual tests on the first try**

  **Corollary: Great political pressure to field unqualified hardware generally results in disaster**

  - **Slipped schedules, cost overruns**
  - **Early application retirement**
  - **Minimal learning**
  - **Decreased credibility**
- **Qual tests must be periodically updated to reflect field experience with previously tested modules**
- **Long-term life testing at parametric stress levels is required for quantitative correlation to extended field performance**

## Figure 7. Qualification Test Experience

- Temperature cycling and humidity tests are workhorse tests with good correlation to field failures; they are generally the most difficult to pass
- Hot-spot testing is controversial, but correlates well to field experience. Its complexity requires a high skill and knowledge level
- Mechanical loading, twist, and hail tests are effective design requirements and generally straightforward to meet
- Voltage standoff (hipot) requirements require great care in design and are troublesome to meet
- Photothermal testing (UV) is extremely complex with poor correlation with field results (no Qual test exists)
- Soiling evaluation is best done in field tests, but is highly site-dependent (no Qual test exists)

## Figure 8. Field Test Experience

- Most problems are not accepted as problems until encountered in large operating systems
  - Large statistical sample size aids quantification
  - Operational user-interface stresses are present

  Corollary: Good module not proven good until tested in large operating system

  Corollary: Operational interaction of module with user system is important source of module stress
- Test-stand aging only useful for very generic problems; sample sizes too limited for statistical failures; many user interface stresses not present in test-stand tests
- Reliance on field-failure data places requirements on system experiments:
  - To obtain quantitative data on failures
  - To have failure containment features
  - To have failure contingency plans

## Figure 9. Conclusions

- Crystalline-Si and thin-film modules are expected to have much in common with respect to reliability problems, methods and solutions
- New materials and processes in thin-film modules will require a diliquent reliability program
  - Establishment of mechanism-specific reliability goals
  - Quantification of mechanism parameter dependencies
  - Prediction of expected long-term degradation
  - Identification of cost-effective solutions
  - Testing and failure analysis of trial solutions

## DISCUSSION

YERKES: Can you guess where problems might be different from those with the modules we have been doing for 10 years, in the new thin-film modules? Some insight on your part, from early examination.

ROSS: Most of our testing indicates that thin-film modules and crystalline modules are quite similar; things like hot-spot heating modes are almost identical. The cell-breakage problem is a big difference. Crystalline-silicon cell cracking was one of the more formidable problems, long-term, in differential expansion stresses and processing yields, and thin-film modules will have a different type of processing-yield problem, I'm sure. Crystalline cells allow series-paralleling to solve the cell-shorting mismatch type of problems. I'm not sure if that is going to be a problem with thin-film modules; it depends on how uniformly the deposition can occur. It may be a different problem with stainless-steel-backed modules; they may go through the same kind of cell shorting that crystalline modules do. Corrosion-type issues are clearly going to be different, although the data we have in our electrochemical corrosion studies indicate there is not much difference between the resistances of thin-film modules and those of crystalline modules. When you have a micrometer or so of material and lose a half micrometer you have lost a cell. On a crystalline cell you can lose a lot of the metallization system; there are bulk amounts of material that you can corrode away and still leave an active solar cell. The crystalline cells are less fragile in terms of mechanical damage. With thin-film cells, if you penetrate the back side with something, you could poke a hole right through the cell. At the same time, the thin-film cells are very resistant. If you lose a part of the cell they typically don't shunt and the lateral series resistance is such that a small area of damage doesn't seem to spread across the total cell in terms of total electrical effect. There are differences.

SESSION I

CELL AND SYSTEM CHARACTERISTICS
AFFECTING MODULE DESIGN

Chairman: L. Herwig
(U.S. Department of Energy)

D2

N86-12761

# LIGHT-INDUCED EFFECTS-IMPACTS TO MODULE PERFORMANCE MEASUREMENTS AND RELIABILITY TESTING: AN OVERVIEW

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The stability of solar cells is a key factor in determining the reliability of photovoltaic modules and is of great interest in the case of solar cells having a new technology which has not yet been fully developed. In particular this question arises with hydrogenated amorphous silicon (a-Si) solar cells because a-Si exhibits reversible light-induced changes in its electronic properties, commonly referred to as the Staebler-Wronski effect (SWE).

Continuous progress is being made in the peak conversion efficiencies of a-Si solar cells and efficiencies in excess of 11% have been achieved. This progress results from the continuous improvements made in material synthesis, device processing as well as the introduction of new device structures. This makes it difficult to obtain a detailed evaluation of the effects that light-induced changes in a-Si have on the degradation of solar cell efficiencies. Futhermore because of the time required to characterize the long term stability of solar cells there are relatively few results reported on high efficiency cells. The results however clearly show that stability is still a problem, even though efficiencies to which the devices degrade have significantly improved. Recently, ARCO Solar has reported results on solar cells which, after over a year's exposure to sunlight, under open circuit conditions, still had about 7% conversion efficiency[1]. These results by Ullal et al. are shown in Figure 1. The data in Figure 1, as well as that reported by others, exhibit a region of fast degradation for about a month but that the degradation then becomes very slow.

The large changes that occur quite rapidly, which have been and are being studied quite extensively, are found to be reversible. These light-induced changes in cell performance are generally associated with the SWE rather than changes in the junctions, interfaces and contacts. The light-induced changes associated with SWE occur: in the bulk of the a-Si, they occur with sunlight illumination; they are perfectly reversible upon annealing in the dark at ~200°C; and they result from the introduction of metastable defect. Such changes occur in undoped and doped a-Si films which have been prepared under a wide range of preparation conditions.

The reversible-light induced changes in a-Si were first observed and characterized by the decreases in the dark conductivities and photoconductivities of a-Si films[2]. Figure 2 and 3 show the decreases in dark conductivity (dashed lines) and photoconductivity (solid lines) for glow discharge produced a-Si films during illumination with 200 MW $cm^{-2}$ filtered tungsten light. Figure 1 is for an undoped a-Si film and Figure 2 is for an a-Si film doped with 0.1% $PH_3$[3].

As can be seen in these figures the changes in the dark and photoconductivities can be very large (orders of magnitude) and they occur rapidly upon illumination comparable to 1 sun. Consequently such changes are still used to characterize the presence of light-induced changes in a-Si. However it should be pointed out here that since the changes result from the introduction of metastable defects into the gap of a-Si, the effects of such defects depend strongly on the densities of the initial states in the gap as well as the type and densities of the light-induced defects with larger densities of gap states the conductivity changes may become smaller or even not detectable. Correspondingly solar cells that have low efficiencies to beign with may have much smaller degradation. It

is important also to note here that the changes in conductivities exhibit quasi-exponential decays that depend on the light intensity and which at illuminations of ~1sun may have time constants of the order of 10 hours.

The continuous introduction of the metastable defects leads to continuous changes in the lifetimes of photogenerated carriers. This is illustrated in Figure 3 where the photoconductivity σp, generated by penetrating light is shown as a function of relative light intensity for the undoped a-Si film of Figure 1 after annealing and subsequent prolonged exposure to light to a maximum of 4 hours[2]. These changes indicate that the introduction of metastable defects not only decreases the electron lifetimes but also changes the kinetics of recombination.

The large changes in kinetics seen here illustrate that the extent of the light-induced photoconductivity change depends on the level of illumination. This is important to keep in mind when considering changes in solar cell performance. Because of the device nature of solar cells their recombination kinetics are more complicated and involve both electron and hole lifetimes. The effect of introducing metastable defects on the recombination of carriers will depend both on the type of illumination as well as the device structure itself.

The changes in dark conductivities and photoconductivities are found to be perfectly reversible upon annealing in the dark at temperatures ~ 150 to 200°C. Because the defects are metastable the rate at which they anneal out depends on the temperature. This is illustrated in Figure 4 where the thermal relaxation time is shown as a function of temperature. The measurements were made at the indicated temperatures as shown in the inset where the slope of the line gives an activation energy of 1.5 eV[2]. There is a lack of systematic studies in which the temperature of

the light-induced changes and kinetics of the annealing process have been investigated. However the results shown in Figure 4 indicate that the operating temperatures of solar cells are important in determining light-induced changes of their prformance.

There have been many studies carried out on the reversible degradation in a-Si solar cell characteristics. These studies have been carried out on a-Si materials fabricated under different conditins, materials that contain different types and levels of impurities and defects as well as on solar cells having different device structures. A wide range of results are reported not only on the changes in cell efficiencies but also in the different cell parameters. This wide variation is due to both the different materials and the different device structures used. The cell structures are important because even with the same materials they can be used to modify the recombination kinetics. This changes both the rate at which metastable defects are created as well their effect on the overall characteristics[4]. Because of this wide range of results it is difficult to quantify the relations between metastable defects and the light-induced changes in the cell parameters. In general degradation, to a varying degree, occurs in all three cell parameters.

The open circuit voltage appears to be the least sensitive to light-induced changes but significant degradations can be found especially after long exposures. Some of these changes however are not reversible which would exclude the SWE as the principal cause. Changes in the short-circuit currents are the primary causes of light induced degradation in a-Si solar cells.

The short-circuit currents are affected by the indroduction of metastable defects because their effect on the carrier lifetimes and the

electric field distribution in the cell. As indicated earlier this effect depends strongly on the device structure as well as the types and densities of light-induced defects which are likely to be different for cells fabricated under different conditions. The contribution of changes in the hole lifetimes and the electric field which lead to changes in the short-circuit currents are illustrated in Figure 5. The results in Figure 5 show the change in the spectral response of a Pt/thick a-Si solar cell structure in annealed state A and light soaked state B (30 hours of AMI illumination). In these simple cell structures the increase in the short-wavelength response results from an increase in the surface electric field and decrease at the longer wavelengths results from the shorter hole lifetime and diffusion length[5]. It should be pointed out here that the difference in both the magnitude and spectral response are obtained even with these simple cell structures which result from relatively minor changes in the fabrication of the a-Si and it has been difficult a-priori to predict either the rate of the degree of degradation in the short-circuit current. It is also important to note here that the changes in hole lifetime significantly smaller than the electron (photoconductivity) lifetimes have also been observed, indicating that light-induced defects can be created which are quite different to those initially present in the a-Si.

Because the fill-factor is the cell parameter that is most sensitive to both carrier lifetime and electric field changes, it is also most sensitive to the a-Si material and the cell-structure. It is therefore the most difficult to characterize its changes in terms of light-induced defects particularly since there are such large uncertainties about the exact nature of these defects. Unfortunately it is the cell parameter that often dominates the degradation of high efficiency a-Si solar cells.

Despite the large number of studies on light-induced degradation of cell efficiencies and cell parameters there have been very few studies where these changes have been directly related to the light-induced defects whose densities and electronic properties have been measured using different techniques. Furthermore even though light-induced changes in a-Si have been of interest since 1976 these changes are still not well understood. Although there is general agreement that these changes result from the introduction of metastable defects there are still many unanswered questions regarding their origin, nature and electronic properties. It is not yet known how many different metastable defects can be created in a-Si, if there is a signle type of defect that is dominant in high quality a-Si, whether the defects are related to impurities, dopants or just structure and what is the electronic nature of these defects.

The answer to such questions and the control of these defects are clearly necessary before it is possible to accurately project their ultimate limitation on the long term performance of high efficiency a-Si cells. The present lack of these answers means that great care must be taken in evaluating the degradation in a-Si solar cells and modules.

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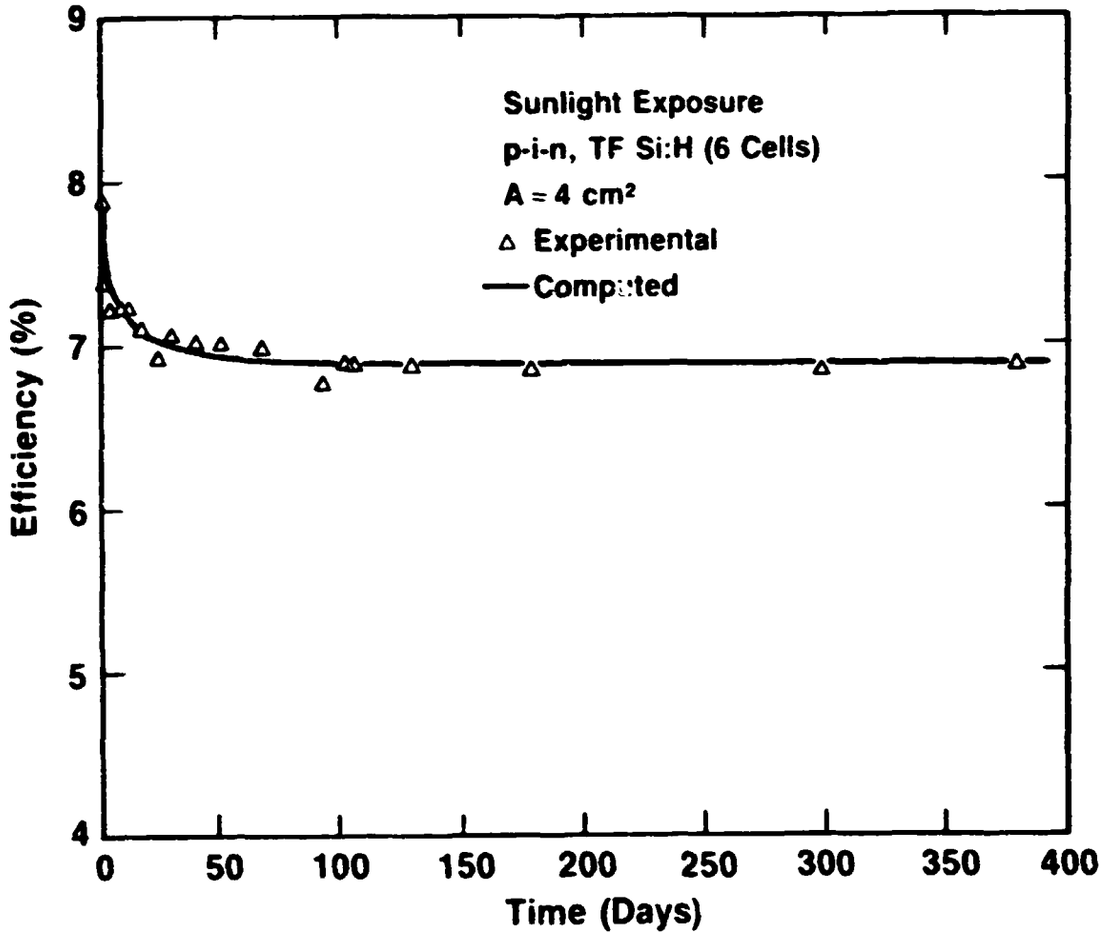
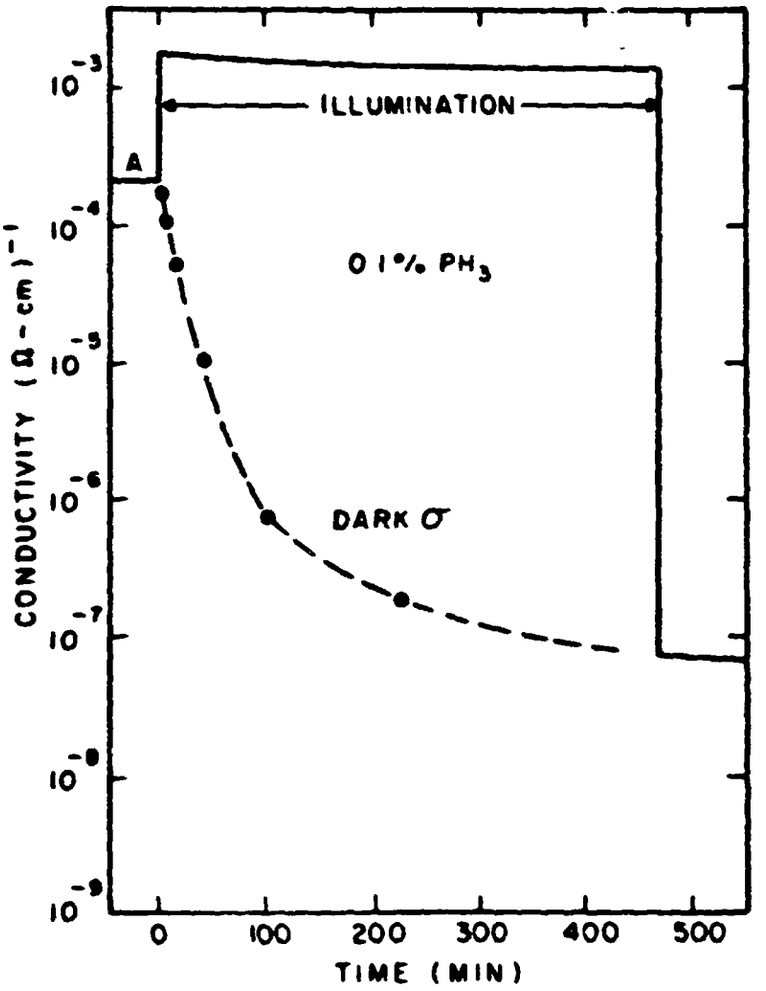
Figure 1




Ullal, Morel, Wilett, Kanani

# STAEBLER-WRONSKI EFFECT

Figure 2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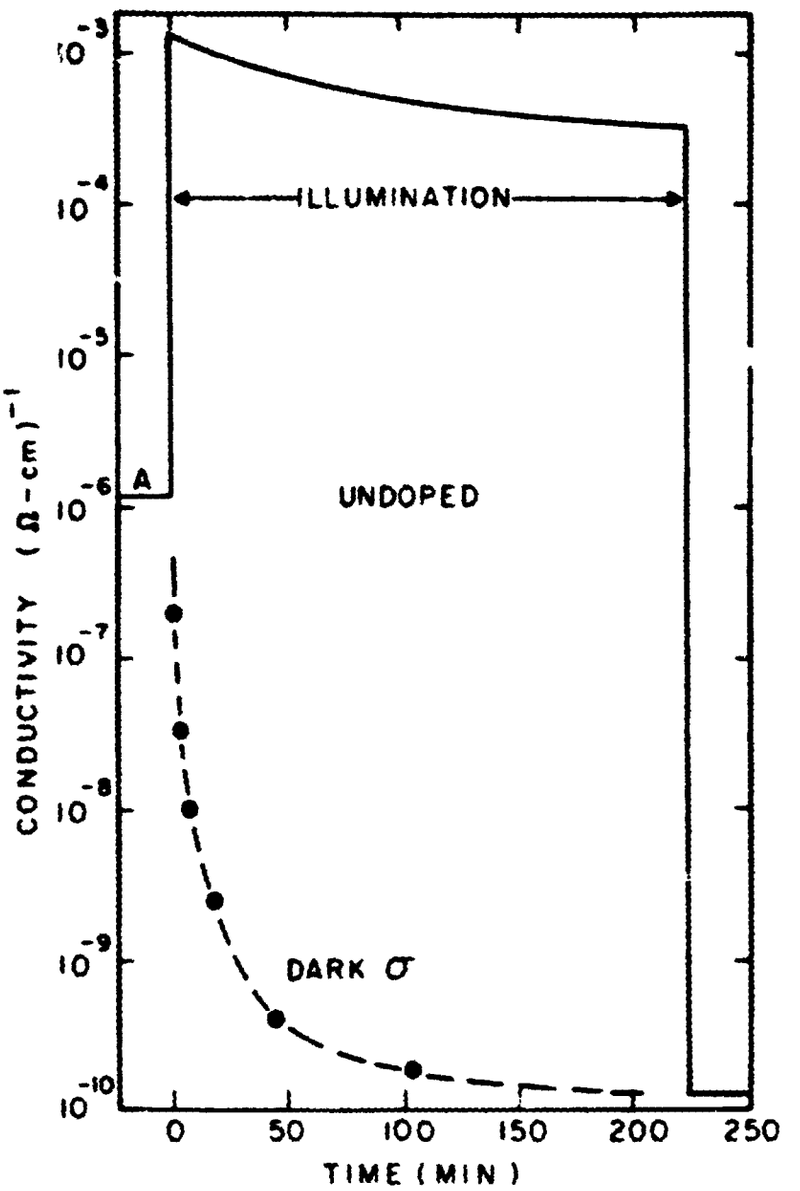
TIME (MIN)

Figure 3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UNDOPED
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250

Figure 4

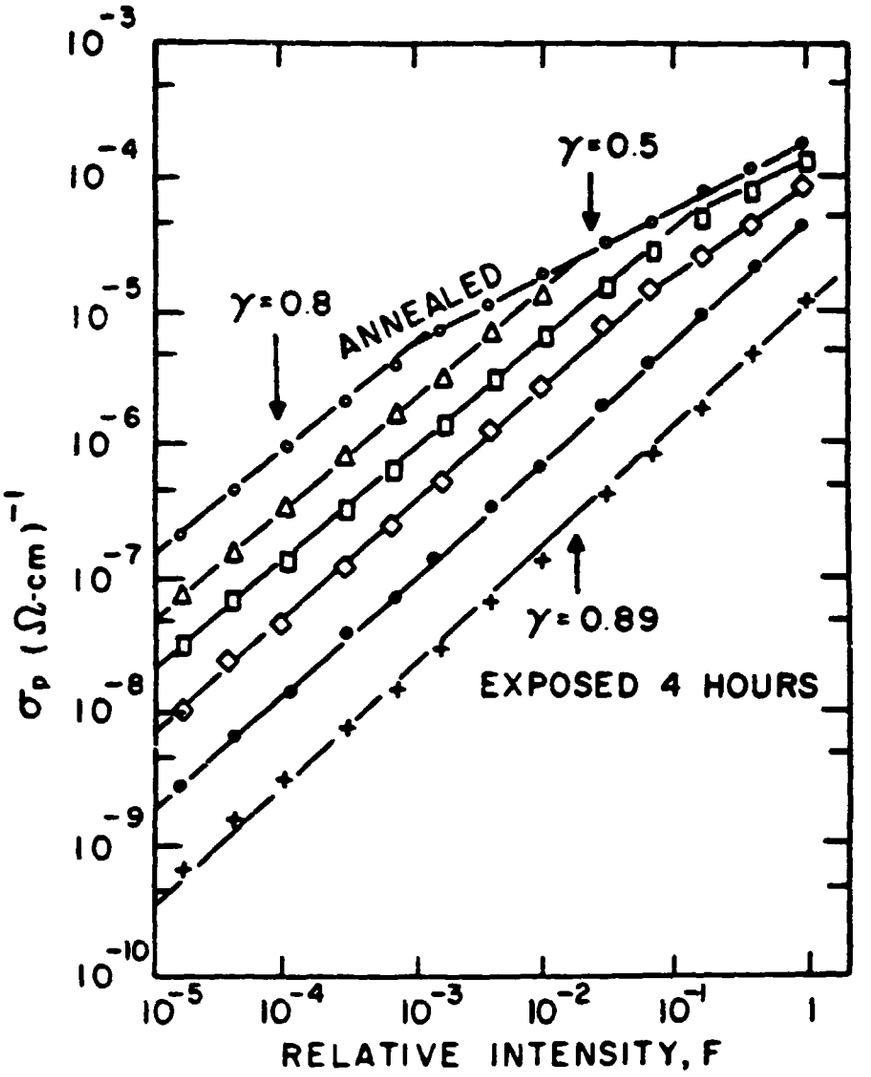

$10^{-3}$
$10^{-4}$
$10^{-5}$
$10^{-6}$
$10^{-7}$
$10^{-8}$
$10^{-9}$
$10^{-10}$
$\sigma_p$ $(\Omega\text{-cm})^{-1}$
$\gamma = 0.5$
$\gamma = 0.8$
ANNEALED
$\gamma = 0.89$
EXPOSED 4 HOURS
$10^{-5}$
$10^{-4}$
$10^{-3}$
$10^{-2}$
$10^{-1}$
1
RELATIVE INTENSITY, F

Figure 5

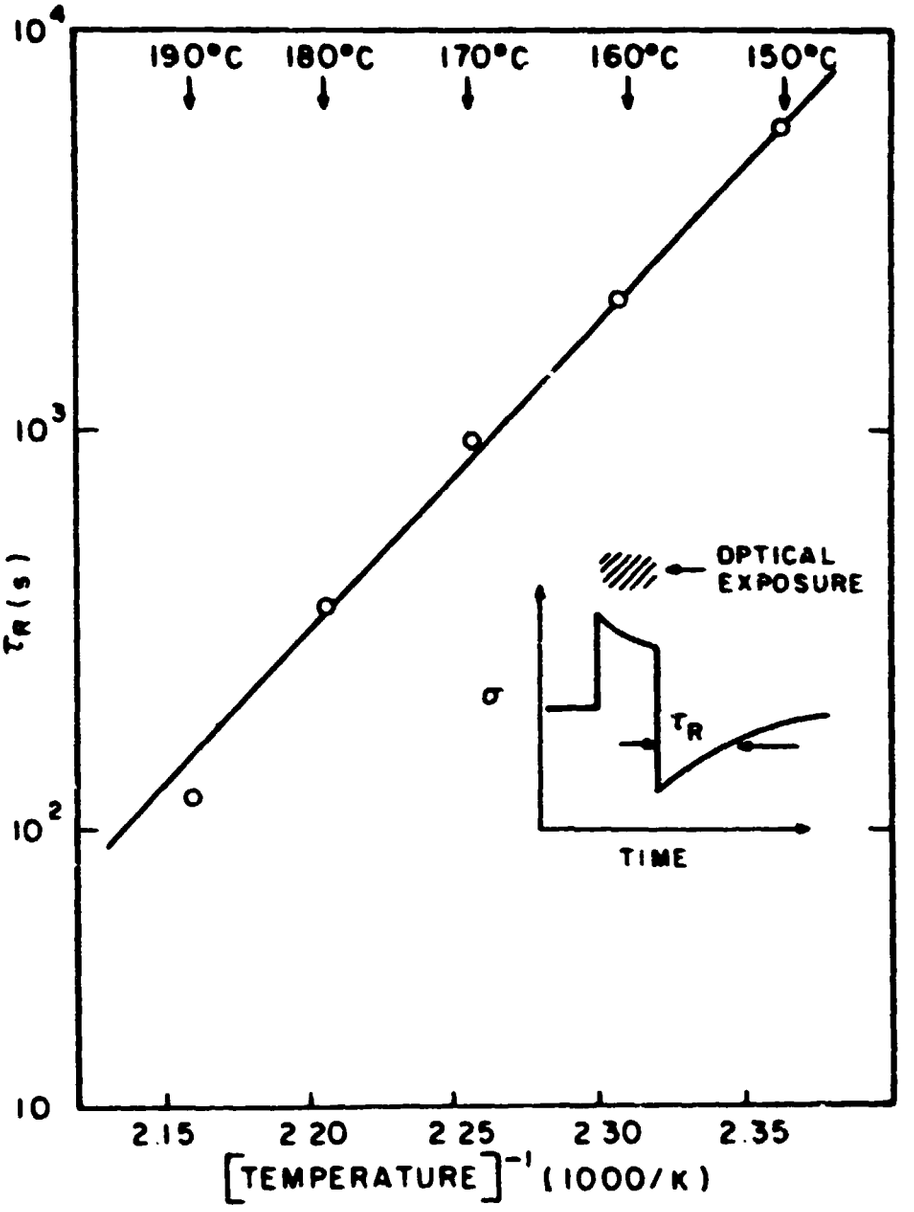

190°C
180°C
170°C
160°C
150°C
$10^4$
$10^3$
$10^2$
10
$\tau_R$ (s)
OPTICAL EXPOSURE
σ
$\tau_R$
TIME
2.15
2.20
2.25
2.30
2.35
[TEMPERATURE]$^{-1}$ (1000/K)

Figure 6

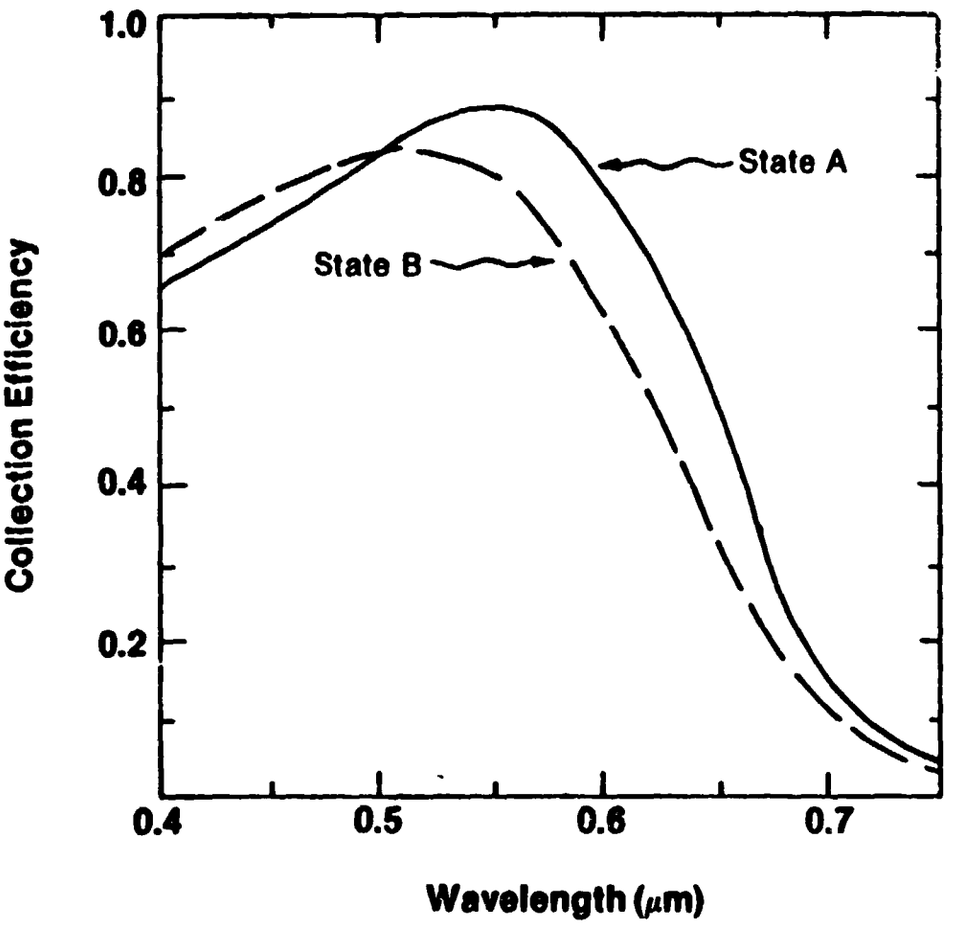

1.0
0.8
0.6
0.4
0.2
Collection Efficiency
State A
State B
0.4
0.5
0.6
0.7
Wavelength (μm)

Figure 7

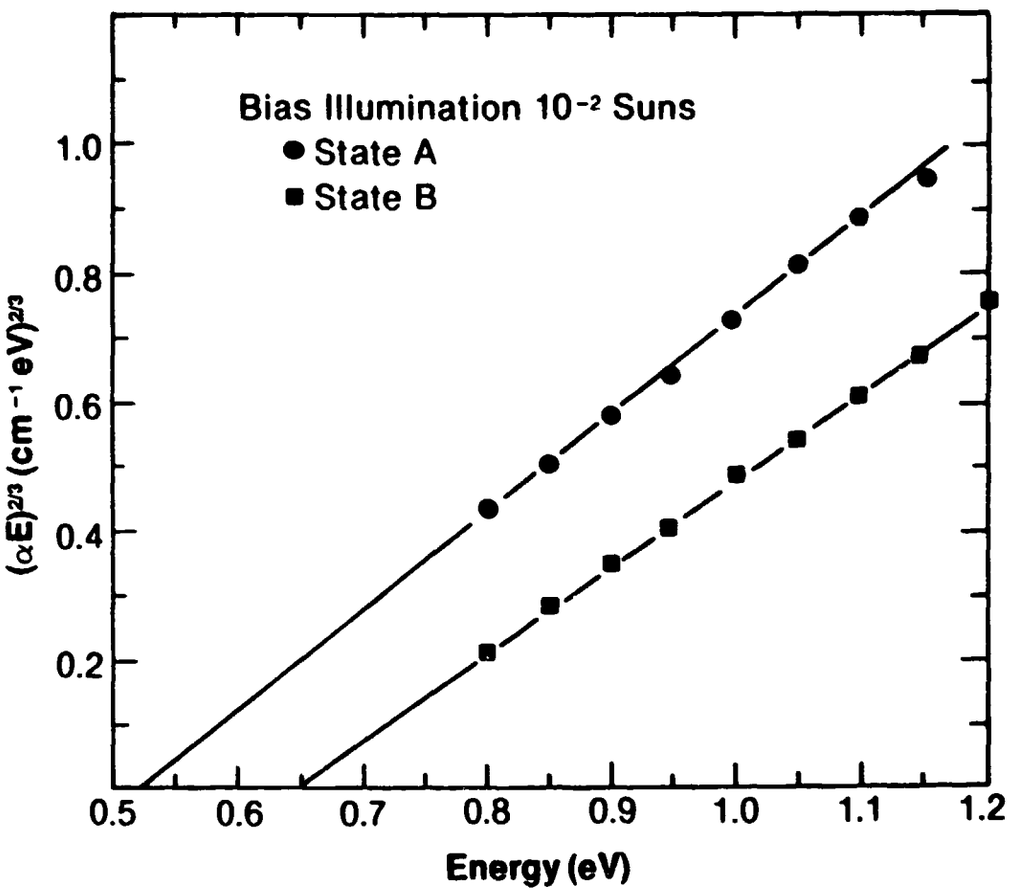

Bias Illumination 10⁻² Suns
State A
State B
1.0
0.8
0.6
0.4
0.2
(αE)^2/3 (cm^-1 eV)^2/3
0.5
0.6
0.7
0.8
0.9
1.0
1.1
1.2
Energy (eV)

Figure 8

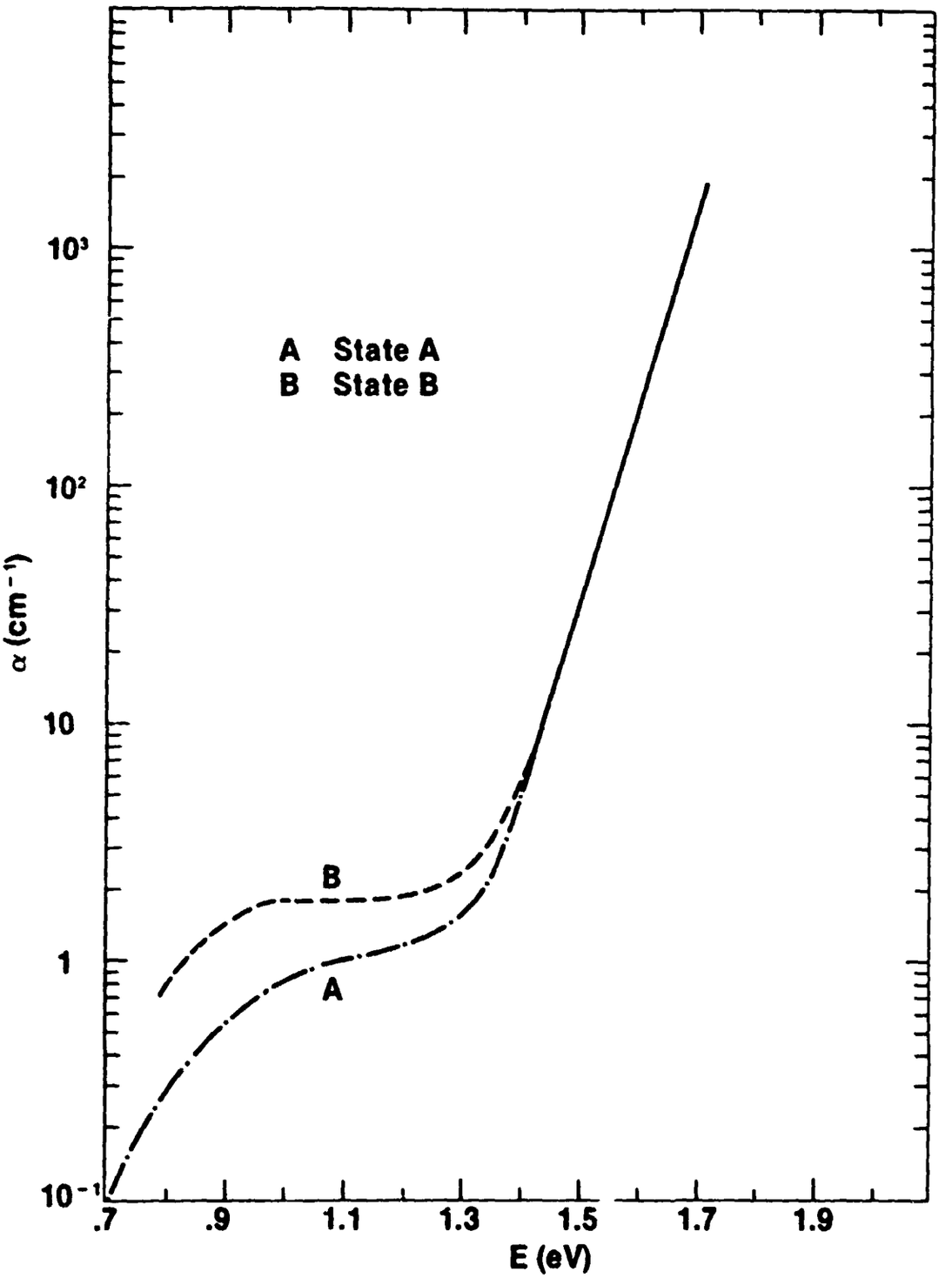
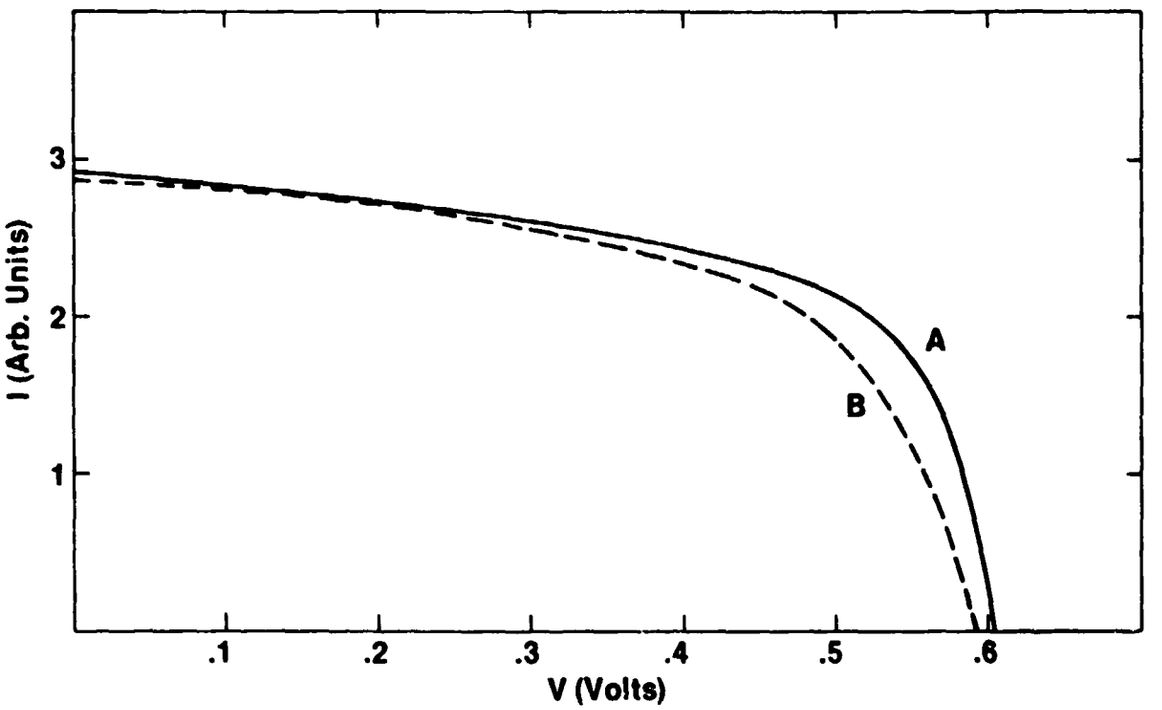


Figure 9



## DISCUSSION

KIM: Do you think that some of the defects are created by laser scribing or some other processing?

WRONSKI: Certainly, but I suggest you ask ARCO and Solarex, Thin-Film Division. Any light-induced stress obviously is going to cause an effect. The other question is what energy has the light used. If you use a laser scriber with a short wavelength you will damage the surface region of the junction. It doesn't seem to be wavelength-dependent, providing you can create the photogenerated carriers, which can be done quite efficiently even with sub-band-gap light. It is the recombination of a hole and an electron. You need a lot of recombination before you get one defect.

HERWIG: Presumably some wavelength would be more active in creating interaction with the impurity that some other wavelength --

WRONSKI: That is correct. The detailed studies have not become reality. There is a lot of work to be done. It is very important for people to get together and exchange their experiences, as this field is completely open.

LESK: I wonder whether these cells behave like crystalline silicon, in that if it's space charge recombination-dominated you get a large $E_g/2kT$ term. You blame some of the effects on recombination. Do you see, under forward bias, a large increase in the 2kT term, or do they behave differently?

WRONSKI: All I can talk about is the Schottky barrier; that's the one we have really studied. The results I've shown here are trying relate the bulk. In order to get at the bulk we try to minimize any effect of a p junction, of cell thickness, and so on. Yes, you do get a degradation, you do get a change in the diode quality factor.

LESK: The bulk is the high region. It's a space-charge region during operation and so it is a very narrow region in crystalline silicon. A second question: with crystalline cells and modules we find the fill factor is very fickle and can be affected by many things, both in series and parallel effects, and you have to be very careful if you blame it on a fundamental mechanism, because it may just be a non-uniformity effect in the single cell or series cell.

WRONSKI: I agree 100%. This is one of the results that seems to tie in with the collection efficiency measurements, except that the fill factor follows the contour of an increased field and lower recombination. But of course the fill factor depends on the most parameters, cell material and so on, and unfortunately it appears to be the one that really degrades the most in high-efficiency cells.

ROSS: One of the issues that we asked you about and I'll ask you again -- this is one that is always difficult for us that are researching mechanisms other than the light-induced effect, which is in fact where our primary focus is at JPL. How does one eliminate this effect in terms of measurements that we are trying to make on some of these other irreversible types of degradation mechanisms? Is there something that one can do to sort out that degradation that's associated with light-induced as opposed to -- or inhibited, for example, by applying reverse bias during, say, the accelerated testing of a different type of test?

WRONSKI: That's perfect. Two questions here. One of course, I think, in principle -- although again I think you should talk to the people who are manufacturing modules. If this is a bulk effect it is perfectly reversible. So, therefore, if you don't degrade something else by heating, in principle, you could remove the effect in the bulk. The other thing you asked?

ROSS: Can you inhibit it?

WRONSKI: Of course; that, by the way, has been done. Again relating back to recombination: If you reverse-bias the cell you put a large field, you decrease the recombination, and indeed, people find that the cell does not degrade from the bulk effect. Conversely, by putting it under load you really increase the recombination. So definitely a bias is an important parameter and is one way of differentiating between them.

HERWIG: I hear that CVD potentially does not introduce the problem while glow discharge does. Do you put any stock in that?

WRONSKI: I believe everything the first time I hear it. I have read it more than once. I think it is an open question. Obviously, if you believe that it is structural, that the defects are related structurally, I believe it. I also believe in impurities. I think they are both there but then of course the way you deposit the material is going to be very important. And CVD, in principle, is more gentle. The Japanese are pushing for CVD in a big way. And there, by the way, they are doing it at the junction now rather than the whole film, to reduce recombination of the hetero contact.

TURNER: I'll try and ask this question so that it's illuminating rather than confusing. I'm not sure I know the answer, but I think I do. You made a remark about recombination causing the degradation or by an increase of these things that Xerox calls D states. I hate to use the word instability because I don't think that something that is reversible can be called an instability. You then made the remark that thin devices degrade less than thick devices because the recombination is less. My understanding of this, and I would like to try it out on you, is that when you see degradation, you generally have put the device out in the sun for some hours, or a bright light for some hours, under open-circuit conditions. Under

those conditions, basically, since the absorption in a thin device is very similar to the absorption in a thick device -- to first order, approximately the same -- under open-circuit conditions, then, the recombination must be the same. But the device does not degrade as much because, being a thinner device, it has a higher electric field. So the fact that there are more D states doesn't hurt you as bad. Did I get that right?

WRONSKI: Yes. That's right. The degradation -- you have got the same built-in potential, so therefore the voltage you are putting on it when you operate it is the same in both cases. Now let's look at it in terms of space charge; if you increase the space charge by the same amount in both cells, the field at the other end is going to be much smaller in the thicker cell than in the thin cell, even though you have increased the space charge density by the same amount. That is the way I look at it. Now the other point I would like to ask you is how critical is the operating condition of the cell in the life test, whether you put it under load or whether you put it under under short-circuit current or under open-circuit voltage? Is that a very important factor?

TURNER: It certainly degrades less rapidly if you operate it at the operating point than if you operate it at open circuit. But what the ultimate end point is, I don't know.

HERWIG: Then there is the question of n-i-p vs p-i-n?

WRONSKI: Well, why the differences occur is again because of the way the cell operates. With the n-i-p you are illuminating at the lowest field region, if you assume that the biggest field region occurs at the peak p-i-n site. I would like to say I don't really use the n-i-p much. The primary manufacturers are using p-i-n.

D3

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# Thin-Film Module Circuit Design - Practical and Reliability Aspects*

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## ABSTRACT

This paper will address several aspects of the design and construction of submodules based on thin-film amorphous silicon (a-Si) p i n solar cells. Starting from presently attainable single cell characteristics, and a realistic set of specifications, practical module designs will be discussed from the viewpoints of efficient designs, the fabrication requirements, and reliability concerns. The examples will center mostly on series interconnected modules of the superstrate type with detailed discussions of each portion of the structure in relation to its influence on module efficiency. Emphasis will be placed on engineering topics such as: area coverage, optimal geometries, and cost and reliability. Practical constraints on achieving optimal designs, along with some examples of potential pitfalls in the manufacture and subsequent performance of a-Si modules will be discussed.

## I. INTRODUCTION

A major advantage of thin-film solar cell technology is the ability to deposit the active film over large areas in a single process step. Practical considerations, however, require that the photovoltaic area be divided and individual cells be interconnected so as to provide specified voltages and currents. For amorphous silicon and several other thin-film devices which are deposited on a transparent conductive surface, the series connected monolithic module has evolved as a convenient and efficient structure to accomplish this division to form practical circuits. Indeed, a-Si modules of this type are now commercially sold in solar powered calculators and battery chargers. This structure is comprised of a number of side-by-side rectangular shaped cells connected electrically in series on a single glass substrate. The interconnection is accomplished by a sequential patterning and deposition of the various films comprising the vertical cell structure. Since the resultant structure is essentially one dimensional, relatively simple design rules can to first order be derived and applied. However, practical structural and circuit requirements force the consideration of two dimensional effects; in addition, limitations of the patterning process, interactions of these processes with film properties, and the necessary junction of dissimilar materials can affect both the module design and its ultimate performance and reliability. Such considerations for a-Si solar cell modules are the subject of this paper.

## II. SINGLE CELL CHARACTERISTICS

In order to design modules for specified electrical performance (voltage, current, power) individual cell IV characteristics should be examined to extract average cell parameters to be used in the design calculations. For a-Si cells of the p i n structure deposited on a transparent superstrate, the I/V curves and parameters shown in Figure 1 are typical of the range that can be obtained

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with present technologies. Several features should be noted when comparing these to the parameters of single crystal silicon (C-Si) cells. First, generated photocurrent is about 1/3 to 1/2 that of C-Si cells, open circuit voltage is about 300mV higher, and the fill-factor is generally lower with a "soft" I/V curve characterized by a somewhat low equivalent shunt resistance as shown in Figure 1(b). The high $V_{oc}$ is a distinct advantage for series interconnection, but the lower generated current implies larger area to achieve a given power output. The "softer" shunt-like I/V characteristics while reducing the maximum power available, may have some advantage for hot-spot tolerance. Parameters close to those of Figure 1(b) will be used in the example presented below.

## III. STRUCTURE AND DESIGN EXAMPLE OF SERIES INTERCONNECTED a-Si MODULE

The cross sectional structure of a monolithic series connected module including bus contacts is shown in Figure 2. The deposition and patterning steps typically used to fabricate this structure are shown in Figure 3. The deposition of the various films will not be discussed here, but the choice of processing method and geometry of the patterning are important to the design considerations. Several methods are available to accomplish the patterning such as screen-print masking followed by wet or dry etch, mechanical scribing, and laser scribing. Laser patterning is desirable because of its speed, dimensional control, economy of area loss and absence of wet chemicals. Typical dimensions achievable with laser scribes are shown in Figure 4. For comparison, also shown in Figure 4, is a typical metal patterning made by a wet etch, which results in a tripling of the area loss.

An example of the design of a module suitable for charging 4 NiCd "D" cells with average available light equivalent to one half AM1 is shown in Figures 5 and 6. The results are given for both laser scribe (values in parenthesis) and wet etched metal patterns. The losses due to bus bars and edges (5.3% and 4.7%) are considerable in this example due to the small size of this modules. The physical size of these parts will not change substantially in large modules resulting in much lower fractional loss (about 6% for $1ft^2$ modules). Note that the shadow and ohmic losses are more than halved for the laser scribed case.

## IV. PRACTICAL RELIABILITY CONCERNS FOR THIN-FILM MODULES

A number of potential reliability issues could arise both during the fabrication of thin-film modules and later on due to environmental stress or aging. These are listed in Table I.

TABLE I

RELIABILITY CONCERNS

PROCESS RELATED

| Type | Cause (s) | Result |
|---|---|---|
| pin holes or stressed areas | dirt or impurities<br>thin a-Si film at edges | shorted or shunted cells |
| segments shorted together | missing laser pulses<br>defects in $SnO_2$ (Fig 7)<br>poor etch or mask control | shorted cells (module) |
| parasitic elements | incomplete a-Si scribe (Fig 8)<br>too complete a-Si scribe | low fill factor<br>power loss |

STRESS RELATED

| Type | Probable Cause | Result |
|---|---|---|
| lateral conductive paths | ionic contamination across small dimensions | shorted segments |
| parasitic elements | loss of ohmic contacts | lower fill-factor |
| arc over | high voltage breakdown under bus extensions | shorted module |
| corrosion | liquid water or water vapor | loss of output |
| pin holes or blistered areas | stress relief, thermal expansion/contraction | loss of voltage |

## V. SUMMARY AND DISCUSSIONS

The series-connected monolithic circuit has shown to be a desirable configuration for fabricating practical thin-film solar-cell modules. It may be applied to a variety of thin-film technologies, and is already in commercial use with amorphous silicon. The design rules are quite simple with no apparent problems in scaling to large area modules.

In realizing design requirements, however, careful consideration must be given to the thin-film deposition and patterning technologies to be used in fabricating the module. In this paper, it was shown that nonuniform film depositions (edge effects), inefficient patterning and/or interactions between patterning steps can lead to large area losses, and can raise concerns over the immediate and future reliability of the module. Examination of presently available a-Si modules indicates that many of these areas are being addressed by allowing generous safety margins in area utillization, incorporating potentially more reliable substructures, and by encapsulating the modules with materials of known reliability. It is for these reasons that current commercial a-Si modules are generally only 5-6% efficient while 10-12% cells are being universally reported. As a-Si deposition technology matures, and advanced laser patterning techniques are used in production, module efficiency will increase even without futher improvement in cell performance. Laboratory and field testing should be used extensively to provide real-world experience, and the vast data already available from the testing of single crystal modules should be consulted to pinpoint potential trouble spots and to reduce time cycles for qualification of thin-film modules.

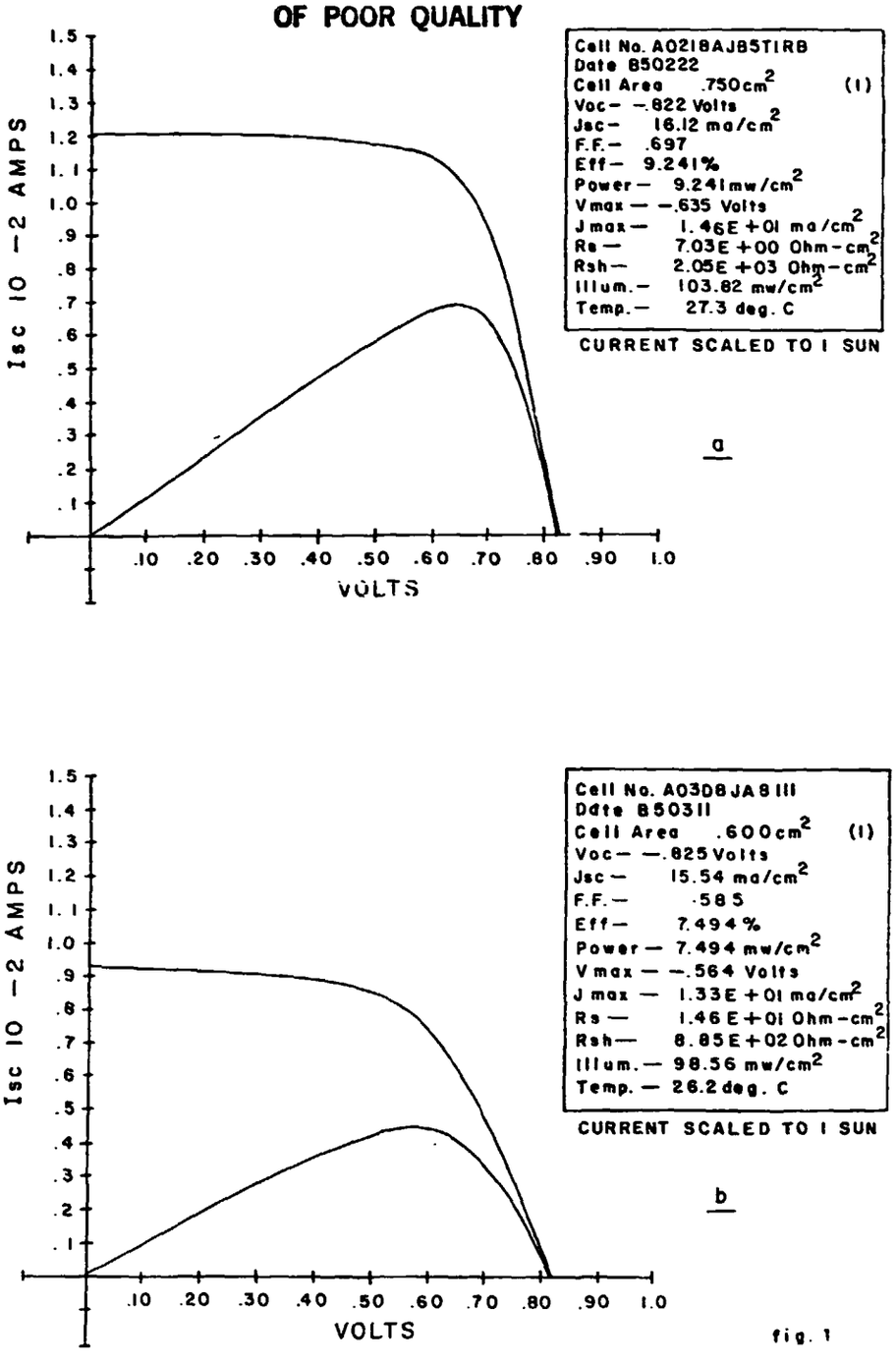



Figure 1

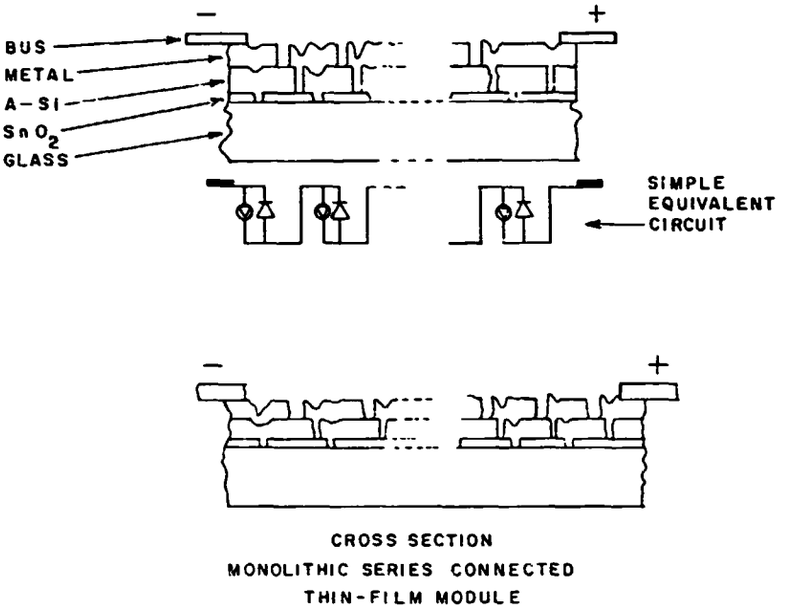



Figure 2

PROCESS STEPS

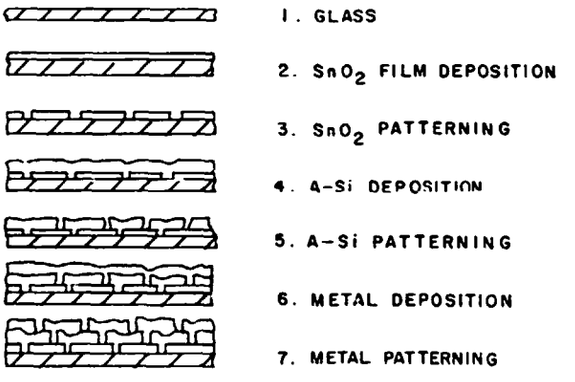
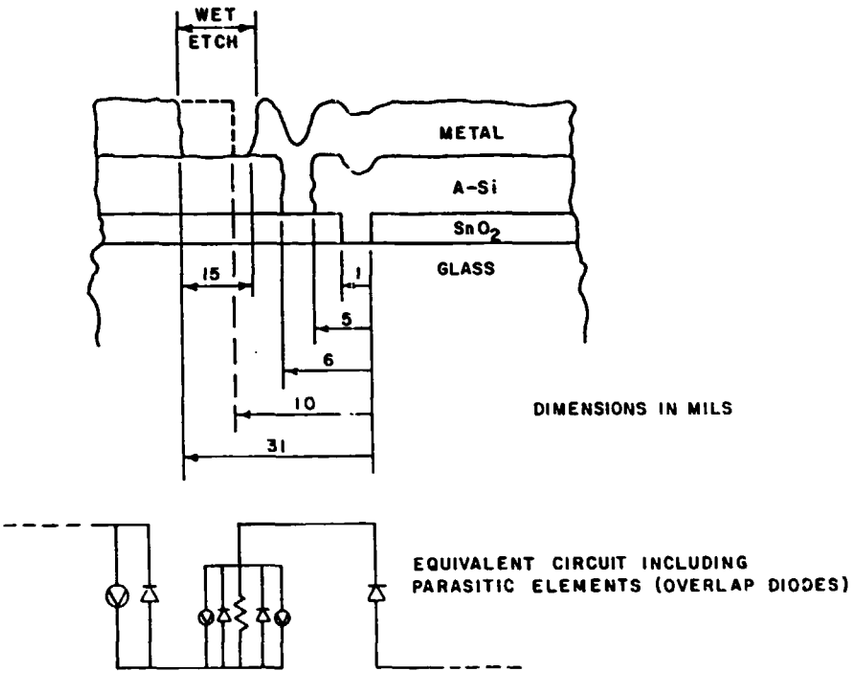



Figure 3




DETAILS OF INTERCONNECT REGION

Figure 4

EXAMPLE: DESIGN OF BATTERY CHARGER MODULE

SPECIFICATIONS: CHARGE 4 "D" CELLS (NiCD) @ 50mA @ 1/2 AM1

$V_M > 4 \times 1.4 = 5.6V$

$N = \frac{5.6}{0.6} = 9.3 =$ 10 SEGMENTS (MIGHT USE 11 FOR GOOD YIELD)

$J_M = 6mA/cm^2$ AT 1/2 AM1

$A = \frac{50}{6} = 8.4\ cm^2$

GEOMETRY $L \times W = 8.4cm^2$

$S_{LOSS} = \frac{1}{3} \frac{J}{V} R\ W^2 + \frac{D}{W}$

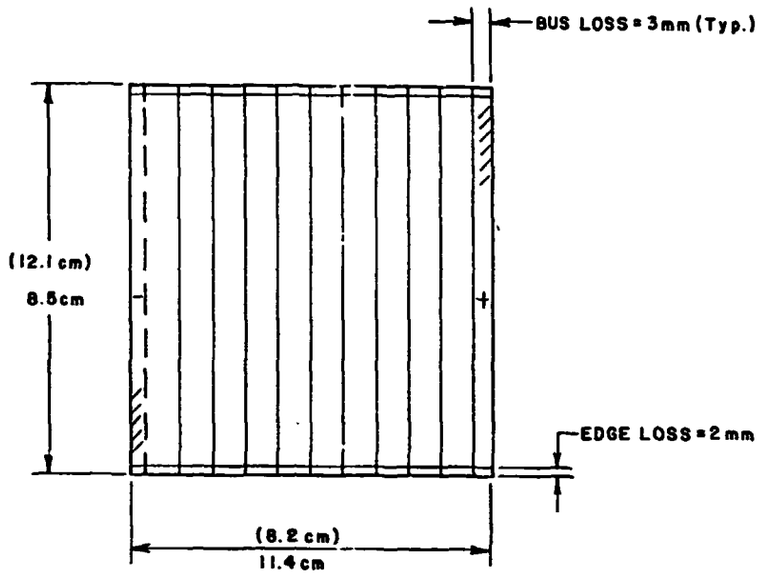
$W_{MIN} = \sqrt[3]{\frac{3DV}{2JR_\square}} = 1.04$ cm (.721cm) (LASER SCRIBED METAL)

$S_{LOSS} = 3.6 + 7.2 = 10.8\%$

$(1.7) + (3.4) = (5.1\%)$

$L = \frac{8.4}{1.04} = 8.1cm$ (11.7cm)

Figure 5




Area loss = 7.2% (shadow) + 5.3% (bus loss) + 4.7% (edge loss) = 17.2% (14.0%)
(3.4%) (7.3%) (3.3%)

Total loss = 17.2% + 3.6% = 20.8%
(14.0%) + (1.7%) = (15.7%)

10% cells ⇒ 8% (8.5%) modules

BATTERY CHARGER DESIGN

Figure 6


Figure 7

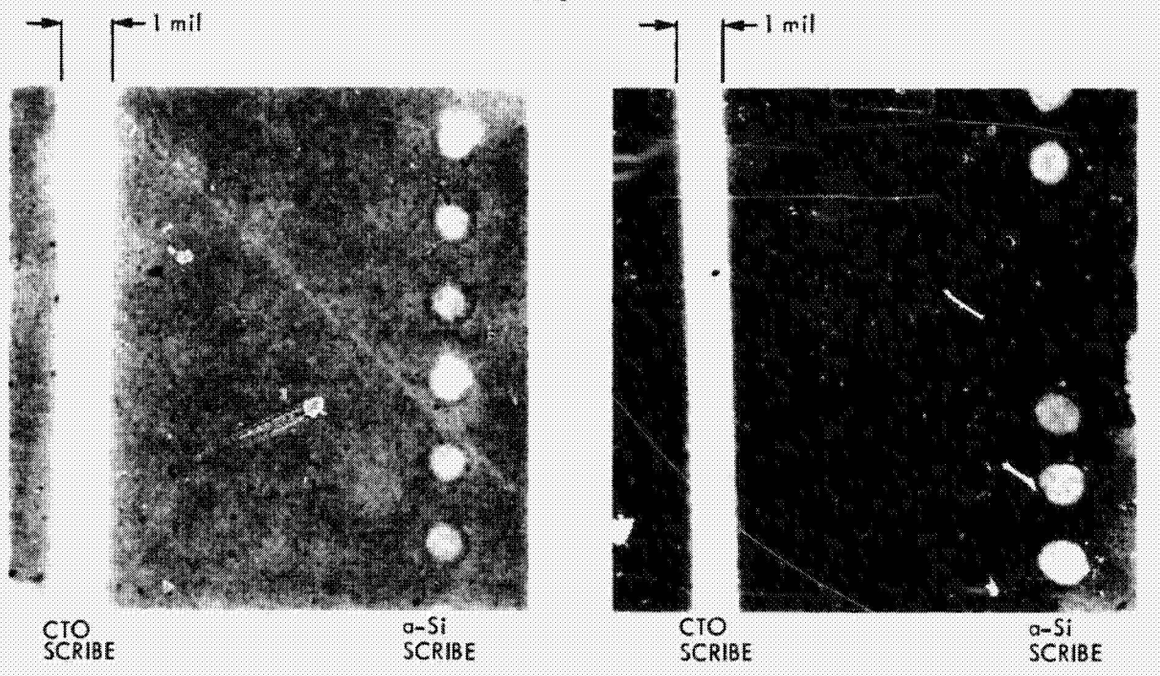



Figure 8

## DISCUSSION

LESK: In the CTO laser scribe, do you actually go all the way and take a bit of the glass, or is it transparent to the last stage, intact?

D'AIELLO: It depends on how much power you use to do the scribe. You can take a bit of the glass away. If you go too far you will cause a deep cavern there, which must be covered by the silicon later, and it's a cause for concern. It is not usually a problem, though in practice --

LESK: If you take a little bit of the glass, you are trying to contact CTO on the edge, and you could get a little layer of glass covering it and have high contact resistance there.

D'AIELLO: That's correct.

YERKES: It looks in your diagram like we have quite a different situation in these designs with regard to paralleling diodes. I know you are not worried about big arrays at this point -- maybe you are -- but some of the things Ron Ross talked about earlier, it looks like this would make potential for either easier dioding or automatically incorporating some parallel leakage in here which could help in breakdown, or maybe hurt, I don't know. Do you have a comment on that?

D'AIELLO: It's a good point. Your imagination can run wild. My background is semiconductor devices, and I'm used to thinking of integrated circuits that I can wrap around these things. And there are many interesting parasitic elements that could be useful in this design, as an integrated monolithic design, that we can add to this. I have only covered the series-connected aspects. You could put some blocking or bypass diodes right on board the circuit. However, there are also some on-board short circuits that are built in that you have to be careful about. That tin oxide is all the way to the edge of the glass, usually, and is quite conductive, so that if it is not separated adequately from the active module you can short the module out. So there's both aspects to worry about.

DELAHOY: I would like to make a quick comment and then I'll ask a question. The fill factors you mentioned around 67%-70% are good and probably typical in production for those in the audience who are not aware of what fill factors can be attained with amorphous-silicon cells. We have seen fill factors as high as 76%. So the potential is there for getting fill factors on amorphous silicon modules almost as high as crystalline cells. As you probably know, the intrinsic contact resistance of aluminum deposited under high-vacuum conditions onto clean tin oxide is indeed very low. I wondered if you had any information regarding the long-term stability for the direct aluminum-to-tin-oxide contact that is commonly used in many modules?

D'AIELLO: Well, as I mentioned in the talk, you could easily imagine how that situation that you just described would not occur in practice. If you evaporate aluminum on clean tin oxide, I agree, you will more than likely form an ohmic contact with reasonably low contact resistivity. However, we are not doing that in practice; we're removing the silicon first with a high-power laser or perhaps some other means. And you might damage the tin oxide below, change its chemistry -- if it became oxygen-rich, for example, you could easily imagine how you might affect the formation of aluminum oxide. We have looked at that interface region but I am not at liberty to comment on what the results are.

# HOT-SPOT HEATING SUSCEPTIBILITY DUE TO REVERSE BIAS OPERATING CONDITIONS

C.C. GONZALEZ

## HOT-SPOT TEST--TEST PARAMETERS

Because of field experience (indicating that cell and module degradation could occur as a result of hot-spot heating), a laboratory test was developed at JPL to determine hot-spot susceptibility of modules. The initial hot-spot testing work at JPL formed a foundation for the test development.

The test parameters are selected in the following way. For high-shunt resistance cells, as discussed above, the applied back-bias test current is set equal to the test cell current at maximum power. For low-shunt resistance cells, the test current is set equal to the cell short-circuit current. The shadow level is selected to conform to be that which would lead to maximum back-bias voltage under the appropriate test current level as discussed previously. The test voltage is determined by the bypass diode frequency.

The test conditions are meant to simulate the thermal boundary conditions for 100 $mW/cm^2$, 40 C ambient environment. The test lasts a total of 100 hours.

A key assumption made during the development of the test is that no current imbalance results from the connecting of multiparallel cell strings. Therefore, the test as originally developed was applicable for single-string cases only. Additional work has been done by JPL in conjunction with the personnel involved with the Sacramento Municipal Utility District photovoltaic-central-station array to widen the applicability of the laboratory test to multi-string applications.

## KEY LESSONS LEARNED FROM CRYSTALLINE SILICON

Several lessons learned from the testing and field experience associated with crystalline silicon modules are summarized in this section. It cannot be assumed that all of these can be applied directly to amorphous modules:

(1) The maximum allowable temperature for encapsulants before noticeable degradation is 120 C to 140 C. This will apply to amorphous modules if the same types of encapsulants are used.

(2) The hot-spot temperatures reached by different cells varied with the differences in the cell shunt resistance.

(3) The increase in temperature is affected by the ability of the module encapsulant and superstrate and/or substrate to transfer heat laterally from the hot-spot region.

(4) For crystalline cells, a common failure at high heat levels is cell shorting; the preliminary phase of amorphous cell testing does not indicate that this is also true for amorphous cells.

(5) The typical crystalline-silicon module requires bypass diodes around every 12 to 18 cells to limit hot-spot heating to an acceptable level.

(6) Hot-spot heating is a highly nonlinear function of applied current and voltage. First, cells possess nonlinear reverse I-V characteristics. Also, the shunt-resistance and hot-spot area change with temperature, the latter inversely with temperature increase.

## AMORPHOUS-CELL HOT-SPOT TESTING

An amorphous-cell hot-spot testing task has been initiated at JPL and is based on the prior crystalline work performed. As the testing has evolved, several issues have surfaced. One of these is the problem of attaching the electrical leads required for testing the cells in an encapsulated module without causing damage. This is a problem for any type of module, especially for glass rear surface modules where attachment is impossible without damage. Hot-spot testing of this type of module requires specially prepared modules with leads attached prior to lamination. The sensitive cell metallization of amorphous cells necessitates the development of techniques different from those used for crystalline cells where leads were simply soldered to the metal backing. The new techniques being considered include use of conductive adhesives, spring-loaded precious-metal-plated contacts and conductive elastomeric gasket material. The latter is good for making distributed current interfaces in applying back-bias current where use of point contacts would lead to burning away of the cell metallization.

Another issue is that of illuminating the long-narrow cells characteristic of amorphous modules. An ELH lamp is used to illuminate crystalline cells. The light pattern produced by the lamp coincides well with round or even square cells, however, it does not conform well to the long cells. Therefore, more lamps will be required to produce the same light intensity per cell active area leading to an added heat load.

Thus far, the testing has been performed on small, unencapsulated test structures. The extrapolation of these results to large cells and encapsulated modules is not straightforward. In fact, the correlation of these types of tests with results obtained or expected from full-size modules requires the ability to accurately simulate module heat transfer characteristics.

## AMORPHOUS-CELL HOT-SPOT TESTING OBJECTIVES

The objectives of the JPL amorphous-cell hot-spot testing task are:

(1) To develop the techniques required for performing reverse-bias testing of amorphous cells.

(2) To quantify the response of amorphous cells to reverse biasing.

(3) To develop guidelines for reducing hot-spot susceptibility to amorphous modules.

(4) To develop a qualification test for hot-spot testing of amorphous modules.

To date, the first objective is about 75% complete and a qualitative understanding of cell response has been achieved, but not a quantitative one. Work on the last two objectives has not begun yet.

## APPROACH

Amorphous cells are being tested using two techniques. The first is equivalent to that used in the hot-spot testing of crystalline cells; an IR camera is used to monitor hot-spot temperature and a reverse-bias I-V curve is plotted. The testing in the preliminary phase has been performed in the absence of illumination. There are two reasons for this: First, because this phase involved the development of techniques and the identification of relevant cell characteristics, it was decided to limit the number of variables influencing test results. Also, the appropriate illumination level is dependent on the circuit configuration of the test cell and cell area. Because small test structures were used in the initial phase, the required information was not yet available. It should be noted that conclusive results cannot be obtained without performing tests under illumination.

The second technique consists of pulsed reverse-bias voltage ranging in duration from 0.01 to 100 ms. A power-quadrant I-V curve was plotted initially and after each pulse. This test complemented the one discussed above for the following reasons. In some of the cells tested using steady-state back-biasing, the hot-spot reaction proceeded slowly until a voltage breakdown point was reached where the cell began to rapidly heat up, necessitating shutdown before the test structure was destroyed. The pulse testing, on the other hand, produces a controlled and uniform reaction, dependent on pulse duration and voltage test level, with essentially no heating. Therefore, the cell response can be observed in a gradual way before significant damage occurs.

## PRELIMINARY OBSERVATIONS

The preliminary observations can be summarized as follows. First, amorphous cells undergo hot-spot heating similar to crystalline silicon cells. Hot-spot heating in amorphous cells does not seem to be any less or any more severe than in the case of crystalline cells. Their shunt resistance levels are similar and their tolerance to hot-spot heating is similar. Second, the same techniques used to reduce the hot-spot susceptibility of crystalline modules are applicable to amorphous cells with the addition of new ones tailored to the unique characteristics of amorphous cells. Foremost, module design must address hot-spot heating. The more heat sinking provided by the module for the cells, the lower the hot-spot temperature. Also, because hot-spot heating is a focused phenomenon being concentrated in a small region of the cell, use of smaller cells will result in a lower maximum current and, consequently, lower hot-spot heating. Finally, the use of bypass diodes is a good technique for reducing the back-bias voltage.

## FUTURE WORK

The amorphous-cell hot-spot testing task will continue with work in the following areas:

(1) Refinement of measurement techniques in order to differentiate between effects ir. ·ed unique to the technique and effects unique to tne cell, e.g., some effects at first attributed to the cell response were because of changes in the conductive pad contacting the cell.

(2) Continuation of the testing of cells and modules as they become available from manufacturers.

(3) Correlation of the results of the test cells with module results in terms of:

   (a) The amount of additional heat sinking available.

   (b) The difference in cell size relative to the current output and increased conductance over the front surface.

(4) Performance of tests under an illumination level appropriate to given module series/paralleled configuration, cell size, and bypass diode frequency.

(5) Strive to understand the changes in cell structure after hot-spot heating.

In the last regard, particularly, JPL welcomes the opportunity to work with cell and module manufacturers.

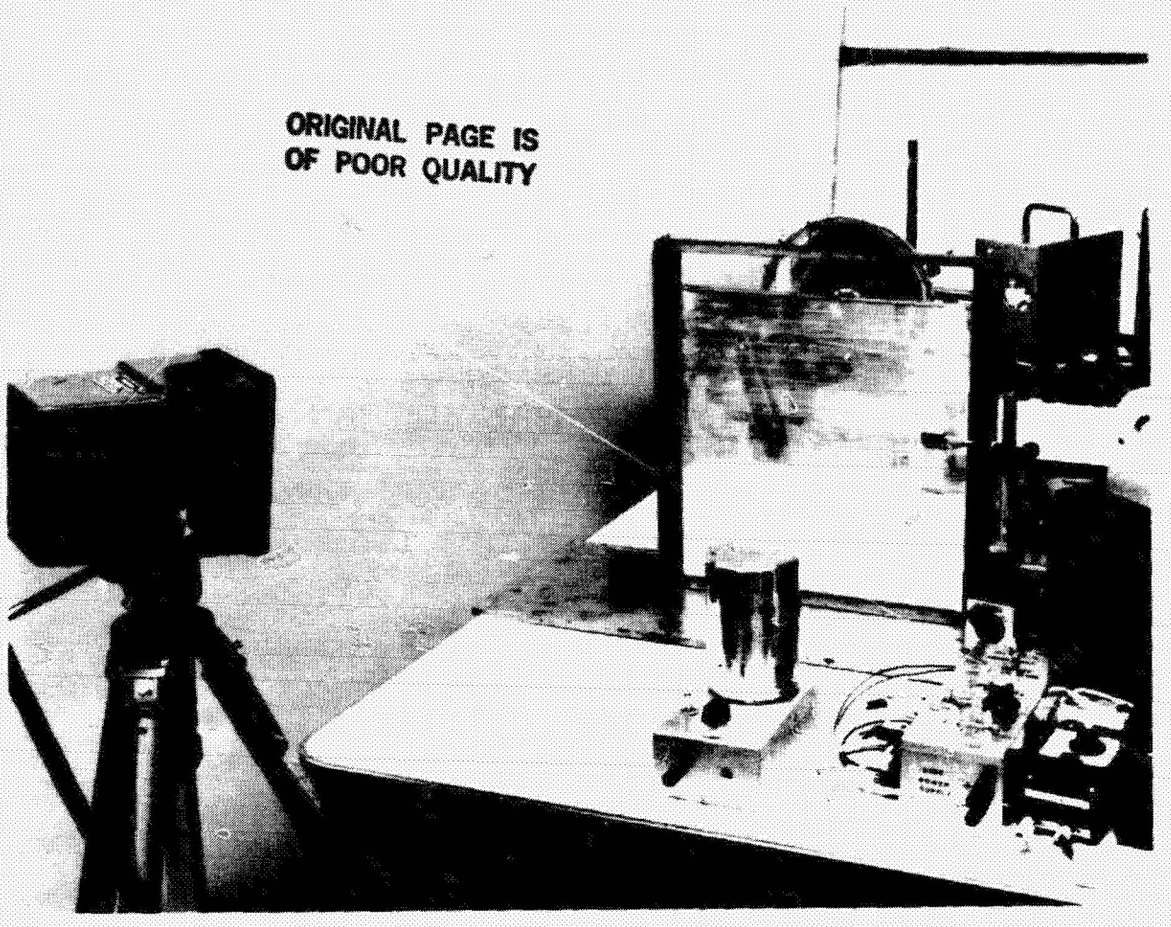


Figure 1. IR Camera and Module Test Setup

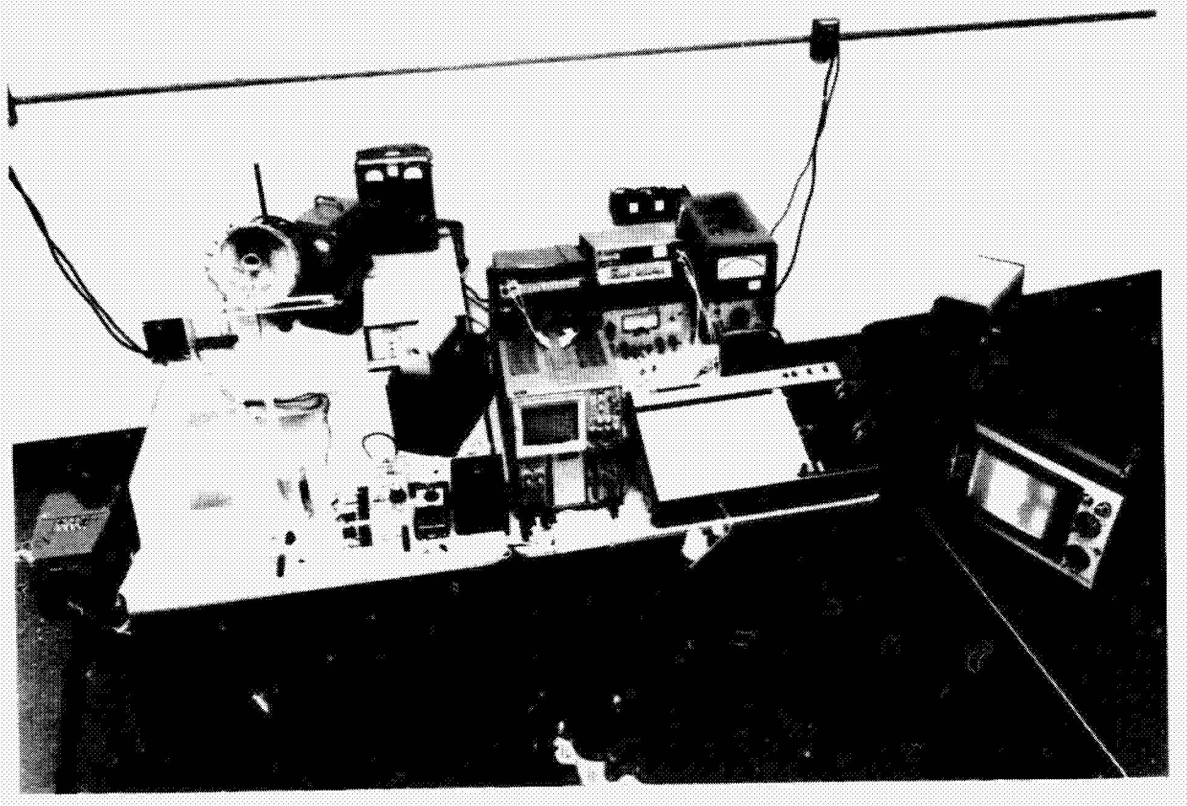


Figure 2. Hot-Spot Test Setup Including All Equipment Used

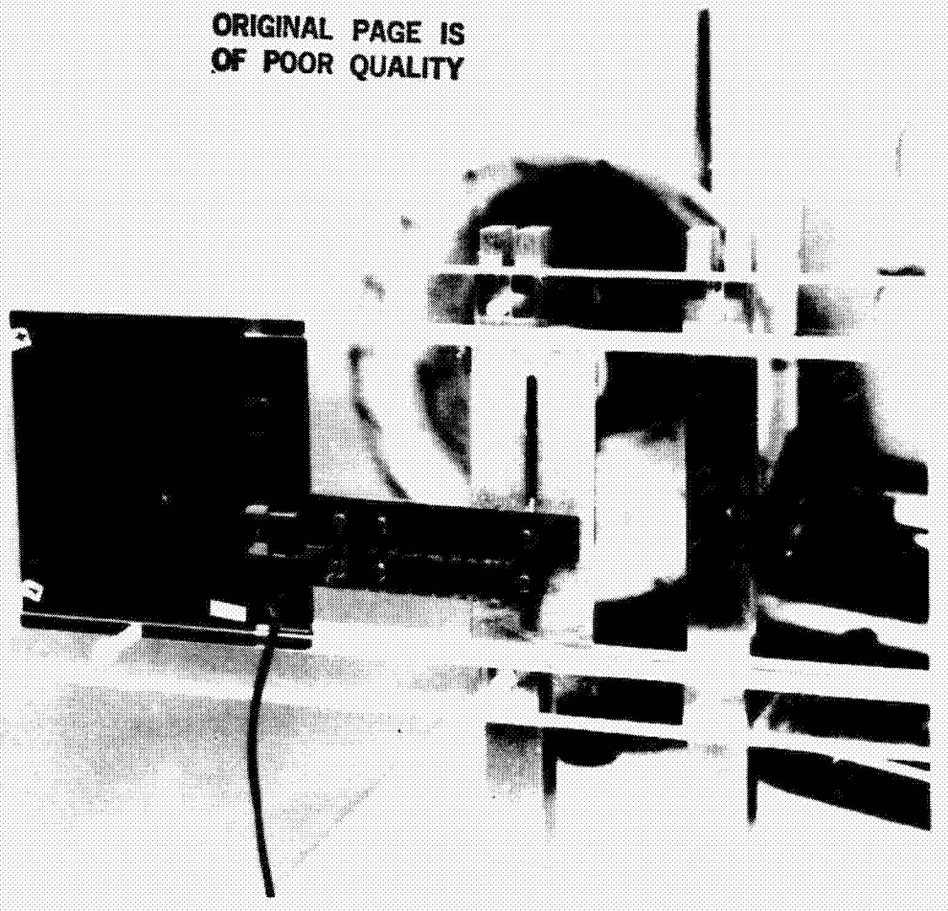


Figure 3. Test Setup Showing Submodule and Contacts Using Conductive Elastomeric Material

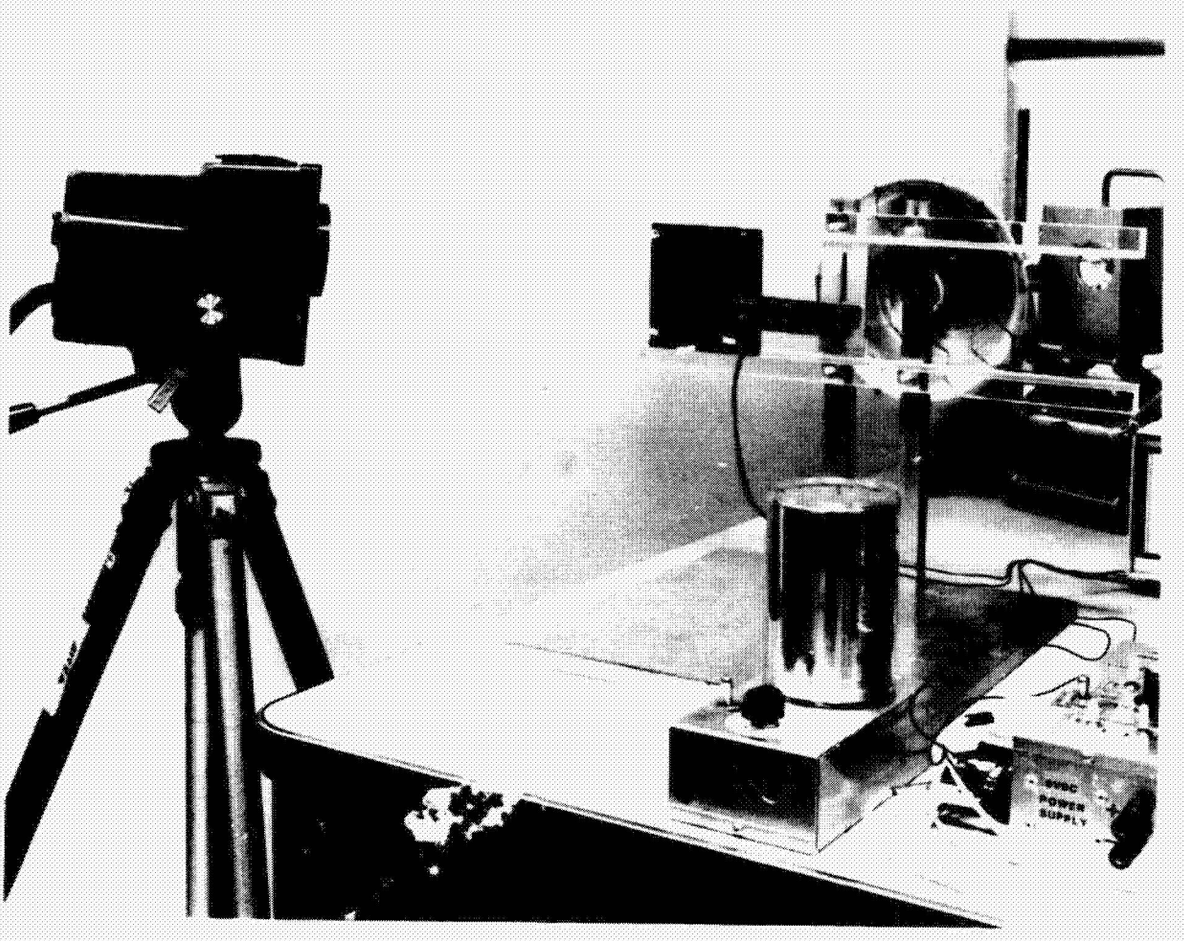



Figure 4. Infrared Camera with Submodule Test Setup

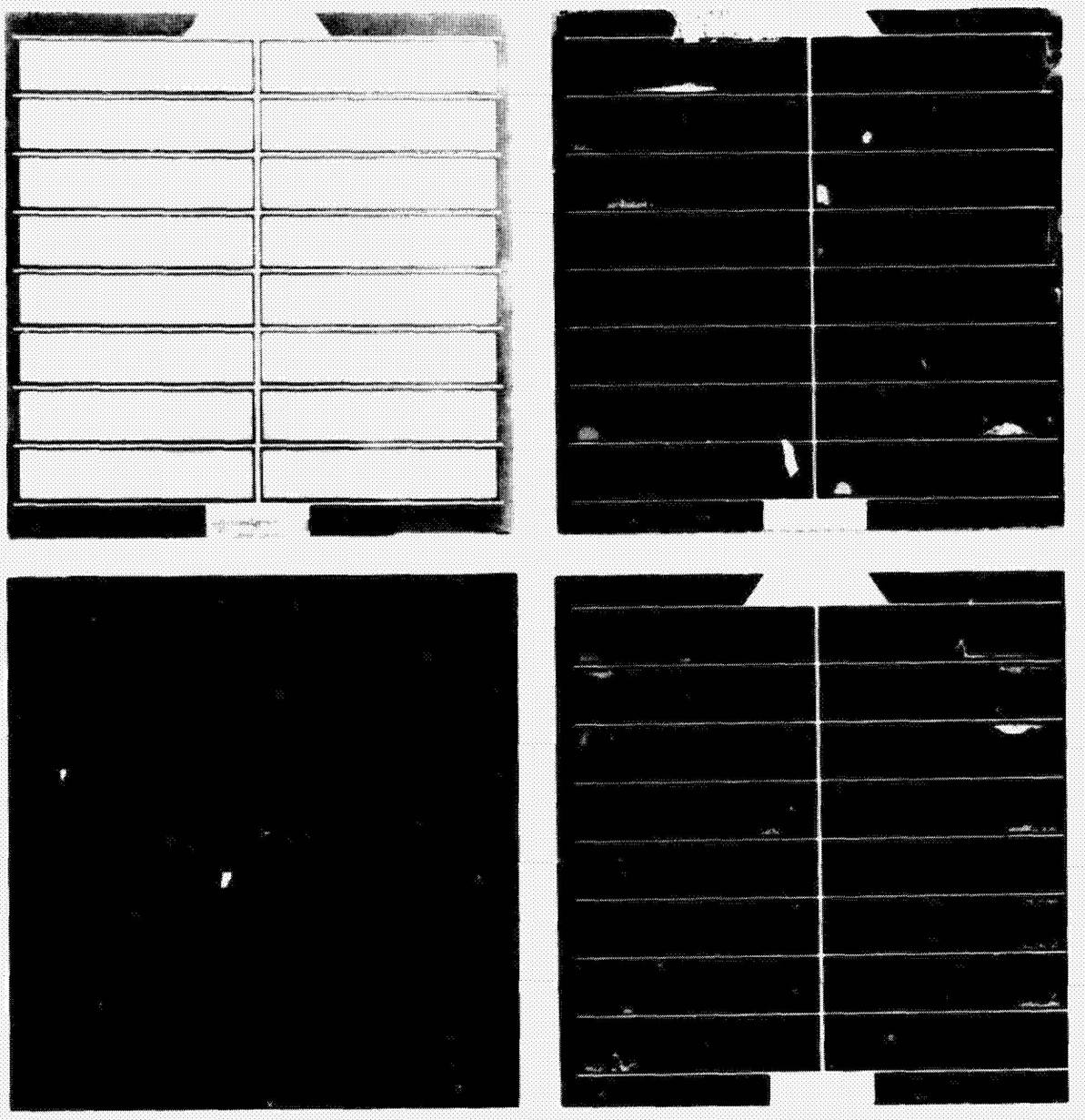


Figure 5. Submodules, Front and Back View, with Hot-Spot Erosion Shown

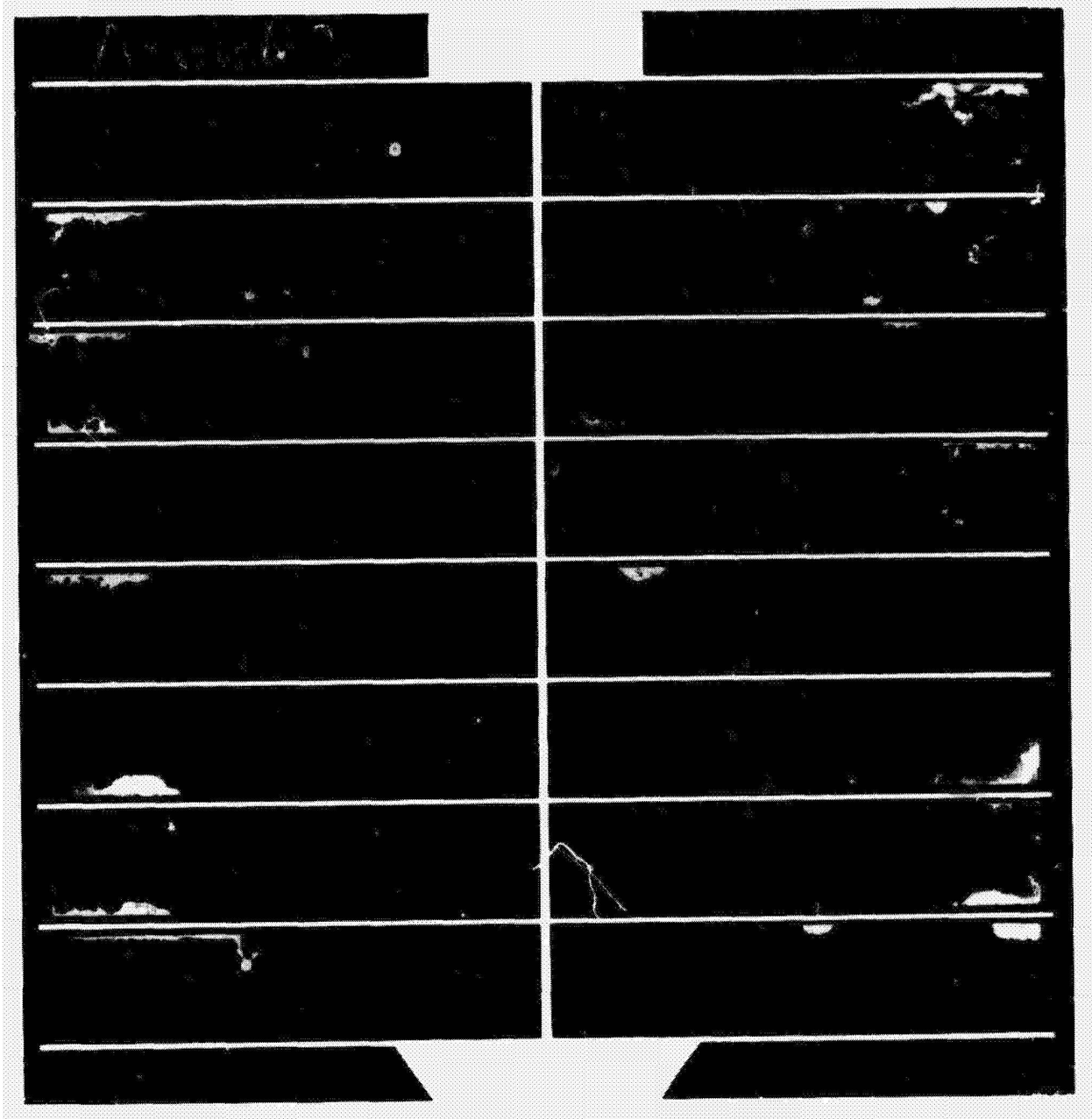


Figure 6. Close-up of Hot-Spot Erosion

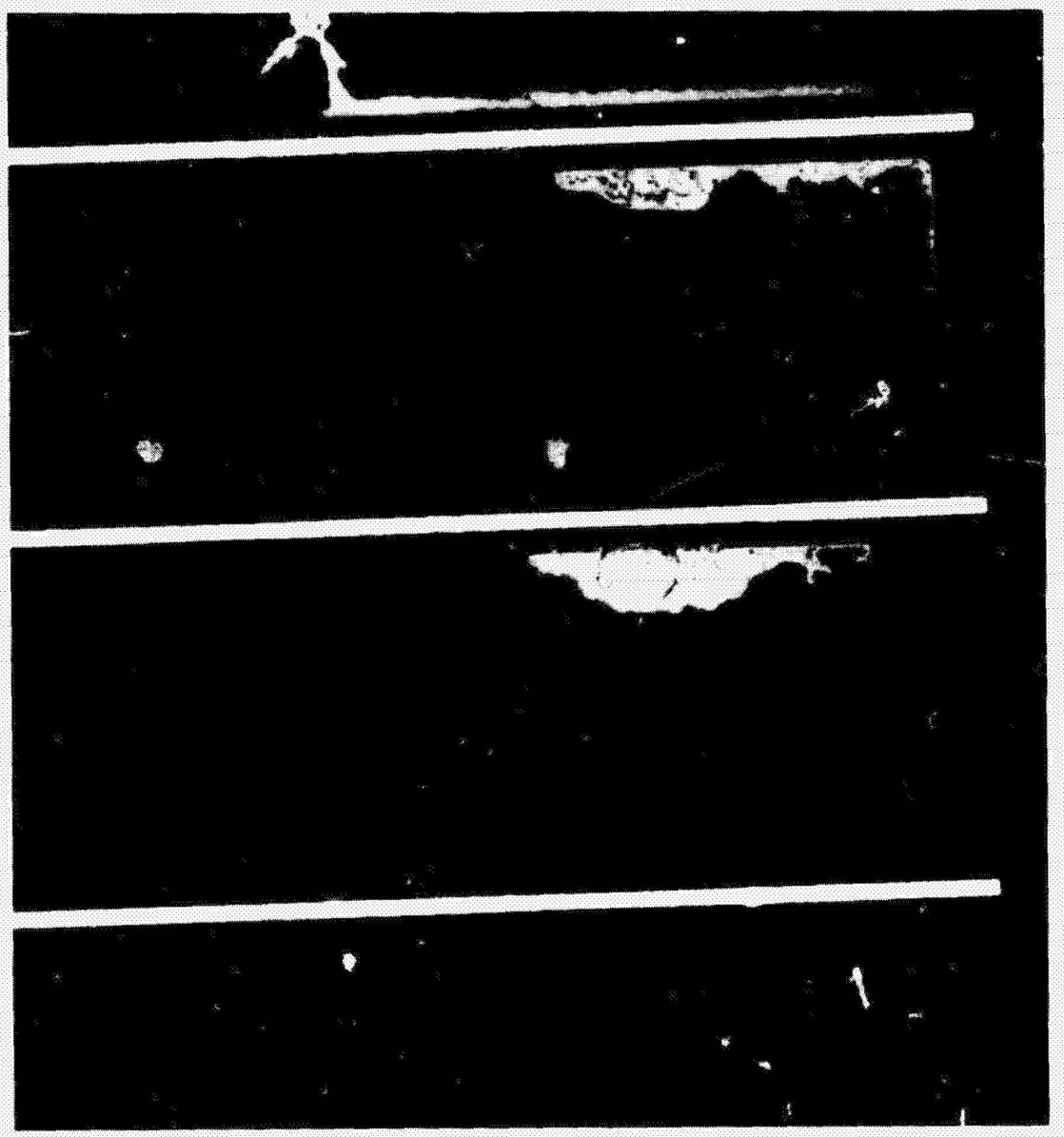
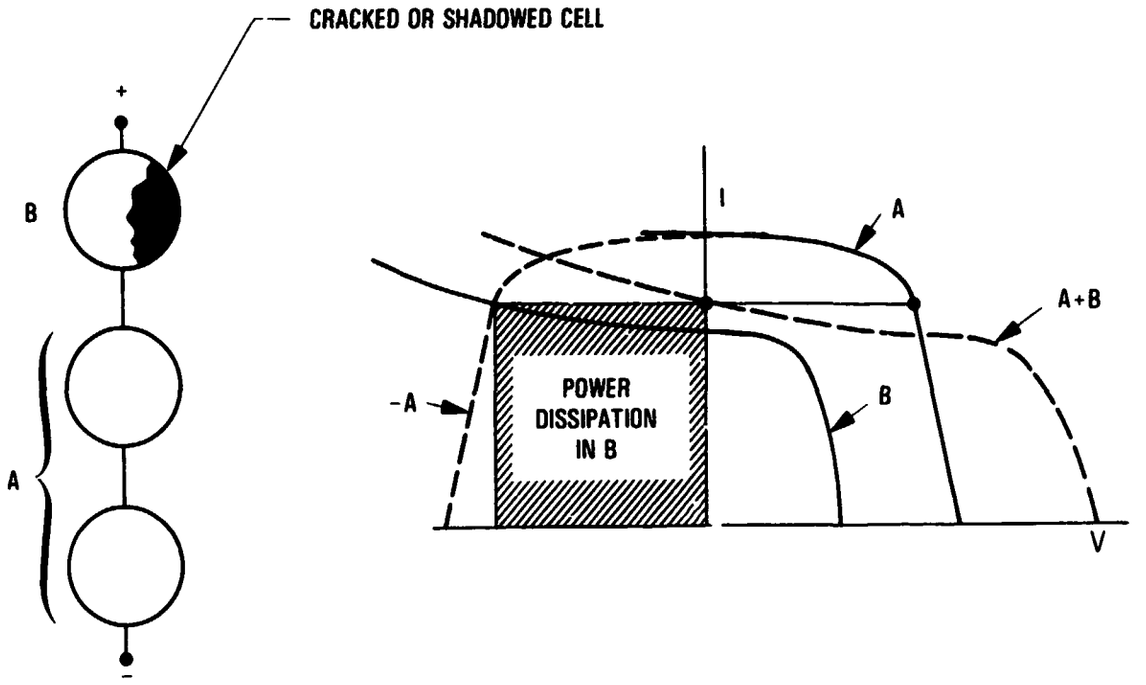
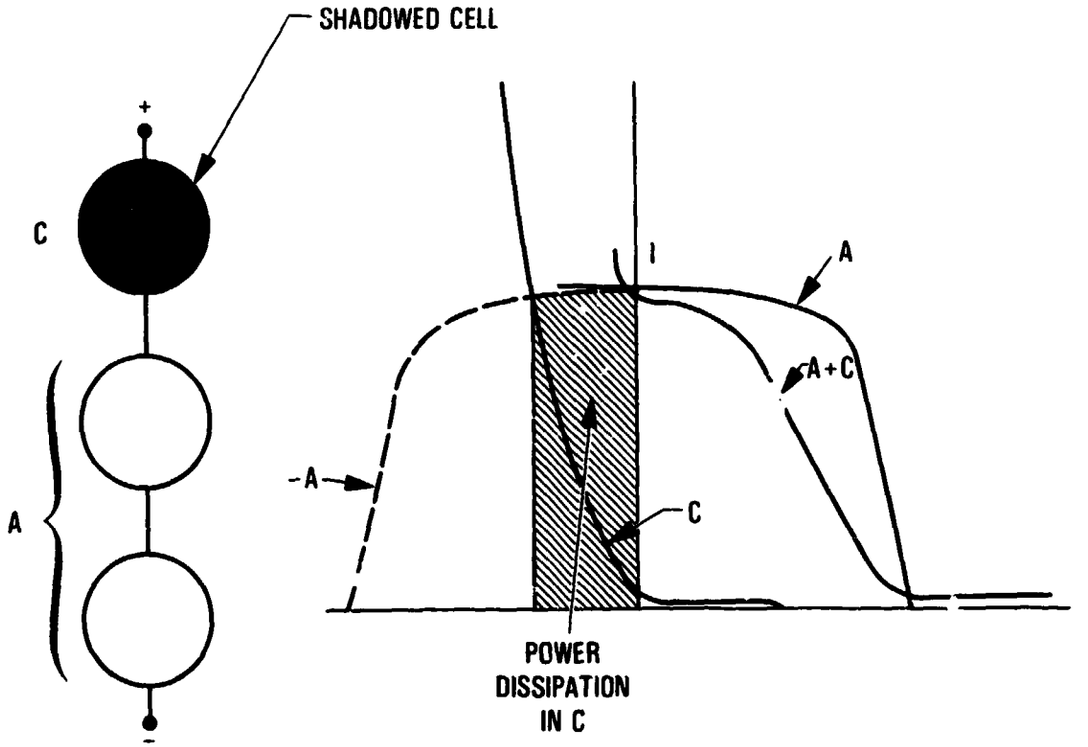


Figure 7. Close-up of Cell Erosion

# VISUALIZATION OF HOT-SPOT CELL HEATING WITH HIGH-SHUNT-RESISTANCE CELL

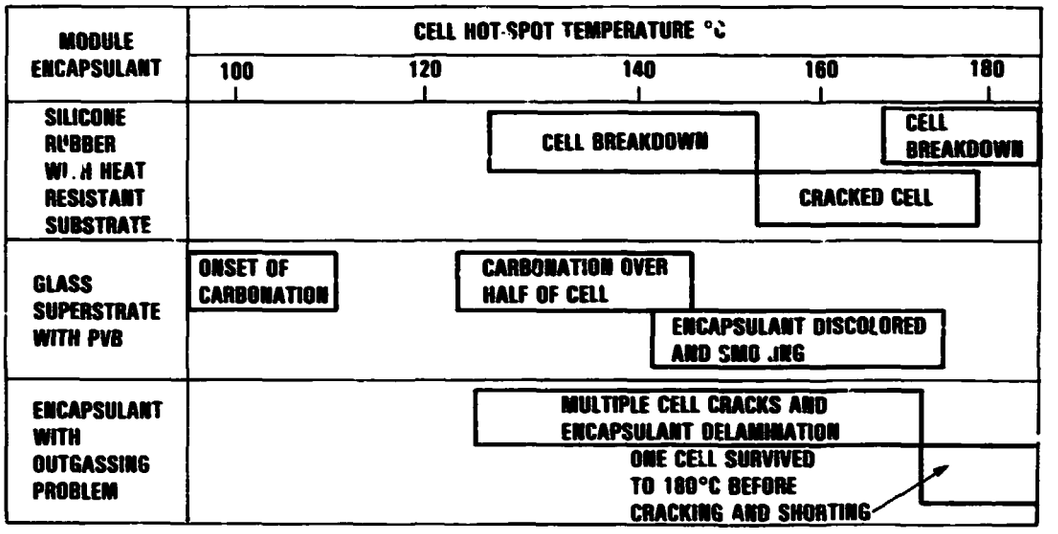


# VISUALIZATION OF HOT-SPOT CELL HEATING WITH LOW-SHUNT-RESISTANCE CELL



Flat-Plate Solar Array Project

# OBSERVED MODULE RESPONSE VS CELL TEMPERATURE



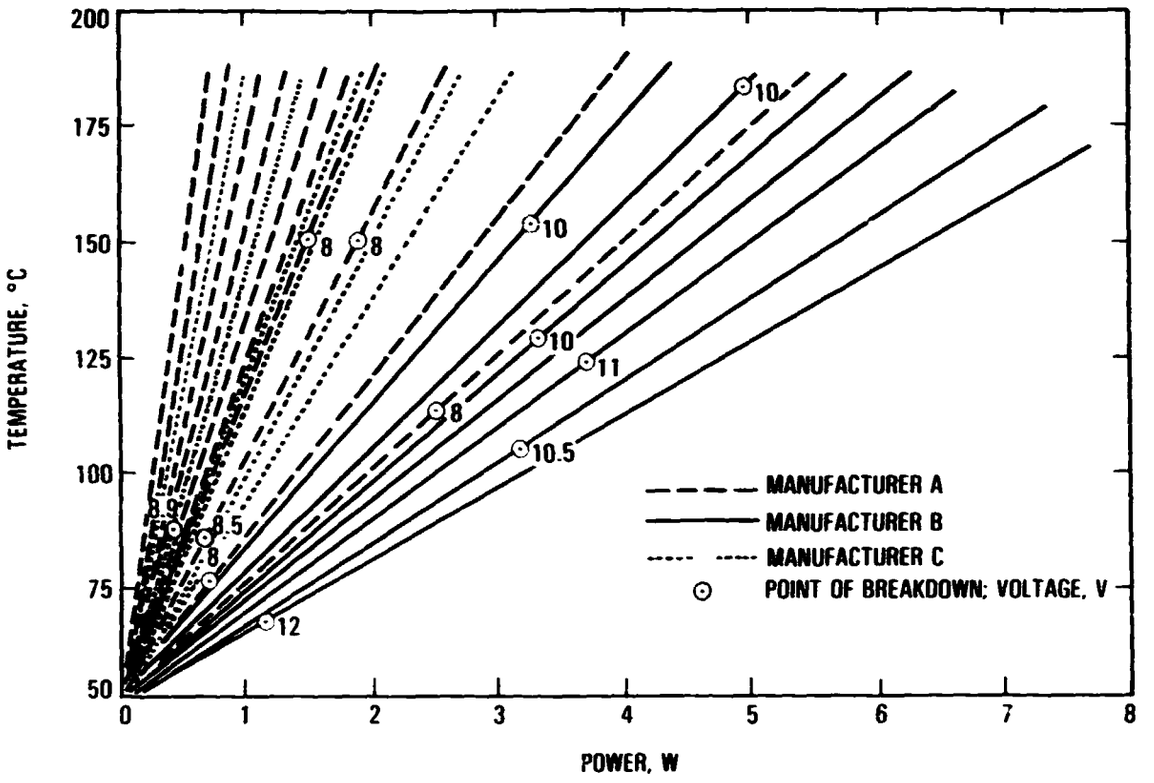

CONCLUSION:

- Hot-spot temperatures should be kept below approximately 120°C

Flat-Plate Solar Array Project

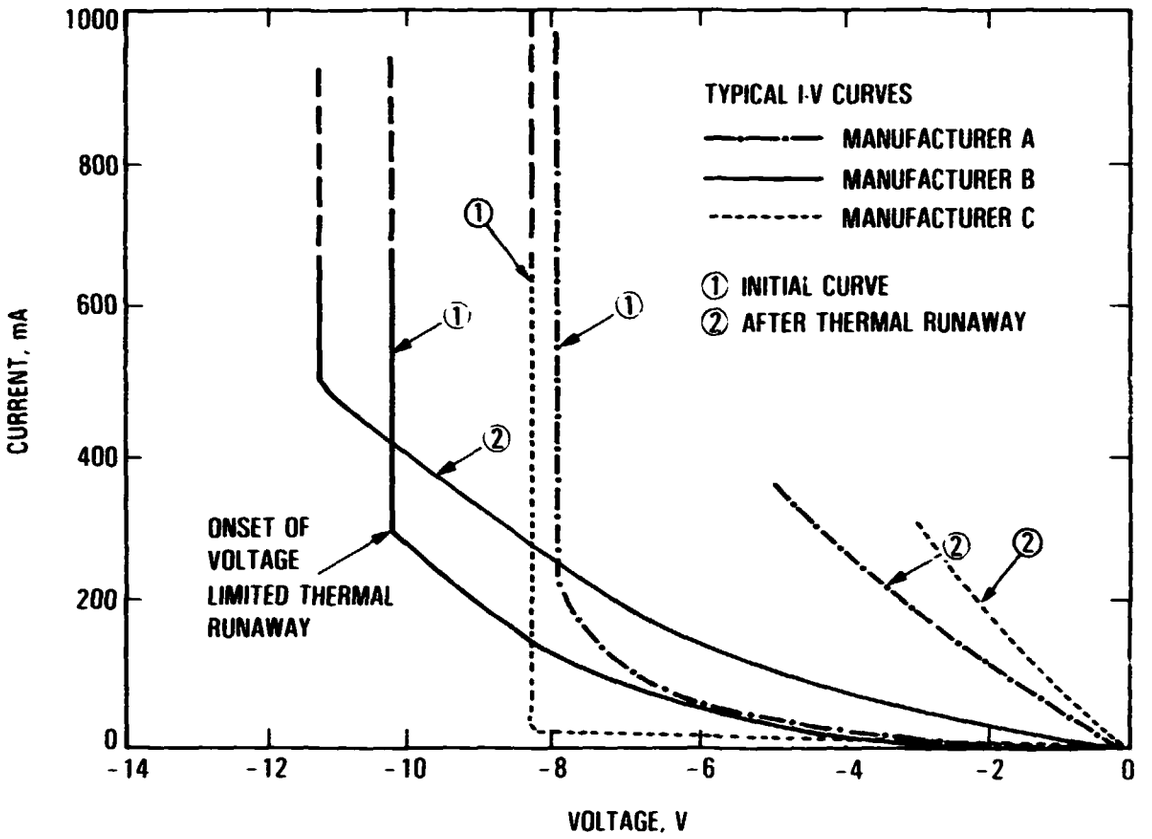
# HOT-SPOT TEMPERATURE VS POWER

## (UNENCAPSULATED *a*-Si SUBMODULES, NO ILLUMINATION)



Flat-Plate Solar Array Project

# AMORPHOUS-CELL REVERSE-QUADRANT I-V CURVES



## DISCUSSION

HARTMAN: Did you see any cells repair themselves if you applied a pulse?

GONZALEZ: We have seen some of that in the pulse testing. That's the only test where we did any front-quadrant I-V curves. We have seen some strange changes in those I-V curves, changes that occur when you just let the cell sit for a while and then continue to test. After it gets a pulse sometimes it gets better. Yes, there are changes.

KNIAZZEK: Can you describe what the effects were that you showed photographs of? What was the morphological change that you photographed?

GONZALEZ: That, I can't get into in detail. You will have to talk to one of the cell manufacturers. The only thing I can see is that the entire material of the cell was eroded away like a volcanic eruption. If you look at the 200X picture -- it just kicked out of there. Now, what's happening actually in the cell I don't know, except that physically it is just being -- it just eroded it, just blew the stuff away.

TURNER: First of all, your concern that the test really should be done illuminated as opposed to in the dark is well warranted. Because it may turn out there is not a significant difference, but one of the significant differences between amorphous cells and crystalline cells is that superposition holds in crystalline cells, that is, their dark I-V curve can be translated to produce the light I-V curve, and that's in general not true of amorphous cells. It's quite a different device in the dark than it is in the light.

GONZALEZ: I didn't mean to imply that we are proposing doing them in the absence of illumination, just that we are trying to get a handle on what's going on and that was the starting point.

TURNER: I understand. You have to start someplace. question is, with the design of these modules, they are usua a very narrow cell and very wide. Or very short and very wide, if you like. The opportunity for causing shadowing would seem to be different -- I don't know how different -- than it is in the case of crystalline modules, which are blocks, and if you have a lion walking across it with muddy prints then he could cause problems. Well, that did happen at Mt. Laguna. I wonder if anybody has attacked the problem of the probability of occurrence of the kind of shadowing that might cause a problem? If, for example, you say the worst case is the one where a module might blow but what you have to do is to hold a pencil two-thirds of the way across one, and only one, cell in the proper orientation. Has anybody wrestled with that problem?

GONZALEZ: I refer you to the work we did about a year ago that Jim Arnett from ARCO was involved in, and that's with the SMUD arrays, where we looked at the types of shadows and what they would do, so some work has been done on that. Not for amorphous; I thought you meant that as a question in general.

TURNER: Particularly because of these modules, which would seem to be less susceptible, but it can be tricky; a telephone line could certainly cause complete shadow.

D5

N86-12764

# Accelerated Stress Testing of Thin Film Solar Cells -- Development of Test Methods and Preliminary Results

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## 1.0 INTRODUCTION

The reliability characteristics of solar cells intended for low-cost terrestrial applications, either central power generation or distributed residential usage, will be a key factor in determining the economic feasibility of such systems. Typical cost models are based on a 30-year module life, which is generally accepted to mean that the power output of an array should not decrease by more than 10% during this period. The achievement of such a degree of system reliability requires the use of very stable cells. Clemson University, under JPL sponsorship, has had a program to assess the relative reliability attributes of silicon solar cell technologies through laboratory accelerated stress testing since 1977. Much information has been gathered on crystalline cells whose starting material was produced by a variety of techniques -- Czochralski, EFG, dendritic, and HEM. Recently attention has turned to thin film technology and this paper discusses the methodology of using accelerated testing to evaluate the reliability attributes of this type of cell. In this paper necessary conditions for initiating a comprehensive thin film test program including test samples, accelerating stresses, and electrical measurement techniques are discussed and some preliminary test results related to commercial a-Si cells are given.

Accelerated test methodology involves subjecting cells to stresses higher than normally encountered in hopes that naturally occurring degradation mechanisms, which might take years to detect in the field, can be detected in the laboratory within days or weeks. Cells are initially visually inspected and electrically measured, subjected to the desired level of stress, and then measured and inspected again. Changes which occur can then be assumed to be due to the effect of stress and through analysis of the observed degradation related to fundamental physical, chemical, or metallurgical changes. In this way accelerated stress testing can be used to uncover potential failure mechanisms in a relatively short period of time, permitting preventative measures to be taken.

For accelerated testing to provide useful results, however, three conditions must be met: 1) the samples being stressed must be representative of the manufactured population, 2) a stress window must exist, and 3) the measurement methods used must have a sufficient degree of repeatability. Each of these points will be discussed in detail as it pertains to the stress testing of thin film cells.

## 2.0 TEST SAMPLE CONSIDERATIONS

Thin film modules are fabricated monolithically, i.e. a number of interconnected cells are fabricated simultaneously on a single substrate or superstrate. Stress testing, however, is most effective when it seeks to examine the effect of stress on each individual cell rather than a complete module, since not every cell will be affected equally by the stress. This requirement for individually addressable cells means that in contrast to single crystal cells, where test samples could be taken directly from a manufacturer's current production prior to assembly and encapsulation, special test vehicles will need to be manufactured specifically for the purpose of accelerated testing.

These specially made test vehicles should be as nearly identical as possible to the monolithic structure, however. They should have the same composition of materials and be processed in the same way. The test vehicles should include simulated interconnects so the effect of stress on the metal interfaces can be examined. The role played by encapsulation is not at all clear in thin film cells, but because thin films are obviously subject to more rapid degradation through corrosive and dissolution effects than the thicker layers of crystalline cells, encapsulation can be expected to strongly influence a cells response to accelerated testing.

Finally an assurred source of test samples representing state-of-the-art technology is required. The great value of crystalline cell testing was its ability to compare the reliability attributes of material and processing changes as they developed. Becuase of reasons stated above, the regular availability of 100-quantity lots of test samples will require considerably greater dedication to accelerated testing on the part of manufacturers than was the case for crystalline cells.

## 3.0 STRESS WINDOW AVAILABILITY

As noted above, the amount of stress applied to a cell must be sufficient to provide considerable acceleration of the degradation mechanism over that which occurs in real time. Typically one would like to achieve at least an acceleration factor of 100. With an acceleration factor of 100, effects occurring in 30 years will be observed to have the same magnitude in approximately 100 days. Determination of actual values of acceleration factors, in general, is difficult, but for the case of those degradation mechanisms which are a function of temperature only it is possible to use the Arrhenius equation to establish a relationship between high temperature stress and room temperature stress. Under these conditions the acceleration factor will depend on an activation energy as well as temperature. A mechanism with a high activation energy will have a much higher acceleration factor for a given temperature, as shown in the accompanying viewgraph. Most common degradation mechanism have activation energies between 0.4 and 0.7 eV.

In an effort to achieve a high acceleration factor, or at any rate one which is at least 100, the tendency is to increase the stress temperature. This can only be done within limits, however, since certain thresholds may be exceeded at sufficiently high temperatures as to introduce new failure modes which did not occur at lower temperatures. An example of this behavior would

be the change of phase of a material, such as solder melting. The metallurgical leaching aspects of molten solder are completely different from the diffusion characteristics of solid solder. Consequently Arrhenius extrapolation is no longer possible when thresholds such as this are exceeded. The introduction of new failure mechanisms, in effect, places an upper limit on the magnitude of the accelerating stress which may be used. Thus the combination of minimum acceleration factor and maximum stress results a test "window" for some activation energies and not for others. In the graphical example shown in the viewgraph, where a minimum acceleration factor of 100 and a maximum temperature of 140 C were assumed, a window ot testability can be seen to exist for an activation energy of 0.5 eV, but not for 0.4 eV.

Because there is no extensive history of accelerated testing on thin film cells, activation energies have not been determined and little is known concerning the existence of phenomenological thresholds which will limit stress. One technique for determining the upper stress limits for accelerated testing is to perform step stress testing. In step stress testing samples are consecutively subjected for equal lengths of time (steps) to ever increasing stress levels. It is possible to select the stress level magnitudes and times such that there will be little cumulative effect. Consequently a sudden change in the amount of degradation from one level to the next signals the existance of a phenomenological threshold and accelerated testing should only be performed at lower levels of stress. A classic example of this type of behavior was observed when some unencapsulated a:Si cells were subjected to unbiased temperature step stress testing as shown in the accompanying viewgraph. Obviously the threshold occurred between 130 and 140 C. Further work will be needed to determine the cause of this threshold.

## 4.0 MEASUREMENT REPEATABILITY

The ability to make repeatable electrical measurements days, weeks, and months apart is essential to an accelerated test program. The greater the repeatability of the measurement instrumentation the smaller the changes which are able to be detected, and consequently the shorter the acceleration time that is needed to induce degradation. Measurement repeatability necessitates being able to accurately reproduce after stress the same temperature, contact, and illumination conditions that existed before stress.

Cell temperature control requires use of a shuttered light source combined with rapid data acquisition so that the temperature of the cell will not be influenced by its illumination. A constant flow of temperature controlled air is used to precondition the cells prior to illumination. Cell contacts should be of the Kelvin type with separate current carrying and voltage sensing contacts to eliminate the effect of varying contact resistance. Thin film cells do not have soldered leads attached, as was the case for crystalline cells, so pressure contacts must be made directly to the thin conductive films. Metal spring contacts tend to scratch the films so that the measurement process itself will introduce degradation. It has been found that conductive, elastic rfi gasket material is an excellent non-damaging contact material, particularly when jigs are designed so that conduction is across the width of the gasket rather than along its length.

Under the Clemson-JPL contract, a short interval measurement system,

embodying the Kelvin contact and temperature control principles mentioned above, was developed for characterizing crystalline cells up to 4-inches in diameter. This instrument, which has proven in practice to be repeatable to within 1%, cannot be used directly for a:Si cells because of the difficulty in reproducibly setting illumination levels over extended periods. This is due to the fact that ELH simulator lamps tend to change their spectral characteristics over time and stable, spectrally appropriate thin film reference cells are not available for adjusting the lamps' intensity, as was the case for crystalline cells. Various approaches are being followed in a number of different laboratories which will permit the simulation of thin film spectral characteristics using stable silicon cells. The ability to make accurate accelerated stress test measurements will need to await the outcome of this development effort.

At the present time accelerated test measurement data at Clemson is obtained by digitizing cells' IV characteristics and storing this information on floppy disks. It was found in measuring crystalline cells that valuable information concerning degradation mechanisms could be obtained from the shape of the characteristic in all three quadrants (reverse, power, and far-forward). The amount of data necessary for the complete comparison of before and after stress characteristics can quickly mount up, even for a modest test program. For some time reduced data quantities have been used in an effort to simplify this comparison and perhaps ultimately eliminate the need for ever increasing amounts of storage. The reduced parameters now being collected are Voc, Isc, Pm, Vm, and Im. Modelling work has indicated that the addition of the parameters Rs (series resistance), Rsh (shunt resistance), Io (effective diode leakage current), and n (diode ideality factor) will permit reasonably accurate modelling of the shape of the IV characteristic, at least in the power quadrant. Consequently effort is underway to automatically acquire these paramters and eliminate the need to store individual data points. Standard statistical packages are available which permit the statistical analysis of these reduced data parameters.

## 5.0 PRELIMINARY RESULTS

A comprehensive accelerated stress test program for thin film cells has not as yet been started. Initiation of such a program is dependent on successful completion of the steps outlined above, particularly the availability of an assurred supply of representative state-of-the-art cell test structures. Consequently very little data is available at this time, but some preliminary measurements are underway in an effort to define an appropriate test schedule for a:Si cells. The test schedule which has been utilized in the past for crystalline cells is shown in the accompanying view graph and, while this schedule will need to be modified for a:Si and other types of thin film cells, it can serve as a point of departure for these initial investigations.

Having acquired a number of individually addressable, but unencapsulated a:Si cells, which were fabricated in multiples of 16 on a common superstrate, the first step was to subject them to unbiased step stress testing. This resulted in the data mentioned earlier which indicated a threshold effect occurring between 130 and 140 C. A crystalline reference cell was used for these measurements, which implies that measurement errors of a few percent were superimposed on the stress related changes, but nevertheless the data

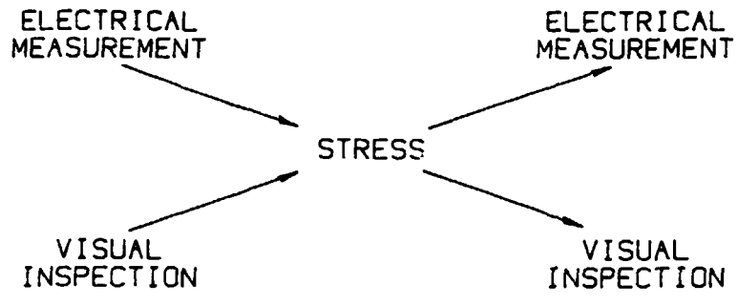
obviously supports the existance of a stress related transition temperature. It is not known at this time, however, if the transition temperature applies only to this type of cell construction or the reason for its existance.

In order to investigate the effect of high humidity on these cells a subgroup of 16 cells was subjected to the standard 85/85 test (85 C and 85% relative humidity). Initial measurement indicated that the cells could be divided into two classes -- "good" and "poor" -- on the basis of their power output. Good cells had relatively rectangular IV characteristics (good fill factors) with Pmax in excess of 20 milliwatts, while poor cells had Pmax less than 20 milliwatts. Thus far, data has been collected after 200 and 400 total stress hours with results as shown in the accompanying viewgraph. The two classes of cells behaved quite differently. During the first stress period the maximum power output of the poor cells increased by more than 50%, on the average, with only a slight further increase being observed during the second stress period, while the poor cells showed a slight decrease in Pmax after both stress levels. As shown in the viewgraph, poor cell improvement was accompanied by increases in Voc and FF, but not Isc. This test is continuing. More work will need to be done to define the degradation mechanism, but one phenomenon that will certainly be investigated is hydrogenation as a result of water vapor dissociation at the aluminum back contact.

As a second experiment to investigate the effect of high humidity, another group of 16 a:Si cells was subjected to pressure cooker stress (121 C, 15 psig H20) for 25 hours, the minimum stress time in the crystalline cell schedule. Physical examination of the stressed cells indicated that most of the metallization and much of the silicon had been removed, although the ITO layer appeared to have remained in place. Obviously this length of stress was much too long for unprotected thin film cells. Next a second group of 16 cells was subjected to 1 hour of pressure cooker testing. Results closely paralleled the 85/85 tests described above, with good cells showing degradation and poor cells showing improvement. This test is now being extended to longer stress times.

## 6.0 SUMMARY

It is clear that if thin film cells are to be considered a viable option for terrestrial power generation their reliability attributes will need to be explored and confidence in their stability obtained through accelerated testing. Development of a thin film accelerated test program will be more difficult than was the case for crystalline cells because of the monolithic construction nature of the cells. Specially constructed test samples will need to be fabricated, requiring committment to the concept of accelerated testing by the manufacturers. A new test schedule appropriate to thin film cells will need to be developed which will be different from that used in connection with crystalline cells. Preliminary work has been started to seek thin film schedule variations to two of the simplest tests: unbiased temperature and unbiased temperature-humidity. Still to be examined are tests which involve the passage of current during temperature and/or humidity stress, either by biasing in the forward (or reverse) directions or by the application of light during stress. Investigation of these current (voltage) accelerated tests will involve development of methods of reliably contacting the thin conductive films during stress -- a potentially difficult task.

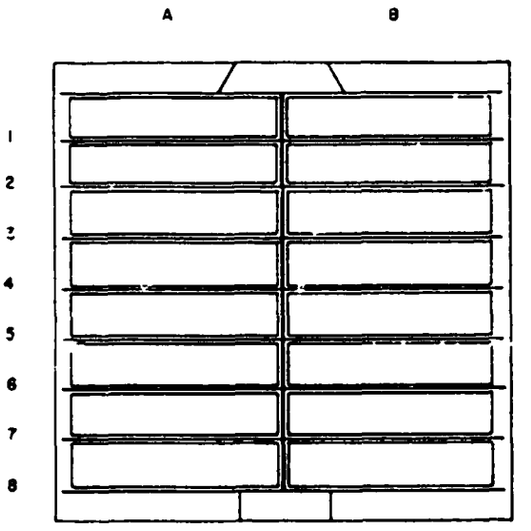



- REPRESENTATIVE SAMPLES
- STRESS WINDOW
- MEASUREMENT REPEATABILITY

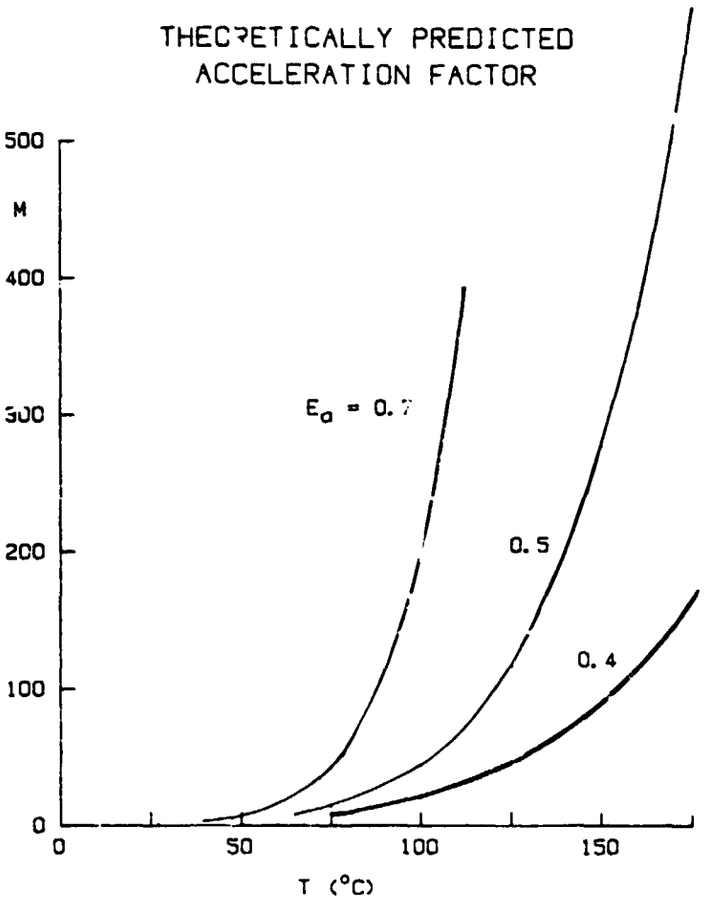
ACCELERATED STRESS METHODOLOGY
AND NECESSARY REQUIREMENTS

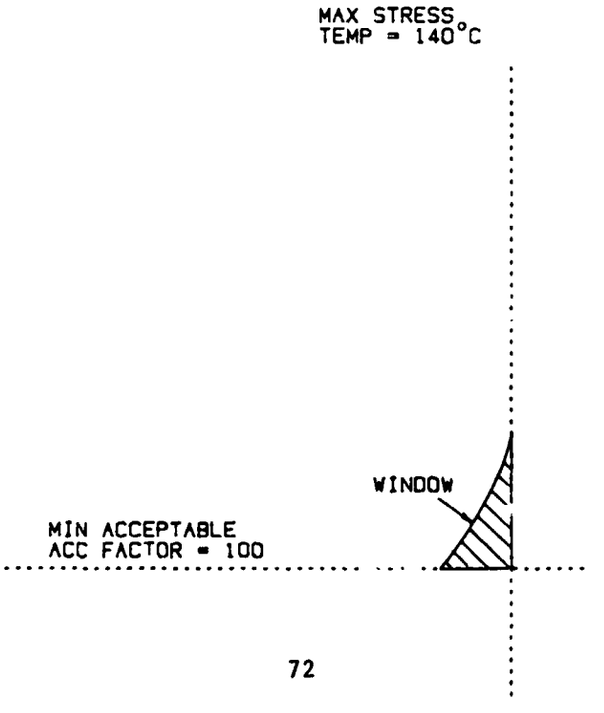
- TEMPERATURE CONTROL
  - SHUTTERED LIGHT
  - CONSTANT TEMP AIR FLOW
- REPRODUCIBLE ILLUMINATION
  - REFERENCE CELL
  - AREA UNIFORMITY
- KELVIN CONTACTS
  - ELASTIC CONTACTS
- DIGITIZED DATA
  - 3-QUADRANT CHARACTERIZATION
  - $V_{OC}$. $I_{SC}$. $P_M$. $V_M$. $I_M$
  - $R_S$. $R_{SH}$. $I_O$. $n$

ACCELERATED STRESS TESTING
MEASUREMENT CONSIDERATIONS




CONTACT LAYOUT FOR INDIVIDUALLY ADDRESSABLE a:Si TEST STRUCTURE

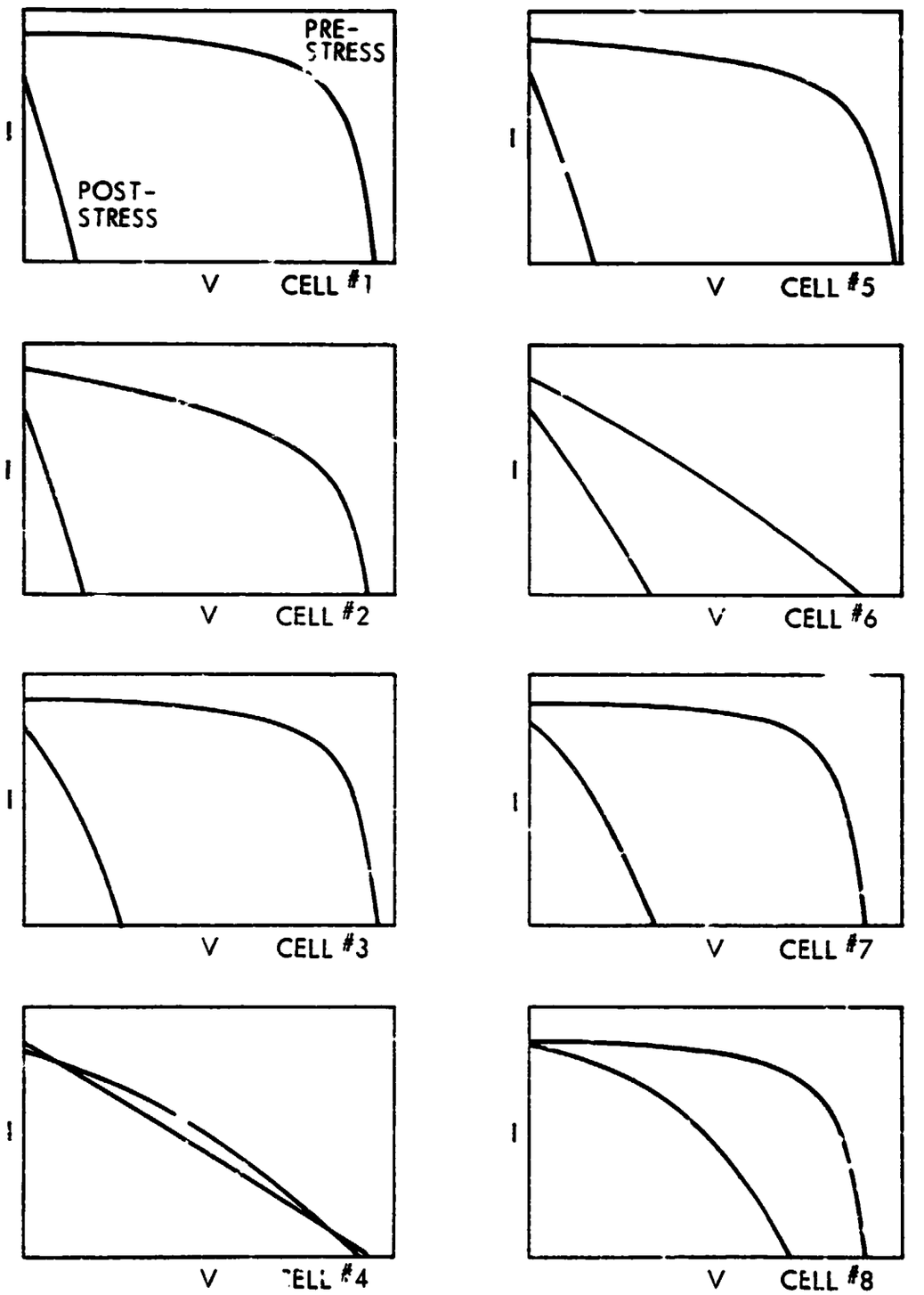

THEORETICALLY PREDICTED
ACCELERATION FACTOR
500
M
400
300
200
100
0
$E_a$ = 0.7
0.5
0.4
0
50
100
150
T (°C)

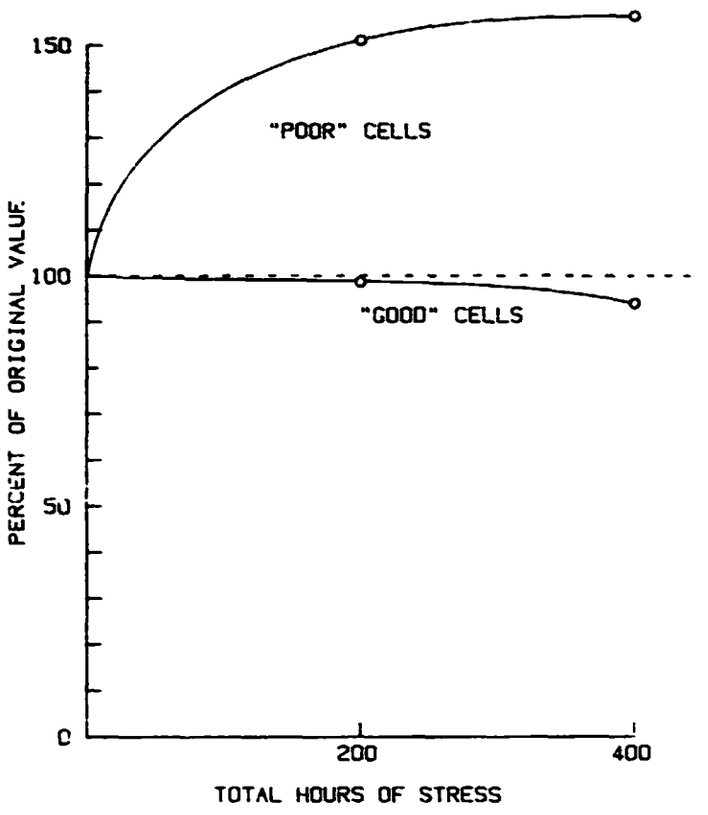

MAX STRESS
TEMP = 140°C
WINDOW
MIN ACCEPTABLE
ACC FACTOR = 100

TYPE OF a-Si CELL DEGRADATION BEING OBSERVED

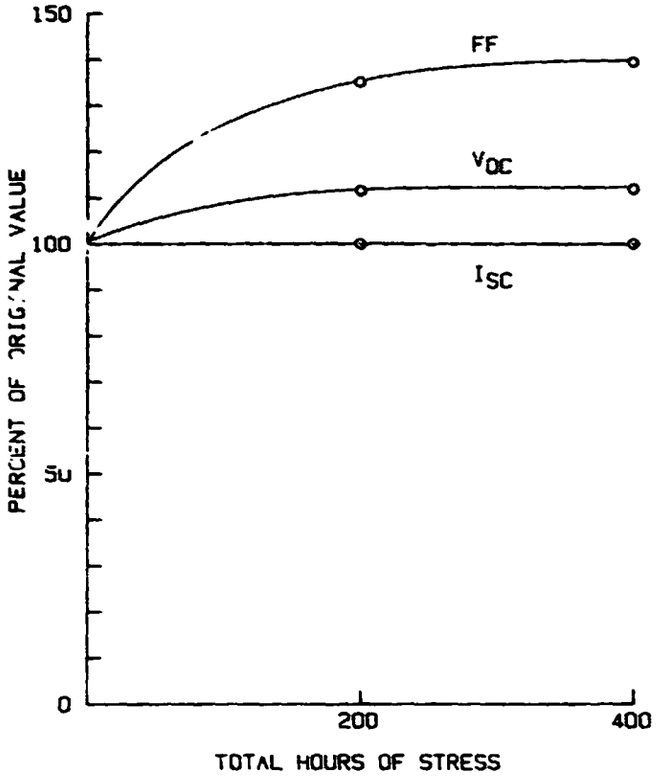
(20 HOURS AT 140 °C, OPEN CIRCUIT)

IV CURVES: PRE-STRESS AND POST-STRESS (8 a-Si CELLS IN ONE SUBMODULE)






NORMALIZED $P_M$ AS A FUNCTION OF 85/85 STRESS TIME FOR a-Si SOLAR CELLS




NORMALIZED $I_{SC}$, $V_{OC}$, AND FF AS A FUNCTION
OF 85/85 STRESS TIME FOR "POOR" a-Si SOL CELLS

## DISCUSSION

SULLIVAN: With the actual increases in performances seen in the 85/85 environment, I assume the samples were removed from the environment and allowed to dry out for a certain period of time, or something like that. You tested an hour or so after you pulled them out of the chamber?

LATHROP: Yes. I don't know that we considered this critical, and we probably did not time it. But the test devices were taken out, and then within a reasonable time measured; I don't know what it is.

WRONSKI: Did the improvements deteriorate, just on standing, afterwards?

LATHROP: We did not measure that. We just measured them and stuck them back in the system, in the 85/85 chamber.

WRONSKI: I see. It would be interesting -- maybe it was an improvement.

LATHROP: That is a very good comment.

JESTER: For instance when you showed the 130°? I really didn't understand if you had humidity in that exposure?

LATHROP: That was just room ambient humidity. We could see a slight change in color. It was enough so that if you knew what you were looking for you could see it in a 35 mm slide, but, if I were to put it up here and show you, quickly, you might not detect it. We saw a very slight change -- no change in the contacts at all, however, that we could see, but a change in the color of the silicon.

VASEASHTA: Did you also run the spectral response to see which portion of the spectrum it degrades in?

LATHROP: No, we have not done that, but that would be an excellent thing to do. We need to do that.

LESK: It looks like in some of those, you removed a very bad shunt. Do you think this might become part of the manufacturing process?

(LAUGHTER)

LATHROP: I rather doubt it. I think it is too expensive in terms of time and all that kind of thing -- that is, burn-in. On the other hand, I have heard people discuss that -- upon certain kinds of stress they see modules improve, when you look at the overall module. What may be occurring there is that the bad cells in the module are getting better, and the good ones in the module are not getting any worse. This may occur. This is a different situation from what we see in crystalline cells, where you pick and choose and

you select and you start out with things that are already pretty uniform. In fact, when we get cells from the manufacturers, they are very close to being identical. Here we see cells that are very, very different. This may be a thing in the manufacture of these modules that is going to cause some concern.

ARNETT: Making sure I understand, in the data that you are showing us: you seem to be using the step test, where you are proceeding from step to step with increasing temperature to establish the point at which you begin to introduce new mechanisms. It is not clear from what you have told me that you wouldn't have seen the same thing that you saw as the normal means of failure if you had not continued for a longer period of time at one of the lower temperatures. Do you have data to show that the mechanism you are using to say that 130° is the maximum temperature you can use because it is a new mechanism -- do you have data that says that is the case, or is it something you would actually have seen if you just continued these other tests for a longer period of time? I'm not convinced that what you saw is a different failure mode.

LATHROP: I see what you are saying, but where it is just a relatively short time but quite a large temperature difference, namely 10°, if you look at the Arrhenius extrapolation of this you would not expect to see any effect of the previous stressing. In other words, the cumulative effect of the stresses up to 130°C -- prior to 130°C would be negligible compared with a 130°C step -- because of a consideration of time and temperature. I think that on these grounds my inclination is to say that it is a mechanism which is suddenly occurring. We have run some limited tests: we put them in ovens directly at 140°C, and zap, they go bad and we put them in lower temperatures and they haven't gone bad within the times that we have run. It is, in my thinking -- at least, it is a semi-valid sort of thing; we don't have much data on it, though, -- that it's possible there is a cumulative affect.

GAY: My only comment is one of caution about too rigorously associating interpretation of the results at 130°C, because modules are laminated at 150°C.

LATHROP: Right, but they are not laminated for 20 hours or so. Nevertheless, your point is well taken. This was one module that we used. Maybe that module is unique; it was from one manufacturer. Maybe that process on these modules was unique. I am just saying this is -- I am not trying to prove a point that there is an upper limit and one can run some fairly quick tests that allow you to see where that upper limit is. That's the only thing I am saying.

D6

N86-12765

# ELECTRICAL SAFETY REQUIREMENTS: IMPLICATIONS FOR THE MODULE DESIGNER

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## ABSTRACT

Commercial photovoltaic array installations, which include residential and intermediate applications, are subject to building and electrical codes and to product safety standards. The National Electrical Code (NEC) Article 690, titled "Solar Photovoltaic Systems," contains provisions defining acceptable levels of system safety and emphasizes the system design and its installation. The Underwriters Laboratories, Inc. (UL), document titled Proposed First Edition of the Standard for Flat-Plate Photovoltaic Modules and Panels, UL-1703, identifies module and panel construction requirements that ensure product safety. Together these documents describe requirements intended to minimize hazards such as shock and fire. Although initial focus of these requirements is on single-crystal silicon modules, they are generic in nature, and are equally applicable to high-voltage (>30 Vdc), multi-kilowatt, thin-film systems.

A major safety concern is insulation breakdowns within the module or array wiring system, or discontinuities within the electrical conductors. These failures can result in ground faults, in-circuit arcs, or exposure to hazardous electrical parts. Safety issues include:

Allowable construction practices: material temperature limitations, ampacity of current-carrying parts, compatibility of connection means with recognized wiring systems, spacing between uninsulated live parts, wiring compartment volume and construction, metallic coating thickness, edge sharpness, accessibility of live parts, and markings.

Electrical insulation system integrity and grounding requirements: leakage current levels, bonding path resistance, dielectric voltage withstand, inverse current overload, and continuity of grounding connection.

Environmental durability: pull test for leads or cables, push test, cut test, terminal torque test, impact test, exposure to water spray test, accelerated aging of gaskets and seals, temperature cycling test, humidity test, corrosive atmosphere test, hot-spot endurance test, flammability test, and mechanical loading test.

As in other electrical systems, safeguards that address these issues may be incorporated in the module, the installation, or both. These safety-related features are evaluated at the system level in terms of compliance with electrical codes, and at the component (module) level in terms of satisfying product safety standards. This overview presentation is intended to provide a basic understanding of the electrical safety implications for the module designer of thin-film modules.

## INTRODUCTION

The objective of this presentation is to provide a summary of safety requirements for thin-film modules intended for use in high-voltage ( 30 Vdc) systems. The focus is a basic understanding of the electrical safety implications for the designer of thin-film modules. The basis for examining appropriate safety design practices consists of two documents: the 1984 National Electrical Code (NEC) Article 690, "Solar Photovoltaic Systems" (Reference 1), which addresses safety issues at the system level, including system design and installation, and the unique characteristics of photovoltaic systems that could result in an unsafe installation; and the Underwriters Laboratories, Inc. (UL) document Proposed First Edition of the Standard for Flat-Plate Photovoltaic Modules and Panels, UL1703 (Reference 2), which addresses construction practices and electrical safety requirements at the module level, including product safety as related to the factory-built item.

## SYSTEM SAFETY CONCERNS

Certain unique electrical characteristics have resulted in the 1984 NEC addressing photovoltaics in a separate article. Since full system voltage is present at very low illumination levels, a shock hazard is present at all times, and unlike conventional power sources that can be turned off, the array is always "hot." This is illustrated in Figure 1, showing that the maximum open-circuit voltage exists even at very low levels of illumination. Additionally, since the short-circuit current is limited, the operation of overcurrent safety devices may be impaired. Note, in the same figure, that the short-circuit current is a function of illumination level, unlike conventional power sources that typically have infinite short-circuit current.

As in most electrical equipment, the identification of safety requirements begins at the system level with overall safety concerns that include: (1) protection of personnel and the prevention of electrical shock hazards; (2) protection of equipment by minimizing electrical stresses in the event of ground faults; and (3) protection against fire hazards from internally generated sources, such as overheated parts or arcing, and from externally generated sources, such as burning brands or the spread of flames.

The array safety philosophy is based on the concept of safety in depth: a primary protection scheme together with a number of redundant protection schemes that are compatible with the overall photovoltaic system design. The primary protection consists of the module and wiring insulation that isolates electrically active parts of the equipment and cables. In addition, several secondary protection schemes are employed, each independent of the primary scheme both in design and in function. Frame grounding, circuit grounding, ground-fault detection, and blocking diodes and overcurrent devices are typical examples of secondary schemes. The key element of this philosophy is that a single failure should not render both primary and backup schemes inoperable.

ISOLATION AND GROUNDING SAFETY CONCEPTS

Figure 2 represents an example of a photovoltaic system that incorporates this safety-in-depth philosophy. The diagram shows two parallel source circuits consisting of series-connected modules, each module mounted in a conductive frame. The module frames are bonded together and permanently attached to the frame structure ground in such a way that removal of a single module does not affect the integrity of the bonding path. Each source circuit has in series both a blocking diode and an overcurrent device (in this example, a fuse). One of the circuit conductors is grounded and the array circuit incorporates a ground-fault-detection system. The photovoltaic array is connected to a power conditioner (PC), whose case is grounded. The output of the PC is then connected to the load.

In the event of an insulation failure, each of the secondary protection schemes provides an additional, independent measure of protection.

Frame Grounding:

Protects against shock hazards associated with module frame members that have become energized by failure of the primary insulation system. It does not protect against direct contact with the circuit conductors.

The approach is to provide a low-resistance path to ground to conduct fault current and to maintain frames at close to ground potential (below shock hazard level: $\geq$30 Vdc and 1 mA).

Circuit Grounding:

Protects against excessive voltage stress on the primary insulation system. It also enables shock hazard protection if combined with a ground-fault-detection system.

The approach is to prevent the source circuit from floating to a high voltage with respect to ground by solidly grounding one of the array circuit conductors. Alternative approaches include: a center-tap ground that limits the maximum voltage stress to one-half the output voltage of the source circuit; or a resistance-to-ground that limits ground-fault currents to a safe value.

Ground-Fault Detection:

Protects against shock hazards associated with personal contact with system conductors. It may be used to protect equipment in conditions associated with arcing between system conductors and ground.

The approach is to install a sensor (such as a Hall effect device) that detects a current imbalance in the circuit conductors. An alternative approach is to sense the voltage drop across a resistor situated in the circuit ground path.

Blocking Diode and Overcurrent Device:

Protects against reverse current through modules during fault conditions.

The approach is to install a blocking diode to prevent other parallel source-circuit currents from entering the faulted source circuit. The overcurrent device, a fuse, provides additional protection in case of a shorted diode.

The purpose of this example is to illustrate that the module design must be compatible with the overall safety system configuration. For example, the module voltage-isolation capability is constrained by the system voltage, and not by the module voltage. In the source circuits shown in Figure 2, the modules physically connected near the circuit ground will experience voltage stresses equal to their module voltage, whereas the modules located near the blocking diode will experience voltage stresses equal to the system voltage, which could be many times higher than the module voltage. Additionally, it can be seen that the module reverse-current capability requirement is a function of the series fuse rating and not the short-circuit current of the module.

## MODULE ELECTRICAL INSULATION SYSTEM INTEGRITY AND GROUNDING REQUIREMENTS

Based on this need for compatibility between the module and the system configuration, product safety standard UL 1703 sets forth module and panel construction practices and electrical requirements to ensure product safety for the factory-built item. For convenience in presentation, the requirements have been classified into three categories. Figure 3 identifies major module electrical insulation system integrity and grounding requirements; Figure 4 highlights the details of specific module electrical insulation and grounding tests. Note that for system voltages equal to or greater than 30 Vdc, the test voltage for the module-isolation capability requirement is equal to two times the system voltage plus 1000 Vdc.

## MODULE SAFETY COMPONENT DURABILITY TESTS

Figure 5 summarizes module safety component durability tests that are based on the expected use environment. Many of these requirements are based on conditions encountered during handling, packing, and transporting of modules to the installation site. For example, the strain relief test for leads and cables is a test of the attachment means, consisting of a 20-pound force applied for one minute in any direction, without damaging the lead or cable, its connecting means, or the module or panel. The ARCO Gemini module experienced no difficulty in passing this test. As another example, the impact test consists of dropping a 2-inch-diameter steel ball, weighing 1.18 pounds, onto the most vulnerable part of the module from a height of 51 inches. The criteria for passing this test is that there are no accessible live parts, or shards of glass larger than 1 square inch. Although the glass superstrate of an ARCO Gemini module cracked when subjected to this test, the 1/8 inch glass substrate remained intact. Since there were no accessible live parts, or shards of glass larger than 1 square inch, as shown in Figure 6, the module is considered to have passed this test.

## MODULE CONSTRUCTION PRACTICES AND MATERIALS

Finally, required module construction practices and materials, summarized in Figure 7, identify basic, good engineering design practices applicable to photovoltaic modules. For example, compatibility of connection means with recognized wiring systems refers to NEC provisions that identify acceptable terminals, connectors, or pigtail leads (with a minimum free length of 6 inches).

## MODULE FLAMMABILITY TESTING: MANUFACTURER'S OPTION

The last topic to be addressed is module flammability testing, an optional test performed at the manufacturer's request. Module flammability involves three distinct risk areas: (1) the ability of a module to self-ignite due to an electrical arc; (2) the susceptibility of a module to ignition from an external flame source; and (3) the extent to which an array affects the flammability of a fire-sensitive application. The last two items are a major consideration for fire-rated applications, such as roof-mounted photovoltaic arrays on public buildings and in certain residential communities with a high fire concern. Three specific fire-resistance ratings have been defined: Class A, effective against severe fire exposure; Class B, effective against moderate fire exposure; and Class C, effective against light fire exposure. UL 1703 has identified two tests from another safety standard, Tests for Fire Resistance of Roof Covering Materials, UL 790 (Reference 3), as applicable to photovoltaic modules. The spread-of-flame test is designed to measure resistance to flame spread due to an external source of flame impinging on the top surface of a photovoltaic array. The burning-brand test measures the ability of an array to resist penetration due to burning brands. Figure 8 summarizes the principal parameters of each test. Findings indicate that most EVA modules will barely qualify for a Class C fire rating, and that special materials and constructions are required for Class B and Class A fire ratings (References 4 and 5). During or after these tests, the modules are not required to be operational. (Over the past two years the Jet Propulsion Laboratory has done extensive work in the area of module flammability. Additional information can be obtained from the author.)

## SUMMARY

The summary, Figure 9, focuses on two points: for systems designed to operate at above 30 Vdc, electrical safeguards must be incorporated in the module, the installation, or both; and for intended operation in fire-sensitive installations, optional module flammability tests determine the fire classification.

## ACKNOWLEDGMENTS

The author expresses appreciation to Theresa Jester of ARCO Solar, Inc., for providing the ARCO Gemini modules used in the exploratory tests performed in support of this presentation.

REFERENCES


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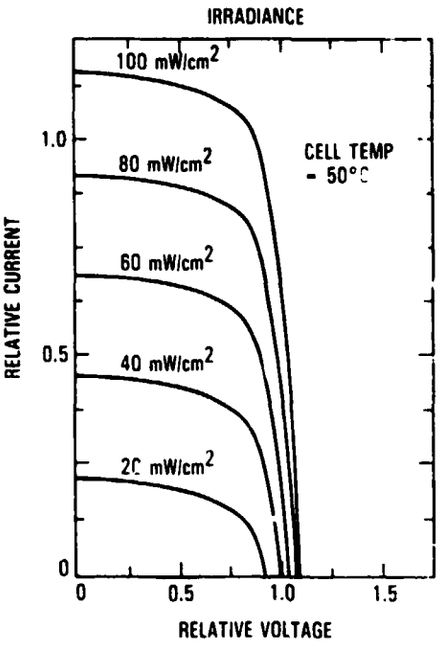
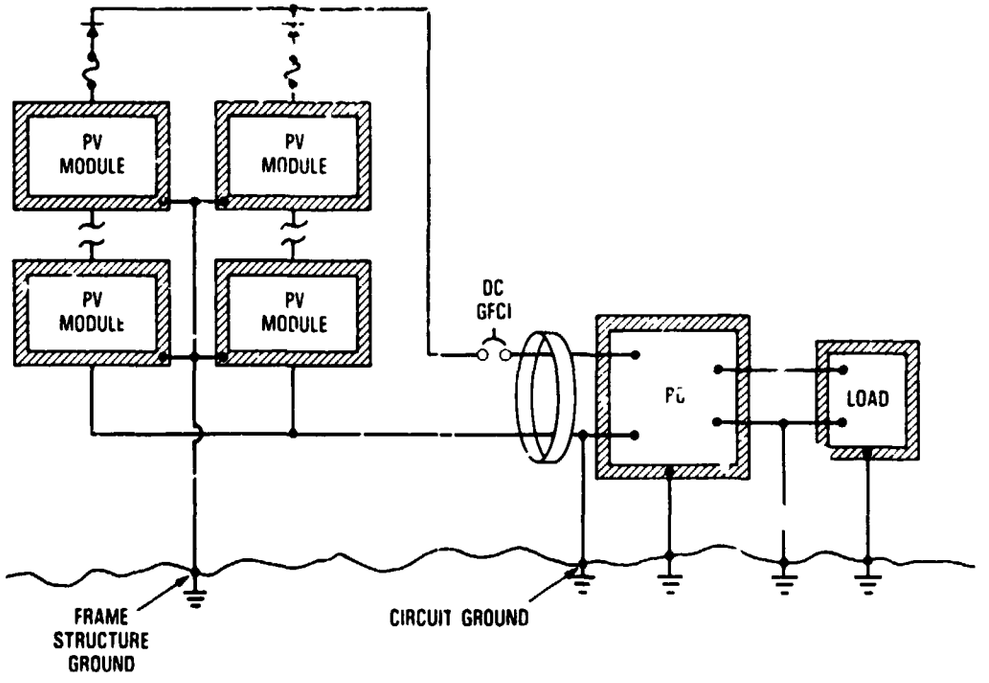
Figure 1. Unique Photovoltaic Electrical Characteristics




- **Array is always "on"**
- **Voltage present at very low illumination — shock hazard exists at early morning & late evening**
- **Current proportional to illumination**
- **Short-circuit current is limited — may affect operation of overcurrent devices**

Figure 2. Isolation and Grounding Safety Concepts



## Figure 3. Module Electrical Insulation System Integrity and Grounding Requirements

- Dielectric voltage withstand (cell string to frame)
- Maximum allowable leakage current (cell string to frame)
- Maximum allowable bonding resistance in the ground path
- Tolerance to inverse current overload
- No accessible live parts
- Minimum spacing between conductors
- Maximum allowable temperatures for polymeric materials

## Figure 4. Module Electrical Insulation and Grounding Tests

| Test | Test Level | Conditions | Acceptance Criteria |
|---|---|---|---|
| Dielectric voltage withstand (cell string to frame) | 500 Vdc for systems<30 Vdc; 2 x system voltage + 1000 Vdc | Dry, after water spray, temperature cycled, humidity tested, and exposed to corrosive atmosphere | Leakage current: ≤50 μA |
| Leakage current levels (cell string to frame or insulating surfaces) | Rated maximum system voltage | Dry and after water spray | Leakage current: ≤10 μA cell string to frame; ≤1 mA cell string to insulating surfaces |
| Bonding resistance in the ground path | Current: twice the rating of the series fuse | Dry | Resistance: ≤0.1 ohm |
| Inverse current overload | Reverse current: 1.35 x rating of the series fuse | Dry | No flaming of cheese cloth or tissue paper |

Figure 5. Module Safety Component Durability Tests

- Temperature cycling test
- Humidity test
- Hot-spot heating test
- Impact test
- Terminal torque test
- Mechanical loading test
- Strain relief test for leads and cables
- Push test
- Cut test
- Accelerated aging of gaskets and seals
- Corrosive atmosphere test

C-2

Figure 6. ARCO Gemini Module After Impact Test

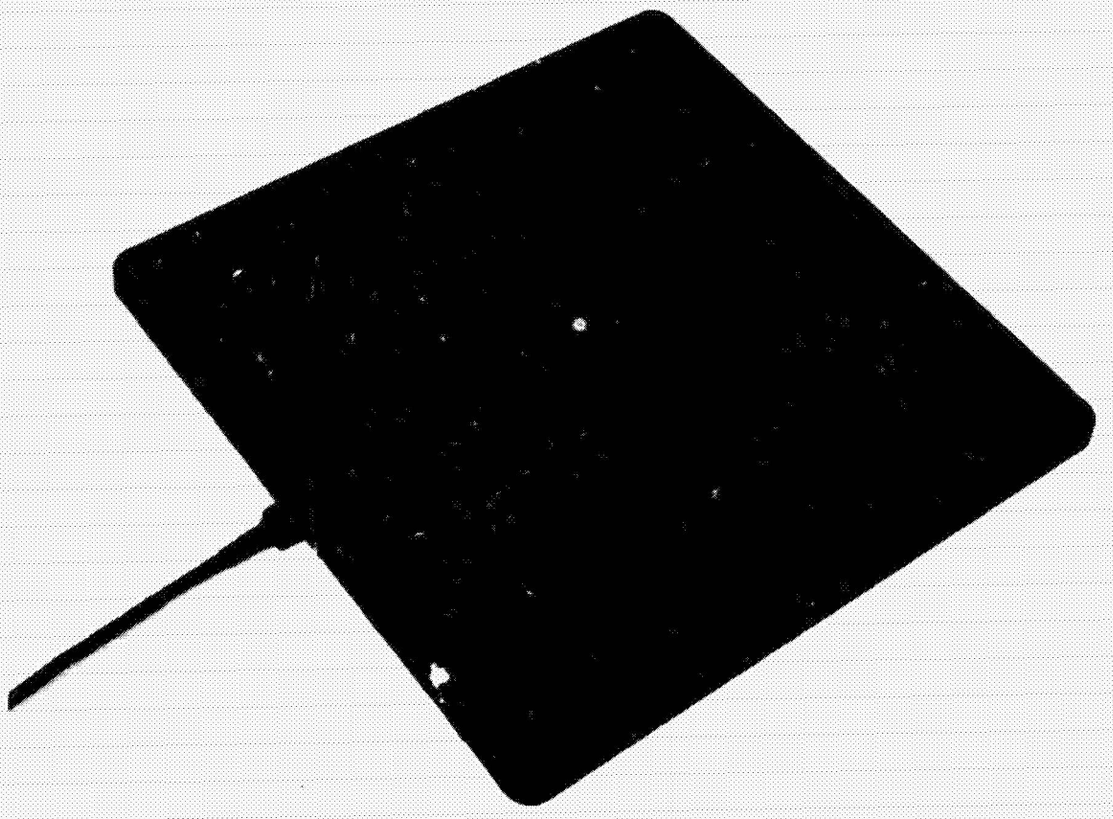


Figure 7. Required Module Construction Practices and Materials

- Compatibility of connection means with recognized wiring systems
- Wiring compartment volume and construction
- Metallic coating thickness
- Edge sharpness limitations
- Markings

## Figure 8. Module Flammability Testing: Manufacturer's Option

- **Tests for Fire Resistance of Roof Covering Materials, UL-790**
  - **Spread-of-flame test — distance that flame has spread; no flaming or glowing brands of roof material**
  - **Burning-brand test — until flame, glow and smoke disappear; no sustained flaming on underside, production of flaming or glowing brands of roof material**

| Fire Rating | Spread-of-Flame Test | | | Burning-Brand Test | | |
|---|---|---|---|---|---|---|
| | Flame Temperature, °F | Flame Application Time, min | Allowable Flame Spread Distance, ft. | Brand Size, in. | Brand Ignition Temperature, °F | Approximate Peak Module Temperature, °F |
| Class A | 1400 | 10 | ≤ 6 | 12 x 12 x 2¼ | 1630 | 1980 |
| Class B | 1400 | 10 | ≤ 8 | 6 x 6 x 2¼ | 1630 | 1400 |
| Class C | 1300 | 4 | ≤13 | 1½ x 1½ x 25/32 | – | – |

- **Most EVA modules will barely qualify for a Class C fire rating**
- **Special materials and constructions are required for Class B and Class A fire ratings**

## Figure 9. Summary

- **Electrical safeguards must be incorporated in the module, the installation, or both, for systems designed to operate at above 30 Vdc**
  - **Evaluation at the module level — conformance to product safety standards: Proposed First Edition of the Standard for Flat-Plate Photovoltaic Modules and Panels, UL-1703**
  - **Evaluation at the system level — compliance with electrical codes: 1984 NEC Article 690, Solar Photovoltaic Systems**
- **For intended operation in fire-sensitive installations, optional module module flammability tests determine the fire classification — Tests for Fire Resistance of Roof Covering Materials, UL-790**
  - **Burning-brand test**
  - **Spread-of-flame test**

## DISCUSSION

ARNETT: I think it might be a good idea to clarify, for those system designers who happen to come to this conference, how you specify what the system voltage is. Most of us who are system designers think of system voltage as the voltage point at which you get your maximum power out of the system, in which you tend to operate. For purposes of safety I believe there is a different way in which that is specified.

SUGIMURA: Yes. That's taking a module at 100 $mW/cm^2$, $0^oC$, and open circuit. The number of modules that are in a source circuit are then added up to come up with that system voltage.

HARTMAN: Has any determination been made -- if you have an isolated frame material, hardware -- if that should be grounded or not? I might have missed it if you talked at it at the beginning.

SUGIMURA: Are you talking about a polymeric frame, perhaps with metal screws or metal fasteners?

HARTMAN: On a metal structure, what should be grounded?

SIGUMURA: A metal structure will definitely have to be grounded. You are talking about a ground-mounted array, to meet National Electrical Code requirements you will have to ground that metal structure. If you are talking about a polymeric frame using metal screws that are going into a wood substructure, I think it is a matter of whether or not UL feels that those metallic screws or fasteners could somehow become energized. Whether that becomes 1 in. or 1/2 in. is basically up to them. In discussions with Underwriters Laboratories, they might be able to give you some guidelines on what they consider at the present time to be safe.

VAN LEEUWEN: On the viewgraphs you had up, delineating all of the tests that UL applies to modules, the bottom of the list was corrosive environment. I believe I heard you say that aluminum, stainless steel and polymeric materials are not subjected to this test?

SUGIMURA: They are excepted from those tests, per the standard. This was as of March 1984.

VAN LEEUWEN: So all that's left is the glass? If you don't have aluminum, stainless steel or polymeric materials -- are they accepted or excepted?

SUGIMURA: They are excepted from the test. The test is not performed if you have a glass module with those particular components on it.

VAN LEEUWEN: So what type of modules are there that --

SIGUMURA: Well, if you were to use a sheet-steel frame or a metallic frame that was not properly protected, they would go ahead and perform the corrosive atmosphere test. I am not aware of modules that they have performed this test on, it was just that when they set out to establish these requirements, they tried to consider all possible configurations of a photovoltaic module.

TRENCHARD: In deploying our modules we have a lot of problems with people getting their hands cut on these things. I have not been able to find a good specification for preventing that or to build into the design. Do you happen know if there is a standard for that?

SUGIMURA: For what? Sharpness? I think UL does have it in that 1703. I don't remember the name of the UL standard that addresses that situation, but there is one. I'll check with you after the program.

SESSION II

THIN-FILM MODULE DESIGN
DEVELOPMENTS

Chairman: E. Royal
(Jet Propulsion Laboratory)

D7

# Large-Area Thin-Film Modules

N86-12766

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## Abstract

The low-cost potential of thin-film solar cells can only be fully realized if large-area modules can be made economically with good production yields. This paper deals with two of the critical challenges. A scheme is presented which allows the simple, economical realization of the long recognized, preferred module structure of monolithic integration. Another scheme reduces the impact of shorting defects and, as a result, increases the production yields. Analytical results demonstrating the utilization and advantages of such schemes will be discussed.

## Introduction

Thin-film solar cells are actively being studied because of their potential as truly low-cost, large-scale, power-generation devices. As a result, there have been significant improvements in the performance of these cells in the last few years. More than 10% conversion efficiency has been reported for at least four material combinations: (CdZn)S/$Cu_2S$,[1] a-Si,[2] $CuInSe_2$/CdS,[3] and CdS/CdTe.[4] To fulfill the low-cost potential, however, it is not enough to use thin semiconductor films for device construction. Considerable efforts are required in every aspect of cell design and fabrication to ensure that these cells could be manufactured economically. This paper deals with two such aspects: the large area module design and the reduction of detrimental effects due to shorting defects.

## Large-Area Module Design

Since solar cells are low-voltage, high-current devices, large-area cells needed for large-scale generation of electricity

cannot be produced by making large-area coatings. Some economic schemes for tapping the electrical output of the cells with minimum Joule losses have to be devised. This is not a trivial problem with thin-film cells, since the conductivity-limiting element is often the electrode layer buried under the thin active layers. Grid electrodes commonly used for bulk single-crystal or polycrystal cells cannot be used. In fact, even in cells whose structure allows the use of grid electrodes, pinhole problems (to be discussed later) make this approach undesirable. Instead, a monolithic integration design is preferred.

In a monolithic integration design, a large-area solar cell is divided into small area elements which are then connected in series. This has the benefit that the voltage rather than the current of the small area elements is added when a large-area cell is made, and it also reduces the current path. Both tend to reduce the Joule loss. The merits of such a design for large-area solar modules have long been recognized.[5-10] With techniques such as photolithography developed for integrated circuits, it is also obvious that, although the process will be rather expensive, the design is technically feasible. The challenge is to design a scheme and a process compatible with the large-scale manufacturing of solar modules at low cost.

Earlier, we presented such a scheme using a CdS/CdTe thin-film cell as an example.[11] This is done by dividing the transparent conductive ITO or $SnO_2$ coating (Fig. 1a) into electrically isolated, elongated stripes (Fig. 1b). Continuous CdS and CdTe layers are then coated (Fig. 1c), followed by a scribing process designed to expose some of the underlying conductive coating (Fig. 1d). A continuous top electrode layer is then coated, making contact to the exposed transparent conductive layer (Fig. 1e). A third scribing process separates the top electrode layer into stripes, completing the integration (Fig. 1f). Figure 2 shows the perspective view of a completed module.

This scheme using three scribing operations to complete the monolithic integration is attractive because it does not use the expensive photofabrication process. Furthermore, no masking is needed in any of the thin-film deposition processes, and only

one-dimensional registration is required during the scribing steps. The spacial relationship of the three scribe lines also relaxes the registration requirements making the scheme compatible with low-cost production processes.

Scribing can be done by a variety of methods. For the transparent conductive layer, laser scribing is desirable because of its speed and cleanliness, and because of the mechanical hardness of the layer. For the other two cases, however, the necessity to scribe the top layers without damaging the underlying transparent conductive layer and the potential for laser-induced degradation of electrical properties in the semiconducting layers make mechanical scribing more desirable. The CdS/CdTe cell is particularly suitable for mechanical scribing because these semiconductor layers are much softer than the $SnO_2$ or ITO layers.

Increasing the width of the individual cell elements reduces the fraction of wasted area due to integration but increases the current path and hence the Joule loss. The optimum cell width is therefore determined by seeking a compromise between these two factors. It is easy to show that the power loss due to these two mechanisms can be expressed by

$$P = J^2 R_{\square} L^3 (L + W)^{-1} + PW(L + W)^{-1} \qquad (1)$$

where J and P are the current and power density of the cell at the operating point, respectively; $R_{\square}$ is the sheet resistivity of the oxide layer, W is the width of the wasted region due to scribing, and L is the active width of the cell. Assuming $W << L$, the optimum width of the cell can be expressed by:

$$L = \frac{3}{2}\left(\frac{PW}{J^2 R_{\square}}\right)^{1/3} \qquad (2)$$

For a given kind of cell it is thus determined by the conductivity of the conducting oxide and the amount of area wasted for scribing. The calculated optimum element width and the corresponding

power loss are shown in Figs. 3 and 4 for a sample case of P = 10 $mW/cm^2$ and J = 18 $mA/cm^2$.

## The Pinhole Problem

Another problem unique to thin-film cells is that of shorting pinholes. This problem arises because thin-film solar cells often use two continuous electrode layers separated from each other only by the semiconductors, which are just a few micrometers thick. Any defects in the semiconductor layers might result in a short between these electrodes, severely degrading the cell performance.

Randomly distributed pinholes can be described by the Poisson distribution:

$$P(x, A, N_d) = \frac{(A \cdot N_d)^x \exp(-A \cdot N_d)}{x!} \qquad (3)$$

where $P(x, A, N_d)$ gives the probability of finding defects in an area A with an average defect density $N_d$. Thus, the probability of finding a defect-free cell is:

$$P(0, A, N_d) = \exp(-A \cdot N_d) \qquad (4)$$

This probability is thus extremely area sensitive. For example, for a defect density of 0.001/$cm^2$, the probability of getting a defect-free 1-$cm^2$ cell is maybe as high as 99.9%, easily leading one to conclude that defect problems do not exist in this thin-film cell system. In fact, however, the probability of producing just a 1000-$cm^2$ cell is less than 37% (Table 1).

**Table 1. Yields of Pinhole Free Cells**

| | Pinhole Density, $cm^{-2}$ | | | |
|---|---|---|---|---|
| Area, $cm^2$ | 0.001 | 0.01 | 0.1 | 1 |
| 0.1 | 99.99 | 99.9 | 99 | 90.5 |
| 1 | 99.9 | 99 | 90.5 | 36.8 |
| 10 | 99 | 90.5 | 36.8 | $5 \times 10^{-5}$ |
| 100 | 90.5 | 36.8 | $5 \times 10^{-5}$ | $4 \times 10^{-44}$ |
| 1000 | 36.8 | $5 \times 10^{-5}$ | $4 \times 10^{-44}$ | 0 |

Since large-area cells have to be fabricated in a mass production environment, and care in manufacturing process control can only reduce defect density to a certain limit, it is desirable to devise a scheme that would reduce the detrimental effect of defects if they do exist. The scheme has to be compatible with low-cost processes also. The use of the monolithic integrated scheme accomplishes some of this mission. The area of the module is divided into many elements, which are then connected in series. A defect degrades only the element it resides on and not the whole cell; its effect is thus reduced.

The detrimental effect of defects can be further reduced by a cross-cutting scheme.[12] Basically, an integrated module is indiscriminately divided into many parallel subarrays by cutting, perpendicular to the direction of the scribes for integration, through all the thin-film coatings on the substrate (Fig. 5). The subarrays are electrically isolated from each other except at the two ends, where common electrodes connect them in parallel.

The beneficial effect of cross-cutting can be appreciated from a special example (Fig. 6). A module having 10 cells connected in a series is assumed to have 10 defects strategically placed such that there is a defect in each individual element. The whole module is inoperative because all the elements are shorted. Now if the module is cross-cut into 10 subarrays each containing just one defect, only 10% of the power output from the

module is lost because only one element in each subarray is shorted.

The effect of cross-cutting in a more general case can be analyzed as follows. We assume that all cells behave ideally with their I-V relationship given by

$$I = I_0(\exp \frac{eV}{nkT} - 1) - I_L \qquad (5)$$

where $I_0$ is the reverse saturation current, $I_L$ is the light generated current, n is the diode factor, e is the electron charge, and k is the Boltzmann's constant. We also assume that all defects behave like perfectly conducting paths, rendering the cell elements on which they reside totally inoperative but not adding any series resistance to the rest of the array.

The defect density has to be in a reasonable range for the cross-cutting to be effective or meaningful. Too high a defect density necessitates cross-cutting the array into such fine divisions that it becomes impractical. It is easy to show that, with such reasonable defect density, for a module of area A consisting of N cells connected in series and divided into M subarrays, essentially none of the M subcells contain more than one defect. Thus a subarray with x defects behaves like one with (N - x) subcells in a series. The I-V relationship of such a subarray can be represented by

$$I = \frac{1}{M}(I_0[\exp(\frac{eV}{(N - x)nkT}) - 1] - I_L) \qquad (6)$$

Since an array is constructed of M subarrays in parallel, the I-V relationship of the array is given by

$$I = \sum_{i=1}^{M} \frac{1}{M}(I_0[\exp(\frac{eV}{(N - x)nkT}) - 1] - I_L) \qquad (7)$$

where the subscript i denotes the ith subarray.

In practical applications, many of these arrays are connected in parallel. The large number of subarrays involved justifies the use of probabilities and Eq. (7) is replaced by:

$$I = \sum_{x=0}^{\infty} P(x, M, N_d)\{I_0[\exp(\frac{eV}{(N - x)nkT}) - 1] - I_L\} \qquad (8)$$

where x is the probability for finding x defects in a subarray:

$$P(x, M, N_d) = \frac{1}{x!}(\frac{N_d \cdot A}{M})^x \exp(-\frac{N_d \cdot A}{M}) \qquad (9)$$

Given the values for the various constants in Eq. (8), the power output of the parallel assembly can be calculated and compared with that of a defect-free case ($x = 0$, $N_d = 0$).

Such calculations have been carried out using parameters for an idealized thin-film CdS/CdTe solar cell:[3] $I_L = 19$ mA/cm², $I_0 = 5.4 \times 10^{-10}$ A/cm², $n = 1.78$ under 75 mW/cm² of AM2 sunlight. In these calculations the array is assumed to consist of 60 cells in a series. Figures 7 and 8 show the calculated power loss and $V_{oc}$, respectively, as a function of cross-cutting for several $N_d \cdot A$ values. Figure 9 compares the power loss as a function of $N_d \cdot A$ between an undivided array and one which has been divided into 10 subarrays. The reduction of power loss is substantial, and this reduction is achieved through indiscriminative cross-cutting of the array.

The power loss can be further reduced by increasing cross-cutting, but the marginal benefit decreases. In practice the degree of cross-cutting is determined by a balance between the benefit and the added production costs as well as area lost due to cross-cutting.

## Summary

Two simple schemes which improve the potential for low-cost production of large area thin-film solar cell modules have been presented. The analysis was carried out based on thin-film CdS/

CdTe solar cells but the schemes should be generally applicable to other thin-film cells as well.

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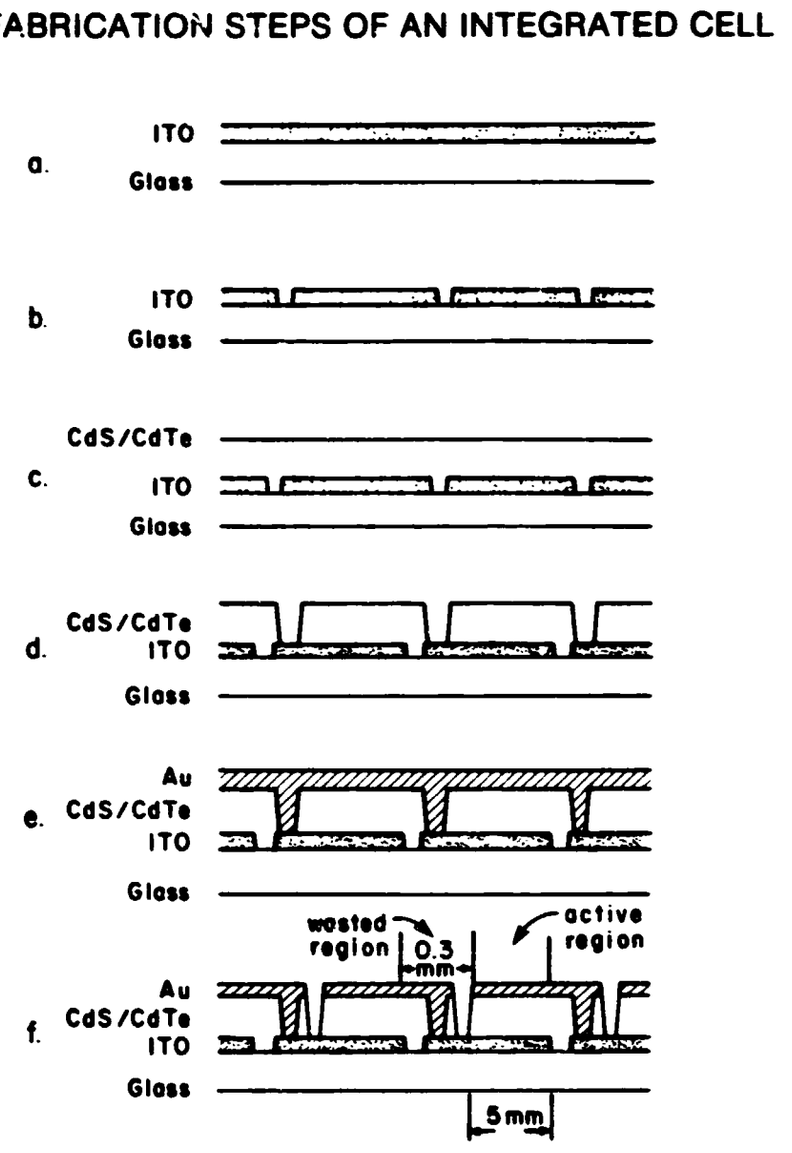


**Figure 1.** Fabrication steps of a monolithically integrated module.

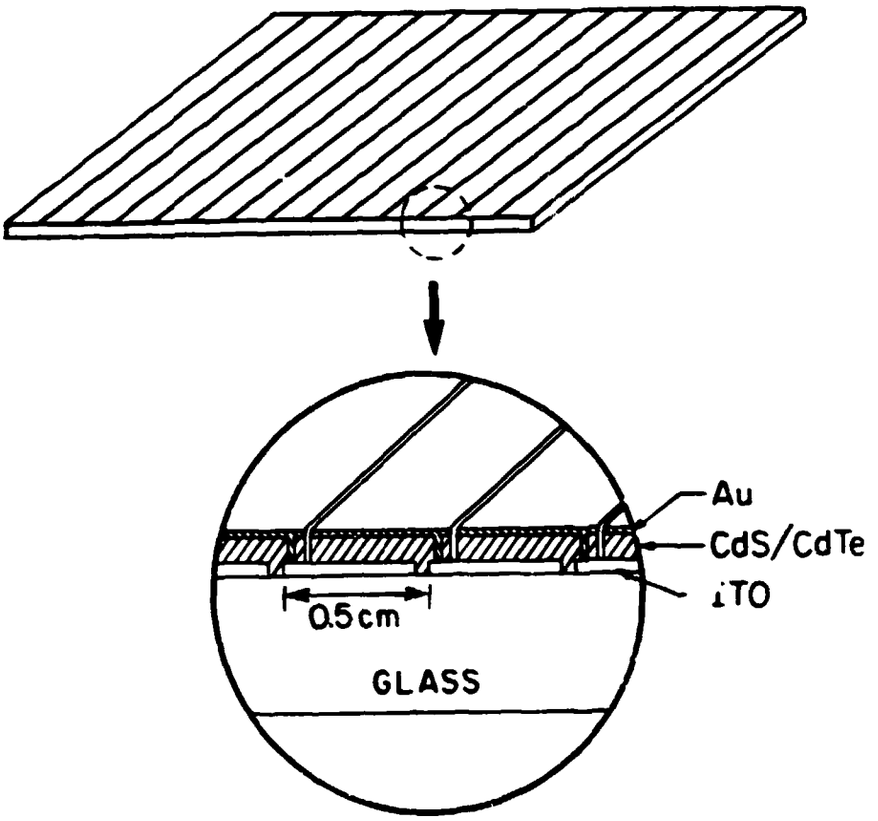


**Figure 7.** Perspective view of a monolithically integrated CdS/CdTe module.

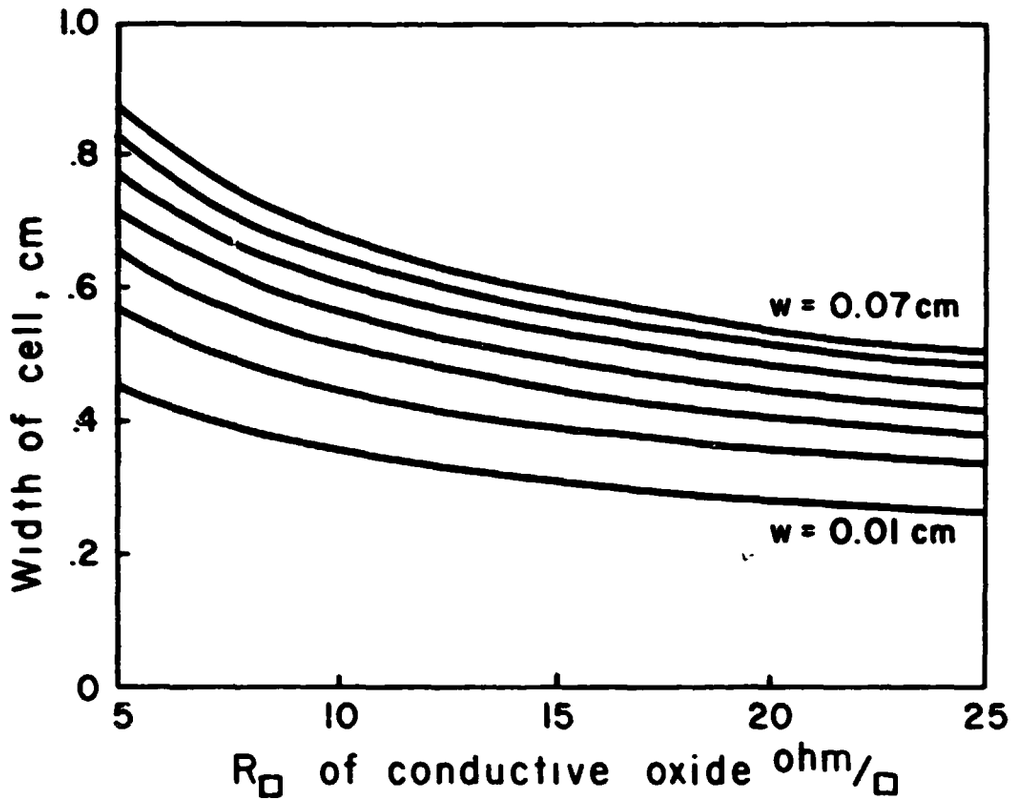


Figure 3. Dependence of the optimum cell width on the resistivity of the conductive oxide layer and the scribing waste.

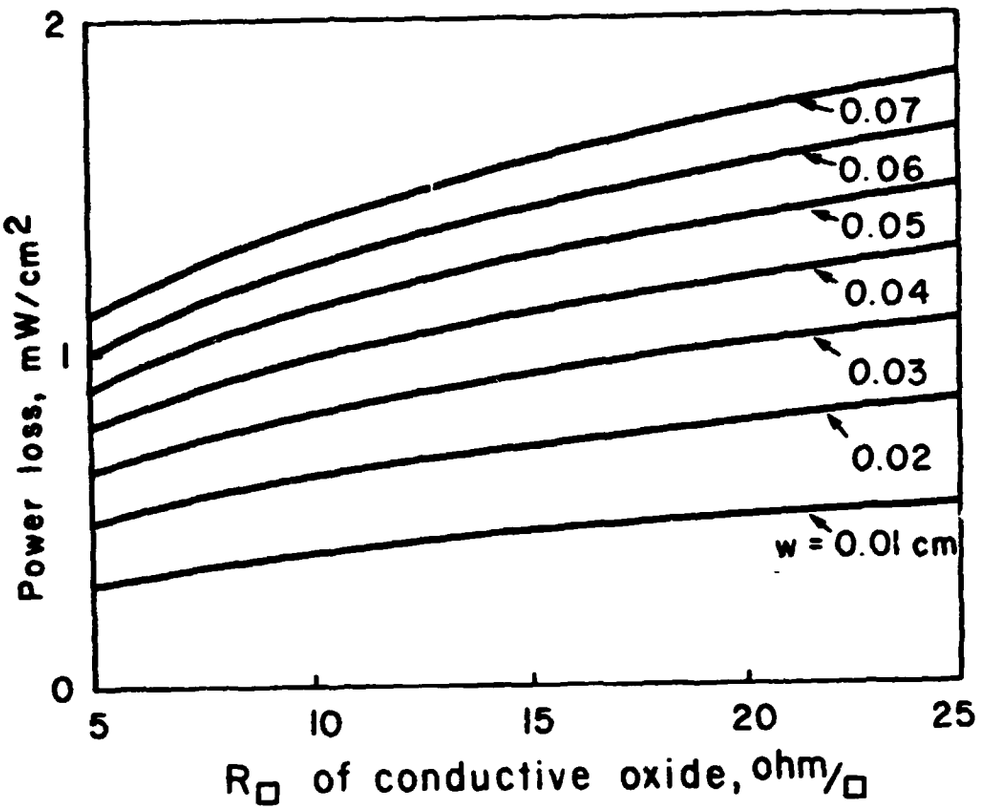


**Figure 4.** Dependence of the power loss at optimum cell width on the resistivity of conductive oxide and scribing waste.

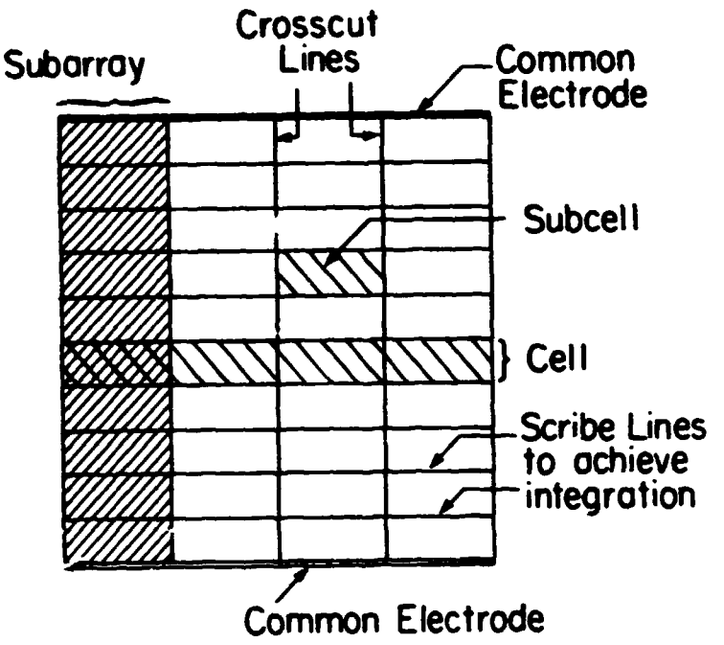


**Figure 5.** A monolithically integrated array with cross-cuts. The cross-cut lines are scribe lines cutting through all thin-film layers on the substrate.

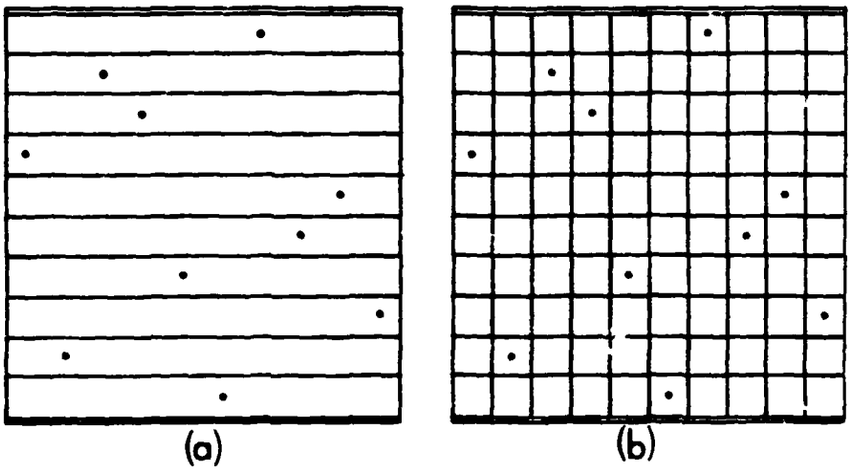


**Figure 6.** A special example showing the beneficial effect of cross-cutting. (a) Without cross-cutting, all cells in the array have one shorting defect. No output is expected from the array. (b) With cross-cutting, one cell in each subarray has a shorting defect. Only 10% of the power is lost due to defects.

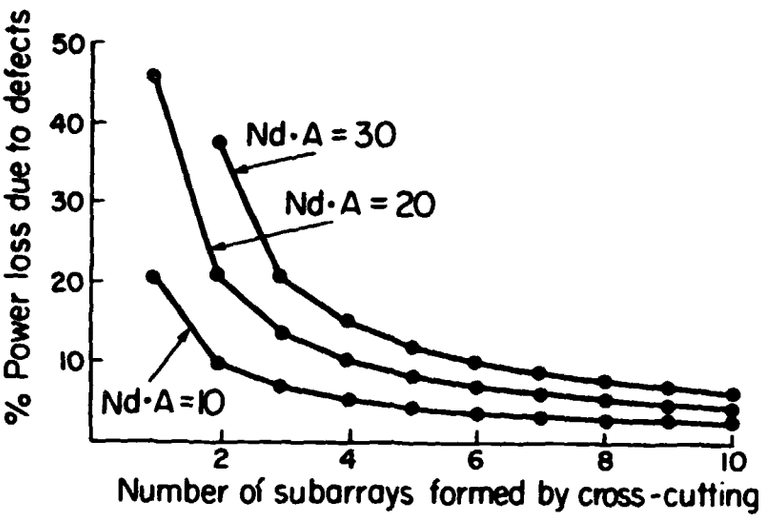


**Figure 7.** Effect of cross-cutting on the defect-induced power loss of an integrated array consisting of 60 cells in series.

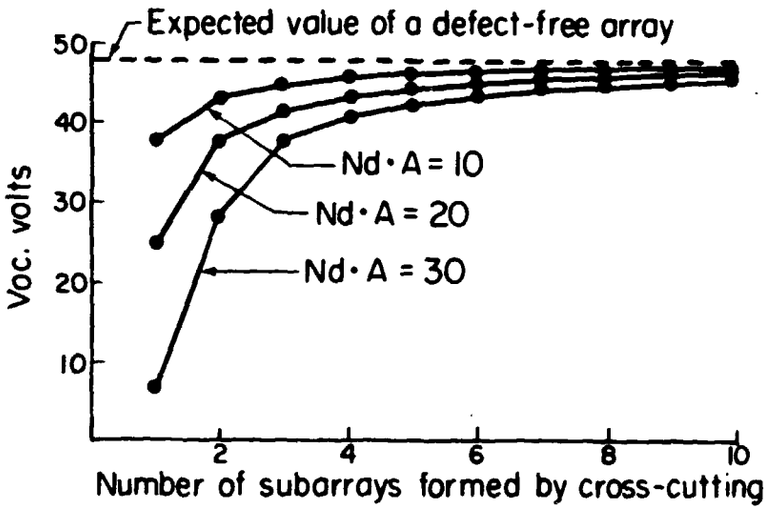


**Figure 8.** Effect of cross-cut on the voltage output of an integrated array consisting of 60 cells in series.

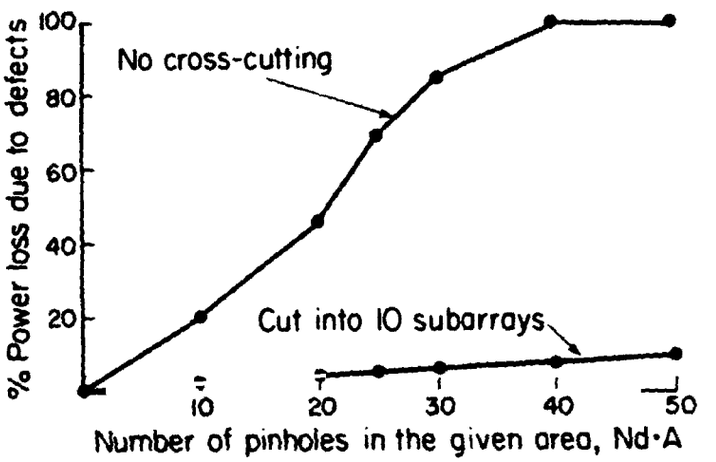


**Figure 9.** Percentage power loss due to shorting as a function of defect density for an array of 60 cells in series.

## DISCUSSION

**LESK:** Are these shorts just through the cad sulfide, which is about a hundred times thinner than the cadmium telluride, or do you have to go all the way through both layers and short cold to the ITO?

**TYAN:** There are all kinds of different shorts. We are in the situation where we are not producing 1 $ft^2$ cells. We are in the laboratory, so our yield is pretty good, about 99%. We are not actually experiencing a large number of defects. What we are presenting here is a schome that will take care of defects when you make large-area modules. It doesn't really matter what kind of shorts you have.

**LESK:** Your cad telluride is quite conductive compared with intrinsic amorphous silicon. If you had a short just through the cad sulfide layer, it would make it look like a short all the way through, is that right?

**TYAN:** Cad sulfide is a semiconductor also. In the process we use the cad sulphide is rather insulated. So, even if we have a direct short between metal and cad sulfide, you still have some contact with resistance, which may or may not be enough when you try to make a module. We still have the shorting problem due to that contact. You can reduce the impact by doing this.

**ROYAL:** I noticed that there are very high temperatures in the process, where you have a substrate temperature of 600°C or so. Are there any problems in that area?

**TYAN:** That is the only way we know of making it.

**BICKLER:** It might be worth pointing out to people who contemplate using this process that Eastman Kodak has patented this design. Am I correct?

**YERKES:** Why don't you go ahead and make a 1 $ft^2$ array? What is holding you up? We've been hearing this from Kodak since 1982. Let's go ahead and do something!

D8

N86-12767

# Interconnect Resistance of Photovoltaic Submodules

Prepared for

JPL Research Forum
on

Reliability and Engineering of
Thin-Film Photovoltaic Modules

by

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## Interconnect Resistance in Submodules

Small area amorphous silicon solar cells generally have higher efficiencies than large interconnected submodules. Among the reasons for the differences in performance are the lack of large area uniformity, the effect of non-zero tin oxide sheet resistance, and possibly pinholes in the various layers. Another and usually small effect that can contribute to reduced performance of interconnected cells is the resistance of the interconnection i.e. the series resistance introduced by the metal to tin oxide contact through silicon.

Our 1' X 1' and 1' X 3' PV panels have tin-oxide to aluminum contacts that are approximately 0.03cm wide and nominally 30 and 142 cm long for the two different sized panels (approximately 0.4 cm inactive edges are allowed for see Figure 1). To a first approximation the effect of the contact resistance is simply that of a series resistance; this is easily calculated and is shown in Figure 2. Here the fill factor is calculated using the ideal diode equation for tin oxide sheet resistances of 5 and 20 ohms per square.

There is another effect which can, under certain circumstances, be important. It is due to small parasitic cells resulting from the patterning of the submodule. A schematic representation of the cross section of a portion of a monolithic submodule is shown in Figure 3. Also shown is the electrical schematic for a cell and its interconnect region. This interconnect scheme results in a main cell with area, A3 and two small cells with areas A1 and A2. The two small cells are in parallel and are shunted by the contact between the tin oxide and aluminum with contact resistance Rc. In the ideal case where tin oxide to aluminum contact resistance is zero, the only detrimental effect of the two small cells is to reduce the effective area of the large cell. In this case in addition to the approximately 0.03cm lost to the three patterning operations another 0.05cm (the width of A1 + A2) is lost due to the parasitic cells. If however Rc is not zero then additional losses result, their extent depending on the magnitude of Rc and the areas A1 and A2. Figure 4 shows approximately how to output characteristic of the total cell is changed by a fairly high Rc. Here curve A is the I-V curve for the combination of A1 and A2, curve B is that of the main cell, A3 and curve C is the resultant curve due to all three. In the open circuit condition, the large cell is not loaded; the small cells however are shunted by Rc and for not excessively large Rc, their I-V curve is a straight line with an open circuit voltage of Vsoc. This voltage subtracts form the open

circuit voltage of the large cell, Vloc, to give a measured open circuit voltage, Vmoc, of Vloc-Vsoc. If Is is the short circuit current of the small cells, then clearly the contact resistance is given by Vsoc/Is. To obtain a value for Rc we need to know Is and we assume it to be proportional to the short circuit current of the large cell, Il, as is the area. We can obtain Vloc by shading the two small cells from light (in this condition the small cells produce no current). Thus

$$Rc = \frac{Vloc-Vmoc}{Il} \times \frac{A3}{(A1+A2)}$$

It might appear that a simple way to reduce Rc is to make the contact wider. Simple calculations show that is not very effective unless Rc is very high. In Figure 5 the equivalent circuit for a tin oxide to aluminum contact is shown. Here W is the contact width, Rsh is the tin oxide sheet resistance and $\rho c$ is the specific contact resistivity in cm2. The linear effective contact resistance Rceff in cm can be obtained from this model in closed form and is

$$Rceff = (Rsh\,\rho c)\ \coth\{w(\frac{Rsh}{\rho c})1/2\}$$

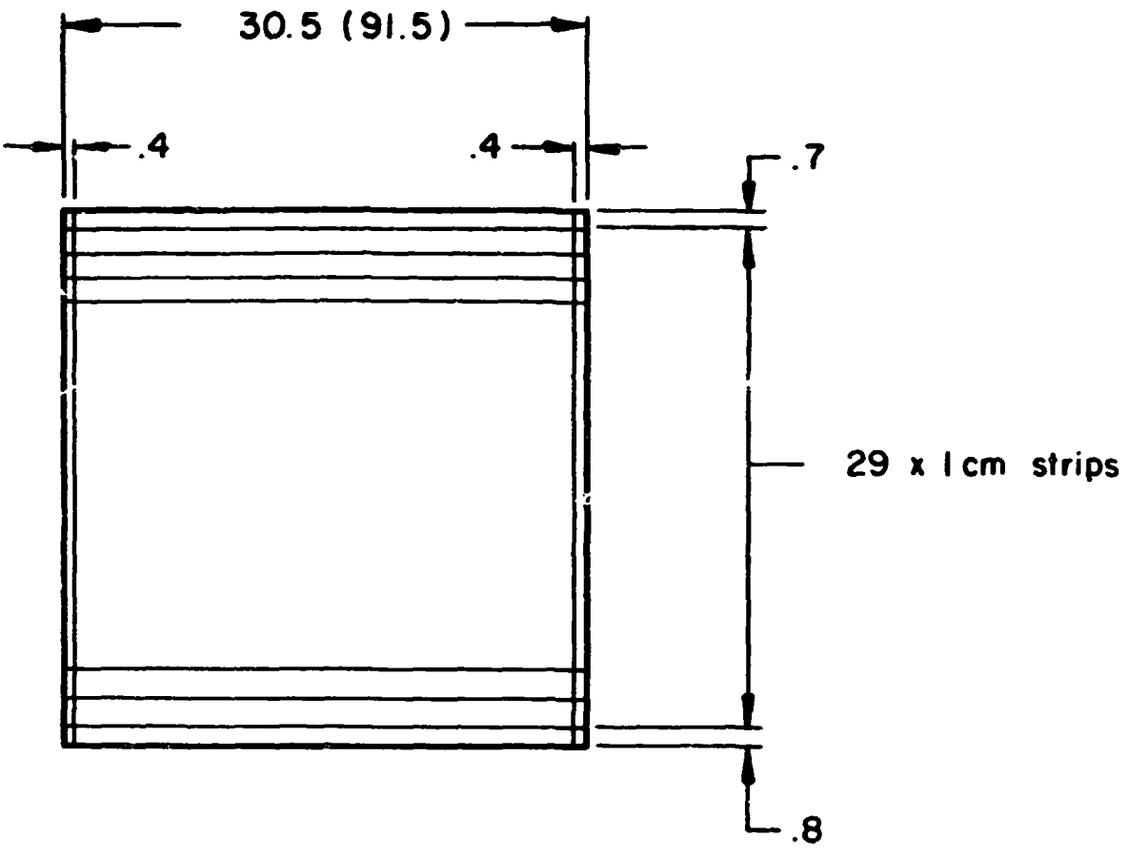
From a plot of this equation, shown in Figure 6, it can be seen that for specific contact resistivities of $10^{-3}$ cm2 or less, little can be gained by increased contact widths beyond 0.01cm; that is Rceff is an acceptable 0.01 $\Omega$ for a 1cm long contact.

Experimental determination of Rceff and $\rho c$ under controlled conditions gave values for $\rho c$ of $10^{-4}\,\Omega$ cm2 for aluminum evaporated directly onto tin oxide. When aluminum was evaporated on tin oxide through a 0.01cm wide cut in silicon, somewhat higher values for $\rho c$ were obtained, $\sim 10^{-3}\,\Omega\,cm^2$

There are likely many factors that affect the magnitude of contact resistances. Three that are easily identified are the condition of the tin oxide surface, the quality of the cut in the silicon and the conditions prevailing during the metalization. We have found, not unexpectedly, that dirty tin oxide results in poor contacts. Not quite as obvious was the observation that when the silicon was laser cut from the silicon side (silicon facing the laser) poorer contacts were obtained on the average than when the glass faced the laser. The reason for this is that reflections from the silicon side are significantly greater than from the glass side and because of slight thickness variations in the films,

reflections are variable; See Figure 6. Thus it is more difficult to achieve constant laser power levels at the Si when cutting the silicon with the silicon side up. The third factor that we looked at was the metalization step. Here we found that evaporating aluminum at high pressures, e.g. $10^{-4}$ torr, produces generally poor contacts. The cleanliness of the metalization chamber also seems to play an important role in the quality of the contact.

While the above discussion shows that poor contacts can be obtained, they can also be avoided by proper processing procedures. On our large PV panels, the contact resistances are generally too small to measure by the method discussed above, i.e. they are less than ~ 0.05Ω. Extrapolation the values obtained on smaller 4" X 12" diagnostic panels where more sensitive techniques can be used suggests that contact resistances for large panels are in the low mΩ range. Thus they cause negligible degradation in panel performance. This conclusion is supported by the fact that 70+% fill factors have been measured for many individual interconnected cells and values near 70% for square foot panels.




| | 1' X 1' | 1' X 3' |
|---|---|---|
| Total area : | 929 $cm^2$ | 2787 $cm^2$ |
| Active area : | 792 $cm^2$ (85%) | 2421 $cm^2$ (87%) |

Figure 1 - Series connected cell patterns on 12" X 12" (or 12" X 36") panels.

Note: all measurements in cm

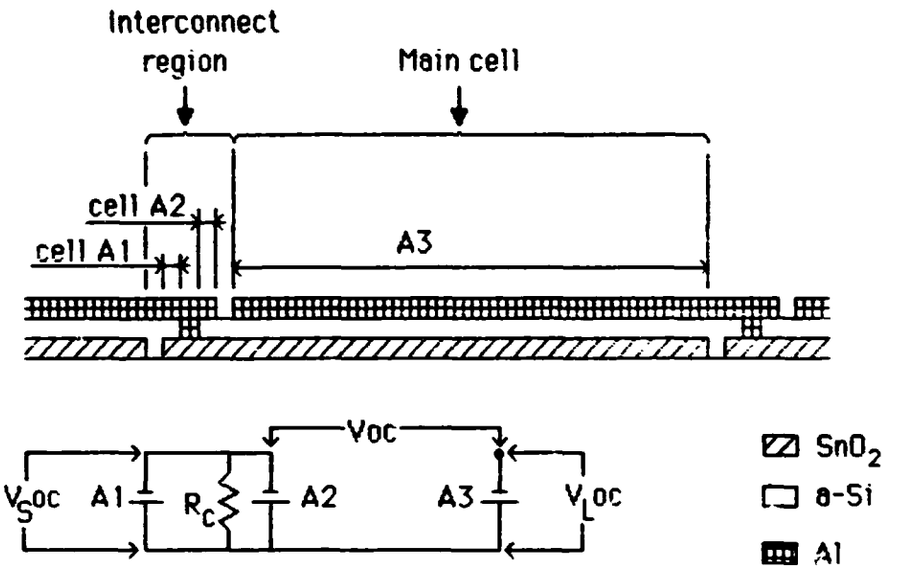



Fig. 2 Schematic presentation of the cross-section of a monolithic submodule showing a cell and the two adjacent interconnect regions.

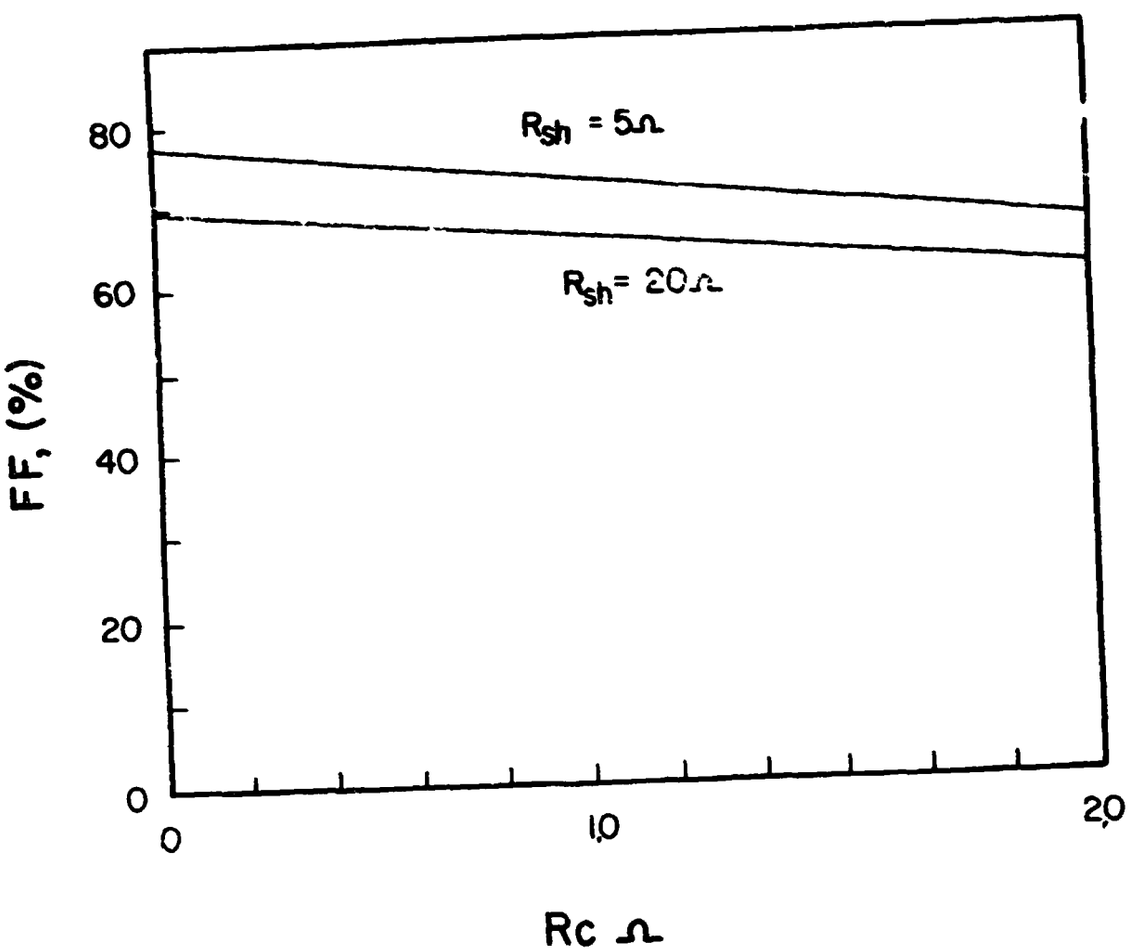



Figure 3 - Calculated dependence of FF on contact resistance

$R_c$ ; $R_{sh}$ = $SnO_2$ sheet resistance.

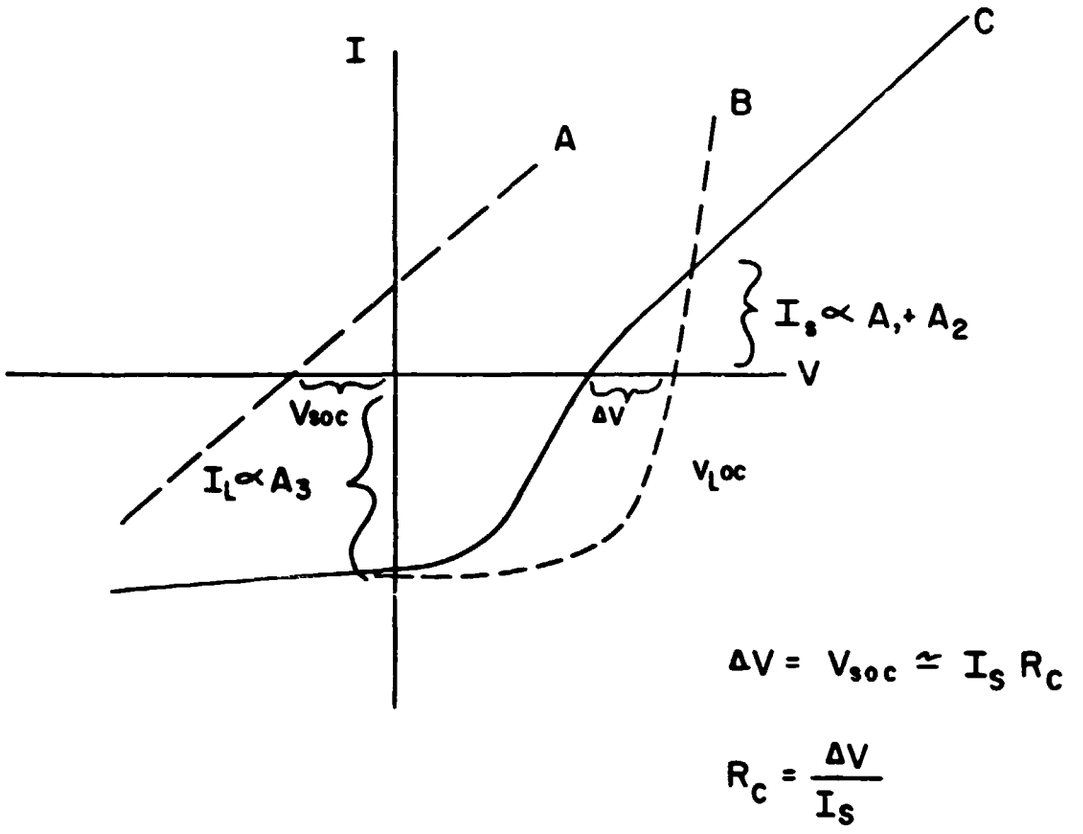
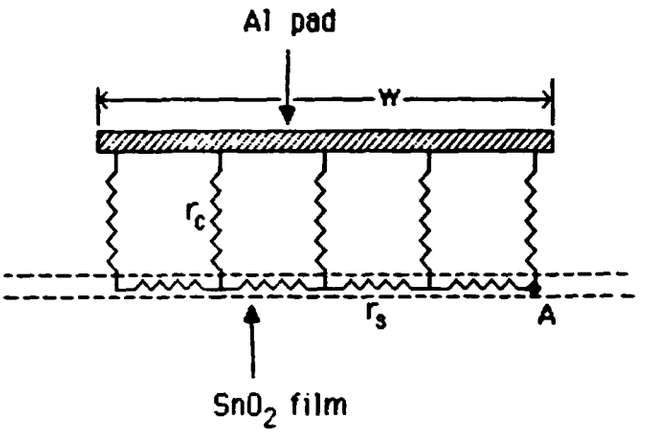



Figure 4 - Effect of the parasitic cells on the I-V characteristics of monoliticaly interconnected a-Si solar cell. See text for explanation.




$$r_s = \frac{R_{sh}\, dx}{W}$$

$$\frac{1}{r_c} = \frac{dx}{\ell_c}$$

Fig. 5 -Equivalent circuit model of Al / $SnO_2$ contact.

$R_{sh}$ : sheet resistance of $SnO_2$ film.

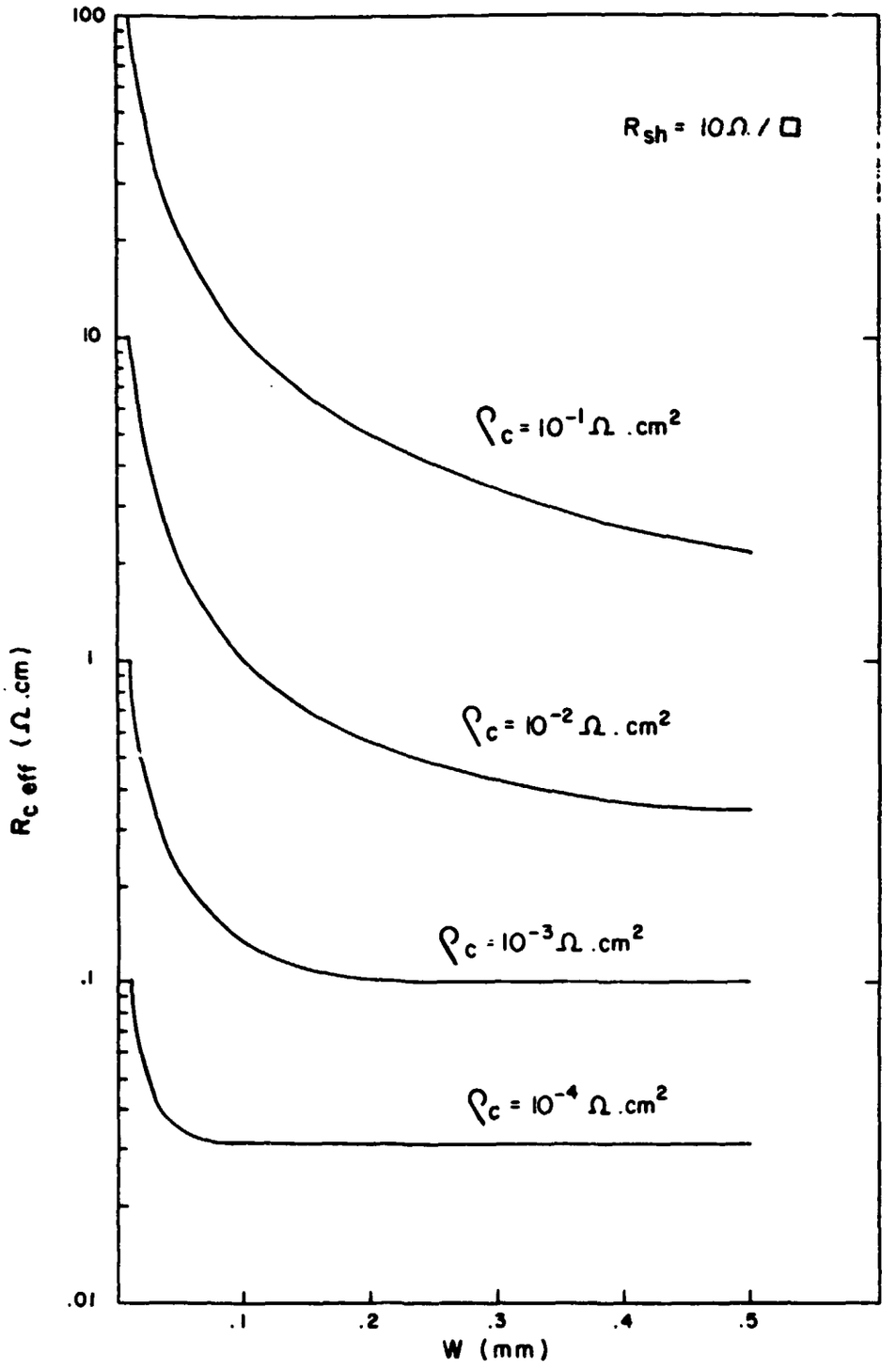
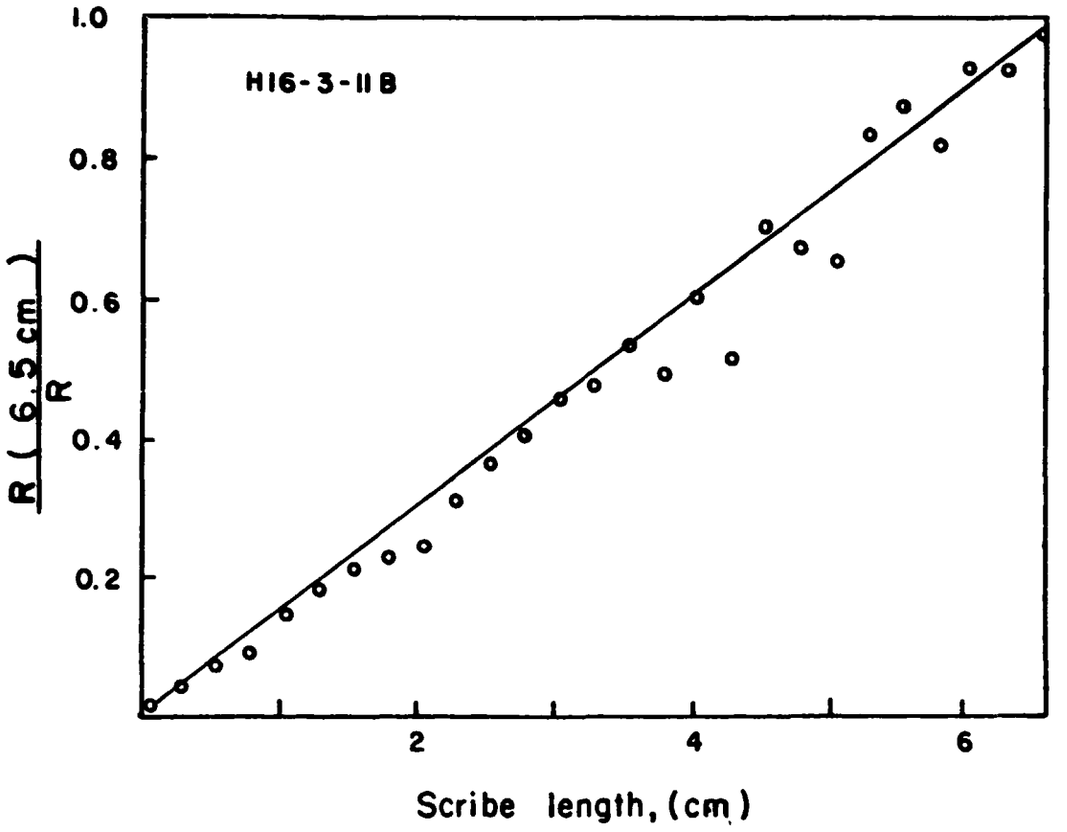



Figure 6 - Dependence of the effective Al / $SnO_2$ contact resistance on the contact width $R_{sh}$:sheet resistance of $SnO_2$ film; :specific contact resistivity.




Variation of contact resistance with $SnO_2$/Al contact area

Figure 7 - Normalized inverse Al / $SnO_2$ contact resistance as a function of laser scribed contact length. Scribe width = 0.01cm.

## DISCUSSION

LESK: When you do your laser cutting through the alpha silicon down to the tin oxide, ITO, if you don't go far enough you will leave a little bit of amorphous material, and it'll be of very high contact resistance. I presume you have to go a little too far. What is the accuracy of cutting into the tin oxide, since it is so thin? If you go all the way through, your contact on the edge of the ITO -- which is very bad -- these are practical problems that have to be solved.

VOLLTRAUER: These are practical problems, right. That's why having conditions where the power is controlled -- the power going into the films is controlled -- is important. There are a few other things we have done; one, for instance, is to make two laser cuts. Either the first one at a higher power level, where you might do some damage to the tin oxide but are assured of cutting all the silicon, and the other one displaced by a fraction of a scribe where you reduce the power to the point where you are assured of not cutting the tin oxide and you very likely will cut the silicon. That has worked out very well.

D9

N86-12768

# Thin Film Module Development

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ARCO Solar, Inc. has developed and now produces a 5 watt thin film silicon photovoltaic module, the Genesis G100. As the first commercially available thin film product from ARCO Solar, the G100 module package incorporates excellent reliability, manufacturing ease, and consumer aesthetics.

This paper outlines the evolution of the Genesis module with emphasis on the design and construction of this commercial product.

The design of the Genesis G100 module was driven by several criteria, including environmental stability (both electrical and mechanical), consumer aesthetics, low materials costs, and manufacturing ease. The module circuitry is designed as a 12-volt battery charger, using monolithic patterning techniques on a glass superstrate. This patterning and interconnect method (Fig. 1) proves amenable to high volume, low cost production throughput, and the use of glass serves the dual role of handling ease and availability.

The mechanical design of the module centers on environmental stability. Packaging of the glass superstrate circuit must provide good resistance to thermal and humidity exposure along with hi-pot insulation and hailstone impact resistance. The options considered are given in Table I. ARCO Solar's reliability and manufacturing experience, based on production of over ten megawatts of photovoltaic modules and large-scale long-term field operations and testing, were employed to a high degree.

Ethylene vinyl acetate (EVA) was chosen as the pottant material for its excellent weatherability. An evolution of backsheet, framing, and termination techniques were built on this choice of EVA pottant.

We made direct use of materials and construction used in our Cz module products for the first thin film module prototype. The module design in Fig. 2 shows a glass/EVA/coated sheet metal laminate framed with anodized aluminum extrusions. Termination of this design was accomplished with two terminal posts protruding from the back of the laminate. Several problems emerged:

- The metal frame and metal backsheet produced low hi-pot resistance when the thin film circuitry was carried close to the edge, resulting in an inefficient active area/module ratio.
- The back side termination did not permit flush mounting after wire routing was installed.
- For shipping considerations, the package was too heavy and bulky.

- Aluminum extrusions were very costly for a square foot product.

The second design iteration improved with the use of a low profile side rail, as shown in Fig. 3. These roll-formed sheet metal rails framed a glass/EVA/glass laminate and provided flush mounting. Termination was accomplished by routing two wires along either side rail. Disadvantages to this design were:

- From a customer's standpoint, the termination wires proved difficult to use.

- The aesthetics needed improvement.

Our third prototype design approached the consumer aesthetics criteria with a glass/EVA/mirrored glass laminate framed with low profile roll-formed rails. The spade lug terminations were embedded in the side rails, offering a smooth product look. Two problems remained with this prototype:

- Terminations would have saddled customers with the expenses of special tools purchases and of special employee training to prepare wires for module connections.

- Difficulties in mounting this module were encountered.

A fourth prototype evolution progressed from discrete frame pieces to a one-piece rubber gasket. The glass/EVA/Tedlar-coated sheet metal laminate was terminated with a narrow printed circuit board onto which wires were soldered to exit the module frame. This one-piece frame approach provided manufacturing ease and improved termination options. Difficulties remaining to be solved were:

- Poor adhesion of the rubber to the glass laminate allowed the rubber to pull away from the laminate.

- Easy mounting holes were not designed into the frame.

The final commercial design of the Genesis G100 product made use of all of the strong points of the previous designs and added excellent consumer aesthetics as well as mounting ease for the customers. The design choices embodied in this module, and the rationale for each, are outlined in Table 2.

As shown in Figs. 4 and 5, the module is constructed from a glass/EVA/tempered glass laminate framed with a one-piece plastic frame. Termination is accomplished with a narrow printed circuit board laminated to the back sheet and a one-piece, two-conductor cable soldered to the board.

The physical and electrical characteristics of the final design are given in Table 3. The Genesis G100 module features mechanical and electrical environmental reliability, manufacturing and shipping ease, and consumer aesthetics, a package truly designed with pride by ARCO Solar to fulfull customer expectations.

**Table I.** Thin film module design options.

| Pottants | Backsheets | Edge Seals | Frames | Terminations |
|---|---|---|---|---|
| EVA | Plastic | Tape | Injection molded plastic | J-box |
| PVB | Coated sheet metal | Gasket | Aluminum extrusions | Pigtail |
| Acrylic adhesives | Tempered glass | RTV | Roll-formed sheet metal | |
| Silicones | | | Gasket | |

**Table II.** Thin film module design choices.

| | Pottants | Backsheets | Edge Seals | Frames | Terminations |
|---|---|---|---|---|---|
| **Choice** | EVA | Tempered glass | RTV | Injection molded plastic | Pigtail |
| **Reasons** | Weatherable | Strength | Low cost | Low cost | Low cost |
| | Low cost | Low cost | Weatherable | Aesthetics | Weatherable insulation |
| | Vacuum lamination processing | Aesthetics | Easy application | | |
| | | Weatherable | | | |
| | Hi-pot/ voltage isolation | Hi-pot/ voltage isolation | | | |

**Table III.** Characteristics of Genesis G100 commercial design.

| Physical Parameters | | Power Specifications | |
|---|---|---|---|
| Length | 13.7" (34.7 cm) | Maximum Power (typical ± 10%) | 5 Watts |
| Width | 13.1" (33.3 cm) | Voltage at max power (typical) | 14.5 lts |
| Depth | 0.5" (1.3 cm) | Current at max power (typical) | .35 Amps |
| Weight | 3 lbs. (1.4 kg) | Open Circuit Voltage (typical) | 20.8 Volts |
| Cable | 16 AWG | Short Circuit Current (typical) | .435 Amps |
| Cable Length | 5 ft. (1.5 m) | | |

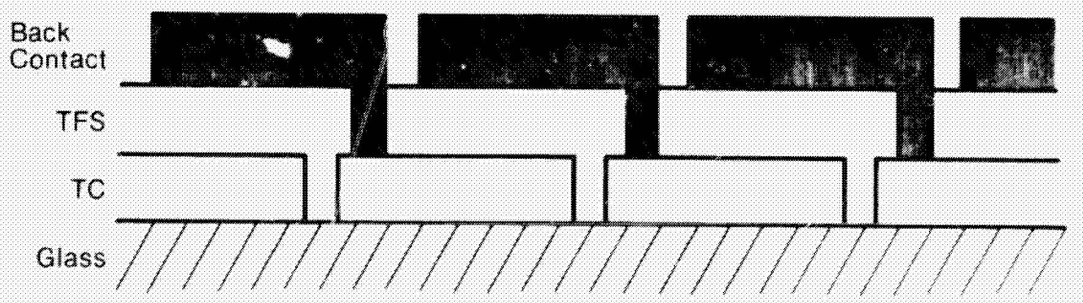



**Fig. 1.** Thin film module monolithic structure.

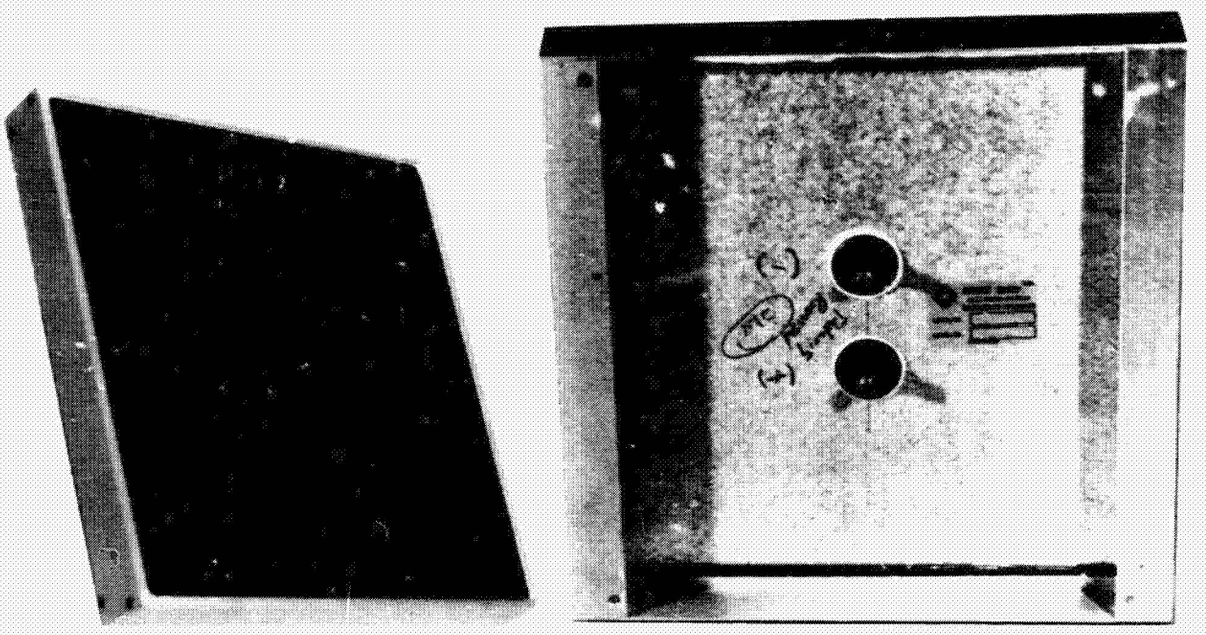


**Fig. 2.** Experimental packaging design based on Cz module design.

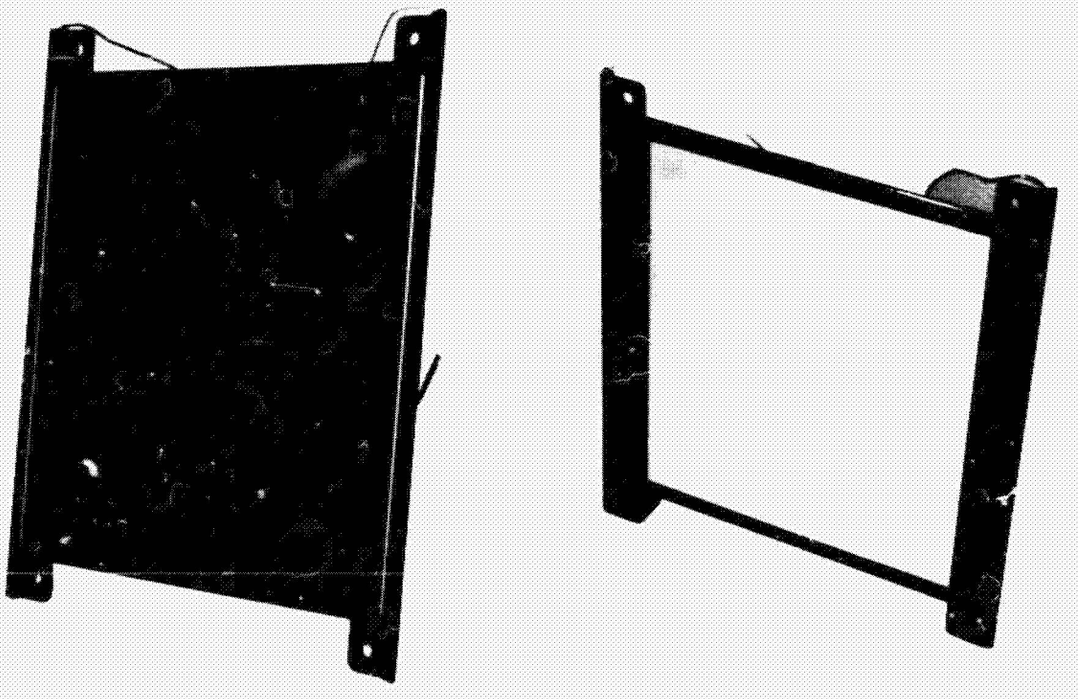


**Fig. 3.** Low-profile metal frame design.

**Fig. 4.** Genesis G100 module.

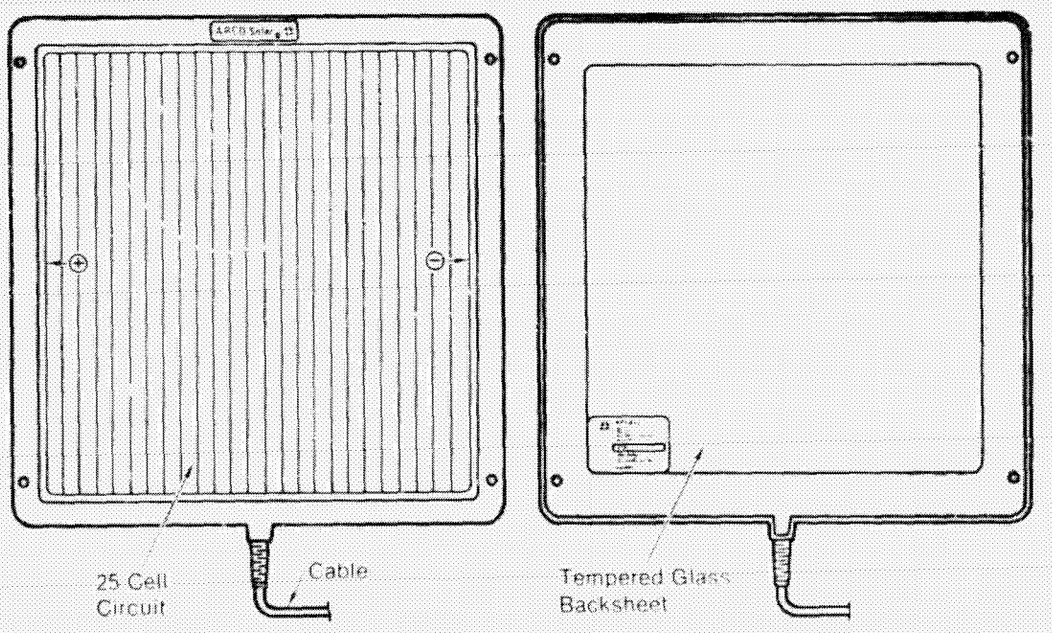



**Fig. 5.** Design details of commercial module.

## DISCUSSION

VASEASHTA: Two things that I don't understand: No. 1, when I opened the module, beneath the IC board there was an epoxy, which I believe was still wet or sticky. Was there some technical consideration for that?

JESTER: Actually what we have done is, we coated that printed circuit board with RTV to keep any corrosion or moisture from attacking the contacts there, and it remains slightly tacky. But it should have been completely dry by the time you got it, unless you got one hot of the press -- did you come to ARCO and pick it out? It's for corrosion reasons that we coat that.

VASEASHTA: Second question, I also looked at the scribing. The tin oxide laser scribe looks thin, while the amorphous silicon looks kind of wide. It does not look like as if it is laser-scribed. If it is not proprietary, could you tell us the process?

JESTER: I really can't tell you that. But it is wider; you are right.

D'AIELLO: Two questions. One quick one: you mentioned the composition of the frame, or at least the trade name for it. Would you say that again?

JESTER: It's Rovel, and it's got some rubber in it for slight mechanical flexibility. It is a Dow product.

D'AIELLO: I assume the frame surface serves no mechanical function. Is it aesthetic?

JESTER: It is aesthetic, and it actually provides mounting. Most of the mechanics, though, come from that glass-glass package -- the mechanical strength. It is injection-molded high-temperature UV-stable material.

D'AIELLO: The question I really wanted to ask relates to the backing material. I noticed that in one earlier case you had mirrors and in the final case you have a glass backing, which is actually black. Two different cases for reflection of radiation, would you comment about that?

JESTER: Actually we went with black because aesthetically it looks very nice. It's just a painted material.

D'AIELLO: You don't attribute any thermal function to the back?

JESTER: Typically these modules are mounted flush on something -- there is not a lot of radiation possible.

BICKLER: I'm curious about your strain relief on the cable. It seems to me that if you mounted that in the same rectangular boss you have it tangertial instead of coming out perpendicular, and you could place these modules next to each other. Is there a reason for that?

JESTER: Actually, since these were designed to be single-battery chargers, we did not worry too much about stacking them close together. You can stack in the other direction, of course, on an array. We actually include in this feed port some of the strain relief. There is some capture there.

ROYAL: With glass-on-glass, has putting that together been any trouble?

JESTER: Actually, it's been a very easy layup. It uses the vacuum lamination technique that we perfected out at our Camarillo facility. It really built on a lot of things that we knew about laminating. It's been very effective -- we don't get any bubbles. That's been real nice in that glass-glass package. It has been very resistant to humidity, of course, which has been a real plus.

ROYAL: You see no bubbles?

JESTER: Well, we actually haven't experienced a bubble problem. Actually, what we did is, in designing, we set the EVA processing temperature and pressures. When we first started out we had a problem with bubbles, but it had to do with the processing technique, so we have worked that out to where we have virtually 100% yield through lamination. Of course, as mentioned by someone else regarding edge-grinding, we found that treating the edge of the glass has made a difference in keeping that yield high. And that is a standard in tempering and in any kind of glass-handling plants. They treat the edges of their glass if they don't want any of these small fracture points to start a major crack. That has been real helpful in keeping our yields high in the lamination area.

LESK: A couple of questions. You didn't mention it, but I assume the 1-mm glass is also tempered?

JESTER: Actually, it is not. And how we obtained the good mechanical strength is, we get a very thin bond line between the thin glass and the 1/8 in. tempered back sheet. And in processing the EVA was one of the things we had to work out -- it's getting a real good mechanical couple by a thin bond line there.

LESK: So that's why it chipped on the steel ball test?

I have another question: 14 1/2 volts, if you are working with a system with a regulator, I thought was a little low for high-temperature applications. Are these designed primarily for systems without a regulator?

JESTER: That's right. We recommend not using a diode in installing these in a battery-charging system. They hook directly to the battery, and the leakage current on these modules at night is very low.

DE BLASIO: A couple of questions, one regarding the qualification of the modules. Are these Block V qualified?

JESTER: Actually, we have done internal testing to Block V and that testing has pointed, as we were developing the product, to areas that need improving. In fact, we have some modules we are starting to go through Ron's people to do some testing externally. We have been very successful in testing against Block V.

DE BLASIO: I was just curious, because if these were power-producing modules for residential application, I assume they will have to meet the UL and also the NEC requirements. Based on this morning's discussions, we have a double-insulated scenario relative to primary-secondary electrical insulation. Now I'm building up to the question: is the plastic acceptable in this case, where you have similar polymeric materials insulating an electrical conductor? Does that still provide you with a primary-secondary isolation?

JESTER: Maybe Russ can help me with the answer to that. The hi-pot on these, of course, is very good because there are no conductors.

DE BLASIO: I'm just bringing it up as a possibility: if you use similar materials, trying to protect or isolate from the electrical system, you will probably end up with a single layer of protection rather than a double layer. I think, with the plastic you get in the residential applications, you may get into that problem.

ROYAL: What are the commercial applications of Rovel?

GAY: The only UL-qualified hot tub uses Rovel. It is in standard use for fairly extreme conditions, chemicals, high temperatures, steam, and is able to meet the standards that you all have.

YERKES: You mentioned that you just put this on a battery and you don't need a diode at night. Is this because of amorphous material not being conductive in the dark? Is this a feature of amorphous modules that you are all finding, or is this just an ARCO Solar finding?

JESTER: I can't speak for the rest of the people making modules, but we have set up tests with modules and batteries and found that the leakage current at night is so low that you don't have to worry about that. Maybe some of the other manufacturers can answer that.

ROSS: The Coast Guard has done quite a bit of studying and has found that even crystalline-silicon modules generally do not require a diode relative to battery charging, and the reverse leakages are very, very low.

JESTER: We have measured numbers much less than a milliamp in reverse. If you look at that over tens of hours of darkness, it doesn't add up to very much. It is a negligible power loss for what you are putting in, even at low light levels. The module at low light levels still produces very high voltages. Our fill factor actually gets much better at low light levels because of the front conductor that everybody has mentioned. So at lower light levels it's a very good fill factor, and our voltage is retained, so even on a cloudy day we are going to be putting juice into the battery; we are not going to be feeding back.

ROYAL: You are charging 400 millimeters?

JESTER: That's right. In ratio to that, you look at the time. It's very small.

KNIAZZEK: Two questions. It was mentioned that the polymeric frame was good in high-temperature, active situations, and yet it seems that the bond is not totally integral between polymeric frame and glass, thus it is not a total water seal. That would imply that the EVA overhang was an inadequate moisture barrier. Is that the case?

JESTER: That's actually what we rely on for our moisture resistance of the laminate itself. And, like I mentioned, the RTV helps in our connection area. You are right that the frame is not where the hermetic seal comes from; it comes from the way we package the glass-glass in EVA.

KNIAZZEK: Another question. You mentioned that the pigtails are soldered to a printed circuit-material. Could you comment on how the printed-circuit material is bonded to the active photovoltaic material?

JESTER: It's actually by ribbons, standard soldering to the part, and then to the printed circuit board.

KNIAZZEK: Standard soldering to the metallic-back contact? Would you comment on what that material is? The back contact?

JESTER: I would rather not.

ROYAL: As you went through the several design evolutions, were you running tests and if so, were you changing largely due to aesthetics, or was it because they did not pass Block V type tests? Is that what happened before you went to glass on glass?

JESTER: As I mentioned, all of our prototypes and design evolutions use the EVA glass front and metal or glass back, so that gave us our environmental seal. And the frame, that was the other issue. Of course, as Ron mentioned this morning, if you put products out and you have not tested them, that is not a real good position to be in. Of course we were testing as we went along.

D'AIELLO: Ed's (Royal) question brought another question to mind. None of your evolutions used standard ARCO backing, which is EVA Tedlar. Did you find something particular about this module that precluded that?

JESTER: Actually, we wanted to get more mechanical strength from the back sheet than our standard material provides.

D'AIELLO: It wasn't a function of the protection?

JESTER: No, not at all. In fact, EVA-Tedlar is the material on crystalline-silicon modules that passed Block V at JPL. So it is a very good material, and the mechanical strength is the reason that we went for the back sheet.

D'AIELLO: The question that I came up to ask really relates to the design with the 25 segments, and the specified 14 1/2 volt operation to charge batteries. My question relates to the voltage that you get out of a module versus the charging voltage. It seems that you are awfully close to the minimum required for charging batteries as they charge up. And if you were to lose a segment for some reason, your yield is impacted dramatically. I wondered why you didn't design it at a higher voltage for charging 12-volt batteries.

JESTER: The max power voltage when we first manufactured the module was higher than that. We have sized the power over that, so that as the product stabilizes it's at the specifications that we publish.

D'AIELLO: So what you are saying is the actual measured $V_{max}$ will be higher than the 14 1/2 specified initially?

JESTER: Initially, and then as it stabilizes it becomes closer to what we specified.

D'AIELLO: What length of time do we expect it to take to stabilize?

JESTER: It will be about a month. Of course, it depends on the weather conditions and where it is installed. Like I said, we have oversized the initial power; we put out much more than 5 watts at the beginning.

D'AIELLO: So the 25 segments are giving you an operating voltage of well over 14 1/2, and you expect the voltage to drop because of fill factor degradation?

JESTER: As Chris Wronski has talked about, everybody is aware of it.

ARNETT: I just wanted to respond to, and add a point to, the gentleman's question about the EVA from Kodak. I just wanted to comment that the modules that we supply to Sacramento Municipal Utility District as part of their PV program use an encapsulation system that does not employ an edge seal, so if you have a glass-EVA in

the back-sheet laminate and it has been through Block V qualification -- we feel that the approach here, even though this frame does not provide a complete contiguous seal, is certainly an acceptable and durable lamination and encapsulation scheme for withstanding the humidity-freeze and other environments in Block V.

YERKES: I think a couple of questions have come up about this ARCO Genesis module. This thing is not designed to be a large SMUD array module; it was designed for a specific market where one module primarily is sold to self-regulate a charge on a 12-volt battery in a boat, or something like that, and therefore it is targeted at something not requiring those leads to fit 20 or 40 panels together. It has a big wide frame around it, and things that you wouldn't do if you were going for high efficiency, but it is going to sell.

SOHIO
Solar Systems™

# AMORPHOUS SILICON
# MODULE DEVELOPMENT IN SOHIO

DR. ROBERT A. HARTMAN

# SOVONICS:

STARTED 1981

JOINT VENTURE BETWEEN THE STANDARD OIL COMPANY AND ENERGY CONVERSION DEVICES

STARTED 1983

MODULE DEVELOPMENT GROUP

STARTED 1984

PILOT PLANT

DEPOSITION AT TROY , MICHIGAN

MODULE FABRICATION AT CLEVELAND , OHIO

## AMORPHOUS SILICON:

THIN STAINLESS STEEL SUBSTRATE
(14" WIDE * 1000' LONG)

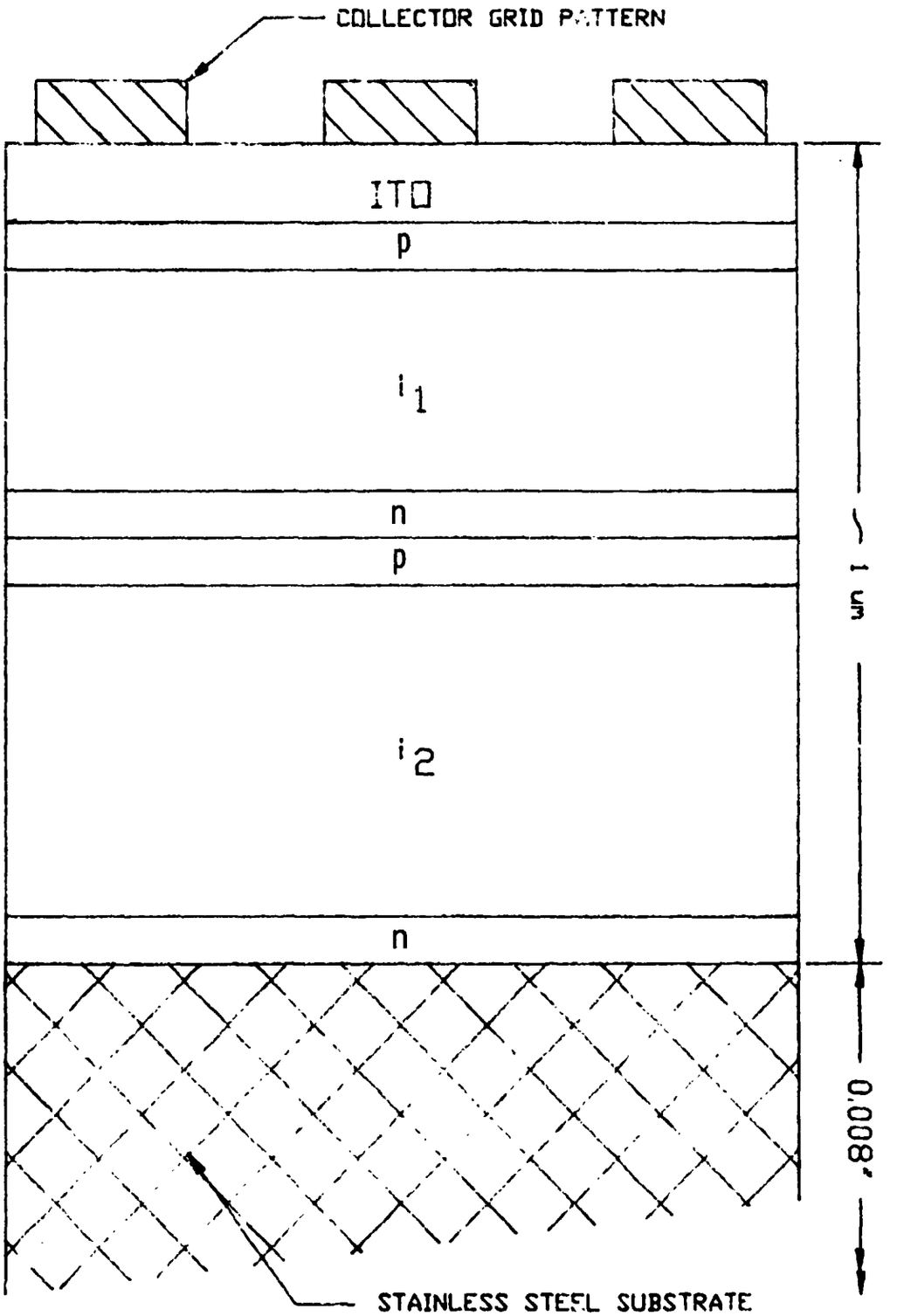
TANDEM

ITO TOP CONDUCTOR

## METALLIZATION:

SILVER INK

A-SI TANDEM CELL PROFILE



# MODULE CIRCUIT

14 CELLS IN SERIES

120 INTERCONNECTS CELL TO CELL

14 BY-PASS DIODES LAMINATED IN MODULE

## ENCAPSULATION

TOP COVER - TEDLAR

ENCAPSULANT - EVA

BACK COVER - PET / TEDLAR

## GASKET

EPDM RUBBER GASKET

## FRAME

FOAMED , GLASS FILLED POLYCARBONATE

INJECTION MOLDED

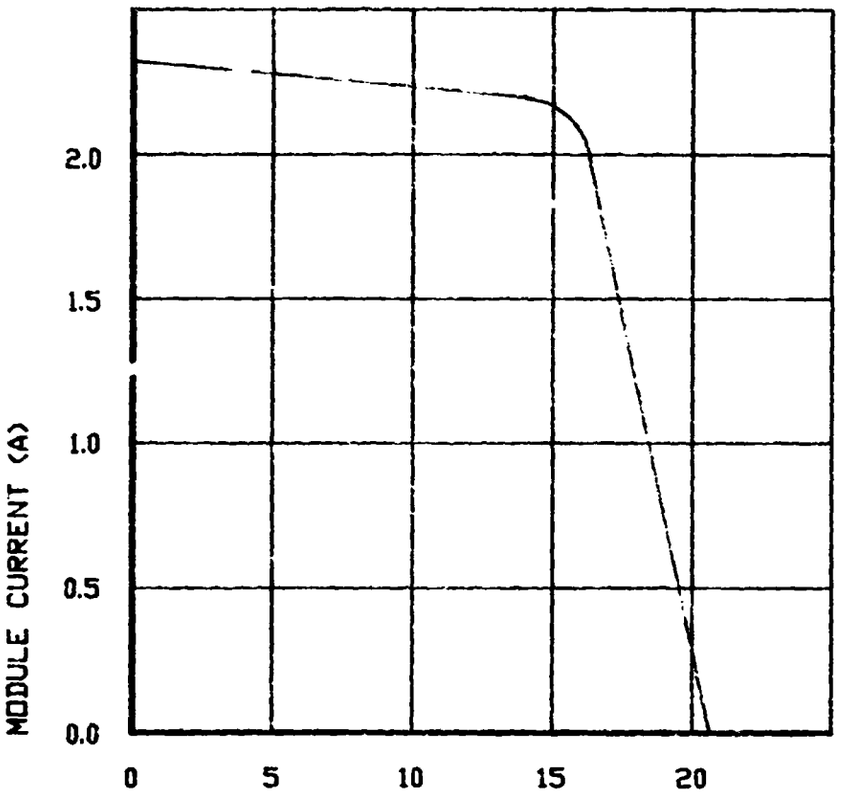
# SPECIFICATIONS:

DIMENSIONS: 119.3 * 59.2 * 4.5 CM.

WEIGHT: 5.4 Kg.

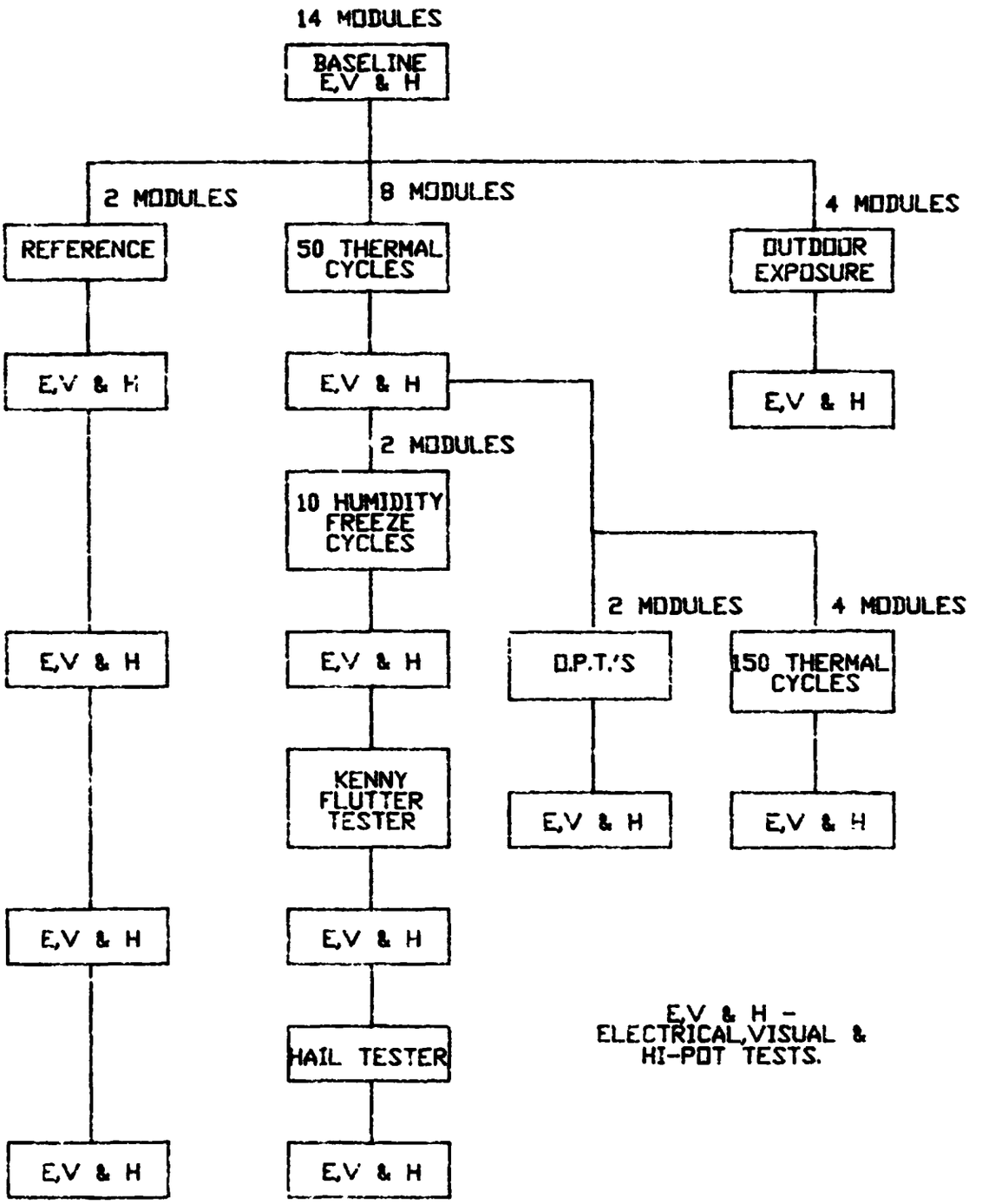
POWER: 32 W ±10%
(@ AM 1.5 GLOBAL 100 mW/CM$^2$ , 25°C)

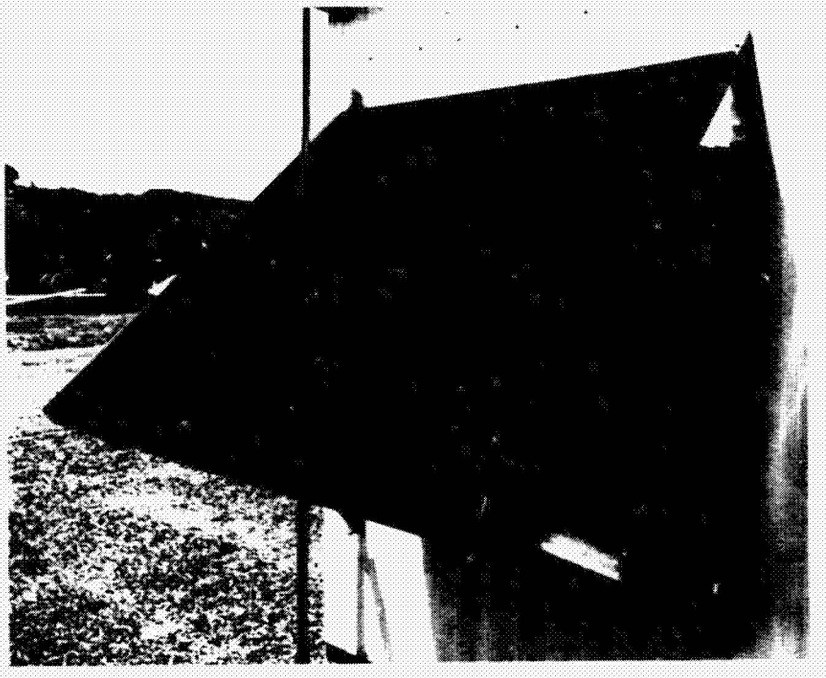
MECHANICAL
LOADING: 50 PSF



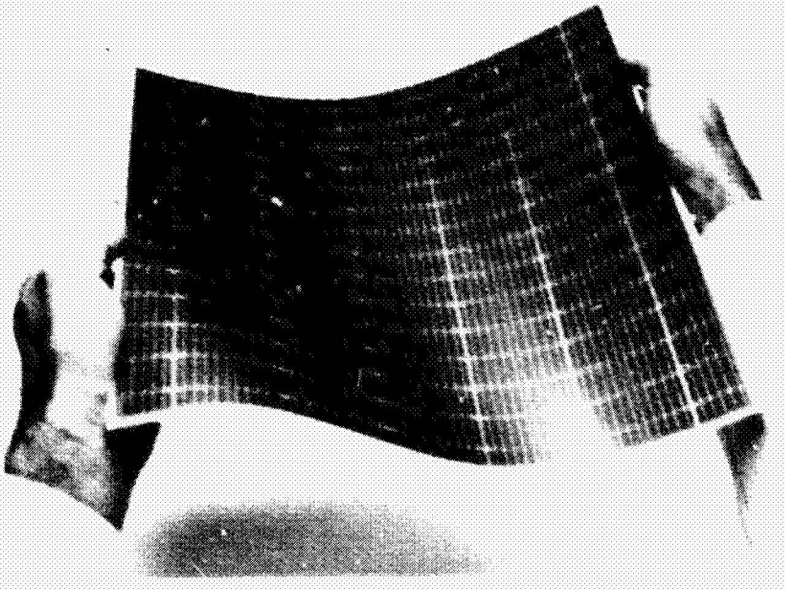

VOLTAGE TEMPERATURE COEFFICIENT -0.42 mV/°C
CURRENT TEMPERATURE COEFFICIENT 1.2 mA/°C

# QUALIFICATION TESTS





Sovonics a-Si 32-Watt Modules



Flexible, All Polymer Encapsulation System (no glass)

## DISCUSSION

ROYAL: You have a shingle-type interconnection scheme between adjacent cells -- would you talk about how this is done and if there were any problems?

HARTMAN: There is a problem if you don't do it right, I guess. That is probably true with all things. The shingle buys us something -- we can hide some things behind that shingle, of course, so we can put all kinds of tolerances under the shingle, which surely is attractive, but actually it requires the laminates to be slightly stronger. It is a pity we cut up the stainless steel and then interconnect them back again. By having a small gap in a shingle we gain some of that back. We re-glue the things to stainless. It is a potential area for shorts, of course, if you have problems, but I think we solved that.

VAN LEEUWEN: I understand you have a continuous process and then you chop that thing up into tiny little increments? And then you solder interconnects between those shingles, or wires?

HARTMAN: Let's say they are connected with wire.

VAN LEEUWEN: You mention flexibility of that basic unit. What kind of a flex radius will it take without having spalling of the amorphous surfaces?

HARTMAN: We have gone for the basic material by itself, we went down to something like a centimeter radius, and that's not really a problem. I don't know if you want to do that a million times.

LESK: I'm sorry, I did not understand about shingling. I thought shingling was used to interconnect cells like in space modules, or it used to be, but now you are using wires also? What is being shingled and what is connected by wires?

HARTMAN: We connect the central part of the cell to the back of the neighbor cell. If you look closely you can see the arrangement. Of course, it buys us a lower resistance loss that way. The shingle joined by itself is not a conductive joint, it is a mechanical joint.

LESK: How thick is your Tedlar?

HARTMAN: I think the total is something near 50 mils.

LESK: Are the ribs glued to the back?

HARTMAN: Yes, the laminate is attached to the frame.

ARNETT: With respect to your test sequence here, do you have any feeling on what you are going to do with this in a hail test? You've got this plastic front and the molded-plastic back sheet is certainly

going to give. The test requires that you hit the module in nine of the most likely, suspect places, among those being the point at which you have 3-mil-diameter wires, which are of course, at a point where you could have a fairly substantial bending radius, substantially less than a centimeter. Any thoughts on changing that front surface over to a glass, or anything like that, to take care of the hail requirement?

HARTMAN: No, I don't think we need to. Of course we have to clarify that the hail balls will leave an indentation; they won't degrade the performance We are not contemplating coming out with a glass-faced module.

ROYAL: You said it was a shame that you had to cut the stainless steel substrate. What are the technical advantages over superstrate?

HARTMAN: Well we have flexibility that a superstrate product does not have. The shading is not that great, 2% or 3%, and you buy that back in resistor flaws reduction. It's a tradeoff.

JESTER: One of the difficulties we have always had in laminating the films is stretching, expansion and contraction, and we always had problems with things pulling together. Do you see a yield problem with that as you deal with both these stretchable films?

HARTMAN: No. It took a while to get the technique down to some process where it works out all right. At present they are doing fine. It took a while to get that out, things like wrinkling and all kinds of little problems, we have that under control. I think it is reasonable now.

D'AIELLO: Could you please comment on the expected performance of the electrical characteristics that you gave as a function of time?

HARTMAN: The 32 watts is derated for our own specification -- that's after our expected degradation. When we will reach that, and how much, we are really still working on.

D'AIELLO: Can you comment on how much a customer can expect to experience in change during the first month or so of operation?

HARTMAN: No, I can't.

YERKES: What kind of adhesive is used?

HARTMAN: EVA.

YERKES: So you put the back sheet, the EVA and then the metal, then EVA and then the Tedlar?

HARTMAN: Yes.

YERKES: Congratulations on building a large module. I think it took a lot of guts and I hope ARCO and Chronar can catch up with you.

ROYAL: You have an option of not interconnecting each individual subcell?

HARTMAN: Yes, we built a piece of equipment that takes 60 of these small cells on a strip. Then we gather data for each cell. We get a multitude of data.

ROYAL: Do you try to match them?

HARTMAN: There is some matching done at the moment, I'm not sure if we want to do that in the future.

SHIMADA: What is the advantage of using tandem cells in this particular module, in comparison with a single-junction, other than gaining the voltage?

HARTMAN: Well, it's not only gaining the voltage, it's reducing the current, which always helps, and it reduces light-induced degradation.

SHIMADA: The efficiency seems to me about the same as the single-junction module. Perhaps the production costs might be a little higher?

HARTMAN: The initial efficiency is the same; the long-term one is much better.

ROYAL: Have you observed light-induced degradation with your tandem cell? It has been said to be less susceptible to it than single-junction cells.

HARTMAN: There might be certain types of tandem cells that don't have it, but we have seen some.

LESK: Congratulations. You are doing a super job using a tandem cell; you have got 1 1/2 volts open-circuit voltage. Can you say if you are using an alloy for the underneath junction?

HARTMAN: The amorphous-silicon material is hydrogenated and fluorinated.

LESK: But there's a lower-band-gap material on the bottom side?

HARTMAN: It is germanium-doped, or something like that.

TYAN: My understanding of the tandem cells is that you have to match the current output of the bottom cell with the top cell. I assume you will have different spectral response. I also assume that your cells optimize with respect to 1.5AM spectrum. Do you see a faster degradation of your cell output in morning, afternoon, or a cloudy day? When the spectrum changes?

HARTMAN: Yes, there is actually some of that effect.

YERKES: The machine that you showed a picture of was one that Stan Ovshinsky was building while I was giving him a contract at ARCO Solar. You said that has gone to Japan and he has a new one now. I think one of the problems with large continuous rolls, at least from having looked at it for five years, is that those machines are quite expensive, and the paradox is that the roll moves relatively

slowly because the deposition time is still fairly long. That is a key problem people are working on -- deposition rate. That's one of the reasons why people struggle to make very thin layers of amorphous. But the other problem is that the thin layers can tend to have pinholes or other problems. Making two almost identical or similar layers of just amorphous hydrogen or silicon alloy can solve some of those problems in separate compartments. I'm just assuming or guessing that those are some of the things that lead to that kind of a decision with this product. I think the die was cast on making that flexible thing a long time ago. I think for this meeting, in general, it's an issue that we are getting into that is real exciting, because now we are starting to look at the manufacturing methods on a large scale, glass superstrates versus some other methods. I don't think the final answers are in on that.

**KNIAZZEK:** You mentioned the silver paint and some temperature testing. Have you seen any effect of diffusing silver into silicon in temperature testing? What temperature testing have you done?

**HARTMAN:** I think 90°C. Of course, lamination goes 150°C. We have not seen silver migration into the device; we have not found it.

**ROYAL:** Now we would like to hear about the design process that led you to select Tedlar for the front cover.

**HARTMAN:** A very common top cover material at present is glass; we did not choose to use that. Organic films are quite stable. Tedlar is quite a good material. It comes to how far you load it with UV inhibitors and a lot of other goodies in that film. This was a grade that we tested for a long time. We have been through quite a number of variations of this material -- also, in conjunction with EVA behind it. There are some combinations that don't hang in at all and there are some we are quite confident about. Obviously we chose one we are quite confident about. I am not sure if we will stay forever with Tedlar; we are looking at higher fluorination levels. The problem, though, is that you also get a film that is extremely hard to bond to. Also, we have very low soiling rate.

N86-12769

# AMORPHOUS SILICON PHOTOVOLTAIC MODULES AND TEST DEVICES DESIGN, FABRICATION AND TESTING

MATT VAN LEEUWEN
HUGHES AIRCRAFT COMPANY
LONG BEACH, CALIFORNIA
MARCH 20, 1985

In July of 1984, Hughes and JPL initiated a contract for Hughes to design, fabricate and test 10 thin film Amorphous Silicon (a-Si) photovoltaic power modules. These modules were slated to be 1 ft x 4 ft in size. They were to be preceded by the delivery of 10 a-Si 4 in. square test devices.

This effort is very timely since thin film PV development has progressed to the point where intermediate load power applications are on the horizon. It's important to know if current a-Si submodule design and manufacturing processes yield a product that is compatible with the packaging needed to meet a 20 to 30 year life span expectancy. The term submodule is assigned to an interconnected assembly of 28 a-Si cells deposited on a 1 foot square glass superstrate. Our next viewgraph depicts a set of four of these submodules. Two are shown face up and two are inverted. Naturally these assemblies are equipped with electrical terminations which appear in the picture as copper tabs at the four corners of the inverted submodules. It is these submodules that we are interconnecting and packaging into power modules, as opposed to the interconnected individual crystalline cells packaged into todays PV modules.

The primary purpose of my talk today is to acquaint you with the experience gained and the lessons learned while performing this task. Since the primary objective of this effort is to evolve an environmentally survivable thin film module, an integral part of this program is the testing and evaluation of the various materials and manufacturing processes used in module fabrication. The test results help us identify and rectify problem areas which may prevent us from achieving the desired survivability. Final environmental testing will be performed by JPL to their Block V Design and Test Specifications for Intermediate load applications. To facilitate this testing, ten 4 in. square test devices have been delivered to JPL to allow them to characterize the spectral response of the a-Si cells and to build standard cells.

The a-Si test devices and submodules for this program were bought from an a-Si submodule manufacturer with whom Hughes has agreed to collaborate in establishing the requisite submodule design changes required to produce a field ready module. Some of these changes will be discussed later. The test devices are 4 in. squares cut from a 1 ft square submodule. This small device has 8 series interconnected a-Si cells which are terminated at the opposing edges. The rear surface configuration is shown on our next viewgraph. The rear surface is coated with a black vinyl protective paint with exception of the two termination pads and a bare strip down the center. This strip was provided at JPL's request to allow contact to the individual a-Si cells for detailed output characterization. The terminations consist of 1/2 in. wide copper foil tape with a conductive adhesive. This acrylic adhesive contains a 3% dispersion of tiny copper particles equal in size to the nominal adhesive thickness. It is applied full length along opposite edges of the test cell.

Shortly after contract award, a kickoff meeting was held at JPL to share views on module design and testing. JPL cautioned us to seam the submodule edges to help minimize breakage due to thermally induced stresses. A lesson learned from the JPL Block II module installation at natural bridges is that a substantial percentage of modules having untempered glass superstrates have broken during their several years of environmental exposure. This information was relayed to the submodule manufacturer and the submodules were received with seamed edges.

The design philosophy employed during the module design effort is quite conservative in that it borrows heavily from current module design practice. Our next viewgraph lists the design features shared with current production modules.

The tempered low iron glass superstrate has become a standard feature on almost all intermediate load application modules. It withstands the physical rigors of JPL's hailstone, wind loading and thermal testing and also has an excellent track record of environmental survivability.

EVA has developed into the encapsulant of choice for most PV module manufacturers. Its lower cost, hygroscopic nature, thermosetting properties, and ease of processing have gained it a leading position over the silicones and PVB which were formerly popular.

Tedlar is a very commonly used module back cover. Its availability and excellent performance history made it our choice. Conveniently, it is available already laminated to a sheet of EVA.

An AMP J-box with its accommodation for an integral bypass diode was chosen as a simple, reliable module termination. Its successful history and availability made it an obvious choice. The fact that AMP donated them for this project is appreciated.

The extruded aluminum frame sections designed for this job are depicted on our next viewgraph. Again, our goal was to minimize surprises. The sections are simple, open extrusions designed for self-tapping screw assembly. The only reason that an available extrusion couldn't be applied to this project is the extrusion's 0.4 in. wide laminate groove. This wide groove is required to grip the double glass laminate plus an adequate rubber gasket.

Our next viewgraph shows a typical section through a modules side rail/laminate interface. Beginning at the top we have the superstrate glass laminated to the a-Si submodule with a layer of EVA. The tedlar back cover is also bonded to the submodule back surfaces with EVA. The copper tape terminal is shown in section as it runs along the entire length of both module side rails.

Surrounding the entire periphery of each laminate is a layer of Kapton film tape. An enthusiastic vendor reported that this tape has a dielectric strength of 10,000 volts and it was thought that surely this would readily handle the 3,000 volt Hi Pot test requirement. To assure the electrical isolation between the circuit and the frame, a 0.06 thick rubber extrusion was applied along all edges of the laminate. This gasket was to protect the film tape from damaging contact with the frame and also to provide additional electrical insulation.

Figure 7 is a schema 'c diagram of the module. The 28 cell series are oriented across the module width and are interconnected in parallel along the modules 4 ft sides. The AMP J-box is located near a module end and accommodates the bypass diode.

Figure 8 defines the material used to wire the laminate assembly. Redundant copper ribbons join each submodule terminal end. Heavier copper ribbons bring the module output to the J-box area where they are attached to copper solder pads. After lamination, a 1/2 in. square of tedlar and EVA is removed from each solder pad and the AMP J-box leads are soldered on.

With the basic module design established and the required hardware and tools gathered, the fabrication effort began.

Component and process testing is an integral part of this type of prototype development effort and in this case it began with the submodule. The search for a locally available facility capable of accurately evaluating a-Si performance proved fruitless. JPL agreed that a comparative output evaluation would be sufficient to allow the matching of submodule peak power voltages for efficient assembly into modules. We were aware that a-Si modules tested in a simulator calibrated for crystalline modules would show a diminished reading, but the 45% loss of output indicated by our measurements on a Spire simulator took us completely by surprise. The submodule manufacturer suggested outdoor testing using a crystalline reference cell. This testing was performed and it resulted in higher output measurements than the Spire readings. As a final check, three submodules were returned and their initial output measurement was verified. Lamination testing could now begin.

Test laminations were made to settle two questions. First, would a craneglass layer be required between the glass panes to facilitate laminate evacuation and second, would the submodule protective back paint be compatible with the EVA encapsulant? The craneglass showed up as milky swirls in the first lamination sample, but destruction of the first laminate revealed a strong bond between the manufacturer's paint and our EVA. Test laminate No. 2 showed that eliminating the craneglass caused no visible lamination voids or defects.

Following lamination testing, submodules were grouped by their peak output voltage and functional laminate stacks were assembled. They were then interconnected in the manner shown on our viewgraph. Adjacent submodule edges were cushioned with a layer of teflon film tape to prevent contact. Kapton tape was used to hold the submodules together and in proper location on the tempered glass superstrate since the lamination tests had shown that the submodules tended to shift during lamination.

With all the known possibilities for failure accounted for, we laminated our first two laminates on a Spire type laminator. The result was disappointing. One of the submodules had broken during lamination resulting in a 50% lamination yield on our first attempt. Obviously our 30% failure allowance would not cover this low yield. We then used a laminating oven. It was rationalized that the oven's air heating and cooling would yield a softer laminating environment.

Oven lamination didn't yield improved results. Submodules kept breaking. We tried adding 15 minutes to the cooloff period. At first we thought it was helping - until the next submodule broke. Metal strips of laminate thickness were then placed around the laminate stacks to relieve possible edge pressure from the flexible laminating envelope cover - also to n avail.

Since our resources for lamination process improvement were exhausted, we were forced to look to the submodules for a solution. The edge quality of these units, while seamed, could still be improved. The submodule edges sometimes contained a number of chips, notches, and cracks. The seaming operation removed the sharp edges while the larger imperfections remained. It is felt that these defects were a possible source of submodule breakage and steps are being taken to eliminate this possibility in future laminations.

After our module component resources were exhausted, we had 7 visually acceptable laminates. These units had patches of tedlar and EVA removed from their terminal solder pads, the AMP terminal loops were soldered on, and the AMP J-Boxes bonded in place with the recommended scotchgard #3501 epoxy.

The terminated laminates were then electrically tested and the numbe of acceptable units fell from 7 to 6. The low output module was the first one successful laminated and we failed to insulate the bus strips leading to the solder pads on this laminate. It seems likely that the copper ribbon or a solder pad shorted through the submodules protective paint to the electrically active aluminum cell layer beneath. The healthy laminates were then edge-taped with kapton film to provide the HiPot insulation and rubbe gasket segments were cut and installed into the framing parts.

Initial attempts to fit a frame to a laminate were foiled by a sticky, incompletely cured rubber gasket material. This material exhibited a tendency for the gasket channel legs to fold into the frame groove rather than slip over the laminate. To ease the assembly task, a rubber lubricant was applied to the gasket and laminate edges. Assembly then progressed smoothly.

After framing and a final cleanup, the modules (as shown on our next slide) were taken to the HiPot testing area. An Associated Research 5 KV tester was used. On the initial HiPot test, the module failed so completely that the tester was deemed suspect. Testing a standard module restored our confidence in the tester. We tested more amorphous modules with continued failures. Subsequent investigation showed the rubber lubricant to be quite conductive and the rubber insulating gasket without lubricant passed an Amp of current over an inch of length at 500 volts. Obviously, improved insulating materials and methods are called for.

A meeting was held at JPL on the eleventh of this month to discuss design improvements. A few salient points were agreed on. First, the sharp corners at the submodule edge imperfections are electrical stress points which can increase the electrical pressure significantly during HiPot testing. We now have another reason to improve submodule edge finish. Second, rubber is not necessarily a good insulator. Fillers can increase conductivity dramatically - carbon black being a leading contender for this honor. Third, the distance from the module circuit to the frame should be increased. Crystalline modules

typically have the circuits inboard about 1/4 to 1/2 in. from the frame. Our modules have the a-Si circuit about a sixteenth of an inch from the aluminum frame.

These lessons have been integrated into an improved module design whose edge configuration is depicted on Figure 10. To implement this new arrangement, we will acquire superstrate glass about 1/2 in. larger in length and width. While this change adds a 1/8 in. wide inactive border around the modules periphery, it will also eliminate the 2% average output loss experienced by our laminates due to frame shading. In fact, the elimination of cell shading at oblique sun angles will further reduce module efficiency losses in the field.

To accommodate the larger superstrate, new longer frame pieces will be fabricated and a thicker gasket of greatly improved electrical resistance will be used. EPDM and silicone rubber both promise to provide the required insulation; HiPot testing them will firm up the choice. The kapton tape has been eliminated from this design. We feel that the HiPot requirement can be met without it and at $26.00 per roll, it is not conducive to the attainment of low cost goals.

## SUMMARY

The Submodules initially received were very early production units. Future units are expected to reflect improvements in glass cutting and finishing processes. We are looking forward to greatly improved lamination yields and to an acceptable HiPot capability in the future.

Figure 1. JPL Contract No. BD-8024 19

WITH: HUGHES AIRCRAFT COMPANY

FOR: AMORPHOUS SILICON PHOTOVOLTAIC MODULES AND TEST DEVICES

DELIVERABLES: 10 EA. - 1 FT. X 4 FT. aSi MODULES WITH A MINIMUM OUTPUT EFFICIENCY OF 3 PERCENT

10 EA. - 4 INCH SQUARE aSi TEST DEVICES

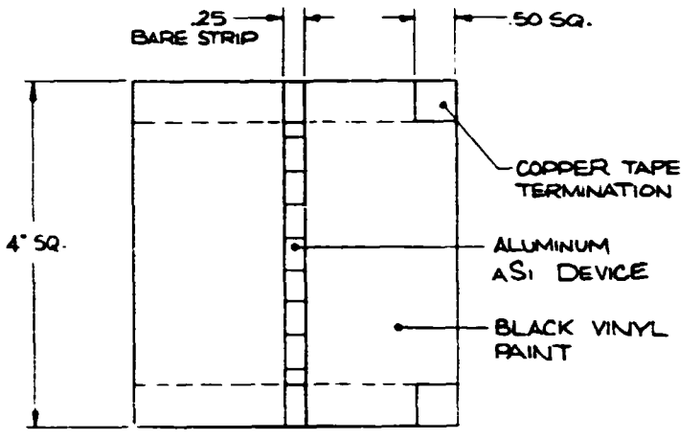
6 EA. - DESIGN DRAWING SETS

1 EA. - AN ORAL PRESENTATION WITH 25 SETS OF PRESENTATION MATERIAL

DURATION: 11 MONTHS

Figure 2. Four Submodules Prior to Final Framing Assembly Steps

Figure 3. a-Si Test Device Details




REAR VIEW

## Figure 4. Shared Module Design Features

- TEMPERED LOW IRON GLASS SUPERSTRATE
- EVA ENCAPSULANT
- TEDLAR BACK FILM
- AMP NO. 121033-1 J-BOX WITH BYPASS DIODE
- EXTRUDED ALUMINUM FRAME

## Figure 5. a-Si Module Frame Sections

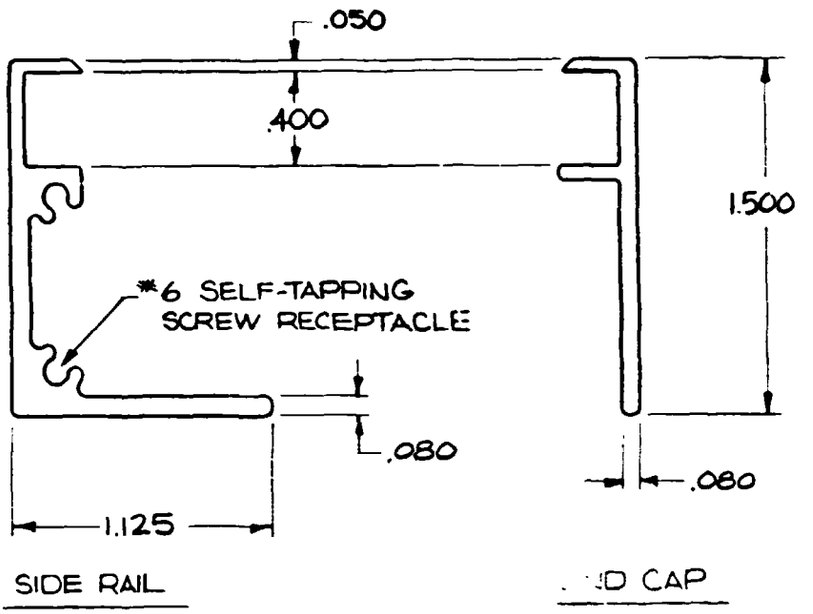


Figure 6. a-Si Module Edge Section

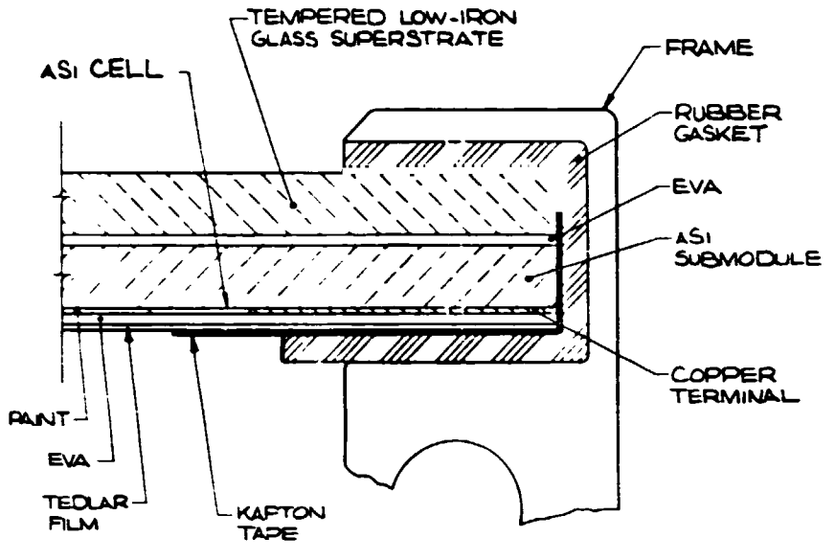



Figure 7. a-Si Module Electrical Schematic

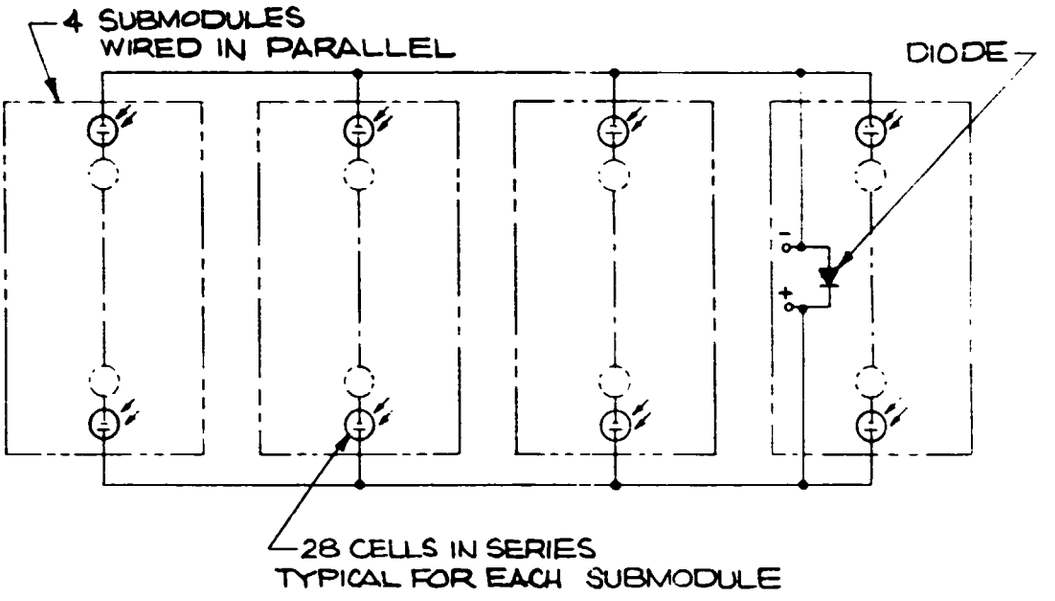


Figure 8. a-Si Module Interconnections

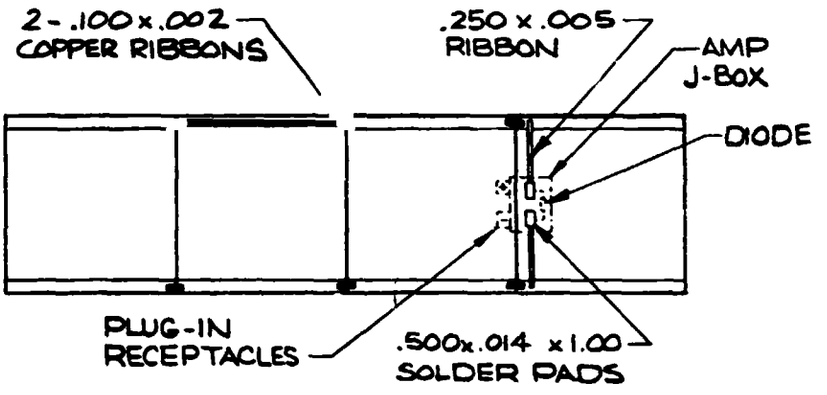


Figure 9. Two Framed Module Assemblies

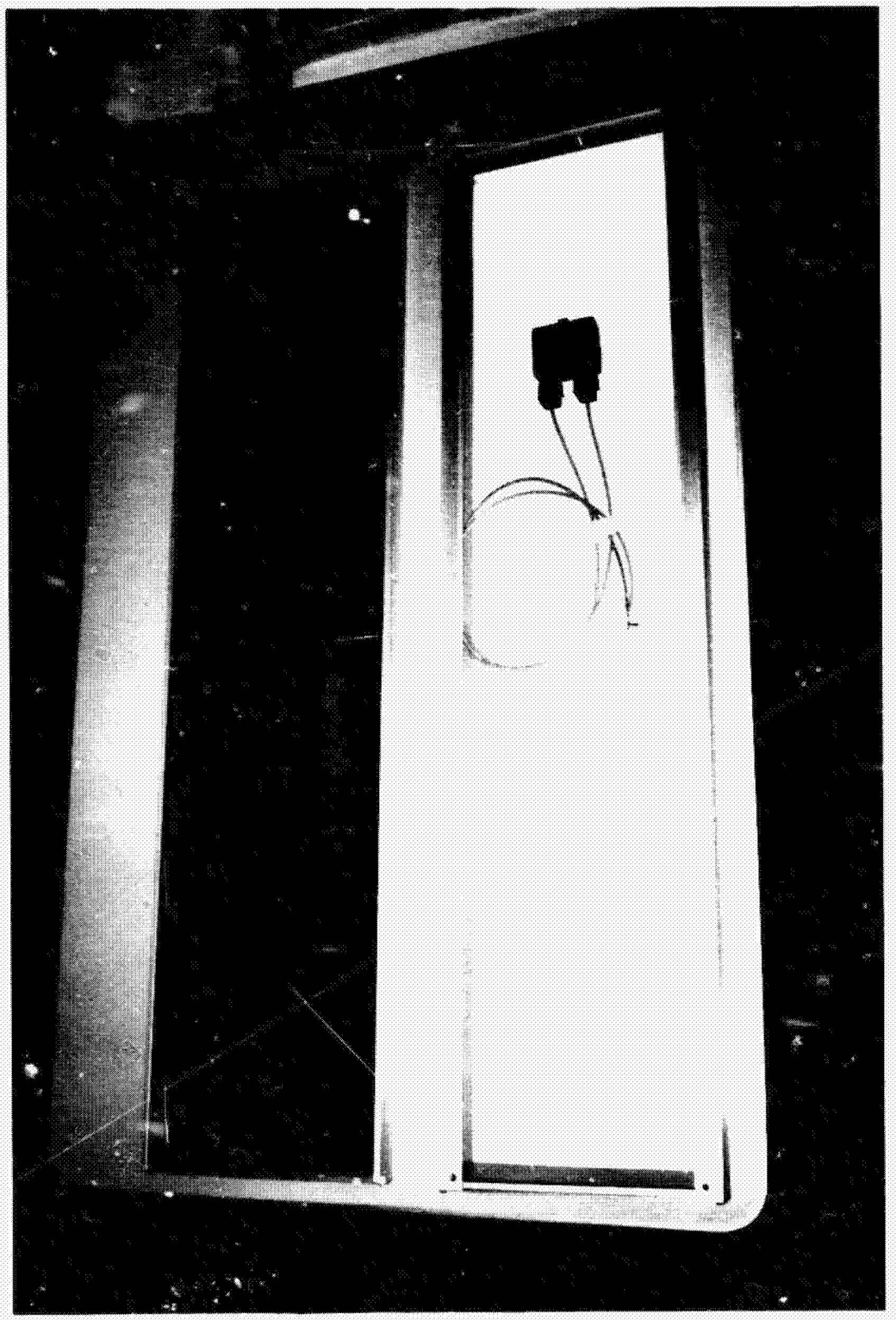
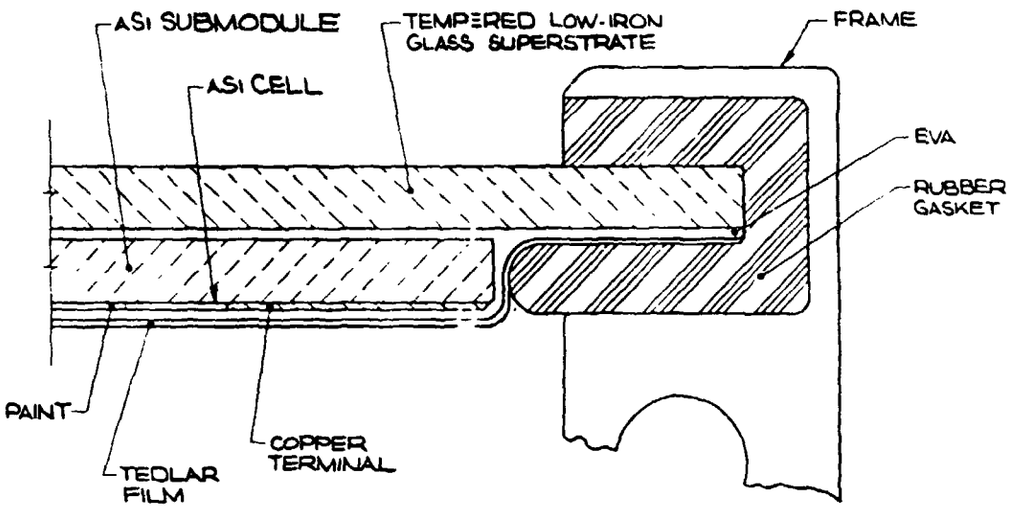


Figure 10. Improved Module Edge Section



## DISCUSSION

YERKES: I would like to know, after you have gone through this, what your opinions are about, say, offering a mass-produced module for large-scale use that uses a lot of 1 $ft^2$ parts? Is that something you think could be done cheaply, or should we get away from that? What are your thoughts on that, now that you have done it?

VAN LEEUWEN: Well, I think laminating several 1 $ft^2$ parts into a larger module is a good way to lose a lot of good pieces, because I have not been able to disassemble a laminate, and I don't know of anyone else that has. And if you can successfully produce submodules of the size of the finished module it would eliminate the frustration of having one pane break out of four and having to throw all four away. So I would think that the larger amorpnous part would be more desirable. If lamination yields and techniques are improving to the point where yield is high, then it probably is a very viable thing to do that. However, you are still burdened with the interconnecting task, putting several pieces together into a large one.

LESK: What is the advantage of using two panes of glass with EVA between, instead of one for the upper part of the module?

VAN LEEUWEN: This submodule is a non-tempered unit. Its strength is, I think, not high. The baseline requirements of this effort were to produce something that would pass the JPL Block V test, which includes hailstone impact.

ROYAL: You mentioned that you had done some measurements. Did you do indoor measurements, and if so, where and how did you do it?

VAN LEEUWEN: On a Spire simulator set up for testing crystalline modules with a crystalline standard. A standard simulator set up to test a crystalline module -- if you put an amorphous module in it, the power will fall almost by half. The spectral response must be radically different to do that, and going outdoors then brought this up less than half way back to the original readings.

CLARK: We were able to filter the reference cell on the Spire tester, crank up the light level and obtain readings within 10% to 12% accuracy. You can use the Spire tester if you fix the reference cell to respond closer to what amorphous might.

## SESSION III

## RELIABILITY RESEARCH AND PERFORMANCE INVESTIGATION

Chairman: R. Ross
(Jet Propulsion Laboratory)

N86-12770

# Thin Film Module Electrical Configuration vs. Electrical Performance

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## INTRODUCTION

In spite of the worldwide interest in thin film Si:H (TFS) as the leading thin film PV material, relatively few reports on module and device design have appeared. The differences in performance and design options for TFS relative to crystalline Si are significant enough to warrant redevelopment of much of the current design methodology which is largely based on crystalline Si. In Section I below, several aspects of this design issue which have been addressed by the author will be reviewed. The intent here is merely to highlight the main points of those studies since they relate to the discussion in the following section and to the general issues of TFS module design. In the second section the effect of module stability on design is discussed. The changes in module output as they are presently known and understood impact future designs as well as some of what has already been done where constant output was assumed. Only the drop in initial output is treated below. Daily and seasonal increases in output due to annealing will be treated in future studies.

## I. REVIEW OF PERTINENT TFS MODULE DESIGN ISSUES

One of the early attempts at understanding how TFS based modules might work under actual outdoor conditions involved use of a Weather/Insolation simulation model (Ref. 1). The then known properties of early modules were fed into the model which could then predict performance at any location for an actual year in terms of total energy delivery. The results are summarized in Table 1 from that study.

**Table 1. Yearly Energy (Watt-Hours) Derived from PVSYS Runs for Cz and Si:H Modules**

| Location | Cz Si | TF Si:H | Ratio TF/Cz |
|---|---|---|---|
| Chatsworth, California | 16945 | 6794 | 0.4009 |
| Victorville, California | 18256 | 7319 | 0.4009 |
| Perth, Australia | 16115 | 6493 | 0.4029 |

The model had previously been used for crystalline Si (Cz Si). One of the outcomes of the exercise was a direct comparison with Cz Si. It was shown that on an energy delivery basis, TFS modules enjoyed a ~5% relative advantage over their Cz counterparts if they were identical in peak output. This advantage was partially due to FF intensity dependence caused by transparent conductor sheet resistance properties. Ongoing studies along these lines indicate continual modifications in performance which require renewed assessments. In general, TFS module design can be tuned to take full advantage of such differential behavior. The addition of stability performance to the data base discussed in Section II below is an attempt to do so.

As experience with module fabrication improved it became possible to construct modules according to predictions based on design simulation. This allowed the gathering of actual outdoor data over extended periods to compare with model predictions and to refine the input to such models. One such study (Ref. 2) was a comparison of two types of 30x30 monolithic modules, one with half the cell width and hence twice the number of cells as the other. These so called "single and double string" (two parallel strings) modules are shown schematically in Fig. 1. A cross section of the monolithic design is shown in Fig. 2. The difference in outdoor performance of the two modules is shown in Fig. 3. The difference in performance was primarily attributed to differences in FF intensity dependence because of the contribution to series resistance of the transparent conductor. As shown below, on a peak performance basis, design B was 7% more efficient than A.

| Ratio of: | FF | $I_{sc}$ | Eff | Yearly Energy |
|---|---|---|---|---|
| Module B / Module A | 1.13 | 0.95 | 1.07 | 1.05 |

Some of this advantage was lost on a comparison based on yearly energy delivery because of the lower average effective insolation that modules actually experience under real operating conditions. The choice of the best design had to be dictated in the final analysis by the application and by manufacturing economies.

A final area of particular interest to the TFS community is that of tandem modules. These are felt to be the means to achieving the 15-20% efficiency values needed for large scale implementation of PV (Ref. 3). These objectives are most likely to be met with Si top and Si/Ge alloy bottom devices. However, there are some potential near term advantages of Si/Si tandems over single cell devices (Ref. 4). A comparison of these module structures under actual outdoor conditions was recently undertaken (Ref. 5). The intent of the study was to gather data on actual performance to serve as input for modeling and simulation. A comparison of module output for a typical day is shown in Fig. 4. The modules with Si/Ge bottoms were observed to be less sensitive over the course of the day to changes in intensity and spectral content than their Si/Si counterparts. This is not unexpected and is primarily due to the greater spectral breadth of the Si/Ge alloys. As will be discussed below, the device thickness variations used in these structures have important stability implications. These will have to be included in future design efforts for tandem modules.

## II. EFFECTS OF STABILITY

### A. Stability Simulation

The details of stability related performance in TFS and the underlying mechanisms giving rise to this performance are still the subject of intensive study throughout the world. Just as the as-made performance varies from laboratory to laboratory, so also does the stability. The stability behavior of our devices is discussed in Ref. 6. In summary, we observe an initial loss of 10-15% which is a function of device thickness and details of preparation condition. The primary loss is in FF, with secondary losses sometimes observed in $J_{sc}$ and $V_{oc}$. Output is then stable and does in fact improve during warm periods due to an annealing process. Most of the initial loss occurs during the first 20 hours of exposure.

In order to simulate these losses for module design purposes a simple approach was taken. In essence, it is found that stability losses can be nicely modeled by considering them simply as increases in series resistance. This was demonstrated by working with 4 $cm^2$ test structures and showing correlations between FF and the power curve slope at $V_{oc}$. This correlation for devices in the as-made state, B (before), and degraded state, A (after light exposure), is shown in Fig. 5. A change in slope of one unit corresponds to an increase in series resistance of ~0.67 ohm for these devices. This behavior is also a function of device thickness as shown in Fig. 6. The slopes of these lines is a measure of the bulk contribution to $R_s$ in each of the states, while the zero thickness intercept is the interface contribution. It is seen then that the degraded state A derives from the B state through an increase in both bulk and interface components of $R_s$ and will be modeled accordingly. Further details of this analysis will be provided elsewhere.

### B. The Module Model

Details of the model used in this study are presented elsewhere (Ref. 2). For purposes of the discussion which follows, the aspect of interest is series resistance, $R_s$. There are two contributions to $R_s$, that due to the sheet rho of the electrodes and that due to contact resistance and to internal resistance of the photoactive material. The electrode resistance is dominated by typically high sheet rho's for transparent conductors and is described by standard distributed resistance formulas. The remaining components are lumped into the product of "$R_c$" and "contact length" (e.g. Fig. 7). What is shown as "$R_{series}$" in the data is the sum of these terms. Much of the analysis involves use of the $R_c$ term to simulate degradation in terms of increased series resistance as discussed above.

### C. Module Performance

The starting point for this investigation is the power curve for an actual 30x30 cm module which is shown in Fig. 7. The module configuration is 25 series cells "single string" as shown in Figures 1 and 2. The data shown in the figure are actually the simulation that resulted in a fit to this actual measured curve for the module. The actual and simulated curves for the module exactly overlap at 7% efficiency and 0.54 FF. The manner in which the fit was achieved will now be discussed. In Fig. 8 the measured power curve is

superimposed on a simulation of the "ideal" curve for the module. All of the data shown are for the ideal simulation. $J_{sc}$, $J_o$, n, T, area, module length, module width, cell width, cell length, and contact length are all variables whose known values as shown are input. $R_{sq}$, $R_c$ and $R_{shunt}$ are set at ideal values. The remaining parameters are calculated from this known set. As is seen, for $R_s = 0$ (total series resistance) and $R_{sh} = \infty$ (total shunt resistance), the module efficiency would be 8.75% with a 0.8 FF. It should be noted that the ideal FF of 0.8 agrees well with the extrapolated ideal from Fig. 6 for cells. The effect of including the known values of sheet resistance for the front (8 ohms/square) and rear (0.15 ohms/square) electrodes is shown in Fig. 9. These combine to result in a $R_s = 2.8$ ohms which reduces the FF to 0.74 and the efficiency to 8.2%.

Addition of the remaining series components will be accomplished by use of Fig. 6. First the contribution of the bulk photoconductor is calculated from the slope of the state B curve at a thickness of ~4500Å. For these 4 $cm^2$ test cells, a ~10% drop in FF is realized for each added ohm of $R_s$. Correcting this to the ~30 $cm^2$ cell areas in the module and to the fact that 25 such cells are in series results in the use of $R_c = 0.0167$ to effect an increase in $R_s$ of ~1 ohm. This has only a minimal effect on FF, dropping it to 0.73 (Fig. 10). Again referring to Fig. 6 to get at the interface component of $R_s$, and again using the above corrections results in use of $R_c = 0.071$ and a resulting $R_s = 6.8$ ohms. This doubling of $R_s$ due to the interface drops FF to 0.67 and efficiency to 7.3%. As can be seen in Fig. 11, the fit is close, but further adjustments are required.

All inputs to the model to this point are measured. Final fit however will be based upon observation rather than direct measurement. From the non-zero slope at $I_{sc}$ of the measured power curve, it is apparent that some shunting should be included. The effect of adding $R_{sh} = 1000$ ohms-$cm^2$ (or ~33 ohms) is shown in Fig. 7. This simulated curve with only one adjusted parameter, $R_{sh}$, is an exact fit to the measured curve for the module.

The final step in the procedure is degradation of the module. This is accomplished by use of the state A data from Fig. 6. Combining both bulk and interface components results in $R_c = 0.16$ and $R_s = 11.8$ ohms. This increase in $R_s$ of ~5 ohms drops FF to 0.56 and efficiency to 6.1% (Fig. 12), which corresponds directly to actual module behavior. It is to be noted that the degraded state was contributed to equally by bulk and interface losses. Solutions of either can bring module stability to the 95% vicinity.

A summary of the above procedures of first simulating and then degrading a module is given in Fig. 13. With the exception of a slight shunt loss, the entire process of loss is based upon accumulating series resistances. Opportunities for improving the as-made as well as stabilized performance of these modules lie with eliminating these resistances. Some implications of the present stability phenomena to module design are discussed in the following sections.

## D. Design Issues

### 1. Transparent conductor (TC) sheet rho

Since TC sheet rho and degradation both contribute to $R_s$, the optimum

sheet rho for a degraded module will not be the same as an as-made module. The effect of varying TC sheet rho for B and A states is shown in Fig. 14. In the high FF regime of low sheet rho, to first order there is little difference in the slopes of the B and A curves, and hence degradation is a non issue. Only at higher sheet rho values, where the degraded state starts asymptoting faster than the B state, is there some leverage. This is not a normal design regime for most applications however, and thus degradation does not play a significant role in module sheet rho choice. Broader, more leveraging issues such as transmission and cost trade-offs will still dominate.

2. Module cell density

For most current applications these modules have the constraint of generating voltages consistent with 12-volt battery charging or 12 volt devices. This and TC sheet rho largely drive cell size in 30x30 cm modules. The result is a series string of ~25 cells ~1 cm wide yielding $V_{mp}$ of 13-15 volts.

As mentioned above and discussed in Ref. 2, paralleling allows other options on cell size. Additionally, other applications not tied to 12-volt systems, such as utility grid power, largely relax $V_{oc}$ constraints. The effect on module design of relaxing this constraint is shown in Fig. 15. The trade-off that is occurring, as shown in Fig. 16, is that between FF and $I_{sc}$. FF increases with increasing cell density because the sheet rho contribution of the TC to $R_s$ decreases as cell widths decrease. $I_{sc}$ decreases in a straightforward way with decreasing cell width. Referring back to Fig. 15, it is seen that the 25-cell design is just below the efficiency peak which occurs at ~32 cells. Such a design would produce a $V_{mp}$ of over 20 volts, which is inappropriate for 12-volt systems and thus useful only in non-constrained voltage applications.

The effect of degradation is only a small shift in the design point. This is demonstrated in Fig. 17, which is a plot of the percent of state B output maintained in state A. As can be seen, in terms of stability performance the current 25-cell design is nearly a full percentage point below the peak of maintained efficiency (~86.5 vs. ~87.5). In terms of stabilized output then, the optimum design point is ~35 cells (for non-constrained voltage applications).

## CONCLUSIONS

The as made and degraded states of TFS based modules have been modelled in terms of series resistance losses. The origins of these losses lie in interface and bulk regions of the devices. When modules degrade under light exposure, increases occur in both the interface and bulk components of the loss based on series resistance. Actual module performance can thus be simulated by use of only one unknown parameter, shunt losses. Use of the simulation to optimize module design indicates that the current design of 25 cells per linear foot is near optimum. Degradation performance suggests a shift to ~35 cells to effect maximum output for applications not constrained to 12 volts. Earlier studies of energy based performance and tandem structures should be updated to include stability factors, not only the initial loss factor tested here, but also appropriate annealing factors.

**ACKNOWLEDGEMENTS**

Special thanks are extended to Kim Mitchell for use of the computer code and to Dennis Willett for cell thickness data.

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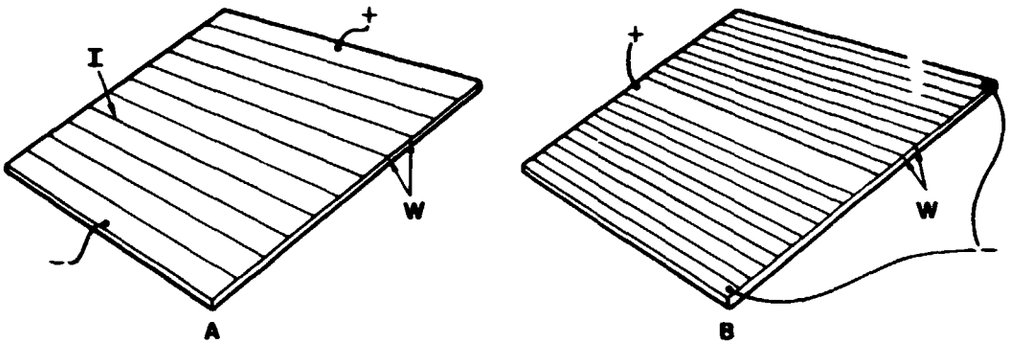
Fig. 1
## MODULE OPTIONS




**Single String**
**25 Series Connected Cells**
**1.0 cm Width**
**$V_{mp}$ = 13–15 Volts**

**Double String**
**25 Series Connected Cells**
**0.5 cm Width**
**2 Parallel Strings**
**$V_{mp}$ = 13–15 Volts**

Fig. 2
## MONOLITHIC MODULE CROSS SECTION

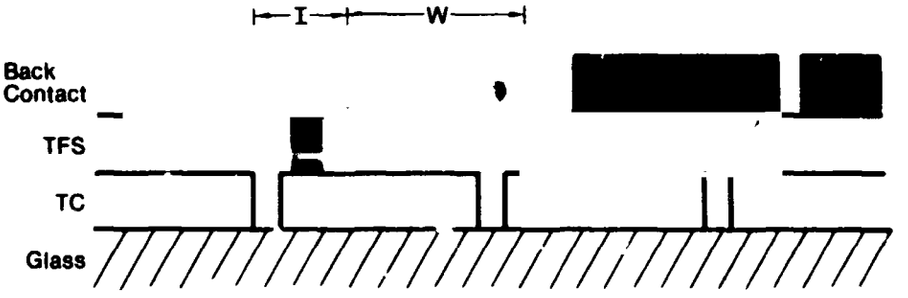


Fig. 13
## MODULE FILL FACTOR LOSS MAP

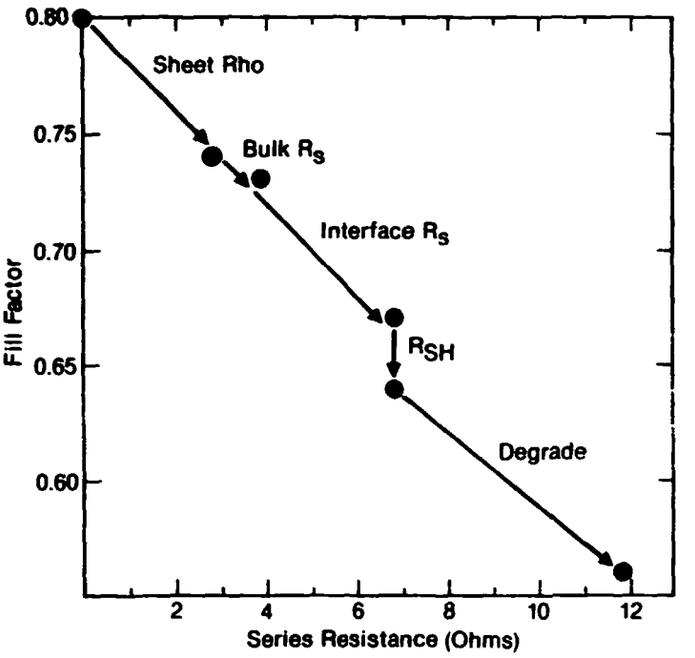



Fig. 14
## MODULE FILL FACTOR VS. FRONT ELECTRODE SHEET RHO

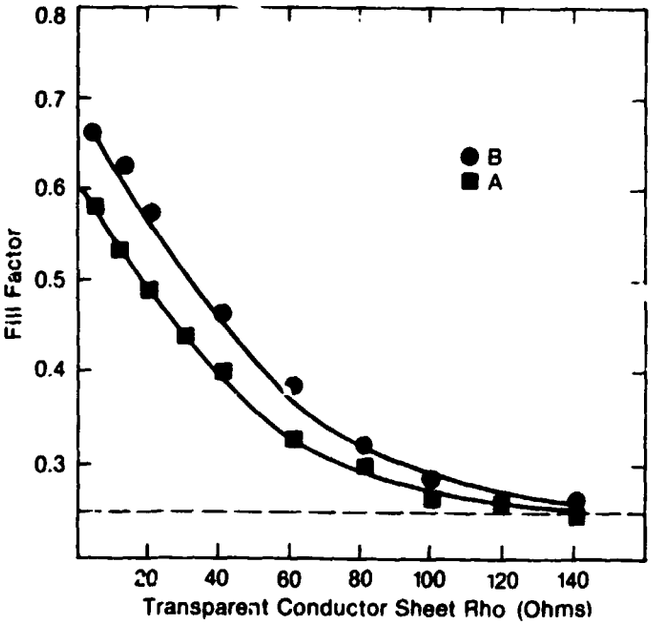


Fig. 3
## ROOFTOP MODULE EFFICIENCY

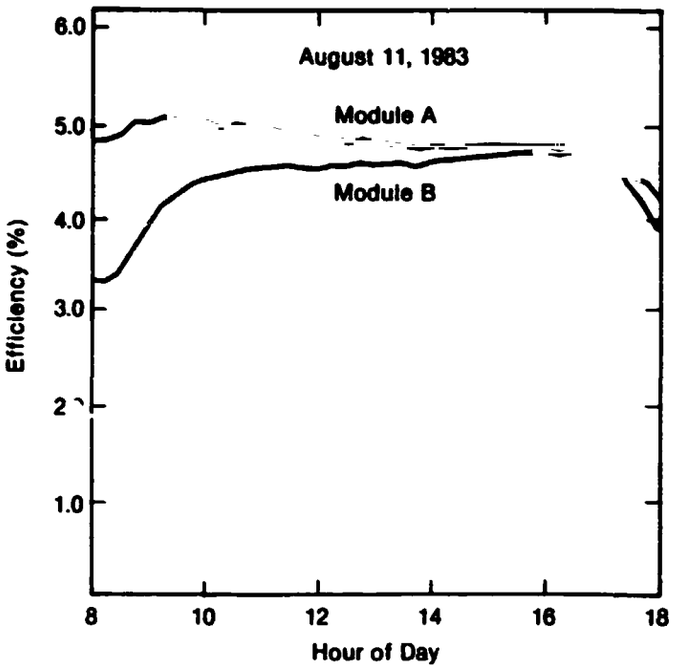



Fig. 4
## Si/Si AND Si/Ge PERFORMANCE vs TIME

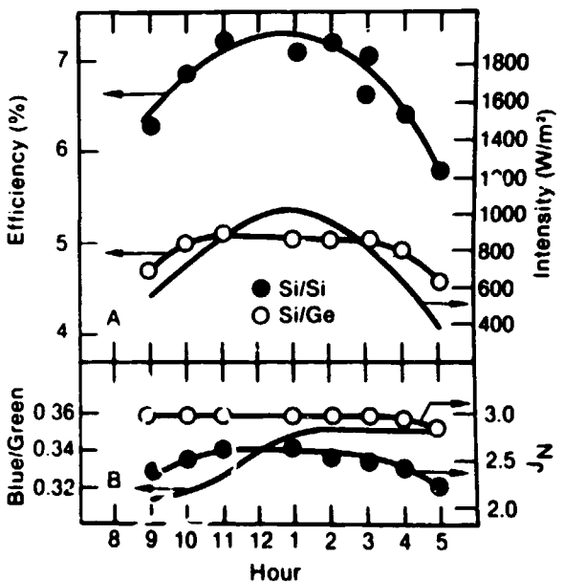


Fig. 5

## SLOPE AT $V_{OC}$ VS. FILL FACTOR FOR STANDARD CELL POPULATION IN B AND A STATES

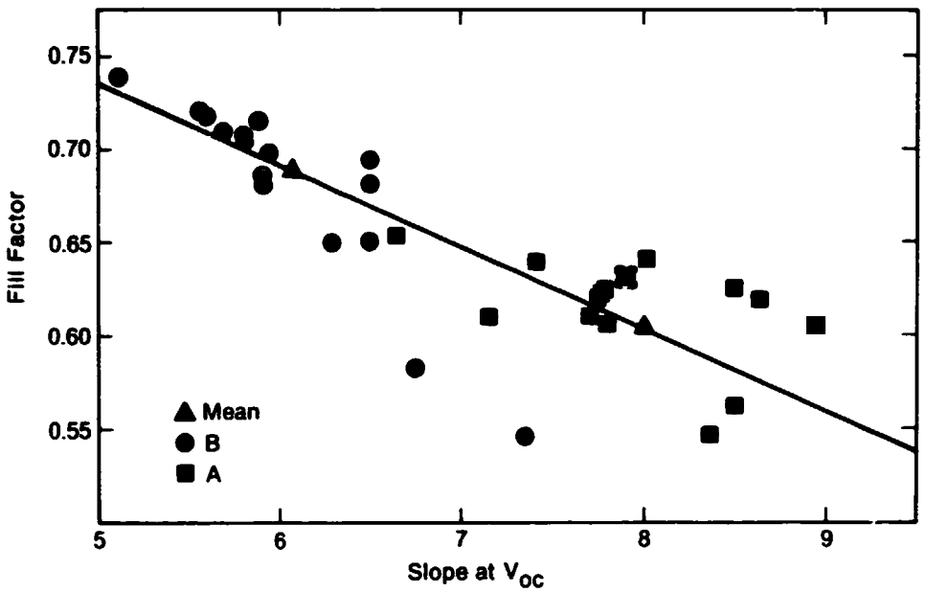



Fig. 6

## FILL FACTOR VS. CELL THICKNESS FOR B AND A STATES

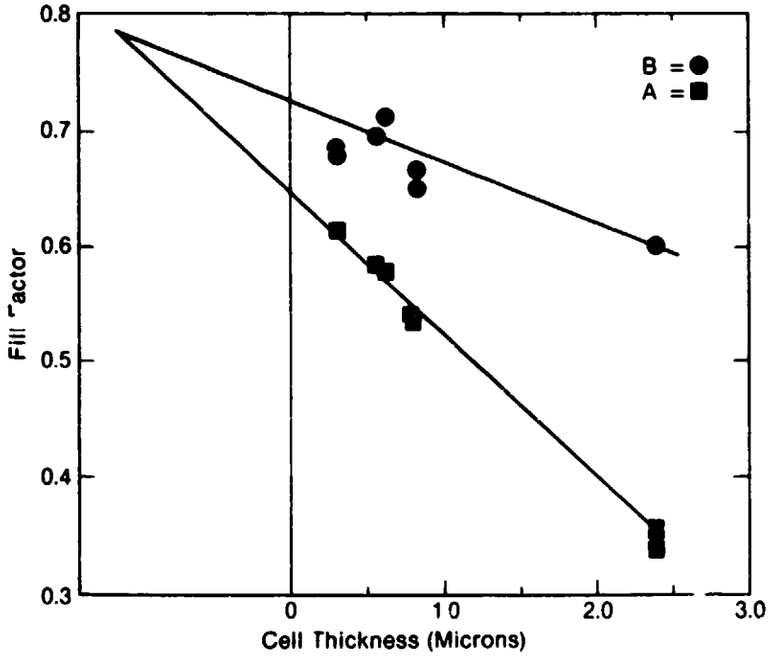


Fig. 7

## MODULE I-V CURVE: $R_{sh}$ INCLUDED

**TFS 431 (1 String/25 Segments) Conc. = 1 sun**
**Shorted Segments = 0**

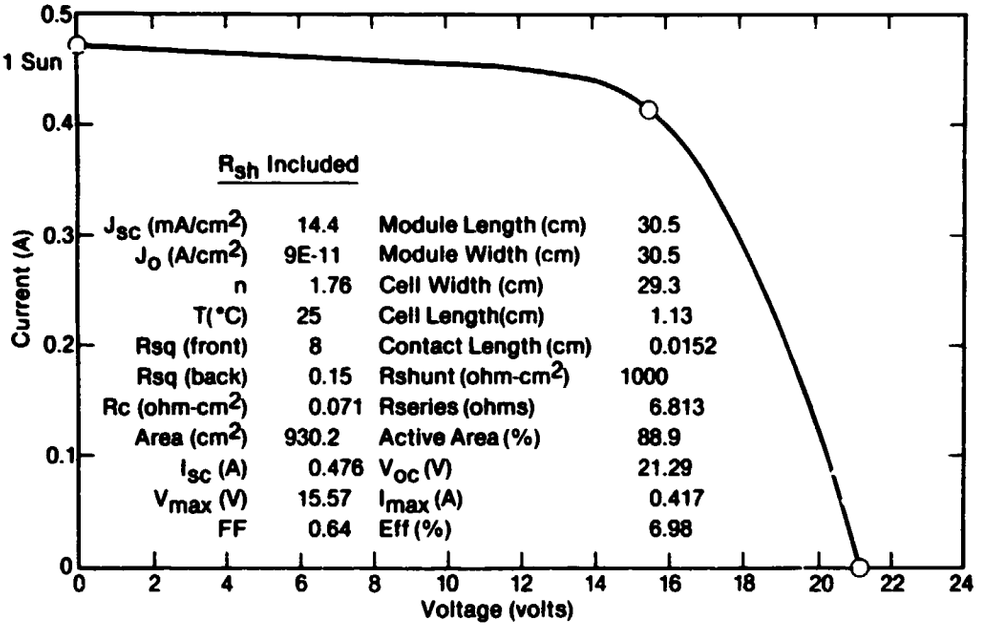



Fig. 8

## MODULE I-V CURVE: IDEAL

**TFS 431 (1 String/25 Segments) Conc. = 1 sun**
**Shorted Segments = 0**

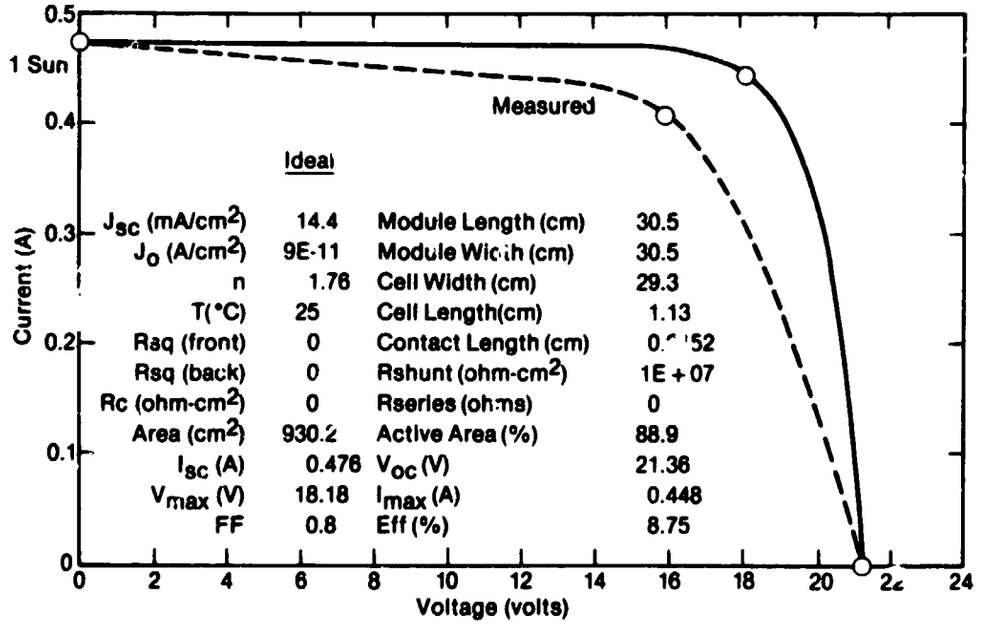


Fig. 9

## MODULE I-V CURVE: SHEET RHO INCLUDED

**TFS 431 (1 String/25 Segments) Conc. = 1 sun**
**Shorted Segments = 0**

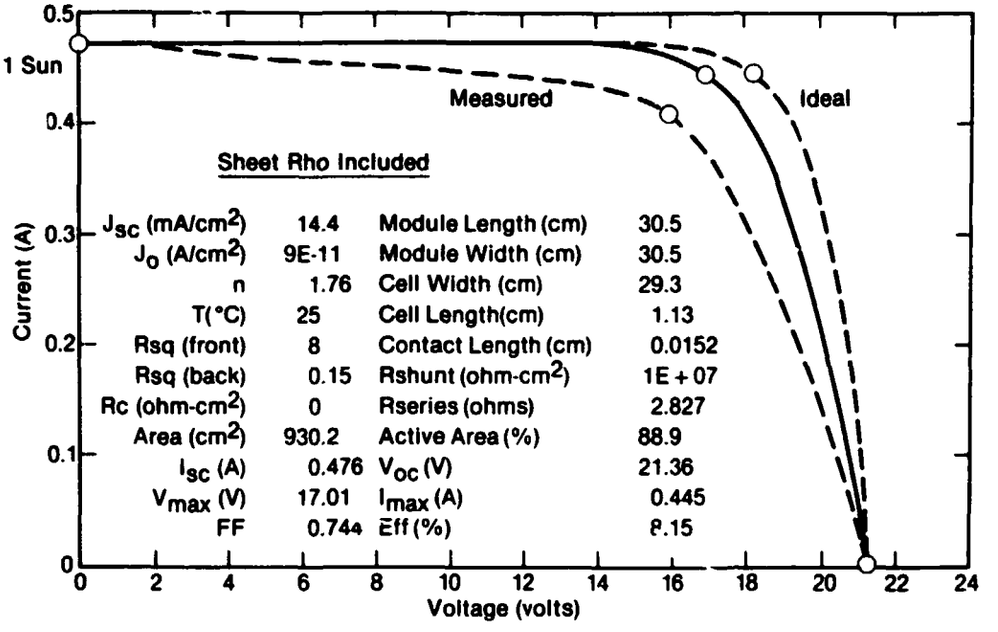



Fig. 10

## MODULE I-V CURVE: BULK $R_S$ INCLUDED

**TFS 431 (1 String/25 Segments) Conc. = 1 sun**
**Shorted Segments = 0**

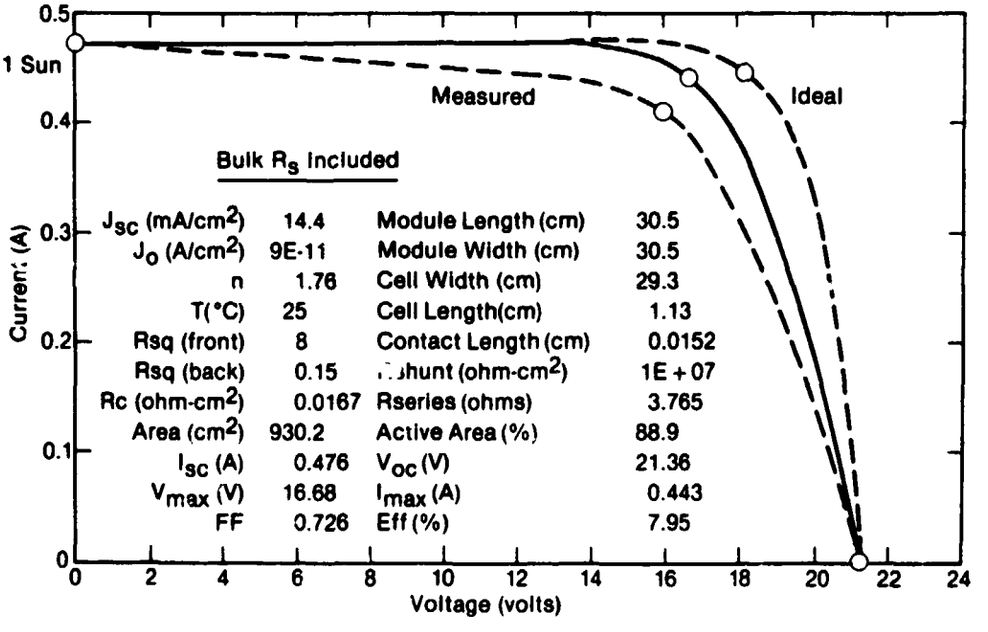


Fig. 11

## MODULE I-V CURVE: INTERFACE $R_S$ INCLUDED

**TFS 431 (1 String/25 Segments) Conc. = 1 sun**
**Shorted Segments = 0**

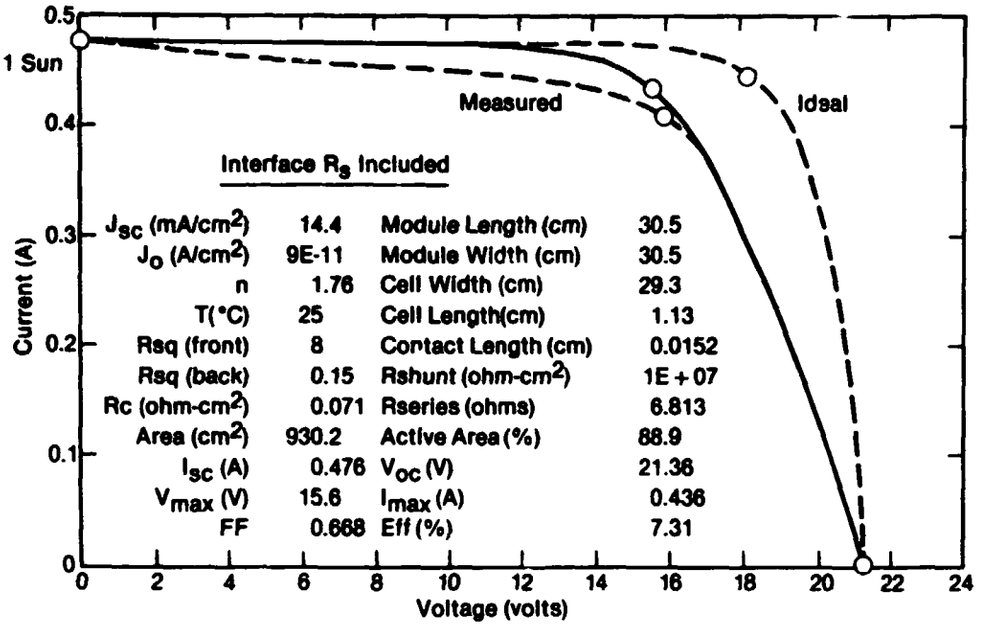



Fig. 12

## MODULE I-V CURVE: DEGRADATION INCLUDED

**TFS 431 (1 String/25 Segments) Conc. = 1 sun**
**Shorted Segments = 0**

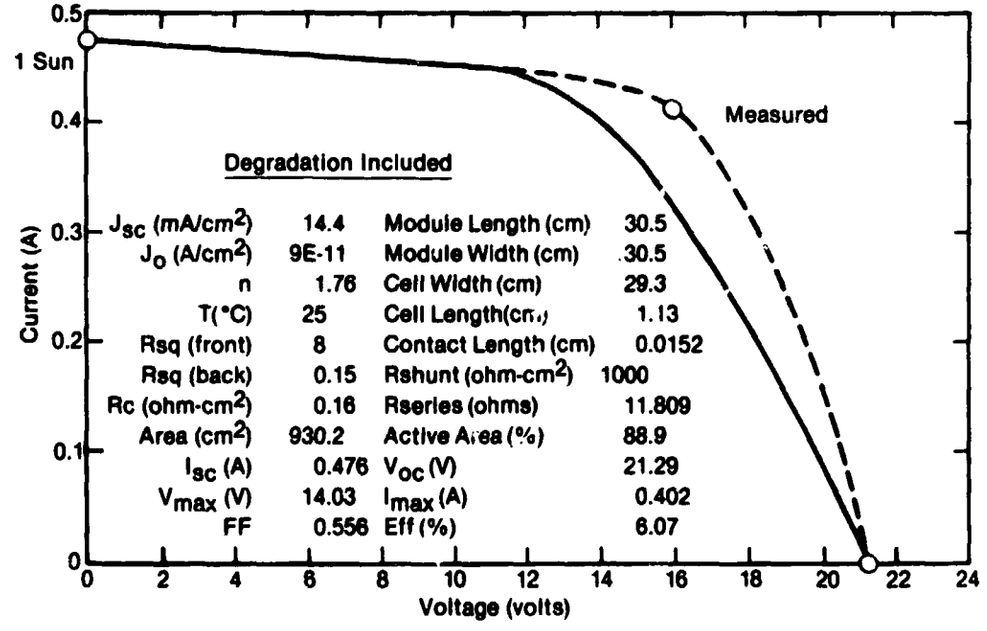


Fig. 15
## MODULE EFFICIENCY VS. CELLS PER FOOT FOR B AND A STATES

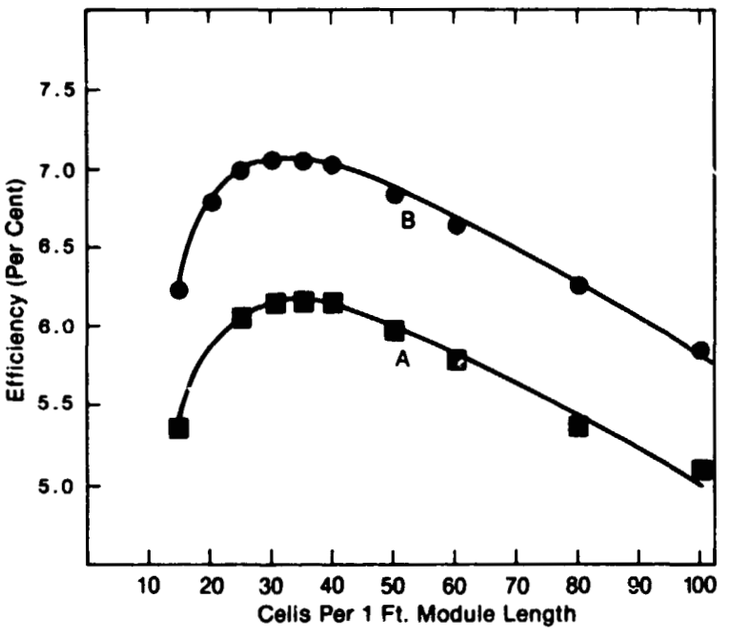



Fig. 16
## FILL FACTOR AND SHORT CIRCUIT CURRENT VS. CELLS PER FOOT FOR B AND A STATES

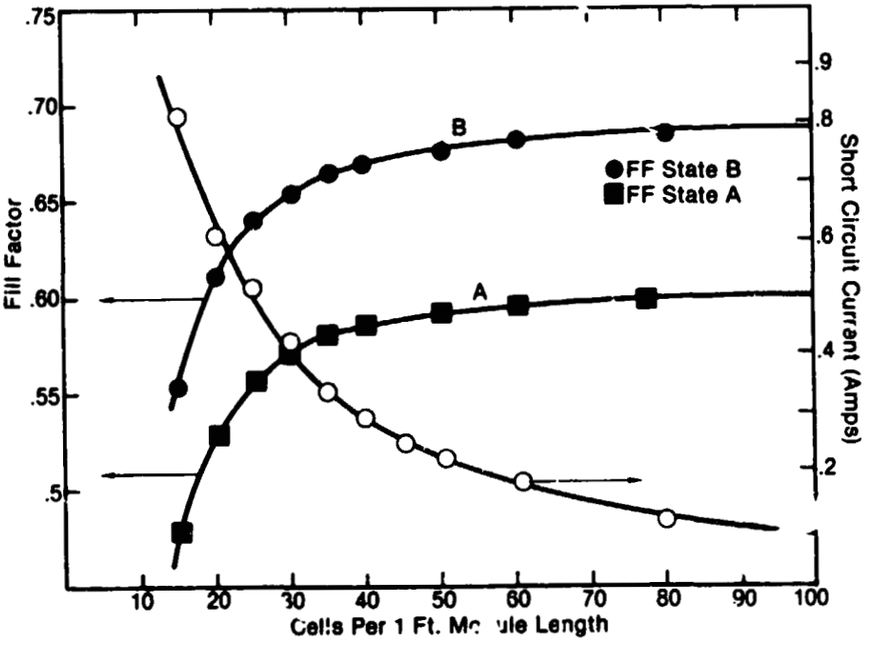
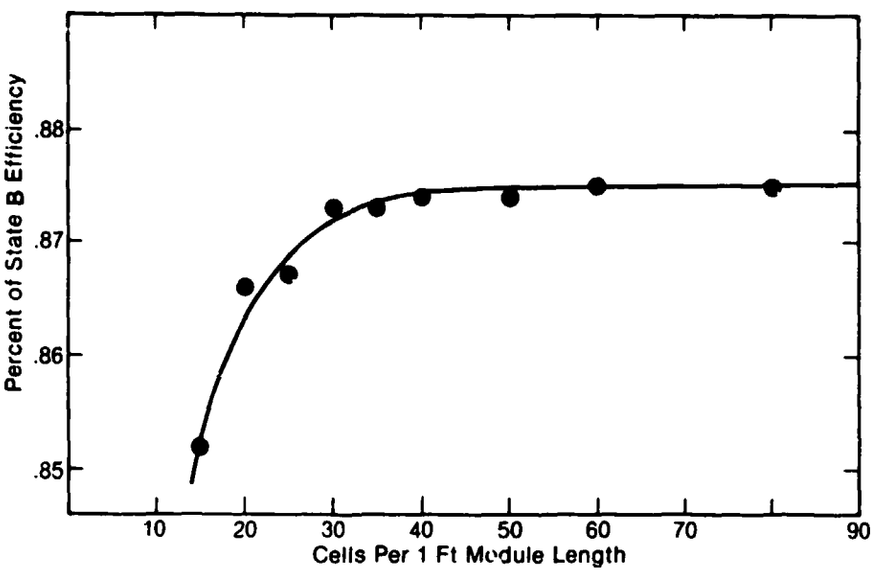


Fig. 17

## PER CENT OF STATE B MAINTAINED BY A VS. CELLS PER FOOT



DISCUSSION

WRONSKI: You raised several very important questions. One is the difference between a tandem cell and a single cell; I think that should be taken into account. I have one question, though. It is very nice to parameterize the cell performance instead in terms of the R-shunt, R-series and so on. There is one difference I think between amorphous-silicon and crystalline-silicon cells, that the recombination per se rather than the series resistance can give characteristics that could be interpreted in terms of those parameters. I think that this should be pointed out, because it becomes very important when people start doing degradation studies and are looking for contact resistance and short resistance. But what I want to ask you is, have you got any feeling as to how we can tell the difference between the two mechanisms?

MOREL: Again I apologize, because what I'll say tomorrow addresses these very points you are making -- such as why this looks like series resistance. I have looked at it a little bit, the underlying physics, and it turns out that you picked one of the models in the literature that is a recombination model. I can come up with some things that come close to fitting what I have, although there are some wrinkles that are different in it. But I think the way to tell now is that there is an interface component and a bulk component. I think if we do some activation energy studies of annealing and so forth, we might be able to see the differences, and separate the two, and understand which is doing what.

LESK: I think it would be valuable from a modeling standpoint to show how your shunt resistance varies as a function of intensity. At night you would draw 12 amps reverse bias. That's got to drop very rapidly as a function of intensity in the dark. The shunt resistance basically has got to disappear. The energy is what looks like a function of intensity for modeling at less than one sun.

MOREL: I calculated what the current contribution of that was. Certainly, for the standard performance of the module out in the sunlight, light is not a big problem. But for the kind of issue you are raising, I don't know what the exact number would be if you calculated it out. We'd have to look at it more carefully to see how long it could stay in the dark before there is a problem. I don't know, offhand.

D'AIELLO: The interface component interests me. It looks very large in the module that you have. Do you have any thoughts on its origin, related to the physical effects?

MOREL: Truthfully, all of this was done in the last couple of weeks, and I have not had time to push it further than where it is right now, other than to try to relate the bulk part of it to some of the lifetime models. The interface part of it -- all I can do is speculate, and think that it has something to do with the

p-transparent conductor interface, which seems to be a very sensitive thing. Also, one could point to the interface between the end and the back metal. There have been some comments made already that some oxidation can take place there. I would not expect that to be reversible, however, and so we need to go back and look at some activation energies of reversibility and so forth to understand which parts of this are reversible and which are not. Then maybe we will understand.

N86-12771

# OUTDOOR PERFORMANCE TESTING OF THIN-FILM DEVICES

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Golden, Colorado 80401

The Advanced Systems Research Group supports the PV AR&D project by providing outdoor (global) testing of PV cells, submodules, modules, and arrays. The group also provides in-house engineering and analysis to identify and determine how technical issues such as cell/module/system adaptations, long-term stability, reliability, economics, materials availability, safety, and environmental impacts affect the development and ultimate use of advanced PV thin film, innovative cell and material technologies.

A major thrust of the research effort is to develop and utilize instrumentation and procedures for monitoring and analyzing PV cells and submodules including outdoor performance and stability testing and life-cycle accelerated stress testing. Through testing and simulation, researchers can identify problems that require further laboratory research and can help to focus, as well as support, advanced PV systems research.

To accomplish the above, the SERI outdoor PV test facility was established in 1982. The facility is located directly west of SERI's field test laboratory building in Golden, Colorado. The group has designed testing systems and analysis procedures for, and has tested, numerous amorphous silicon thin film submodules provided by SERI subcontractors and has performed long-term outdoor stability tests on CdS/$CuInSe_2$ and hydrogen passivated silicon solar cells. A significant contribution from this facility over the past year was the testing of large-area amorphous silicon submodules which supported the achievement of major milestones in the DOE/SERI PV Program.

The outdoor testing operations are presently divided into four functional areas: (1) Outdoor Performance Testing; (2) Stability Performance Testing; (3) Accelerated Stress Testing, and (4) Systems Simulation Testing. The following provides an overview of outdoor performance and stability testing capabilities at SERI, selected test results and performance trends.

- Outdoor Performance Testing: This activity includes the measurement of PV cell and submodule I-V characteristics in an outdoor environment under sunlight. Figure 1 illustrates typical test and measurement data and information recorded during a test program. The mainstay of the testing system is an HP 3054A data system (Figure 2) controlled by an HP 9836 computer. A specially designed test bed (Figure 3), with temperature control capabilities, vacuum hold down provisions, motor controlled light shutter, and calibrated pyranometer, can accommodate cells and submodules ranging in sizes up to .61 meteres (2 ft) by 1.1 meters (3.5 ft). A unique testing capability has been incorporated into this system which makes it possible to simultaneously test and measure individual cell I-V characteristics of series connected cells on a submodule substrate.

Over 200 tests have been performed on various thin-film submodules in the last two years. Selected test results are provided in Table 1 illustrating the range in submodule sizes (active areas) tested and corresponding performance data obtained during outdoor tests. Test results taken from Table 1 (efficiency and fill factor) are plotted against time (Figure 4) and submodule active area (Figure 5) illustrating performance trends.

Stability Performance Testing: A variety of testing systems are being utilized for long-term performance and stability measurements of cells and submodules. These systems include a hermetically sealed test chamber purged with nitrogen for outdoor stability exposure tests of cells and is monitored by an HP 3054A data system controlled by an HP 85 computer. Two additional outdoor test beds, which can accommodate large submodules and modules ranging in sizes up to .61 meters (2 ft) by 1.1 meters (3.5 ft) have provisions for temperature and environmental control during testing and are controlled and monitored by an HP 3054A or Acurex Autodata Ten/10 data systems. Recent testing utilizing these systems included outdoor stability testing of CdS/$CuInSe_2$ and hydrogen passivated silicon solar cells. Selected stability performance test results are illustrated by Figures 6 and 7 for a CdS/$CuInSe_2$ solar cell and by Figure 8 for a hydrogen passivated silicon solar cell.

# Advanced PV Systems Research — Outdoor Testing

## Typical Test and Measurement Data and Information Recorded during a Testing Program

- Date of test
- Time of test
- Test specimen I.D. number
- Insolation before and after test
- Temperature
- Area
- $I_{sc}$ (short circuit current)
- $V_{oc}$ (open circuit voltage)
- $P_{max}$ (maximum power output)
- Current at $P_{max}$
- Voltage at $P_{max}$
- Current at $V_{oc}$
- Voltage at $I_{sc}$
- Efficiency
- Fill factor
- I-V curve and listing of data points
- Solar spectral response curve and listing of data points

Figure 1

## Amorphous Silicon Test — Data & Control System

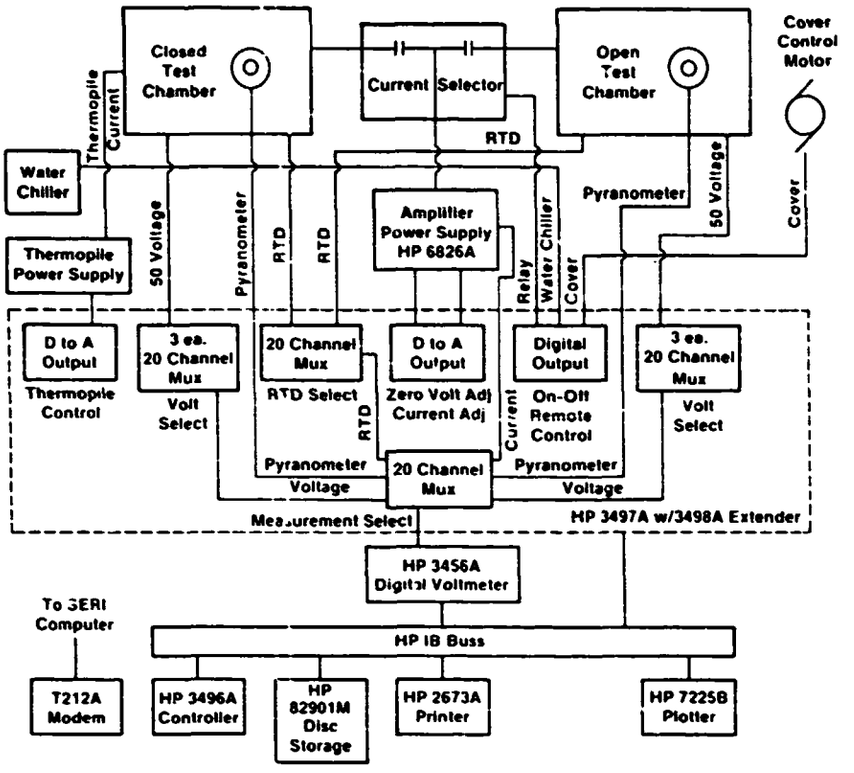
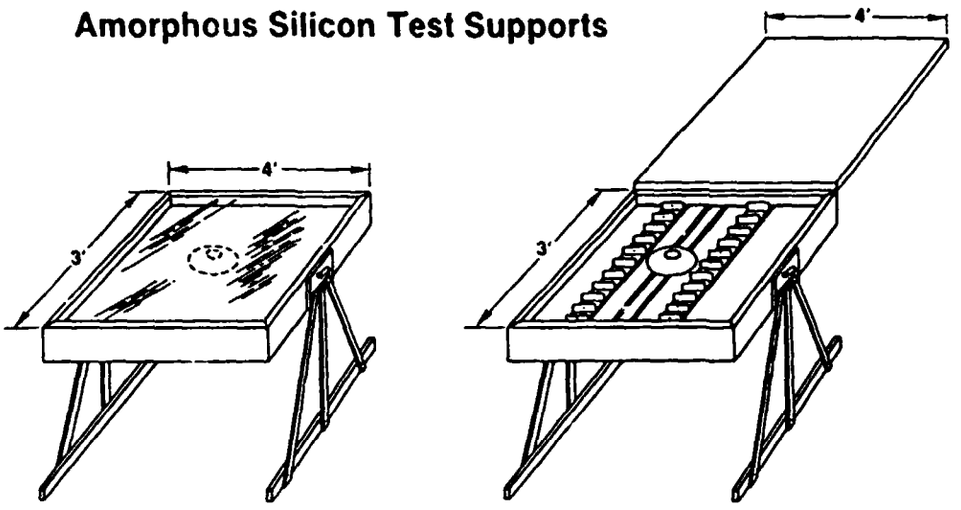



Figure 2

## Amorphous Silicon Test Supports




**Closed Chamber**
**Glass Cover**
**Dry $N_2$ Purge**
**Temperature Control 10° - 60° C**
**Pyranometer**
**RTD Temperature Measurements**
**Module Space**
**2 ea. 1' × 2-1/2'**
**or 1 ea. 2' × 3-1/2'**
**Contacts for 50 Cells**

**Open Chamber**
**Remote Control Lid and Light Shutter**
**Pyranometer**
**RTD Temperature Measurements**
**Module Space**
**2 ea. 1' × 2-1/2'**
**or 1 ea. 2' × 3-1/2'**
**Contacts for 50 Cells**

Figure 3

PV Thin-Film Submodule Outdoor Performance Test Results

| Sample Code No. | Material Type | Date Meas. | Time Meas. | Insolation $W/m^2$ | Cell Temp. $C^o$ | Isc (ma) | $V_{oc}$ (volts) | FF (%) | Eff. (%) | Active Area ($cm^2$) | Dimensions (cm) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| AS1 | Amorphous Si | 5/24/83 | P.M. | 957 | 39.0 | 70.9 | 15.3 | 51.2 | 4.6 | 126.9 | --- |
| AS2 | " | 5/24/83 | P.M. | 896 | 39.2 | 110.5 | 26.0 | 48.5 | 4.4 | 350.0 | --- |
| AS3 | " | 6/23/83 | P.M. | 1047 | 39.0 | 69.7 | 21.1 | 45.1 | 4.3 | 149.0 | --- |
| AS4 | " | 8/2/84 | A.M. | 923 | 36.3 | 66.1 | 15.1 | 58.1 | 6.1 | 102.4 | 21 x 10 |
| • AS5 | " | 9/28/84 | A.M. | 1205 | 35.8 | 319.9 | 23.7 | 54.5 | 5.0 | 693 | 30 x 30 |
| • AS6 | " | 9/28/84 | A.M. | 1049 | 36.1 | 314.9 | 23.1 | 57.0 | 5.5 | 722.4 | 30 x 30 |
| AS7 | " | 2/7/85 | A.M. | 1182 | 32.1 | 341.5 | 22.7 | 57.1 | 5.1 | 733 | 30 x 30 |
| AS8 | " | 2/8/85 | P.M. | 906 | 44.2 | 62.1 | 11.1 | 64.3 | 5.9 | 82.5 | 21 x 21 |

o Test Site Location: SERI Advanced PV Systems Outdoor Test Facility - Golden, Colorado

o Insolation Measurement Uncertainty: ±5% (Global)

• Encapsulated

Table 1

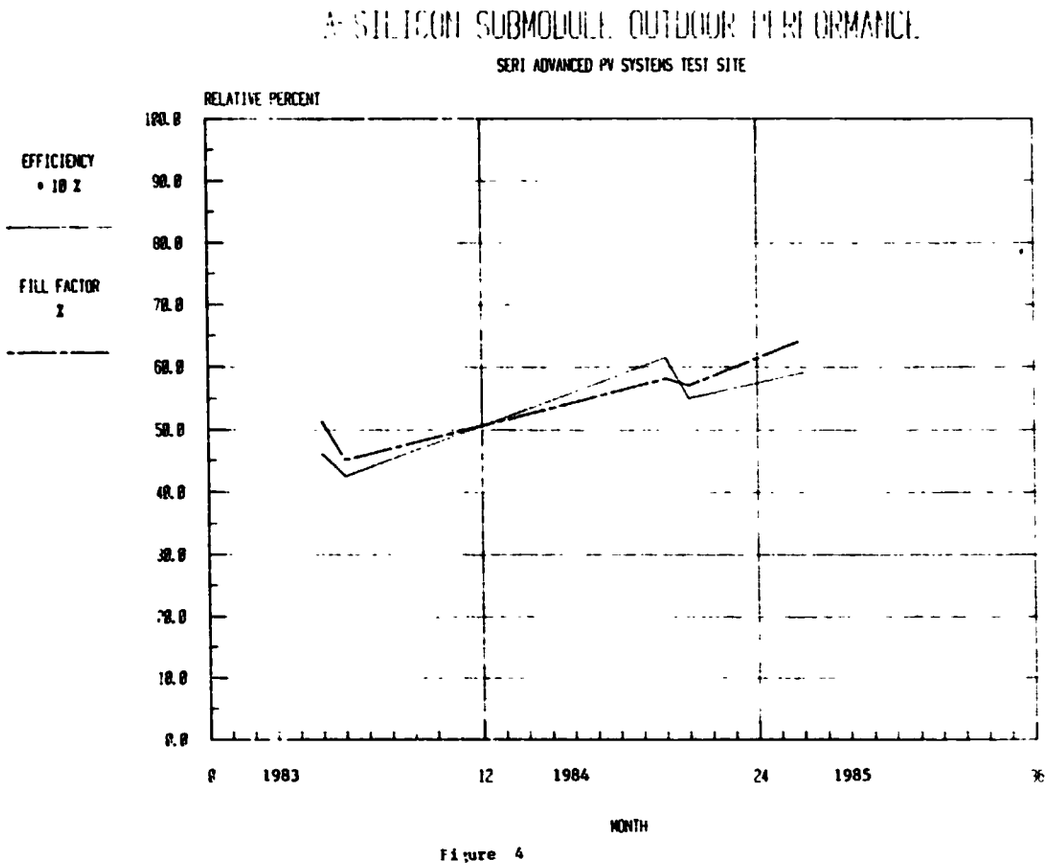



Figure 4

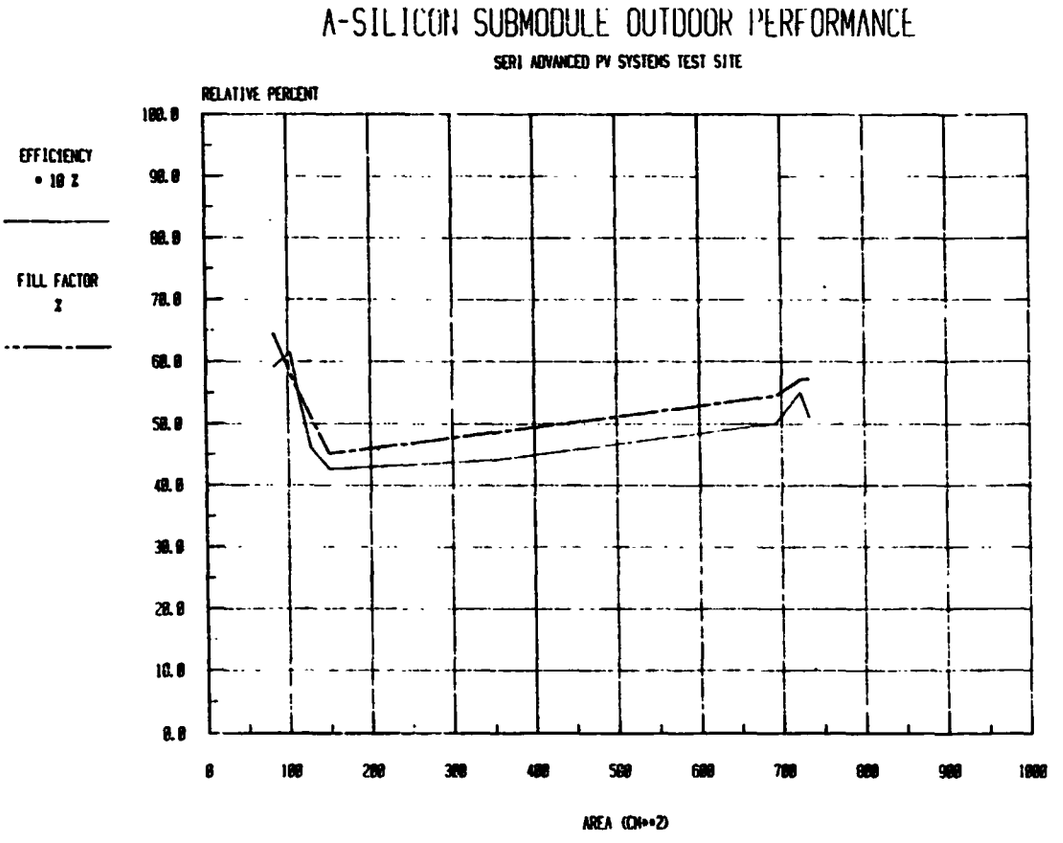

A-SILICON SUBMODULE OUTDOOR PERFORMANCE
SERI ADVANCED PV SYSTEMS TEST SITE
RELATIVE PERCENT
EFFICIENCY
• 10 Z
FILL FACTOR
Z
100.0
90.0
80.0
70.0
60.0
50.0
40.0
30.0
20.0
10.0
0.0
0
100
200
300
400
500
600
700
800
900
1000
AREA (CM**2)

Figure 5

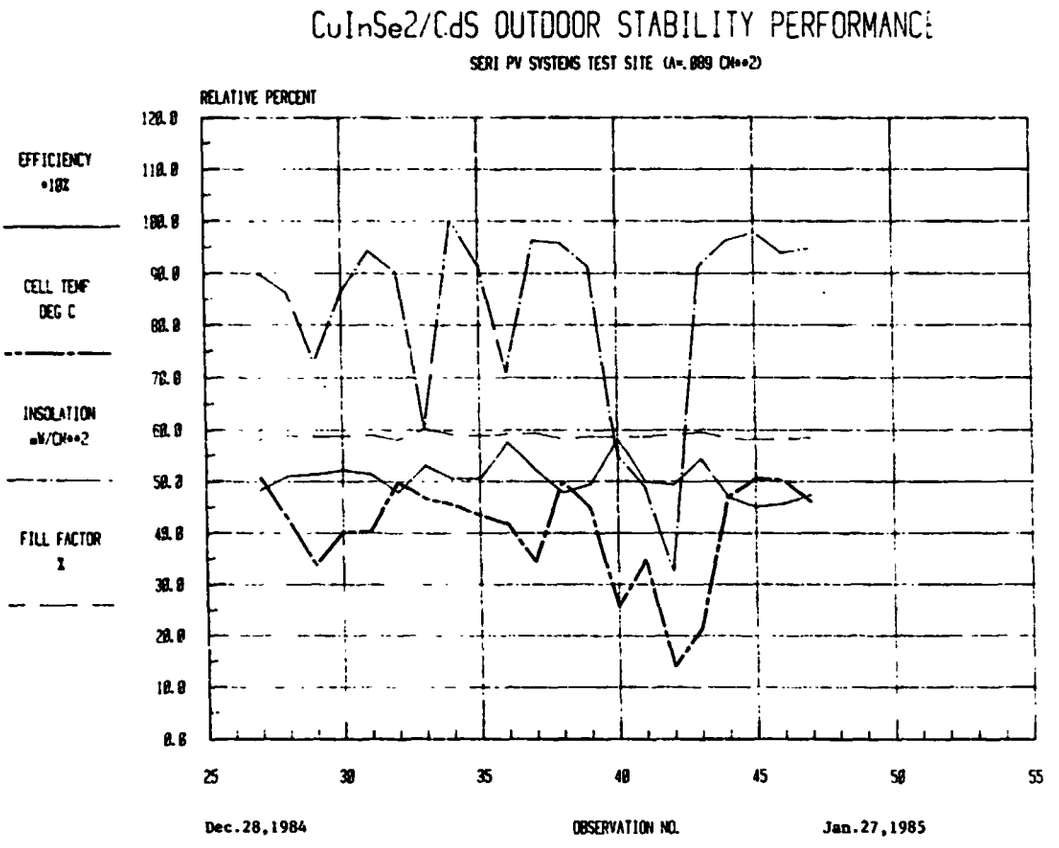

CuInSe2/CdS OUTDOOR STABILITY PERFORMANCE
SERI PV SYSTEMS TEST SITE (A=.009 CM**2)
RELATIVE PERCENT
EFFICIENCY *10%
CELL TEMP DEG C
INSOLATION mW/CM**2
FILL FACTOR %
120.0
110.0
100.0
90.0
80.0
70.0
60.0
50.0
40.0
30.0
20.0
10.0
0.0
25
30
35
40
45
50
55
Dec.28,1984
OBSERVATION NO.
Jan.27,1985

Figure 6

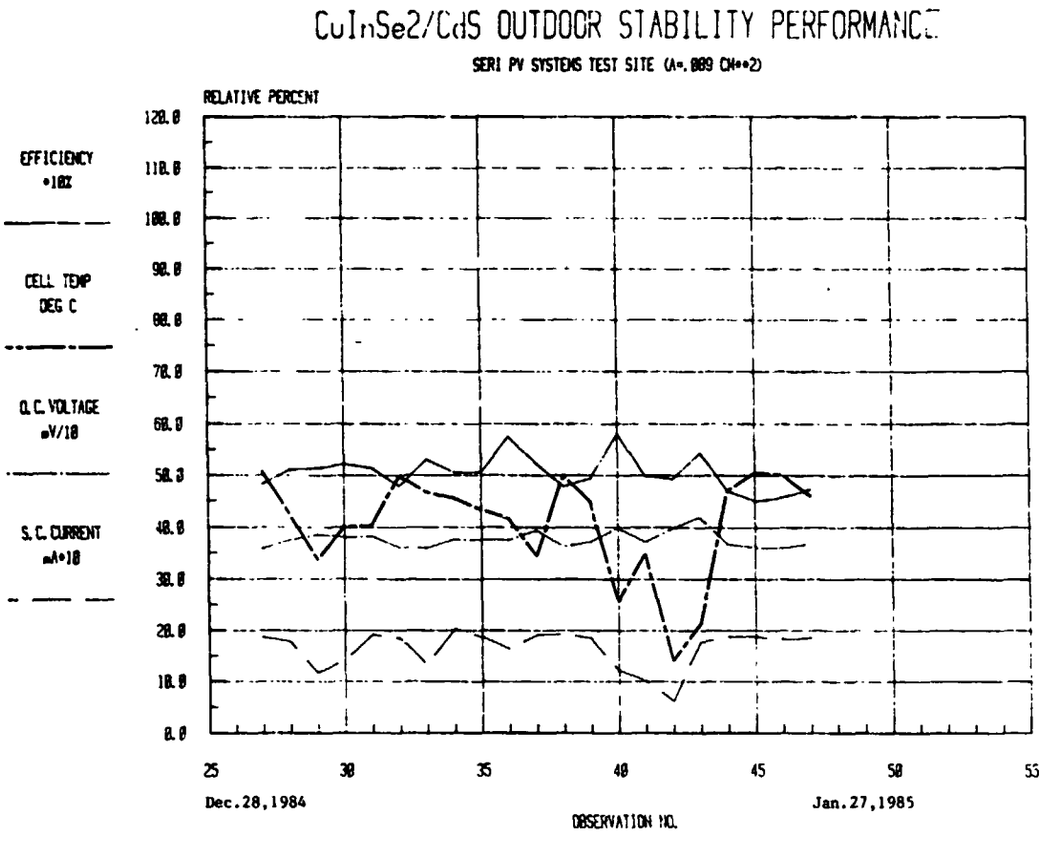

CuInSe2/CdS OUTDOOR STABILITY PERFORMANCE
SERI PV SYSTEMS TEST SITE (A=.089 CM**2)
RELATIVE PERCENT
EFFICIENCY
*10%
CELL TEMP
DEG C
O.C. VOLTAGE
mV/10
S.C. CURRENT
mA*10
120.0
110.0
100.0
90.0
80.0
70.0
60.0
50.0
40.0
30.0
20.0
10.0
0.0
25
30
35
40
45
50
55
Dec.28,1984
Jan.27,1985
OBSERVATION NO.

Figure 7

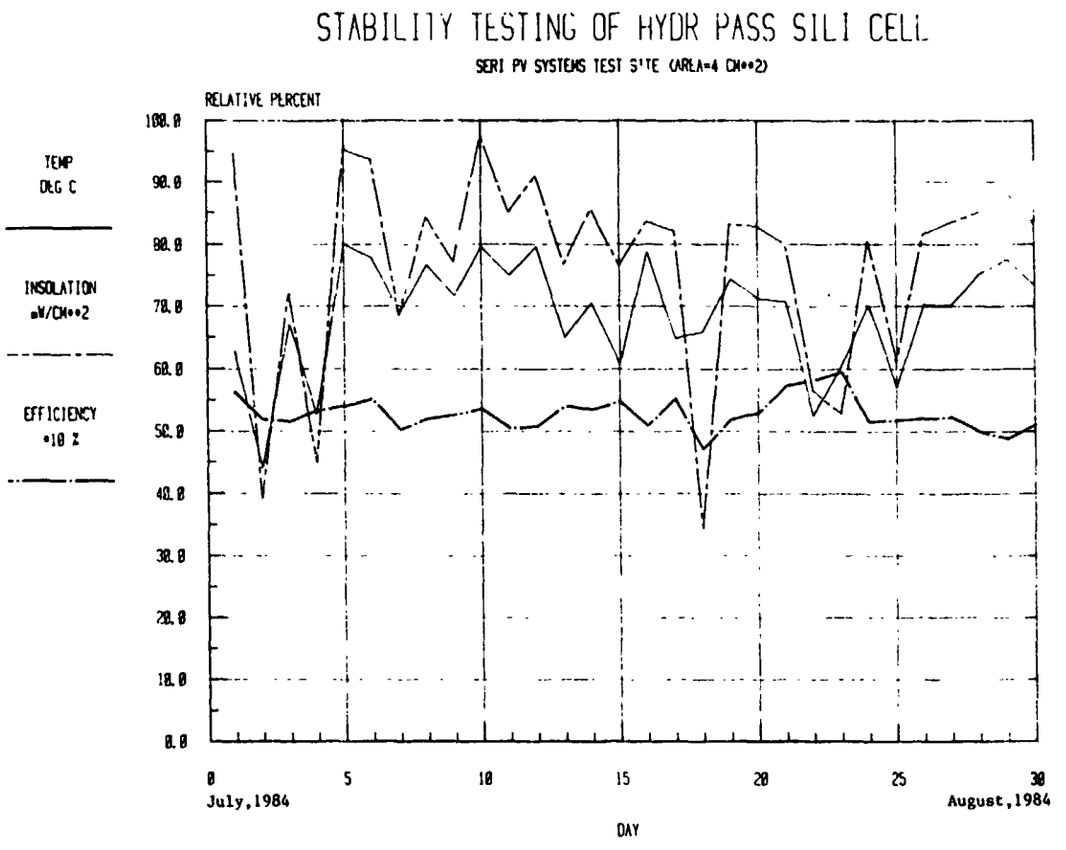

STABILITY TESTING OF HYDR PASS SILI CELL
SERI PV SYSTEMS TEST SITE (AREA=4 CM**2)
RELATIVE PERCENT
TEMP
DEG C
INSOLATION
mW/CM**2
EFFICIENCY
*10 %
100.0
90.0
80.0
70.0
60.0
50.0
40.0
30.0
20.0
10.0
0.0
0
5
10
15
20
25
30
July,1984
August,1984
DAY

Figure 8

## DISCUSSION

**LESK:** I have seen some very high insolation values. You had one at 1200 $W/m^2$ with reflection from clouds adding on to a clear beam. Was that a special circumstance for that one, or will something else give it that high a value?

**DE BLASIO:** That is typical at our test facility on a clear summer day. There we average 1100, 1150, 1200, even up to 1240. Hard to believe, but it's true.

# MODULE VOLTAGE ISOLATION AND CORROSION RESEARCH

Gordon R. Mon
Jet Propulsion Laboratory

This paper presents a summary of recent research at JPL on two topics related to achieving long-term reliability of photovoltaic modules: voltage isolation and electrochemical corrosion. Special emphasis is given to similarities and differences in performance between crystalline-silicon modules and amorphous-silicon modules.

## VOLTAGE ISOLATION

The problem of voltage isolation is to confine the generated energy to the module circuitry. Energy may dissipate from the module slowly in the form of low-level leakage current, or rapidly as in insulation breakdown (Figure 1). If leakage-current levels in a photovoltaic array are excessive, proper operation of ground-fault detection equipment may be disrupted. A conventional solution to this problem is to use very-high-resistivity polymer insulations as module encapsulants.

The rapid dissipation of energy known as module breakdown, or more generally as voltage breakdown, can have several causes (Figure 2). It has been observed that, for a fixed applied voltage stress, the breakdown probability of polymer substrate films such as Tedlar and Mylar increases with increasing environmental exposure. Thus, regions within the insulation--here referred to as flaws--become more susceptible in time to puncture by applied voltage stresses. Voids in insulation are thought to be one type of flaw: gaseous microbubbles in the insulation that may be "manufactured in" or that may have evolved from defects at the molecular level. Normal cell-frame electrode stresses may discharge these voids, causing internal erosion. These measurable internal discharges provide information on insulation breakdown tendencies.

These insulation flaws may be further stressed by stress concentration centers on electrified parts, such as sharp points on solar cells. It is expected that in amorphous-silicon modules, sharp points with sub-micrometer radii, resulting from laser-scribing operations, may result in voltage breakdown of the amorphous silicon.

The performance of edge seals and gaskets must not be overlooked in considering the problem of voltage breakdown. In crystalline-silicon modules, such devices share the voltage stress load with the encapsulation, but in amorphous-silicon modules, the devices may bear all of the applied voltage stress.

A list of practical design techniques to reduce the likelihood of module voltage breakdown is presented in Figure 3: Use relatively few layers of

relatively thick, high-resistivity, flaw-free insulating films; use rounded, burr-free, and adequately spaced cell-frame electrodes; and use low-conductivity gaskets and edge seals (Reference 1).

## ELECTROCHEMICAL CORROSION

The fundamental principles of photovoltaic module electrochemical corrosion can be understood with the aid of Figure 4. Leakage current is composed of charge carriers that move under the influence of voltage and concentration gradients through the insulation, reacting with it and with the cell-frame electrodes to produce corrosion products. Leakage current levels are determined in part by the electrical conductivity of the insulation, which varies with changing environmental conditions of temperature, and the relative humidity to which the module is exposed, as indicated for two popular photovoltaic insulations in Figure 5. Note that for the same conditions of temperature and humidity, the conductivity of polyvinyl butyral (PVB) is about three orders of magnitude larger than that of ethylene vinyl acetate (EVA). This will explain in part the higher equilibrium leakage current levels observed in amorphous-silicon modules encapsulated in PVB (Figure 6).

Leakage current integrated over time yields charge transferred between the cell-frame electrodes. The quantity of charge transferred is an important measure of the degree of electrochemical corrosion. The cell maximum power output is an important measure of device performance. As environmental exposure continues, the cell power output decreases (Figure 7), as the quantity of charge transferred increases. Quantifying this relationship between total charge transferred and reduction of maximum cell power output for crystalline-silicon modules (Figure 8) and amorphous-silicon modules (Figure 9) reveals similar aging characteristics: 1 to 10 C/cm of charge transferred between cell and frame are required to produce a significant level, say 50%, of cell failures. This observation of a quantitative electrochemical failure threshold enables the prediction of module field life (Reference 2).

Assuming that equal quantities of charge transferred in laboratory and field environments produce equivalent electrochemical damage enables the determination of equivalent laboratory and field exposure times. This equivalence may form the basis of a qualification test for photovoltaic modules (Reference 3).

The important fundamentals of photovoltaics module electrochemical corrosion are summarized in Figure 10.

## PHYSICAL OBSERVATIONS

Typical corrosion observed in crystalline-silicon modules is depicted in Figures 11 through 13. Typical corrosion in positive polarity is characterized by missing cell metallization and the formation of cathodic dendrites; the dissolved metallization ions have migrated to the frame, where they deposit as dendritic crystallites. Typical corrosion in negative polarity exhibits less obvious characteristics to the naked eye, but microscopic examination reveals the formation of anodic corrosion salts and

the evolution of gas bubbles at the metallization-silicon interface, resulting in metallization delamination. Although the corrosion mechanisms in the two polarities differ, the corrosion rates are comparable.

At this stage in amorphous-silicon module research, nothing observed can be said to be typical. This notwithstanding, results of one set of corrosion tests on amorphous-silicon modules are presented here.

Two amorphous-silicon configurations tested are shown in Figure 14. The parallel modules consist of 16 separate amorphous-silicon cells, all of which share a common electrode--the $SnO_2$ layer deposited on the underside of the glass superstrate. The series modules consist of eight amorphous-silicon cells interconnected in a series-circuit configuration. The individual module units are encapsulated, together with aluminum bars serving as frames, in either PVB or EVA and are then exposed for more than 300 hours in an environmental chamber held at 85°C and 85% RH, with 500 volts applied between cell and frame. Front and rear views of the actual parallel modules are shown in Figures 15 and 16; front and back views of the actual series modules are shown in Figures 17 and 18. Note that wire attachments to individual cells in Figures 16 and 18 were accomplished with the use of Cho-bond silver epoxy. Note also that the series modules in Figure 18 arrived from the manufacturer with a layer of protective black paint on their rear surfaces; this paint layer was removed from all modules save No. 3 before testing. This negative-polarity series module encapsulated in EVA underwent a chemical reaction at the paint-metallization interface: the metallization extending beyond the paint edge began to disappear after 40 hours of exposure (Figure 19), and had completely disappeared after 130 hours (Figure 20).

Figures 21 through 23 show a front-face view of progressive corrosion of series module No. 6 (negative polarity, PVB) at 40, 130, and 300 hours, respectively. Note the progressive pinhole-like loss of metallization and amorphous silicon. Note also the squiggly, worm-like configurations generated by the loss of metallization. Figures 24 through 26 show front views of progressive corrosion of the same module. Clearly, some type of ion is moving from the frame toward the center of the module, perhaps an impurity in the PVD.

Figure 27 depicts series module No. 7 at 300 hours of exposure. Note the extensive loss of metallization and the worm-like patterns. Also note the voltage breakdown pit at the cell-frame interface, a result of internal discharge pulse counting at 5 kV. Figures 28 and 29 show a close-up of this region at 130 and 300 hours, respectively. The series modules exhibited a greater propensity for voltage breakdown than did the parallel modules, due no doubt to differences in materials and fabrication processes.

Corrosion of parallel modules, with one exception, was considerably less severe. Parallel module No. 688F (positive polarity, EVA) exhibited an unidentified discoloration of the rear metallization (Figure 30) after 300 hours. Parallel module No. A690E (negative polarity, PVB) exhibited some interesting effects. Figures 31 and 32 present a front view at 130 and 300 hours, respectively. Note again the worm-like metallization loss patterns and their growth with time of exposure. Figures 33 and 34 show the corresponding rear views. Figures 35 and 36 show close-ups of one cell at 40 and 300 hours, respectively. Note, in addition to the worm-like patterns, the pinhole-like losses of both metallization and silicon.

These observed degradations have yet to be subjected to surface analysis techniques such as EDX, SIMS, etc., so much remains to be learned about amorphous-silicon module corrosion at the mechanism level. Additional testing is required to categorize the long-term corrosion behavior of amorphous-silicon modules with non-metallic frames.

It should be emphasized that, although amorphous-silicon module corrosion appears to involve extensive loss of silicon material, the quantitative data of Figures 8 and 9 indicate that corrosion rates are comparable.

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2. Mon, G., Orehotsky, J., Ross, R., and Whitla, G., "Predicting Electrochemical Breakdown in Terrestrial Photovoltaic Modules," Proceedings of the 17th IEEE Photovoltaic Specialists Conference, pp. 682-692, Institute of Electrical and Electronics Engineers, Inc., New York, 1984.

3. Mon, G., Whitla, G., Neff, M., and Ross, R., "The Role of Electrical Insulation in Electrochemical Degradation of Terrestrial Photovoltaic Modules," IEEE Transactions on Electrical Insulation, Institute of Electrical and Electronics Engineers, Inc., New York, June 1985 (in press).

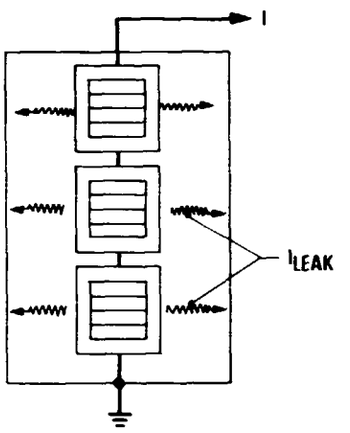
# LABORATORY EXPERIENCE WITH VOLTAGE BREAKDOWN

JET PROPULSION LABCRATORY

G.R. Mon

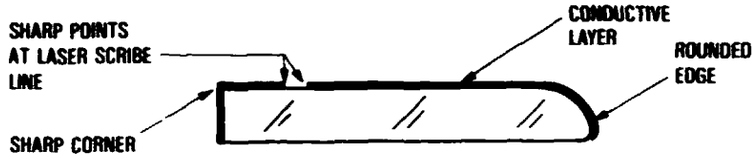
## Figure 1. Voltage Isolation Overview

- **Two problems associated with photovoltaic module insulations:**
  - **Applied voltage may stress the insulation to breakdown**
  - **Excessive leakage current levels may wreak havoc with proper operation of ground-fault detection equipment and may contribute to catastrophic breakdown of the insulation**
- **High-resistivity encapsulations assure low leakage-current levels**
  - **Encapsulation resistivity generally decreases as temperature and moisture content increase**
  - **Encapsulation resistivity decreases with time of exposure**



## Figure 2. Topics in Voltage Isolation Research

- **Voltage stress vs breakdown probability of pristine and environmentally exposed substrate (polymer) films**
- **Stress enhancement factors for geometrically sharp electrodes (such as solar cells)**

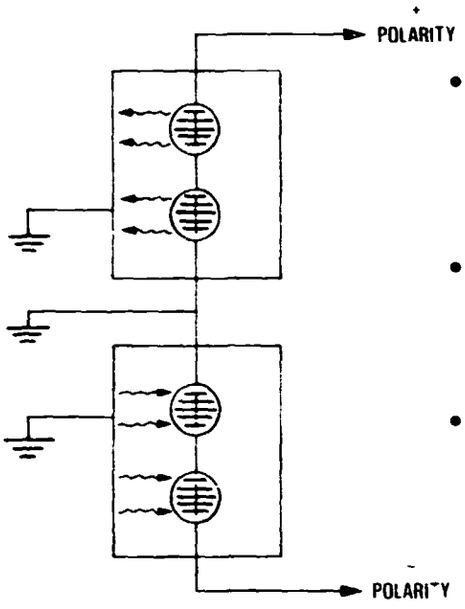



- **Internal discharge characterization of photovoltaic modules**
- **Performance of edge seals, gaskets, etc.**

## Figure 3. Voltage Isolation Research Results and Effective Design Practices

- **At a fixed voltage, the breakdown probability of polymer films increases with environmental exposure**
  - **Use high resistivity, pinhole-free insulating films**
  - **Use multiple layers of insulating films to reduce the probability of breakdown**
  - **Economics dictates the use of fewer layers of thick films rather than many layers of thin films**
- **Design for low module breakdown probability**
  - **Use rounded, burr-free cell and frame electrodes**
  - **Maintain adequate clearance between cell-frame electrodes**
  - **Use low-conductivity gaskets and edge seals**

## Figure 4. Relationship Between Leakage Current and Electrochemical Damage




- Cell string and frame behave as opposite polarity electrodes; the intervening pottant behaves as a solid state electrolyte
- Module leakage current increases with increasing temperature and relative humidity
- Observed and electrically measured electrochemical damage increases with increasing accumulated charge transfer

## Figure 5. Electrical Conductivity of PVB and EVA

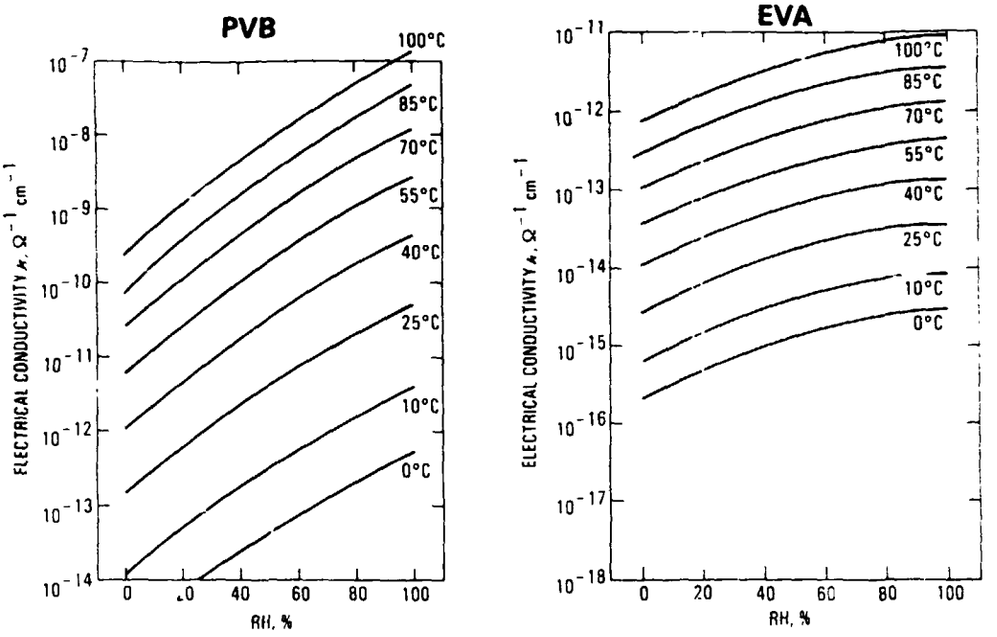


Figure 6. Amorphous Modules: Leakage Current vs Time of Exposure at 85°C/85% RH/500 Volts

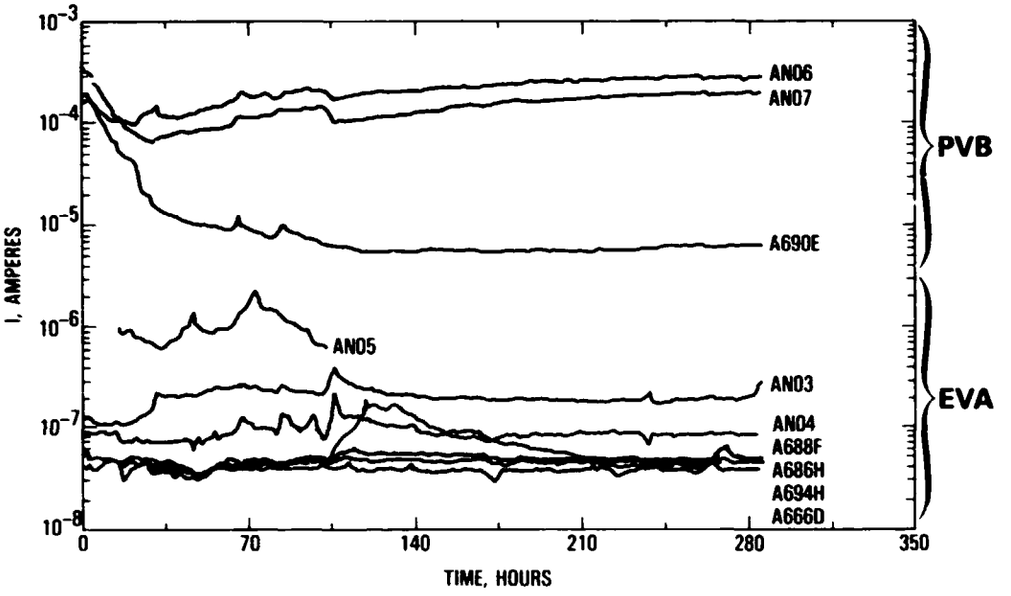



Figure 7. I-V Curves for Cell No. 6, Parallel Module A690E: 85°C/85% RH/500 Volts

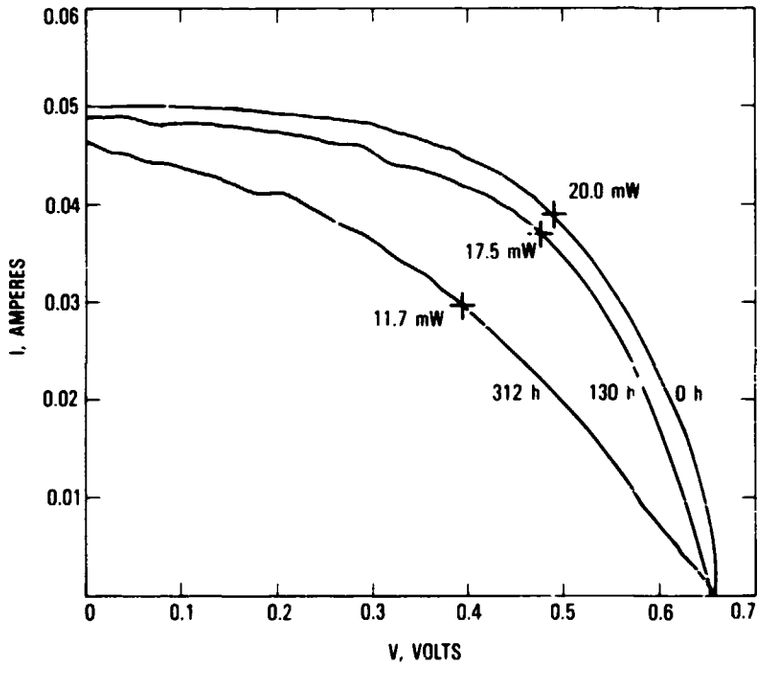


Figure 8. Power Output Reduction vs Accumulated Unit Charge Transfer

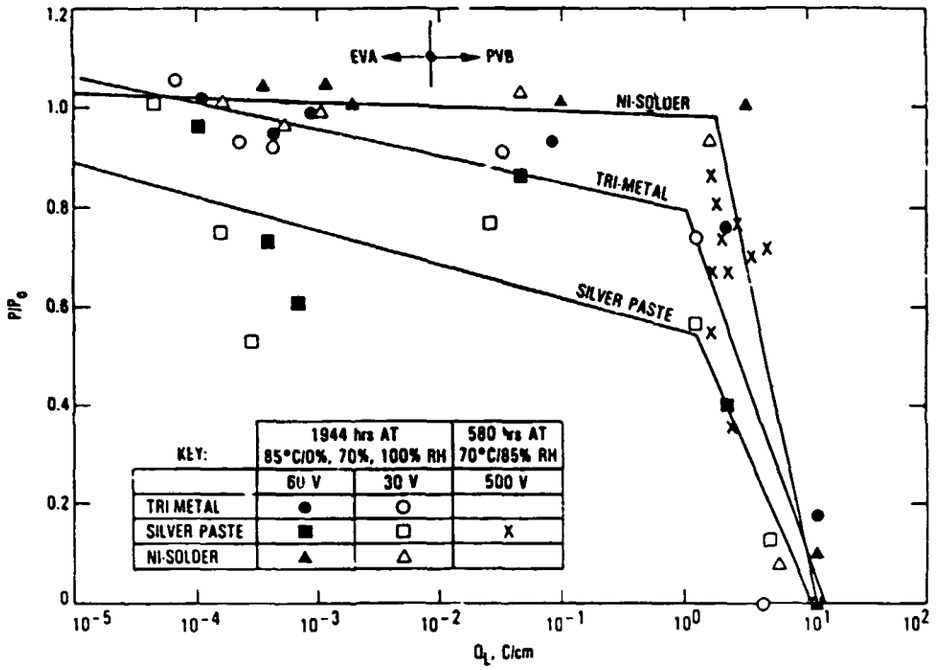



Figure 9. Amorphous Modules: Maximum Cell Power Output vs Charge Transfer per Unit Cell-Frame Length

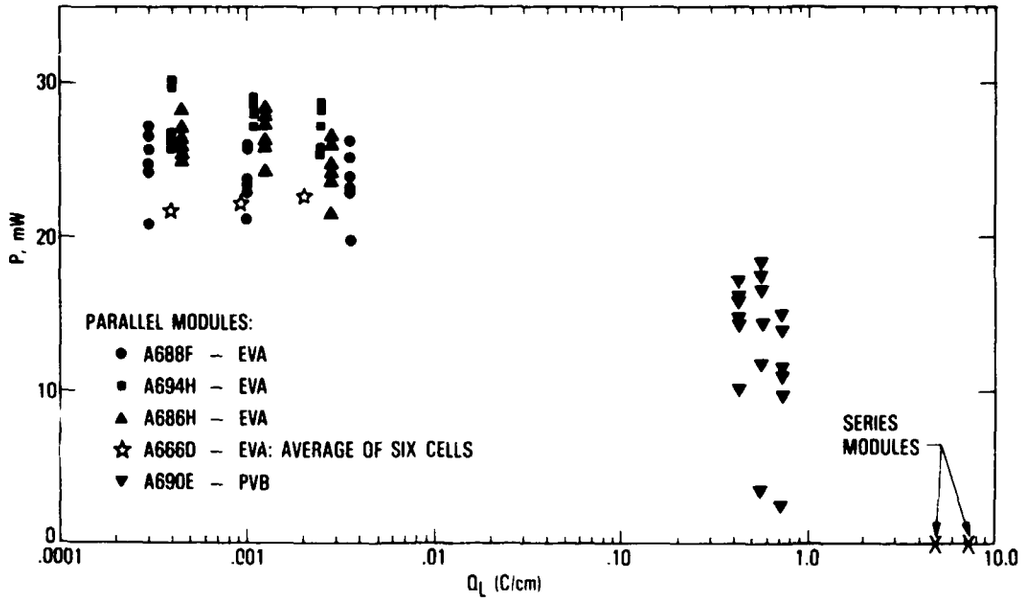


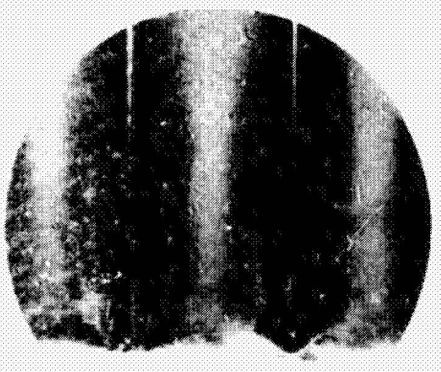
Figure 10. Electrochemical Corrosion Overview

- Total charge transferred between cell and frame is an important measure of the degree of corrosion
  - Leakage current is a manifestation of the movement between cell and frame of mobile ions in response to voltage and concentration gradients
  - Ions interact with the encapsulant and the cell-frame electrodes to produce corrosion products
  - Assuming that equal quantities of charge transferred in lab and field environments produce equivalent electrochemical damage enables the determination of equivalent lab/field exposure times
- Maximum cell power output is an important measure of cell performance
  - Cell power output degrades as corrosion progresses
  - Quantifying the relationship between cell power output reduction and total charge transferred enables module field-life prediction

Figure 11. PV Cell Electrochemical Degradation in Two Polarities: 500 V, 580 h at 70°C/85% RH

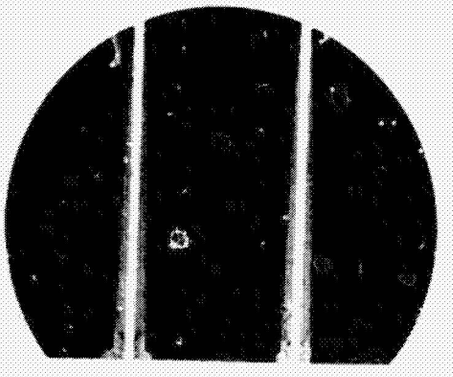
Figure 12. PV Cell Electrochemical Degradation in Two Polarities: 500 V, 580 h at 70°C/85% RH (Cont'd)

QXIP500



Cell + showing metallization dissolution and migration

QXIN500



Cell − showing metallization delamination

Figure 13. PV Cell Electrochemical Degradation in Two Polarities: 500 V, 580 h at 70°C/85% RH (Cont'd)

QXIP500

Frame – showing dendrite formation

QXIN500

Frame + showing white "fuzzball" corrosion salts

Figure 14. Amorphous Modules: Series and Parallel Configurations

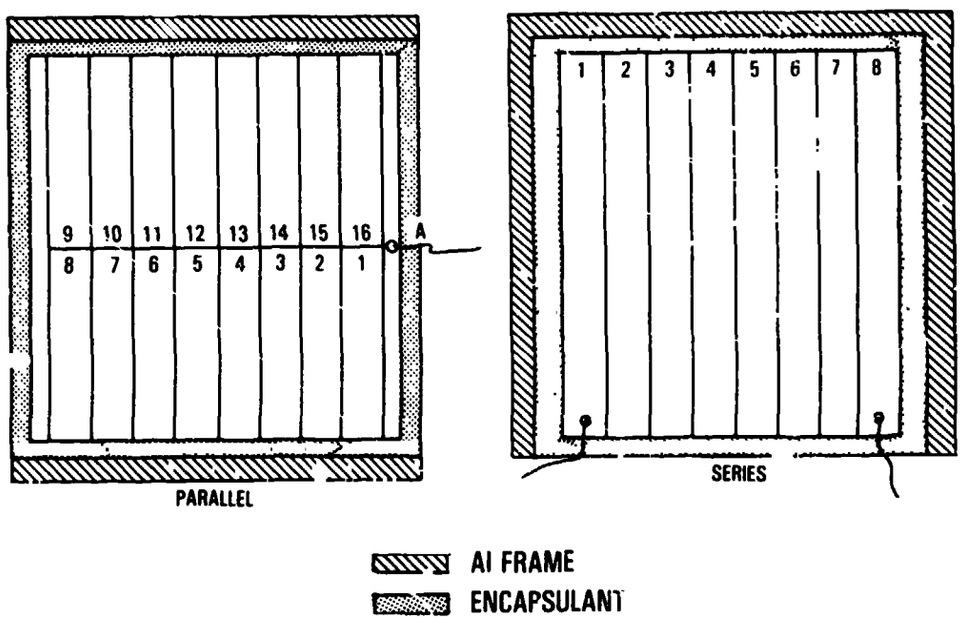


Figure 15

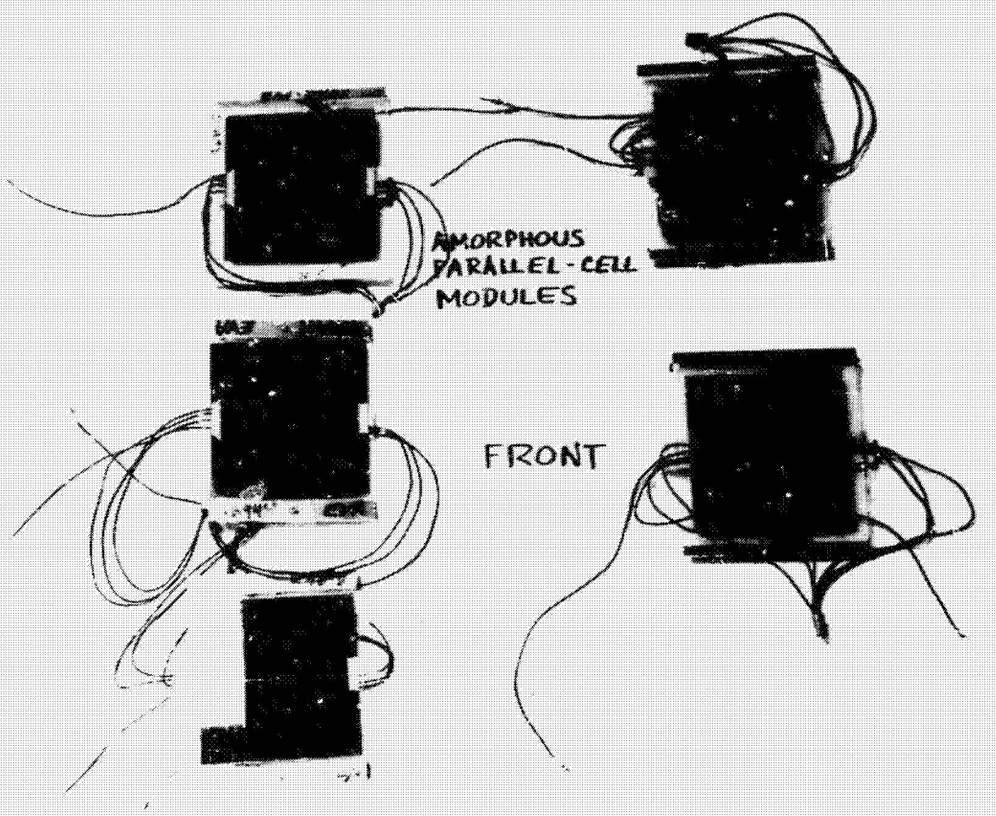


Figure 16

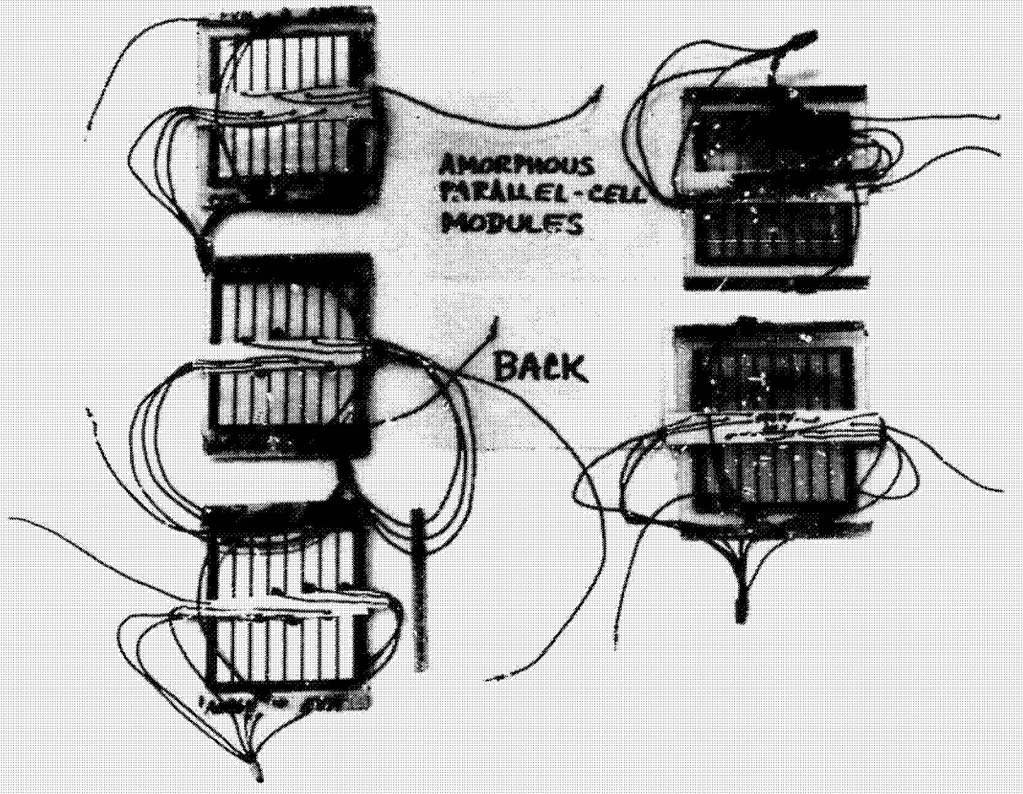


Figure 17

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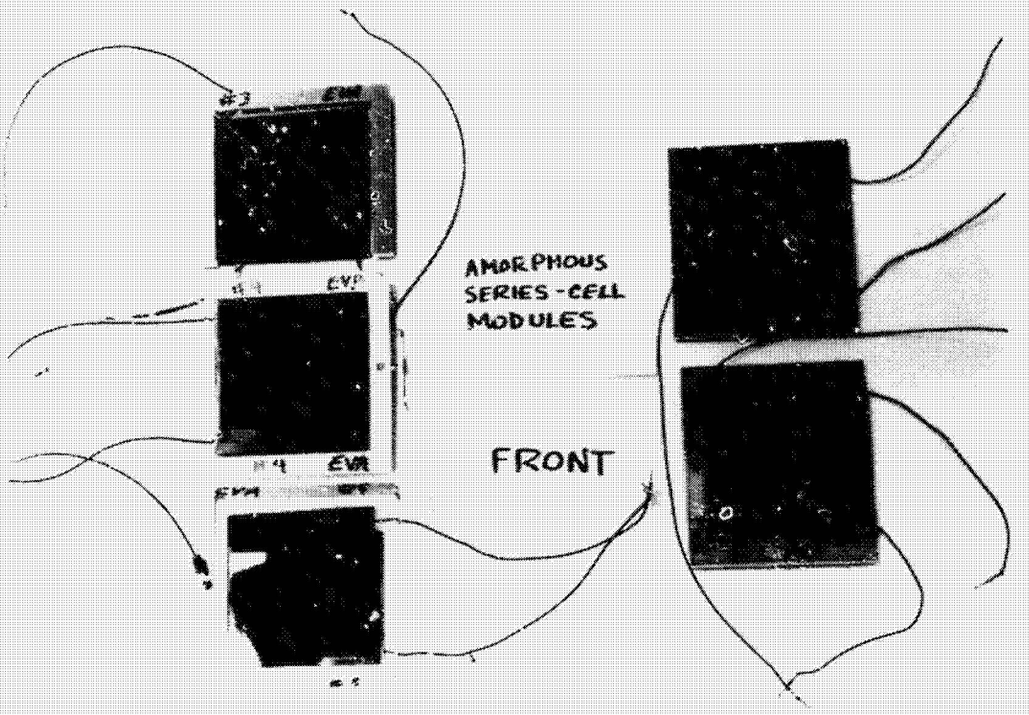


Figure 18

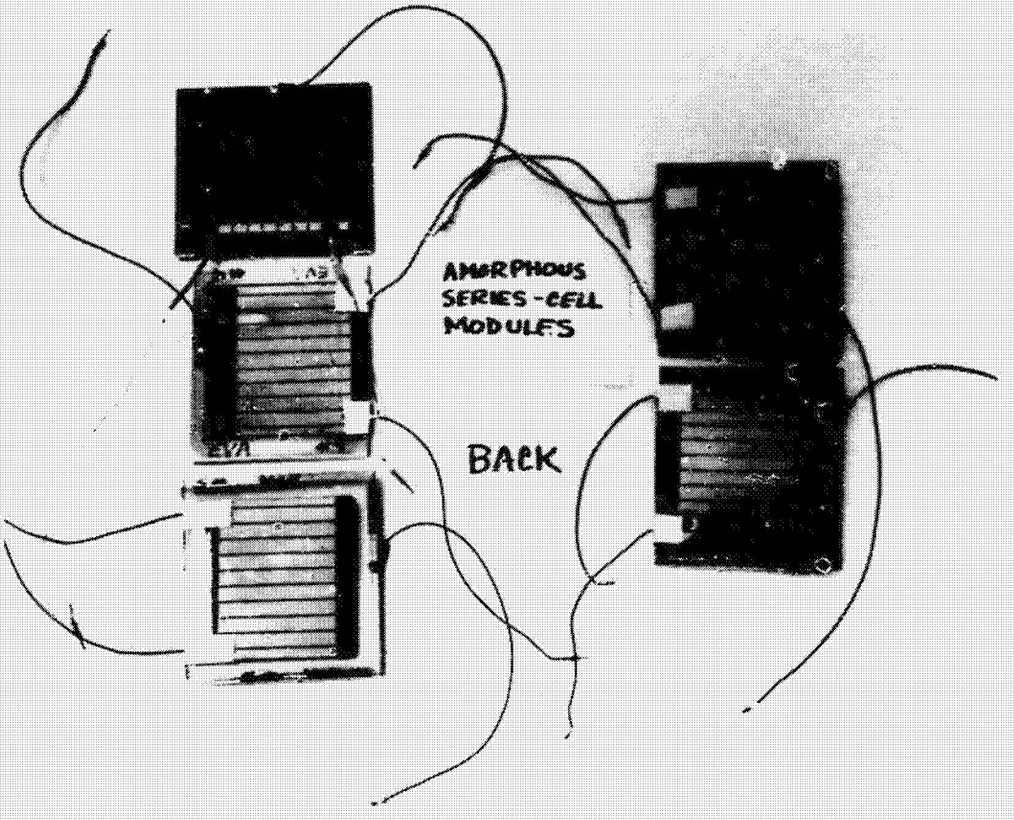


Figure 19

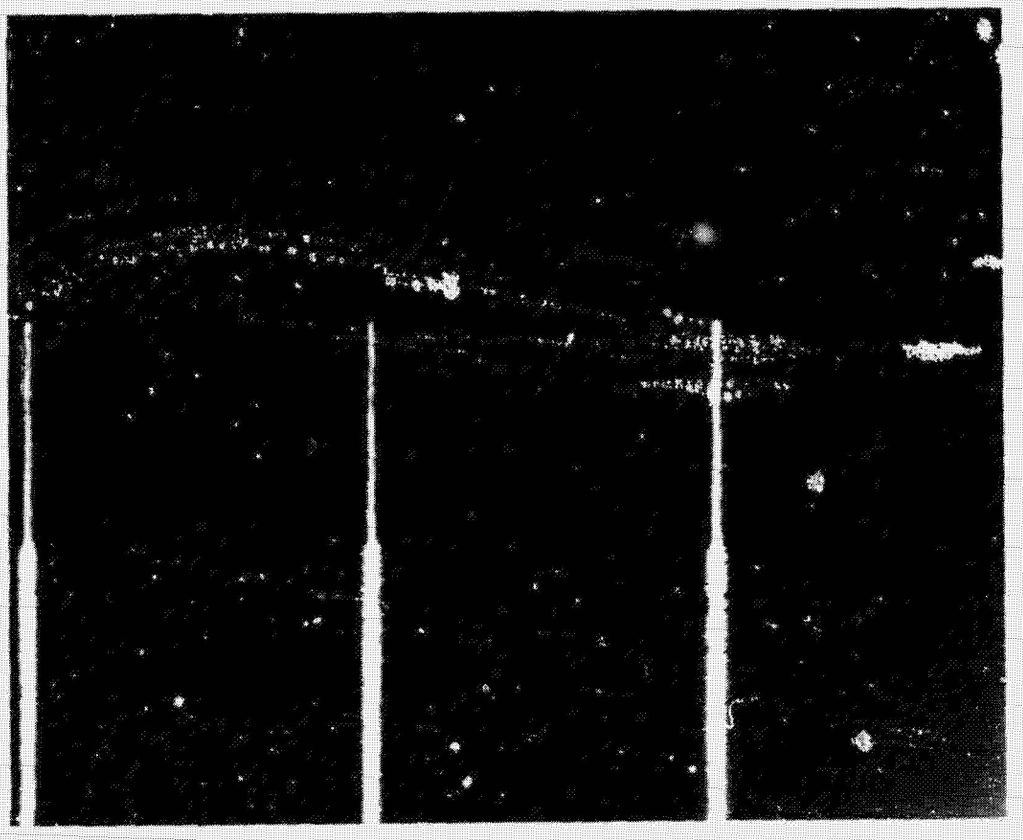


Figure 20

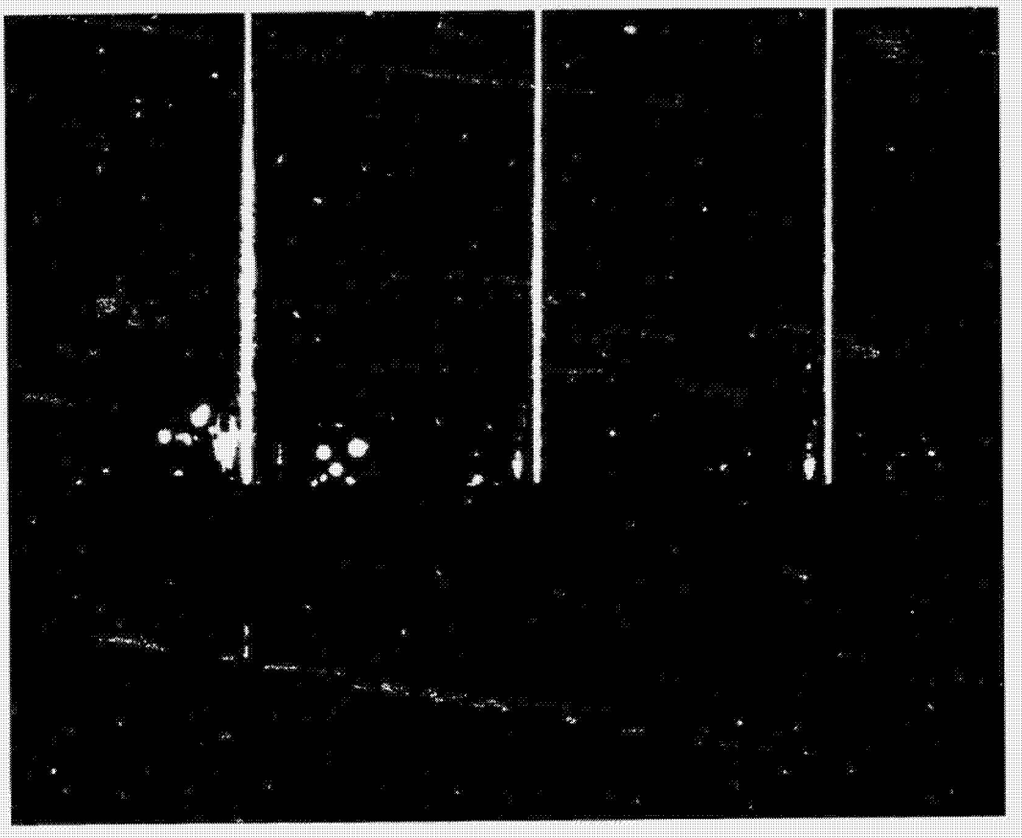


Figure 21



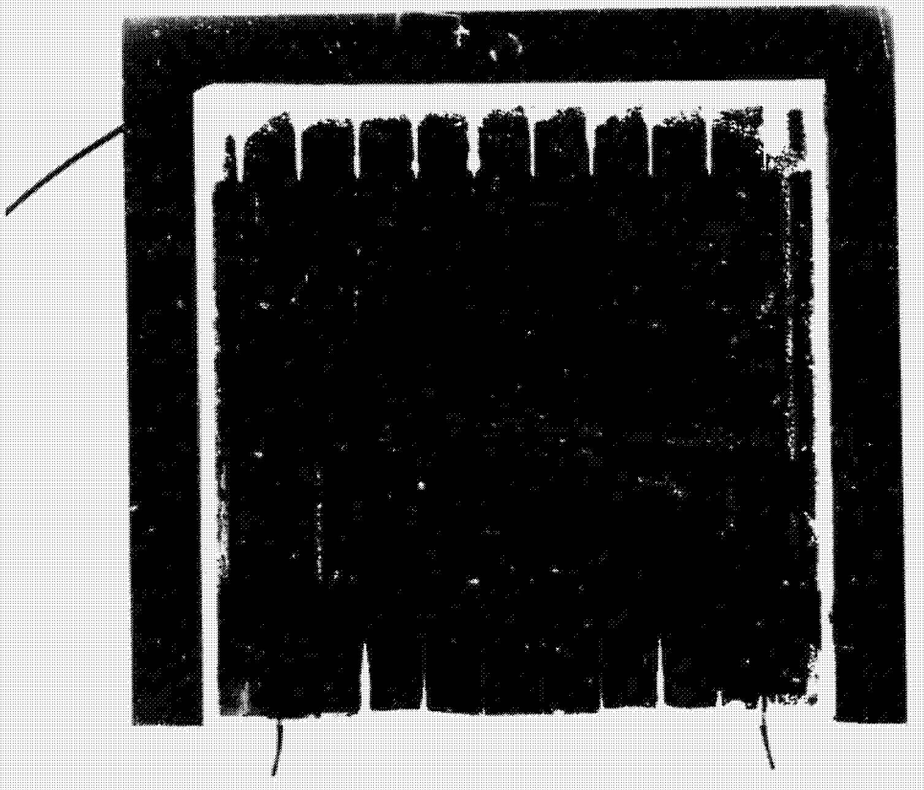
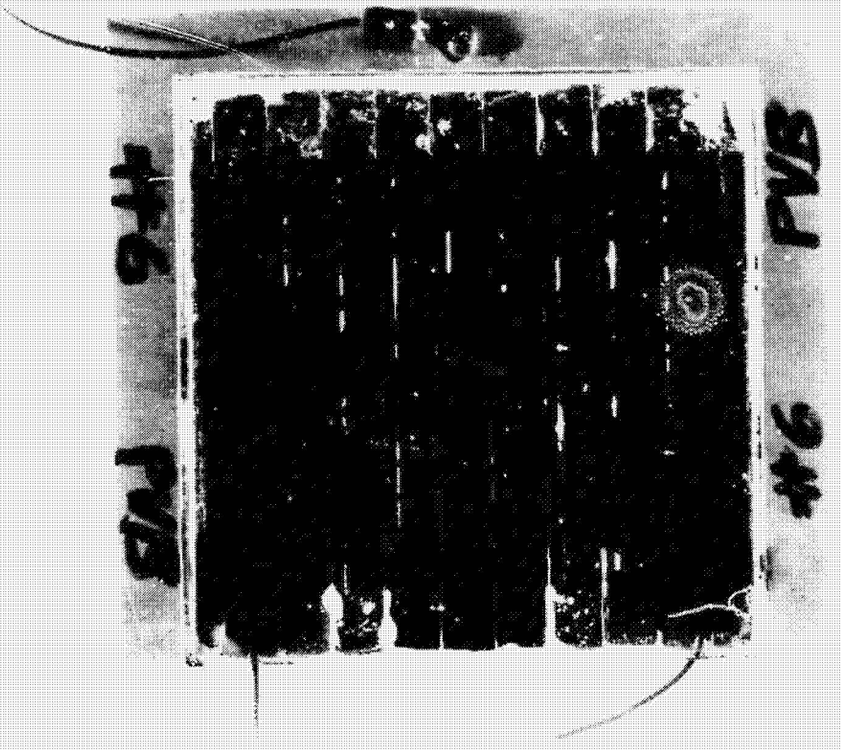


Figure 22

Figure 23





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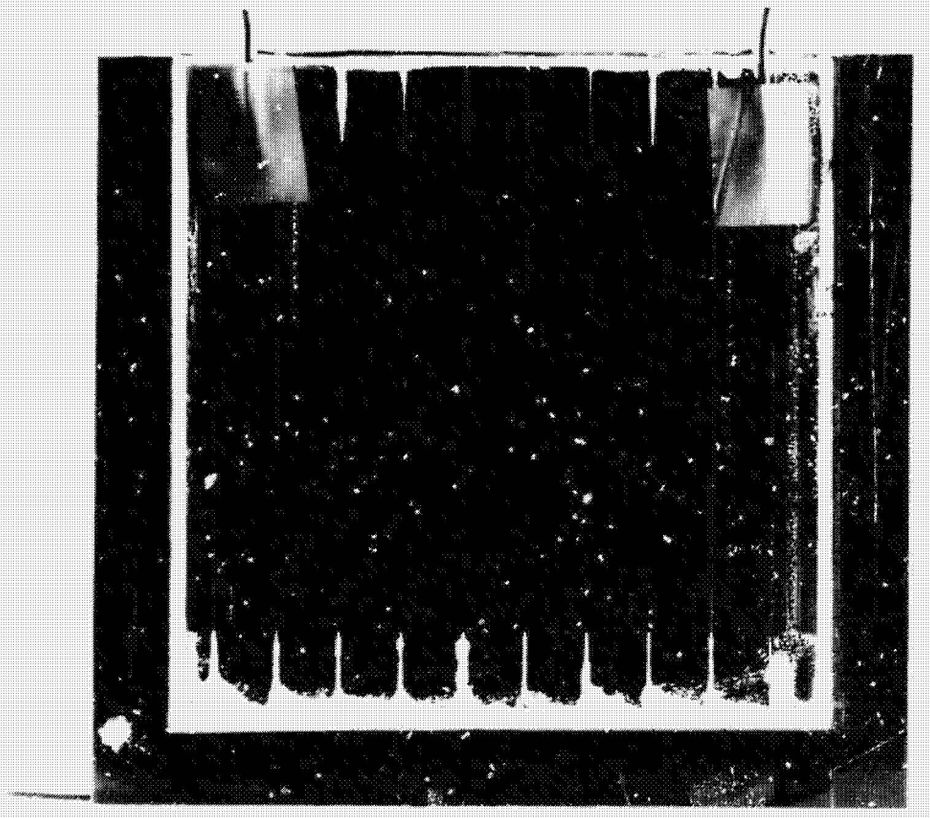
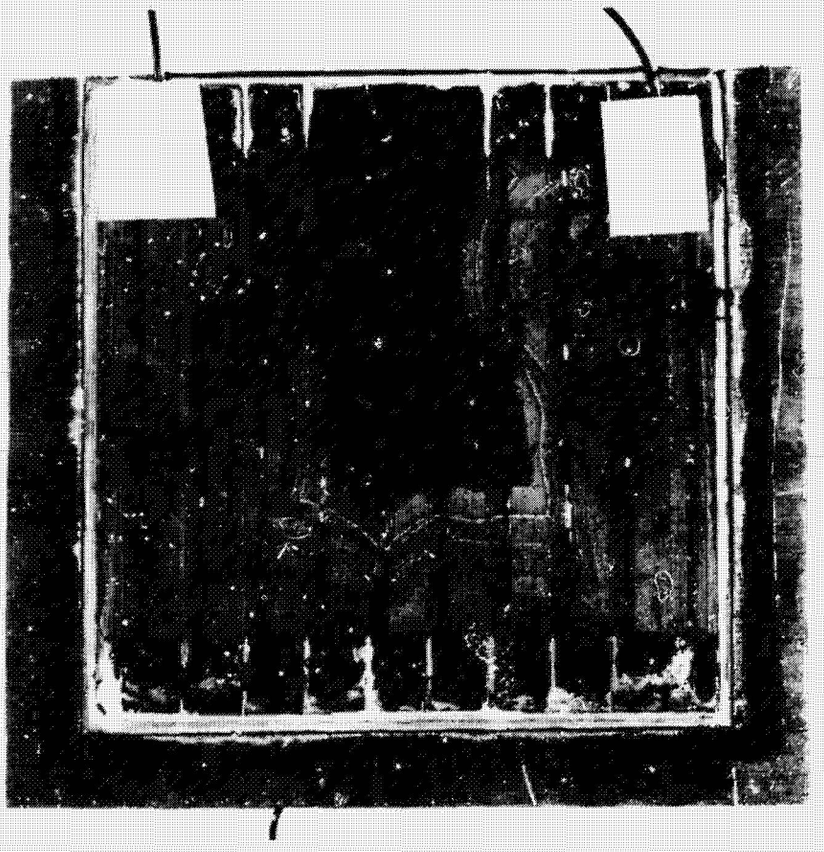


Figure 25





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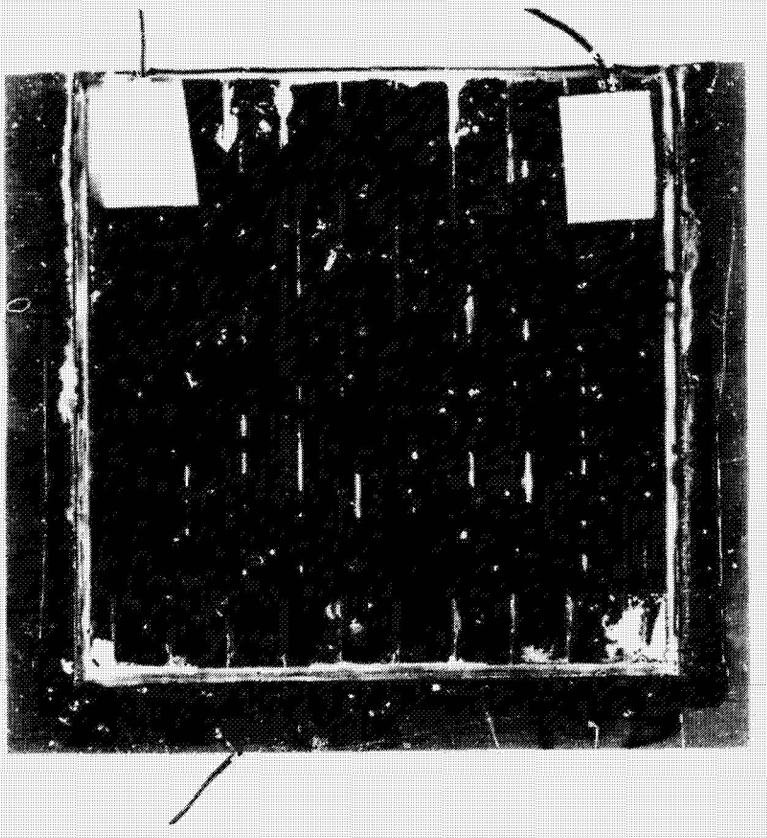
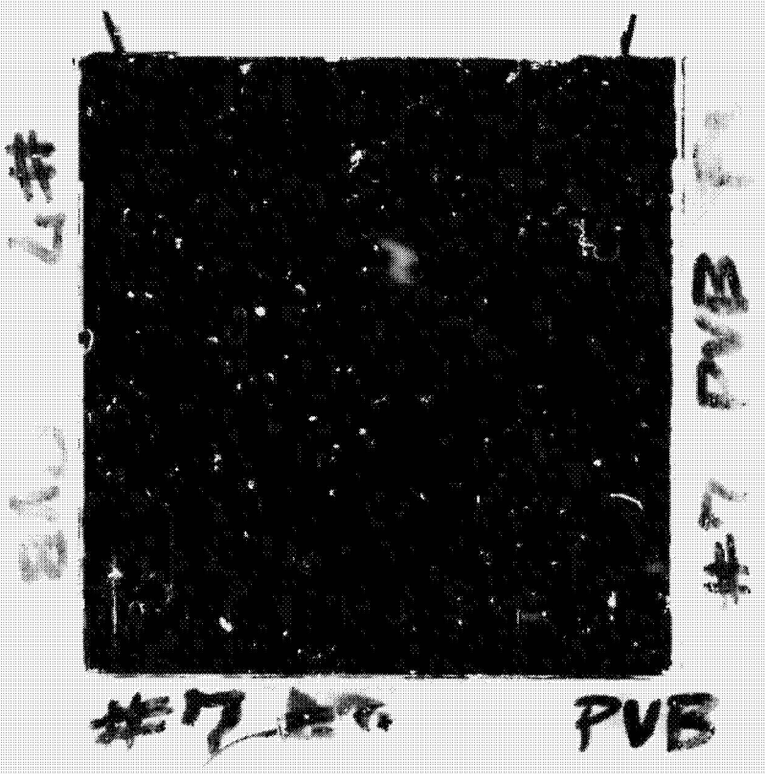


Figure 27





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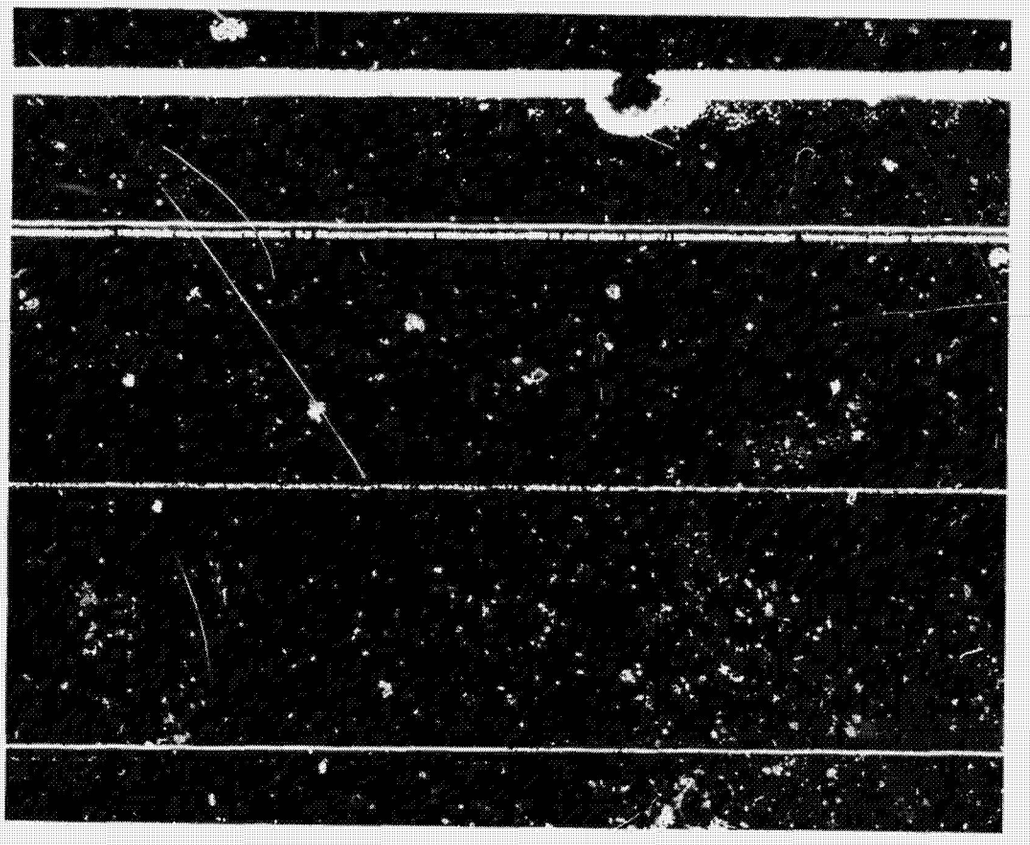


Figure 29



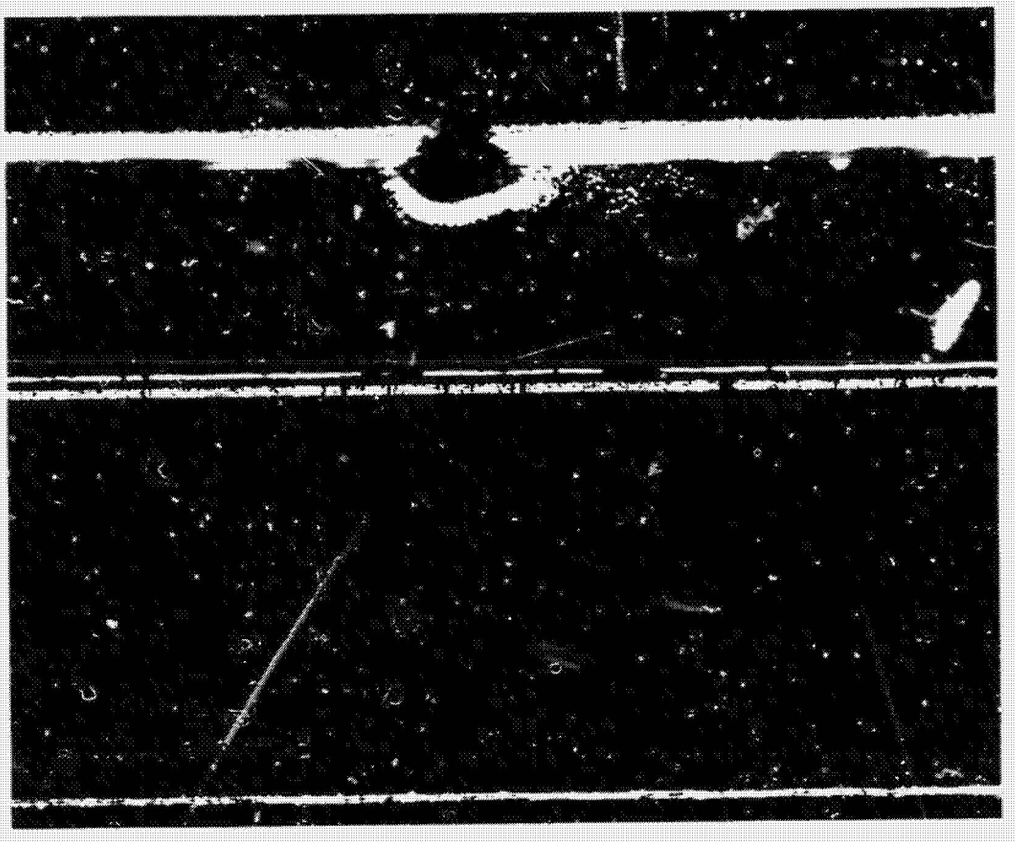
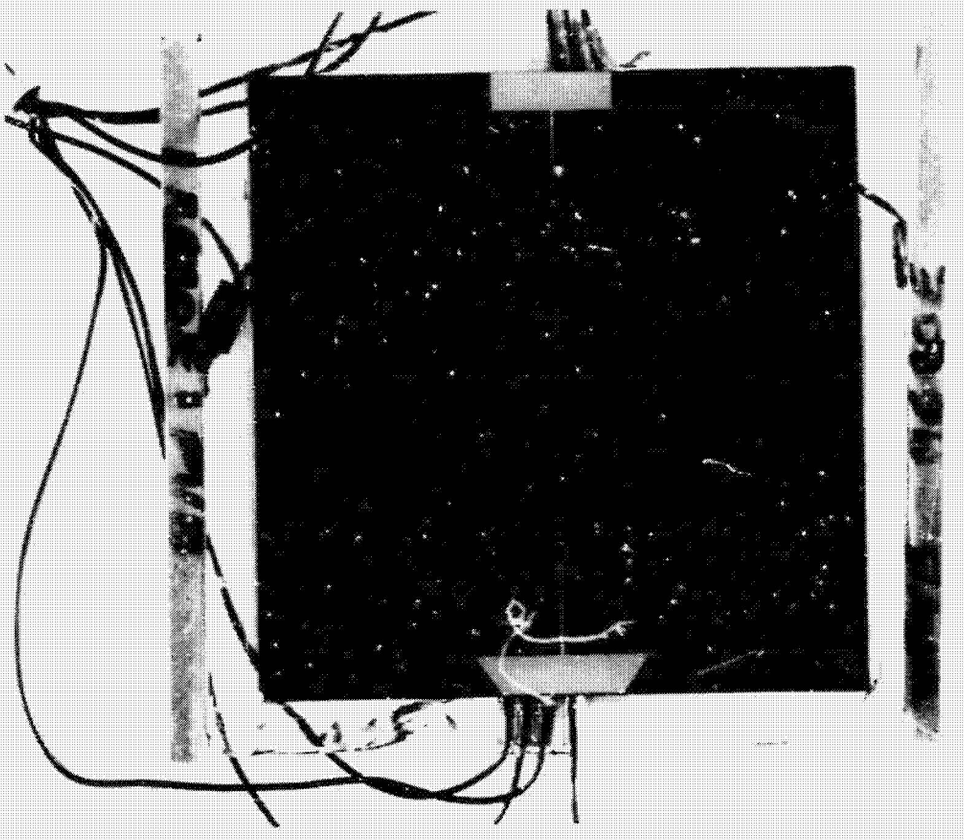


Figure 30

Figure 31





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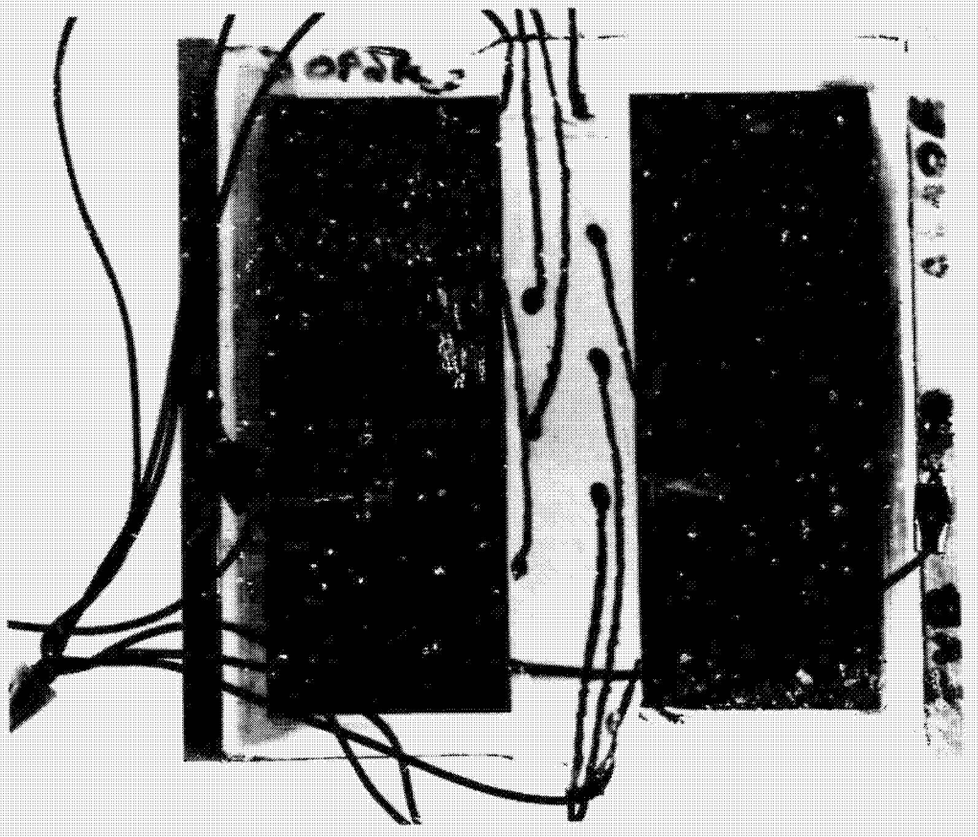


Figure 34



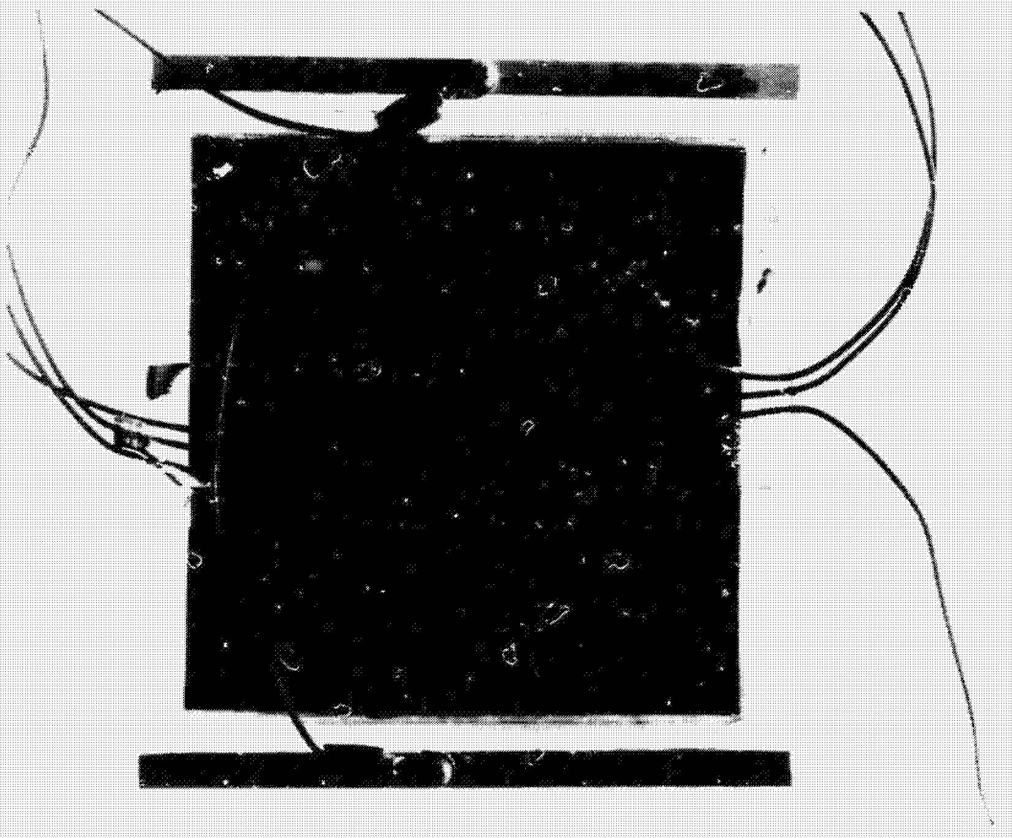


Figure 35

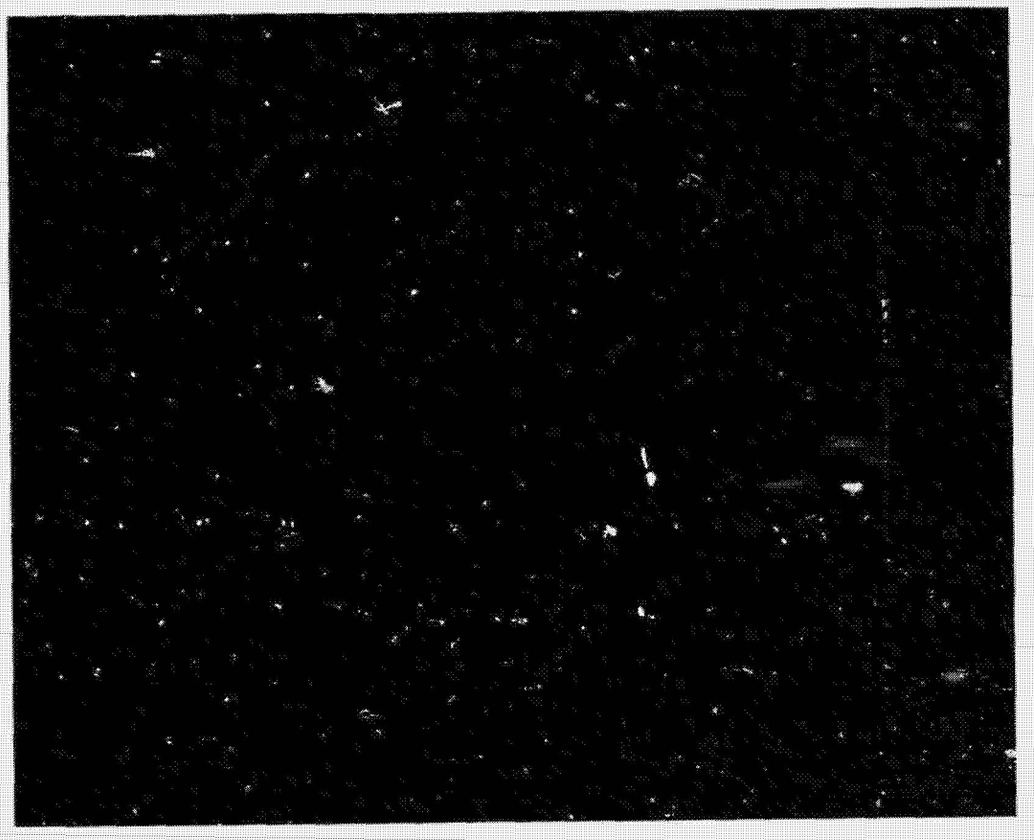
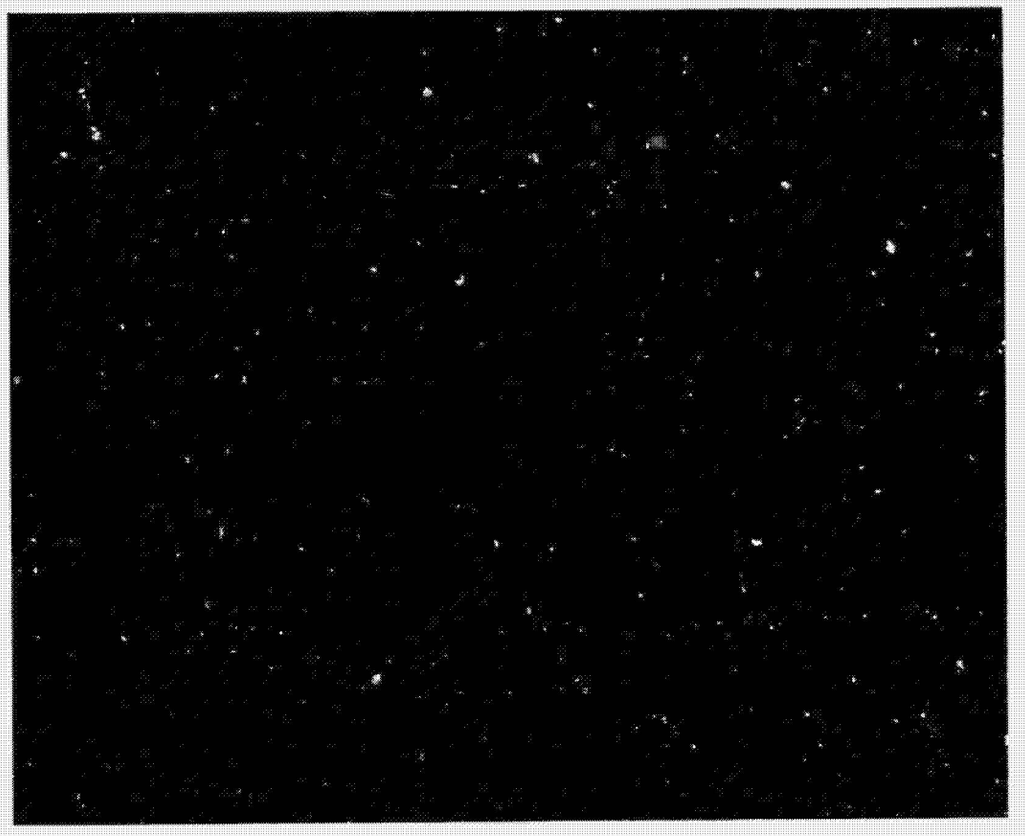


Figure 36



## DISCUSSION

ROSS: Let me start out with just a comment to second what Gordon said at the very beginning. Even though these things look horrible, in fact the total amount of charge transfer to destroy an amorphous module is very comparable to what it is for the crystalline-silicon module. What is interesting here is that this particular mechanism is causing a form of degradation that we don't really understand, in terms of these little wormy looking erosions that don't follow the normal patterns. In crystalline we always erode the part of the cell that's next to the electrode. With amorphous we don't see erosion next to the electrode; we see this very selective strange-looking erosion out in the middle of the cell at some seemingly random spot.

JESTER: Did you measure the I-V curves of any of those cells before and after? I mean obviously they looked terrible, but did it show up as series resistance, as you might expect?

MON: We had a weirdness happen when we were attempting to measure pre-test I-V curves, so we got hardly any, but we did get I-V curves at 40 hours, 130 hours and 300 hours. The basic degradation occurred in series resistance, although there was some short circuit current reduction, probably due to encapsulation obscuration. I must say that we have had a crash program to gather data, but we haven't had much time to analyze, to go deeply into what's really happening.

JESTER: I was wondering if they all do it, or was there one cell on one module, or many of them?

MON: No. Four parallel modules survived unscathed -- the four modules encapsulated in EVA -- except for that one picture I showed, where it looked like there were watermarks. And then the fifth parallel module was PVB, and that was the one that gave us all these wormholes. So, it's something to do with the PVB, probably with the plasticizer and all the alien ions in the plasticizer. All the series modules showed extensive degradation.

JESTER: Are these modules all from one company?

MON: We got these modules from two companies. If you want to know the names of them, see me later. The parallel modules were basically test modules. They certainly had no pedigree, we just got them and tested them. The series modules were made for the purpose, I guess, of producing power.

MARSHALL: We have seen similar mysterious corrosion in aluminum layers on space cells. Primarily contamination by borides or bromides. Polarities have a second-order effect; you may be looking at something that would have occurred without voltage. If you had some kind of contaminant in there at those humidities -- there is

some literature on it. Primarily in painted metal surfaces on ships and things. We have seen it on the back-surface reflector of a cell, usually in greater than 70% relative humidity.

LESK: For central-power generation your first curve showed that no matter what the metallization system, after 1 C/cm they all died. Are you saying there is a finite calculable lifetime for central power where your voltage will be above 500 volts?

MON: I'm saying it seems to be that between 1 and 10 C of charge per cm of frame edge length is necessary to produce, say, 50% failures. We don't have this down solid. It was surprising that the amorphous gave a very similar result. So I think I can say with some justification that somewhere between 1 and 10 C/cm you are going to get about 50% cell failure. We have taken that number and run with it. We developed a life-prediction algorithm; the question is, how much faith do you have in that algorithm? The answer is, I have a lot of faith in it. Even though I could not say it is precisely 4.2 C/cm, it is somewhere between 1 and 10, an order of magnitude. That is basically all you are interested in, in life prediction anyway, at this point.

ARNETT: Was it dangerous for us to bid on the SMUD program, then?

ROSS: First of all, with EVA-encapsulated modules we have done some life prediction, and it appears you have the equivalent of almost 30 years of life with conventional crystalline or amorphous modules. It is a non-problem. Now that I have said that, let me withdraw all of that and say, with respect to a lot of amorphous modules, there is not any EVA between the module and the frame. The conductive oxide layer goes on the amorphous module right out to the edge of the glass. And it turns out that it's your gasket, your lovely gasket that the Hughes person spoke about earlier, that may be, in fact, the determiner of these integrated corrosion currents. This is why it becomes terribly important -- the selection of the edge treatment of these modules, in terms of the isolation of the TO coating away from the edge of the glass, and the very careful treatment of that gasket isolation from the frame. This also obviously includes wet environments, so that even if you have a plastic frame, if the entire surface of the plastic is wet and it's matted on a metal structure, you may have basically an electrically conductive path up to the edge of whatever this gasket is. The PVB here, even though it looks bad, really works for us as a standard of known high-conductivity encapsulant material that allows us to have fairly large numbers of amp-hours in fairly short periods of time, which means you could accelerate it in a testing environment. EVA, with a very high resistivity, is a thousand times less effective in the test of showing degradation, so things come out looking very pretty. The bottom line is to take these data now on total corrosion currents and try to relate them to your module design with your particular edge treatment and your particular gasket. This gives you a feeling that you can measure corrosion currents with your modules; you can relate it back to whether or not you will survive

in the field. If you predict between 1 and 10 C/cm of edge for your module, you will be in trouble. You can show that it is in the order of magnitude below that, then you are probably not in too bad shape.

ARNETT: Just to clarify my thinking on the construction of the test samples that you used, was it only the edge that is exposed, and PVB between?

ROSS: The whole thing is encapsulated in EVA. That in the gap between the frame and the cell is EVA. The submodule has EVA on all sides of it. The whole thing is floating in a blob of material.

MON: The front surface is glass, the back surface is EVA.

ARNETT: So, like in an 85-85 environment, you have the maximum penetration capability. If you had a back sheet on that, or if it was glass, then you would be looking at the edge. At some point would you attempt to repeat these tests with a structure that represents more of a real-world module?

MON: Yes. That is one of our next steps.

ARNETT: Do it!

N86-12773 D14

# GLASS BREAKING STRENGTH--THE ROLE OF SURFACE FLAWS AND TREATMENTS

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## ABSTRACT

Although the intrinsic strength of silicon dioxide glass is of the order of $10^6$ lb/in.$^2$, the practical strength is roughly two orders of magnitude below this theoretical limit, and depends almost entirely on the surface condition of the glass, that is, the number and size of flaws and the residual surface compression (temper) in the glass. Glass parts always fail in tension when these flaws grow under sustained loading to some critical size.

Over the past eight years, research associated with glass-encapsulated crystalline-Si photovoltaic (PV) modules has greatly expanded our knowledge of glass breaking strength and developed a sizeable data base for commercially available glass types. A detailed design algorithm has been developed for thickness sizing of rectangular glass plates subject to pressure loads. This algorithm employs nomographs based on sophisticated non-linear finite-element stress analyses to determine the maximum stress in a glass plate. This stress is compared with the practical strength of glass plates derived from a large body of existing glass breakage data. Additional studies have examined the strength of glass under impact-loading conditions such as that caused by hail.

Although the fundamentals of glass breakage are directly applicable to thin-film modules, the fracture strength of typical commercial glass must be replaced with data that reflect the high-temperature tin-oxide processing, laser scribing, and edge processing peculiar to thin-film modules.

This paper reviews the fundamentals of glass breakage applicable to thin-film modules and presents preliminary fracture-strength data for a variety of 1-ft-square glass specimens representing pre-processed and post-processed sheets from current amorphous-Si module manufacturers.

## DISCUSSION

The objective of this presentation is to examine the applicability of current knowledge of glass breakage strength to the structural design of glass-supported thin-film PV modules. To this end, the research associated with glass-encapsulated crystalline-silicon PV modules is briefly reviewed. The applicability of this knowledge to thin-film glass modules is examined. Finally, the results of preliminary tests to characterize the mechanical strength of glass-supported thin-film PV modules are summarized.

The intrinsic strength of glass is on the order of $10^6$ lb/in.$^2$ The strength of large rectangular, commercially available, soda-lime glass sheets falls in the range of 3,000 to 20,000 lb/in.$^2$ depending on the surface condition and temper of the glass. This huge discrepancy between the intrinsic and usable strength of glass is due to the fact that glass is a brittle material. As such, it always fails in tension at pre-existing surface

flaws. The brittle failure mechanism of glass is helpful in explaining the dependency of the measured strength of glass on the factors delineated below:

(1) Strength increases with increased residual surface compression (temper) because applied tensile loading is reduced by the amount of the residual surface compression.

(2) Strength decreases with increased time duration of loading, because under a sustained load pre-existing flaws grow to some critical size, at which failure occurs.

(3) Strength decreases with increased stressed area due to the greater probability of a flaw existing within the stressed area.

Because the strength of glass depends on the number and size of flaws in the specimen tested, it is not surprising that apparently identical test specimens and loading conditions exhibit widely different measured strengths. For this reason, the strength of glass must always be cited for a given probability of failure.

In connection with the research devoted to glass-encapsulated crystalline-silicon PV modules, a design algorithm for thickness sizing of rectangular glass plates subject to pressure loads, such as wind, has been developed. This algorithm employs nomographs based on sophisticated non-linear finite-element stress analysis to determine the maximum stress in a glass plate. The maximum applied stress, so obtained, is compared with the strength of glass plates derived from a large body of empirical glass breakage data. Highlights of this design algorithm are shown in the figures that follow this text.

Thin-Film Glass Strength Tests

As discussed above, it is desired to establish the strength of the glass used for thin-film PV modules as a function of the processing to which the glass is subjected; i.e.,

(1) Edge treatment

(2) Thermal treatments

(3) Coatings applied

(4) Scribing

To accomplish this, burst-pressure tests were done on 1 x 1-ft-square glass specimens. The apparatus designed to do this is shown in a figure. Essentially, it consists of a rigid aluminum frame that provides simple support to the four edges of the square glass plates. Tap water, a pressure regulator and a needle valve are used to slowly pressurize the glass plate. A pressure transducer and a linear-motion transducer, with a strip chart recorder, are used to record the pressure and displacement versus time.

So far, 51 of 1 x 1-ft-square glass plates have been tested. These are described below by the number tested, thickness, temper, edge and surface

treatments. Note that the surface for which the surface treatment is described was placed in tension (convex) during the test.

| Number Tested | Description |
|---|---|
| 11 | 0.125 in.-thick annealed float glass with as-cut edges tested with tin side in tension |
| 21 | 0.125 in.-thick annealed float glass with sanded edges tested with tin-side in tension |
| 4 | 0.125 in.-thick annealed glass with as-cut edges obtained from manufacturer after TiO conductive coating had been applied |
| 10 | 0.042 in.-thick annealed glass with carefully rounded edges obtained from manufacturer after TiO conductive coating had been applied |
| 5 | 0.042 in.-thick annealed glass with carefully rounded edges obtained from manufacturer after scribing |

Photographs are included for three fractured glass specimens:

(1) 0.125 in.-thick annealed glass with as-cut edges.

(2) 0.042 in.-thick annealed glass with carefully rounded edges and TiO conductive coating.

(3) 0.042 in.-thick annealed glass with carefully rounded edges, TiO and Si coatings, and scribed.

The burst-pressure data obtained from these tests were converted to strength data using the non-linear design nomograph. These strength data are plotted on a graph included here that shows glass strength versus probability of failure. Also shown on this graph is the glass strength obtained from previous burst-pressure tests made by other investigators. Although somewhat on the low side, the strength values obtained in the current tests are in reasonable agreement with previously obtained results for glass strength. As is often the case when studying glass breakage data, the results of the current tests defy simple explanation. It would be expected, for example, that the specimens of annealed 1/8 in.-thick glass with ground edges would exhibit higher strength than the specimens with as-cut edges, but the test results show a higher strength for the specimens with as-cut edges. Another unexpected result is that the scribed 0.042 in.-thick specimens exhibited a higher average strength than their unscribed counterparts.

## Hail Impact Resistance

It is also desired to ascertain the hail impact resistance of glass-supported thin-film PV modules. Preliminary hail-impact tests have been conducted on thin-film modules from two manufacturers using the hail gun

developed for testing of crystalline-silicon PV modules. The hail gun uses air pressure to propel a frozen ice ball at a test specimen. These exploratory tests showed that the 0.125 in.-thick annealed-glass modules from one manufacturer were marginally inadequate for 1-in.-dia ice balls at 52 mi/h. Failure occurred in 2 of 42 impacts made near the edges of three modules. It is thought that the as-cut edges of these modules was a significant contributor to these failures. Photographs of two of these failures are included. The other module tested consisted of a 0.042 in. thick front glass-cover bonded to a 0.125 in.-thick back cover glass by a thin layer of a soft encapsulant material. This module survived 16 edge impacts of 1-in.-dia ice balls at 52 mi/h. It was not tested for larger ice balls. Finally, a bar graph shows the hail-impact resistance of PV modules for various module constructions.

## CONCLUSIONS

The analytical and empirical tools developed over the past eight years to characterize the mechanical strength of crystalline-silicon PV modules are applicable to the structural design of thin-film glass-supported PV modules. Preliminary test results indicate that glass-supported thin-film modules will be structurally adequate, but additional testing is mandatory to characterize further the strength of glass used for thin-film modules as a function of the surface treatments and processes to which it is subjected.

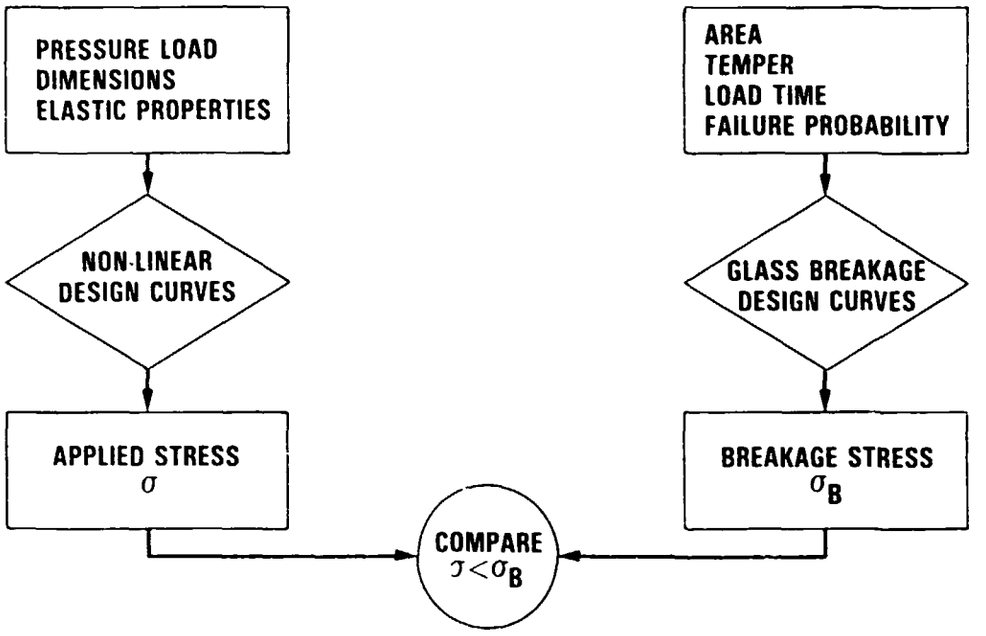
## Agenda

- Review of current knowledge of glass breakage
  - Theoretical considerations
  - Empirical results
- Application of this knowledge to thin-film glass modules
- Examine problems peculiar to thin-film glass modules
  - Especially surface treatments of glass

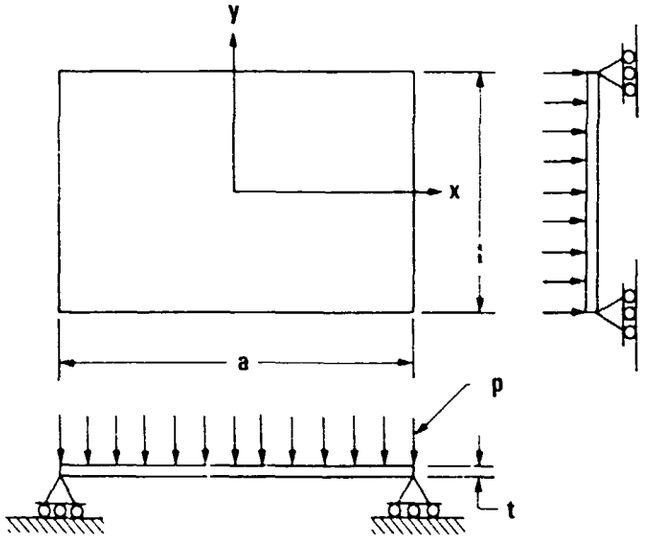
## Glass Breakage Strength

- Inherent strength $\approx 1{,}000{,}000$ lb/in.$^2$
- Apparent strength $\approx 3{,}000$ to $20{,}000$ lb/in.$^2$
- Brittle failure mechanism explains why
  - Glass always fails in tension at flaws
  - Strength increases with increased surface compression (temper)
  - Strength decreases with increased flaw size
  - Strength decreases with increased duration of load
  - Strength decreases with increased stressed area
- Strength of glass is therefore stated for a given probability of failure

## Glass Thickness Sizing Method




## Uniformly Loaded, Simply Supported Rectangular Plate




a = LENGTH OF PLATE

b = WIDTH OF PLATE

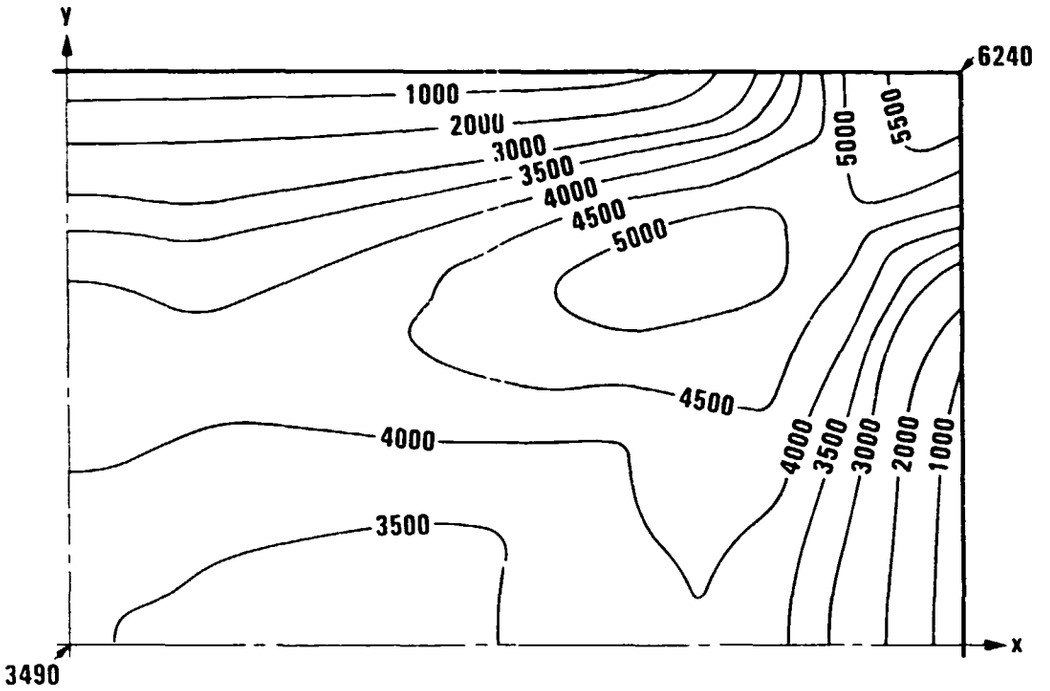
t = THICKNESS OF PLATE

p = PRESSURE

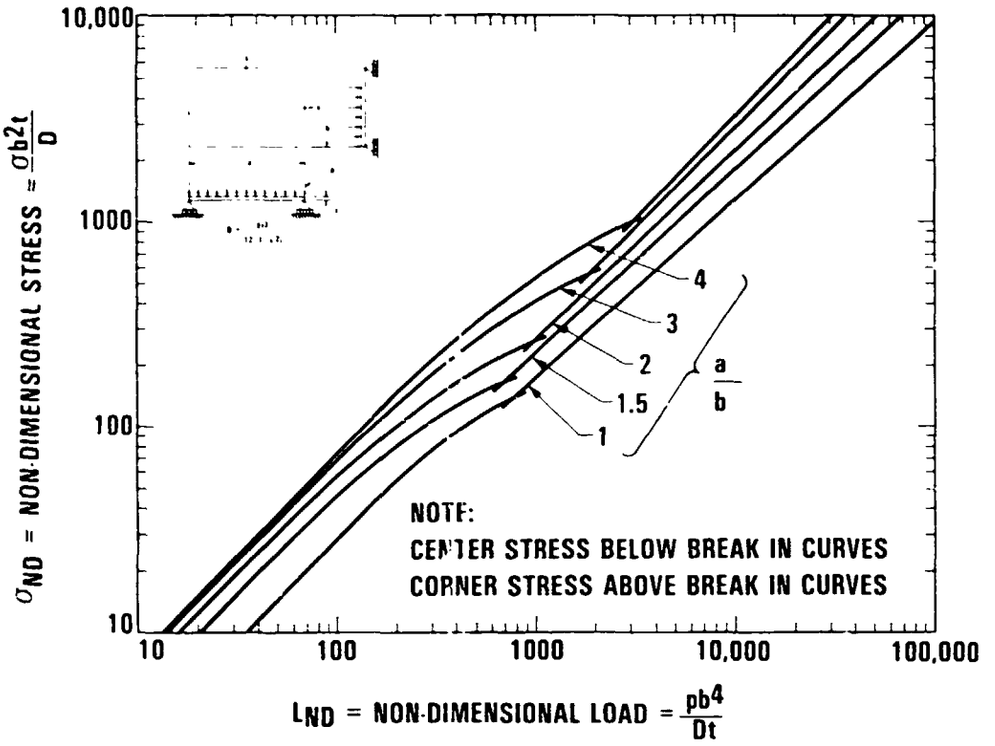
E = YOUNG's MODULUS

$\nu$ = POISSON's RATIO

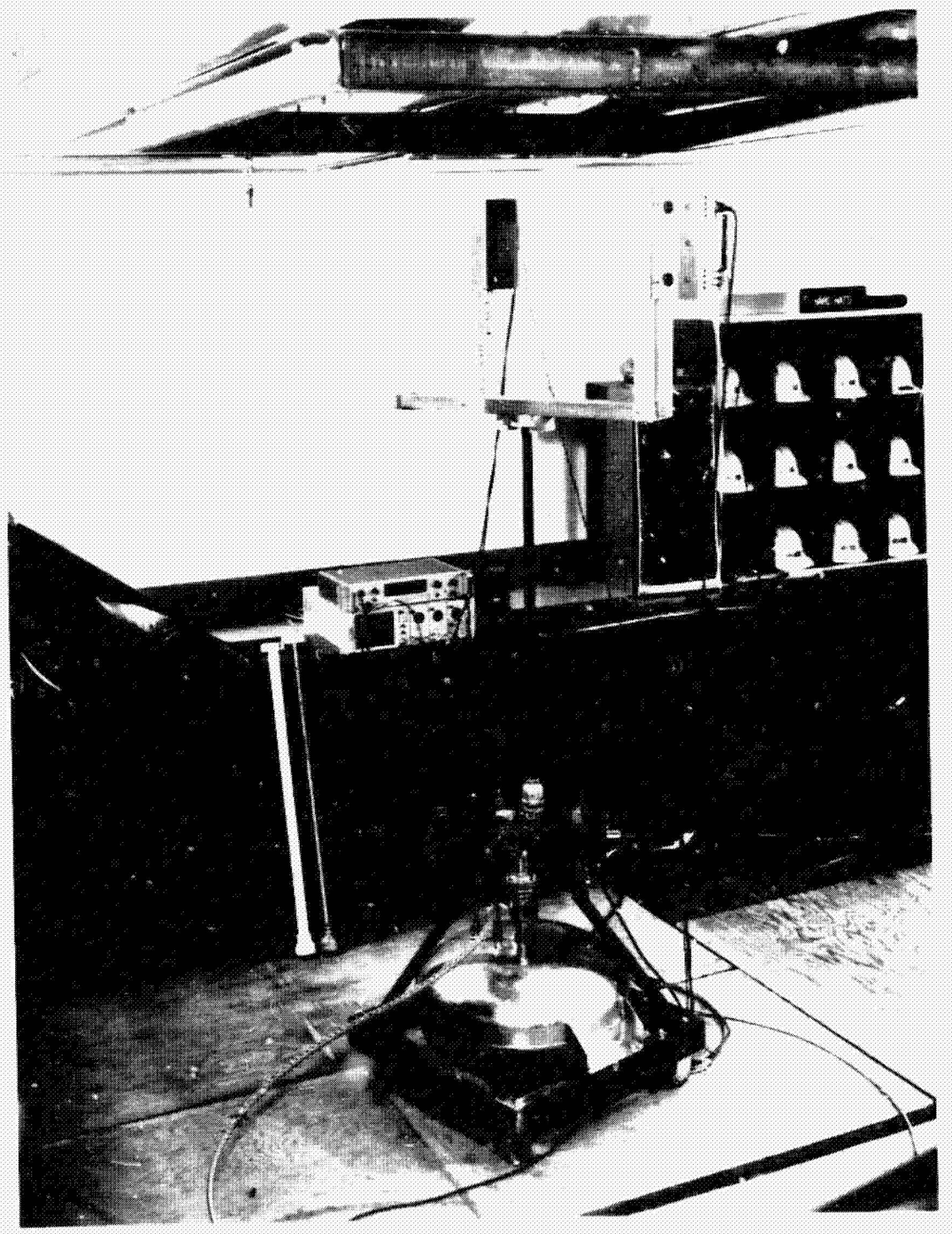
Maximum Principal Stress Contours



## Stress vs Load



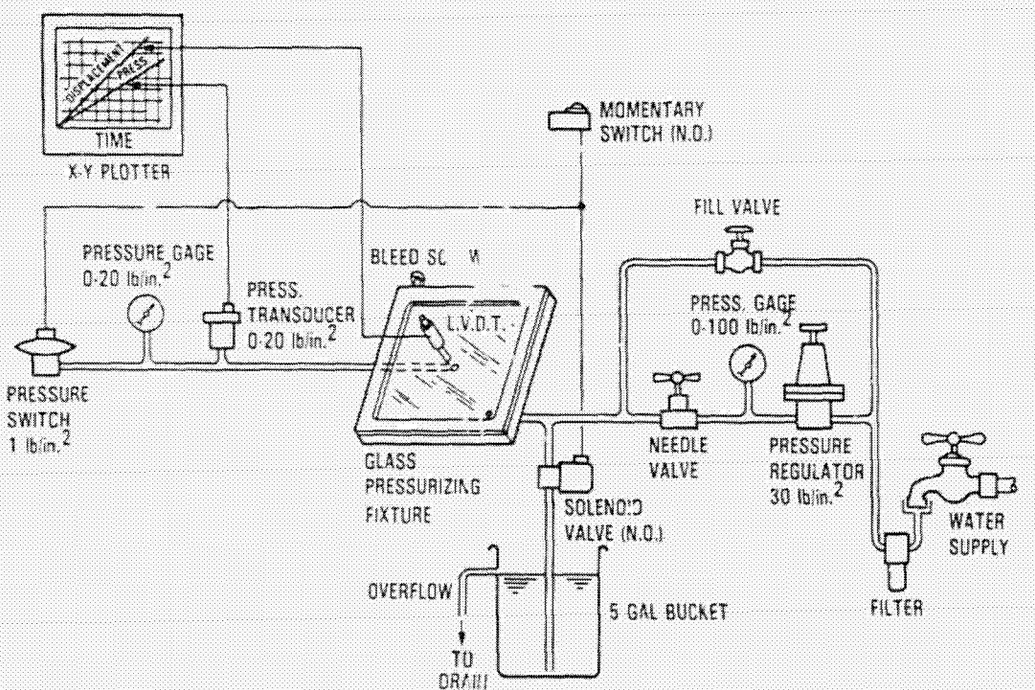
Hail Gun Uses Air Pressure to Propel
Frozen Ice Balls at Specimen



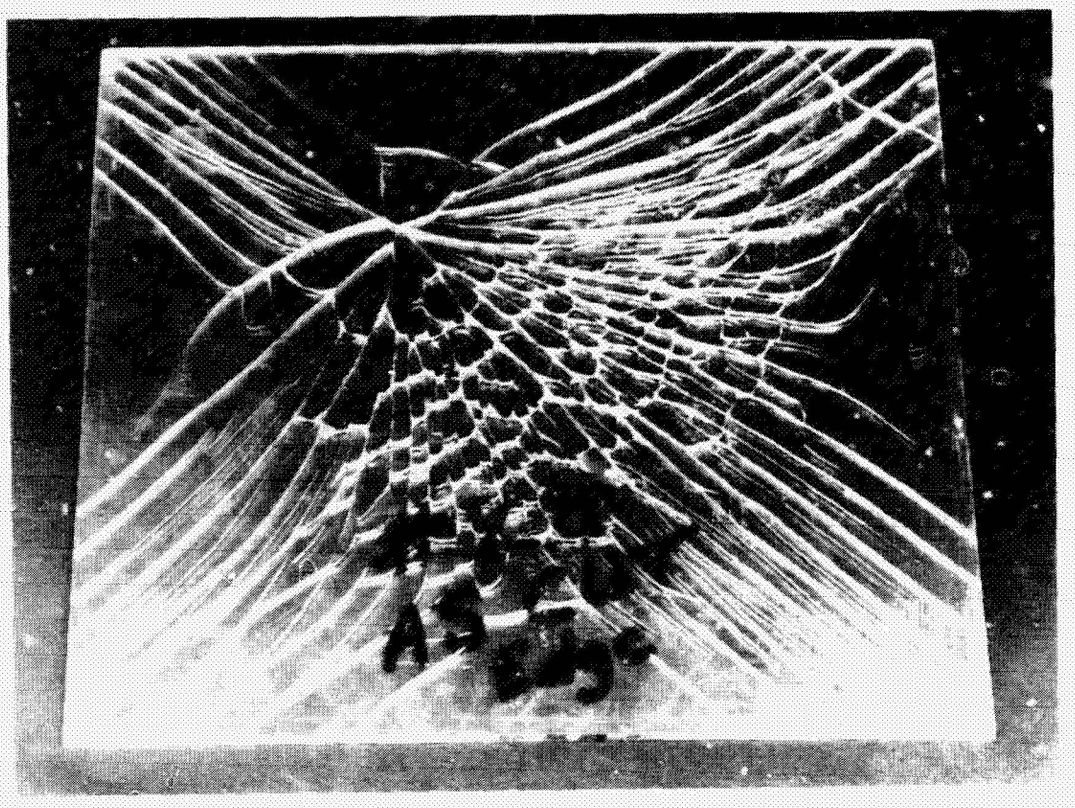
## Strength of Thin-Film Glass Modules

- Problem:
  - Establish breakage strength statistics for treated glass used for thin-film photovoltaic modules as a function of:
    - Edge treatment
    - Conductive coating (TiO)
    - Laser scribing
- Approach:
  - Conduct burst pressure tests of treated 1 x 1 ft. glass samples

## Glass Burst-Pressure Test Apparatus for 1 x 1-ft Glass Samples



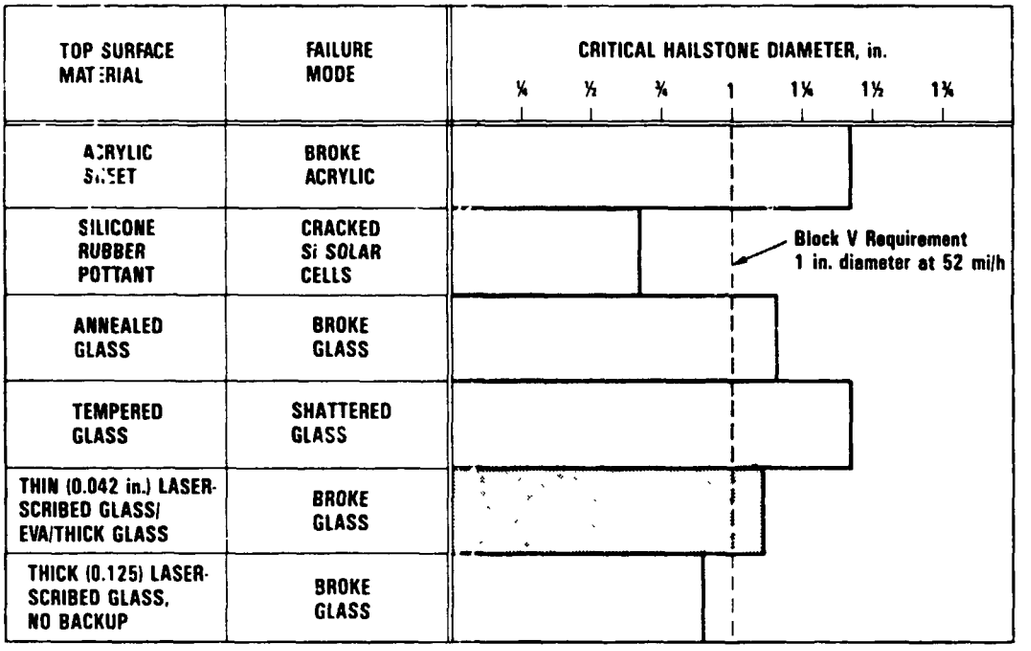
0.125 x 12 x 12-in. Annealed Glass Plate
With As-Cut Edges Failed at 4.67 lb/in.$^2$



0.042 x 11.8 x 11.8-in. Annealed Glass Plate With Rounded Edges and TiO Conductive Coating; Failed at 0.90 lb/in.$^2$

0.042 x 11.8 x 11.8-in. Annealed Glass Plate With Rounded Edges, TiO and Si Coatings, and Scribed; Failed at 0.99 lb/in.$^2$

# Hail Impact Resistance



# ENCAPSULANT SELECTION AND DURABILITY TESTING EXPERIENCE

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## ABSTRACT

The Flat-Plate Solar Array Project (FSA) has established technically challenging cost and service-life goals for photovoltaic modules. These goals are a cost of $\$70/m^2$, and an expected 30 years of service life in an outdoor weathering environment. Out of the cost goal, $\$14/m^2$ is allocated for encapsulation materials, which includes the cost of a structural panel. At FSA's inception in 1975, the cumulative cost of encapsulation materials in popular use, such as room-temperature vulcanized (RTV) silicones, aluminum panels, etc., greatly exceeded $\$14/m^2$. Accordingly, it became necessary to identify and/or develop new materials and new material technologies to achieve the goals.

Many of these new materials are low-cost polymers that satisfy module engineering and encapsulation processing requirements but unfortunately are not intrinsically weather-stable. This necessitates identifying lifetime and/or weathering deficiencies inherent in these low-cost materials and developing specific approaches to enhancing weather stability. In addition, relevant accelerated aging techniques must be developed to enable assessment of encapsulation system lifetimes. Specific items include the development of chemically attachable stabilization additives [ultraviolet (UV)-screening agents, antioxidants, etc.], computer-assisted kinetic modeling of outdoor weathering reactions, and the use of novel outdoor heating racks and controlled environmental reactors in accelerated aging techniques. Other encapsulation technologies related to life and durability include soiling, electrical insulation, and primers and adhesives.

## Encapsulation Systems

The two basic encapsulation systems for terrestrial photovoltaic modules are the substrate system and the superstrate system. These design classifications refer to the method by which the encapsulated solar cells are supported mechanically. A substrate design has encapsulated cells supported by a structural backside panel, and in the superstrate design the encapsulated cells are supported by a transparent, sunside structural panel (e.g., glass). These two basic systems have up to nine material components, called construction elements. These are illustrated in a viewgraph, with their designations and encapsulation functions.

Low-cost candidates for the substrate panels are mild steel and hardboard; glass is the lowest-cost candidate for the superstrate panel. Plastic materials used structurally as either a substrate or a superstrate are considerably

higher in cost. The low-cost candidate for the porous spacer is a non-woven E-glass mat. Low-cost candidates for all of the other construction elements are polymeric.

Polymeric Encapsulation Materials

Pottants. The central core of an encapsulation system is the pottant, a transparent, elastomeric material that is the actual encapsulation medium in a module. It totally encloses and embeds all of the solar cells and their associated electrical circuitry. The demands on a pottant material are numerous; some of the more significant requirements follow:

(1) It must be highly transparent in the silicon solar-cell response region of 0.4 to 1.1 μm.

(2) It must function as electrical insulation for isolating high-voltage circuitry.

(3) It must provide mechanical cushioning and stress media for fragile solar cells.

(4) It must be readily processable in automated module fabrication.

The cells and circuitry encapsulated with the pottant must be supported mechanically by either a structural substrate panel or a transparent structural superstrate panel. If supported by a backside (substrate) panel, the top surface of the soft elastomeric pottant must be covered with a hard, durable front-cover film to reduce soil accumulation. Soft surfaces have a greater tendency to retain soil than do hard surfaces. To identify the lowest-costing transparent elastomeric materials that could function as pottants, it was specified that the pottant material, either as is or with appropriate additives, shall be resistant to hydrolysis and thermal oxidation at temperatures up to 80°C, but UV sensitivity was allowed. This selection approach was predicated on the concept that the lowest-costing encapsulation systems could not isolate the elastomeric pottant from atmospheric moisture and oxygen, but that cost-effective UV filtering could be accomplished either by a glass superstrate or by the a low-soiling front-cover plastic film placed over the pottant on a substrate module.

Four pottant materials have emerged as most likely candidates and are currently in various stages of development or industrial use: ethylene vinyl acetate (EVA), ethylene methyl acrylate (EMA), poly-n-butyl acrylate (PnBA), and aliphatic polyether urethane (PU). EVA and EMA are dry films designed for vacuum-bag lamination at temperatures up to 150°C. Above 120°C during the lamination process, EVA and EMA undergo peroxide crosslinking to become tough, rubbery thermosets. PnBA and PU are liquid casting systems. PnBA, a polymer-monomer syrup, was developed jointly by JPL and Springborn Laboratories, Inc. PnBA is being formulated to cure within 15 minutes at 60°C. A commercial polyether urethane for pottant application is available from Development Associates, North Kingston, Rhode Island, marketed under the designation Z-2591.

Ethylene Vinyl Acetate. EVA is a copolymer of ethylene and vinyl acetate,

typically sold in pellet form by Du Pont Co. and U.S. Industrial Chemicals, Inc. (USI) The Du Pont trade name is Elvax; the USI trade name is Vynathane. The cost of EVA typically ranges between $0.55 and $0.65 per pound. All commercially available grades of EVA were examined and the list was reduced to four candidates, based on maximum transparency: Elvax 150, Elvax 250, Elvax 4320, and Elvax 4355. Because EVA is thermoplastic, processing it into a module is best accomplished by vacuum-bag lamination with a film of EVA. Therefore, based on film extrudibility and transparency, the best choice became Elvax 150. Elvax 250 was an extremely close second choice.

Elvax 150 softens to a viscous melt above 70°C, and therefore is not suitable for temperature service above 70°C when used in a fabricated module. A cure system was developed for Elvax 150 that results in a temperature-stable elastomer. Elvax 150 was also compounded with an antioxidant and UV stabilizers, which improved its weather stability and did not affect its transparency. These ingredients are compounded into Elvax 150 pellets, followed by extrusion at 85°C to form a continuous film. The thickness of the clear film is nominally 18 mils. The selective curing system is inactive below 100°C, so that film extruded at 85°C undergoes no curing reaction. The extruded film retains the basic thermoplasticity of the Elvax 150. Therefore, during vacuum-bag lamination, the material will soften and process as would a conventional laminating resin.

This EVA pottant has undergone extensive industrial evaluation, and manufacturers of photovoltaic (PV) modules have reported certain advantages:

(1) Lower cost.

(2) Good appearance.

(3) Clarity.

(4) Non-yellowing.

(5) Obviates cold storage.

(6) Dimensional stability.

(7) Pressure autoclave not required.

(8) Good flow properties and volumetric fill.

Although this encapsulation-grade EVA has been favorably received by the industry, its status is still considered to be experimental. To advance EVA, several developmental tasks remain to be completed:

(1) Faster processing, primarily in the cure schedule, which involves a reduction in cure time and temperature; the minimum cure temperature will be dictated by the requirement that the curing system must not become active during film extrusion.

(2) Optimization of the UV-stabilization additives; the present additives were selected on the basis of literature citations and industrial experience with polymers similar to EVA.

(3) Identification of the maximum service temperature allowed for EVA in a module application to ensure long life.

(4) Industrial evaluation of the desirability of having a self-priming EVA, recognizing the possibility of an additional cost component (cost-benefit-performance tradeoff).

Consideration of these tasks has led to the development of an advanced formulation for EVA, designated 18170.

EVA Aging Studies. Elvax 150 can be degraded by UV photooxidation, thermal oxidation, and by purely thermal decomposition of the acetate groups to acetic acid. These degradation reactions are stated in order of decreasing severity, and as protection against each in order is provided, the life and associated peak service temperature of EVA encapsulant can be extended.

Fundamental analysis of Elvax 150 suggests that the UV wavelengths deleterious to this material, and necessary for UV photooxidation, are those shorter than 360 nm. Isolation of Elvax 150 from these UV wavelengths by means of UV-filtering outer covers and/or compounding additives such as Cyasorb UV-531 stops UV photooxidation and reduces the aging characteristics of Elvax 150 to thermal effects. This basic and very simple concept was established as a fundamental module-design philosophy, and no problem with this concept has been identified in the experimental aging results to date.

For example, testing of EVA samples in the RS/4 UV chambers at 55°C included the following combinations:

(1) Elvax 150 without any protection, either additives or UV-screening film overlays.

(2) Elvax 150 with a UV-screening film overlay, but with no antioxidant or UV-absorbing additives.

(3) Fully compounded and cured A-9918 EVA, with an antioxidant and UV-absorbing additives but with no UV-screening film overlay.

The Elvax 150 sample (No. 1) without any protection yellowed visibly and degraded within 1000 h of exposure, whereas samples Nos. 2 and 3 with UV protection as indicated have survived 20,000 h to 30,000 h of exposure without any degrading incidences. Accepting that the UV protection for the latter two samples acted to isolate or protect them from deleterious UV wavelengths, then their aging at 55°C was reduced to that of thermal aging. And further, as no aging effects were detected in these two samples, with or without an antioxidant, these tests indicate strongly that Elvax 150 at 55° either is naturally resistant to thermal oxidation, or undergoes negligibly slow thermal oxidation.

If it can be assumed that a module using Elvax 150 as a pottant provides the necessary UV protection, and if it can be assumed that such a module may

be at or near a daily array peaking temperature of 55°C for about 5 h each day, then 20,000 h to 30,000 h of accumulated thermal aging in the RS/4 chambers corresponds to 11 to 16 years of potential outdoor service. For module applications having daytime peaking temperatures near 55°C, it appears that the life of the EVA encapsulant is related more to the life of the UV protection schemes and less to either the thermal behavior of the EVA or thermal protection schemes (for example, antioxidants).

Between 55°C and 93°C (200°F) there is no direct experimental or literature information on the thermal aging behavior of Elvax 150. Unresolved questions relate to knowing if a threshold temperature exists for Elvax 150, above which thermal oxidation begins, to knowing the temperature dependence of the rates of thermal oxidation of Elvax 150, and to knowing the effectiveness of antioxidants and the associated temperature dependence of their protective induction periods. Although the 10 mo (7200 hours) of thermal stability observed at 90°C for the dark-thermal aging of cured A-9918 EVA is encouraging, it is not known whether this is natural to the Elvax 150, or that 10 mo was still within the protective induction period of the antioxidant. In addition, the concentration of Cyasorb UV-531, a critical element of the UV protection scheme, was not monitored in these thermally aged specimens.

The potential for long service life of EVA in modules at rooftop temperatures (e.g., 85°C) looks encouraging, but predictions of lifetime would be premature. As at 55°C, UV protection and permanence of the UV protection are essential. After that, it is not clearly established which of the thermally driven processes is most critical. These processes include the basic thermal oxidation properties of the Elvax 150, of antioxidants and the associated temperature dependency of their protective induction periods, and the temperature dependence of any physical loss and depletion of the protective compounding additives themselves, such as the UV and thermal stabilization additives.

UV Screening Plastic Films. The module front cover is in direct contact with all of the weathering elements: UV, humidity, dew, rain, oxygen, etc.; therefore, the selected materials must be weatherable. Only four classes of transparent materials are known to be weatherable: glass, fluorocarbons, silicones and polymethyl methacrylate.

In addition to weatherability, the front cover must also function as a UV screen, to protect underlying pottants that are sensitive to degradation by UV photooxidation or UV photolysis. The outer surface of the front cover should also be easily cleanable and resistant to atmospheric soiling, abrasion-resistant, and antireflective to increase module light transmission. If some or all of these outer-surface characteristics are absent in the front-cover material, additional surfacing materials may have to be applied.

Excluding glass, the only commercially available transparent UV-screening plastic films that have been identified are fluorocarbon films (Tedlar, Du P , and PMMA films (Acrylar, 3M Co.).

Back Covers. Back covers are back-surface material layers that should be weatherable, hard, and mechanically durable and tough. Engineering analysis indicates that the color of the back-surface material layer should be white, to aid module cooling. Back covers function to provide necessary back-side

protection for substrates, such as (for example) corrosion protection for low-cost mild-steel panels, or humidity barriers for moisture-sensitive panels. For superstrate designs, the back cover provides a tough overlay on the back surface of the soft, elastomeric pottant. If a metal foil is selected for the back cover of a superstrate design, an additional insulating dielectric film should be inserted in the module assembly between the cells and the metal foil.

Edge Seals and Gaskets. Trends based on technical and economic analysis suggest that butyls should be considered for edge seals, and EPDM elastomers should be considered for gaskets. Several materials for each application are under investigation. One of the more promising edge-seal materials is a butyl-edge sealing tape designated 5354 (3M Co.), and one of the more promising EPDM gasket materials is designated E-633 (Pawling Rubber Corp.).

Primers and Adhesives. Continuing FSA work on this encapsulation technology has resulted in the development of three general-purpose primers for all module interfaces. It should be pointed out that these primers are experimental, and that an assessment of their lifetime and durability is in progress. Results are extremely encouraging.

Electrical Insulation. A new concept has been developed regarding the possible definition of the intrinsic dielectric strength of insulating materials, which can be considered as a fundamental material property similar to Young's modulus, index of refraction, etc. The concept, if valid, provides an absolute material property related to electric insulation that can be directly monitored as a function of accelerated and/or abbreviated aging. This concept will be evaluated as part of the module life assessment studies.

Outdoor Heating Racks. A novel accelerated aging technique has been developed using outdoor racks on which test materials and modules can be heated to fixed temperature levels above ambient, to accelerate aging from exposure to the natural weathering elements, e.g., oxygen, UV, humidity and pollution. Trial outdoor aging tests are currently being carried out at 70°C, 90°C and 110°C. The outdoor heating racks are programmed to turn on at 6:00 a.m. to a preset temperature, and to turn off at 6:00 p.m. to permit test materials and modules to cool overnight. It is intended that the rates of change of material properties and module performance parameters monitored at elevated temperatures in the natural environment can be used to estimate ongoing rates at the lower temperatures associated with actual module performance.

A viewgraph shows polypropylene aging data measured on the these racks. Extrapolation of the higher-temperature aging data to ambient predicts an outdoor aging lifetime for this polypropylene of about a third to a half of a year. This is virtually the actual aging lifetime for unstabilized and/or unprotected polypropylene outdoors. With this satisfying observation, future work will shift to encapsulation materials, and to fully fabricated modules.

Low-Soiling Surface Coatings. Evolving soiling theories and physical examinations of soiled surfaces suggests that soiling accumulates in three layers. The first layer involves strong chemical attachment, or strong chemisorption of soil matter on the primary surface. The second layer is physical, consisting of a highly organized arrangement of soil matter effecting a gradation in surface energy, from a high associated with the energetic first layer, to the

lowest possible state on the outer surface of the second layer. The lowest possible surface-energy state is dictated by the chemical and physical nature of the regional atmospheric soiling materials. After these first two layers are formed, the third layer constitutes a settling of loose soil matter, accumulating in dry periods and being removed during rainy periods. The aerodynamic lifting action of wind can remove particles greater than about 50 μm from this layer, but is ineffective for smaller particles. Thus, the particle size of soil matter in the third layer is generally found to be less than 50 μm.

Theories and evidence to date suggests that surfaces that should be naturally resistant to the formation of the first two rain-resistant layers are hard, smooth, hydrophobic, free of first-period elements (for example, sodium), and have the lowest possible surface energy. These evolving requirements for low-soiling surfaces suggest that surfaces or surface coatings should be of fluorocarbon chemistry.

Two fluorocarbon coating materials, a fluorinated silane (L-1668, 3M Co.), and perfluorodecanoic acid, are under test. The perfluorodecanoic acid is chemically attached to the surfaces with a Dow Corning chemical primer, E-3820. The coatings on glass and on the 3M Acrylar film are being exposed outdoors in Enfield, Connecticut, and the loss of optical transmission by natural soil accumulation is being monitored by the performance of standard solar cells positioned behind the glass and film test specimens. These test specimens are not washed. Twenty-eight months of test results are shown for glass and Acrylar.

After 28 months outdoors, soil accumulation on the uncoated glass control has resulted in about a 2.65% loss of cell performance, whereas the glass coated with L-1668 has realized only about a 1.59% loss. The glass sample coated with perfluorodecanoic acid has realized about the same loss. The uncoated Acrylar control has realized about a 7.20% loss, whereas the loss on the sample coated with perfluorodecanoic acid is only about 7.20%, and the loss on the Acrylar sample coated with L-1668 is about 4.2%. Similar results are obtained on the Tedlar samples. The test results indicate that compared with untreated controls, soil accumulation is being reduced on those test samples treated with the candidate fluorocarbon surface coatings.

Encapsulation Engineering. An engineering analysis of encapsulation systems has been carried out to achieve a reliable and practical engineering design. This analysis involves four necessary features of a module:

(1) Structural adequacy.

(2) Electrical isolation (safety).

(3) Maximum optical transmission.

(4) Minimum module temperature.

One of the goals of this analysis is the generation of guidelines for minimum material usage for each of the construction elements.

The analyses for structural adequacy showed that thermal expansion or wind deflection of photovoltaic modules can result in the development of mechanical

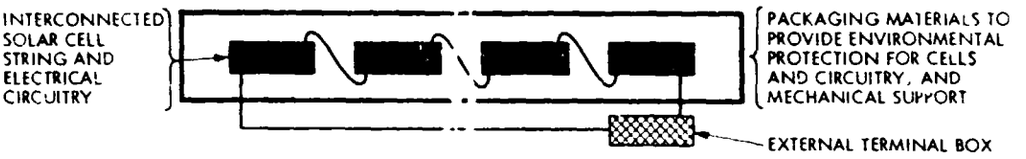
stresses in the encapsulated solar cells sufficient to cause cell breakage. The thermal stresses are developed from differences in the thermal expansion properties of the load-carrying panel and the solar cells. However, the analysis showed, interestingly, that the solar-cell stresses from either thermal expansion differences or wind deflection can be reduced by increasing the thickness t of the pottant, or by using pottants with lower Young's modulus E. In other words, the analysis indicates that the load-carrying panel can be considered to be the generator of stress, and that the pottant acts to damp the transmission of the stress to the cells. The pottant's ability to damp transmitted stress is directly related to the ratio of its thickness to modulus (t/E).

For example, the analysis finds, for a 4-ft-square glass-superstrate module undergoing a 50 mph wind deflection, that the pottant t/E ratio should be equal to or greater than 4:1, where t is in mils and E is in units of klb/in.$^2$. At a ratio of 4:1, the solar-cell stresses are just at their allowable limit. If the pottant were EVA having a Young's modulus E of 0.9 klb/in.$^2$ would necessitate that the thickness of that pottant be correspondingly increased. It should be mentioned that the t/E requirement of a glass-superstrate module undergoing thermal expansion is only 2:1. Thus solar-cell stresses generated by the wind deflection of a glass-superstrate module, rather than thermal expansion effects, dictate the minimum usage requirements of pottants.

This kind of output from the engineering analysis begins to enable a cost-comparison basis for candidate materials. For example, compared with EVA, a higher-costing pottant having a higher Young's modulus would be much more costly to use for reasons of both higher materials cost and the need for more thickness. On the other hand, a higher-costing pottant having a lower Young's modulus may be just as cost-effective due to an allowed thinner usage.

Advanced Thin-Film Encapsulation Concepts. The last four viewgraphs illustrate some advanced encapsulation concepts for thin-film photovoltaic modules. Essentially, the concepts involve direct coating of a liquid resin onto the cell surfaces, followed by photo-curing, or by electron-beam curing. A novelty is that the liquid resin is actually a mixture of immiscible polymer fluids that, before the curing phase, separate into layers, from a soft elastomeric inner layer to a hard, tough, and weatherable top layer.

## Basic Components of a Photovoltaic Module




COST ALLOCATION (1980 DOLLARS) FOR PACKAGING MATERIALS

TOTAL MODULE COST = 70 CENTS / WATT ≈ $7.00/FT$^2$ ≈ $70.00/m$^2$

PACKAGING COST = 14 CENTS / WATT ≈ $1.40/FT$^2$ ≈ $14.00/m$^2$

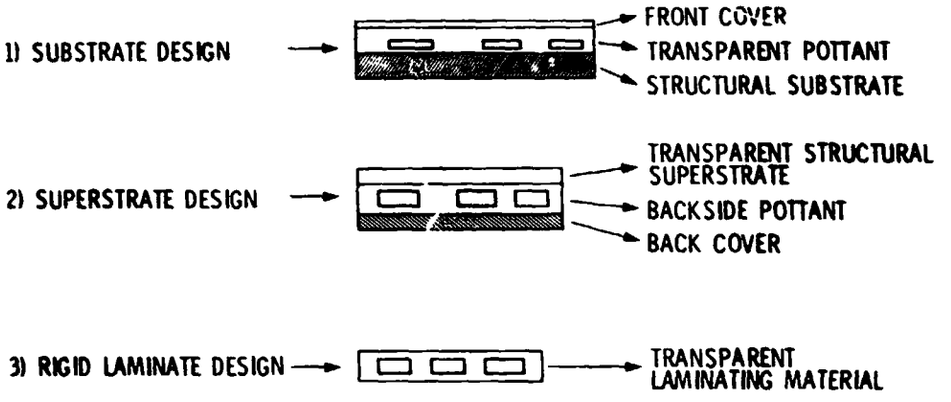
ALL ELSE = 56 CENTS / WATT

- CELLS
- INTERCONNECTS
- TERMINAL
- MANUFACTURING
- PROFITS
- TAXES

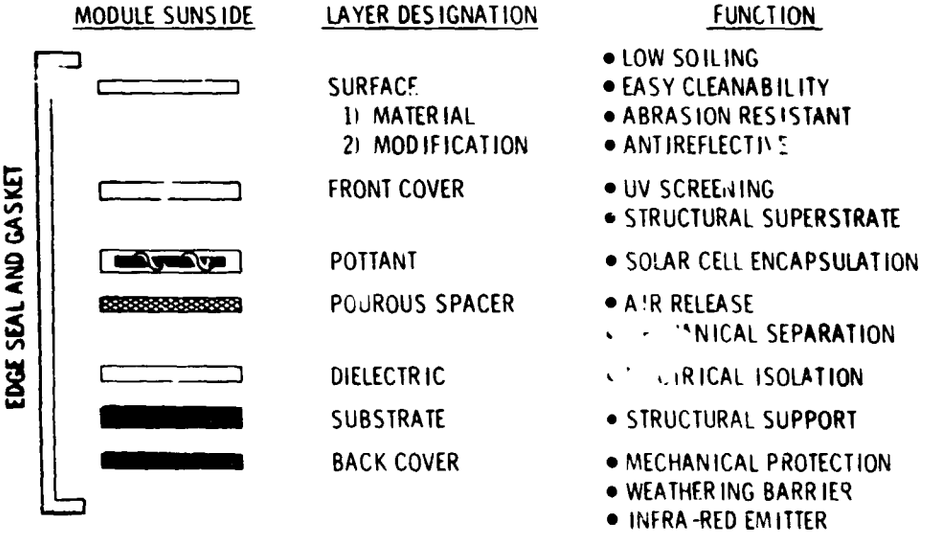
## Encapsulation Requirements

| | |
|---|---|
| • OUTDOOR LIFE | 30 YEARS |
| • OPTICAL TRANSMISSION TO SOLAR CELLS | >90% OF INCIDENT |
| • LOSS IN MODULE POWER AFTER 30 YEARS | <10% OF INITIAL |
| • PROCESSING AND FABRICATION | AUTOMATED |
| • STRUCTURAL PERFORMANCE (INCLUDING HANDLING AND WEATHERING) | NO FAILURES |

## Encapsulation Design Classifications




## Encapsulation Materials: Module Construction Elements




PLUS NECESSARY PRIMERS/ADHESIVES

## Transparent Encapsulation Pottants

1. WEATHERING ACTIONS
   a. UV REACTIONS
   b. THERMAL OXIDATION
   c. HYDROLYSIS

2. COST/WEATHERING RELATIONSHIP

| MATERIAL COST | WEATHERING ACTIONS |
|---|---|
| 25¢ TO 65¢/LB | a, b, c |
| 65¢ TO $1.00/LB | a (RESISTANCE TO b AND c, UP TO 80°C) |
| > $1.00/LB | NONE |

3. CANDIDATE POTTANT MATERIALS
   a. LAMINATION FILMS
      ETHYLENE VINYL ACETATE (95¢/LB)
      ETHYLENE METHYL ACRYLATE (95¢/LB)
   b. CASTING LIQUIDS
      POLY-N-BUTYL ACRYLATE (85¢/LB)
      ALIPHATIC POLYETHER URETHANE (≈ $3.00/LB)

## Pottants: Evolving Specifications and Requirements

- GLASS TRANSITION TEMPERATURE < -40°C
- MECHANICAL CREEP RESISTANCE AT 90°C
- TENSILE MODULUS ≤ 3000 LB/IN.$^2$ AT 25°C
- OPTICAL TRANSMISSION (0.4 TO 1.1 μm), > 90%
- THERMAL OXIDATION RESISTANCE AT 80°C
- HYDROLYSIS RESISTANCE AT 80°C
- UV REACTION SENSITIVITY < 350 nm
- CHEMICAL INERTNESS AT 80°C (COPPER, NICKEL, SOLDER, ETC.)
- WATER ABSORPTION < 0.5 WT % AT 20°C/100% RH

## Front Covers for Substrate Designs: UV Screening Plastic Films

| MATERIAL | COMMERCIAL COST | STATUS |
|---|---|---|
| 1. ACRYLIC | | |
| a. ACRYLAR X-22416, 2 MILS | $\approx 4.8¢/FT^2$ | AVAILABLE, 3M |
| b. ACRYLAR X-22417, 3 MILS | $\approx 6.7¢/FT^2$ | |
| 2. FLUOROCARBON | | |
| a. TEDLAR 100 BG 30 UT, 1 MIL | $\approx 7¢/FT^2$ | AVAILABLE, DU PONT |
| b. TEDLAR 400 BG 20 SE, 4 MILS | $\approx 30¢/FT^2$ | |

## Other Candidate Encapsulation Materials

**1. Structural panels**
- **a. Tempered, low-iron, soda lime float glass ($\approx 75$ ¢/ft$^2$, 1/8 in. thick)**
- **b. Cold-rolled mild steel ($\approx 0.8$ ¢/ft$^2$ · mil, 8-mils minimum rqmt)**
- **c. Wood hardboards ($\approx 13$ ¢/ft$^2$, 1/8 in. thick)**

**2. Back covers (white-pigmented plastic films)**
- **a. Tedlar 150 BL 30 WH, 1.5 mils thick (Du Pont)**
- **b. Tedlar 400 BS 20 WH, 4.0 mils thick (Du Pont)**
- **c. Scotchpar 10 CP White, 1.0 mils thick (3M Co.)**
- **d. Scotchpar 20 CP White, 2.0 mils thick (3M Co.)**
- **e. Korad 63000 White, 3.0 mils thick (Xcel Corp.)**

**3. Edge seal and gasket**
- **a. But, edge sealing tape (5354, 3M)**
- **b. EPDM gasket material (E-633, Pauling Rubber Co., Pauling, NY)**

**4. Porous spacer**
- **a. Craneglas non-woven E-Glass mats, Type 230**

## Encapsulation Primers and Adhesives

PRIMERS

3) ELASTOMERS TO PLASTIC FILM SURFACES

| COMPONENT | COMPOSITION |
|---|---|
| Z-6030 SILANE (DOW CORNING) | 1 WT. % |
| Z-6040 SILANE (DOW CORNING) | 1 WT. % |
| RESIMENE 740 (MONSANTO) | 8 WT. % |
| ISOPROPYL ALCOHOL | 90 WT. % |

ADHESIVES

1) TEDLAR TO EVA/EMA, DU PONT ADHESIVE 68040

2) SCOTCHPAR TO WOOD, 3M ADHESIVE 4910

## Adhesive Bond Strengths for EVA Bonded to Glass

| | | BOND STRENGTHS, LB/IN. OF WIDTH | | |
|---|---|---|---|---|
| MATERIALS | PEROXIDE | CONTROL | 2 WK IMMERSION | 2 HOURS BOILING WATER |
| SUNADEX GLASS | L-101 | 34.8 | 30.0 | 32.3 |
| WINDOW GLASS | L-101 | 39.6 | 37.9 | 27.1 |
| WINDOW GLASS (SELF-PRIMING EVA) | L-101 | 35.4 | 41.9 | COHESIVE |
| SUNADEX GLASS | L-TBEC | 51.3 | 32.9 | 33.3 |

## Adhesion Experiment Using TBEC-Cured EVA Mechanical Test Specimens Filled With 30% by Volume Glass Beads

| EFFECT OF HYDROLYTIC AGING IN WATER AT 85°C | | | | | | |
|---|---|---|---|---|---|---|
| SAMPLE AND PROPERTIES | IMMERSION TIME | | | | | |
| | CONTROL | 24 HRS | 96 HRS | 192 HRS | 360 HRS | 528 HRS |
| UNFILLED EVA | | | | | | |
| ELONGATION | 575% | 563 | 565 | 560 | 580 | 540 |
| TENSILE | 3,630 psi | 2,259 | 2,709 | 2,577 | 2,660 | 2,460 |
| MODULUS | 755 psi | 1,000 | 1,040 | 801 | 874 | 729 |
| FILLED EVA | | | | | | |
| ELONGATION | 262% | 270 | 280 | 190 | 205 | 120 |
| TENSILE | 980 psi | 1,119 | 1,160 | 847 | 1,028 | 1,333 |
| MODULUS | 1,800 psi | 1,900 | 2,200 | 610 | 1,900 | 2,800 |

## Electrical Insulation: ac and dc Intrinsic Dielectric Strength

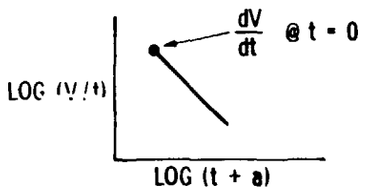
AC

- DATA CORRELATION

$$V_A = (V/t) = K(t + a)^{-n}$$

- AC INTRINSIC DIELECTRIC STRENGTH

$$(dV/dt) = K(a)^{-n}$$



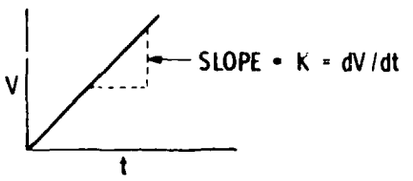

DC

- DATA CORRELATION

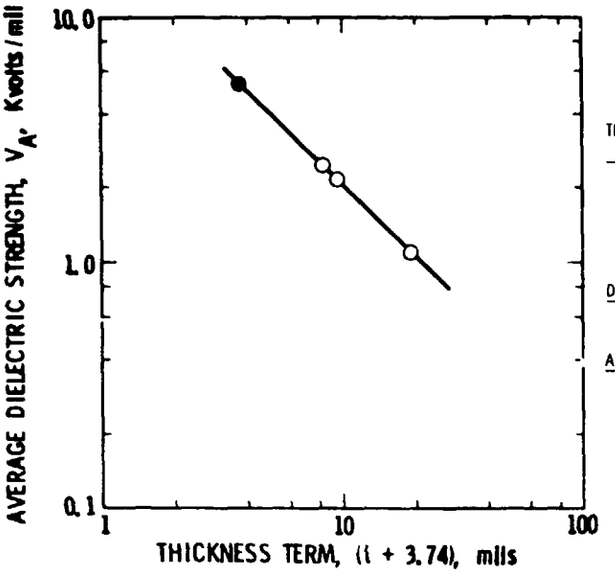
$$V = Kt$$

- DC INTRINSIC DIELECTRIC STRENGTH

$$(dV/dt) = (V/t) = K$$



## Ac Dielectric Strength of A-9918 EVA




| THICKNESS t, mils | AC BREAKDOWN VOLTAGE, KV | AVERAGE DIELECTRIC STRENGTH, $V_A$ = V/t, KV/mil |
|---|---|---|
| 4.7 | 11.7 | 2.49 |
| 6.0 | 13.0 | 2.17 |
| 15.7 | 17.6 | 1.12 |

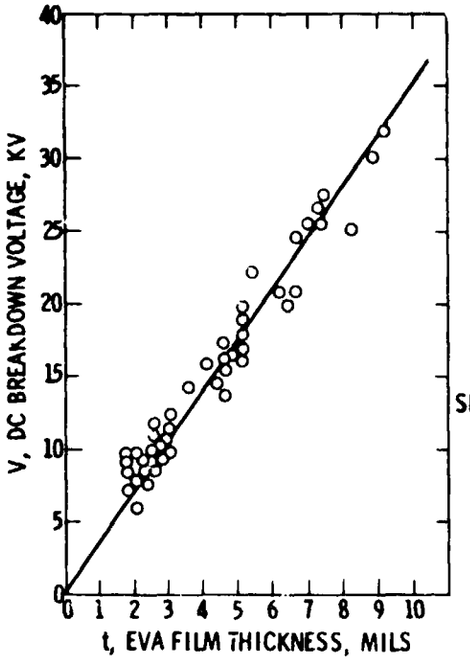
DATA CORRELATION

$V_A = 19173\,(t + 3.74)^{-0.96}$

AC INTRINSIC DIELECTRIC STRENGTH

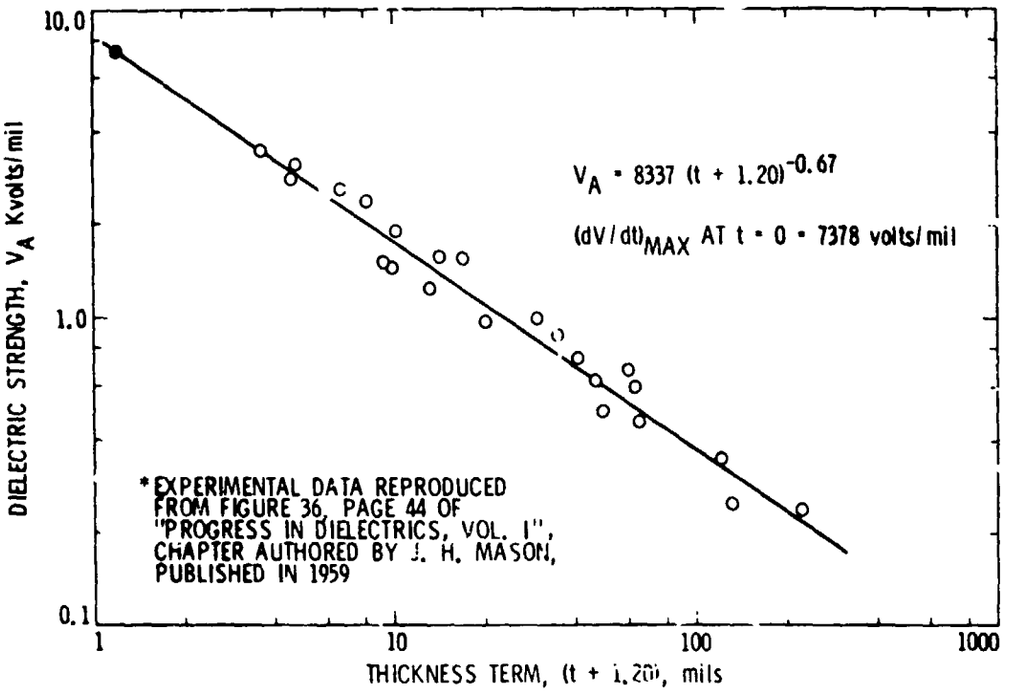
$\left(\frac{dV}{dt}\right)$ = 5404 VOLTS/MIL @ t = 0

## Dc Dielectric Strength of A-9918 EVA

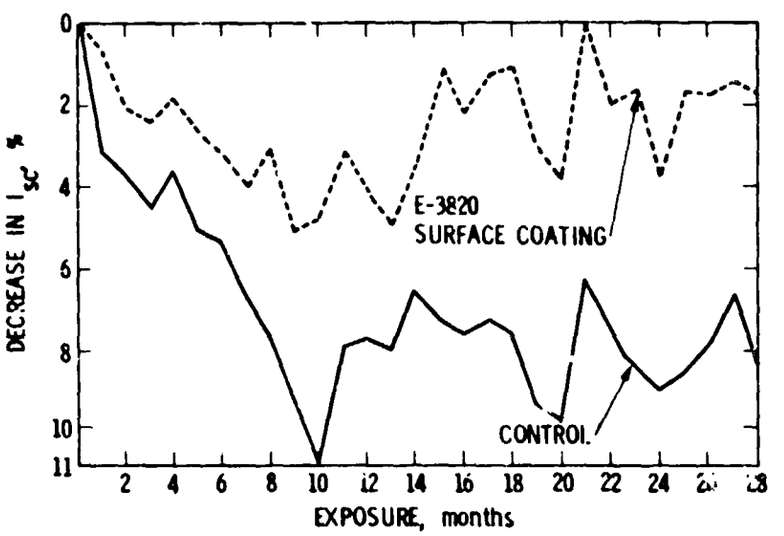



SLOPE = dV/dt = 3650 VOLTS/MIL

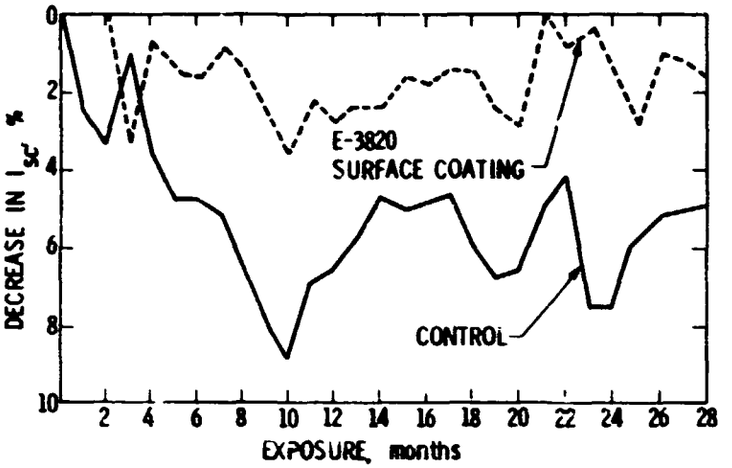
## Dielectric Strength of Polyethylene*



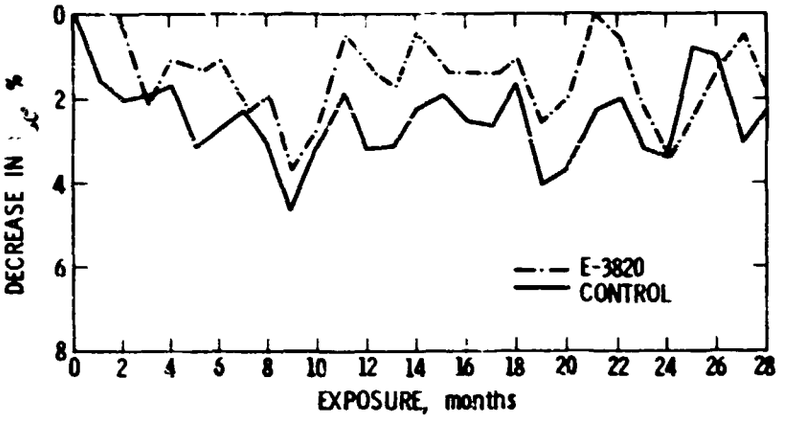

## Outdoor Soiling Behavior of Acrylar X-22417 Plastic Film With & Without Fluorocarbon Antisoiling Coating



Outdoor Soiling Behavior of Tedlar 100BG30UT Plastic Film With & Without Fluorocarbon Antisoiling Coating



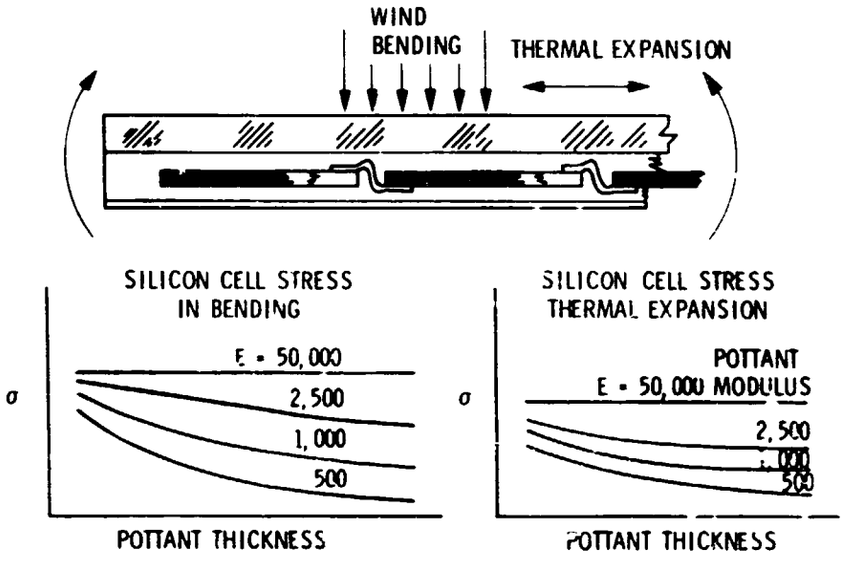

Outdoor Soiling Behavior of Glass With & Without Fluorocarbon Antisoiling Coating



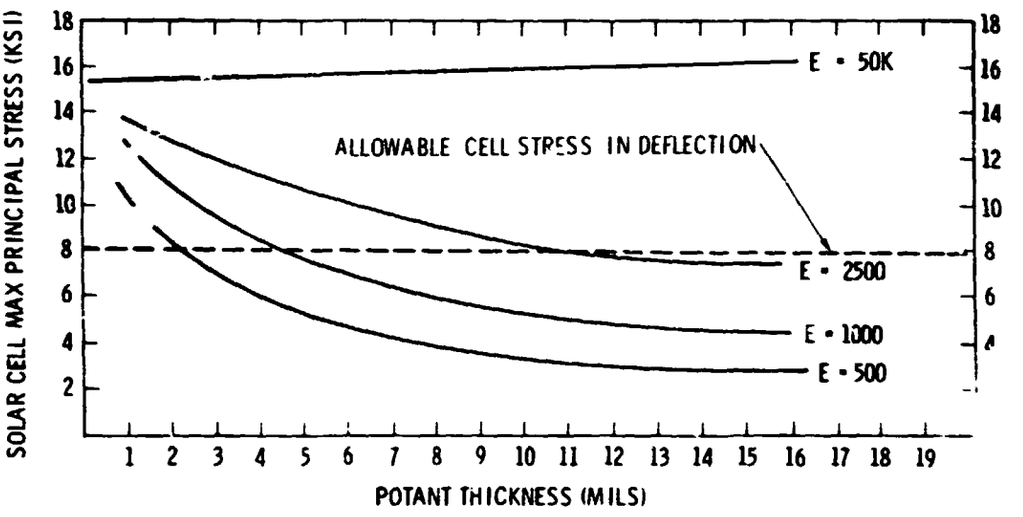
## Time-Averaged Optical Losses After 28 Months of Outdoor Soiling in Enfield, CT

| MATERIALS | TIME-AVERAGED OPTICAL LOSSES, % |
|---|---|
| GLASS | |
| CONTROL | 2.65 |
| WITH E-3820 | 1.55 |
| WITH L-1668 | 1.59 |
| TEDLAR | |
| CONTROL | 5.38 |
| WITH E-3820 | 1.70 |
| WITH L-1668 | 4.43 |
| ACRYLAR | |
| CONTROL | 7.20 |
| WITH E-3820 | 2.59 |
| WITH L-1668 | 4.21 |

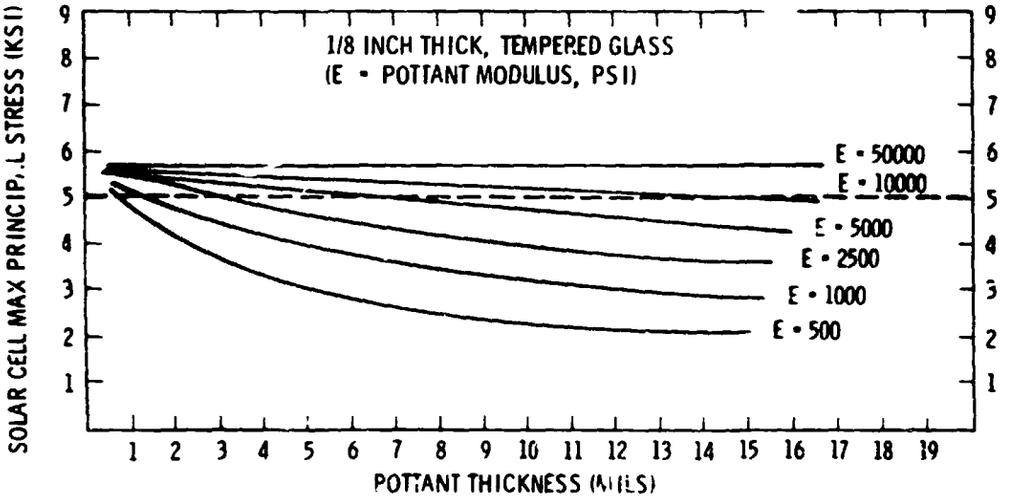
## Encapsulant Design Analysis



## Deflection Analysis: Glass Superstrate Design

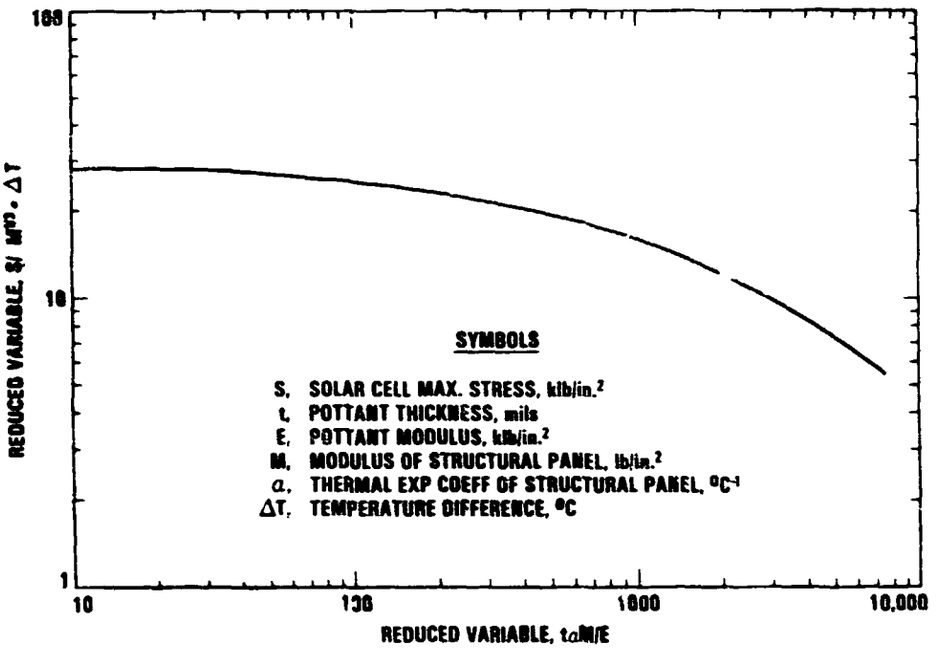



## Thermal Stress Analysis ($\Delta T = 100°C$): Glass Superstrate Design




DOTTED LINE - ALLOWABLE CELL STRESS IN TENSION

## Master Curve for Thermal Stress Analysis



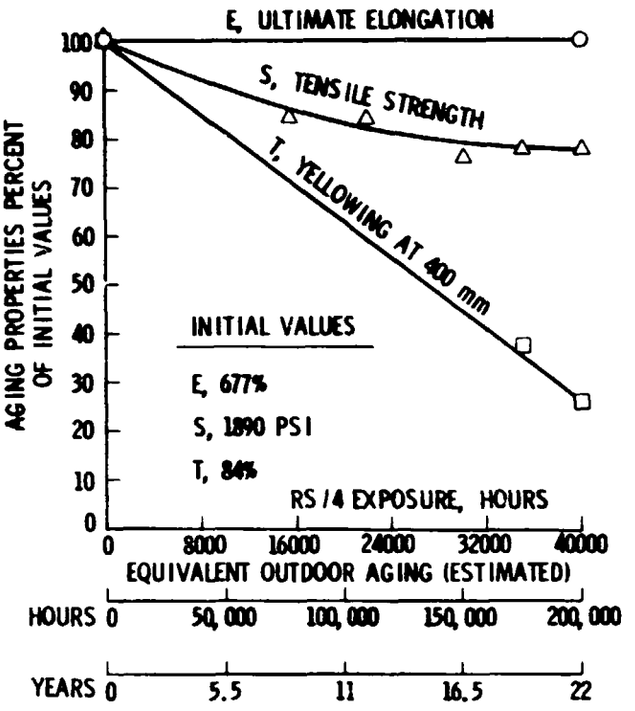

## Life Assessment Program

1. DEVELOP PREDICTIVE AGING MODELS
   a. CONNECT CHANGE AND RATES-OF-CHANGE IN ENCAPSULATION MATERIAL PROPERTIES TO MODULE PERFORMANCE AND LIFE

2. ACCELERATED AGING METHODS
   a. AIR OVENS
   b. RS/4 SUN LAMPS (1.4 SUNS UV INTENSITY AT 50°C AND 85°C)
   c. CONTROLLED-ENVIRONMENTAL REACTORS (6 SUNS UV INTENSITY, ADJUSTABLE SAMPLE TEMPERATURE AND WATER-SPRAY CYCLE)
   d. OUTDOOR HEATED AGING RACKS (EXPOSURE OF MATERIALS AND MODULES TO NATURAL AGING ENVIRONMENT AT ADJUSTABLE ELEVATED TEMPERATURES)

3. MATERIAL TECHNOLOGIES
   a. CHEMICALLY ATTACHABLE UV ABSORBERS
   b. CHEMICALLY IN-SITU UV ABSORBERS
   c. POLYMERIC UV ABSORBERS

Aging of A-9918 EVA in RS/4 Sun Chambers at 50°C



# Summary of EVA Aging at 50°C
## EXPERIMENTAL

| WEATHERING ADDITIVES | UV-SCREENING FILM OVERLAY | AGING REMARKS |
|---|---|---|
| NO | NO | YELLOWED AND DEGRADED WITHIN 1000 HOURS |
| NO | YES | NO YELLOWING OR DEGRADATION UP TO 20,000 HOURS |
| YES | NO | NO DEGRADATION, BUT GRADUAL YELLOWING UP TO 40,000 HOURS |

### FINDINGS

1) EVA APPEARS NOT TO UNDERGO THERMAL OXIDATION AT TEMPERATURES UP TO $50^{0}$C

2) EVA DOES UNDERGO PHOTO-OXIDATION

### CONCLUSION

LIFE OF EVA POTTANT IN OUTDOOR SERVICE AT $50^{0}$C (OR LESS) RELATED TO PERMANENCE OF THE MODULE'S UV PROTECTION SYSTEM

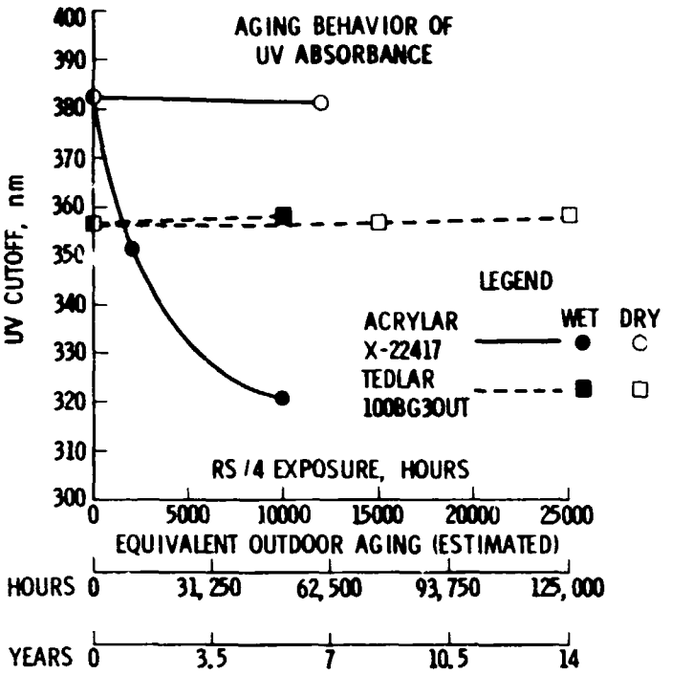
## Limitations Identified for the Current Version of A-9918 EVA

| MATERIALS | PROBLEM | CORRECTION |
|---|---|---|
| 1) PEROXIDE CURING AGENT<br>a) LUPERSOL 101 | • EVA IMMISICIBILITY<br>• RAPID PHYSICAL LOSS<br>• POOR STORAGE LIFE<br>• EVA CURE PROBLEMS | REPLACE WITH LUPERSOL TBEC; IMPROVED BLENDING, STORAGE, CURE |
| 2) WEATHERING STABILIZERS<br>a) TINUVIN 770<br>b) CYASORB UV-531 | • LOW MOLECULAR WEIGHT<br>• RAPID PHYSICAL DEPLETION<br>• GRADUAL LOSS OF EVA WEATHERING PROTECTION | REPLACE WITH NON-FUGITIVE WEATHERING STABILIZERS |

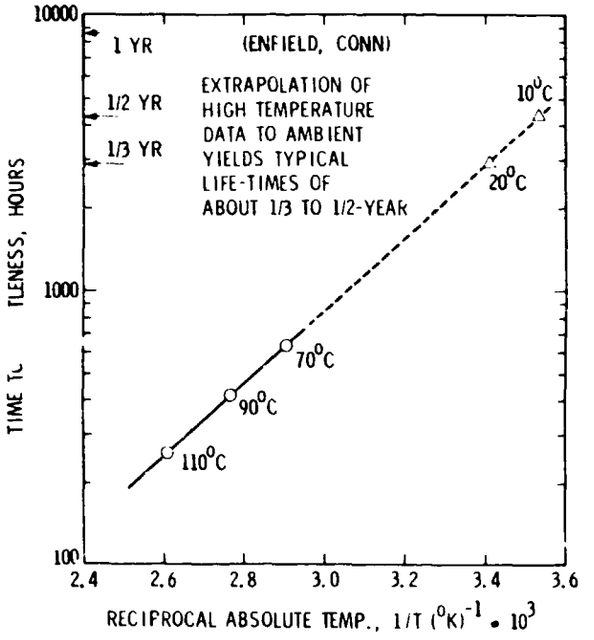
## Advanced EVA Formulation (Experimental): Springborn No. 18170

| COMPONENT | FUNCTION | REMARK |
|---|---|---|
| • ELVAX 150 | EVA RESIN | SAME AS A-9918 |
| • TBEC | CURING AGENT | FASTER, LOWER TEMPERATURE CURING, IMPROVED STORAGE LIFE |
| • UV-2098 | UV-SCREEN | CHEMICALLY ATTACHABLE, NON-FUGITIVE |
| • UV-3346 | HINDERED AMINE LIGHT STABILIZER (HALS) | POLYMERIC, NON-FUGITIVE |

Aging of Commercial UV Screening Films in RS/4 Sun Chambers at 50°C




Natural Outdoor Aging of Polypropylene on the Outdoor Heating Racks at 70°C, 90°C and 110°C



## Accelerated Aging Program: Quantifiable Aging Properties

| PROPERTY | MEASURABLE |
|---|---|
| 1) OPTICAL | • UV, VISIBLE, IR SPECTRA<br>• % TRANSMISSION AT 400 nm |
| 2) MECHANICAL | • MODULUS, STRENGTH, ELONGATION |
| 3) ELECTRICAL | • DC INTRINSIC DIELECTRIC STRENGTH |
| 4) CHEMICAL | • ADDITIVE CONCENTRATIONS<br>• RESIN CHEMISTRY/COMPOSITION |
| 5) ADHESION | • INTERFACE FTIR SPECTROSCOPY<br>• MECHANICAL PROPERTIES OF GLASS-BEAD FILLED SPECIMENS |

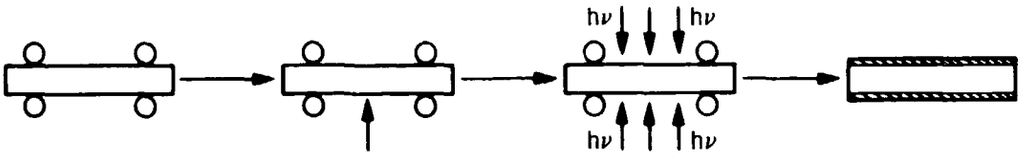
## New Concepts for Thin-Film Silicon Cell Encapsulation

- DEVELOPMENT OF CONFORMAL POLYMERIC LAYERS ON THIN FILM SILICON CELLS USING PHOTOPOLYMERIZATION TECHNIQUES
  - WHAT IS PHOTOPOLYMERIZATION?
    - MONOMER + CATALYST $\xrightarrow{h\nu}$ POLYMER
  - ADVANTAGES
    - ROOM TEMPERATURE PROCESSING
    - EXTREMELY RAPID PROCESSING (1 - 10 sec)
    - CAN HANDLE VINYLS, ACRYLICS, SILICONES, SILICONE-ACRYLICS, FLUOROPOLYMERS, EPOXIES, URETHANES, POLYESTERS – A WIDE VARIETY OF POLYMERS
    - IN SITU PROCESSING CAN LEAD TO ENCAPSULATION IN ONE STEP

## Current Industrial Applications of Photopolymerization

- ENCAPSULATION OF OPTICAL FIBERS
- DEPOSITION OF RESIST FILM ON MICROCIRCUITS

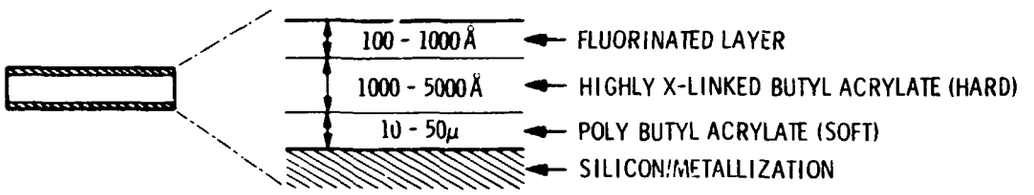
## Example of an Encapsulation Scheme Using Photopolymerization




ADD: n-BUTYL ACRYLATE + A TO COAT MODULE

A: $CF_3(CF_2)_9COON\left[(CH_2)_3COOC(CH_3)=CH_2\right]_2$

A: PERFLUORINATED ACRYLIC X LINKING AGENT (HIGH $T_g$) – IMMISCIBLE WITH NBA




## Potential Reliability Issues

- EFFECT OF STABILIZING ADDITIVES ON THE PHOTOPOLYMERIZATION PROCESSING CONDITIONS
- LONG TERM STABILITY OF THE COATING AND INTERFACES – EFFECTIVENESS OF ADDITIVES IN ULTRATHIN LAYERS
- ROLE OF THE SURFACE FLUORINATED LAYER AS AN OXIDATION INHIBITOR
- ANTISOILING CHARACTERISTICS OF THE SURFACE LAYER

RELIABILITY AND ENGINEERING OF THIN-FILM PHOTOVOLTAIC MODULES

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