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Thin-Film Module Circuit Design - Practical and Reliability Aspects*

R.V. D'Aiello and E.N. Twesme
Solarex Thin Film Division
Newtown, PA

ABSTRACT

This paper will address several aspects of the design and construction of submodules based on thin-film amorphous silicon (a-Si) p i n solar cells. Starting from presently attainable single cell characteristics, and a realistic set of specifications, practical module designs will be discussed from the viewpoints of efficient designs, the fabrication requirements, and reliability concerns. The examples will center mostly on series interconnected modules of the superstrate type with detailed discussions of each portion of the structure in relation to its influence on module efficiency. Emphasis will be placed on engineering topics such as: area coverage, optimal geometries, and cost and reliability. Practical constraints on achieving optimal designs, along with some examples of potential pitfalls in the manufacture and subsequent performance of a-Si modules will be discussed.

I. INTRODUCTION

A major advantage of thin-film solar cell technology is the ability to deposit the active film over large areas in a single process step. Practical considerations, however, require that the photovoltaic area be divided and individual cells be interconnected so as to provide specified voltages and currents. For amorphous silicon and several other thin-film devices which are deposited on a transparent conductive surface, the series connected monolithic module has evolved as a convenient and efficient structure to accomplish this division to form practical circuits. Indeed, a-Si modules of this type are now commercially sold in solar powered calculators and battery chargers. This structure is comprised of a number of side-by-side rectangular shaped cells connected electrically in series on a single glass substrate. The interconnection is accomplished by a sequential patterning and deposition of the various films comprising the vertical cell structure. Since the resultant structure is essentially one dimensional, relatively simple design rules can to first order be derived and applied. However, practical structural and circuit requirements force the consideration of two dimensional effects; in addition, limitations of the patterning process, interactions of these processes with film properties, and the necessary junction of dissimilar materials can affect both the module design and its ultimate performance and reliability. Such considerations for a-Si solar cell modules are the subject of this paper.

II. SINGLE CELL CHARACTERISTICS

In order to design modules for specified electrical performance (voltage, current, power) individual cell IV characteristics should be examined to extract average cell parameters to be used in the design calculations. For a-Si cells of the p i n structure deposited on a transparent superstrate, the I/V curves and parameters shown in Figure 1 are typical of the range that can be obtained

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with present technologies. Several features should be noted when comparing these to the parameters of single crystal silicon (C-Si) cells. First, generated photocurrent is about 1/3 to 1/2 that of C-Si cells, open circuit voltage is about 300mV higher, and the fill-factor is generally lower with a "soft" I/V curve characterized by a somewhat low equivalent shunt resistance as shown in Figure 1(b). The high V_{oc} is a distinct advantage for series interconnection, but the lower generated current implies larger area to achieve a given power output. The "softer" shunt-like I/V characteristics while reducing the maximum power available, may have some advantage for hot-spot tolerance. Parameters close to those of Figure 1(b) will be used in the example presented below.

III. STRUCTURE AND DESIGN EXAMPLE OF SERIES INTERCONNECTED a-Si MODULE

The cross sectional structure of a monolithic series connected module including bus contacts is shown in Figure 2. The deposition and patterning steps typically used to fabricate this structure are shown in Figure 3. The deposition of the various films will not be discussed here, but the choice of processing method and geometry of the patterning are important to the design considerations. Several methods are available to accomplish the patterning such as screen-print masking followed by wet or dry etch, mechanical scribing, and laser scribing. Laser patterning is desirable because of its speed, dimensional control, economy of area loss and absence of wet chemicals. Typical dimensions achievable with laser scribes are shown in Figure 4. For comparison, also shown in Figure 4, is a typical metal patterning made by a wet etch, which results in a tripling of the area loss.

An example of the design of a module suitable for charging 4 NiCd "D" cells with average available light equivalent to one half AM1 is shown in Figures 5 and 6. The results are given for both laser scribe (values in parenthesis) and wet etched metal patterns. The losses due to bus bars and edges (5.3% and 4.7%) are considerable in this example due to the small size of this modules. The physical size of these parts will not change substantially in large modules resulting in much lower fractional loss (about 6% for $1ft^2$ modules). Note that the shadow and ohmic losses are more than halved for the laser scribed case.

IV. PRACTICAL RELIABILITY CONCERNS FOR THIN-FILM MODULES

A number of potential reliability issues could arise both during the fabrication of thin-film modules and later on due to environmental stress or aging. These are listed in Table I.

TABLE I

RELIABILITY CONCERNS

PROCESS RELATED

Type	Cause (s)	Result
pin holes or stressed areas	dirt or impurities thin a-Si film at edges	shorted or shunted cells
segments shorted together	missing laser pulses defects in SnO_2 (Fig 7) poor etch or mask control	shorted cells (module)
parasitic elements	incomplete a-Si scribe (Fig 8) too complete a-Si scribe	low fill factor power loss

STRESS RELATED

Type	Probable Cause	Result
lateral conductive paths	ionic contamination across small dimensions	shorted segments
parasitic elements	loss of ohmic contacts	lower fill-factor
arc over	high voltage breakdown under bus extensions	shorted module
corrosion	liquid water or water vapor	loss of output
pin holes or blistered areas	stress relief, thermal expansion/contraction	loss of voltage

V. SUMMARY AND DISCUSSIONS

The series-connected monolithic circuit has shown to be a desirable configuration for fabricating practical thin-film solar-cell modules. It may be applied to a variety of thin-film technologies, and is already in commercial use with amorphous silicon. The design rules are quite simple with no apparent problems in scaling to large area modules.

In realizing design requirements, however, careful consideration must be given to the thin-film deposition and patterning technologies to be used in fabricating the module. In this paper, it was shown that nonuniform film depositions (edge effects), inefficient patterning and/or interactions between patterning steps can lead to large area losses, and can raise concerns over the immediate and future reliability of the module. Examination of presently available a-Si modules indicates that many of these areas are being addressed by allowing generous safety margins in area utillization, incorporating potentially more reliable substructures, and by encapsulating the modules with materials of known reliability. It is for these reasons that current commercial a-Si modules are generally only 5-6% efficient while 10-12% cells are being universally reported. As a-Si deposition technology matures, and advanced laser patterning techniques are used in production, module efficiency will increase even without futher improvement in cell performance. Laboratory and field testing should be used extensively to provide real-world experience, and the vast data already available from the testing of single crystal modules should be consulted to pinpoint potential trouble spots and to reduce time cycles for qualification of thin-film modules.

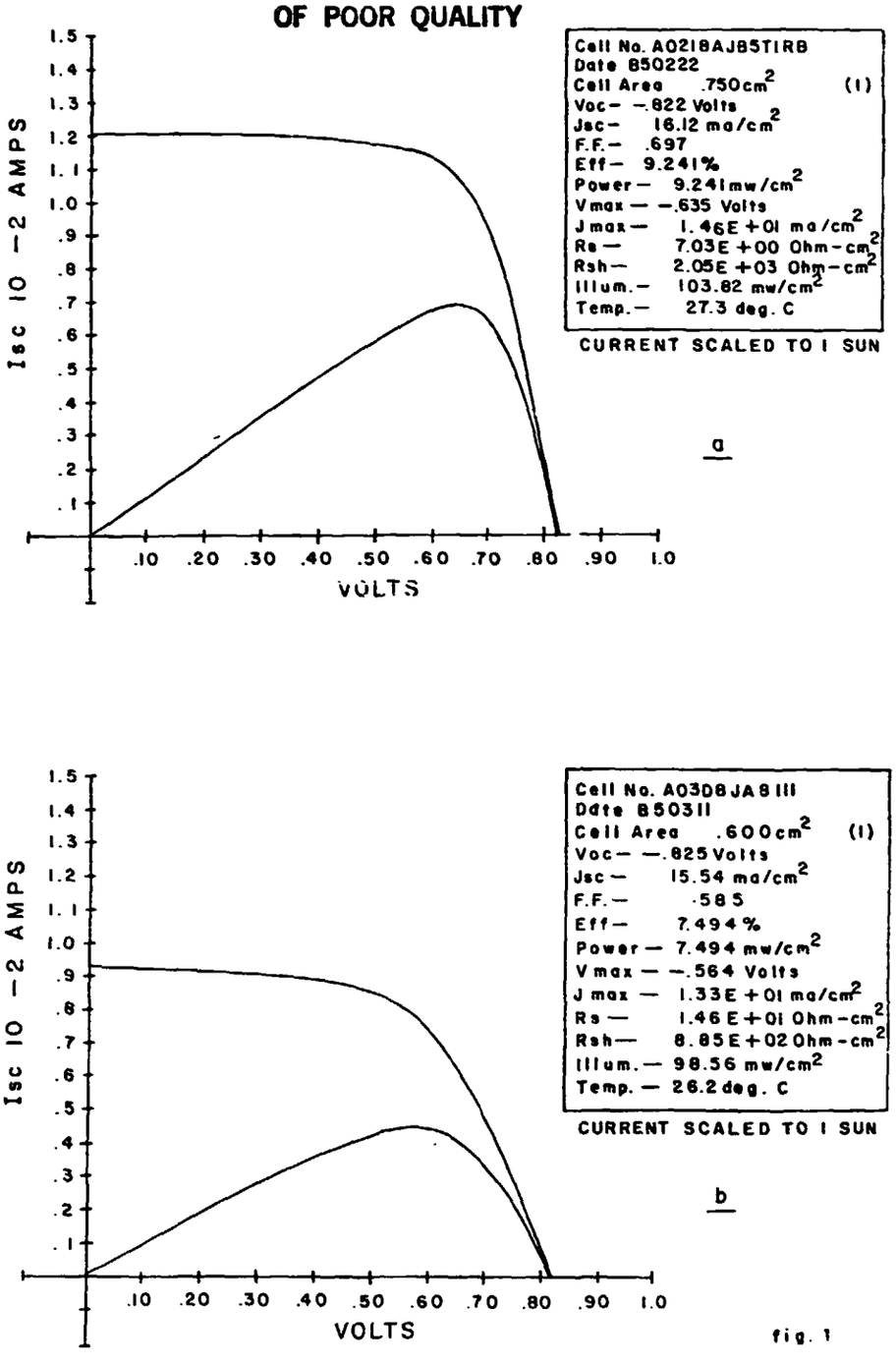


Figure 1

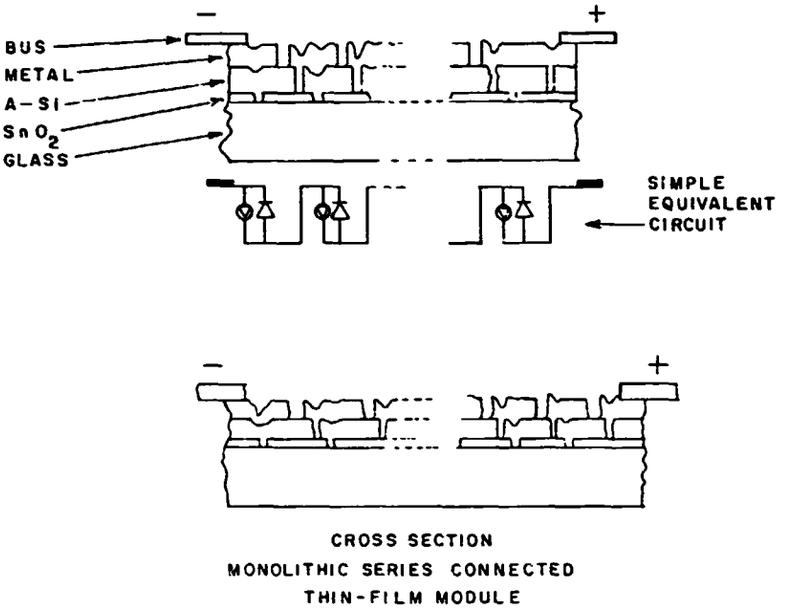


Figure 2

PROCESS STEPS

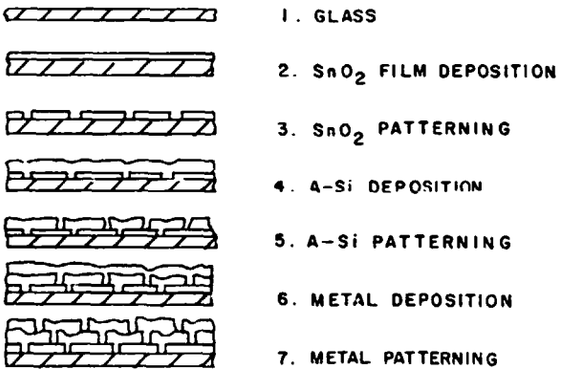
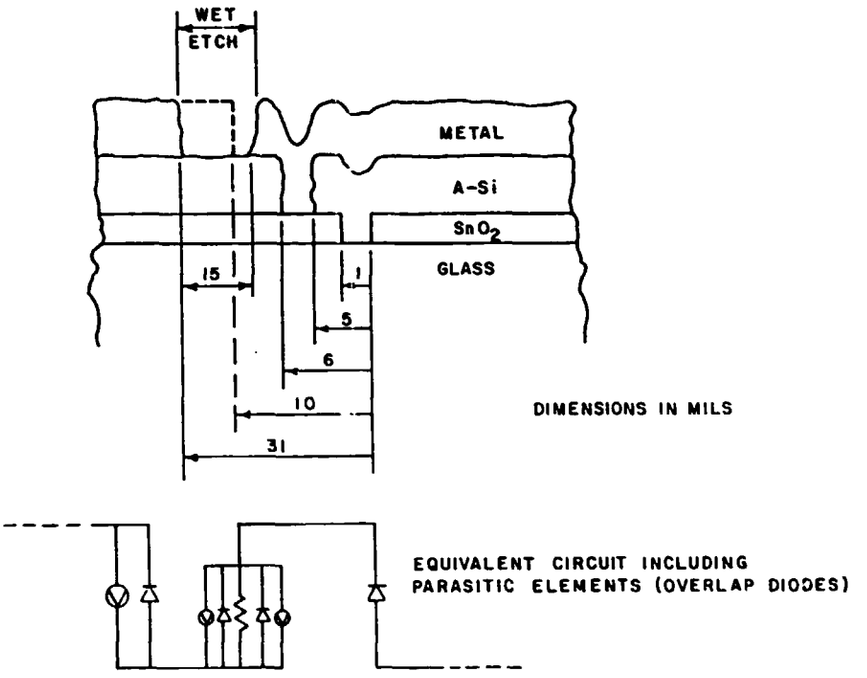


Figure 3



DETAILS OF INTERCONNECT REGION

Figure 4

EXAMPLE: DESIGN OF BATTERY CHARGER MODULE

SPECIFICATIONS: CHARGE 4 "D" CELLS (NiCD) @ 50mA @ 1/2 AM1

$V_M > 4 \times 1.4 = 5.6V$

$N = \frac{5.6}{0.6} = 9.3 =$ 10 SEGMENTS (MIGHT USE 11 FOR GOOD YIELD)

$J_M = 6mA/cm^2$ AT 1/2 AM1

$A = \frac{50}{6} = 8.4\ cm^2$

GEOMETRY $L \times W = 8.4cm^2$

$S_{LOSS} = \frac{1}{3} \frac{J}{V} R\ W^2 + \frac{D}{W}$

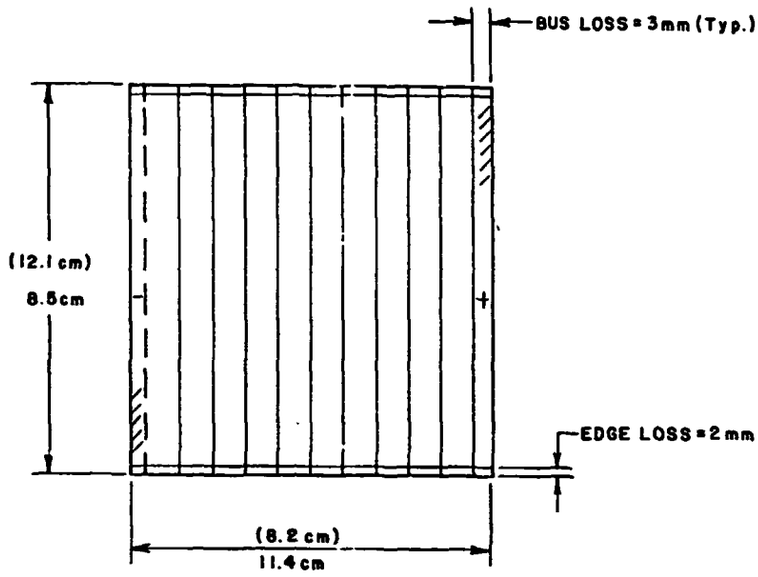
$W_{MIN} = \sqrt[3]{\frac{3DV}{2JR_\square}} = 1.04$ cm (.721cm) (LASER SCRIBED METAL)

$S_{LOSS} = 3.6 + 7.2 = 10.8\%$

$(1.7) + (3.4) = (5.1\%)$

$L = \frac{8.4}{1.04} = 8.1cm$ (11.7cm)

Figure 5



Area loss = 7.2% (shadow) + 5.3% (bus loss) + 4.7% (edge loss) = 17.2% (14.0%)
(3.4%) (7.3%) (3.3%)

Total loss = 17.2% + 3.6% = 20.8%
(14.0%) + (1.7%) = (15.7%)

10% cells ⇒ 8% (8.5%) modules

BATTERY CHARGER DESIGN

Figure 6

Figure 7

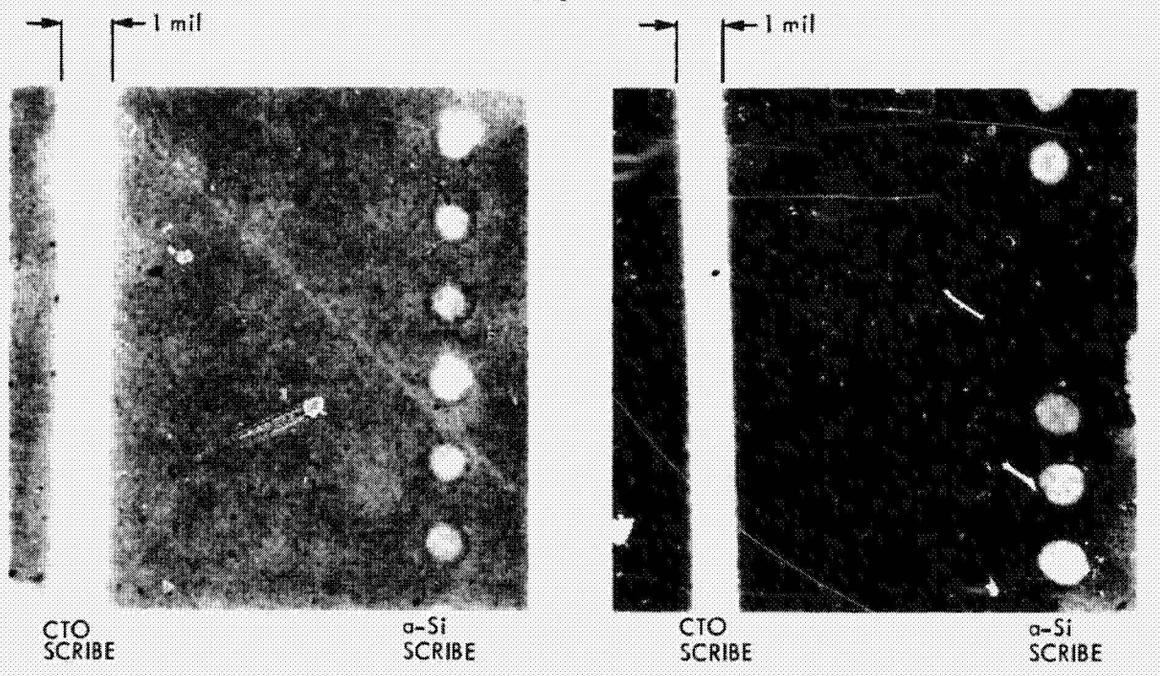


Figure 8

DISCUSSION

LESK: In the CTO laser scribe, do you actually go all the way and take a bit of the glass, or is it transparent to the last stage, intact?

D'AIELLO: It depends on how much power you use to do the scribe. You can take a bit of the glass away. If you go too far you will cause a deep cavern there, which must be covered by the silicon later, and it's a cause for concern. It is not usually a problem, though in practice --

LESK: If you take a little bit of the glass, you are trying to contact CTO on the edge, and you could get a little layer of glass covering it and have high contact resistance there.

D'AIELLO: That's correct.

YERKES: It looks in your diagram like we have quite a different situation in these designs with regard to paralleling diodes. I know you are not worried about big arrays at this point -- maybe you are -- but some of the things Ron Ross talked about earlier, it looks like this would make potential for either easier dioding or automatically incorporating some parallel leakage in here which could help in breakdown, or maybe hurt, I don't know. Do you have a comment on that?

D'AIELLO: It's a good point. Your imagination can run wild. My background is semiconductor devices, and I'm used to thinking of integrated circuits that I can wrap around these things. And there are many interesting parasitic elements that could be useful in this design, as an integrated monolithic design, that we can add to this. I have only covered the series-connected aspects. You could put some blocking or bypass diodes right on board the circuit. However, there are also some on-board short circuits that are built in that you have to be careful about. That tin oxide is all the way to the edge of the glass, usually, and is quite conductive, so that if it is not separated adequately from the active module you can short the module out. So there's both aspects to worry about.

DELAHOY: I would like to make a quick comment and then I'll ask a question. The fill factors you mentioned around 67%-70% are good and probably typical in production for those in the audience who are not aware of what fill factors can be attained with amorphous-silicon cells. We have seen fill factors as high as 76%. So the potential is there for getting fill factors on amorphous silicon modules almost as high as crystalline cells. As you probably know, the intrinsic contact resistance of aluminum deposited under high-vacuum conditions onto clean tin oxide is indeed very low. I wondered if you had any information regarding the long-term stability for the direct aluminum-to-tin-oxide contact that is commonly used in many modules?

D'AIELLO: Well, as I mentioned in the talk, you could easily imagine how that situation that you just described would not occur in practice. If you evaporate aluminum on clean tin oxide, I agree, you will more than likely form an ohmic contact with reasonably low contact resistivity. However, we are not doing that in practice; we're removing the silicon first with a high-power laser or perhaps some other means. And you might damage the tin oxide below, change its chemistry -- if it became oxygen-rich, for example, you could easily imagine how you might affect the formation of aluminum oxide. We have looked at that interface region but I am not at liberty to comment on what the results are.