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Introduction

This effort is a follow-on to that developed under NASA Contract NAS8-32634. In that work it was shown that the NASA/MSFC C-015 Devices are not sufficiently proton radiation resistant, and therefore are not suitable for prolonged space flight missions. It was recommended that various techniques be investigated which appear to have the potential for improving the radiation hardness of these devices. The three key recommended processing techniques for producing more radiation tolerant CMOS structures are

1) Making the gate oxide thin. It has been shown that radiation degredation is proportional to the cube of oxide thickness [1] so that a relatively small reduction in thickness can greatly improve radiation resistance.
2) Cleanliness and contamination control.
3) Investigate different oxide growth conditions (low temperature dry, TCE and HCL).

High quality clean oxides are more radiation tolerant [1-3]. Technique 2 addresses the reduction of metalic ion contamination. Technique 3 will produce a higher quality oxide by using slow growth rate conditions, and will minimize the effects of any residual sodium contamination through the introduction of hydrogen and chlorine into the oxide during growth.

Robert De Hayes / EB13

FINAL TECHNICAL REPORT

DEVELOPMENT OF A RADIATION-HARD CMOS PROCESS

BY

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HUNTSVILLE, ALABAMA

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Processing Plan

The processing steps involved in this effort followed the MSFC Complementary Metal Oxide Semiconductor (Including Multilevel Interconnect Metalization) Process Handbook as outlined in NASA Technical Memorandum 78188. The process employed deviated from the NASA process in the following manner. The gate oxide thickness was reduced from 1300Å to a Range of 800-900Å. The oxides were grown using (a) a dry oxide, (b) a HCL oxide and (c) a trichloroethylene oxide. In addition, the furnace tubes were carefully cleaned to insure that they were free from any contaminants, particularly sodium [3-5]. The cleanliness procedure involved removing all tubes from the furnace and cleaning them in nitric and hydroflouric acid solutions. Prior to each diffusion or oxidation process the tube was purged using a mixture of trichloroethylene and oxygen at 1100°C for ten to twenty four hours.

The processing steps employed are as follows: The starting material was an N-type silicon wafer phosphorous doped, 5-8 ohm-cm, <100> orientation. Seven wafers were employed for each run. Wafer numbers 1, 2, and 7 were test wafers, and wafer numbers 3, 4, 5, and 6 were device wafers. The initial cleaning process involved first a mechanical clean in which wafers are spun at 2000 RPM and scrubbed with cotton swab wet with methanol. The second cleaning step was a solvent clean in which the wafers are placed in boiling trichloroethylene for five minutes, then placed in boiling acetone for five minutes, then placed in boiling methanol for five minutes, and finally a dionized water rinse for five minutes.

The pre oxidation/diffusion cleaning process involves both an organic clean and a metallic ion clean. In the organic cleaning process the wafers are placed in a boiling (95°C) mixture consisting of 70% sulfuric acid and 30% hydrogen peroxide for a period of five minutes. They are then rinsed in DI water for one minute. The wafers are then dipped in a 10% HF solution for 30 seconds. They are then washed in DI water for five minutes.

In the metallic cleaning process the wafers are placed in a boiling (95°C) mixture consisting of equal parts of HCL, Hydrogen Peroxide, and DI water for a period of five minutes. They are then rinsed in DI water for one minute. The wafers are then dipped in a 10% HF solution for 30 seconds and finally washed in DI water for five minutes. Wafers are then blown dry with N_2.

Gate Oxide Process Development

Three types of oxide were grown to determine/define a process for producing an oxide as free from positive mobile ions as possible. They were: a dry oxide, an oxide grown in a trichloroethylene vapor to provide Cl ions to gather positive mobile ion, and an oxide grown in an HCL vapor.

The dry and TCE oxides were grown at 1000°C because of the slow growth rate at lower temperatures, the HCL oxide was grown at 900°C. In all cases the furnace was purged in a TCE-Oxygen vapor at 1100°C for 11 to 24 hours before the process run.

Dry Oxide Process

Furnace Temperature 1000°C

Slow Push wafers into furnace 5 minutes.

Gas	Time
N_2 - 1ℓ/min O_2 1ℓ/min	5 minutes
O_2 - 1ℓ/min	2 hours
N_2 - 1ℓ/min	15 minutes

Slow pull from furnace 5 minutes.

This schedule produced an oxide of ≃ 1075Å.

TCE Oxide Process

The TCE was introduced into the furnace by bubbling N_2 through liquid TCE in a quartz liquid source bubbler. TCE temperature maintained at 20°C. Ratio TCE vapor to oxygen 1:10.

Furnace Temperature 1100°C

Slow push wafers into furnace 5 minutes.

Gas	Time
N_2 1ℓ/min O_2 1ℓ/min	5 minutes
N_2 + TCE 100cc/min	1 hour
O_2 1ℓ/min	
N_2 1ℓ/min	15 minutes

Slow pull from furnace 5 minutes.

This schedule produced an oxide of ≃ 1050Å.

HCL Oxide Process

HCL vapor was introduced into the furnace by bubbling O_2 through a solution of HCL and DI water at a ratio of HCL to H_2O of 1:1. A 1 liter quartz water bubbler was used temperature maintained at 95°C.

Furnace Temperature 900°C

Slow push wafers into furnace 5 minutes.

Gas	Time
N_2/O_2 - 1ℓ/min	5 minutes (push in)
O_2 - 1ℓ/min	10 minutes
O_2 + HCl - 1ℓ/min	60 minutes
N_2 1ℓ/min	20 minutes

(Furnace Temperature increased to 1050°C)

Slow pull from furnace 5 minutes (N_2).

Oxide Test - CV Plot

All oxides were etched in BOE at 20°C to approximately 900Å and an aluminum film was deposited on the wafers 7500Å thick.

A standard photolithagraphy was used to pattern the aluminum with dots, each dot has an area of 100 circular mils. The pattern is a grid with the dots spaced 50 mils apart. A measurement of the capacitor formed by the Al-oxide dielectric-silicon indicates the thickness of the oxide.

CV Plots were made with a bias sweep from -5V to +5V and a stress of +10V, with wafers heated to 300°C.

	Thickness	Cap	Shift
Dry oxide	856Å	26 pf	0.53V
TCE	891Å	25 pf	0.14V
HCL	909Å	24.5 pf	0.03V

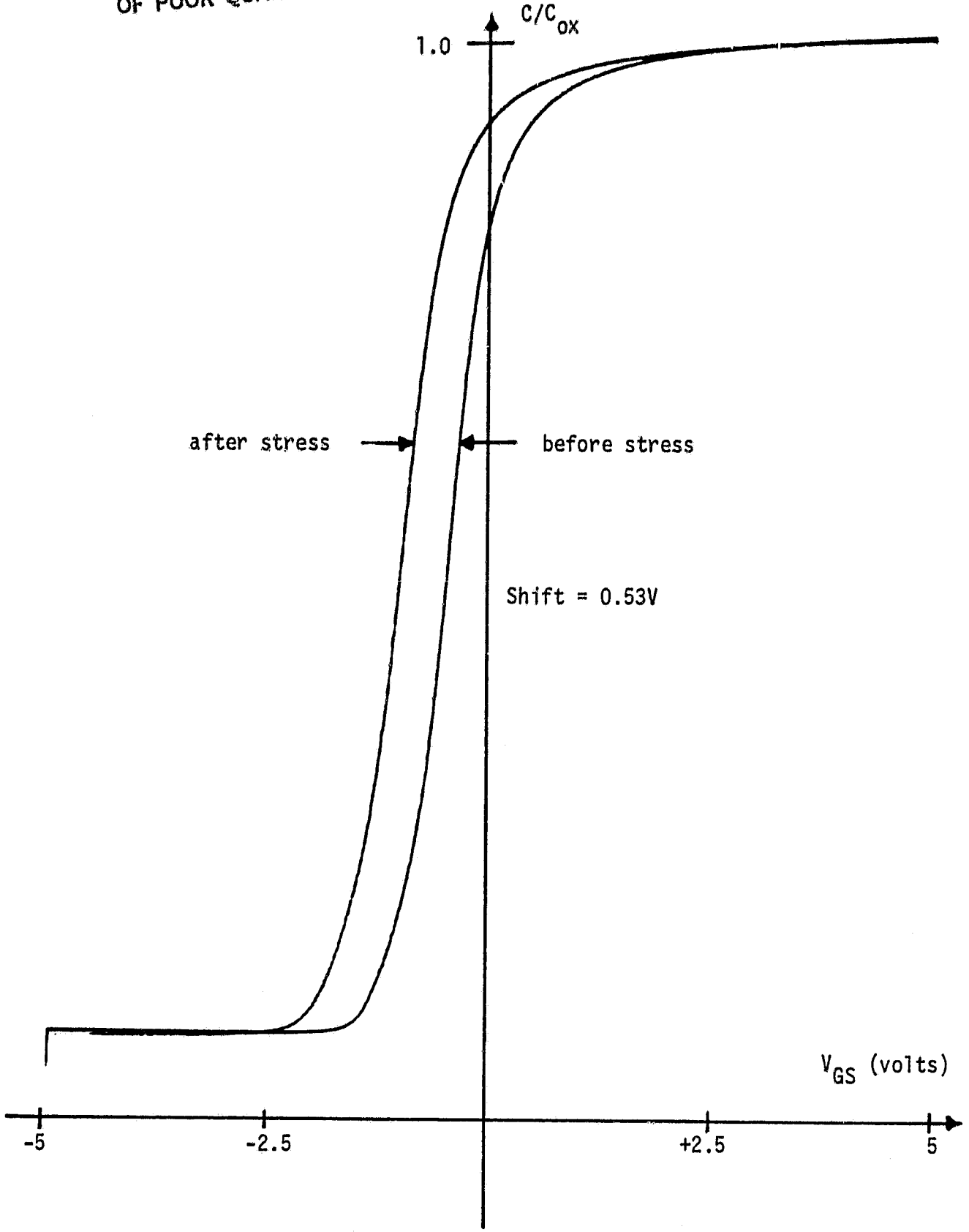


Figure 1. Dry Oxide C-V Characteristic T_{ox} = 856Å C_{ox} = 26 pF.

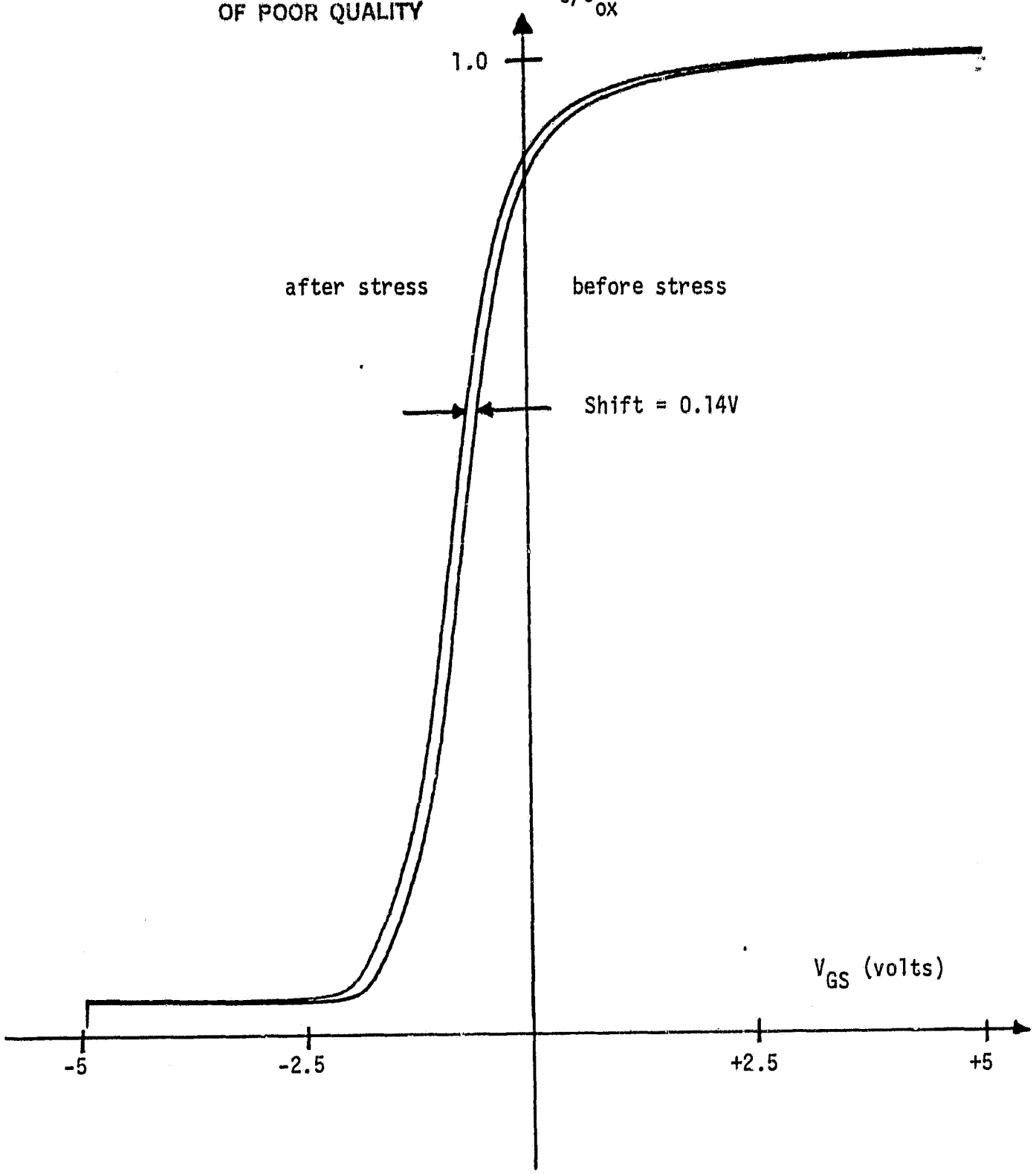


Figure 2. TCE Oxide C-V Charateristic T_{ox} = 891Å C_{ox} = 25 pF.

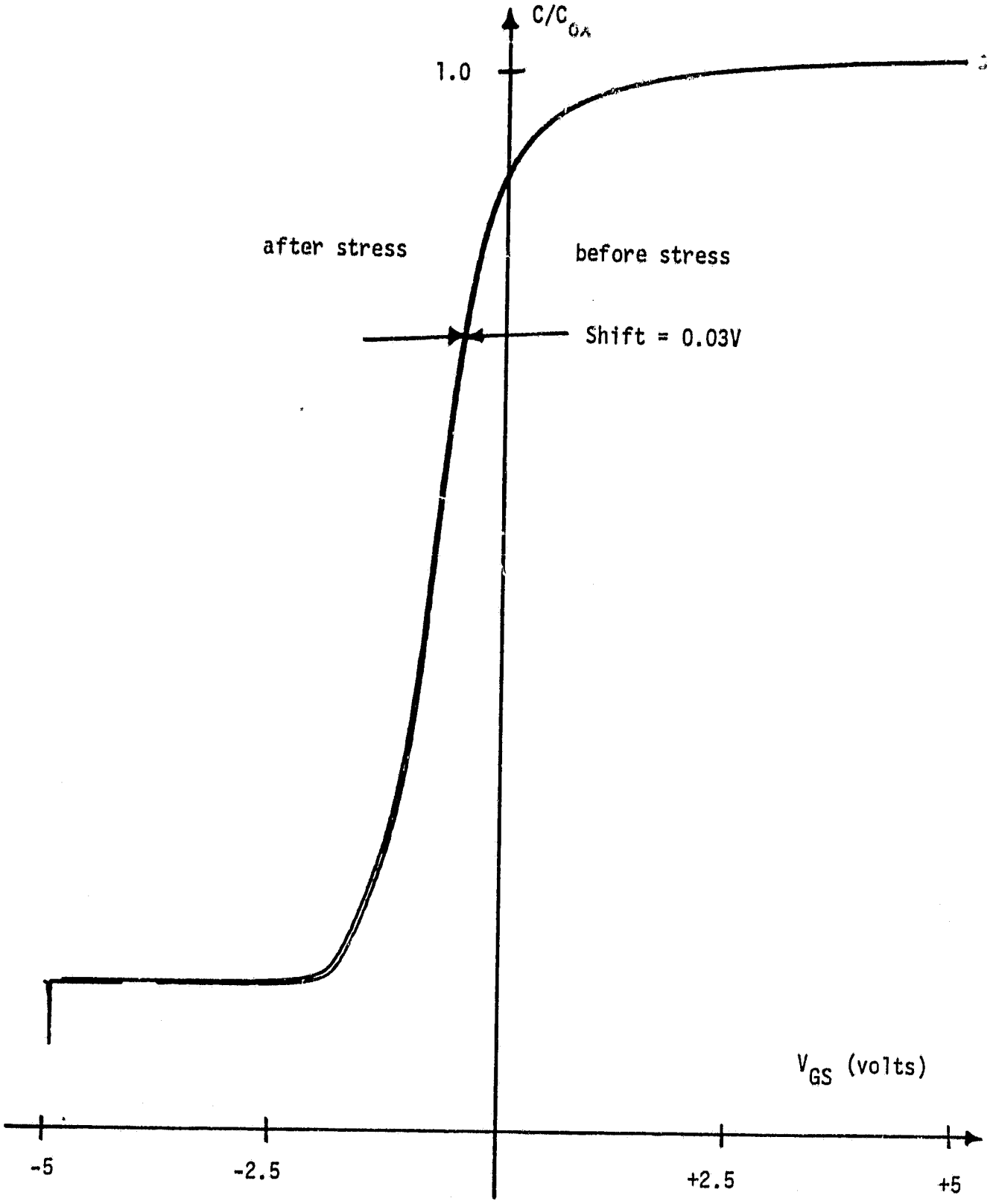


Figure 3. ACL Oxide C-V Characteristic T_{ox} = 909Å C_{ox} = 24.5 pF.

Typical CMOS Process

I. First Oxide

Wafers 1 through 7

1. Initial Clean
2. Pre-oxidation clean
3. Oxidation - Furnace Temperature 1150°C

Slow push wafers 1 through 6 into furnace.

Gas	Time
N_2 1ℓ/min	5 minutes
O_2 1ℓ/min	5 minutes
O_2+H_2O(95°C) 1ℓmin	50 minutes
O_2 1ℓ/min	5 minutes
N_2 1ℓ/min	20 minutes
Slow pull from furnace	
N_2 1ℓ/min	5 minutes

Oxide was blue-green color indicating approximately 6000Å thickness. Wafers 1 and 2 were etched in buffered oxide etch until all oxide was removed. Temperature of BOE 23°C, time 6 minutes. The BOE 6:1 at this temperature has an etch rate of silicon dioxide of 1025Å/min. indicating an oxide thickness of 6100Å.

II. P Well Ion Implantion

Wafers 3 through 6

1. Photolithography Process with mark #1
   a. Apply photoresist ("Waycoat HR200")
   b. Spin at 5000 RPM - 20 sec.
   c. Prebake in infared oven 15 amps 1.5 min.
   d. Expose in 'Kasper' 2000 mask aligner with P Well mask number 1. 4 sec.
   e. Spray develop with photoresist developer for 20 sec.
   f. Spray rinse with N Butyl Acetate for 20 sec.
   g. Post bake in infared oven 15 amps 5 min.
2. P Well Etch
   a. Etch wafer #3 through 6 in BOE etch at 23°C for 6 min.
   b. Strip photoresist in a solution of 70% H_2SO_4 30% H_2O_2 for 5 min.
3. Implant protective oxide
   a. Pre-oxidation clean wafers 1 through 6
   b. Slow push in furnace Temperature 1100°C 5 min.

Gas	Time
N_2 1ℓ/min	5 minutes
O_2 1ℓ/min	10 minutes
N_2 1ℓ/min	15 minutes
Slow pull from furnace	5 minutes

Oxide color light brown indicating approximately 500Å. Run #5, wafers 1-6 were sent to MSFC at Huntsville for P Type Boron Ion Implantion at 120 Kev to a concentration of 2.5×10^{13} cm^3.

A variation of this process was to leave the photoresist on after the P Well Etch and to omit the protective oxide.

4. P Well Drive In

   a. Remove photoresist (if left on) in a solution of 70%-30% H_2SO_4 - H_2O_2.

   b. Etch 4000Å of silicon dioxide in BOE for 4 min. at 22.5°C. This step removes all the implant protective oxide and leaves 2000Å of masking oxide for pattern definition to facilitate alignment with mask #2.

   c. Pre oxidation cleaning process.

   d. Slow push into cleaned boron drive in furnace wafers 1-7. Temperature 1150°C.

Gas	Time
N_2 1ℓ/min	5 minutes
O_2 1ℓ/min	16 hours
N_2 1ℓ/min	30 minutes
Slow pull from furnace	5 minutes

   e. Etch oxide from wafer #1 to base silicon. BOE etch 22.5°C, 6.5 min. Oxide was 6500Å thick.

   f. Check P well depth by gruve and stain technique. - 7.5 μ.

   g. Check resistivity with four-point probe 2200 Ω/□.

III. P^+ Boron Diffusion

1. Photolithography process mask #2. (Same as photo process mask #1). Wafers 3 through 6

2. P^+ boron diffusion etch.

a. Etch wafer #7 to base silicon in BOE etch solution. Rate time and temp. (6.5 min - 22.5°C - oxide 6500Å).

b. Etch wafers 3-6 for above time plus 30 sec.

c. Strip photoresist in H_2SO_4 - H_2O_2 solution 70:30 5 minutes.

d. Pre diffusion cleaning process.

3. P^+ Boron diffusion

Wafers 2-7

Boron source was Boron-Titride wafers, "B/N 975" manufactured by the "Carborundum Company".

a. Boron Pre-Deposit - furnace temperature 1000°C

Slow push in H_2	5 minutes
Gas	Time
N_2 250 cm^3/min	25 minutes
Slow pull from furnace	5 minutes

4. Borosilicate glass removal

a. Etch wafer in BOE at 22.5°C 1 min.

b. Rinse in DI water 5 min.

c. Etch in Jacobsons etch 95°C 1 hr.

d. Rinse in DI water 5 min.

e. Etch in BOE 1 min.

f. Rinse in DI water

g. Blow dry in N_2.

5. Check Resistivity wafer #7 with four point probe (33 Ω/□) typical.

6. Boron Drive In - N^+ Masking oxide

   Wafers 1-7

   Furnace temperature 950°C

a. Slow push in	5 minutes
Gas	Time
N_2 1ℓ/min	5 minutes
O_2 1ℓ/min	5 minutes
O_2+H_2O @ 95°C 1ℓ/min	60 minutes
O_2 1ℓ/m	5 minutes
N_2	10 minutes
Slow pull from furnace	5 minutes

IV. N^+ Phosphorous Diffusion

1. Photolithography process mask #3 (Same as photo process mask #1).

   Wafers 3 through 6

2. N^+ phosphorous diffusion etch. Wafers 2 through 6. Oxide is left on test wafers 1 and 7.

   a. Etch wafer #2 to base silicon in BOE etch. Note time and temperature.

      22.5°C 4.2 min. - 4200Å

   b. Etch wafers 3 through 6 for above time plus 30 sec.

   c. Strip photoresist from wafers in H_2SO_4 - H_2O_2 solution 70-30 for 5 min.

   d. Pre diffusion cleaning process wafers 1 through 7.

3. N^+ Phosphorous Diffusion Wafers 1 through 7. Phosphorous pre deposit is done over masking oxide on test wafers 1 and 7 to check integretity of oxide.

a. Phosphorous pre-deposit.

Phosphorous source was "Phosphorousiliconfilm" CO=$5x10^{20}$ manufactured by the Emulsitone Company, a liquid, it is spun on the wafer at 3000 RPM.

b. Phosphorous furnace purged in TCE + O_2 Temperature 1100°C for 12 hours. Temperature reduced to 1000°C for pre-deposit. Wafers dried at mouth of furnace for 20 minutes.

Slow push in	5 minutes
Gas	Time
N_2 1ℓ/min	20 minutes
slow pull from furnace	5 minutes

c. Phosphosilicate glass removal.

All oxide to be removed from wafers prior to growth of field oxide during N^+ phosphorous drive in.

Etch wafers in BOE at 225°C to base silicon time 7.5 minutes.

4. Resistivity check - Four point probe method.

Wafer #1 (P well $\bar{P}$) - 2200 Ω/□

Wafer #2 (N^+ Phos.) - 18 Ω/□

Wafer #3 (P^+ Baron) - 105 Ω/□

5. <u>N^+ Phos. Drive-in - Field Oxide</u>

a. Pre diffusion clean all wafers.

b. Furnace Temperature 950°C slow push in 5 minutes.

Gas	Time
N_2 1ℓ/min	5 minutes
O_2 1ℓ/min	10 minutes
O_2+H_2O 95°C 1ℓ/min	60 minutes

Gas	Time
O_2 1ℓ/min	10 minutes
H_2 1ℓ/min	20 minutes
Slow pull from furnace	5 minutes

V. Gate Oxide

1. Photolithography process mask #4 (same as photo process mask #1).
   Wafers 3 through 6.
2. Gate oxide etch wafers 1 through 7.
   a. Etch wafers 1, 2, 7 in BOE at 50°C to base silicon.
      time 50 sec. oxide ≃ <1000Å Thick
   b. Etch wafers 3-6 in BOE at 50°C for 60 sec.
   c. Strip photoresist in H_2SO_4 - H_2O_2 (70-30) for 95°C for 5 min.
      Rinse in DI water 10 min.
3. Resistivity check - Four Point Probe Method
   Wafer #1 - 2300 Ω/□
   Wafer #2 - 16 Ω/□
   Wafer #3 - 115 Ω/□
4. Gate Oxidation
   a. Pre oxidation wafers 1 through 7.
   b. Slow push in to pre purged furnace. Furnace temperature 900°C.

Gas	Time
N_2 1ℓ/min	5 minutes
O_2 1ℓ/min	10 minutes
O_2 bubbled through a solution of H_2O-HCL (50-50) at 95°C.	

Gas	Time
1ℓ/min	60 minutes
O_2 1ℓ/min	10 minutes
N_2 1ℓ/min (Furnace temperature increased to 1050°C)	20 minutes

c. Slow pull from furnace in H_2 5 minutes

Wafers a dark purple color indicating approximately 1000Å of oxide.

VI. Contact Opening

1. Photolithography process with mask number 5.
2. Contact etch. Wafers 1 through 7.
   a. Etch wafers 1, 2 and 7 in BOE at 22.5°C. Time one minute indicating approximately 1000Å.
   b. Etch wafers 3 through 6 in BOE at 22.5°C for 75 sec.
   c. Check Gate Oxide Thickness Etch in BOE to 900Å.
   d. Remove Photoresist in boiling (95°C) H_2SO_4 H_2O_2 solution.
   e. Wash in running DI water 15 minutes.
3. Resistivity check wafers 1, 2, and 7.

   Wafer #1 - 2300 Ω/□

   Wafer #2 - 16 Ω/□

   Wafer #3 - 120 Ω/□

VII. First Metal Level

1. Pre diffusion clean all wafers.
   a. Load wafers into Electron Beam evaporation chamber.

b. Evacuate chamber to a pressure of $1x10^{-6}$ Torr. Heat chamber to 100°C for 1 hour before evaporation to remove all water vapor from wafers and chamber.

c. Evaporate 99.990% Pure Aluminum at 20Å/sec. for 6.25 minutes to a thickness of 7500Å.

d. Allow chamber to cool to room temperature before opening.

2. Photolithography process wafers 3 through 6. Mask #6.

3. Metal etch

a. Etch wafers in Aluminum etch at 25°C until metal pattern is clear. Check pattern under microscope. Return to etch both if necessary.

b. Strip resist in photoresist stripping solution ("EC strip by Allied Chemical Corp.") 3 minutes at 95°C.

c. Clean wafers by boiling in Trichloroethylene for 3 minutes, acetone for 3 minutes, and methanol 3 minutes. Wash in running DI water 10 minutes.

d. Blow dry with nitrogen.

e. Electrical test. At this time the test devices on the wafers were checked to determine if they were functional.

Tests were made using a micro probe station and a "Tektronix" model 177 curve tracer.

Working test devices were found on all wafers with N MOS threshold voltages from 1 to 3 volts and P MOS threshold voltages from -1 to -4 volts.

VIII. Intermetal Oxide

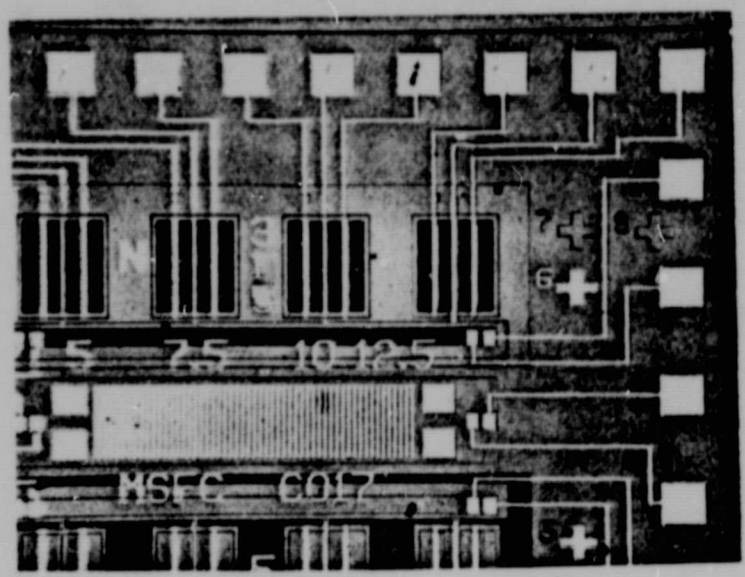
1. All wafers were sent to MSFC at Huntsville for CVD intermetal oxide to 8000Å.
2. Intermetal Oxide - VIA etch.
   a. Photolithography process mask #7 wafers 3-6.
   b. Etch wafer #2 in BOE at 22.5°C to base silicon. Time 3 minutes.
   c. Etch wafers 3-6 in BOE at 22.5°C for 3 minutes + 15 seconds.
   d. Strip photoresist in "EC Strip" photoresist stripping solution.
   e. Clean wafers in boiling Trichloroethylene for 3 minutes, acetone 3 minutes, and methonal 3 minutes. Wash in running DI water 10 minutes.
   f. Blow dry with N_2.

IX. Second Metal Level

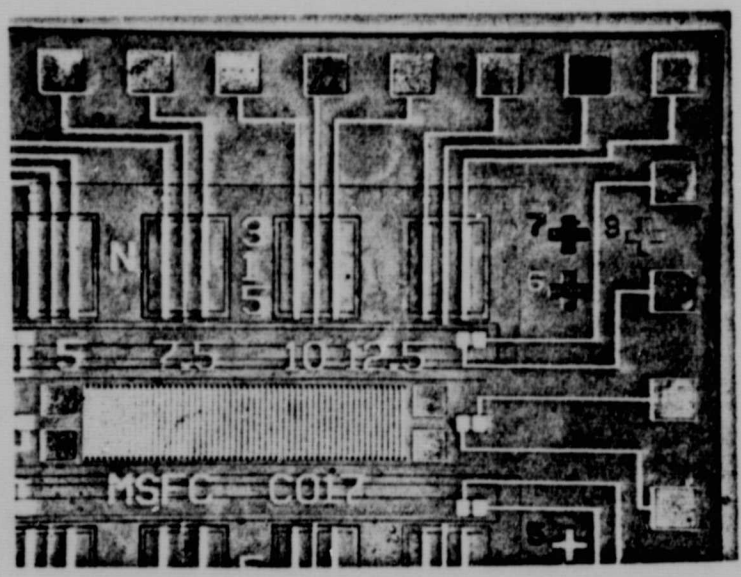
Wafers returned to MSFC at Huntsville for passivation and second metal process. Only the passivation was applied to the wafers. The second level metal was not attempted. The wafers were then returned to Auburn. When contact window opening was attempted, the metal pads were destroyed, and reliable contact could not be made for further testing. The photomicrographs on the next page show the wafers before and after the inter-metal passivation and contact etching. In photograph b the pad areas have been opened, but the pad metal has been etched away.

Conclusions

1. Results of tests show that a good quality oxide of the thickness required for a theoretically better Rad Hard device can be grown. Low temperature HCL oxides give the best quality oxide.



(a) Before Intermetal Oxide



(b) After Intermetal Oxide

Figure 4. Photomicrographs of Wafers Before and After Intermetal Passivation and Contact Etching.

2. The testing of devices at progressive steps of fabrication illustrated that successful C-MOS circuits using the process developed at MSFC with modifications to the cleaning steps and gate oxide growth, can be made. At intermediate stages during processing, test devices showed correct threshold voltages on both the n- and p-channel devices.
3. The devices could not be completed and tested for Rad Hardness because of damage to the wafers that occured during delays in shipping them back and forth between Auburn and MSFC. Large negative threshold voltage shifts were also noted before and after shipment of the wafers. Many of the n-channel transistors had become depletion-mode devices (threshold voltage < 0). These threshold shifts prevent proper operation of CMOS logic. These problems could be resolved by doing all the processing in one facility.

References

[1] B. L. Gregory, IEEE Trans. on Nuclear Science, NS-22, No. 6, pp. 2295-2302 (1975).

[2] G. F. Derbenwick, B. L. Gregory, IEEE Trans. on Nuclear Science, NS-22, No. 6, pp. 2151-2156 (1975).

[3] B. E. Deal, Journal Electrochemical Society, pp. 198C-205C, June 1974.

[4] R. S. Clark, Solid State Technology, pp. 80-82, November 1978.

[5] P. H. Robinson and F. P. Herman, Journal Electrochemical Society, pp. 141-143, January 1971.