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DEFECTS AND DEVICE PERFORMANCE

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The necessity for a low-cost crystalline silicon sheet material for photovoltaics has generated a number of alternative crystal growth techniques that would replace Czochralski (Cz) and float-zone (FZ) technologies. A major thrust with these alternative techniques has been to increase the efficiency of FZ and Cz silicon. At present, efficiencies of devices fabricated from low resistivity FZ silicon are approaching 20%, and it is highly likely that this value will be superseded in the near future. FZ silicon has an advantage in obtaining this goal since sufficiently long-minority carrier lifetimes are possible at low resistivities ($\approx$ 0.1 ohm-cm.). However, FZ silicon is expensive, and is unlikely ever to be used for photovoltaics. Cz silicon has many of the desirable qualities of FZ except that minority-carrier lifetimes at lower resistivities are significantly less than those of FZ silicon. However, it appears that an efficiency of 20% can be exceeded even for Cz silicon, but more of the burden will fall on the fabrication of the device, i.e., to compensate for higher-resistivity material that has a longer-minority carrier lifetime, thinner silicon and effective back-surface fields will be necessary to attain higher efficiencies. Even with Cz silicon, it is unlikely that cost goals can be met because of the poor-material yield that results from sawing and other aspects of the crystal growth. It is as a consequence of the cost that other sheet technologies have been investigated. However, at this stage, almost all of the technologies result in materials that have characteristics that significantly limit efficiency. Not only are efficiencies limited by the minority carrier lifetimes but also by space charge recombination currents associated with both impurities (gross and point) and structural defects (sub-grain boundaries, dislocations, etc.). The considerable effort that has been expended on these alternate materials has shown that high efficiencies (>16%) can be obtained and that there is not necessarily any fundamental limitation in further improving at least some of these materials. Casting technologies will show some improvement in the cost per watt figures over Cz silicon, because nearly comparable efficiencies can be obtained at lower production costs. However, this technology has the same problem as Cz silicon in that silicon utilization is poor. Some ribbon materials also have the potential for very high efficiencies at reasonable cost, but further work is required in order to resolve structure and impurity problems, as well as problems of dimensional uniformity, stress, throughput, etc.

In summary, 20% efficient solar cells can likely be fabricated from both FZ and Cz silicon, but costs are likely to be ultimately unacceptable. Alternate silicon technologies are not likely to achieve this goal, but cost per watt figures may be eventually better than either of the single crystal technologies and may rival any thin-film technology.

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Objectives

- EVALUATE IMPACT OF CRYSTAL DEFECTS ON DEVICES
- PRESENT EXAMPLES FROM EXPERIENCES WITH CAST SILICON AND GENERALIZE TO OTHER SILICON TECHNOLOGIES

Evaluation Criteria

- QUALITY - EFFICIENCY
- YIELD - CONSISTENT QUALITY, DIMENSIONAL CONTROL, ETC.
- RELIABILITY
- COST

Diode Equation

$$I = \frac{V-IR_S}{R_{SH}} + I_{SCO}\left[e^{e(V-IR_S)/nkT} - 1\right] + I_{QNO}\left[e^{e(V-IR_S)/kT} - 1\right] - I_L$$

- I - MEASURED CURRENT
- V - MEASURED VOLTAGE
- R_S - SERIES RESISTANCE
- R_{SH} - SHUNT RESISTANCE
- I_{SCO} - SPACE CHARGE RECOMBINATION CURRENT
- I_{QNO} - QUASI-NEUTRAL RECOMBINATION CURRENT
- n - DIODE QUALITY FACTOR
- kT - THERMAL ENERGY
- I_L - LIGHT GENERATED CURRENT

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Material Impact, Float-Zone Silicon

$$I = I_{QNO}\left[e^{eV/kT} - 1\right] - I_L$$

WHERE $I_{QNO} = I_{EO} + I_{BO}$

EMITTER BASE

$$I_{BO} = \frac{en_i^2}{N_A}\,\frac{D_n}{L_n}\,\tanh\frac{d}{L_n} \qquad \text{WHERE } L_n = \sqrt{D_n\tau_n}$$

$\therefore$ WE SEE THAT THE MATERIAL CHARACTERISTICS OF IMPORTANCE ARE:

1. THE BASE DOPING, N_A
2. THE MINORITY CARRIER DIFFUSION LENGTH, L_n

➡ HIGHEST EFFICIENCIES ARE OBTAINED FROM HIGHEST N_A AND L_n FOR LOW INJECTION CASE

LIMITS ON EFFICIENCY SET BY AUGER RECOMBINATION (L_n IN FZ SILICON APPROACH AUGER LIMITS)

EVALUATION:

- ✓ QUALITY
- ✓ YIELD
- ✓ RELIABILITY
- X COST

Material Impact, Czochralski Silicon

$$I = I_{QNO}\left[e^{eV/kT} - 1\right] - I_L$$

$$I_{BO} = \frac{en_i^2}{N_A}\,\frac{D_n}{L_n}\,\text{TANH}\,\frac{d}{L_n}$$

AS WITH FZ SILICON, MATERIAL CHARACTERISTICS OF IMPORTANCE ARE:

1. THE BASE DOPING, N_A
2. THE MINORITY CARRIER DIFFUSION LENGTH, L_n

➡ HIGHEST EFFICIENCIES ARE OBTAINED FROM HIGHEST N_A AND L_n FOR LOW INJECTION CASE, HIGHEST L_n FOR HIGH INJECTION CASE.

IN CZ SILICON $\sim$, $L_n \ll L_n^{AUGER}$, PARTICULARLY AT LOW RESISTIVITY.

➡ HOWEVER, HIGH EFFICIENCY CELLS CAN BE FABRICATED FROM CZ SILICON

.

EVALUATION:

- ✓ QUALITY
- ✓ YIELD
- ✓ RELIABILITY
- (?) COST

Alternative Silicon Technologies

o COST ISSUE HAS DRIVEN EFFORTS TO FIND AN ALTERNATE SILICON TECHNOLOGY

1 CASTING
2 - SELF-SUPPORTING RIBBON
3 - RIBBON ON A SUBSTRATE

Efficiency/Yield-Limiting Materials Characteristics

- o DISLOCATIONS IN GRAIN BOUNDARIES
- o DISLOCATION SUB-GRAIN BOUNDARIES
- o INTRA-GRAIN ISOLATED DISLOCATIONS
- o GROSS IMPURITIES - INCLUSIONS, PRECIPITATES
- o ISOLATED IMPURITIES
- o DIMENSIONAL EVENNESS, PROCESSABILITY

Cast Polycrystalline Silicon Examples

1. ELECTRICALLY ACTIVE GRAIN BOUNDARIES - SMALL GRAINS

IMPACT: INCREASE IN SPACE CHARGE RECOMBINATION CURRENTS

DECREASE IN EFFECTIVE MINORITY CARRIER LIFETIME

INCREASE IN DARK CURRENT BECAUSE OF GREATER JUNCTION AREA

CONSEQUENCE: I_{sc}, V_{oc}, FF DECREASED

SOLUTION: CONTROL TEMPERATURE OF CONTAINER AND SOLIDIFICATION RATE

RESULT: POLYCRYSTALLINE WAFERS WITH GRAIN DIAMETERS $\geq$ 5 mm

ALTERNATE SOLUTION: GRAIN BOUNDARY PASSIVATION

Electrically Actived Sub-Grain Boundaries/Isolated Dislocations

IMPACT: INCREASE IN SPACE CHARGE RECOMBINATION CURRENTS

DECREASE IN EFFECTIVE MINORITY CARRIER LIFETIME

INCREASE IN DARK CURRENT BECAUSE OF GREATER JUNCTION AREA

CONSEQUENCE: I_{sc}, V_{oc}, FF REDUCED

SOLUTION: CONTROL OF HORIZONTAL TEMPERATURE PROFILES DURING SOLIDIFICATION AND COOL DOWN

RESULT: REDUCED SUB-GRAIN BOUNDARY DENSITY AND ISOLATED DISLOCATIONS ($< 5 \times 10^3$ cm^{-2})

Gross Impurities—Inclusions in Grain Boundaries

IMPACT: SHUNTS

LOW MINORITY CARRIER LIFETIME

CONSEQUENCE: VERY LOW I_{sc}, V_{oc}, FF

SOLUTION: REDUCTION OF CARBON IN MELT, CONTROLLED SOLIDIFICATION RATES

RESULT: GREATER YIELD OF "HIGH" QUALITY MATERIAL, FASTER SOLIDIFICATION RATES

Table 1. Polysilicon Solar Cell Illuminated I-V Characteristics (100 mW/cm^2, 25°C)

CELL AREA (cm^2)	NO. CELLS	STATISTIC	J_{sc} (mA/cm^2)	V_{oc} (mV)	F.F.	EFFICIENCY (%)
100	50	MEAN	30.6	574	0.761	13.4
		σ	0.66	5.9	0.011	0.31
100	1		31.3	584	0.771	14.1
4.03	1		34.6	601	0.779	16.2

Table 2. Short-Circuit Current Losses for Small and Large Area Polysilicon Cells in the Region 400 to 1100 nm

	16.2% (4.03cm^2)		14.1% (100cm^2)	
LOSS MECHANISM	FRACTION AVAILABLE AFTER LOSS	J_{sc}(mA/cm^2) AVAILABLE AFTER LOSS	FRACTION AVAILABLE AFTER LOSS	J_{sc}(mA/cm^2) AVAILABLE AFTER LOSS
THEORETICAL MAXIMUM	1.0	43.2	1.0	43.2
INTERNAL QUANTUM EFFICIENCY LOSS	0.87	37.6	0.85	36.7
ANTIREFLECTION COATING LOSS	0.97	36.5	0.97	35.6
GRID SHADOWING LOSS	0.95	34.6	0.88	31.3
NET	0.80	34.6	0.73	31.3

Table 3. Dark I-V Characteristics (25°C) for Small and Large Area Polysilicon Solar Cells

PARAMETER	16.2% ($4.03 cm^2$)	14.1% ($100 cm^2$)
SHUNT CONDUCTANCE G(mU/cm^2)	0.18	0.90
SERIES RESISTANCE R_S(Ω-cm^2)	0.38	0.32
SPACE-CHARGE DIODE QUALITY FACTOR, N	3.5	2.0
SPACE-CHARGE CURRENT J_{SCO}(mA/cm^2)	4.6×10^{-3}	6.3×10^{-4}
QUASI-NEUTRAL CURRENT J_{ONO}(mA/cm^2)	2.3×10^{-9}	3.6×10^{-9}
EQUIVALENT VOLTAGE V_E(mV)	522	496
BASE RESISTIVITY (Ω-cm)	1.0	1.7

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Losses Associated With Dark I-V Characteristics in Table 3 for Small Area (Table 4A) and Large Area (Table 4B) Polysilicon Solar Cells

INCLUDED DARK I-V COMPONENTS	I-V CHARACTERISTICS CALCULATED FROM INCLUDED DARK I-V COMPONENTS			
	V_{OC} (mV)	F.F.	η (%)	$\Delta\eta$ (%)
QUASI-NEUTRAL RECOMBINATION	602	0.829	17.2	-
QUASI-NEUTRAL & SPACE-CHARGE RECOMBINATION	599	0.796	16.4	0.8
QUASI-NEUTRAL, SPACE-CHARGE & SHUNT CONDUCTANCE	599	0.793	16.4	0
QUASI-NEUTRAL, SPACE-CHARGE, SHUNT CONDUCTANCE & SERIES RESISTANCE	599	0.775	16.1	0.3
MEASURED CHARACTERISTICS	601	0.779	16.2	-

TABLE 4A

INCLUDED DARK I-V COMPONENTS	I-V CHARACTERISTICS CALCULATED FROM INCLUDED DARK I-V COMPONENTS			
	V_{OC} (mV)	F.F.	η (%)	$\Delta\eta$ (%)
QUASI-NEUTRAL RECOMBINATION	588	0.826	15.2	-
QUASI-NEUTRAL & SPACE-CHARGE RECOMBINATION	584	0.803	14.7	0.5
QUASI-NEUTRAL, SPACE-CHARGE & SHUNT CONDUCTANCE	583	0.791	14.4	0.3
QUASI-NEUTRAL, SPACE-CHARGE, SHUNT CONDUCTANCE & SERIES RESISTANCE	583	0.777	14.2	0.2
MEASURED CHARACTERISTICS	584	0.779	14.1	-

TABLE 4B

Conclusions and Comments

1. PRESENT DAY FZ AND CZ ARE OF SUFFICIENT QUALITY TO OBTAIN EFFICIENCIES IN EXCESS OF 20%. FZ IS THE PREFERRED MATERIAL BECAUSE HIGHER L_n's CAN BE OBTAINED FOR A GIVEN N_A.

2. FZ AND CZ SILICON ARE VERY USEFUL TO THE DEVICE RESEARCHER FOR DETERMINING THE IMPORTANCE OF THE VARIOUS LOSS MECHANISMS AND FOR DEVISING THE PROCESSING TECHNOLOGIES TO REDUCE THE LOSSES.

3. ECONOMIC CELL PROCESSING TECHNOLOGIES WILL ALSO NEED TO BE DEVISED THAT TAKE ADVANTAGE OF THE EXPERIENCE GAINED IN THE LABORATORY.

4. ULTIMATELY, IT IS UNLIKELY THAT EITHER CZ OR FZ SILICON IS ECONOMIC FOR PHOTOVOLTAICS. THIS IS ALSO TRUE FOR ANY TECHNOLOGY THAT REQUIRES WAFERING.

5. THE IMPORTANT ISSUE FOR THE ALTERNATE SILICON TECHNOLOGIES IS WHETHER SUFFICIENTLY HIGH L_n's FOR A GIVEN N_A AND d ARE ACHIEVABLE, AND, IF ACHIEVABLE, WHETHER IT CAN BE DONE QUICKLY AND ECONOMICALLY.

WHAT ARE THE NECESSARY GOALS?

6. FOR CASTING TECHNOLOGIES, IT HAS BEEN POSSIBLE TO REDUCE LOSSES DUE TO STRUCTURAL DEFECTS AND GROSS IMPURITY CONTAMINATION WITH THE RESULT THAT L_n's NEAR 200 μM FOR $\rho \simeq 1$ Ω-CM HAVE BEEN ACHIEVED. FURTHER IMPROVEMENTS APPEAR TO BE POSSIBLE, AND EXPERIENCES WITH CZ AND FZ MATERIAL MAY BE USEFUL.

Questions

1. WHAT ARE THE LIFETIME KILLERS IN AS-GROWN CZ AND FZ SILICON?

2. HOW REPRODUCIBLY CAN THE AS-GROWN LIFETIME BE OBTAINED?

DISCUSSION

RAO: You talked about shadowing losses because of grid-line broadening. Why are you getting the grid-line broadening?

STORTI: In those particular cells, we were trying to use a relatively inexpensive processing technique, similar to what Green has used. We used titanium as the base metal on the silicon with a palladium layer and then we use electroplated silver. What happened was that there was too much silver deposited.

RAO: You talked about isolated dislocation densities of $\leq 5 \times 10^3/cm^2$ and about a diffusion length of 200 μm in the material. If you back-calculate, assuming 5×10^3, the spacing between dislocations is of the order of 150 μm and you have a 200 μm diffusion length material. In that case, these dislocations actively act as sinks for the carriers. How do you reconcile these two numbers?

STORTI: Up until about a year ago the dislocations that we would see in the material for the most part were electrically active. We are beginning to see that there are dislocations that are not electrically active. As a consequence of that, we no longer can use that particular simple relationship. Other people have also found that once they get below a certain level, quite a few of the dislocations that are in the material are not electrically active, at least at room temperature.

WOLF: I'm not certain that today's Cz and FZ can get us to 20% or over 20% efficiency and certainly not anywhere near 25%. The problem really gets down to the lifetime of the material. Anything on device design and processing that you can do has essentially been done.

STORTI: No, I don't think people have tried, for example, to go to narrower bases and at the same time have it such that you will have good back-surface fields, or in other words, a condition where essentially your recombination at the back surface is low. You indicated in one of your papers that 50 μm might be the best thickness to actually use. There is very little work that has been done on those particular levels.

WOLF: On the other hand, for the thicknesses they used, they have not been able to get the diffusion length.

STORTI: This is a polycrystalline cell that had about 601 millivolts open circuit voltage, with a thickness of about 120 μm. We specifically chose that particular thickness because of the possibility of having an effective back-surface field. My contention is that if some of these other people who are working on these problems also went to thinner layers, they have a chance of not having to worry quite so much about the diffusion length of the material.

WOLF: Why not go the high-perfection route of growing Cz material that is single-crystal, rather than casting, which has no capital equipment or throughput economic advantage?

STORTI: It is possible to get a higher volume rate of solidification in a casting process than you can get in the case of Czochralski. In other words, you have the possibility of going out in the X and Y dimensions that you do not have in the case of Czochralski and float-zone silicon. We had cast 120-kg slabs, not by going up in this dimension (vertically), but by going out in that dimension (horizontally). There is some economic advantage associated with that. I will agree there is some question as to how much of an additional advantage you do get.

CISZEK: I would just like to reply to Martin Wolf's comment about the casting process that he saw at Osaka. That must be very different from what Wacker is doing. Wacker's viewpoint, and what I myself think is the real beauty of the casting process, is that throughput is not limited by the solidification rate, and I believe it. In Wacker's operation the pouring is done in an expensive apparatus, but then through a lock that poured material, with appropriate insulation around it and on top of it, is taken out, essentially, on a conveyor belt and another one is brought in. So the cooling takes place in a very low-capital-investment kind of situation and the only limitation is on how fast you can melt and pour the silicon, not how fast you can solidify it. I think that is a strong point of casting. It has other limitations, of course.

KALEJS: It's interesting that the polycrystalline material has achieved 16% efficiency. You showed a lot of problematic grain boundaries where phosphorus diffuses down. Presumably the better cell did not have too many of these. Do you have any feeling for how to avoid them, or why it is that certain boundaries are like that?

STORTI: It has been our feeling that there are dislocations in some of these grain boundaries. There is some circumstantial evidence that if you control the temperature gradients in the X and Y directions, then you will tend to end up with boundaries, even second-order twinning boundaries that are coherent boundaries, rather than boundaries that contain dislocations, so there is a possibility that you can reduce these. I'm not too sure that you have to worry that much about it. The penetration is about 1 μm and you have grain sizes that are on the order of half a cm to several cm.

KALEJS: Did you look at the defects in the high-efficiency cell?

STORTI: We took X-ray topographs at several angles, to get some idea of what the densities were. The dislocation densities were on the order of $5 \times 10^2/cm^2$.

KALEJS: A lot of dislocations perhaps could have migrated into the boundaries during the growth.

STORTI: That particular cell had maybe three or four grain boundaries. It was quite low density.