DOUBLE-INJECTION, DEEP-IMPURITY
SWITCH DEVELOPMENT

NASA CR-174936

D. W. Whitson

Final Report for the Period
February 27, 1984 to February 28, 1985

NASA Lewis Research Center
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Westinghouse R&D Center
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16. Abstract

The overall objective of this program was the development of device design and process techniques for the fabrication of a double-injection, deep-impurity $(DI)^2$ silicon switch that operates in the 2-10 kV range with conduction current values of 5 A at 2 kV and 1A and 10 kV. Other major specifications include a holding voltage of 10 V with no gate current, 10 μs switching time, and power dissipation of 50 W at 75°C.

With this contract it was decided to concentrate on the lateral circular devices in order to optimize the gold diffusion. This resulted in devices that are much better switches (∿ 1 μs switching time), and in a gold diffusion process that is much more controllable than the one developed at the University of Cincinnati. Some results with injection-gated devices were also obtained. The current conduction for $V < V_T$ was analyzed and seen to agree, for the most part, with Lampert's theory.

Various sections of this report describe the device designs, wafer-processing techniques, and various measurements which include ac and dc characteristics and four-point probe.

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1. SUMMARY

The overall objective of this program was the development of device design and process techniques for the fabrication of a double-injection, deep-impurity $(DI)^2$, silicon switch that operates in the 2-10 kV range with conduction current values of 5 A at 2 kV and 1 A at 10 kV. Other major specifications include a holding voltage of 10 V with no gate current, 10 μsec switching time, and power dissipation of 50 W at 75°C.

With this contract it was decided to concentrate on the lateral circular devices in order to optimize the gold diffusion. This resulted in devices that are much better switches (~ 1 μsec switching time), and in a gold diffusion process that is much more controllable than the one developed at the University of Cincinnati. Some results with injection-gated devices were also obtained. The current conduction for $V < V_T$ was analyzed and seen to agree, for the most most part, with Lampert's theory.

Various sections of this report describe the device designs, wafer-processing techniques, and various measurements which include ac and dc characteristics and four-point probe.

2. INTRODUCTION

2.1 Double-Injection Deep-Level Devices

The current-voltage characteristics of an idealized double-injection deep-level device are shown in Figure 1. As the voltage is increased the current first responds in a linear fashion, which is the Ohm's law region in segment a. As the voltage is further increased, the current first increases as the square of the voltage (segment b), and then goes into the negative resistance regime (segment c) when the applied voltage exceeds some threshold voltage, V_T. Segment d is due to the formation of current filaments in the device. When the current reaches a certain level after V_T has been exceeded, according to the theory of Lampert and Mark,[1] the current will increase as the square of the voltage (segment e).

Two assumptions are made in the development of the injection theory with these devices: (1) the current is volume controlled, i.e., the contacts impose no significant constraints on the currents which are entering or leaving the crystal, and (2) diffusion currents are negligible. Both of these assumptions are justified if the device is "long enough." In practice, this usually means 2 to 4 mils depending on the material used. Baron[2] analyzed the effects of diffusion and found that some of the power laws were changed slightly. For our purposes, these effects are second-order and will not be considered any further.

The understanding of the I-V curve in Figure 1, with the exception of the current filament region, has come about from the theory first expounded by Lampert.[1,3,4]

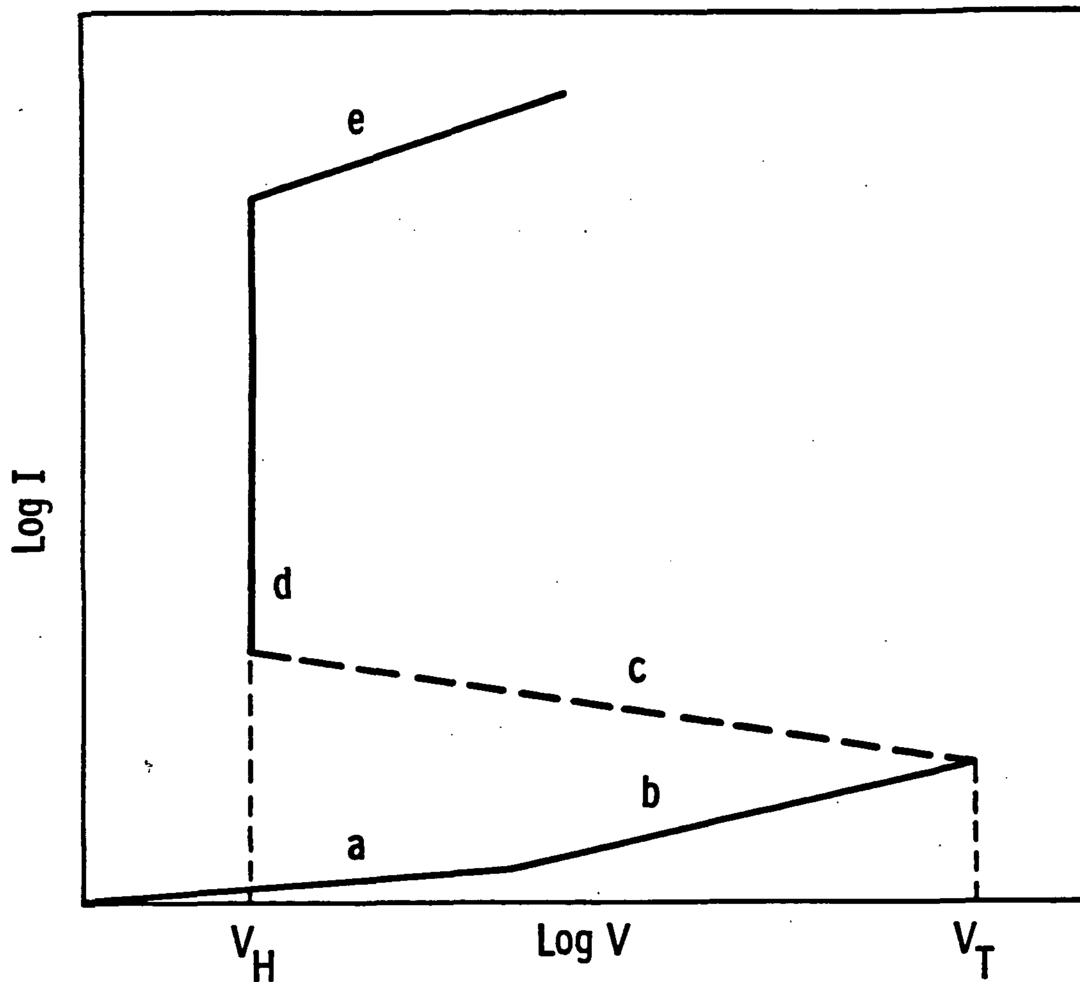


Figure 1. Idealized current-voltage characteristics of a double-injection deep-level switching device. The various regimes are: (a) Ohm's law (I α V); (b) low-injection square law (I α V^2), terminating at the threshold voltage, V_T, and followed by (c), the negative-resistance regime; (d) filament formation at the holding voltage, V_H; (e) high-injection square law (I α V^2).

2.1.1 Current Conduction Without Deep Levels

First, let us consider the case of phosphorus-doped material with no deep traps (Figure 2a). When the applied voltage, V, is less than the threshold voltage, there are two competing processes:

Ohm's law $$J = en\mu_n \frac{V}{L} , \tag{1}$$

and the low-injection square law $$J \cong \varepsilon\mu_n \frac{V^2}{L^3} \tag{2}$$

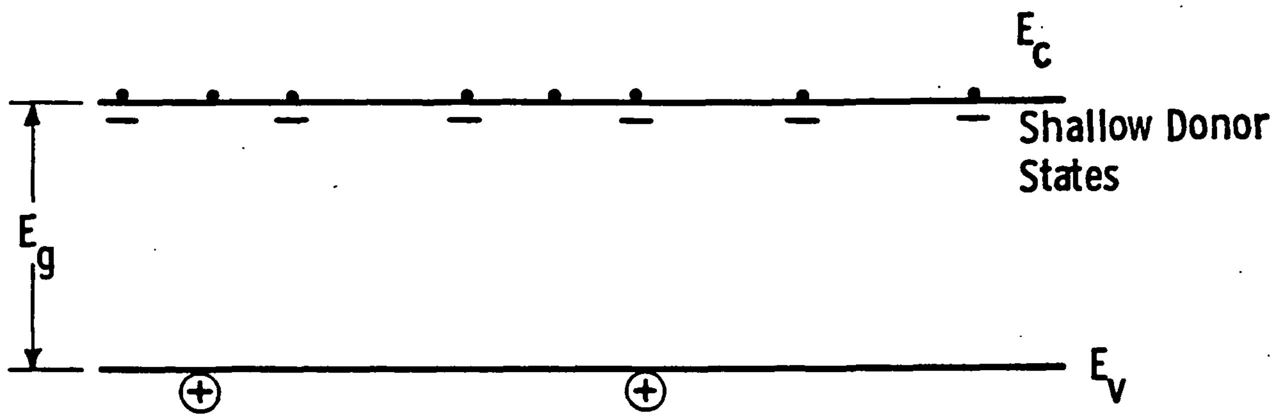
where L is the length of the device (see Figure 5a), μ_n is the electron mobility, n is the electron concentration, e is the electron charge, and ε is the dielectric constant. The latter current is also known as the space charge-limited (SCL) current or as the insulator square law current. At low voltages the Ohm's law current dominates. With the application of the voltage, V, there will be excess charge injected into the device; however, there cannot be significant departures from Ohm's law until the injected, excess, free-carrier density becomes comparable to the existing carrier density, n. This transition from Ohm's law to square law current occurs at the transition voltage:

$$V_{tr} \cong \frac{enL^2}{\varepsilon} \tag{3}$$

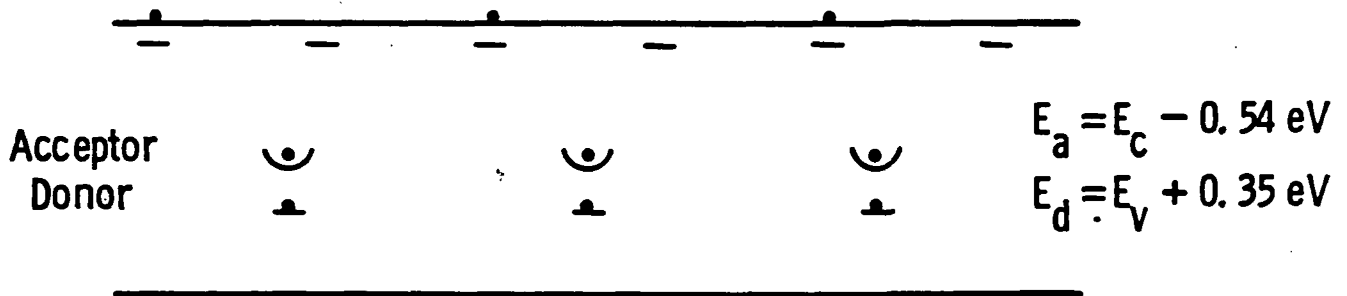
or when $$t_{tr} = \tau_D \tag{4}$$

where $\tau_D = \frac{\varepsilon}{en\mu_n}$ is the dielectric relaxation time and $t_{tr} = \frac{L^2}{\mu V_{tr}}$ is the carrier transit time between cathode and anode at the voltage V_{tr}.

Thus, the injected excess carriers dominate the existing free carriers, n, when the transit time for the excess carriers is too short for their charge to be relaxed by the thermal carriers.



(a)



(b)

Figure 2. (a) Silicon doped with phosphorus. (b) Phosphorus-doped silicon partially compensated by deep gold acceptor states, i.e., $N_t < N_D$. The gold donor states are filled and are neutral; the filled acceptor states are negatively charged.

2.1.2 Silicon Compensated With Gold

Let us now consider what happens with the addition of a deep-level impurity such as gold. The gold levels are given in Figure 2b. The donor level at $E_v + 0.35$ eV is not believed to affect the functioning of the device. The acceptor level at $E_c - 0.54$ eV, however, is what causes the "S"-type negative resistance response. When the density of gold atoms is less than the density of the phosphorus atoms (see Figure 2b), the Fermi level lies far enough above the gold acceptor levels that they are all filled. This reduces the number of free carriers and the resistivity of the bulk material increases. Thus, as the gold concentration increases, the resistivity of the n-type silicon increases. Figure 3 shows the case when the phosphorus-doped silicon is totally compensated by gold, i.e., $N_t = N_D$. For the unbiased sample almost all of the free carriers are thermally generated. Almost all of the gold acceptor levels will be filled. These filled levels are negative and have a large cross section for holes. Those gold acceptor levels that are empty are neutral and have a small cross section for electrons.

Figure 4 shows the change of resistivity that occurs as the gold concentration is increased. Note that when $N_t = N_D$, the material is essentially intrinsic and an increase in gold concentration at that point will cause the material to invert, i.e., turn p-type. If the conductivity type is checked with a hot-probe, the material will not register p-type when N_t is just barely larger than N_D because of the higher mobility of the electrons. As the gold concentration is increased further ($N_t > N_D$), the resistivity of the material decreases and the material becomes stronger p-type. The above effects occur no matter how the deep levels are created, e.g., with radiation or gold diffusion.

2.1.3 Current Conduction With Traps

A simple $(DI)^2$ device is shown in Figure 5a. The p^+ and n^+ regions are mainly for the injection of holes and electrons,

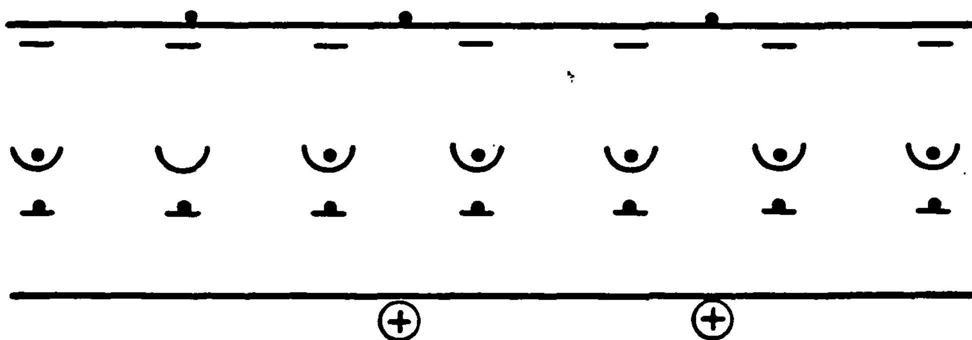


Figure 3. Silicon totally compensated by gold, i.e., $N_t \cong N_D$. For the unbiased sample almost all the carriers are thermally generated.

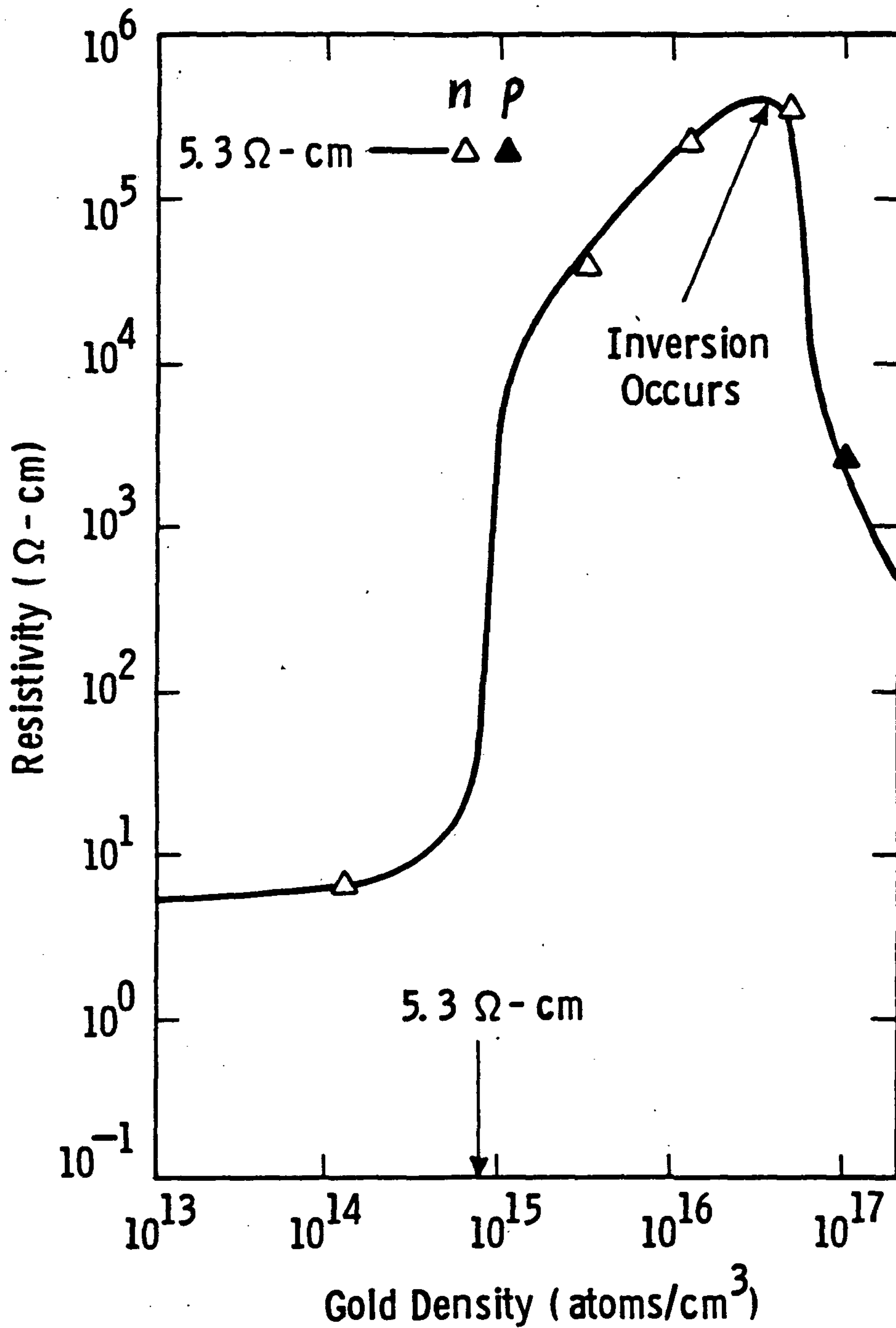
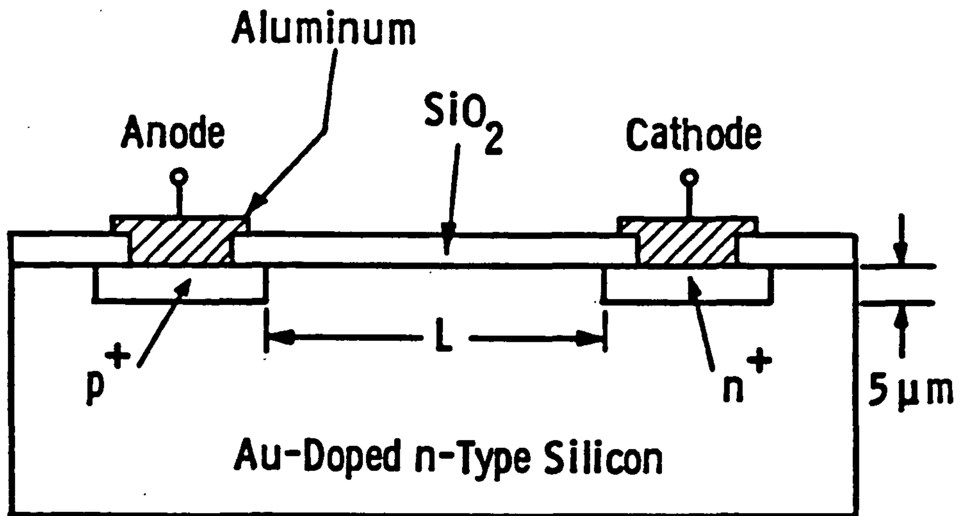
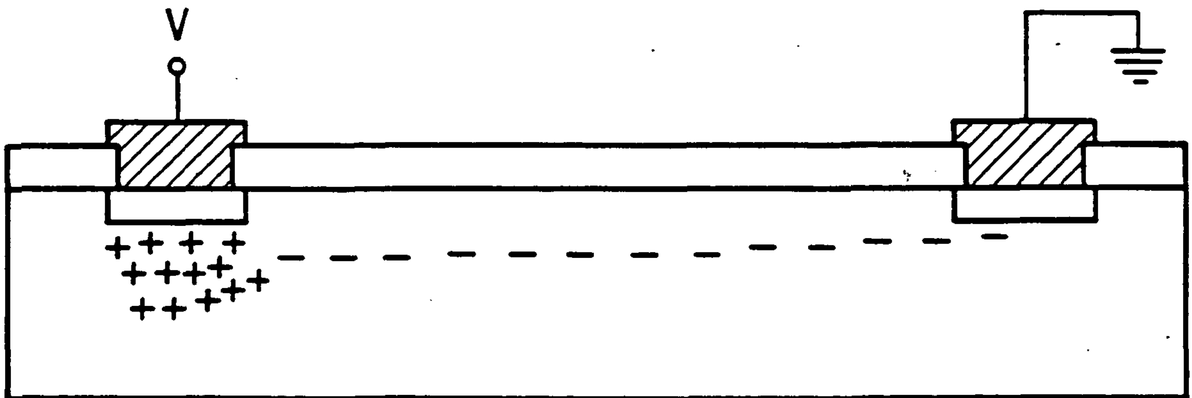


Figure 4. Change of resistivity due to deep levels. For n-type silicon a 5.3 ohm-cm resistivity sample has a donor concentration of about 9×10^{14} cm^{-3} (after Thurber and Bullis[5]).



(a)



(b)

Figure 5. Lateral $(DI)^2$ device. At low-voltage values the holes have a short lifetime and are captured near the anode. The electrons have a long lifetime and they set up a space charge between the cathode and anode. The current is mainly ohmic, i.e., $I \alpha V$.

respectively, into the bulk. Other than the injection of carriers, the electrodes play a minor role.

The negatively ionized gold sites exhibit a much larger trapping cross section, σ_p, for excess holes than the trapping cross section for electrons, σ_n, that is exhibited by the neutral gold acceptor levels. In fact, it is this very inequality ($\sigma_p >> \sigma_n$) that leads to the negative resistance behavior.

It is usually assumed that

$$\tau_n = \frac{1}{\sigma_n V_n N_t^0} \quad (5)$$

and

$$\tau_p = \frac{1}{\sigma_p V_p N_t^-} \quad (6)$$

where $\tau_n(\tau_p)$ and $V_n(V_p)$ are the electron (hole) lifetime and thermal velocity. N_t^0 is the density of traps that are neutral (i.e., not filled with an electron) and N_t^- is the density of traps that are negative and filled with an electron. We also have

$$N_t = N_t^0 + N_t^- \quad (7)$$

where N_t is the density of traps. Equations 5 and 6 are used to derive expressions for V_T and V_H. However, these equations are valid only under the approximations[6,7,8] that the excess carrier (injected charge) concentration and the trap density are much less than the equilibrium carrier concentration. For the $(DI)^2$ device, however, the trap density is approximately equal to the donor density. For the sake of simplicity it will be assumed that equations 5 and 6 hold, but for a more detailed analysis the more complex equations[6,8] that are correct for large trap densities should be used.

Figure 5b shows the carrier distribution for low voltages. The holes have short lifetimes ($N_t^- \cong N_t$) and are captured near the anode. The electrons have long lifetimes ($N_t^0 << N_t$) and set up a space charge between the cathode and anode. The voltage between the anode and cathode is dropped across this space charge. At these low voltages there is again an Ohm's law region, but the carrier concentration is only the thermal free carriers so that

$$J = en_o \mu_n \frac{V}{L} \tag{8}$$

where n_o is the concentration of the thermal free carriers. Since $\tau_n >> \tau_p$ the current is dominated by the electrons.

As the voltage is increased there is a value where the space charge-limited current takes over, as discussed in Section 2.1.1. Equations 3 and 4 hold here as well, but with $n = n_o$.

2.1.4 Threshold Voltage and Holding Voltage

At low levels of injection, the current is dominated by the electron flow because of the large coulombic trapping cross section of the ionized gold sites for hole capture. However, as the applied voltage is increased and more holes are injected, more holes are trapped on the negatively ionized gold sites near and increasingly beyond the anode, thus making it increasingly easier for holes to transfer into and across the material. The lifetime of the holes thus increases until it becomes equal to the transit time of the holes from the anode to the cathode, i.e., $V = V_T$ and

$$t_p = \frac{L^2}{\mu_p V_T} \cong \tau_{p,low} \tag{9}$$

where t_p is the transit time of the holes and $\tau_{p,low}$ is the lifetime of the holes in the low injection case. For this equation it is assumed that the correct lifetime to use is the low injection hole lifetime with $N_t^- \cong N_t$, i.e., the traps are still filled with electrons, and thus:

$$\tau_{p,low} = \frac{1}{\sigma_p V_p N_t^-} \cong \frac{1}{\sigma_p V_p N_t} . \quad (10)$$

Equations 9 and 10 lead directly to:

$$V_T = \frac{V_p \sigma_p L^2 N_t}{\mu_p} . \quad (11)$$

Lampert and Mark[1] find a threshold voltage that is one-half of equation 11:

$$V_T = \frac{V_p \sigma_p L^2 N_t}{2\mu_p} . \quad (12)$$

Their solution uses a regional approximation method and a rigorous neutrality theory and probably gives a better estimate of N_t^- than the above approximation. In fact, if one assumes that the switching condition occurs when $\tau_n = \tau_p$, then the ratio of N_t^- to N_t^0 would be

$$\frac{N_t^-}{N_t^0} = \frac{\sigma_n V_n}{\sigma_p V_p} . \quad (13)$$

If $\sigma_n V_n \cong \sigma_p V_p$, then

$$N_t^- \cong \frac{1}{2} N_t \quad (14)$$

and thus the factor of one-half. It would be useful to be able to establish a switching criteria that depends on the density of N_t^-.

The holding voltage was found by Lampert and Mark[1] to be:

$$V_H = \frac{1}{g(a)} \frac{L^2}{\mu_p \tau_h} \tag{15}$$

where $g(a) \cong 0.48$ for silicon at room temperature and τ_h is the common high-level injection lifetime. Here is assumed that $N_t^0 = N_t$ and

$$\tau_h = \tau_n = \frac{1}{\sigma_n V_n N_t} \tag{16}$$

so that the ratio of the two voltages (equation 12 and 15) is:

$$\frac{V_T}{V_H} = \frac{g(a)}{2} \frac{V_p \sigma_p}{V_n \sigma_n} . \tag{17}$$

Tuntasood[9] found that $V_T/V_H \cong 2$. This agrees reasonably well with many workers' measurements of σ_p and σ_n. However, the values of σ_p and σ_n for gold are somewhat controversial.[10]

2.1.5 Current Filaments

Lampert and others predict that the current follows a square law after going through the negative-resistance regime. However, it is found experimentally, in most cases, that the current rises almost vertically as the voltage increases in the post-breakdown regime. The reason for this behavior is attributed to the existence of current filaments.

A current filament is defined as the nonuniform distribution of current density in a sample with a uniform electric field. The existence of current filaments in "S"-type negative-resistance devices

was theoretically predicted by Ridley[11] and experimentally verified by Barnett and Milnes.[12] Ridley used the principle of the production of least entropy to define the stability of current filaments. Barnett[13] later analyzed and reported on this phenomenon in some detail. The reason for the almost vertical rise of current in this region is that most of the current flowing in the device flows through the established filament (or filaments) and then the filament grows in a cross-sectional area until it (or they) fills the cross-sectional area of the device. During this growth the voltage changes very little. Dudeck and Kassing[14] reasoned that if the size of the electrodes was smaller than the observed size of the current filaments (~ 200 μm), then only one current filament would be formed. Such devices were fabricated in order to be able to compare experimental and theoretical results. The agreement was quite good. Multiple current filament formation at large current levels (large electrodes) can cause some behavior problems[9] in these devices.

2.2 Symmetric Electrodes

In most of the work done on $(DI)^2$ devices it is assumed that the electrodes have little effect on the properties of the device and that the device current is volume controlled. Shieh and Henderson,[15] however, have found that the use of a shorted anode both increases V_T and decreases V_H. Shieh and Henderson term the device shown in Figure 6 as the "double-compound electrode SADIS device" (Shorted-Anode-Double-Injection Switching). For the sake of brevity this type of electrode will be referred to as the symmetric electrode. The SADIS device has a regular cathode (n^+ region) along with the symmetric electrode for the anode. The double compound electrode SADIS device has symmetric electrodes for both the anode and the cathode.

Y. Amemiya et al.[16] have used this type of electrode, which they term as an ideal ohmic contact, in order to produce a low-loss and high-speed diode for power applications.

Shieh and Henderson explain that the SADIS electrode decreases the hole injection efficiency in the prebreakdown regime at the anode and thus increases the breakdown voltage. With this electrode more negative space charge is built up because more of the injected electrons are not completely neutralized by injected holes. No holes will be injected from the SADIS electrode until the anode-channel junction is experiencing a bias voltage of more than one diode voltage drop, which is built up by the electron current that flows through the internal resistance near the anode. Figure 6 shows a top view and cross-sectional view of a device with the symmetric electrode used for both the anode and the electrode. Shieh constructed both this device and one with the anode having a symmetric electrode and a conventional cathode (i.e., n^+ region). For the latter device he found $V_T \cong 280$ volts and $V_H \cong 5.5$ volts. With the former device he found that the response was symmetric, i.e., in the positive direction ($V_T \cong 280$ V and $V_H \cong 5.5$ V), and in the negative direction, $V_T \cong -280$ V and $V_H \cong -5.5$ V. In both cases, the channel length was 4 mils.

2.3 Advantages of the $(DI)^2$ Switch For Power Devices

In a $(DI)^2$ device the voltage is dropped across the entire bulk area instead of just across a depletion area as in a conventional device (see Figure 7). Because of this the electric field is reduced in the bulk and some problems are alleviated. The breakdown voltage is not dependent on p-n junctions but on the bulk properties. Thus, the high voltage devices are limited only by the bulk breakdown limit. The possibility arises of using ohmic contacts (e.g., the symmetric electrodes in Section 2.2) instead of p-n junctions. Also, the topology of electrodes does not seem to be as important.

2.4 Switching

The devices produced using gold diffusion and irradiation can be classified as poor switches, better switches, and good switches. Some

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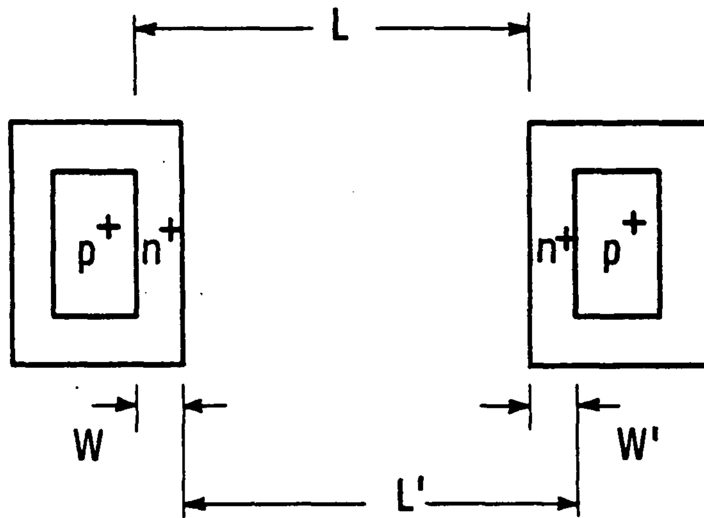


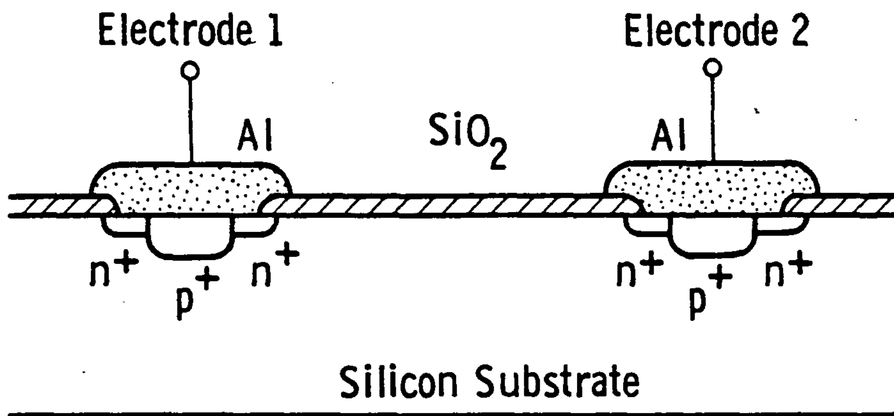
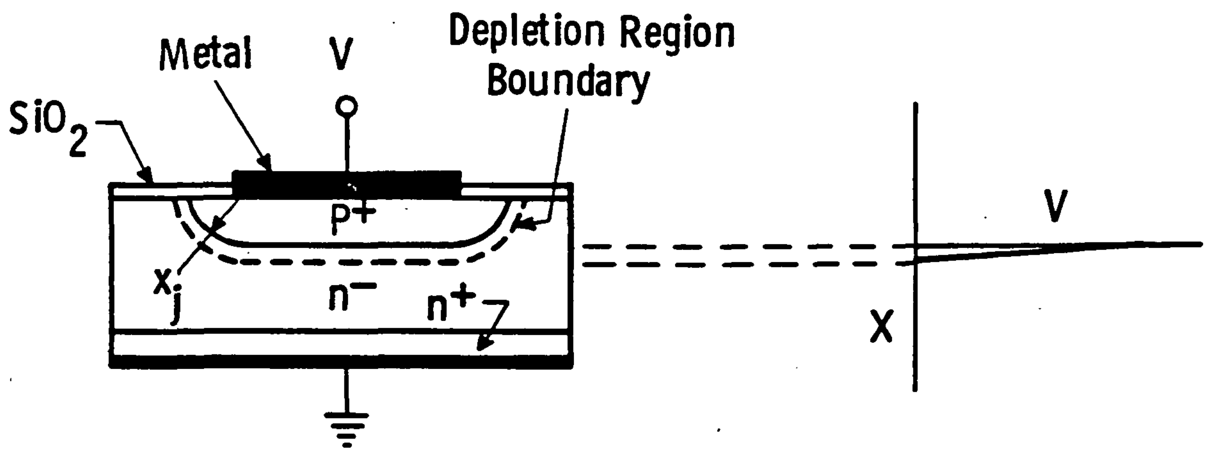
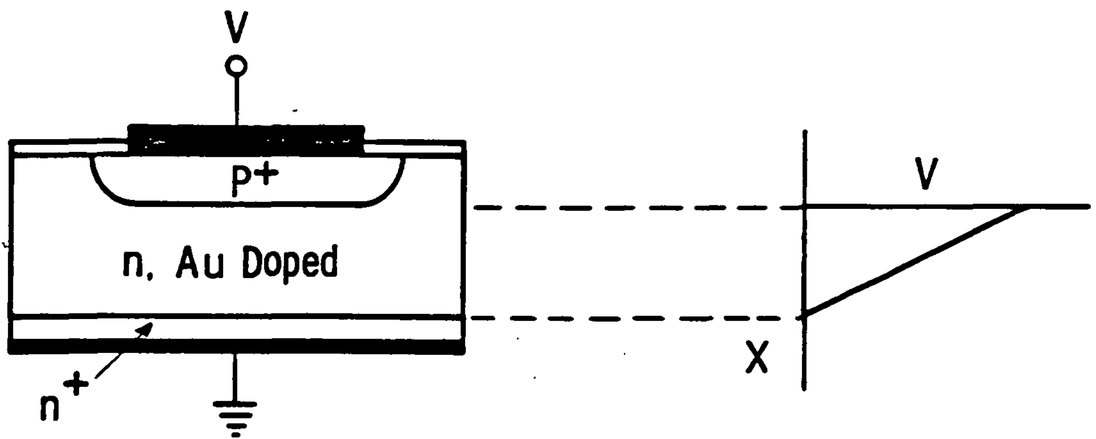


Figure 6. Top view (a) and cross section (b) of a double-compound electrode SADIS device or device with symmetric electrodes.



(a)



(b)

Figure 7. (a) Conventional bipolar device where the voltage is dropped across the depletion region. (b) $(DI)^2$ device where the voltage is dropped across the entire bulk region.

good switches have been measured[17] to have a switching time on the order of a microsecond (see Figure 8). Examples of poor switches are shown in Figure 9c and Figure 10 and a better switch is shown in Figures 9a and 9b.

The results shown in Figures 8, 9b, and 10 were made using an ac I-V curve tracer. A fully rectified 60 Hz sine wave (i.e., f = 120 Hz) with a peak voltage, V_p, was applied to the device in series with a 3 k-ohm resistor. Figures 9a and 9c were made using what is essentially a dc technique, i.e., a multiple exposure using ac pulsed testing with 80 μsec pulse so that the response is equivalent to a dc response. The peak value of the pulse is changed manually while the shutter of the camera is held open.

In Figure 8 the switch is fast enough so that it recovers fully between 120 Hz pulses. However, for the switch shown in Figure 9b (the "better switch") the device only partially recovers. This is evidenced by the threshold voltage only being about 680 volts in Figure 9b, while in Figure 9a it is seen to be 1350 V. Figures 9a and 9b are responses of the same switch, although in one case, 9a, the response is dc and in the other case, 9b, the response is ac.

The ac response of a poor switch is shown in Figure 10. As the peak voltage, V_p, increases from zero to the threshold voltage, the current increases with the device voltage. However, when the peak voltage is larger than the threshold voltage, the device voltage decreases as the current increases (V_p also is increasing), i.e., this is a negative resistance response. The very tip (i.e., the maximum current value for a given value of V_p) of the I-V curve traces out the dc response similar to that shown in Figure 9c. It doesn't match in this case because the device used in Figure 10 was not the same as in Figure 9c.

In the text the values of V_T recorded are the largest voltages obtainable before the device goes into the negative resistance regime. In Figure 9a the threshold voltage is about 1350 V, and in Figure 9c it

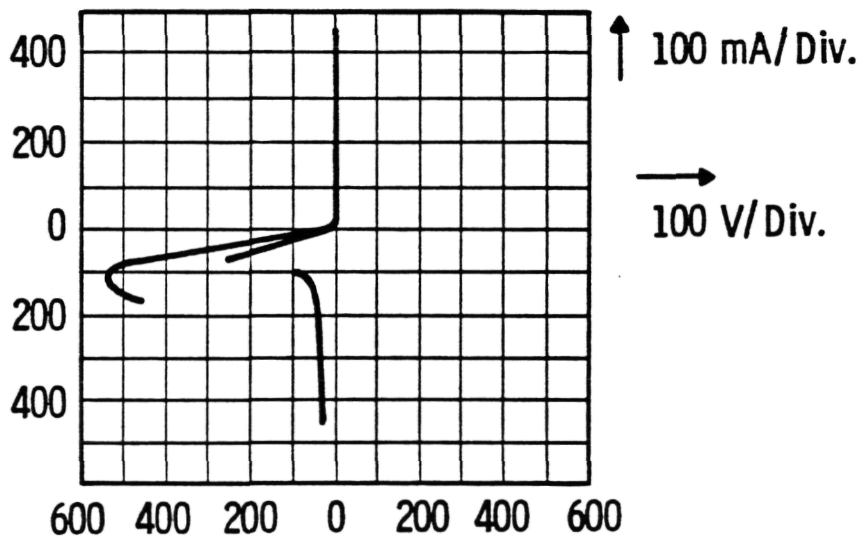


Figure 8. Response of a good switch [wafer 3-8(a)] to an ac curve tracer. The switching time was measured to be about one microsecond.

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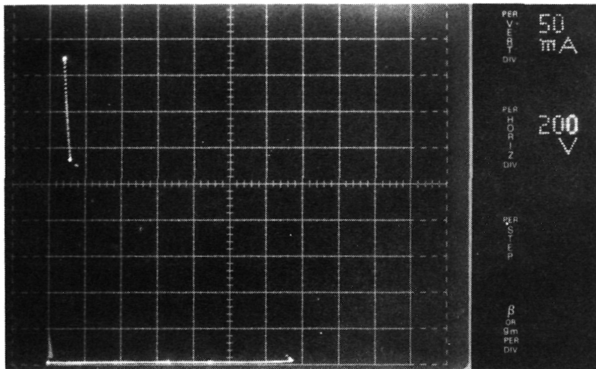
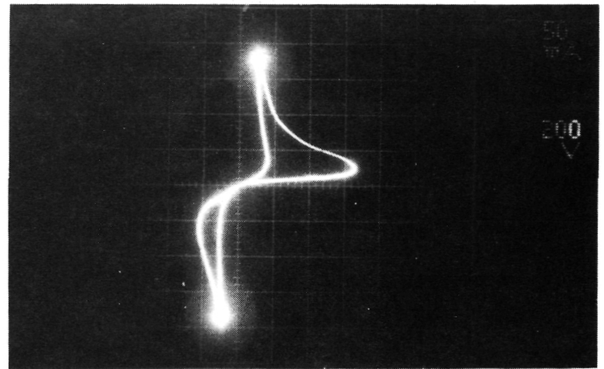


(a)



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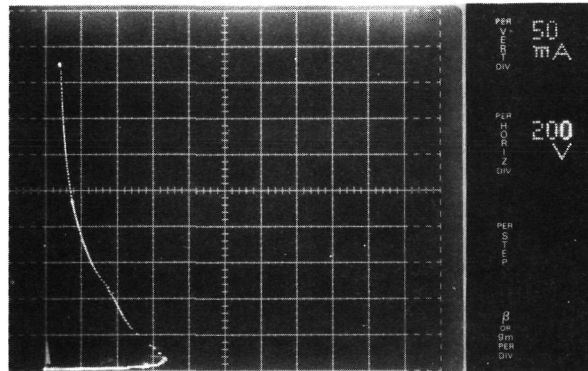

(c)

Figure 9. The I-V response $(DI)^2$ devices. Parts (a) and (c) are essentially a dc response and part (b) is an ac response. Parts (a) and (b) are for a switch that is classified as a better switch, while part (c) is for a poor switch. All graphs are 50 mA/cm for the vertical and 200 V/cm for the horizontal.

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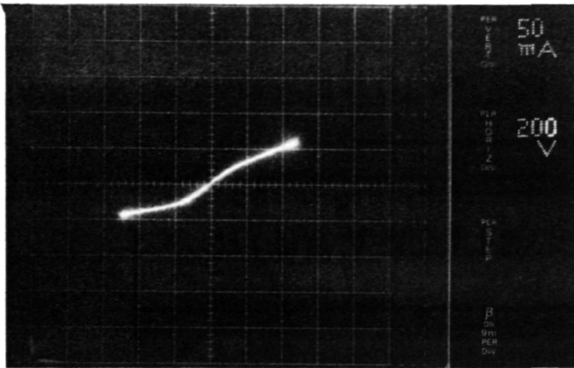
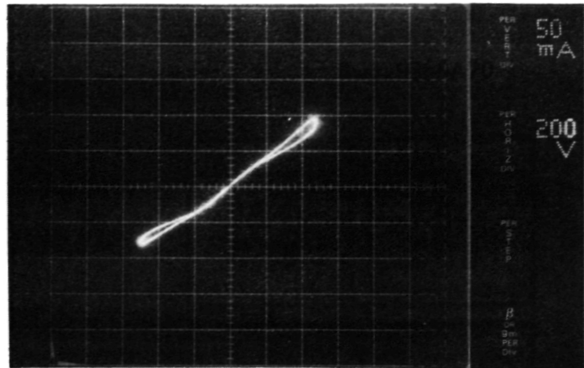
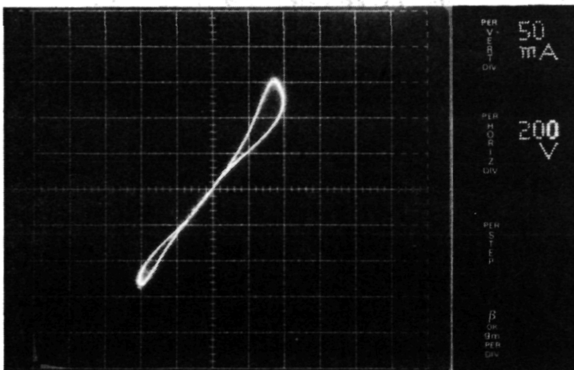


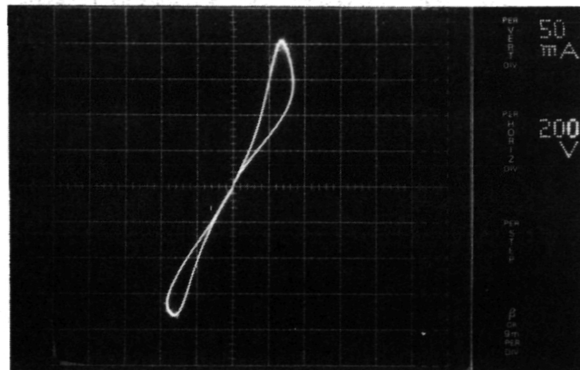
(a) Vp = 630 Volts



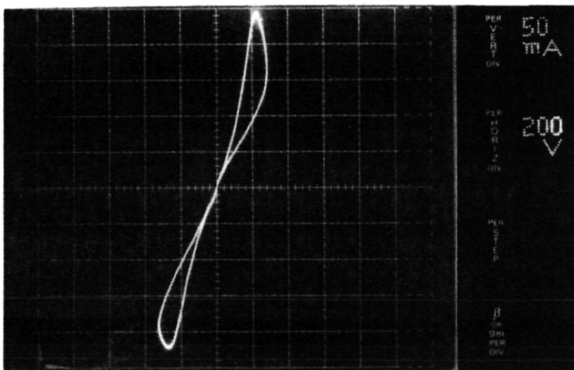
(b) Vp = 780 Volts



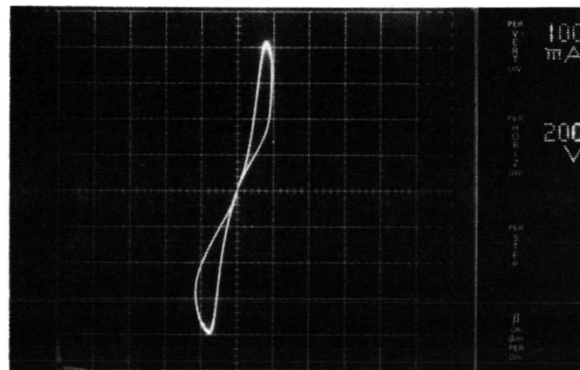
(c) Vp = 900 Volts



(d) Vp = 975 Volts



(e) Vp = 1095 Volts



(f) Vp = 1500 Volts

Figure 10. Typical I-V response of a $(DI)^2$ device classified as a poor switch to an ac curve tracer. The voltage V_p is the peak voltage of the 120 Hz rectified sine wave. Parts (a) through (e) have the vertical deflection at 50 mA/cm and the horizontal at 200 V/cm, and part (f) has the vertical at 100 mA/cm.

is about 630 V. The holding voltage is taken as the lowest voltage after the negative resistance regime and is about 80 V in Figures 9a and c. The resistance, R_B, is the blocking resistance and is measured in the blocking regime ($V < V_T$) by taking the I-V characteristics with the vertical deflection set to a more sensitive scale, e.g., 2 mV/cm.

2.5 Vertical Devices

The purpose of this section is to review some of the results that were presented in the final report[18] of the Westinghouse companion program to the NASA Contract NAS3-22247 and in the Final Report[19] for the NASA Contract. Some of these results have also been presented elsewhere.[20,21] Much of the analysis presented in this section is, however, new and was not presented in the Westinghouse report or in the NASA report. This section is necessary for the understanding of some of the material presented in Section 4.3.

2.5.1 Electron and Proton Irradiation

Radiation (electron, proton, and alpha-particle) processing typically produces many levels in silicon. In n-type material Kimerling[22] has found that the most populous defects are the electron trap E1 and the hole trap H2. The level E1 is at E_c - 10.8 eV and the level H2 is at E_v + 0.42 eV. These two defects are introduced at approximately the same rate and anneal together. As these two levels anneal with increasing temperature, another electron trap at E_c - 0.27 increases in density. Brotherton et al.[23] and Rai-Choudhury et al.[24] have found similar results, i.e., some trap densities decreasing and other trap densities increasing as the sample is annealed.

Attempts have been made to determine the levels that control the lifetime. Most authors have found that the E1 level along with the H1 (E_v + 0.28 eV) are the dominant recombination centers. However, Evwaraye and Baliga[25] have shown that the E3 (E_c - 0.41 eV) defect level is the principal recombination center that controls lifetime following

room temperature irradiation. Also, it was observed that upon annealing of the E3 defect level the minority carrier lifetime does not recover to the pre-irradiation value. This is due to the emergence of a secondary defect level, E4 (E_c - 0.35 eV), as the E3 defect level anneals out.

The effects of radiation on the resistivity values of different starting resistivity material has been measured. Table 1 shows the results of electron irradiation from which it is seen that the technique is not totally reproducible (e.g., for two samples of 100 ohm-cm with 10^{17} cm^{-2} dosage, one has a resistivity 3.5 times that of the other). However, the different results under the same conditions are not as widely varying as the results tend to be with gold diffusion.

Note the inversion from n-type to p-type conductivity with the larger dosage level. This effect has also been observed in neutron transmutation doping[26] of Si.

When the samples are annealed the resistivity drops until its value is below that of the original material (see Table 2). Note that the material remains p-type through all of this.

Proton irradiation (as shown in Table 3) has a similar effect on the resistivity, but the subsequent anneal did not drop the resistivity below that of the original material.

It appears that the annealing has reduced the density of some defect levels and increased the density of others. This is in keeping with the results from the literature that were reported above.

2.5.2 DLTS Measurements

In an attempt to characterize the deep levels by which the switching devices operate (see Section 2.5.3), DLTS measurements were made both on irradiated starting material and on PIN diodes that had been irradiated and annealed according to the schedule for switching devices. Starting material with resistivity of 100 ohm-cm, n-type, was irradiated with 2 MeV electrons with doses of 10^{15}, 10^{16}, and 10^{17} cm^{-2}.

Table 1. The effect of different doses of 2 MeV electrons on the resistivity of silicon of different starting resistivities. All samples are n-type with <111> orientation. A hot probe was used to measure the type (p or n).

Starting Resistivity	Electron Dosage	4-Point Probe, ρ	Type After Electron Dose
10	10^{16} cm^{-2}	14.4 Ω-cm	n
10	10^{17}	5.7×10^3	n
10	10^{18}	3.2×10^4	p&n
100	10^{15}	2.9×10^3	n
100	10^{15}	3.3×10^3	n
100	10^{16}	8.6×10^4	p
100	10^{16}	2.9×10^4	p
100	10^{17}	3.2×10^4	p
100	10^{17}	9.2×10^3	p
1300	10^{14}	2.9×10^3	n
1300	10^{14}	1.4×10^3	n
1300	10^{15}	5.4×10^4	n
1300	10^{15}	5.0×10^4	n
1300	10^{16}	3.8×10^5	p
1300	10^{16}	4.6×10^5	p
3000	10^{15}	5.9×10^4	p
3000	5×10^{15}	6.8×10^4	strong p
3000	10^{16}	4.5×10^4	very strong p

Table 2. Sample VT-1 was irradiated with 2 MeV electrons (dose 10^{17} cm^{-2}), then annealed six times starting at 300°, and working up to 500°, and then was irradiated again and annealed at 475°C. Sample IR 4-100 was irradiated twice, then annealed five times and then irradiated and annealed again. The samples were annealed each time for 200 minutes.

Sample: VT-1, 1300 Ω-cm (a)

Electron Rad.	Anneal Temperature						Electron Rad.	Anneal Temp.
$10^{17}cm^{-2}$	300°	350°	375°	.400°	450°	500°	$5 \times 10^{16}cm^{-2}$	475°C
ρ 3.6×10^4	3100	390	227	140	75	70.5	1.3×10^4	48
Type p	p	p	p	p	p	p	n	p

Sample: IR4-100, 100 Ω-cm (b)

Electron Rad.		Anneal Temperature					Electron Rad.	Anneal Temp.
$10^{16}cm^{-2}$	$6 \times 10^{16}cm^{-2}$	300°	350°	400°	450°	500°	$6 \times 10^{16}cm^{-2}$	475°C
ρ 1.3×10^4	8.9×10^3	1000	130	74	41	394	121	84
Type p	p	p	p	p	p	p&n	p	p

Table 3. Samples that have been irradiated with protons and then annealed at 475°C for 200 minutes. A hot probe was used to measure the type (p or n).

	Proton Irradiation			Anneal	
Starting Resistivity	Radiation Dose	4-Point Probe ρ	Type	4-point probe ρ	Type
14 Ω-cm	2.50×10^{14} cm^{-2}	2.93×10^3 Ω-cm	p&n	237 Ω-cm	n
100	2.50×10^{13}	39.70×10^3	p	545	p
100	1.25×10^{14}	8.76×10^3	p	275	p
100	2.50×10^{14}	10.30×10^3	p	147	p
1300	1.25×10^{13}	86.60×10^3	n	38.6×10^3	p
1300	2.50×10^{13}	75.90×10^3	p	11.5×10^3	n&p
1300	1.25×10^{14}	51.10×10^3	p	567	n

Schottky diodes were fabricated on the starting material and on the three irradiated samples by depositing 300 Å Ti on the silicon followed by 2000 Å of gold. The metals were evaporated through a shadow mask in order to form 30 mil Ti/Si Schottky diodes. The gold layer was used to facilitate wire bonding.

The diodes were examined on a curve tracer, and from the slope and polarity of the forward characterization, the resistivity and dopant type of the silicon substrate could be determined. Results showed that the starting material was 110 ohm-cm, n-type, while the material irradiated at 10^{15}, 10^{16}, and 10^{17} cm^{-2} was 1800 ohm-cm, n-type, 13,000 ohm-cm, p-type, and 11,000 ohm-cm, p-type, respectively. Thus, the radiation appears to be creating acceptors which first partially compensate and then overcome the initial donor concentration.

DLTS measurements on the 100 ohm-cm starting material did not indicate the presence of any trap levels. Thus, an upper bound of trap level concentration of 3×10^{10} cm^{-3} can be placed on the starting material by the detection limit of the DLTS system. Because the resistivity of the irradiated samples is so high, the Q-factor associated with the capacitance of the reverse-biased Schottky diode is too low for the capacitance meter in the DLTS system to operate properly. Consequently, DLTS measurements could not be made on the irradiated wafers.

Attempts to make DLTS measurements on a PIN diode that had been irradiated and annealed met with more success. Using 1300 ohm-cm, n-type starting material, p^+ and n^+ square regions were diffused into the front and back surface of the wafer, respectively (see Figure 16b). Aluminum was used to make contact to the n^+ and p^+ regions. The diodes were subjected to a dose of 1×10^{16} cm^{-2} of 2 MeV electrons. This was followed by an anneal of 475°C for 200 minutes in a nitrogen atmosphere. This is the same schedule that was found to lead to good switches in the deep-level switching devices fabricated on identical material. After the irradiation and anneal, the resistivity was found

to be 630 ohm-cm, a reduction of a factor of two from the 1300 ohm-cm starting material. The irradiation and anneal had thus caused the creation of additional donors. The donor concentration associated with 630 ohm-cm is 6.6×10^{12} cm^{-3}.

The results of the DLTS measurements on such a PIN diode are shown in Figure 11. Three distinct peaks are evident in each of the four temperature scans, two peaks associated with electron traps and one associated with a hole trap. The two electron traps have concentrations of $(2.2 \pm 0.3) \times 10^{12}$ cm^{-3} and $(2.3 \pm 0.1) \times 10^{12}$ cm^{-3} and positions in the bandgap of E_c - (0.17 ± 0.04) eV and E_c - (0.51 ± 0.03) eV. The position of the hole trap in the bandgap is E_v + (0.040 ± 0.006) eV, but the concentration cannot be determined because the number of holes injected into the n^- base by the forward bias pulse is not known. Since both the divacancy complex and the oxygen-vacancy complex are expected to be annealed out at 475°C, it is suspected that these levels are of some other origin. Note that one level, E_c - 0.51 eV, is near the middle of the bandgap, which is a desirable location for a recombination center. It is speculated that this level might be responsible for the improved switching characteristics in the deep-level device following the schedule of irradiation and anneal described above.

2.5.3 Vertical Switches Produced Using Irradiation

The switches produced by electron and proton irradiation without any anneal gave results similar to the devices shown in Figures 9c and 10, i.e., they were poor switches. Tables 4, 5, and 6 show results from electron irradiation (no anneal) on vertical samples made with symmetric electrodes from 1300 ohm-cm material. Tables 4a and 4b show the effects of different sample thickness, i.e., changing L. The threshold voltage, V_T, increases dramatically as the thickness increases but does not increase with L^2 as predicted by equation 12. If the threshold voltage were directly proportional to L^2 it would be 4000 V for the 40 mil sample in Table 4a (extrapolating from the 10-mil sample). In fact, the data in Table 5 indicate that the dependence is much closer to linear than

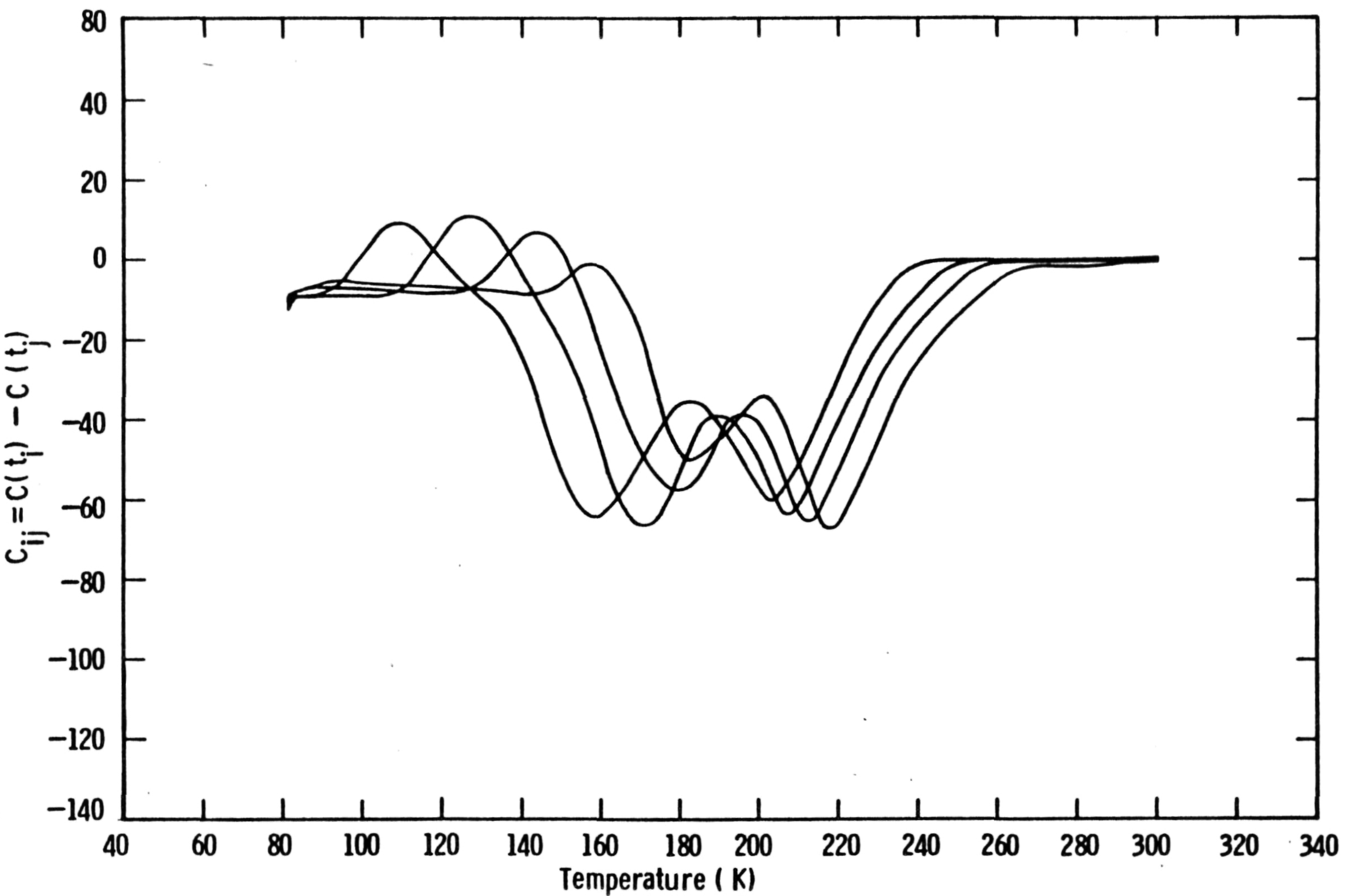


Figure 11. Deep-level transient spectroscopy (DLTS) measurement of a p-i-n diode after irradiation by 2 MeV electron (10^{16} cm^{-2}) followed by an anneal at 475°C for 200 min. Starting material was n-type 1300 ohm-cm Si.

Table 4. Vertical devices made from 1300 ohm-cm material irradiated with 2 MeV electrons at a dosage level of 6.7×10^{16} cm^{-2}. The value of V_H was taken at 400 mA on the I-V curve.

(a) The measurements were made on the smallest electrodes (500 μm × 500 μm).

Sample	Thickness	V_T	V_H	V_T/V_H	R_B
2-2	10 mil	250 V	50 V	5.0	400 kΩ
2-6	20 mil	600 V	80 V	7.5	400 kΩ
2-9	40 mil	1250 V	180 V	6.9	400 kΩ

(b) The measurements were made on the largest electrodes (2000 μm × 2000 μm).

Sample	Thickness	V_T	V_H	V_T/V_H	R_B
2-2	10 mil	300 V	40 V	7.50	300 kΩ
2-6	20 mil	480 V	80 V	6.00	300 kΩ
2-9	40 mil	750 V	200 V	3.75	400 kΩ

(c) Measurements were made on sample 2-9, which has a thickness of 40 mil.

Dimensions of Electrodes	V_T	V_H	V_T/V_H	R_B
500 μm × 500 μm	1200 V	180 V	6.7	400 kΩ
1000 μm × 1000 μm	1000 V	190 V	5.3	320 kΩ
1500 μm × 1500 μm	900 V	190 V	4.7	320 kΩ
2000 μm × 2000 μm	750 V	200 V	3.8	80 kΩ

Table 5. Vertical devices made from 1300 ohm-cm starting material that were irradiated with 2 MeV electrons. Samples 2-2, 2-6, and 2-9 were given a dose of $6.7 \times 10^{16} cm^{-2}$ and were not annealed, while sample 1-5 had a dose $10^{17} cm^{-2}$ and was annealed at 475°C

Sample	L	Anneal (475°C)	V_T	V_H	V_T/V_H
2-2	10 mil	no	250 V	50 V	5.0
2-6	20 mil	no	600 V	80 V	7.5
2-9	40 mil	no	1250 V	180 V	6.9
1-5	20 mil	yes	24 V	1 V	24.0

Sample	L	Anneal	V_T/L^2 (V/mil^2)	V_T/L (V/mil)	V_H/L^2 (V/mil^2)	V_H/L (V/mil)
2-2	10 mil	no	2.5	25	0.50	5
2-6	20 mil	no	1.5	30	0.20	4
2-9	40 mil	no	0.78	31.25	0.11	4.5
1-5	20 mil	yes	0.06	1.2	0.0025	0.05

Table 6. Vertical devices made from 1300 ohm-cm material 40 mil thick and irradiated with 2 MeV electrons. The measurements were made on the smallest electrodes (500 μm × 500 μm) and V_H was taken at 400 mA.

Dose	Sample	V_T	V_H	V_T/V_H	R_B	Test Piece	ρ	Type
None	1-8	4.8 V	2.5 V	1.9	4 kΩ	VT-1	1300 Ω-cm	n
None	2-9	6.2 V	1.8 V	3.4	6 kΩ	VT-2	1420	n
10^{14} cm^{-2}						14	2900	n
10^{15}	1-8	~200 V	~190 V	1.1	~1 kΩ	15	54000	n
10^{16}	1-8	520 V	160 V	3.3	10 kΩ	VT-2	50000	*
10^{16}	2-9	700 V	160 V	4.4	50 kΩ	16	73000	p
5×10^{16}	1-8	1040 V	160 V	6.5	~300 kΩ			
6.7×10^{16}	2-9	1250 V	180 V	6.9	~400 kΩ	VT-2	80000	p
10^{17}	1-8	1500 V	200 V	7.5	~400 kΩ	VT-1	36000	p

*didn't measure it.

quadratic for the unannealed samples. The annealed samples will be discussed later.

In Section 2.1.3 it was pointed out that equations 5 and 6 are probably not the correct ones to use for the $(DI)^2$ devices since $N_t = N_D$ and the derivation of these equations assumes $N_t << N_D$ among other things. The choice of equations for τ_n and τ_p does not, however, affect the theoretical L^2 dependence of V_T. This dependence comes from assuming that the device switches (i.e., $V = V_T$) when the hole transit time is equal to the hole lifetime (equation 9). Thus, any experimental deviation from $V_T \propto L^2$ points out problems with the assumption that the device switches when the transit time is equal to the hole lifetime and not with the choice of τ_p.

From Table 4 it seems that the ratio of threshold voltage to holding voltage, V_T/V_H, increases slightly with L for the smallest electrodes but decreases with increasing L for the largest electrodes.

The value of R_B does not seem to depend on L. This is a bit surprising since one would expect

$$R_B = \rho \frac{L}{A} \tag{18}$$

where ρ is the resistivity, L is length of the device (sample thickness), and A is the cross-sectional area of the device. Thus, the effective resistance of a device should be directly proportional to L.

When the electrode size is increased on a given sample (see Table 4c) all of the important parameters (V_T, V_H, V_T,/V_H, and R_B) deteriorate. However, the value of R_B doesn't decrease as fast as the area increases.

Table 6 shows the effect of the electron dosage level on the properties of the devices. From these results it appears that for 1300 ohm-cm silicon, the material goes from n-type to p-type for a dosage between 10^{16} and 5×10^{16} cm^{-2}, but that the properties of the device seem to get better past this dosage level. On the other hand, Figure 12

room temperature irradiation. Also, it was observed that upon annealing of the E3 defect level the minority carrier lifetime does not recover to the pre-irradiation value. This is due to the emergence of a secondary defect level, E4 (E_c - 0.35 eV), as the E3 defect level anneals out.

The effects of radiation on the resistivity values of different starting resistivity material has been measured. Table 1 shows the results of electron irradiation from which it is seen that the technique is not totally reproducible (e.g., for two samples of 100 ohm-cm with 10^{17} cm^{-2} dosage, one has a resistivity 3.5 times that of the other). However, the different results under the same conditions are not as widely varying as the results tend to be with gold diffusion.

Note the inversion from n-type to p-type conductivity with the larger dosage level. This effect has also been observed in neutron transmutation doping[26] of Si.

When the samples are annealed the resistivity drops until its value is below that of the original material (see Table 2). Note that the material remains p-type through all of this.

Proton irradiation (as shown in Table 3) has a similar effect on the resistivity, but the subsequent anneal did not drop the resistivity below that of the original material.

It appears that the annealing has reduced the density of some defect levels and increased the density of others. This is in keeping with the results from the literature that were reported above.

2.5.2 DLTS Measurements

In an attempt to characterize the deep levels by which the switching devices operate (see Section 2.5.3), DLTS measurements were made both on irradiated starting material and on PIN diodes that had been irradiated and annealed according to the schedule for switching devices. Starting material with resistivity of 100 ohm-cm, n-type, was irradiated with 2 MeV electrons with doses of 10^{15}, 10^{16}, and 10^{17} cm^{-2}.

Table 1. The effect of different doses of 2 MeV electrons on the resistivity of silicon of different starting resistivities. All samples are n-type with <111> orientation. A hot probe was used to measure the type (p or n).

Starting Resistivity	Electron Dosage	4-Point Probe, ρ	Type After Electron Dose
10	10^{16} cm^{-2}	14.4 Ω-cm	n
10	10^{17}	5.7×10^3	n
10	10^{18}	3.2×10^4	p&n
100	10^{15}	2.9×10^3	n
100	10^{15}	3.3×10^3	n
100	10^{16}	8.6×10^4	p
100	10^{16}	2.9×10^4	p
100	10^{17}	3.2×10^4	p
100	10^{17}	9.2×10^3	p
1300	10^{14}	2.9×10^3	n
1300	10^{14}	1.4×10^3	n
1300	10^{15}	5.4×10^4	n
1300	10^{15}	5.0×10^4	n
1300	10^{16}	3.8×10^5	p
1300	10^{16}	4.6×10^5	p
3000	10^{15}	5.9×10^4	p
3000	5×10^{15}	6.8×10^4	strong p
3000	10^{16}	4.5×10^4	very strong p

Table 2. Sample VT-1 was irradiated with 2 MeV electrons (dose 10^{17} cm^{-2}), then annealed six times starting at 300°, and working up to 500°, and then was irradiated again and annealed at 475°C. Sample IR 4-100 was irradiated twice, then annealed five times and then irradiated and annealed again. The samples were annealed each time for 200 minutes.

Sample: VT-1, 1300 Ω-cm (a)

Electron Rad.	Anneal Temperature						Electron Rad.	Anneal Temp.
$10^{17}cm^{-2}$	300°	350°	375°	400°	450°	500°	$5 \times 10^{16}cm^{-2}$	475°C
ρ 3.6×10^4	3100	390	227	140	75	70.5	1.3×10^4	48
Type p	p	p	p	p	p	p	n	p

Sample: IR4-100, 100 Ω-cm (b)

Electron Rad.		Anneal Temperature					Electron Rad.	Anneal Temp.
$10^{16}cm^{-2}$	$6 \times 10^{16}cm^{-2}$	300°	350°	400°	450°	500°	$6 \times 10^{16}cm^{-2}$	475°C
ρ 1.3×10^4	8.9×10^3	1000	130	74	41	394	121	84
Type p	p	p	p	p	p	p&n	p	p

Table 3. Samples that have been irradiated with protons and then annealed at 475°C for 200 minutes. A hot probe was used to measure the type (p or n).

	Proton Irradiation			Anneal	
Starting Resistivity	Radiation Dose	4-Point Probe ρ	Type	4-point probe ρ	Type
14 Ω-cm	2.50×10^{14} cm^{-2}	2.93×10^3 Ω-cm	p&n	237 Ω-cm	n
100	2.50×10^{13}	39.70×10^3	p	545	p
100	1.25×10^{14}	8.76×10^3	p	275	p
100	2.50×10^{14}	10.30×10^3	p	147	p
1300	1.25×10^{13}	86.60×10^3	n	38.6×10^3	p
1300	2.50×10^{13}	75.90×10^3	p	11.5×10^3	n&p
1300	1.25×10^{14}	51.10×10^3	p	567	n

Schottky diodes were fabricated on the starting material and on the three irradiated samples by depositing 300 Å Ti on the silicon followed by 2000 Å of gold. The metals were evaporated through a shadow mask in order to form 30 mil Ti/Si Schottky diodes. The gold layer was used to facilitate wire bonding.

The diodes were examined on a curve tracer, and from the slope and polarity of the forward characterization, the resistivity and dopant type of the silicon substrate could be determined. Results showed that the starting material was 110 ohm-cm, n-type, while the material irradiated at 10^{15}, 10^{16}, and 10^{17} cm^{-2} was 1800 ohm-cm, n-type, 13,000 ohm-cm, p-type, and 11,000 ohm-cm, p-type, respectively. Thus, the radiation appears to be creating acceptors which first partially compensate and then overcome the initial donor concentration.

DLTS measurements on the 100 ohm-cm starting material did not indicate the presence of any trap levels. Thus, an upper bound of trap level concentration of 3×10^{10} cm^{-3} can be placed on the starting material by the detection limit of the DLTS system. Because the resistivity of the irradiated samples is so high, the Q-factor associated with the capacitance of the reverse-biased Schottky diode is too low for the capacitance meter in the DLTS system to operate properly. Consequently, DLTS measurements could not be made on the irradiated wafers.

Attempts to make DLTS measurements on a PIN diode that had been irradiated and annealed met with more success. Using 1300 ohm-cm, n-type starting material, p^+ and n^+ square regions were diffused into the front and back surface of the wafer, respectively (see Figure 16b). Aluminum was used to make contact to the n^+ and p^+ regions. The diodes were subjected to a dose of 1×10^{16} cm^{-2} of 2 MeV electrons. This was followed by an anneal of 475°C for 200 minutes in a nitrogen atmosphere. This is the same schedule that was found to lead to good switches in the deep-level switching devices fabricated on identical material. After the irradiation and anneal, the resistivity was found

to be 630 ohm-cm, a reduction of a factor of two from the 1300 ohm-cm starting material. The irradiation and anneal had thus caused the creation of additional donors. The donor concentration associated with 630 ohm-cm is 6.6×10^{12} cm^{-3}.

The results of the DLTS measurements on such a PIN diode are shown in Figure 11. Three distinct peaks are evident in each of the four temperature scans, two peaks associated with electron traps and one associated with a hole trap. The two electron traps have concentrations of $(2.2 \pm 0.3) \times 10^{12}$ cm^{-3} and $(2.3 \pm 0.1) \times 10^{12}$ cm^{-3} and positions in the bandgap of E_c - (0.17 ± 0.04) eV and E_c - (0.51 ± 0.03) eV. The position of the hole trap in the bandgap is E_v + (0.040 ± 0.006) eV, but the concentration cannot be determined because the number of holes injected into the n^- base by the forward bias pulse is not known. Since both the divacancy complex and the oxygen-vacancy complex are expected to be annealed out at 475°C, it is suspected that these levels are of some other origin. Note that one level, E_c - 0.51 eV, is near the middle of the bandgap, which is a desirable location for a recombination center. It is speculated that this level might be responsible for the improved switching characteristics in the deep-level device following the schedule of irradiation and anneal described above.

2.5.3 Vertical Switches Produced Using Irradiation

The switches produced by electron and proton irradiation without any anneal gave results similar to the devices shown in Figures 9c and 10, i.e., they were poor switches. Tables 4, 5, and 6 show results from electron irradiation (no anneal) on vertical samples made with symmetric electrodes from 1300 ohm-cm material. Tables 4a and 4b show the effects of different sample thickness, i.e., changing L. The threshold voltage, V_T, increases dramatically as the thickness increases but does not increase with L^2 as predicted by equation 12. If the threshold voltage were directly proportional to L^2 it would be 4000 V for the 40 mil sample in Table 4a (extrapolating from the 10-mil sample). In fact, the data in Table 5 indicate that the dependence is much closer to linear than

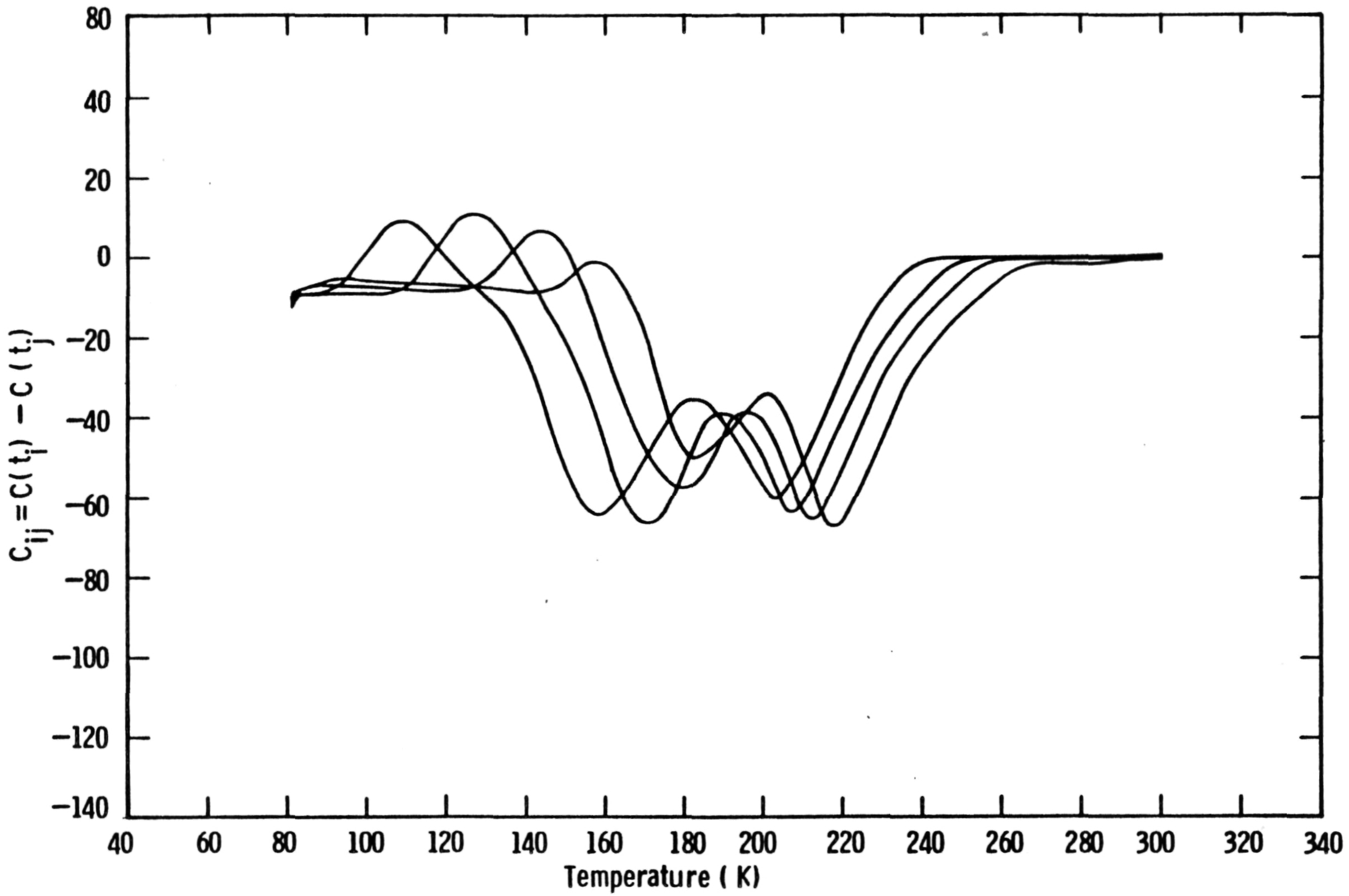


Figure 11. Deep-level transient spectroscopy (DLTS) measurement of a p-i-n diode after irradiation by 2 MeV electron (10^{16} cm^{-2}) followed by an anneal at 475°C for 200 min. Starting material was n-type 1300 ohm-cm Si.

Table 4. Vertical devices made from 1300 ohm-cm material irradiated with 2 MeV electrons at a dosage level of 6.7×10^{16} cm^{-2}. The value of V_H was taken at 400 mA on the I-V curve.

(a) The measurements were made on the smallest electrodes (500 μm × 500 μm).

Sample	Thickness	V_T	V_H	V_T/V_H	R_B
2-2	10 mil	250 V	50 V	5.0	400 kΩ
2-6	20 mil	600 V	80 V	7.5	400 kΩ
2-9	40 mil	1250 V	180 V	6.9	400 kΩ

(b) The measurements were made on the largest electrodes (2000 μm × 2000 μm).

Sample	Thickness	V_T	V_H	V_T/V_H	R_B
2-2	10 mil	300 V	40 V	7.50	300 kΩ
2-6	20 mil	480 V	80 V	6.00	300 kΩ
2-9	40 mil	750 V	200 V	3.75	400 kΩ

(c) Measurements were made on sample 2-9, which has a thickness of 40 mil.

Dimensions of Electrodes	V_T	V_H	V_T/V_H	R_B
500 μm × 500 μm	1200 V	180 V	6.7	400 kΩ
1000 μm × 1000 μm	1000 V	190 V	5.3	320 kΩ
1500 μm × 1500 μm	900 V	190 V	4.7	320 kΩ
2000 μm × 2000 μm	750 V	200 V	3.8	80 kΩ

Table 5. Vertical devices made from 1300 ohm-cm starting material that were irradiated with 2 MeV electrons. Samples 2-2, 2-6, and 2-9 were given a dose of $6.7 \times 10^{16} cm^{-2}$ and were not annealed, while sample 1-5 had a dose $10^{17} cm^{-2}$ and was annealed at 475°C

Sample	L	Anneal (475°C)	V_T	V_H	V_T/V_H
2-2	10 mil	no	250 V	50 V	5.0
2-6	20 mil	no	600 V	80 V	7.5
2-9	40 mil	no	1250 V	180 V	6.9
1-5	20 mil	yes	24 V	1 V	24.0

Sample	L	Anneal	V_T/L^2 (V/mil^2)	V_T/L (V/mil)	V_H/L^2 (V/mil^2)	V_H/L (V/mil)
2-2	10 mil	no	2.5	25	0.50	5
2-6	20 mil	no	1.5	30	0.20	4
2-9	40 mil	no	0.78	31.25	0.11	4.5
1-5	20 mil	yes	0.06	1.2	0.0025	0.05

Table 6. Vertical devices made from 1300 ohm-cm material 40 mil thick and irradiated with 2 MeV electrons. The measurements were made on the smallest electrodes (500 μm × 500 μm) and V_H was taken at 400 mA.

Dose	Sample	V_T	V_H	V_T/V_H	R_B	Test Piece	ρ	Type
None	1-8	4.8 V	2.5 V	1.9	4 kΩ	VT-1	1300 Ω-cm	n
None	2-9	6.2 V	1.8 V	3.4	6 kΩ	VT-2	1420	n
10^{14} cm^{-2}						14	2900	n
10^{15}	1-8	~200 V	~190 V	1.1	~1 kΩ	15	54000	n
10^{16}	1-8	520 V	160 V	3.3	10 kΩ	VT-2	50000	*
10^{16}	2-9	700 V	160 V	4.4	50 kΩ	16	73000	p
5×10^{16}	1-8	1040 V	160 V	6.5	~300 kΩ			
6.7×10^{16}	2-9	1250 V	180 V	6.9	~400 kΩ	VT-2	80000	p
10^{17}	1-8	1500 V	200 V	7.5	~400 kΩ	VT-1	36000	p

*didn't measure it.

quadratic for the unannealed samples. The annealed samples will be discussed later.

In Section 2.1.3 it was pointed out that equations 5 and 6 are probably not the correct ones to use for the $(DI)^2$ devices since $N_t = N_D$ and the derivation of these equations assumes $N_t << N_D$ among other things. The choice of equations for τ_n and τ_p does not, however, affect the theoretical L^2 dependence of V_T. This dependence comes from assuming that the device switches (i.e., $V = V_T$) when the hole transit time is equal to the hole lifetime (equation 9). Thus, any experimental deviation from $V_T \propto L^2$ points out problems with the assumption that the device switches when the transit time is equal to the hole lifetime and not with the choice of τ_p.

From Table 4 it seems that the ratio of threshold voltage to holding voltage, V_T/V_H, increases slightly with L for the smallest electrodes but decreases with increasing L for the largest electrodes.

The value of R_B does not seem to depend on L. This is a bit surprising since one would expect

$$R_B = \rho \frac{L}{A} \tag{18}$$

where ρ is the resistivity, L is length of the device (sample thickness), and A is the cross-sectional area of the device. Thus, the effective resistance of a device should be directly proportional to L.

When the electrode size is increased on a given sample (see Table 4c) all of the important parameters (V_T, V_H, V_T,/V_H, and R_B) deteriorate. However, the value of R_B doesn't decrease as fast as the area increases.

Table 6 shows the effect of the electron dosage level on the properties of the devices. From these results it appears that for 1300 ohm-cm silicon, the material goes from n-type to p-type for a dosage between 10^{16} and 5×10^{16} cm^{-2}, but that the properties of the device seem to get better past this dosage level. On the other hand, Figure 12

seems to indicate that in going from a dose of 5×10^{16} cm^{-2} (Figure 12e) to a dose of 10^{17} cm^{-2} (Figure 12f), the properties of the device deteriorate. There are still some inconsistencies to work out. It should be noted that some of the test pieces were not irradiated at the same time as the devices, therefore the results should only be viewed as suggestive rather than definitive.

With these devices (Tables 4, 5, and 6), whenever $R_B > 300$ K-ohm, the I-V curves tended to look like Figure 9a rather than 9c. For values of $R_B < 100$ k-ohm, the curves looked more like 9c.

Figures 12a through 12g show the effects of increasing the radiation dosage. It appears that the radiation causes defect levels that produce a poor switch and, as the concentration of defects increases, the device parameters (V_T, V_H, and R_B) improve until some sort of limit is reached (see Figure 12f: dosage $10^{17} cm^{-2}$), after which the parameters begin to deteriorate. With all the electron irradiation dosage for the devices with no anneal, there did not seem to be a critical dose that would produce a good switch.

With annealing, however, a good switch can be produced (see Figure 12ℓ). For low temperatures of annealing (Figures 12h through 12k, i.e., 300° to 450°C), the I-V parameters actually deteriorate, but at 500°C the I-V curve shows a good switch. An anneal at a higher temperature (550°C) causes the device to revert to parameters that were seen after an anneal at 450°C.

It appears (see Sections 2.5.1 and 2.5.2) that whatever defect level that causes the negative resistance behavior for the poor switches (before anneal) is annealed out as the temperature increases. At some temperature between 450°C and 475°C the density of a new level increases so that it dominates. This new level gives a good switch with a low V_H, but unfortunately it does not give a high V_T. The data in Table 5 further point out the differences between the annealed samples and unannealed samples. In each case the parameters are quite different.

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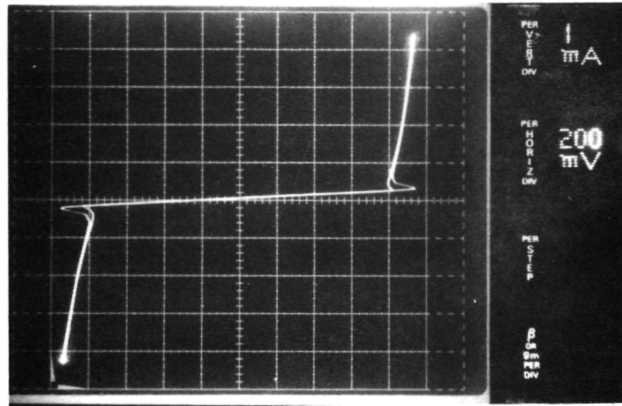
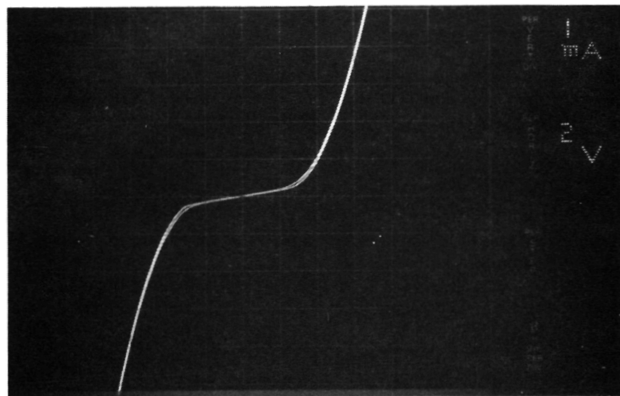
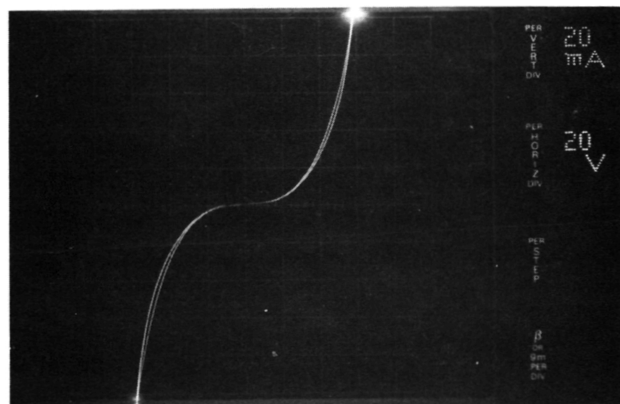


(a) No Irradiation, 1300 Ω-cm, n-Type

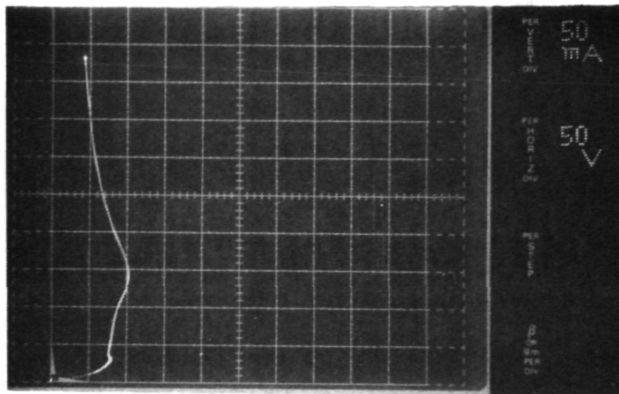


(b) 10^{15} cm^{-2}, 5.4×10^{3} Ω-cm, n-Type



(c) 5×10^{15} cm^{-2}

Figure 12. Vertical devices with symmetric electrodes made from 1300 ohm-cm starting material that have been irradiated with 2 MeV electrons. The results are from sample 1-2 (10 mil thick) and were obtained measuring a 500 μm × 500 μm square electrode. The ac type of measurement was made on (a), (b), (c), (k), and (ℓ). The rest of the measurements were of the



(d) 10^{16} cm^{-2}, 7.3×10^4 Ω-cm, p-Type

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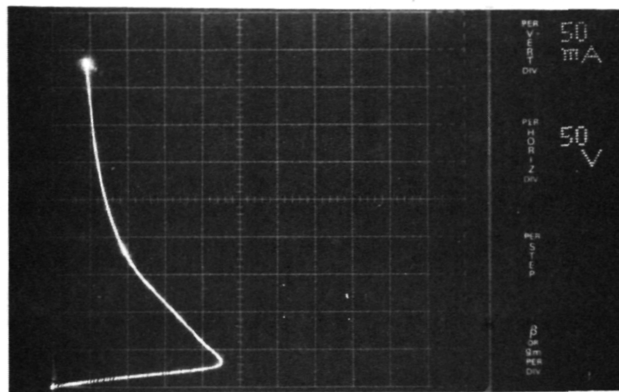
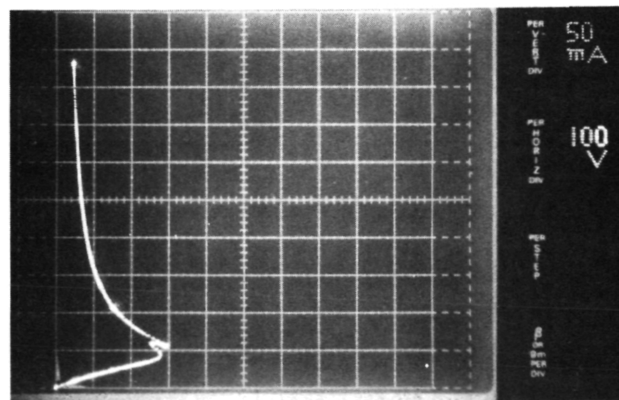
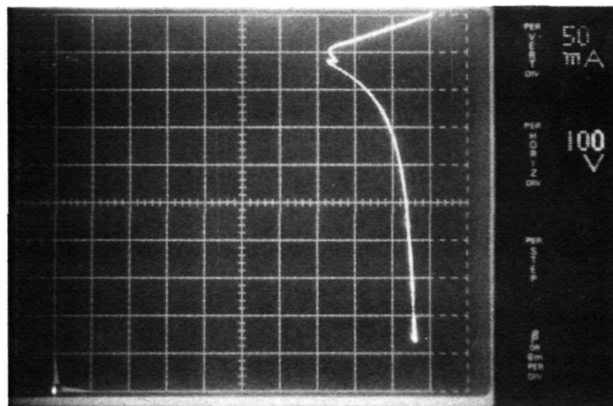


(e) 5×10^{16} cm^{-2}, 8×10^4 Ω-cm, p-Type

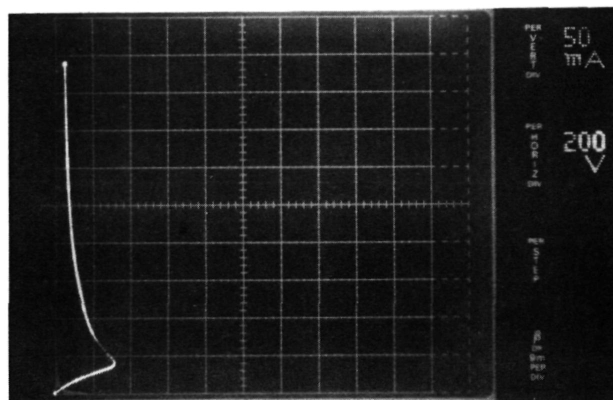


(f) 10^{17} cm^{-2}, 3.6×10^4 Ω-cm, p-Type

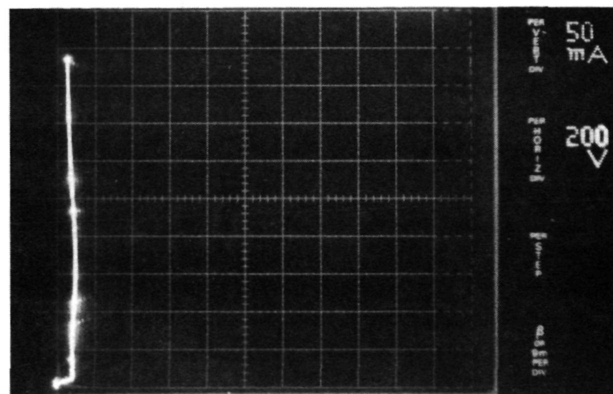
Figure 12 (Continued) dc type. All anneals were for 200 minutes with flowing N_2. Part (g) was a reverse bias measurement with respect to part (f). For part (j), the fourth anneal gave the same I-V curve as the third anneal. After the seventh anneal at 500°C, the results were essentially identical to those after the fifth anneal at 450°C.



(g) 10^{17} cm^{-2}



(h) 10^{17} cm^{-2} and Then Anneal at 300°
3100 Ω-cm, p-Type



(i) Second Anneal at 350°, 390 Ω-cm, p-Type

Figure 12 (Continued)

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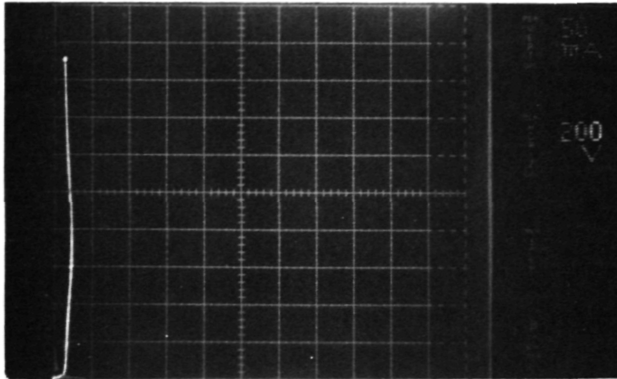
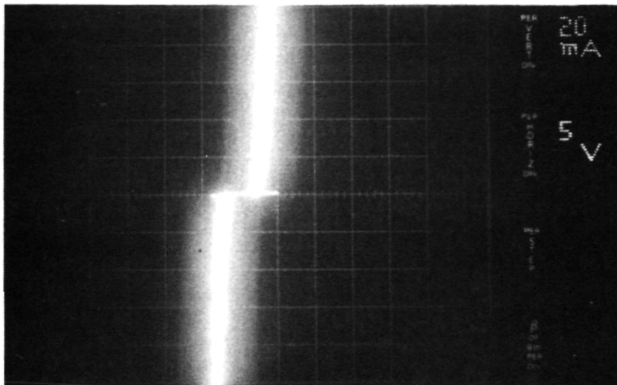
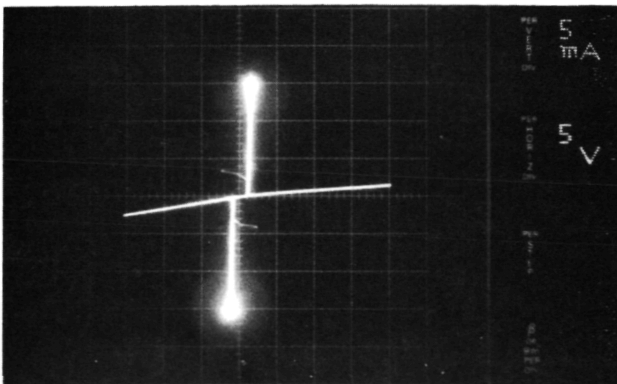


(j) Third Anneal at 375°C (227 Ω-cm, p-Type)
and the Fourth Anneal at 400°C (140 Ω-cm, p-Type)



(k) Fifth Anneal at 450°C (75 Ω-cm, p-Type)
and the Seventh Anneal at 550°C



(l) Sixth Anneal at 500°C, 70.5 Ω-cm, p-Type

Figure 12 (Continued)

The results of other experiments with electron irradiation of 1300 ohm-cm material followed by a 475°C anneal are summarized in Table 7. The I-V curves for these devices are very similar to Figure 12ℓ. The highest threshold voltage was 70 V, the lowest holding voltage was 1 V, and the best V_T/V_H ratio was 32.

Starting material of 3000 ohm-cm gave similar results to those above. From Table 8 it is seen that the holding voltage was lower (0.8 V) than with the 1300 ohm-cm material. The threshold voltage and the ratio, V_T/V_H, however, were not as good.

The results using proton irradiation (Table 9) were not good as for electron irradiation, but good switches were obtained here as well. Note that in Table 3 only the radiation dose 1.25×10^{14} for the 1300 ohm-cm sample gave a resistivity lower than the starting resistivity after irradiation and anneal. This may indicate that a higher dosage of protons than used here are needed in order to duplicate the results found from electron irradiation.

2.6 Materials Requirement

The resistivity of the starting material can have a profound effect on the resulting device. In order for the device to operate as a $(DI)^2$ switch, the density of the deep levels must be about the same as the density of donor atoms, i.e., $N_t = N_D$.

The switching time[9] seems to be proportional to $N_t L$. If this is the case then the switching time could be reduced by starting with higher resistivity material, i.e., assuming $N_t = N_D$. However, for the lateral circular devices it seemed as if better switches resulted from starting with 10 ohm-cm material than 100 ohm-cm material, but not enough cases were comparable to be definitive.

The threshold voltage is proportional to the trap density, N_t (Equation 12), thus it would seem to be better to start with a lower resistivity material so that N_t is larger when $N_t \cong N_D$. For the circular lateral device it was found that for two devices with

Table 7. Vertical devices made from 1300 ohm-cm starting material that were irradiated with 2 MeV electrons. Samples 1-2, 1-5, and 1-8 were given a dose of 10^{17} cm^{-2} and were annealed at 500°C, while samples 2-2, 2-6, and 2-9 were given a dose of 6.7×10^{16} cm^{-2} and were annealed at 475°C. Blank wafers were irradiated and annealed along with the above samples. For irradiation of 10^{17} cm^{-2} and subsequent anneal at 500°C, the blank wafer had a resistivity of 230 ohm-cm and was p-type, and the blank wafer with a dose of 6.7×10^{16} cm^{2} along with an anneal at 475°C had a resistivity of 571 ohm-cm and was also p-type. These devices were all good switches similar to Figure 12ℓ.

Sample	Thickness	Side of Square Electrode	V_T	V_H	V_T/V_H
1-2	10 mil	500 μm	20.0 V	1.0 V	20.0
1-2	10 mil	2000	32.0 V	1.0 V	32.0
1-5	20 mil	500	14.0 V	2.0 V	7.0
1-5	20 mil	2000	24.0 V	1.0 V	24.0
1-8	40 mil	500	70.0 V	15.0 V	4.7
1-8	40 mil	2000	70.0 V	5.0 V	14.0
2-2	10 mil	500	11.0 V	1.2 V	9.2
2-2	10 mil	2000	17.0 V	1.0 V	17.0
2-6	20 mil	500	12.2 V	2.0 V	6.1
2-6	20 mil	2000	18.0 V	1.0 V	18.0
2-9	40 mil	500	20.0 V	10.0 V	2.0
2-9	40 mil	2000	26.0 V	3.0 V	8.7

Table 8. Vertical devices made from 3000 ohm-cm starting material 15 mil thick that were irradiated with 2 MeV electrons and annealed at 475°C. Resistivity measurements were made on blank wafers that were irradiated and annealed along with the samples. These devices were all good switches similar to Figure 12ℓ.

Sample	Electron Radiation Dose	ρ (after)	type (after)	Side of Square Electrode	V_T	V_H	V_T/V_H
3-1	10^{15} cm^{-2}	8.8×10^3 Ω-cm	p&n	500 μm	4.8 V	1.0 V	4.80
3-1	10^{15} cm^{-2}	8.8×10^3	p	2000	1.4 V	0.8 V	1.75
3-2	5×10^{15} cm^{-2}	1500 Ω-cm	p	500	9.0 V	1.0 V	9.00
3-2	5×10^{15} cm^{-2}	1500 Ω-cm	p	2000	10.0 V	0.8 V	12.50
3-3	10^{16} cm^{-2}	670 Ω-cm	p	500	10.8 V	0.8 V	13.50
3-3	10^{16} cm^{-2}	670 Ω-cm	p	2000	2.0 V	1.2 V	1.70

Table 9. Vertical devices made from 1300 ohm-cm starting material that were irradiated with 12 MeV protons. The anneal temperature was 475°C. Resistivity measurements were made on blank wafers that were irradiated and annealed along with the samples.

Sample (thickness)	Proton Radiation Dose	ρ (after)	type (after)	Side of Square Electrode	V_T	V_H	V_T/V_H
1-1 (10 mil)	1.25×10^{13} cm^{-2}	38,600 Ω-cm	p	500 μm	11.0 V	1.2 V	9.2
1-1 (10 mil)	"	"		2000	2.6 V	0.8 V	3.3
1-4 (20 mil)	"	"		500	19.0 V	3.0 V	6.3
1-4 (20 mil)	"	"		2000	1.6 V	1.0 V	1.6
1-7 (40 mil)	"	"		500	no negative resistance		
1-7 (40 mil)	"	"		2000	22.0 V	3.0 V	7.3
2-1 (10 mil)	2.5×10^{13} cm^{-2}	11,460	p	500	4.8 V	0.9 V	5.3
2-1 (10 mil)	"	"		2000	2.0 V	0.8 V	2.5
2-4 (20 mil)	"	"		500	10.0 V	1.0 V	10.0
2-4 (20 mil)	"	"		2000	1.2 V	0.7 V	1.7
2-7 (40 mil)	"	"		500	40.0 V	9.0 V	4.4
2-7 (40 mil)	"	"		2000	17.0 V	2.0 V	8.5
2-5 (20 mil)	1.25×10^{14} cm^{-2}	567	p	500	23.0 V	4.0 V	5.8
2-5 (20 mil)	"	"		2000	5.2 V	1.2 V	4.3
2-8 (40 mil)	"	"		500	28.0 V	6.0 V	4.7
2-8 (40 mil)	"	"		2000	9.0 V	1.0 V	9.0

comparable switching properties, the 10 ohm-cm starting material device had V_T = 1250 V and the 100 ohm-cm device had V_V = 820 V. Both devices were gold diffused (at different temperatures) with $N_t \cong N_D = 4 \times 10^{14}$ cm^{-3} for the 10 ohm-cm material and $N_t \cong N_D = 4 \times 10^{13}$ cm^{-3} for the 100 ohm-cm material.

Thus, it seems that there are divergent requirements for the resistivity of the starting material if one wishes to optimize the two important parameters, V_T and switching time. However, before anything definitive can be said much more analysis and experimentation must be done.

On a practical note with respect to electron radiation, if one started with a 10 ohm-cm sample the dose would have to be on the order of 10^{19} cm^{-2} in order to have the requisite density of deep levels (see Table 1). The 10^{18} cm^{-2} dose took two working days (~16 hours) for one wafer with the Van DeGraaff at Westinghouse, and a 10^{19} cm^{-2} dose would therefore be prohibitive in time and money. This is the main reason 1300 ohm-cm material was used for the vertical devices.

3. DEVICE DESIGN AND PROCESSING

3.1 Background

In the design of a high-power $(DI)^2$ device the main emphasis has been on trying to increase V_T, decrease V_H, decrease the switching time, trigger the device with either a MOS gate or an injection gate, and to increase the off resistance of the device. One of the main concerns has been to try to decrease V_H while at the same time increasing V_T. Theoretical results such as Equation 17 seem to hold little promise for this unless one can find a deep level where $\sigma_p >> \sigma_n$. This is why methods such as proton and electron irradiation were tried along with Au doping.

The success of Shieh and Henderson[15] at the University of Cincinnati with their SADIS design (see Section 2.2) led to the design of the devices with symmetric electrodes.

In order to prevent bulk breakdown or surface breakdown before the voltage on the device reaches V_T, one of the lateral designs has a circular configuration. This device can have either a gate (either MOS or injection) or a guard ring. There is also a vertical design because it allows higher voltage and current capabilities than planar designs. The vertical design does not have any gates. A third device design, lateral rectangular, attempts to examine the dependence of V_T on channel length. This design also has MOS and injection gates.

3.2 Mask Designs

3.2.1 Lateral Circular Design

This design has symmetric electrodes and the anode, cathode, and gate are concentric (Figure 13). The devices can be made with one of

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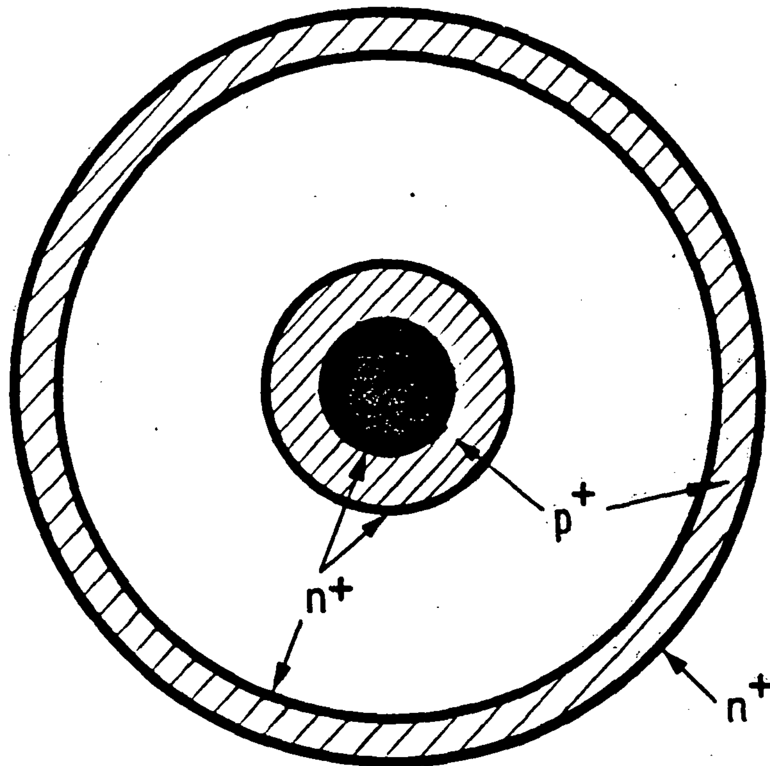

Figure 13. Top view of the lateral circular device shown without the gate. When the gate is present it is concentric with the anode and cathode. The shaded area is p^+ (boron) and the dark area is n^+ (phosphorus).

the following: (1) no gate, (2) MOS gate, (3) injection gate, or (4) guard ring. For the injection gate the diffusion is done at the same time as the p^+ diffusion, and for the guard ring it is done with the n^+ diffusion. The anode-cathode spacing, L, is 30 mils and the cathode-gate spacings are 5, 10, and 15 mils. A cross-sectional view of the device with a MOS gate is shown in Figure 14.

3.2.2 Vertical Design

With this design the current flows vertically through the device, which should allow higher current values to be obtained than with the lateral designs. The top view is shown in Figure 15, and a cross-sectional view of the symmetric electrodes and the p-i-n devices is shown in Figure 16.

The first two masks used (one on top and one on the bottom) are aligned using the infrared aligner. From that point on conventional methods are used to align the masks on their respective sides. Thus, there are two boron diffusion masks (one for the top and one for the bottom) and two masks then for each of the other steps, phosphorus diffusion, etc. For the p-i-n device (Figure 16b) only the boron masks were used, i.e., the top boron mask was used for the boron diffusion and the bottom boron mask was used for the phosphorus diffusion.

3.2.3 Lateral Rectangular Design

This design was made to study the effects of gates, electrode spacing, and electrode area in a lateral configuration. Figure 17 shows the metallization pattern for all the devices on one wafer. Note that some of the devices have gates and others do not. The spacings, L (see Figure 18) between electrodes are 5, 10, 15, 20, and 25 mils. The lengths, ℓ, of the electrodes are 10, 30, and 90 mils. Those devices with 10 mil electrodes, however, have 30 mil metallization pads. The first five devices (upper left-hand corner of Figure 17) have the dimensions: L = 5 mil and $\ell \times W$ = 10 mil $\times$ 4 mil, 10 mil $\times$ 8 mil,

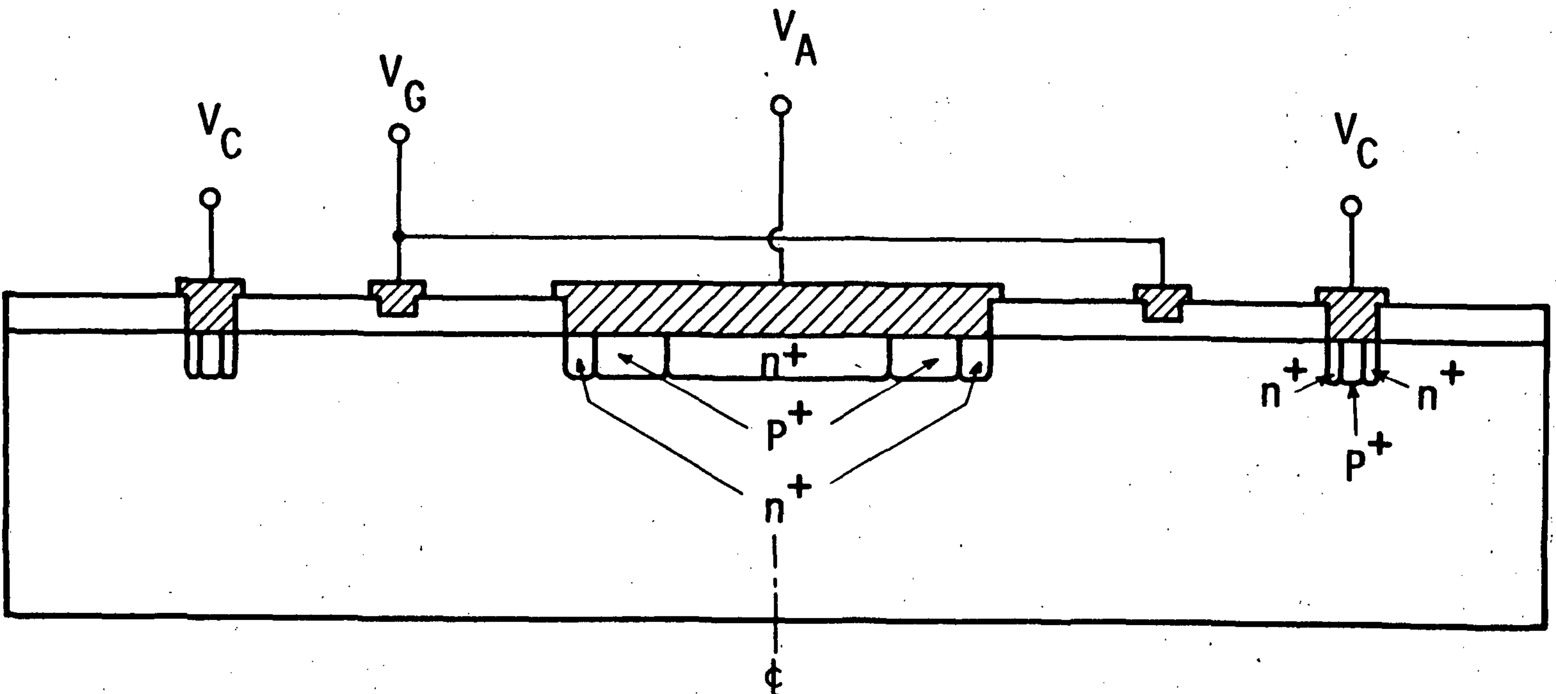

Figure 14. Cross section of the circular lateral device with a MOS gate.

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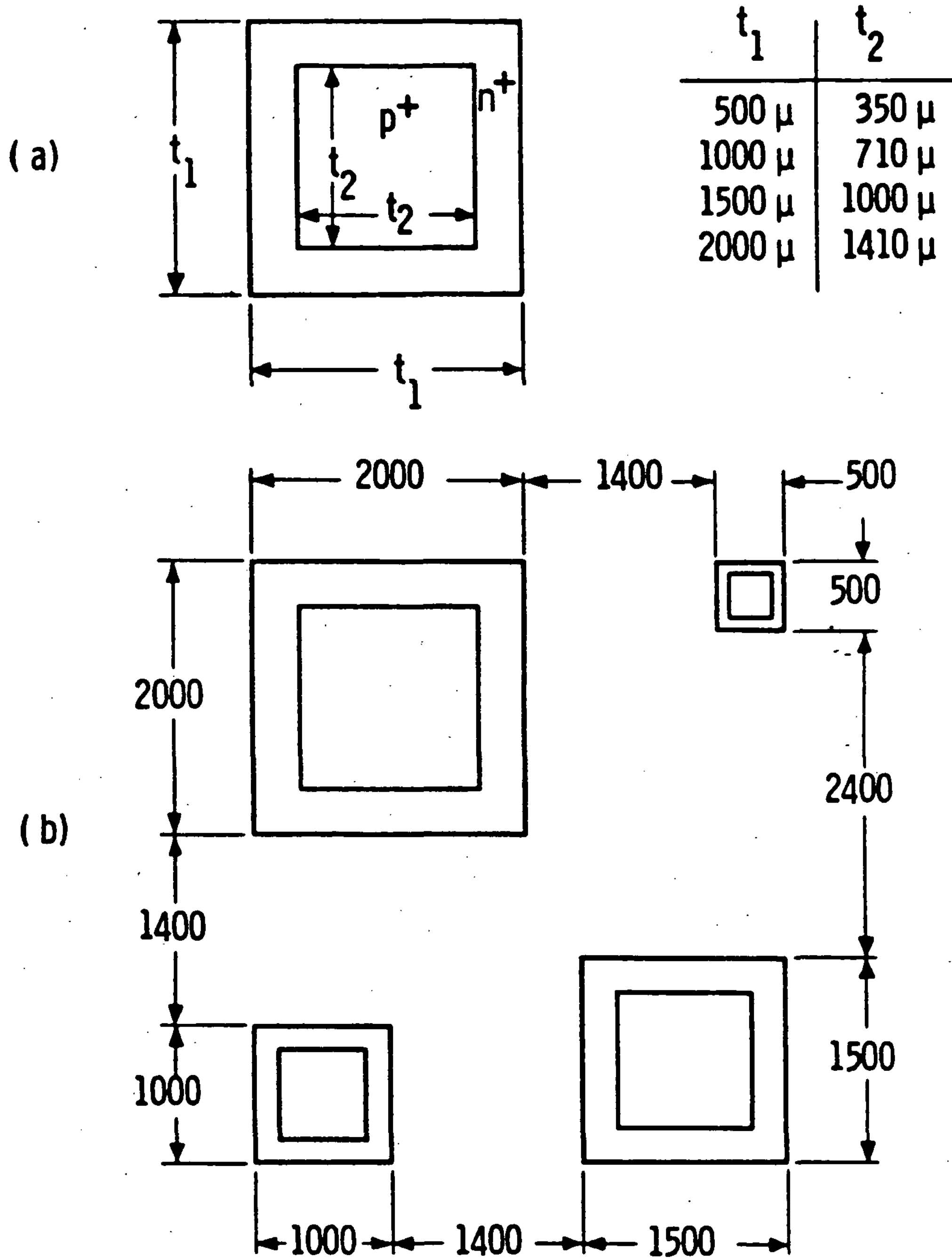

t_1	t_2
500 μ	350 μ
1000 μ	710 μ
1500 μ	1000 μ
2000 μ	1410 μ

Figure 15. (a) Top view of the symmetric electrode for the vertical device. The area of the phosphorus diffusion ($t_1^2 - t_2^2$) is equal to the area of the boron diffusion (t_2^2). For the p-i-n diode, only the boron masks would be used so the dimensions of these electrodes would be given by t_2. (b) One cell consists of four electrodes of different areas. There are nine cells (3 × 3) with 1400 μm spacing between cells.

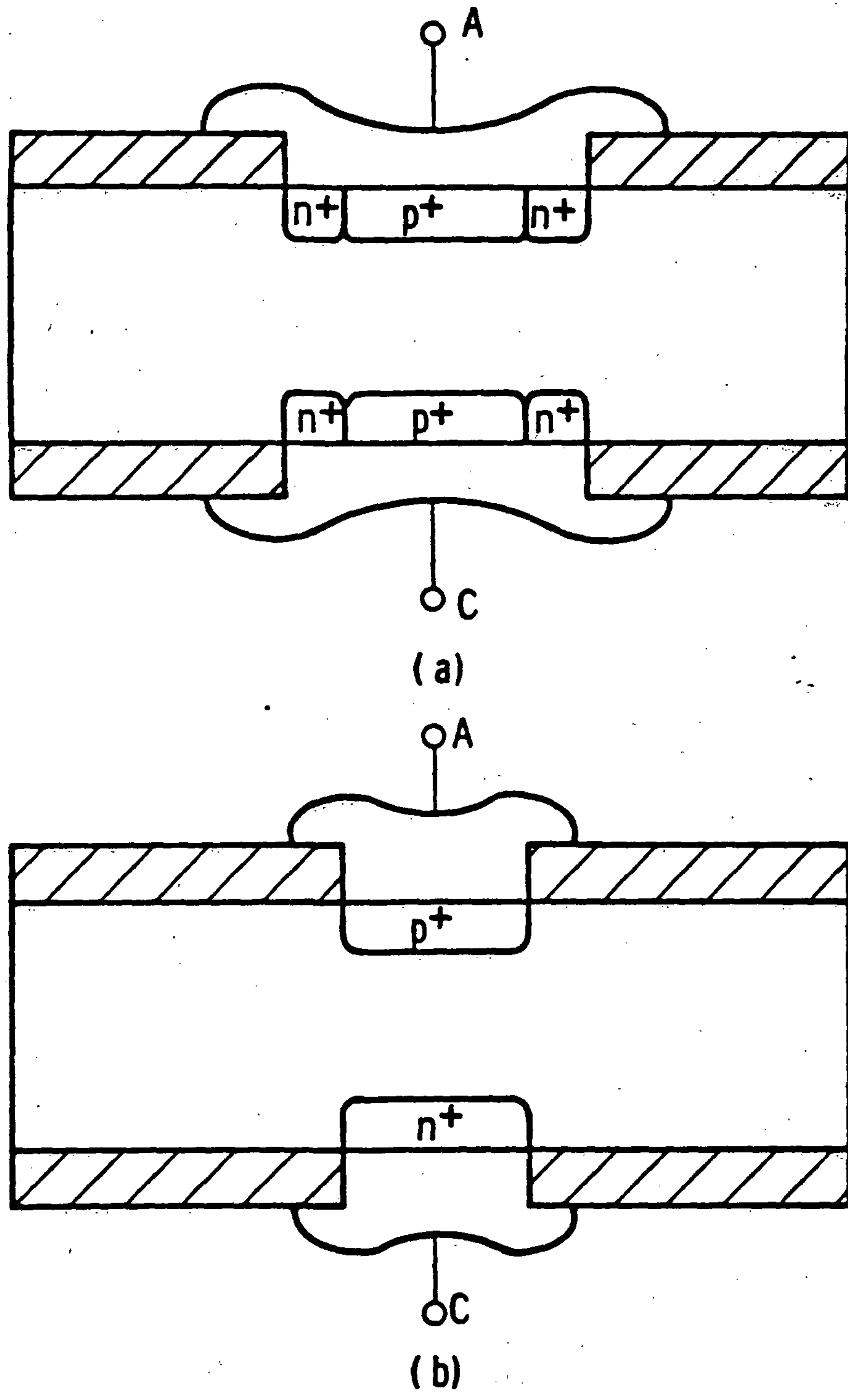

Figure 16. Vertical $(DI)^2$ devices: (a) symmetric electrode design and (b) p-i-n design.

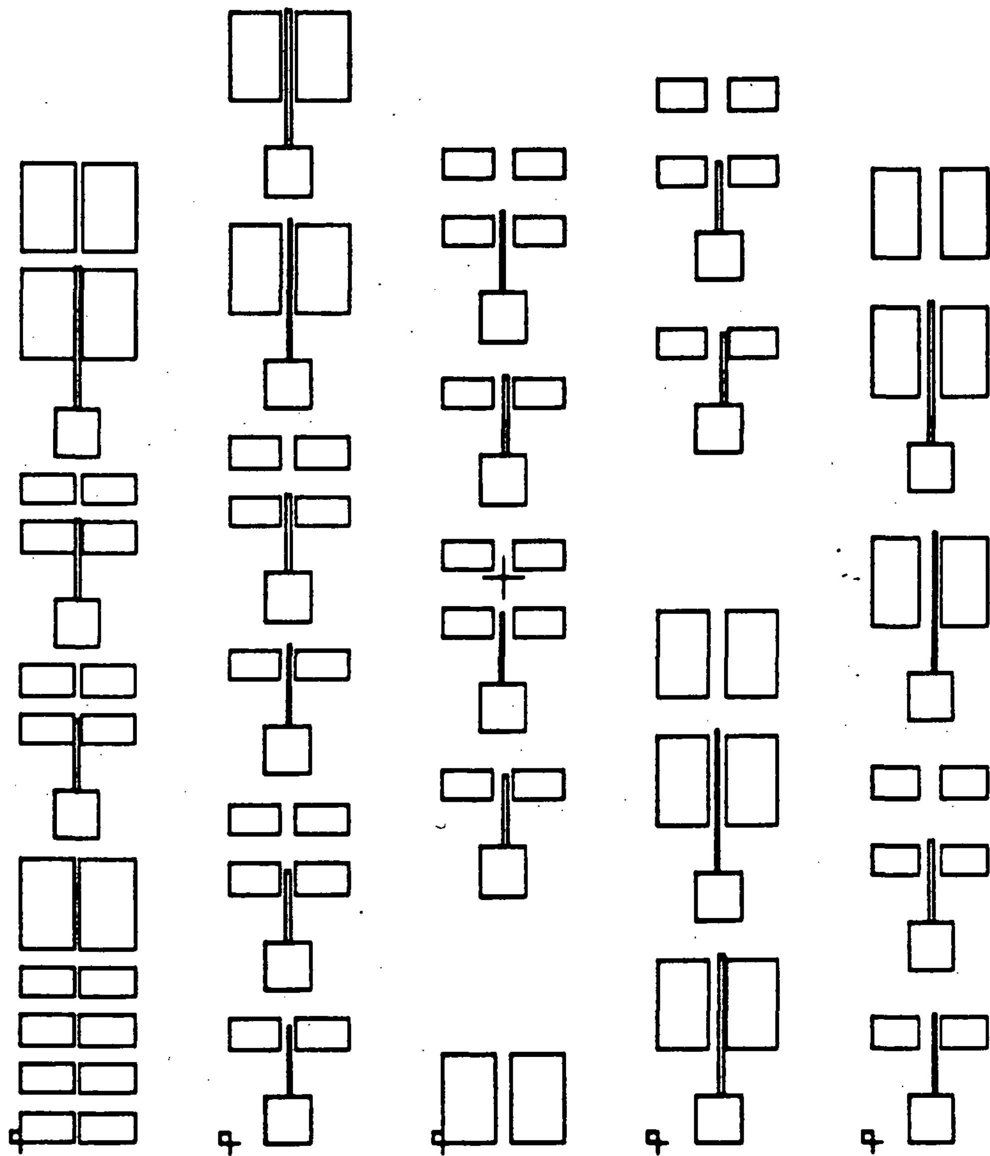

Figure 17. Metallization pattern for the lateral rectangular design.

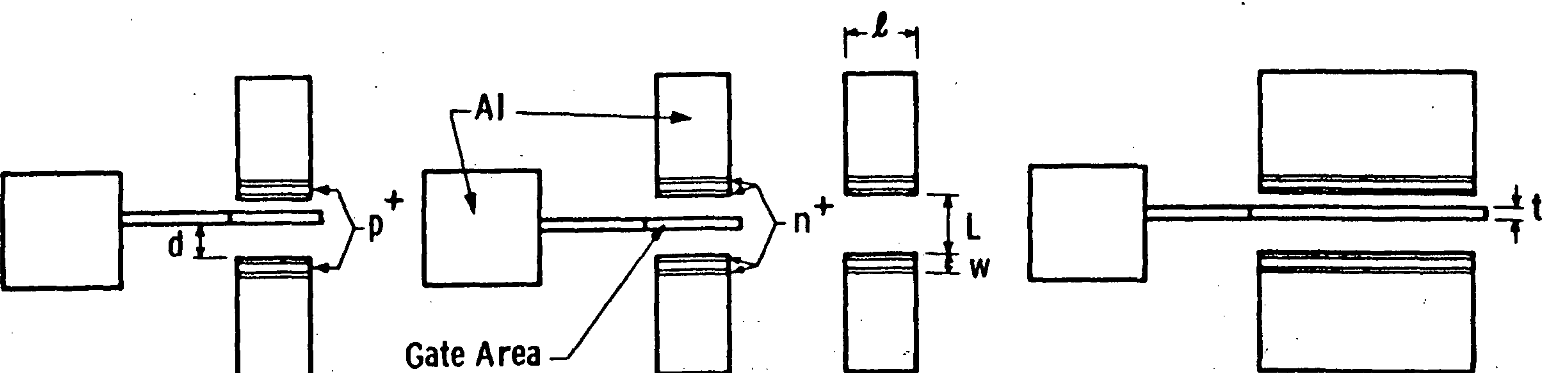

Figure 18. Some representative devices from the lateral rectangular design. The electrodes are all symmetric. The metallization patterns cover the electrodes and then extend out further in order to make probe contact easier.

10 mil × 16 mil, 30 mil × 8 mil, and 90 mil × 8 mil. All other electrodes have width W = 8 mil. For the definition of L, ℓ, and W see Figure 18. The electrodes are all symmetric.

The gates on one wafer all have the same width, t. There are two possible choices for t: 2.4 and 4.8 mil. The gates can be either MOS or injection (p^+ doping). If the boron and phosphorus diffusions are interchanged, then the gate area would be n^+ and would essentially be a guard area which might increase V_T without affecting V_H. Also the gates are positioned at various distances, d, from the electrodes.

3.2.4 Deep-Level Gettering Mask Design

It is known that high concentrations of phosphorus and boron tend to getter gold.[27] In order to check out the gettering by phosphorus and boron on deep levels due to gold, a two-mask set was made (see Figure 19).

3.3 Device Processing

3.3.1 Lateral Device Processing

A processing flow diagram is shown in Figure 20 for lateral devices without gates. The steps are all conventional silicon processing procedures.

Figure 21 shows the change necessary to produce MOS gates. The injection gates are produced as shown in Figure 22. The gates are diffused at the same time as the p^+ diffusion of the electrodes.

In order to produce a guard ring the gate area is diffused at the same time as the n^+ diffusion areas.

3.3.2 Vertical Device Processing

The vertical devices can be made with either symmetric electrodes or with the p-i-n design. The processing flow diagrams for both devices are shown in Figure 23.

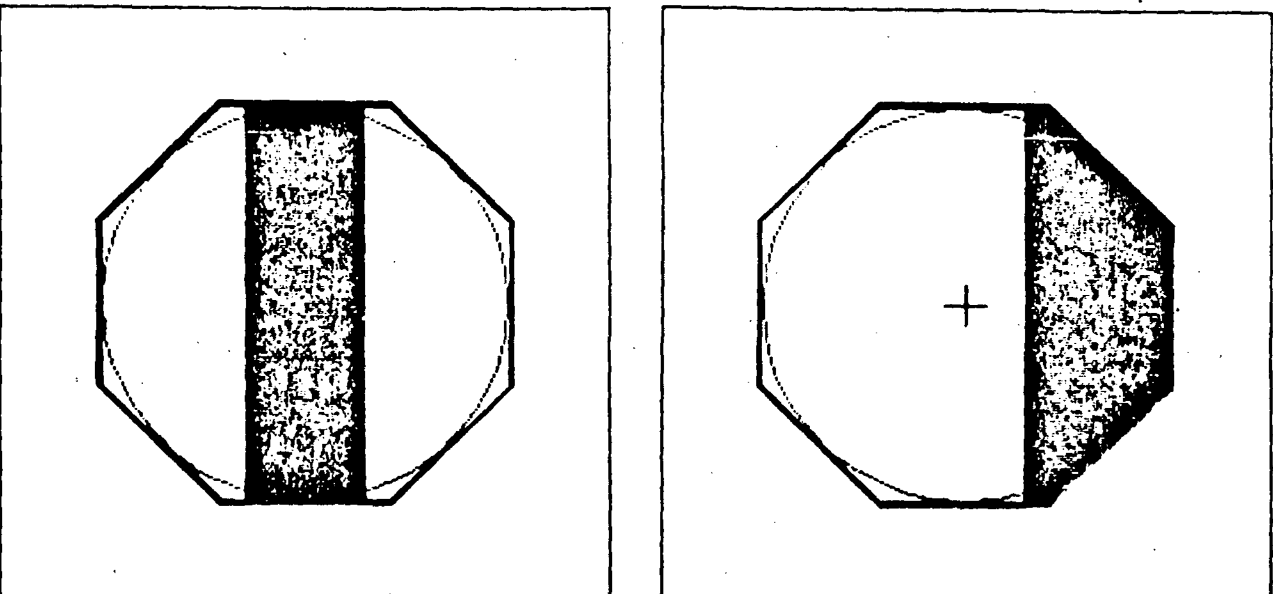

Figure 19. Mask set used to investigate the gettering effects of boron and phosphorus on deep levels caused by gold. Mask (a) is for the boron diffusion and mask (b) is for the phosphorus diffusion.

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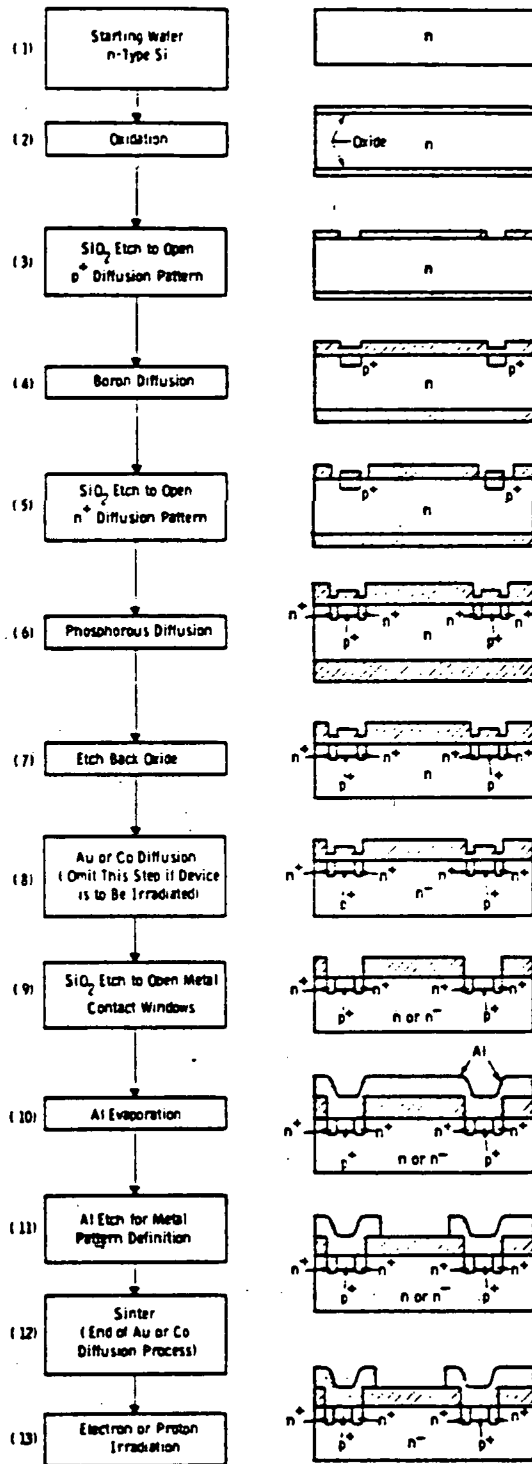

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Figure 20. Processing flow sheet with the device cross section for the lateral devices. For devices with Au or Co diffusion the process includes all the steps through step 12. For devices with irradiation the process goes through step 13 and omits step 8.

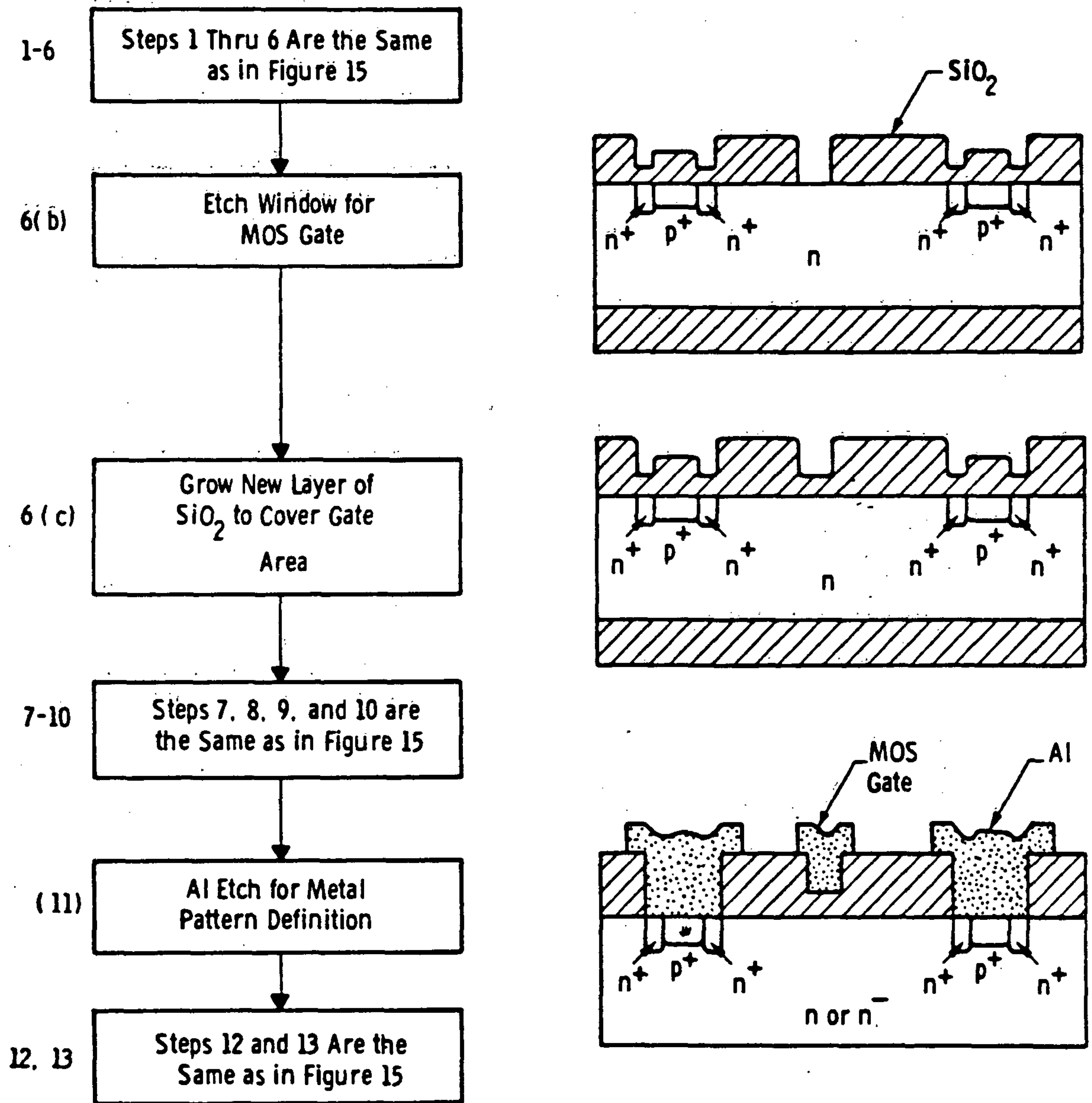

Figure 21. Processing flow sheet with the device cross section for the lateral devices with MOS gates. Steps 6(b) and 6(c) are added to those in Figure 20 and a new mask is needed for the metal etch.

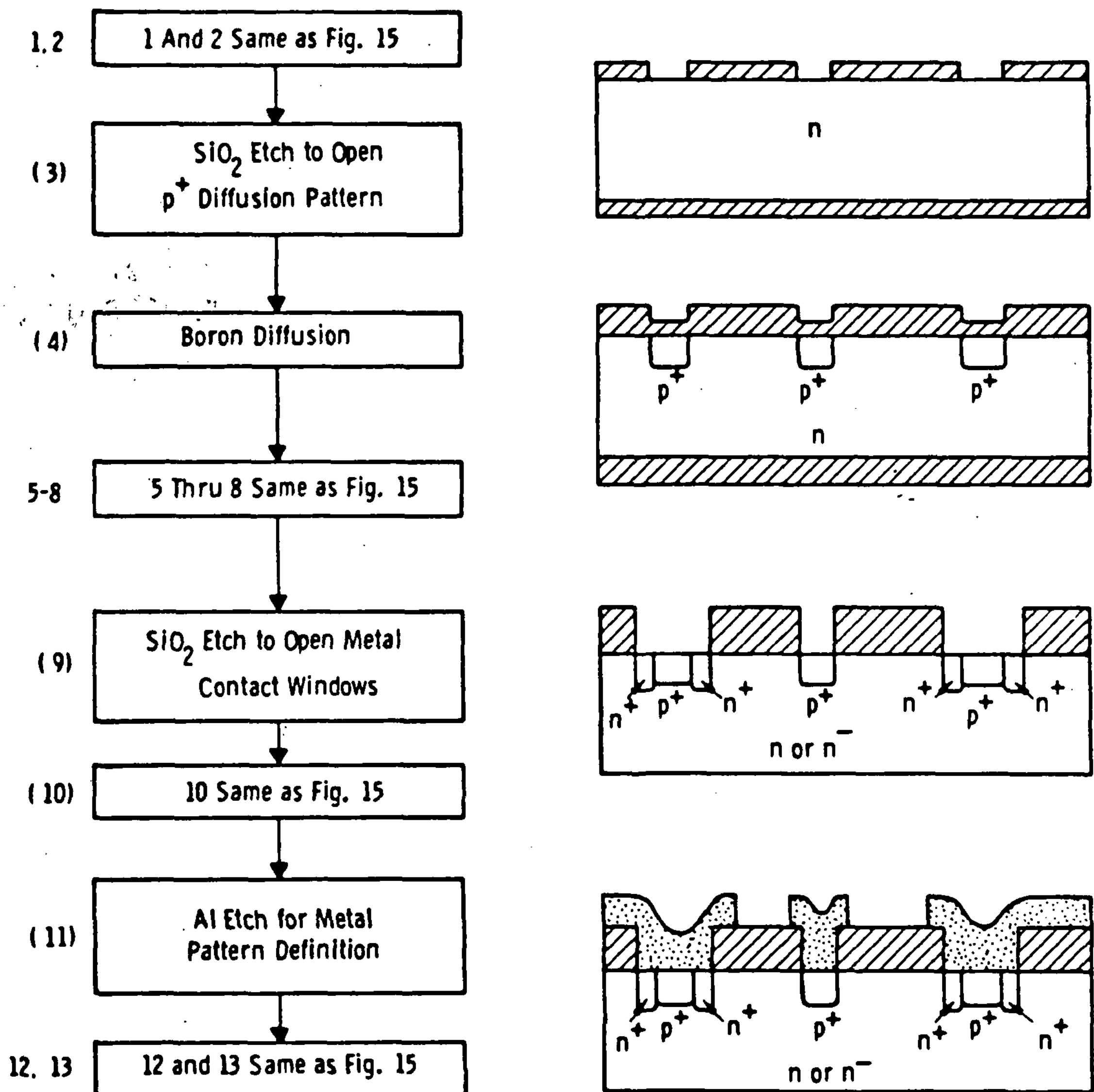

Figure 22. Processing flow sheet with the device cross section for the lateral devices with injection gates. Steps 3, 9, and 11 require new masks.

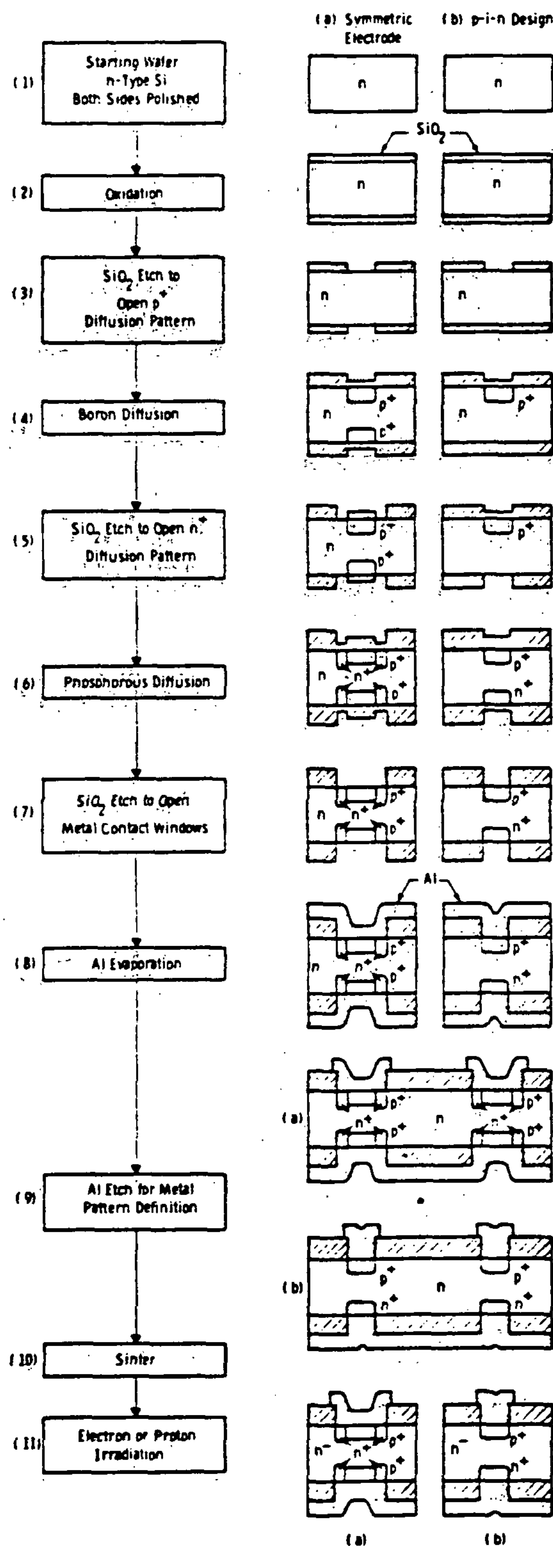

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Figure 23. Processing flow chart with device cross sections for the vertical $(DI)^2$ devices: (a) symmetric electrode design and (b) p-i-n design.

Since both sides of the wafer are covered with an oxide, diffusion techniques cannot be used to introduce the deep levels. These devices are subsequently irradiated with either electrons or protons.

The Al was not etched on one side and therefore covers the entire side of the wafer. This was done to enable contact to the devices. The bottom of the device is in contact with a large cylinder of Al when under test. This was not felt to affect the behavior of the devices since the effective spacing between an anode and a cathode not directly underneath is too long for the device to switch with respect to that cathode before it switches with respect to the cathode directly beneath the anode under test.

3.3.3 Gold Diffusion

For the purpose of this report the University of Cincinnati method of gold diffusion will be referred to as method #1. Methods #2 and #3 were developed at Westinghouse.

3.3.3.1 Method #1 for Gold Diffusion

Henderson and co-workers at the University of Cincinnati Solid State Electronics Laboratory have been using an indirect-source open-tube diffusion technique for their gold diffusion. This is a method they developed specifically to produce double-injection devices.

A gold silica film is painted on the front surface of a wafer which then becomes the source wafer. The source wafer is placed approximately 2 mm from the sample wafers to accomplish the desired diffusion. The direct paint-on technique (putting silicon paint on the sample wafer) was used early in the program but was replaced by the indirect method, which gives better control of the gold diffusion along with the ability to attain lower gold concentrations than were possible with the direct method. Also, the indirect-source diffusion technique gives a clean and uniform diffusion and obviates the difficulty of cleaning the gold silica film off the wafer.

Care must be taken in the production of the source wafer itself. For example, the first time a source wafer is used it will not give off as much gold (consequently lowering the gold concentration in the sample wafer) because a significant amount of gold diffuses into the source wafer itself. After being used a few times the outgassing of gold from the source wafer becomes a constant. Thus, the knowledge of the history of a source wafer becomes important.

Four different parameters that could possibly affect the gold diffusion using the indirect method were measured by Rungseanuvtagul.[28] These were (1) nitrogen flow rate, (2) wafer spacing, (3) diffusion time, and (4) diffusion temperature. The nitrogen flow rate was found to have almost no effect over the range of 200 cc/min to 1300 cc/min. The wafer spacing caused almost no change over a range of 0.5 mm to about 5 mm. Diffusion time did have an effect on the concentration but leveled off at about 1.5 to 2.0 hours. The effect of different temperatures had the most consequence.

The "method #1" used at Westinghouse is essentially the same as described above with the exception that the gold silica was spun on in the same way that photoresist is spun on.

3.3.3.2 Methods #2 and #3

Method #2 is defined as the deposition of a gold film onto the back of the device wafer and then gold diffusion in the furnace at a prescribed temperature. The wafer is cooled after the gold diffusion by pulling it from the furnace into the air.

Method #3 uses the same gold deposition technique as above, but the cooling after gold diffusion is quite different. In this case the wafer is quenched by dropping it directly into water. There is evidence to indicate that this "freezes" the gold at the substitutional sites.

3.3.3.3 Thickness of Gold Film for Diffusion

In choosing a thickness for the gold layer on the back of the device wafer, there must be enough gold to cause compensation of the phosphorus donors. Let us first make a calculation of what the gold concentration would be in the silicon wafer if all the gold were to diffuse into the silicon. The volume of a unit cell of gold is (4.08 Å),[3] and since gold is FCC there are 4 atoms per unit cell. Thus, the density of gold is 5.89×10^{22} atoms/cm^3. Assuming the gold is 200 Å thick, the volume of a one cm^2 area of the gold film would be 2×10^{-2} cm^3. The number of gold atoms/cm^2 in 200 Å of gold is 1.18×10^{17} atoms. The volume of a 10 mil wafer one cm^2 in area is 2.54×10^{-2} cm^3. If all the gold atoms were to diffuse into the silicon, the density of gold atoms/cm^3 in the silicon would be

$$\frac{1.18 \times 10^{17} \text{ Au atoms}}{2.54 \times 10^{-2} \text{ cm}^3} = 4.6 \times 10^{18} \text{ Au atoms/cm}^3. \qquad (19)$$

A 20 ohm-cm silicon wafer has a phosphorus density of 2×10^{14} cm^{-3}, thus the gold density needed for compensation would be 2×10^{14} cm^{-3}, and

$$\frac{4.6 \times 10^{18} \text{ Au atoms/cm}^3}{2 \times 10^{14} \text{ Au atoms/cm}^3} = 2.3 \times 10^4. \qquad (20)$$

This ratio would seem to be sufficient to ensure compensation of the silicon.

4. RESULTS

4.1 Gold Diffusion

4.1.1 Method #1 for Gold Diffusion

A series of gold diffusions was undertaken in order to establish the parameters for successful gold doping. Method #1 (the indirect source method developed at the University of Cincinnati) was used. The gold diffusion in silicon was investigated at different temperatures (950°, 1000°, 1050°, 1100°, and 1138°C) and for samples of different starting resistivities (10 ohm-cm and 100 ohm-cm). The results are shown in Table 10 and Figures 24 and 25, which were also reported in References 18 and 19 and are repeated here for completeness. For a given resistivity there seems to be a diffusion temperature that results in a flat profile. For a starting resistivity of 10 ohm-cm, the flat profile seems to occur between 1050° and 1100°C (see Figure 24). For a different source wafer it was found that flat profiles were obtained at 1100°C. A starting resistivity of 100 ohm-cm, on the other hand, seems to give a flat profile at 1000°C diffusion temperature. When analyzing these curves it is important to remember that when the material is n-type, the higher the gold concentration the higher the resistivity; however, when the gold concentration becomes larger than the n-type impurity and the material actually inverts (i.e., changes from n-type to p-type), the higher the gold concentration the lower the resistivity. It has been established through profile measurements using radioactive gold[29] and spreading resistance[30] that there is a higher concentration of gold near the surface, whatever the gold concentration happens to be. Thus, when the resistivity near the surface has a negative slope, the material is still n-type, and when the resistivity near the surface has a positive slope, the material has switched to p-type.[30] Assuming one wishes intrinsic material, then a good

Table 10. Gold diffusion in Si at 1100°C for one hour (2-inch diameter, ~12.0 mil <111>, n-type).

	RESISTIVITY			
	4-Point Probe		Spreading Resistance	
Sample Number	Before Diffusion	After Diffusion	Before Diffusion	After Diffusion
1	9.8 Ω-cm	2.40×10^4 Ω-cm	10.0 Ω-cm	5.5×10^3 Ω-cm
2	9.1	2.60	9.5	5.3
3	6.2	.81	6.4	4.5
4	8.2	1.02	10.0	4.0

starting point for gold diffusion temperatures would seem to be about 1100°C for 10 ohm-cm material and 1000°C for 100 ohm-cm material.

Devices were made at the gold diffusion temperatures mentioned above and the results were mixed. High-threshold voltages were obtained (~ 1400 volts) but the devices would not switch fast enough in order to have useful applications. It was then decided to study the gold diffusion process further. Tables 11 and 12 show the results of trying many different gold diffusion temperatures with 14 ohm-cm material. The results show almost no correlation between resistivity and diffusion temperature, except that the temperatures 1138°C and 1130°C are probably too high for good results. The devices tested on these wafers all gave about the same results except 18-9, which gave the best results. The devices on sample 18-9 had the highest V_T (~ 1200 V) and were the fastest switches, though they would still be classified as "better" switches and not as "good" switches. From this data it appears that the material should have as high a resistivity as possible while still n-type.

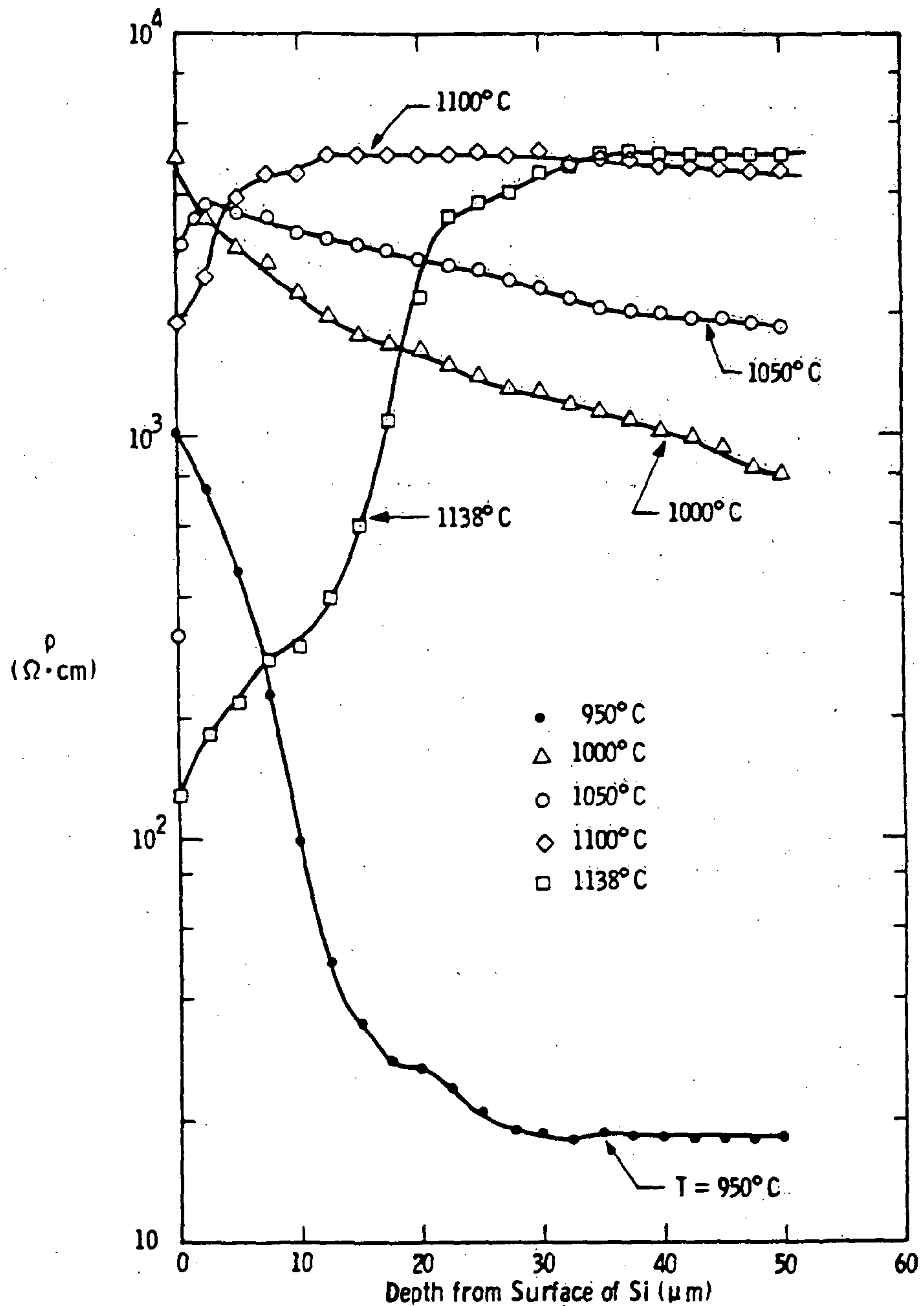

Figure 24. Spreading resistance measurement of Si wafers that have been Au doped at temperatures (950°C → 1138°C) for one hour using an indirect source; starting material is n-type, 10 ohm-cm Si.

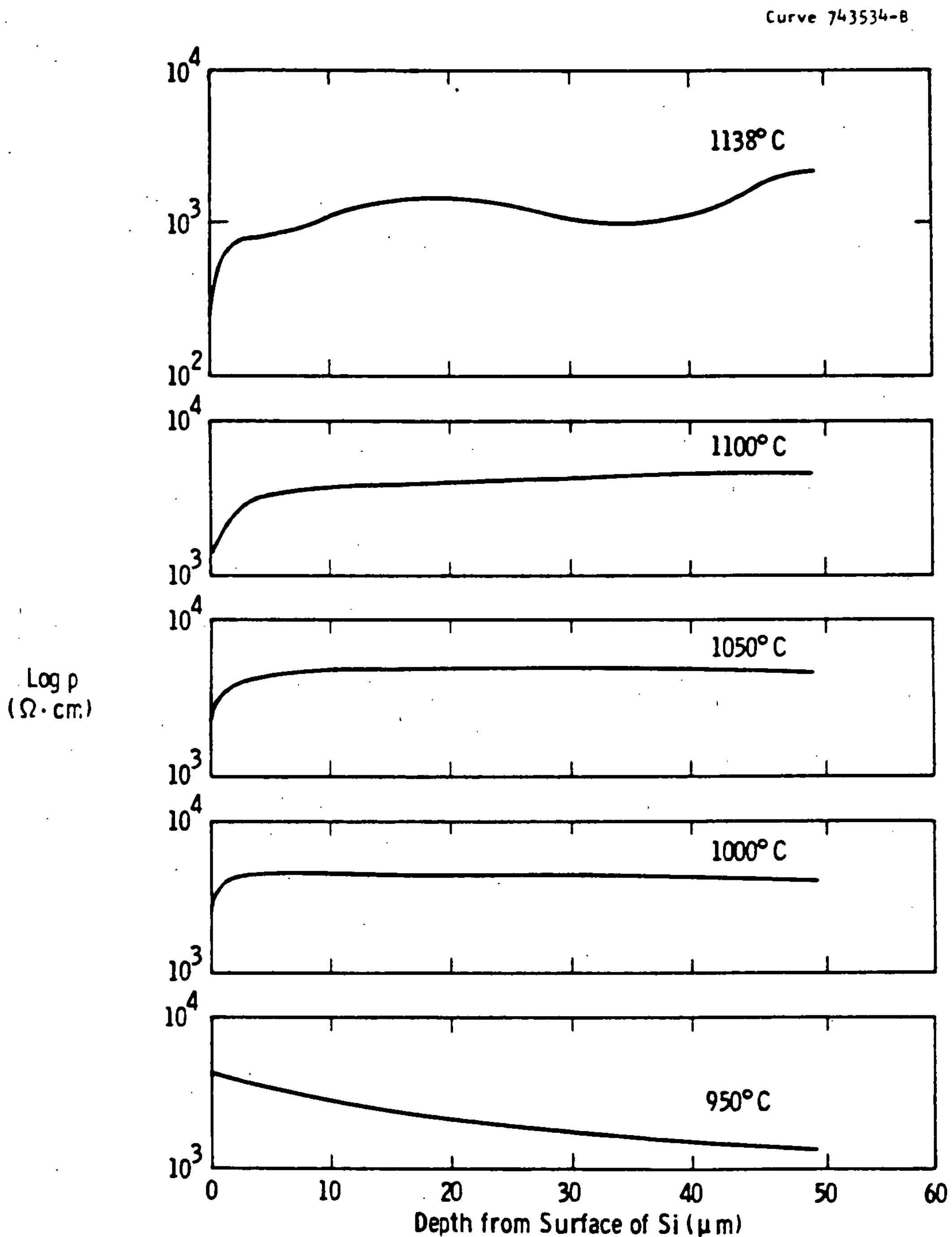

Figure 25. Spreading resistance measurement of Si wafers that have been Au doped at temperatures (950°C → 1138°C) for one hour using an indirect source; starting material is n-type, 100 ohm-cm Si.

Table 11. Gold diffusion for some circular lateral devices made from 14 ohm-cm n-type Si. All the wafers were diffused using the same source, 4-2. A hot probe was used to measure the type (p or n).

			Resistivity, ρ	
Sample	Gold Diffusion Temperature	Type	4-Point Probe	Spreading Resistance
18-1	1138°C	p	45.80×10^3 Ω-cm	3.30×10^3 Ω-cm
18-2	1130°C	p	69.00	4.03
18-3	1120°C	n	11.10	5.07
18-4	1110°C	n	2.04	1.02
18-5	1100°C	n	1.63	11.00
18-6	1090°C	n	3.84	8.14
18-7	1080°C	n	4.57	9.74
18-8	1070°C	n	1.06	9.00
18-9	1060°C	n	18.0	9.09
18-10	1050°C	n	2.28	5.98

Table 12. Gold diffusion for some circular lateral devices made from 14 ohm-cm n-type Si. All the wafers were diffused using the same source, 4-1. These devices had a polysilicon layer between the SiO_2 and the metal. A hot probe was used to measure the type (p or n).

Sample	Gold Diffusion Temperature	Type	Resistivity, ρ 4-Point Probe
17-1	1138°C	p	0.15×10^4 Ω-cm
17-2	1130°C	p	7.80
17-3	1120°C	p	7.90
17-4	1110°C	p	1.30
17-5	1100°C	p	3.20
17-6	1090°C	p	3.90
17-7	1080°C	p&n	1.30
17-8	1070°C	light p	4.20
17-9	1060°C	p&n	2.00
17-10	1050°C	p	2.00

An attempt was made to increase the resistivity by gold diffusing a set of wafers a second time. The results are shown in Table 13. Results were similar to the above when 100 ohm-cm material was gold diffused as shown in Table 14. Also, Table 15 shows the results for more gold diffusions, although this time with wafers that have the lateral rectangular devices on them. The only conclusion that one seems to be able to draw from all this data is that gold diffusion is difficult to control.

4.1.2 Methods #2 and #3 for Gold Diffusion

Method #2 is defined as depositing a layer of gold (using electron beam deposition) onto the back of the device wafer and then cooling relatively slowly (i.e., not quenched in water) after gold diffusion. Method #3 is defined as depositing a layer of gold on the back side of the wafer and then quenching (dropping the wafers immediately into water) after gold diffusion.

Table 16 shows that the four-point probe measurement indicates consistently good (i.e., high resistivity) results with a 24-hour diffusion followed by a water quench. It is felt that with a relatively slow cool (no quench) the gold atoms have a chance to leave their substitutional sites where they are electrically active, and go to interstitial sites where they are not electrically active. It is thought that the water quench "freezes" the gold atoms in the substitutional sites before they have a chance to move. There are two reasons for the 24-hour diffusion. One is that with a 2-hour diffusion followed by quenching, the wafers shattered when they hit the water. Also, sample #12, which did have a 24-hour diffusion, shattered when it hit the water. Sample #12 had a large piece (approximately one-third of the wafer) broken off before the 24-hour diffusion. Apparently the wafers shatter when there is a certain amount of strain in the wafers (probably at the Si/SiO_2 interface) and the 24-hour gold diffusion tends to relieve that strain. Another reason for the 24-hour diffusion is that Stolwijk[31] et al. have measured the penetration profiles of gold

Table 13. Gold diffusion for some circular lateral devices made from 14 ohm-cm n-type Si. The same source, 4-6, was used for all the diffusions. Each of the wafers was gold diffused twice. A hot probe was used to measure the type (p or n).

Sample	1st Gold Diff. Temp.	Type	4-Point Probe, ρ	2nd Gold Diff. Temp.	Type	4-Point Probe, ρ
13-3	1060°C	n	1800 Ω-cm	1100°C	p	11,500 Ω-cm
13-4	1060°C	n	280	1100°C	p	8,200
13-5	1060°C	n	559	1100°C	weak p	23,700
17-11	1050°C	n&p	316	1080°C	p	2,200
17-12	1040°C	n	349	1070°C	p	39,200
18-11	1070°C	n	316	1090°C	p	8,300
18-12	1050°C	n&p	316	1080°C	p	5,500

Table 14. Gold diffusion for some circular lateral devices made from 100 ohm-cm n-type Si. Wafers 14-1, 14-2, and 16-4 were gold diffused a second time (last three entries in the table). A hot probe was used to measure the type (p or n).

Sample	Gold Diff. Temp.	Source	Type	4-Point Probe, ρ
13-1	950°C	4-12	n	309 Ω-cm
13-2	960°C	4-11	weak n	1,900
14-1	970°C	4-10	n	278
14-2	980°C	4-9	n	194
15-1	990°C	4-8	p	16,000
15-2	1000°C	4-7	p	16,000
15-3	1010°C	4-6	p&n	2,170
15-4	1020°C	4-5	p	59,900
16-1	1030°C	4-4	n	343
16-2	1040°C	4-3	n	157
16-3	1050°C	4-2	p	259
16-4	1060°C	4-1	n	263
14-1	1040°C	4-3	p	120,000
14-2	1060°C	4-3	n	7,800
16-4	1080°C	4-3	p&n	5,600

Table 15. Gold diffusion for some lateral rectangular devices made from 14 ohm-cm n-type Si. A hot probe was used to measure the type (p or n).

Sample	Gold Diff. Temp.	Source	Type	4-Point Probe, ρ
LS-1-Au-1	1070°C	4-2	n	0.327 × 10^3 Ω-cm
LS-1-Au-2	1060°C	4-2	n	1.350
LS-1-Au-3	1050°C	4-2	n	25.200
LS-1-Au-4	1080°C	4-2	p	2.000
LS-1-Au-5	1070°C	4-2	p	8.700
LS-1-Au-6	1070°C	4-2	n	40.300
LS-1-Au-7	1050°C	4-4	p	300.000
LS-1-Au-8	1050°C	4-4	n	1.040
LS-4-Au-1	1070°C	4-1	n	0.125
LS-4-Au-2	1070°C	4-2	p&n	0.320
LS-4-Au-3	1070°C	4-6	p	0.213
LS-4-Au-4	1060°C	4-6	p&n	11.500
LS-4-Au-5	1060°C	4-1	p&n	0.780
LS-4-Au-6	1080°C	4-1	p	0.786
LS-6-Au-1	1070°C	4-2	p	0.293
LS-6-Au-2	1070°C	4-2	n	0.231
LS-6-Au-3	1070°C	4-2	n	0.191

Table 16. Gold diffusion using methods #2 and #3 with 200 Å of gold (samples had 7,000 Å of SiO_2 on the polished side)

Sample	Before Diffusion ρ (4-point)	Diffusion Time	Type of Cooling	After Diffusion ρ (4-point)	After Diffusion ρ (Spreading Resistance)	Type
84AU2-1	25 ohm-cm	2 hours	Quench*	391 ohm-cm		n
84AU2-2	21.7	2	Air**	78	8×10^3 ohm-cm	n
84AU2-3	29.6	2	Tube***	69	7×10^3	n
84AU2-4	21.0	24	Quench	4.65×10^5	7×10^3	p
84AU2-5	30.5	24	Air	238	6×10^3	n
84AU2-6	21.3	24	Tube	125	6×10^3	n
84AU2-7	24.7	24	Quench	1.76×10^5		n
84AU2-8	23.9	24	Quench	7.3×10^4		n
84AU2-9	20.2	24	Quench	2.5×10^5		n&p
84AU2-10	20.5	24	Quench	1.27×10^5		n&p
84AU2-11	16.3	24	Quench	$>5.91 \times 10^5$		n&p
84AU2-12	26.5	24	Quench	1.65×10^3		n

*Wafers were dropped immediately into water after gold diffusion.

**Wafers were taken immediately from the tube and placed on a quartz boat in order to cool in ambient.

***Wafers were pulled to the end of the tube (~415°C) and left to cool for about 10 min. before being exposed to ambient temperature.

into silicon and they showed that it takes a long time, between 20 and 70 hours, for the gold concentration throughout the wafer to approach the solubility limit. Thus, it seems that better control over the gold-diffusion process can be attained with the longer diffusion times. They also showed that the "kick-out" mechanism is important for explaining certain aspects of gold diffusion.

With just the four-point probe measurements it appears as if the quench method is superior to the slower cooling methods. The results are not so clearly defined, however, when examining the spreading resistance measurements, which were taken from the surface of the back side to 50 μm into the material. The resistivity of sample #6 was 240 ohm-cm at the surface and then increased to 6,000 ohm-cm at about 20 μm and remained constant. Samples, 2, 3, and 5 showed similar behavior; #2 went from 4,000 to 7,000 ohm-cm in 3 μm, #3 went from 4,000 to 8,000 ohm-cm in 5 μm, and sample #5 went from 2,000 to 6,000 ohm-cm in 15 μm. Sample #4 was 7,000 ohm-cm from the surface to 50 μm. From the spreading resistance measurements it appears that the difference among quenching, air, and tube methods of cooling only exists near the surface, and that after 20 μm or so there is no difference. Also, the 2-hour diffusion time seems to give the same results as the 24-hour diffusion time. It should be noted that spreading resistance measurements have consistently given resistivity values less than the four-point probe measurement.

The samples reported in Table 16 had 7,000 Å of oxide on one side and 2000 Å of gold on the other during gold diffusion. The oxide color was reddish. With samples 1, 2, and 3 (2 hours diffusion) a slight color change (greenish) occurred around the edges. With samples 4, 5, and 6 (24 hours diffusion) the change was more pronounced, and with samples 7, 8, 9, and 10 there were interference patterns set up. With the wafers standing up, the N_2 flowed first to #10, then to #9, and then to #8 and #7. Thus, #10 had no gold diffusing into its oxide from the other samples, while #7 had gold from the other three samples. Sample #10 showed color change only around the edge, but samples 7,

8, and 9 showed many interference rings. It is assumed that the gold diffusion in the oxide has changed the index of refraction of the oxide. Samples 11 and 12 were laid down (oxide down) in 2 furnace tubes and showed very little change in oxide color. Whether or not the change in color is indicative of a problem has yet to be determined, but this change can be prevented by laying the wafers down during gold diffusion.

In Table 17 the resistivity of samples is shown after using method #2. For samples 3-1 and 3-2 there appeared to be a layer of gold (perhaps an alloy) still on the back side after diffusion. For the rest of the samples diffused at 1100°C, the resistivity values are very consistent and, except for sample 3-8, the hot probe indicated intrinsic (i.e., the indicator did not move either toward n-type or p-type). The samples diffused at 1000°C gave fairly consistent results with values of resistivity lower than those diffused at 1100°C.

Six wafers (D2-1 through D2-6) with injection-gated devices were diffused with gold at three different temperatures using method #3. Table 18 shows that the diffusion temperature giving the highest resistivity and the nearest reading to intrinsic (using the hot probe) is 1000°C.

Three wafers (P3-5, P4-5, and P3-6) with areas of phosphorus and boron diffusion on the oxide side were diffused along with the other six wafers. These wafers will eventually be used for gold-gettering studies.

At 950°C, two of the wafers (D2-2 and P3-5) broke when dropped into the water. For the other two temperatures the quenching was delayed for four to five seconds, which resulted in only one wafer (D2-4) breaking. This breakage was probably due to the extra strain put on the Si/SiO_2 interface by the discontinuities created by the devices on samples D2-1 through 6 and the diffusion areas on P3-5, 6, and P4-5.

All the wafers were laid flat on the boat with the oxide down in order to prevent the discoloration of the oxide that had been noticed when the wafers were standing up. A powdery gold compound that is off-white in color formed on the gold-layered side. Some of this compound

Table 17. Resistivity measurements of devices produced using gold diffusion method #2. For those types marked intrinsic, the hot probe indicator did not budge either toward p-type or n-type. Starting resistivity was about 65 ohm-cm.

Wafer Number	Gold Film	Gold Diff. Temp.	Resistivity After Diff. (4-point)	Type
3-1	300 Å	1100°C	0.158 ohm-cm	n
3-2	300	1100°	1.51	n
3-3	300	1100°	6.58×10^4	intrinsic
3-4	300	1100°	$>4.20 \times 10^5$	intrinsic
3-5	300	1100°	4.05×10^4	intrinsic
3-6	300	1100°	6.68 × 104	intrinsic
3-7	300	1100°	$>4.20 \times 10^5$	intrinsic
3-8(a)	300	1100°	5.19×10^4	p
3-8(b)	300	1100°	3.16×10^4	p
5-1	200	1000°	2.53×10^4	n
5-2	200	1000°	1.16×10^3	n
5-3	200	1000°	3.79×10^3	p and n
5-4	200	1000°	1.05×10^4	n

Table 18. Device wafers produced using gold diffusion method #3. The wafers had 200 Å of gold on the back side and were diffused for 24 hours. The resistivity was measured using the four-point probe.

Sample	Before Diffusion Resistivity	Diff. Temp.	After Diffusion Resistivity	Conductivity Type
D2-1	20.6 Ω.cm	950°	1.68×10^4 Ω.cm	strong n
D2-2	28.3	950°	3.39×10^3	strong n
P3-5	24.5	950°	4.50×10^3	strong n
D2-3	29.6	1000°	2.08×10^4	weak p
D2-4	28.2	1000°	1.92×10^4	weak p
P4-5	25.0	1000°	6.63×10^4	weak p
D2-5	31.9	1050°	4.75×10^3	strong p
D2-6	23.9	1050°	1.56×10^3	strong p
P3-6	26.2	1050°	8.69×10^3	strong p

flaked off and apparently got under the wafers and stuck to the oxide. Wafer D2-5 had a number of spots which ruined about 10 devices. These spots were off-white in color (like the gold compound) and had discoloration rings (red and green) around them. The wafers were soaked in aqua regia but the spots did not come off. Next they were soaked in sulfuric acid, which did remove some of the foreign material.

The resistivity values and type indication for the wafers listed in Table 18 exhibit a much better consistency than any of the results using method #1. From the results tabulated in Tables 16, 17, and 18, it can be said that the deposition of gold on the back side of the wafer gives much more predictable and consistent results than the indirect source (method #1). However, it is not clear yet as to whether the quench is necessary. This probably can only be determined by producing devices using both methods #2 and #3.

4.1.3 Gold Gettering Effects of Phosphorus and Boron

The mask set shown in Figure 19 was used to determine the extent of gold gettering by phosphorus and boron. Measurements were made on both 14 ohm-cm and 100 ohm-cm material. Spreading resistance and four-point probe measurements were made on both the front and back of the wafer. In Table 19 note that four-point probe measurements on the back of the wafer [back (p^+) and back (n^+)] directly opposite the p^+ and n^+ diffusion can be misleading. After gold diffusion (method #1) the results are 33.5 ohm-cm and 53 ohm-cm, respectively, but the spreading resistance measurements show that the gold-diffused area outside of the p^+ and n^+ regions (i.e., a depth greater than 6 μm) is essentially the same whether it is under the phosphorus or the boron diffusion areas or under the no-diffusion area. The four-point probe measurements without benefit of the spreading resistance measurements might lead one to assume a much larger gettering effect than actually exists. In fact, the spreading resistance data (both Tables 19 and 20) before the anneal would seem to indicate that there is no gettering effect at all. However, when the 14 ohm-cm sample is annealed, the results are as shown

Table 19. The data in this table were obtained from devices processed with 14 ohm-cm material using the masks shown in Figure 19. The shallow impurity diffusion areas are "none" (no shallow impurity diffusion), "p^+" (boron), and "n^+" (phosphorus). The gold diffusion was at 1100°C for one hour using method #1. The terms "back (n^-)," "back (p^+)," and "back (n^+)" refer to the respective areas on the back of the wafer that are opposite to the following areas on the front: "none," "p^+," and "n^+." A hot probe was used to measure the type (p or n).

Diffusion Area	Type	4-Point Probe, ρ	Spreading Resistance min	Spreading Resistance max	Depth
(a) Before Gold Diffusion					
none	n	7.000 Ω-cm	10.0 Ω-cm	19 Ω-cm	-
p^+	p	3.900	1.7×10^{-2}	17	2.6 μm
n^+	n	.067	10^{-3}	16	5.4
back	n	6.500			
(b) After Gold Diffusion					
none	p	7.70×10^4	7.5×10^3	7.5×10^3	-
p^+	p	3.70 Ω-cm	2.0×10^{-2}	7.0×10^3	2.7
n^+	n	0.06	10^{-3}	5.0×10^3	5.2
back (n-)	p	4.90			
back (p^+)	p	33.50			
back (n^+)	p&n	53.00			
(c) After Gold Diffusion and Annealing					
none	p	3.60×10^4 Ω-cm	8.5×10^3	8.5 × 103	-
p^+	p	3.80 Ω-cm	1.5×10^{-2}	~8.0×10^3*	2.7 μm
n^+	n	0.61	10^{-3}	7.0×10^3*	5.2
back (n)	p	2.90×10^5			
back (p+)	p	30.70			
back (n+)	n	24.80			

*See Figure 26

Table 20. The data in this table were obtained with 100 ohm-cm material using the masks shown in Figure 19. The gold diffusion was at 1000°C for one hour. The terms under "Diffusion Area" have the same meaning here as in Table 9. A hot probe was used to measure the type (p or n).

Diffusion Area	Type	4-Point Probe, ρ	Spreading Resistance ρ_{min}	Spreading Resistance ρ_{max}	Diffusion Depth
(a) Before Gold Diffusion					
none	n	98.000 Ω-cm	120.0 Ω-cm	160 Ω-cm	-
p^+	p	5.400	1.8×10^{-2}	130	2.9 μm
n^+	n	0.095	8.0×10^{-4}	110	4.8
(b) After Gold Diffusion					
none	p	2.900×10^5	6.0×10^3	6.0×10^3	-
p^+	p	5.000	1.5×10^{-2}	8.0×10^3	2.4
n^+	n	0.086	1.0×10^{-3}	5.5×10^3	6.0
back (n^-)	p	2.300×10^5	-	-	-
back (p^+)	p	6.400×10^4	-	-	-
back (n^+)	p	1.000×10^5	-	-	-
(c) After Gold Diffusion and Annealing					
none	p	1.400×10^5	7.0×10^3	7.0 × 103	-
p^+	p	5.900	2.0×10^{-2}	8.0×10^3	2.8
n^+	n	0.082	1.0×10^{-3}	5.0×10^3	6.4
back (n^-)	p	2.400×10^5	-	-	-
back (p^+)	p	1.600×10^4	-	-	-
back (n^+)	p	1.200×10^4	-	-	-

in Figure 26. The gold seems to be partially gettered by the phosphorus to a depth of about 20 μm. The same effect does occur for the boron diffusion with the 14 ohm-cm sample, and the shape of the curve after the anneal is almost identical to the one shown in Figure 26 for the phosphorus diffusion. Phosphorus has been shown[27] to more effectively getter gold but that is not apparent from these results. The 100 ohm-cm sample, however, shows no gettering effects due to the anneal.

Collins, Schroder, and Sah[32] have measured the gold diffusion coefficient, D, from 800°C to 1200°C. By extending their results to 450°C (the anneal temperature), one can make an estimate of the diffusion length, L. Using the data of Collins et al., one has L = 3.4 μm; using data from Struthers (see Collins et al.), one has L = 8.5 μm; using data from Boltak (see Collins et al.), one has $L = 1.7 \times 10^{-3}$ μm. Gold diffusion can occur either interstitially or substitutionally. A high interstitial diffusion rate is combined with a low interstitial solubility, and a low substitutional diffusion rate is associated with a high substitutional solubility. The net result is that the diffusive flux is carried almost entirely by interstitial atoms, and then the interstitial gold atoms combine with vacancies to form substitutional atoms. In material with a high concentration of vacancies the gold diffusion is only limited by the interstitial diffusion rate and is known as an interstitially limited process. However, when the vacancy concentration is low, the diffusion process is limited by the dissociation reaction

$$Au_s \rightleftarrows Au_i + V \quad (21)$$

where Au_s is the substitutional gold atoms, Au_i is the interstitial gold atom, and V is a vacancy. The vacancies must diffuse from a distant source such as from the surface, and thus the diffusion rate is a vacancy rate-limited process. It is felt that Struther's data (L = 8.5 μm at 450°C) reflect an interstitially limited process and that Boltak's data ($L = 1.7 \times 10^{-3}$ μm at 450°C) reflect a vacancy rate-limited process.

C-2

Curve 745877-A

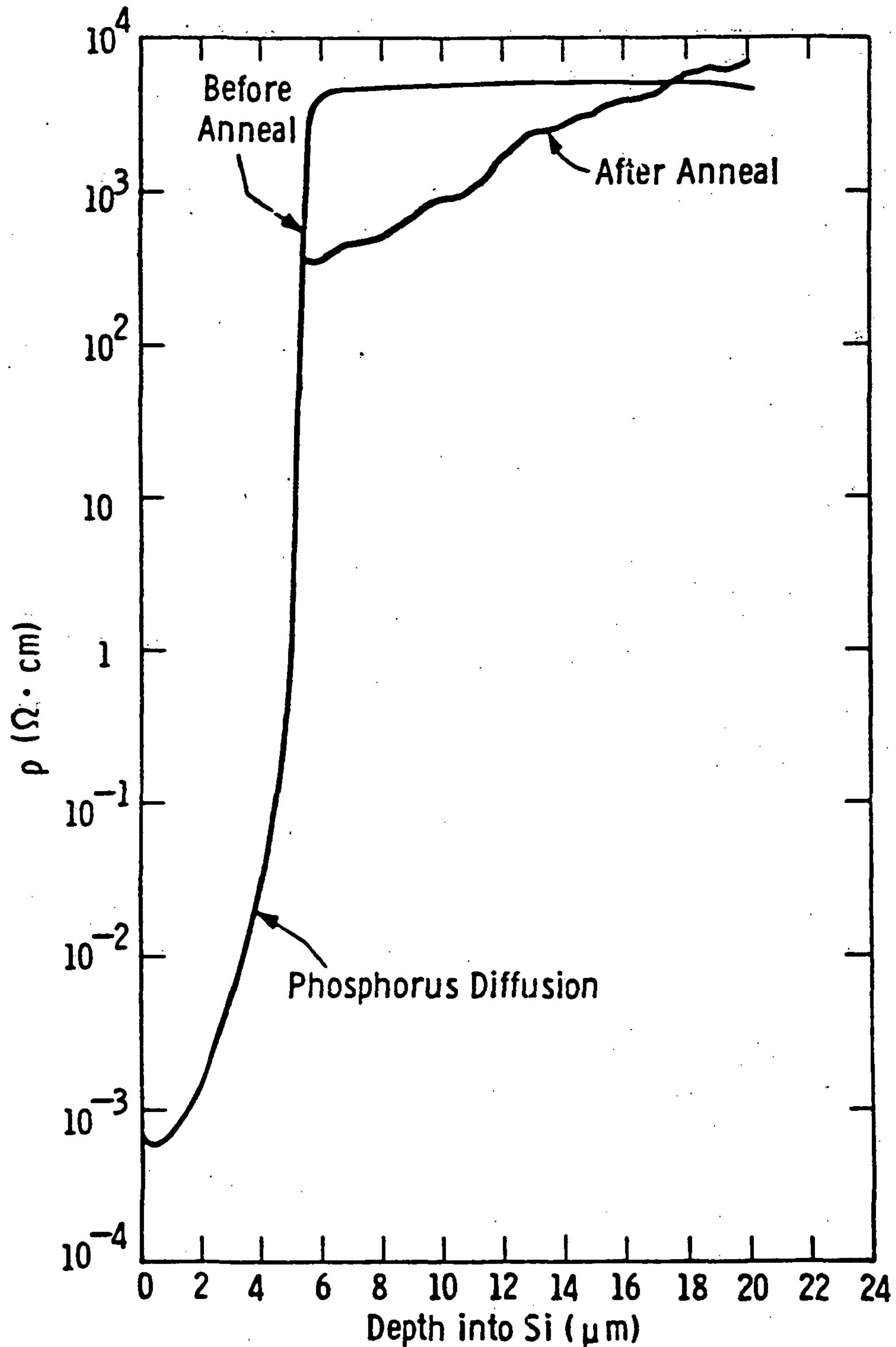

Figure 26. Samples of 14 ohm-cm starting resistivity were diffused with gold at 1100°C for one hour. The anneal was 450°C for one-half hour. The low-resistivity area is the phosphorus diffusion area produced using the masks shown in Figure 19.

The 14 ohm-cm material was Czochralski grown and the 100 ohm-cm was float-zone NTD material. From the limited data reported above, it seems that the 14 ohm-cm material has an interstitially limited gold diffusion, and the 100 ohm-cm material has a vacancy rate-limited process. This conclusion comes from noting that the 14 ohm-cm material getters the gold out to about 20 μm, which would be consistent with $L = 8.5$ μm (interstitially limited process), and the 100 ohm-cm material does not appear to getter at all, which would be consistent with $L = 1.7 \times 10^{-3}$ μm (vacancy rate-limited process). In other words it appears as if the 14 ohm-cm material has a lot more vacancies than the 100 ohm-cm material.

4.2 Devices Produced Using Gold Diffusion

4.2.1 Devices Made Using Method #1

The devices produced using gold diffusion method #1 were all either poor switches or better switches, with no devices classified as good switches (see Section 2.4).

Table 21 shows a summary[18,19] of some of the results obtained for the circular lateral devices with deep levels introduced by gold diffusion. Before sintering, the devices were better switches (similar to Figures 9a and b). However, after sintering (450°C for 30 min. in H_2) the devices had an I-V response such as in Figures 9c and 10, i.e., they went from being better switches to poor switches.

Three possibilities come to mind when considering plausible causes of this deterioration: (1) gold gettering by the phosphorus and boron electrode diffusions, (2) annealing of deep levels in the bulk, and (3) reduction of interface traps.

In Section 4.1.3 it was reported that an anneal temperature of 450°C (30 min) caused a gettering of the gold atoms by the phosphorus and boron diffusion areas. This gettering, however, only occurred for the 14 ohm-cm material and not for the 100 ohm-cm material, while the degeneration of the characteristics of the devices happened with both

Table 21. Circular lateral devices that have been gold diffused. The electrode spacing is 760 μm (~ 30 mil).

Starting Resistivity	Al Sinter 450°C	Gold Diffusion Temperature	V_T	V_H	V_T/V_H	R_B
10 Ω-cm	No	1050°C	850 V	70 V	12.0	400 kΩ
10 Ω-cm	Yes	1050°C	450 V	50 V	9.0	70 kΩ
10 Ω-cm	No	1100°C	1350 V	50 V	27.0	2.5 MΩ
10 Ω-cm	Yes	1100°C	670 V	50 V	13.4	70 kΩ
10 Ω-cm	No	950°C	450 V	100 V	4.5	2 MΩ
100 Ω-cm	Yes	950°C	200 V	120 V	1.7	-
100 Ω-cm	No	1000°C	320 V	60 V	5.3	2 MΩ
100 Ω-cm	Yes	1000°C	300 V	150 V	2.0	-

the 10 ohm-cm material and the 100 ohm-cm material. Also, the change in V_T does not correspond to the effective change in L, i.e., the gettering extended about 20 μm into the material, which would mean a new effective length of about 720 μm or a reduction in V_T of about $(720/760)^2 = 0.90$, while the actual reduction was about 0.5 for most of the devices. Furthermore, this effective reduction of L should not significantly affect R_B, which also decreased dramatically. Thus, the gold gettering is probably not the cause of this problem.

In Figure 12 it is perceived that an anneal of 450°C (Figure 12k) is enough to reduce the deep-level defect states caused by radiation to a density that will not support the negative resistance behavior, but not a high enough temperature to produce the deep levels needed for the good switch behavior (Figure 21). If there is a significant density of defect deep levels caused perhaps by the high density of gold atoms and these defect deep levels anneal out at 450°C, then this could be the cause of the deterioration of the parameters due to the sintering.

The reason for the sintering is to give a better ohmic contact of the aluminum to the n^+ or p^+ regions and to create a more stable bond between the aluminum and the silicon or silicon dioxide. An additional effect is the reduction of the interface trap states. An oxide annealed[33] at 350-500°C in a hydrogen or nonoxidizing ambient can have a reduction in the density of interface trap states as much as two orders of magnitude. Tuntasood's results,[9] however, seem to indicate that a reduction of surface states would bring about an increase and not a reduction in V_T. He found that with a MOS gate the threshold voltage was as high as 220 V when V_G = -4 V and was as low as 60 V when V_G = +4 V, while at V_G = 0 V it was about 135 V. This device did not have symmetric electrodes but had a p^+ region for the anode and a n^+ region for the cathode. The cathode was grounded and the gate voltage was taken with respect to the cathode. The cathode-anode spacing, L, was 4 mil and the gate was located at the center of the channel.

Tuntasood explained the change in V_T with V_G by noting that the theoretical value obtained by Lampert[1,3,4] is smaller than that obtained by Ashley.[34,35] In Lampert's model the electron traps (deep levels) are assumed to be fully occupied by electrons, but Ashley assumes that the electron traps are only partially occupied. For the totally compensated device ($N_t = N_D$), the Fermi level is just slightly above the gold acceptor levels (Figure 27) so that any band bending at the Si/SiO_2 interface will cause a significant change of the electron population in the traps. The population of the donor levels will not change because the Fermi level is so far from them. For the sake of analysis it will first be assumed that there is no oxide charge or interface trap states, i.e., flat band condition with V_G = 0 (see Figure 27b). The application of a negative voltage to the gate will bend the bands upward (Figure 27c) near the Si/SiO_2 interface. As a result the trap states near the interface will also bend upward and the population of electrons in these states will decrease, thus causing V_T to increase, i.e., this now fits Ashley's model. When a positive voltage is applied to the gate, the bands will bend downward and the electron population in the traps will

Curve 749748-B

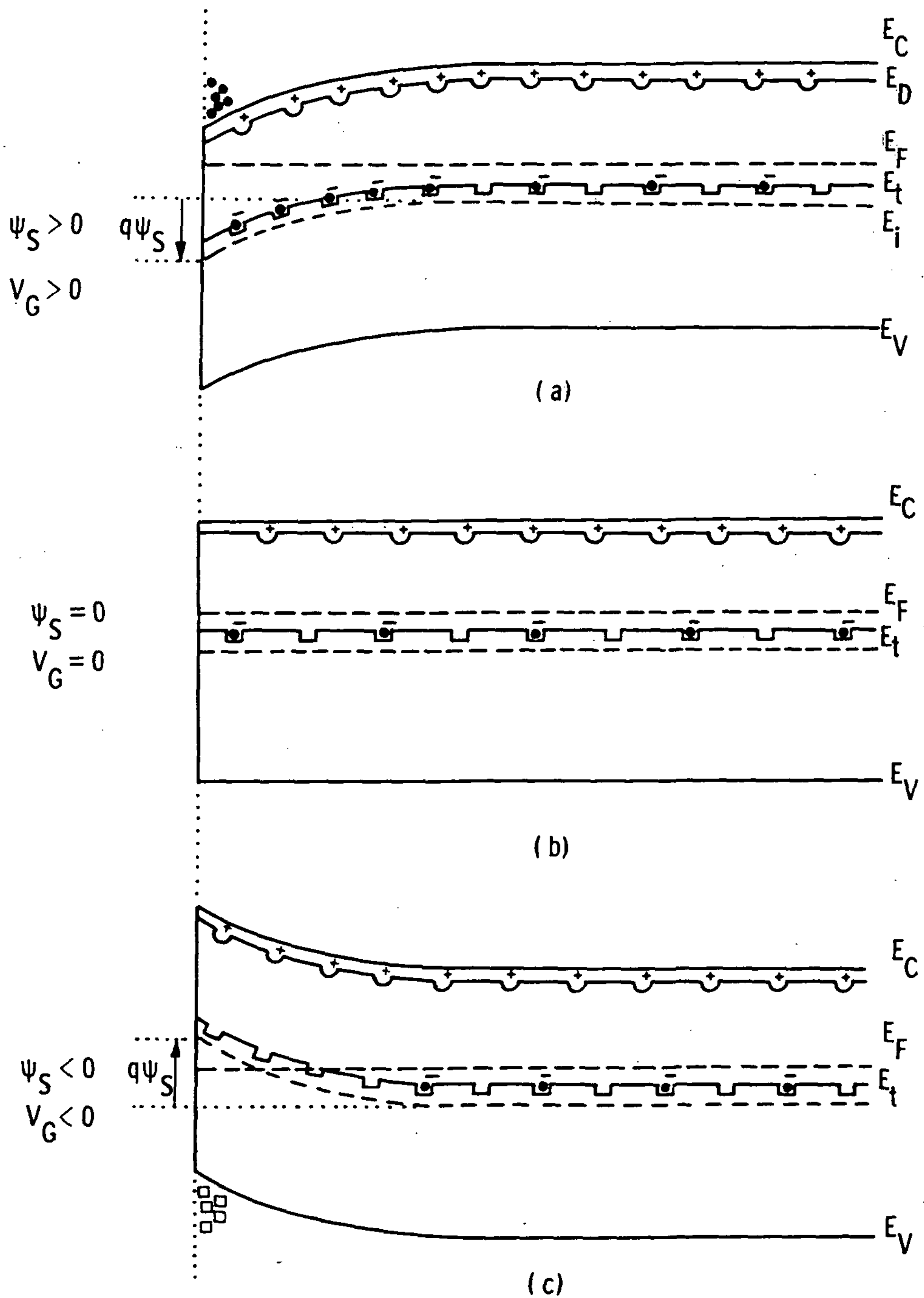

Figure 27. Band bending for an applied gate voltage, V_G, when there is no oxide charge or interface traps.

increase (Figure 27a). This will cause a decrease in V_T since Lampert's model will now be the one more closely satisfied. This theory agrees qualitatively with Tuntasood's experimental results.

The effect of interface trap states, Q_{it}, fixed oxide charge, Q_f, and mobile sodium ions, Q_m, can be represented by a sheet of positive charge at the interface. The effect of this charge is to bend the bands down, thus filling the traps with electrons and, as a result, decreasing V_T. Another source of positive charge in the oxide is the oxide traps, Q_{ot}, created by radiation. The metallization for these devices is E-beam, which causes radiation damage that consists of an increase in both Q_{it} and Q_{ot}. An anneal at 450°C in an H_2 ambient will reduce both Q_{it} and Q_{ot}. Thus, the sintering process should decrease the positive charge which should cause an increase in V_T. Since the sintering caused the opposite effect, either the above outlined theory is not correct or other factors are more important.

A series of experiments could be performed that would help to sort out the effects of interface trap states, oxide charge, and the annealing of deep levels in the bulk. If the degeneration of the properties of the device when sintered is due to Si/SiO_2 interface effects, then gold-diffused vertical devices should not be affected. Up until now all of the vertical devices have been irradiated and the sintering has been done before the irradiation. Also, it might be very useful to include some test devices on the wafers. This could be done by altering the existing masks so that there are separate p^+ and n^+ areas, MOS dots with some oxides the same thickness as the gate and some the same as the field oxide, and areas where Schottky gates can be processed. In this way measurements such as DLTS, OCVD, C-V, etc. can be made on the same wafer that the devices are on. Another possibility is the use of <100> silicon instead of <111> because of the reduced number of interface trap states.

Table 11 (Section 4.1.1) shows the results of gold diffusion for some wafers with circular lateral devices processed on them. The

devices on wafer 18-9 were classified as better switches, while the ones on the other wafers were poor switches. Wafer 18-9 had the highest resistivity (18×10^4 ohm-cm) as measured by the four-point probe for all the wafers that were still n-type. For all devices produced using method #1, the best devices were the ones with wafers having the highest resistivity while still being n-type. Unfortunately, as attested to by the data in Tables 11, 12, 13, 14, and 15, it is not easy to consistently produce wafers with very high resistivity.

4.2.2 Devices Made Using Method #2

Two batches of wafers with circular lateral devices were processed using gold diffusion method #2. The resistivity measurements and characteristics of the devices are shown in Table 22. All devices (64 devices per wafer) on a given wafer showed remarkable consistency for the parameters V_T, V_H, and leakage current. For example, on wafer 3-4, all values of V_T fell between 200 V and 260 V with most at about 230 V. The value of V_H only varied a few volts across the wafer, and the value of leakage current only about 20 mA across the wafer.

The devices on wafers 3-3 through 3-8 were good switches with switching times on the order of one microsecond.[17] The I-V curve for device 3-8(a) is presented in Figure 8 (Section 2.4). One troubling aspect of the I-V response of the devices on wafers 3-3 through 3-8 is that there is no forward blocking. The circular lateral devices have symmetric electrodes which should give them similar responses both with forward bias and reverse bias. In practice it has been found that the reverse V_T has not been as large as the forward V_T. In this nomenclature the center dot is taken as the anode. This asymmetry is a geometric effect, but for all circular lateral devices except this group there has been a respectable V_T in both directions. The response of this group looks very much like the results reported for the p-i-n diode in Reference 19. One possibility is that one of the diffusions (n^+ or p^+) for the electrodes was not done and that they are effectively p-i-n diodes.

Table 22. Resistivity measurements and characteristics of devices produced with gold diffusion method #2. Samples 3-1 through 3-8 had 300 Å of gold deposited on them and were diffused at 1100°C. Samples 5-1 through 5-4 had 200 Å of gold deposited on them and were diffused at 1000°C. For those resistivities marked intrinsic, the hot probe indicator did not budge either toward p-type or n-type. The leakage current was measured at V_T. Starting resistivity was about 65 ohm-cm.

Wafer	After Diffusion ρ (4-point)	Type	V_T (Average)	V_H (Average)	V_T/V_H	Leakage Current
3-1	0.158 ohm-cm	n	-	-	-	1 ohm resistor
3-2	1.51	n	-	-	-	1 ohm resistor
3-3	6.58×10^4	intrinsic	220 V	15 V	14.6	350 mA
3-4	$>4.20 \times 10^5$	intrinsic	230 V	10 V	23.0	300 mA
3-5	4.05×10^4	intrinsic	220 V	16 V	13.8	350 mA
3-6	6.68×10^4	intrinsic	190 V	-	-	380 mA
3-7	$>4.2 \times 10^5$	intrinsic	300 V	100 V	3.0	50 mA
3-8(a)	5.19×10^4	p	530 V	25 V	21.2	100 mA
3-8(b)	3.16×10^4	p	200 V	16 V	12.5	360 mA
5-1	2.53×10^4	n	250 V	50 V	5.0	25 mA
5-2	1.16×10^3	n	250 V	50 V	5.0	25 mA
5-3	3.79×10^3	p and n	250 V	50 V	5.0	25 mA
5-4	1.05×10^4	n	250 V	50 V	5.0	25 mA

Devices on wafers 3-1 and 3-2 acted like one-ohm resistors and the wafers had low resistivities. This may indicate that some form of gold-silicon alloy was formed during the diffusion process. All devices on wafers 5-1 through 5-4 were not good switchers.

The measurement of resistivity for 3-8(a) was taken directly below the one dot that gave $V_T = 530$ V, while the measurement for 3-8(b) was taken at three different places on the rest of the piece of the wafer (this piece had 19 devices on it). Thus, the device that worked best with gold diffusion method #2 had silicon that was p-type and had the highest resistivity.

4.2.3 Devices Made Using Method #3

In an attempt to determine the proper temperature for the gold diffusion using method #3, three different temperatures were used. The results of the resistivity measurements were presented in Table 18 (Section 4.1.2).

As mentioned in Section 4.1.2, two of the device wafers (D2-2 and D2-4) broke when they were dropped into the water. Some more devices were lost when the powdery gold substance flaked off the back side of some of the wafers and stuck to the front side of other wafers. In addition to this, during the HF dip used in order to open the metal contact windows, the photoresist lifted on some of the wafers. Almost all of the devices on wafer D2-5 and most of the devices on wafer D2-1 were ruined. Wafers D2-3 and D2-6, however, were mostly all right.

In summary, this left one wafer (D2-6) diffused at 1050°C and one wafer (D2-3) diffused at 1000°C that were mostly all right. Also, some devices (10 to 15) on wafer D2-1 (950°C) were salvageable.

Unfortunately, none of the gold-diffused devices turned out to be good switches, although it was still possible to gate some of the devices. Wafer D2-1 was used since the devices on it were the best switches. It appears that the optimum temperature for gold diffusion using the quench method should be around 975°C.

For the I-V curve tracer the amplitude of the sine wave was turned up to V_T. At this point the trace is essentially horizontal, and if the amplitude is increased the I-V trace rotates to the vertical position similar to what happens in Figure 10.

These devices have an injection gate located 10 mil from the outer ring. When the center dot is positive a positive gate voltage will cause the I-V curve to begin to rotate (see Figure 28). A voltage of +55 V reduced V_T from 500 V to 450 V. If the grounded electrode is considered to be the cathode, then the gate-to-cathode distance is 10 mil (L = 30 mil).

When the center dot is grounded (outer ring swings positive and negative), the I-V curve is unchanged as the voltage swings positive, but changes for various gate voltages as the voltage swings negative (see Figure 29). When a voltage is applied to the gate (with respect to the grounded center dot) the I-V curve becomes vertical instead of horizontal in the negative quadrant. There is effectively (see Figure 29) a V_H instead of a V_T. The values of V_H with respect to the applied gate voltage are tabulated in Table 23. The effective gate-to-cathode distance is 20 mil. As a future experiment the gate will be placed halfway between the center dot and the outer ring, i.e., L_{GC} = 15 mil. This might give the best results.

4.3 Current Conduction for $V < V_T$

With respect to current conduction in the prethreshold voltage regime ($V < V_T$), the devices can be classified into three categories: (1) Ohm's law response followed by superlinear regime, (2) Ohm's law response followed by sublinear regime, and (3) superlinear through the entire range. Only category (1) is explained by Lampert's theory.

For devices that were good switches, an example of category (1) is shown in Figure 8, category (2) in Figure 30, and category (3) in Figure 31. One interesting aspect of these results is that the I-V curves shown in Figures 8 and 30 were devices that were on the same

Curve 749744-A

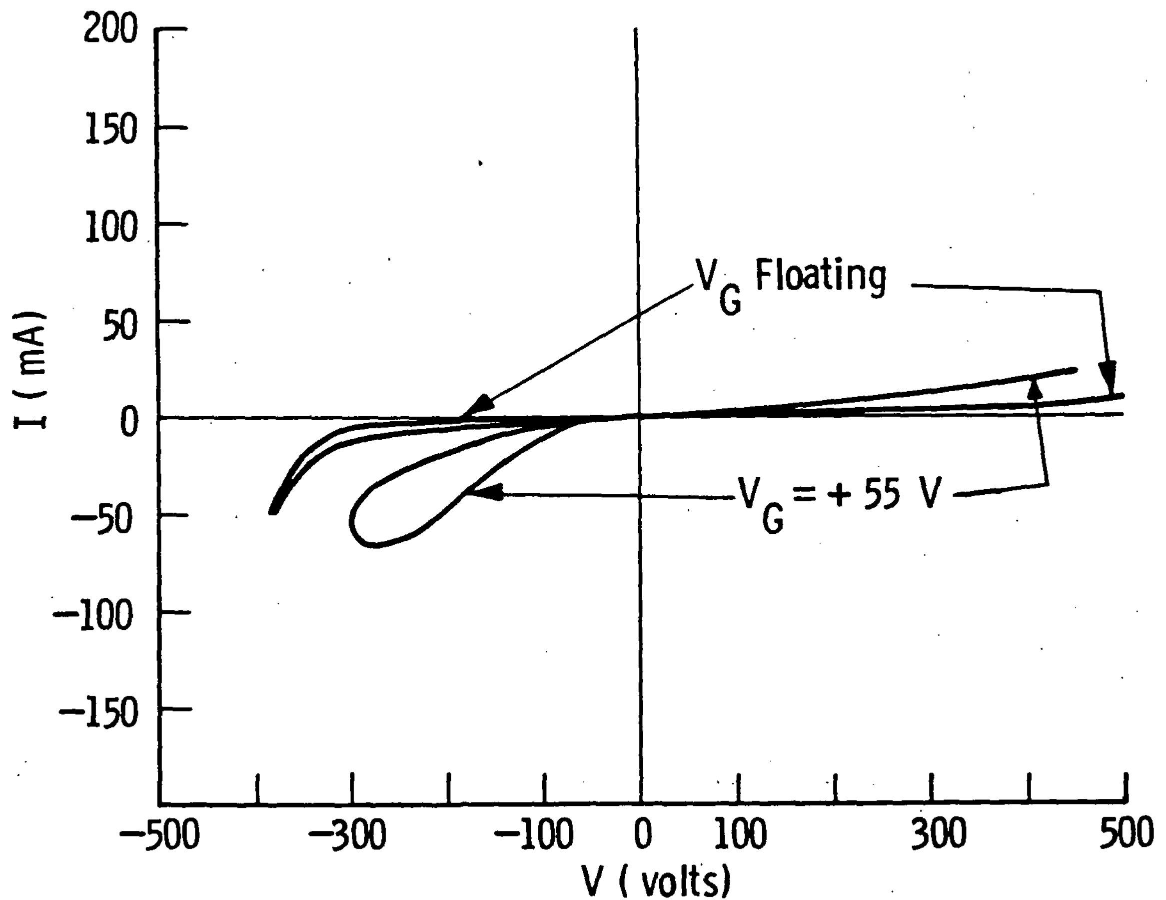

Figure 28. Circular lateral device D2-1 with the outer ring grounded. The distance from outer ring to gate is 10 mil and L = 30 mil. Gold diffusion was method #3 for 24 hours at 950°C.

Curve 749747-A

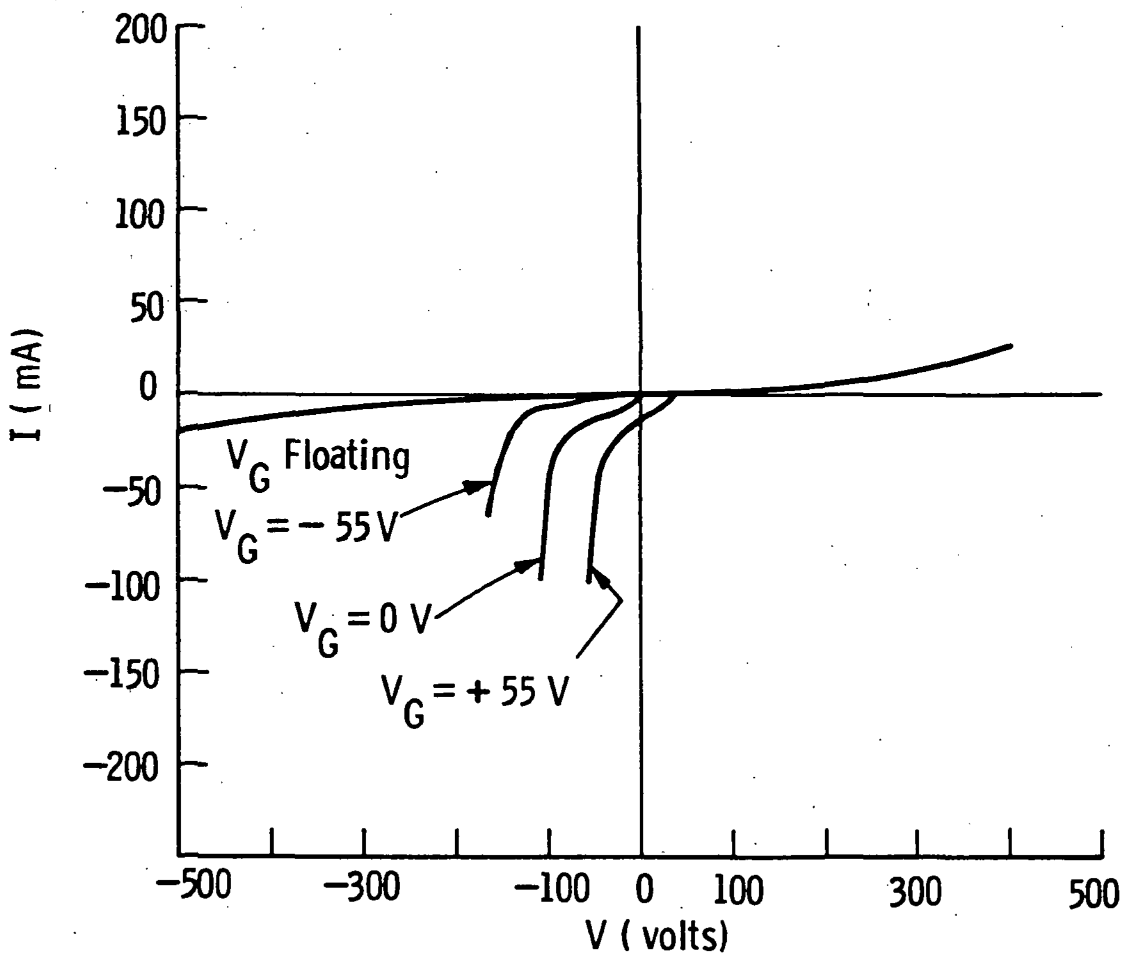

Figure 29. Circular lateral device D2-1 with the center dot grounded. The distance from center dot to gate is 20 mil and L = 30 mil. Gold diffusion was method #3 for 24 hours at 950°C.

Table 23. Injection-gated circular lateral devices, D2-1, with the center dot grounded. Effective L_{GC} = 15 mil and L = 30 mil. Gold diffusion was method #3 for 24 hour at 950°C.

V_{GC}	-55 V	0	+ 55 V
V_H	160 V	100 V	50 V

wafer, 3-8. As reported in Section 4.2.2, the resistivity of the wafer below the device on 3-8(a) (I-V in Figure 8) was 5.19×10^4 ohm-cm, while the resistivity for 3-8(b) (I-V in Figure 30) was 3.16×10^4 ohm-cm. The higher resistivity produced the higher threshold voltage.

In order to find the power law dependence of the current with respect to the voltage of these devices for subthreshold values, I-V curves were plotted on log-log paper. The device A-5 on sample 3-8(a) has the best parameters for a fast switch (~1 μsec switching time). The threshold voltage was about 530 volts and the holding voltage about 25 volts. The current is linear ($I \propto V$) up to about 380 volts, where it begins to turn up sharply before switching (see Figure 32). All the devices on sample 3-8(b) had a threshold voltage of about 200 V and showed a linear response up to about 70 volts and then had a sublinear ($I \propto V^n$, $n \cong 1/3$) response out to the threshold voltage. In the subthreshold regime, device A-5 has a lower leakage current for a given voltage than the other devices as well as having a higher threshold voltage. On the other hand, sample 3-7 had a threshold voltage of about 300 volts and a superlinear dependence ($I \propto V^n$, $n \cong 5.4$) up until the threshold voltage (see Figure 33).

All of the above samples were good switches. Two of them showed a linear response for $V < V_T$, which is just the Ohm's Law region and is expected. However, none of them showed the square law ($I \propto V^2$) that was expected. In fact one was sublinear and the other showed a much stronger ($n = 5.4$) dependence on the voltage. These last two results cannot be explained by Lampert's theory.

Curve 749745-A

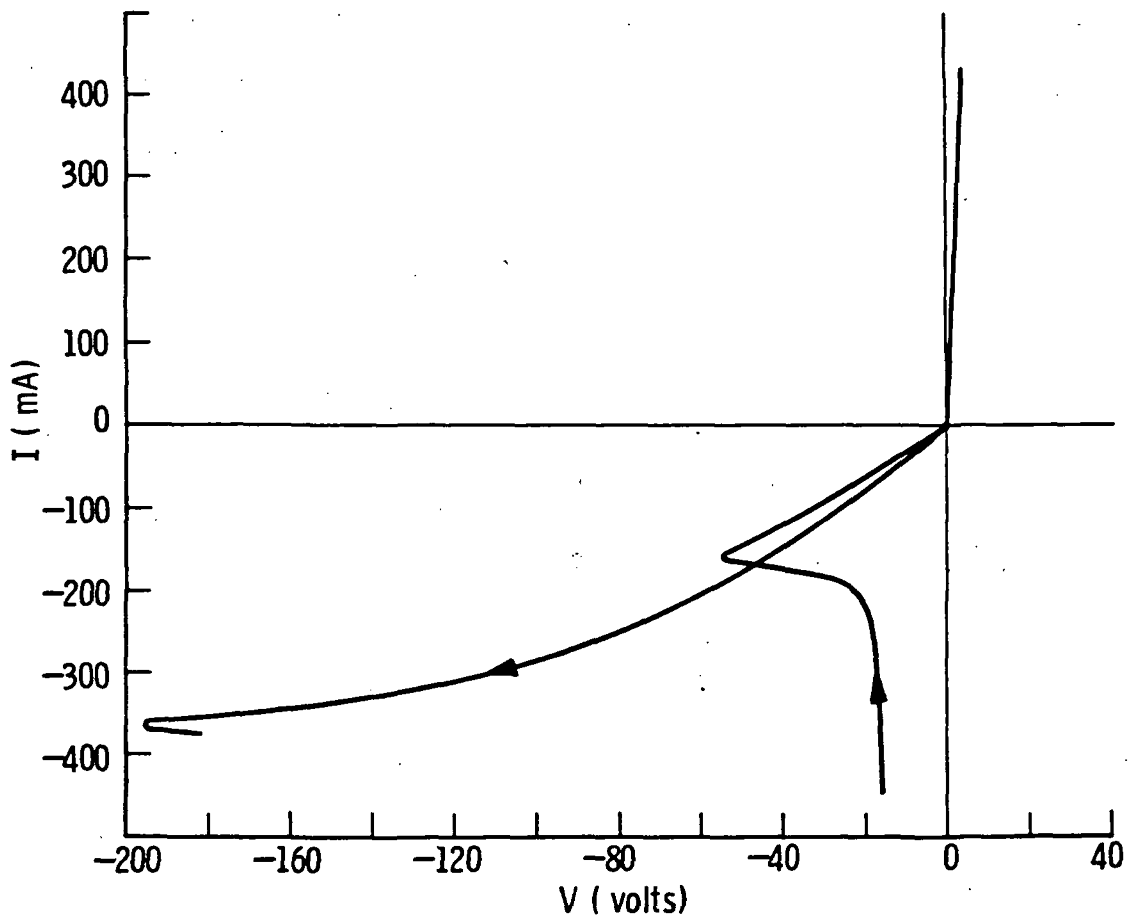

Figure 30. I-V curve of device A-3 on wafer 3-8. Gold diffusion method #2 was used with 300 Å of gold film at 1100°C.

Curve 749746-A

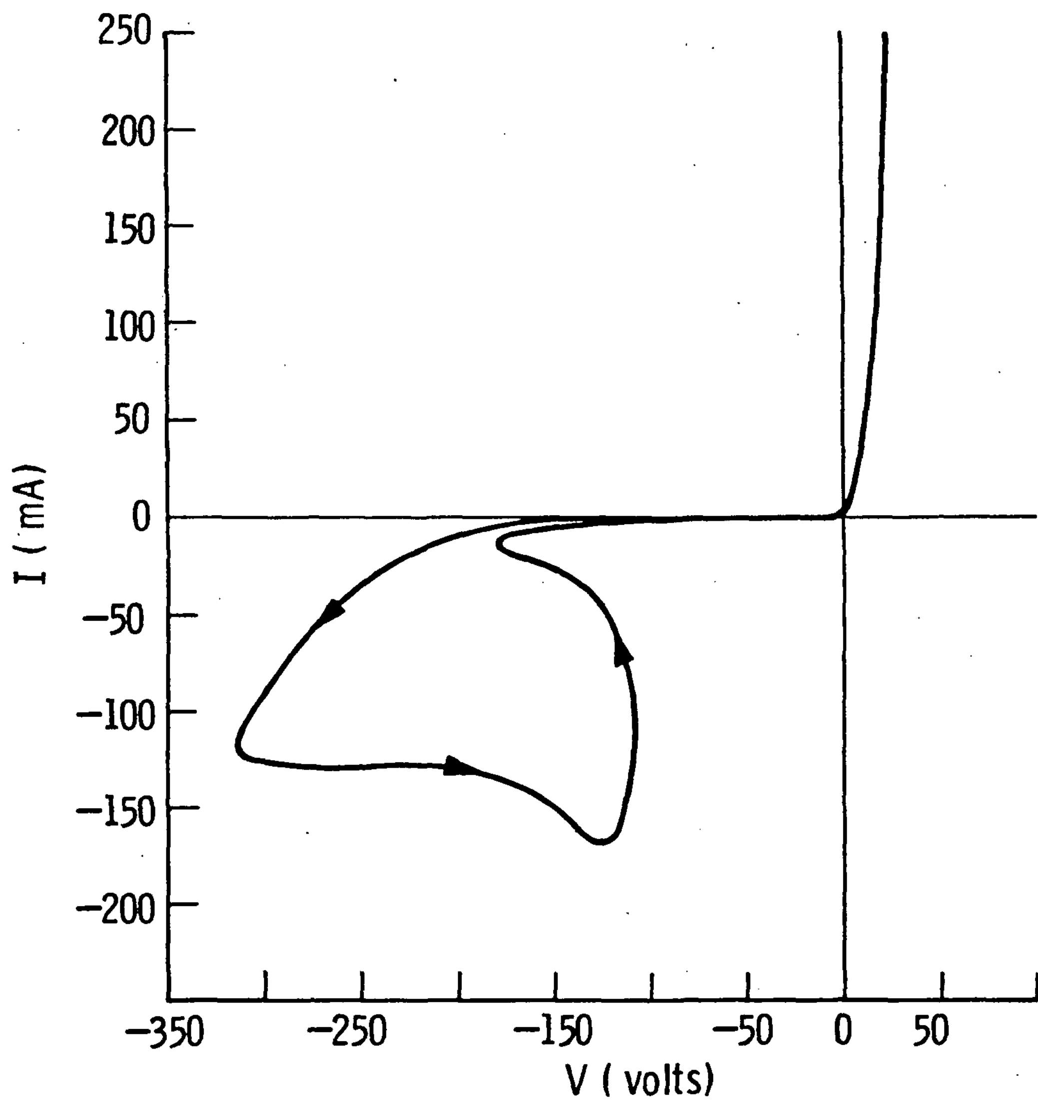

Figure 31. I-V curve of a device on wafer 3-7. Gold diffusion method #2 was used with 300 Å of gold film at 1100°C.

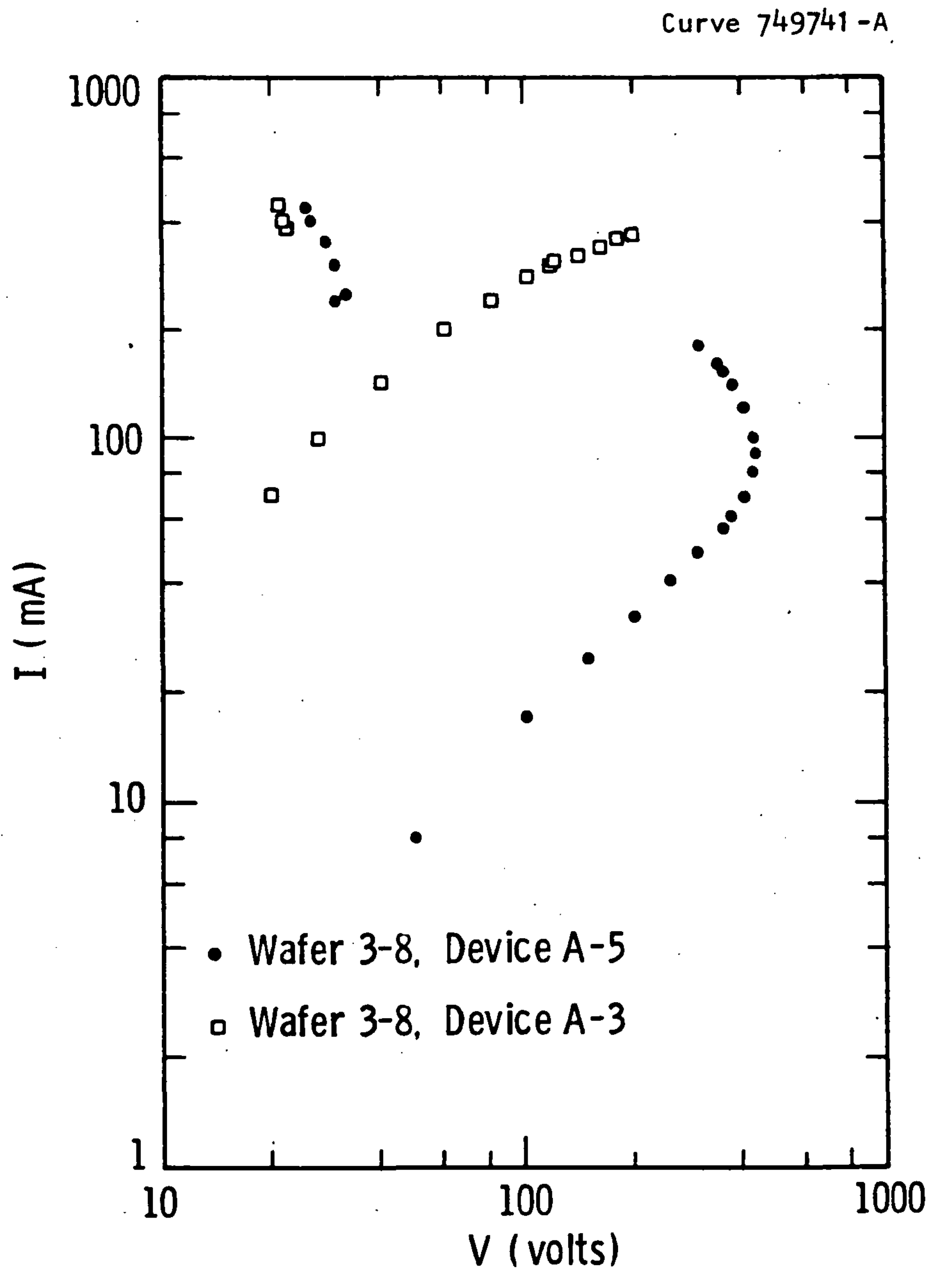

Figure 32. Devices produced using gold diffusion method #2 with 300 Å of gold film at 1100°C; both devices were good switches (see Figures 8 and 30).

Curve 749742-A

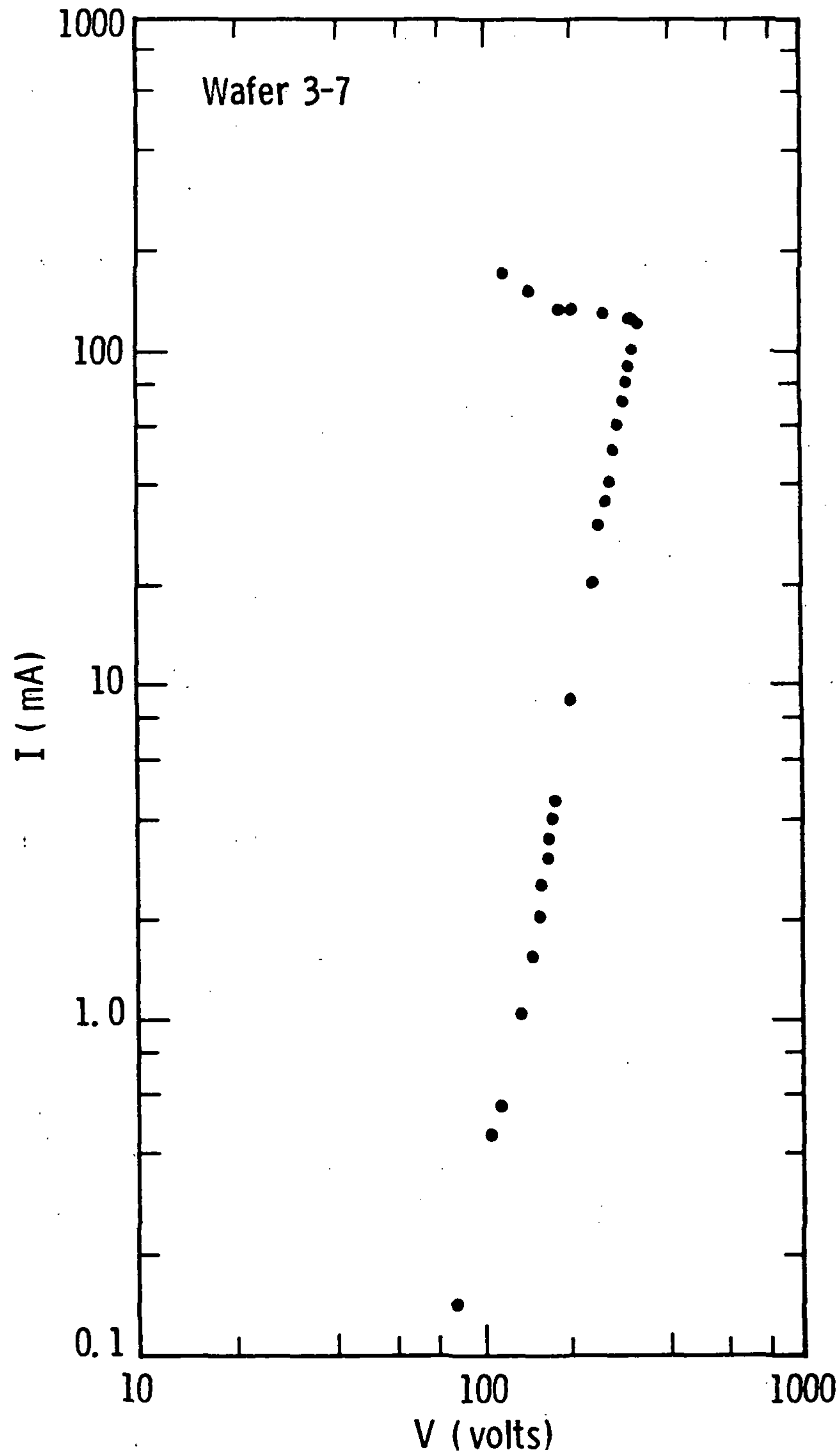

Figure 33. Device was produced using gold diffusion method #2 with 300 Å of gold film at 1100°C; this device was a good switch (see Figure 31).

In order to further elucidate what happened when the gold-diffused circular lateral device was sintered, the I-V curves were plotted on log-log paper (Figure 34). Before sintering, the device had a linear response ($I \alpha V$) right up to V_T = 1200 V (I = 0.6 mA) and then jumped to V = 65 V and I = 260 mA (response is similar to Figure 9a). In contrast, the I-V curve after sintering was continuous (similar to Figure 9c) and had a linear response only out to about 350 V (about half of V_T). There was a square law ($I \alpha V^2$) response from 350 V to 620 V. In addition, the leakage current for the device before sintering is about 30 times less than for the device after sintering ($V < V_T$).

For vertical devices that were irradiated but not annealed, the I-V data for different-sized electrodes were plotted on log-log paper. Figure 35 shows the response for the 1000 × 1000 μm^2 electrodes.

The results for the other electrodes were qualitatively the same. Table 24 displays the results for the four different-sized electrodes. The initial slope was approximately 1.0 for the devices, which corresponds to Ohm's Law, and the second slope was approximately 2.0, which corresponds to the space-charge-limited regime. For the two smallest electrodes, the crossover voltage (when the slope changes) occurred so close to the threshold voltage, V_T, that the second slope was not measurable. These results correspond to Lambert's theory. Note that the crossover voltage, V_{tr}, becomes a smaller fraction of the threshold voltage, V_T, as the size of the electrodes increases.

A possible figure of merit for the off-resistance, R_B (i.e., the ratio V/I in the Ohm's Law regime), is R_B/ρ for the experimental value (ρ is the measured value of resistivity) and $R/\rho = L/A$ for the theoretical value (L = cathode-anode spacing and A = area of effective electrode). The effective electrode area is the area of either the phosphorus diffusion area or the boron diffusion area (the two areas are equal to each other), i.e.,

$500 \times 500\ \mu m^2 \rightarrow 350 \times 350\ \mu m^2$
$1000 \times 1000\ \mu m^2 \rightarrow 710 \times 710\ \mu m^2$
$1500 \times 1500\ \mu m^2 \rightarrow 1000 \times 1000\ \mu m^2$
$2000 \times 2000\ \mu m^2 \rightarrow 1410 \times 1410\ \mu m^2$.

Curve 749740-A

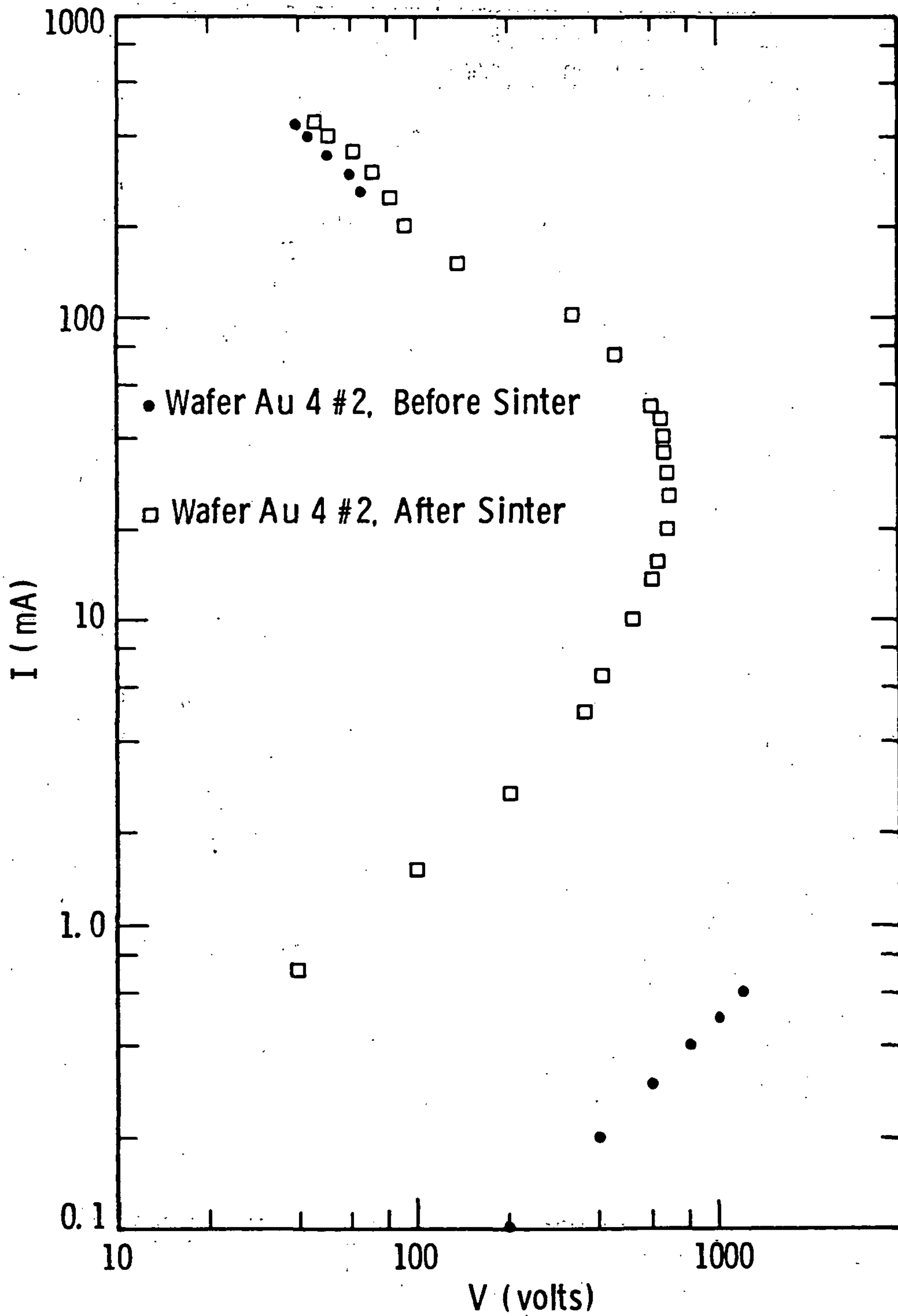

Figure 34. This device was produced using gold diffusion method #1 at 1100°C. Before sintering the device was a better switch, and after sintering it was a poor switch.

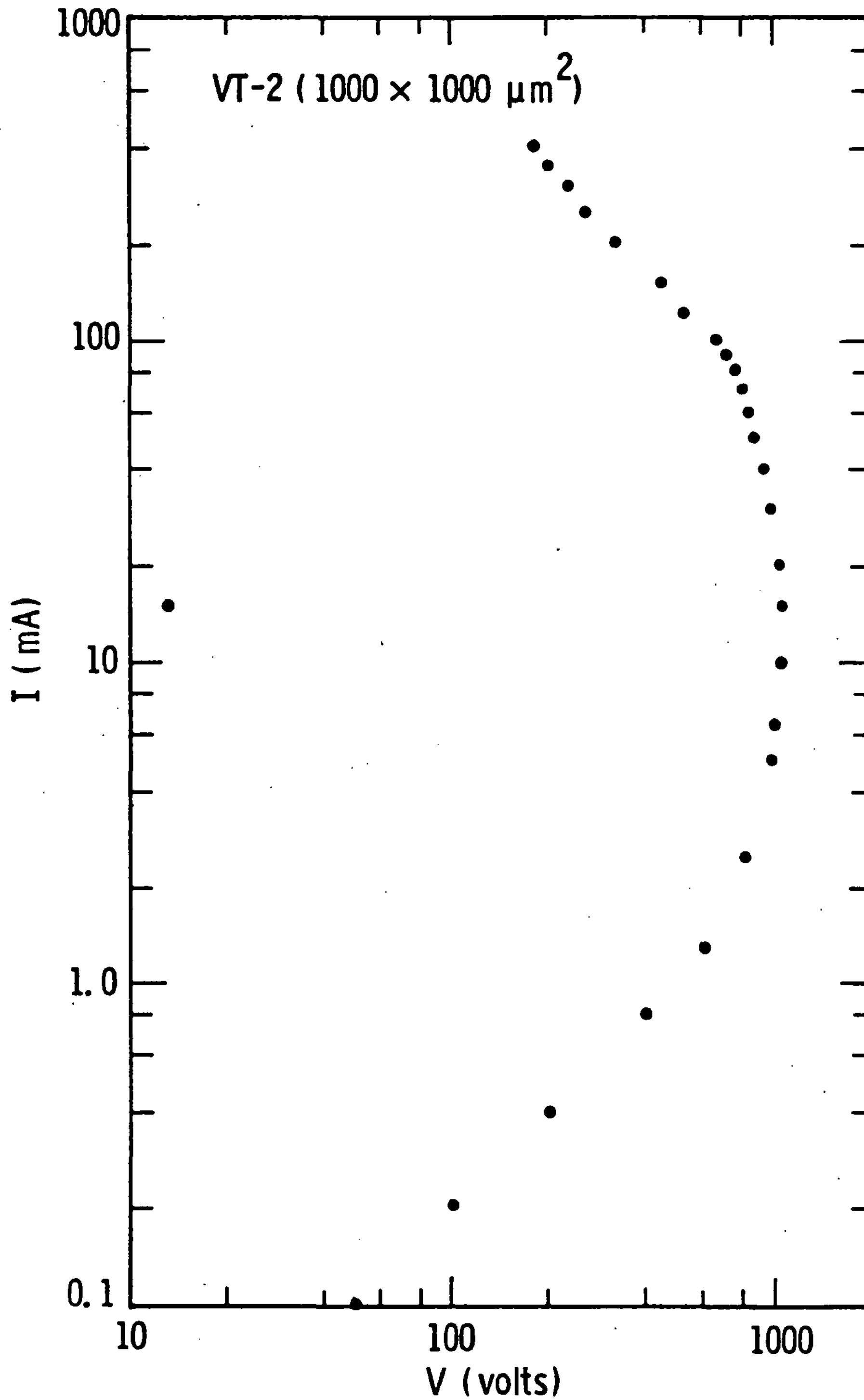

Figure 35. Sample number 2-9 (1300 ohm-cm starting material, 40 mil, vertical device) was irradiated with 2 MeV electrons at a dose of 6.7×10^{16} cm^{-2}. The electrodes were 1000 × 1000 μm^2. This device was a poor switch.

Table 24. Sample Number 2-9 (1300 ohm-cm starting material, 40 mil, vertical device) was irradiated with 2 MeV electrons at a dose of 6.7×10^{16} cm^{-2}.

Dimension of Electrode	Initial Slope	Second Slope	V_{tr} Crossover Voltage	V_T	V_{tr}/V_T
500 × 500 μm^2	0.6	-	800 V	1100 V	0.73
1000 × 1000	1.0	-	750 V	1050 V	0.71
1500 × 1500	1.6	2.15	700 V	1080 V	0.65
2000 × 2000	0.92	~2.0	360 V	640 V	0.56

Table 25 shows that the experimental value (R_B/ρ) does not change much with thickness or electrode area for the unannealed samples. For the annealed sample, 1-2 (good switch), the experimental value is nearly an order of magnitude higher than the theoretical value, L/A.

4.4 Annealing of Virgin Wafers

In order to garner some insight into what happens to the silicon during the 475°C anneal of vertical devices (Section 2.5.3) or the sintering of lateral devices (Section 4.2.1), a number of samples of different resistivity (all n-type) were annealed. The samples were measured with the four-point probe and then annealed at 475°C for a period of one hour for each anneal. Samples E and F were Czochralski grown and the rest of the samples were float-zoned. When silicon is heated in the temperature range around 450°C, a large number of donors are produced.[36] The results for samples D, E, and F (see Table 26) are similar to those reported in the literature. The oxygen concentration in Table 27 is estimated by using Figure 2 in Reference 36. Sample D, which is float-zone material, ends up with about half as many oxygen donor states as E and F, which are Czochralski grown. Other than that, sample D does not particularly stand out from samples E and F.

Table 25. All samples were vertical devices made from 1300 ohm-cm starting material and were irradiated with 2 MeV electrons. Samples 2-2, 2-6, and 2-9 were given a dose of 6.7×10^{16} cm^{-2} and were not annealed (not good switches). Sample 1-2 was given a dose of 10^{17} cm^{-2} and was annealed at 500°C for 200 minutes (was a good switch). The resistivity of samples 2-2, 2-6, and 2-9 was about 10^5 ohm-cm, while that of sample 1-1 was 70.5 ohm-cm.

Sample	Thickness	Dimension of Electrode	R_B	$\frac{R}{\rho} = \frac{L}{A}$ (Theory)	$\frac{R_B}{\rho}$ (Exp)
2-2	10 mil	500 × 500 μm^2	400 k-ohm	21 cm^{-1}	4 cm^{-1}
2-6	20 mil	500 × 500	400	42	4
2-9	40 mil	500 × 500	400	84	4
2-9	40 mil	1000 × 1000	320	20.4	3.2
2-9	40 mil	1500 × 1500	320	10.3	3.2
2-2	10 mil	2000 × 2000	300	1.3	3
2-6	20 mil	2000 × 2000	300	2.6	3
2-9	40 mil	2000 × 2000	400	5.2	4
1-2	10 mil	500 × 500	13	21	184

The rest of the samples do not appear to develop oxygen donor states; in fact, sample 3-7 doesn't even change its resistivity (within experimental error). The other three samples actually increase in resistivity indicating the production of a small number of acceptor states.

This evidence along with that presented in Sections 2.5, 4.1, and 4.2 indicate that anneals in the 450 to 475°C range cause very complex changes in silicon, especially if it has a large number of deep levels.

Table 26. Resistivity of virgin wafers after 475°C anneals (each one-hour). Samples E and F were CZ and the rest were FZ.

Sample	Resistivity Before First Anneal (ohm-cm)	N_D cm^{-3}	First Anneal (ohm-cm)	Second Anneal (ohm-cm)	Third Anneal (ohm-cm)
A	16,100	$\sim 3 \times 10^{11}$	28,700	16,600	11,000
4-5	2,950	$\sim 10^{12}$	43,100	16,500	13,600
B	1,470	3×10^{12}	1,670	5,490	72,400
3-7	127	3.5×10^{13}	121	120	125
D	67.7	6.0×10^{13}	28	15.6	12.5
E	27.0	1.7×10^{14}	9.7	4.97	4.50
F	15.5	3.0×10^{14}	7.5	5.71	4.84

Table 27. Density of oxygen donors as the samples are annealed at 475°C for one hour each anneal. The density of donors of the virgin wafers is N_0 ($=N_D$); the densities after one, two, and three anneals are N_1, N_2, and N_3, respectively. Samples E and F are CZ and D is FZ

Sample	N_0	N_1	N_2	N_3
D	6.0×10^{13} cm^{-3}	1.6×10^{14} cm^{-3}	3.0×10^{14} cm^{-3}	4.0×10^{14} cm^{-3}
E	1.7×10^{14}	4.5×10^{14}	9.0×10^{14}	9.5×10^{14}
F	3.0×10^{14}	5.7×10^{14}	8.0×10^{14}	9.0×10^{14}

	ΔN_1 $N_1 - N_0$	ΔN_2 $N_2 - N_1$	ΔN_3 $N_3 - N_2$	ΔN $N_3 - N_0$
D	1.0×10^{14} cm^{-3}	1.4×10^{14} cm^{-3}	1.0×10^{14} cm^{-3}	3.4×10^{14} cm^{-3}
E	2.8×10^{14}	4.5×10^{14}	0.5×10^{14}	7.8×10^{14}
F	2.7×10^{14}	2.3×10^{14}	1.0×10^{14}	6.0×10^{14}

	$\frac{\Delta N_1}{N_0}$	$\frac{\Delta N_2}{N_0}$	$\frac{\Delta N_3}{N_0}$	$\frac{\Delta N}{N_0}$	$\frac{\Delta N_{max}}{\Delta_t}$	Oxygen Concentration
D	1.67	2.33	1.67	5.67	1.4×10^{14} cm^{-3}/hr	6.2×10^{17} cm^{-3}
E	1.65	2.65	0.29	4.59	4.5×10^{14}	8.5×10^{17}
F	0.90	0.77	0.33	2.00	2.3×10^{14}	6.8×10^{17}

5. CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

The $(DI)^2$ devices seem to offer certain performance advantages over conventional p-n junction devices. The threshold voltage is controlled by the bulk properties instead of the depletion zones as with a p-n junction, and therefore the possibility exists of much higher voltage switches.

New methods of gold diffusion were devised. Method #2 used a thin gold film (200 - 300 Å) on the back of the device wafer and method #3 used this film along with a water quench after the gold diffusion. (Method #1 is the procedure devised by Henderson and co-workers at the University of Cincinnati.) Both new methods seemed to produce high-resistivity wafers with a great deal more consistency than method #1. Four-point probe measurements seemed to indicate that method #3 was better than method #2, but results with spreading resistance measurements did not allow one to differentiate between the two methods. Both methods will be pursued in order to determine which one gives more consistent and controllable results. If they both produce the same results, then method #2 will be used since it is the less cumbersome of the two.

For gold diffusion using method #1, the best device had V_T = 1340 V, V_H = 50 V, and R_B = 2.5 M-ohm. This device and others like it were classified as better switches and poor switches but none were good switches. However, using gold diffusion method #2, devices that were good switches were produced. The devices were measured to switch in one microsecond and the best device had V_T = 530 V, V_H = 25 V, and a leakage current of 100 mA. Devices that were made using gold diffusion method #3 were not good switches but they had injection gates and some gating effects were measured.

The best vertical devices produced using radiation without any anneal had V_T = 1250 V, V_H = 180 V, and R_B = 400 k-ohm. None of these devices were classified as good switches and there seemed to be no level of radiation that would produce a good switch. The parameters V_T, V_H, and R_B improved as the dosage increased until at some value (~ 10^{17} cm^{-2}) they began to degenerate. An anneal (475°C) following the irradiation did produce good switching devices with the best having V_T = 32 V and V_H = 1 V. The highest V_T for the 2 MeV electron radiation followed by an anneal was 70 V (V_H = 15 V). Proton irradiation followed by an anneal gave V_H = 0.8 V with V_T = 10.8 V.

The parameters of the circular lateral devices showed deterioration after being sintered. Of the three possible causes considered it was felt that annealing of bulk defect levels was the most probable, though the effect of a change in density of the surface states was not totally ruled out. The gettering of the gold by the phosphorus and boron was not considered to be a probable cause of this deterioration.

Since annealing and sintering seem to play such an important role in both the vertical devices and the lateral devices, it was decided to look at the effects of sintering conditions on virgin wafers. For three wafers (67.7, 27.0, and 15.5 ohm-cm) the results were as expected, i.e., oxygen donors were formed and the wafers became more n-type. However, for the higher resistivity the results were not anticipated, e.g., the 127 ohm-cm wafer did not change resistivity with the anneals and for higher resistivity material the anneal seemed to produce acceptors as well as donors.

The examination of the dependence of the current on the voltage was investigated for $V < V_T$. Some of the devices showed the expected behavior, i.e., a linear region followed by a quadratic region, but other devices showed behavior which cannot be explained by Lampert's theory.

The work has been quite successful and there is a great deal of promise in the results, but there is still a lot of scientific and engineering work that needs to be done in order to produce a good switch that can be gated on and has a high V_T, a low V_H, and a large R_B.

The areas that need further exploration include:

1. Determination of the proper conditions for gold diffusion (method #2 versus #3).

2. Determination, probably through DLTS (Deep-Level Transient Spectroscopy), of the levels produced thorough irradiation and annealing that give the low V_H values.

3. Determination of the optimum starting resistivity of the silicon.

4. Development of gating techniques for both the lateral and the vertical devices.

5. Determination of the optimum concentration and depth of the p^+ and n^+ areas of the electrodes.

6. Optimization of the electrode topology, the device structure, and the deep-level properties in order to attain specific current-voltage ratings and switching characteristics.

Progress in solving these problems should yield the technology for a new family of high-voltage and semiconductor switching devices.

Some specific recommendations that should elucidate some of these areas are as follows:

1. Design areas on all existing masks and new mask designs that would allow one to make DLTS, lifetime, CV, and four-point probe measurements on the same wafer that the devices are on.

2. Do gold diffusion with the vertical devices. The back side of the wafer would not have electrodes but would have a metal Schottky contact.

3. Design a new mask set for the lateral circular design that would have the p-i-n structure as well as the symmetric electrodes and many different cathode-anode spacings (L values).

6. ACKNOWLEDGMENTS

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