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ANNUAL REPORT
FOR
CONTRACT NO. NAS3-23781
20 GHz GaAs MONOLITHIC POWER AMPLIFIER MODULE DEVELOPMENT
18 May 1983 - 17 May 1984

Prepared for

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7 June 1984

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EXECUTIVE SUMMARY

This report covers work performed during the first 12 months of Contract No. NAS3-23781, a 36-month program for the development of a 20 GHz GaAs FET monolithic power amplifier module for advanced communication applications. Several amplifier design approaches were pursued to accomplish the program goals. Four-way power combining of four 0.6 W amplifier modules is used as the baseline approach. For this purpose, a monolithic four-way traveling-wave power divider/combiner was developed. Over a 20 GHz bandwidth (10 to 30 GHz), an insertion loss of no more than 1.2 dB was measured for a pair of back-to-back connected divider/combiners. Isolation between output ports is better than 20 dB, and VSWRs are better than 2:1

A distributed amplifier with six 300 μm gate width FETs and gate and drain transmission line tapers has been designed, fabricated, and evaluated for use as an 0.6 W module. This amplifier has achieved state-of-the-art results of 0.5 W output power with at least 4 dB gain across the entire 2 to 21 GHz frequency range. An output power of 2 W was achieved at a measurement frequency of 18 GHz when four distributed amplifiers were power-combined using a pair of traveling-wave divider/combiners.

Another approach is the direct common-source cascading of three power FET stages. An output power of up to 2 W with 12 dB gain and 20% power-added efficiency has been achieved with this approach (at 17 GHz). The linear gain was 14 dB at 1 W output. The first two stages of the three-stage amplifier have achieved an output power of 1.6 W with 9 dB gain and 26% power-added efficiency at 16 GHz.

SECTION I
INTRODUCTION

This report covers the first 12 months of a 36-month contract for the development of a 20 GHz GaAs FET monolithic power amplifier module for advanced communication applications. The objective of this program is to develop 20 GHz high power (2.5 W saturation, 1.5 W linear), high efficiency (20% at saturation), high gain (> 15 dB), wide bandwidth (19 to 21 GHz) monolithic GaAs FET amplifier modules for future satellite communication systems.

Several amplifier design approaches were pursued to accomplish the program goals. Four-way power combining of four 0.6 W amplifier modules is used as the baseline approach. For this purpose, a monolithic four-way traveling-wave power divider/combiner was developed. A distributed amplifier with six 300 μm gate width FETs and gate and drain transmission line tapers has been designed, fabricated, and evaluated for use as an 0.6 W module. This amplifier has achieved an output power of 0.5 W with at least 4 dB gain across the entire 2 to 21 GHz frequency range. Another approach is the direct common-source cascading of three power FET stages. An output power of up to 2 W with 12 dB gain and 20% power-added efficiency has been achieved with this approach.

The amplifier requirements and design approaches are discussed in Section II. The development of the divider/combiner submodule, the distributed amplifier submodule, and the three- and four-stage amplifier submodules is covered in Section III. Section IV discusses the monolithic power amplifier configuration. Technical achievements during this report period are summarized in Section V. Plans for the next period are given in Section VI.

SECTION II
AMPLIFIER REQUIREMENTS AND DESIGN APPROACHES

A. Amplifier Requirements

The detailed objective requirements for the GaAs FET monolithic power amplifier module are given in Table 1. The basic objective is to develop 19 to 21 GHz, high power (2.5 W at saturation, 1.5 W linear), high efficiency (20% at saturated power output), high gain (15 dB) GaAs FET monolithic power amplifier modules for advanced communication applications.

B. Design Approaches

To achieve the 2.5 W saturated output power at > 15 dB gain, a multistage amplifier must be used for the GaAs monolithic FET power amplifier module. The linearity requirements also dictate the use of at least an equivalent 6 mm gate width device for the output stage. One of the possible amplifier configurations is shown in Figure 1(a), which illustrates a three-stage amplifier consisting of 1.2 mm, 2.4 mm, and 6.0 mm FETs. The projected power and gain of each stage are also shown. Section III.C of this report details the design, fabrication, and evaluation results of this approach.

Another approach for the cascaded amplifier design is to use circuit-level power combining of the power outputs of lower power amplifiers, using smaller FETs for ease in impedance matching. With a four-way power combiner, the component amplifier should have a power output of ~ 600 mW (saturated). A suitable cascaded amplifier configuration is shown in Figure 1(b). FETs with gate widths of 0.3 mm, 0.3 mm, 0.6 mm, and 1.5 mm are used. These gate widths are the same as those for the four-stage, single-gate module of NASA Contract No. NAS3-22886.[1,2] A distributed amplifier approach using 6 x 0.3 mm FETs was also designed, fabricated, and evaluated. An output power of up to 700 mW has been achieved. The design approach is descussed in Section III.B.

Because it offers topological, bandwidth, and isolation advantages, the traveling-wave divider/combiner approach reported by Bert and Kaminsky[3] was adopted for monolithic implementation on GaAs substrates. A four-way divider/combiner suitable for power combining of monolithic amplifier modules is described in Section III.A.

Table 1

Objective Requirements of the

20 GHz GaAs FET Monolithic

Power Amplifier Module

3.1.1 Electrical and RF Performance Objective Requirements

3.1.1.1 The GaAs FET Power Amplifier Module shall make maximum feasible use of monolithic technology to simultaneously optimize device gain, power, efficiency, and bandwidth.

3.1.1.2 RF Band: The RF band shall be from 19.0 to 21.0 GHz.

3.1.1.3 RF Output Power: The RF output power shall be greater than or equal to 2.5 watts at saturation and 1.5 watts linear (-20 dB 3rd Order Intermodulation Products).

3.1.1.4 RF Gain: The RF gain shall be greater than or equal to 15 dB.

3.1.1.5 Gain Variation: The maximum gain shall not vary more than 1 dB over the entire 2.0 GHz bandwidth and 0.5 dB over any 500 MHz band.

3.1.1.6 Module Power Added Efficiency: The module power added efficiency shall be equal to or greater than 20% at saturation and 15% under linear operation (see 3.1.1.8).

3.1.1.7 Impedance: The nominal input and output impedance shall be 50 ohms. The input and output VSWR shall be less than or equal to 1.3:1.

3.1.1.8 Linearity: Third order intermodulation products shall be less than or equal to -20 dbc under linear operation.

3.1.1.9 Noise Figure: The noise figure at room temperature shall be less than or equal to 20 dB.

3.1.1.10 AM/PM Conversion: The AM/PM conversion shall not exceed 3°/dB.

3.1.1.11 Harmonic and Spurious Response: The harmonic response shall be at least -30 dbc. The spurious response shall be at least -60 dbc.

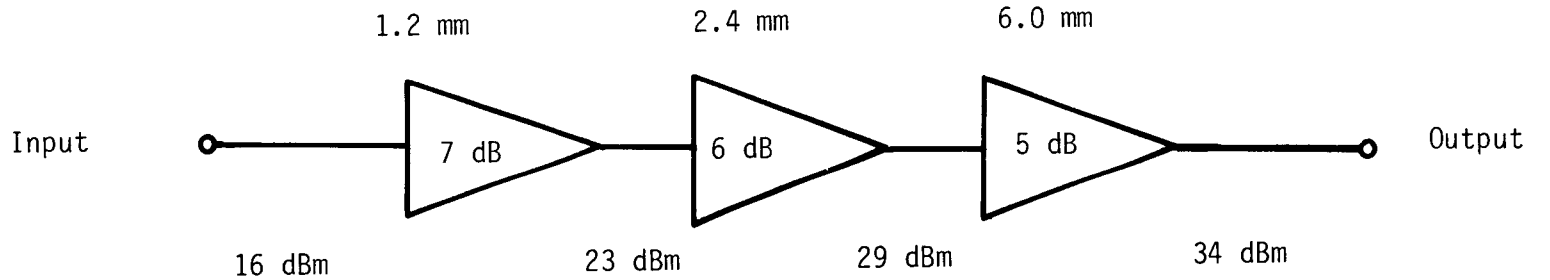
Table 1
(Continued)

3.1.1.12 Maximum FET Channel Junction Temperature: The maximum FET channel junction temperature under worst case thermal conditions shall not exceed 110°C.

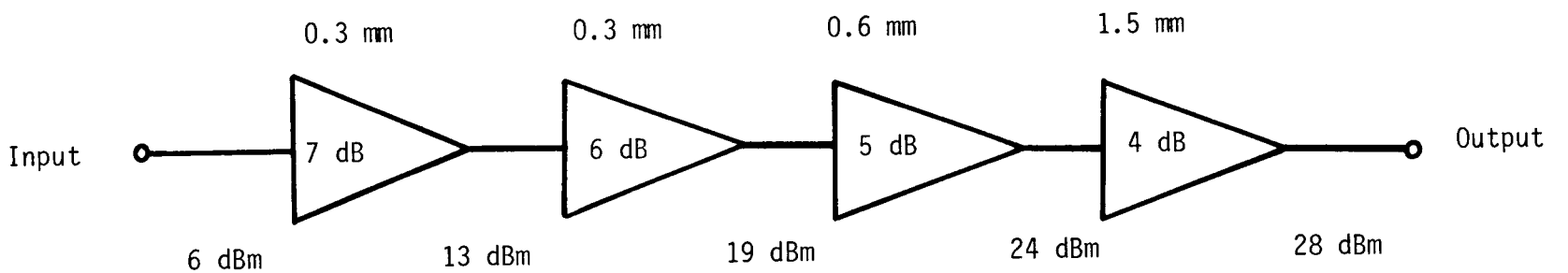
3.1.1.13 Module to Module Gain Variation: For any module, the gain at any given frequency in the bandwidth shall vary by no greater than ± 0.4 dB from the RMS average for all the modules at the given frequency.

3..1.1.14 Module to Module Phase Shift Variation: For any given module, the phase shift at any given frequency in the bandwidth shall vary by no greater than ±10 degrees from the RMS average for all the modules at the given frequency.

3.1.1.15 Group Delay Variation: The group delay variation at and below saturation shall not exceed 0.5 nanoseconds over any 0.5 GHz portion of the operating frequency.



(a)



(b)

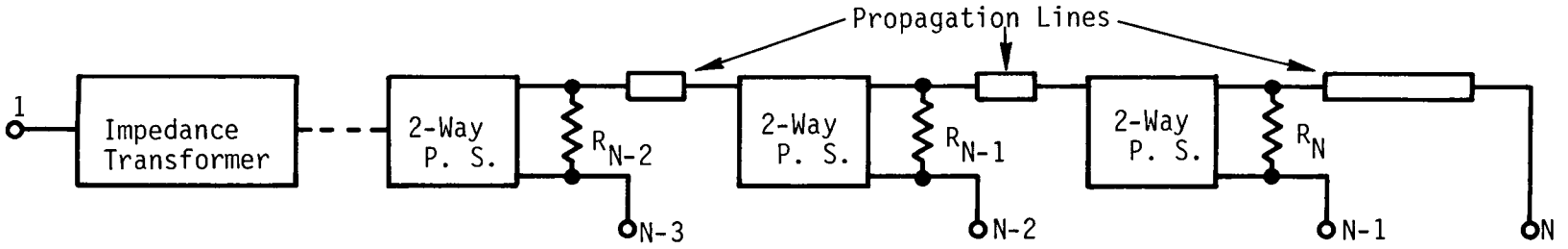
Figure 1 Power Amplifier Configurations
(a) 2.5 W Output
(b) 0.6 W Output

SECTION III
SUBMODULE DEVELOPMENT

A. Monolithic Traveling-Wave Divider/Combiner

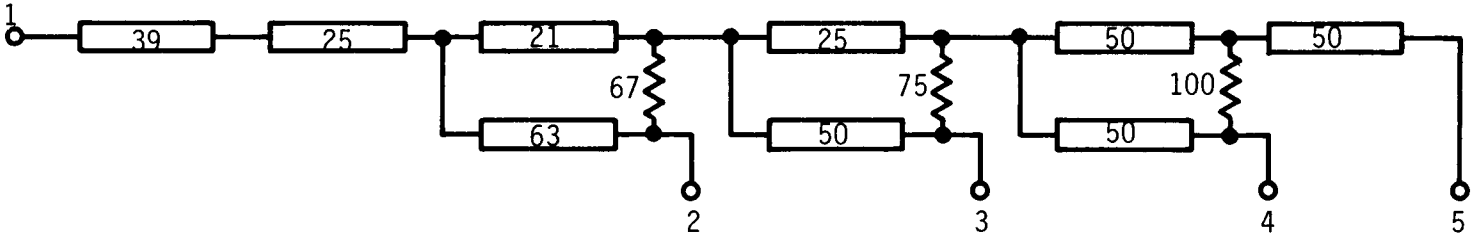
A general configuration for a traveling-wave power divider/combiner for broadband power combining of GaAs FET amplifiers is shown in Figure 2(a). Impedance values of a four-way divider (combiner) are shown in Figure 2(b). All the impedance transformers are 0.25 wavelength at center frequency. Resistors are used to improve port-to-port isolation. For a design center frequency of 20 GHz, the calculated VSWR, power coupling, and isolation are as shown in Figures 3 and 4. The power coupling of the four ports is displayed in Figure 3 along with the input VSWR and output VSWR of port 2 [see Figure 2(b) for port identification]. Since the deviation of the power coupling from the theoretical value (-6 dB) is less than 0.1 dB, the four curves lie within the heavy line shown over the 3:1 bandwidth of 10 to 30 GHz. The calculated VSWRs of all ports are, in general, less than 1.2:1 from 15 to 25 GHz. The broadband isolation characteristics are shown in Figure 4 between the ports indicated. Better than 35 dB isolation is seen across the 19 to 21 GHz band.

The first design of the monolithic four-way traveling-wave divider/combiner is shown in Figure 5(a) in slice form. Figure 5(b) shows a back-to-back connected divider/combiner in a test fixture. Input/output 50 ohm lines on alumina substrates are provided for ease in testing. SMA connectors are used for the input and output ports. A 6 mil ridge was provided for the divider/combiner chip to accommodate the difference in thickness of the alumina substrate (10 mils) and the GaAs substrates (4 mils). With the divider/combiner connected back-to-back as shown, a total insertion loss of no more than 1.2 dB has been obtained over the 10 to 20 GHz frequency range. With the fixture loss (~ 0.5 dB) subtracted, the intrinsic loss of the divider/combiner is only ~ 0.7 dB (0.35 dB for either dividing or combining). These results were obtained with tuning on the second impedance transformers (25 ohms) having two 90° bends. Without tuning, the insertion loss dips at 12 GHz and 20 GHz (~ 3 dB). These effects are attributed to the proximity coupling of the transmission lines between the



(P. S. = Power Splitter)

(a) Schematic of a Traveling-Wave Power Divider



(b) Impedance Values for the Four-Way Traveling-Wave Divider

Figure 2 Passive Traveling-Wave Power Combiner

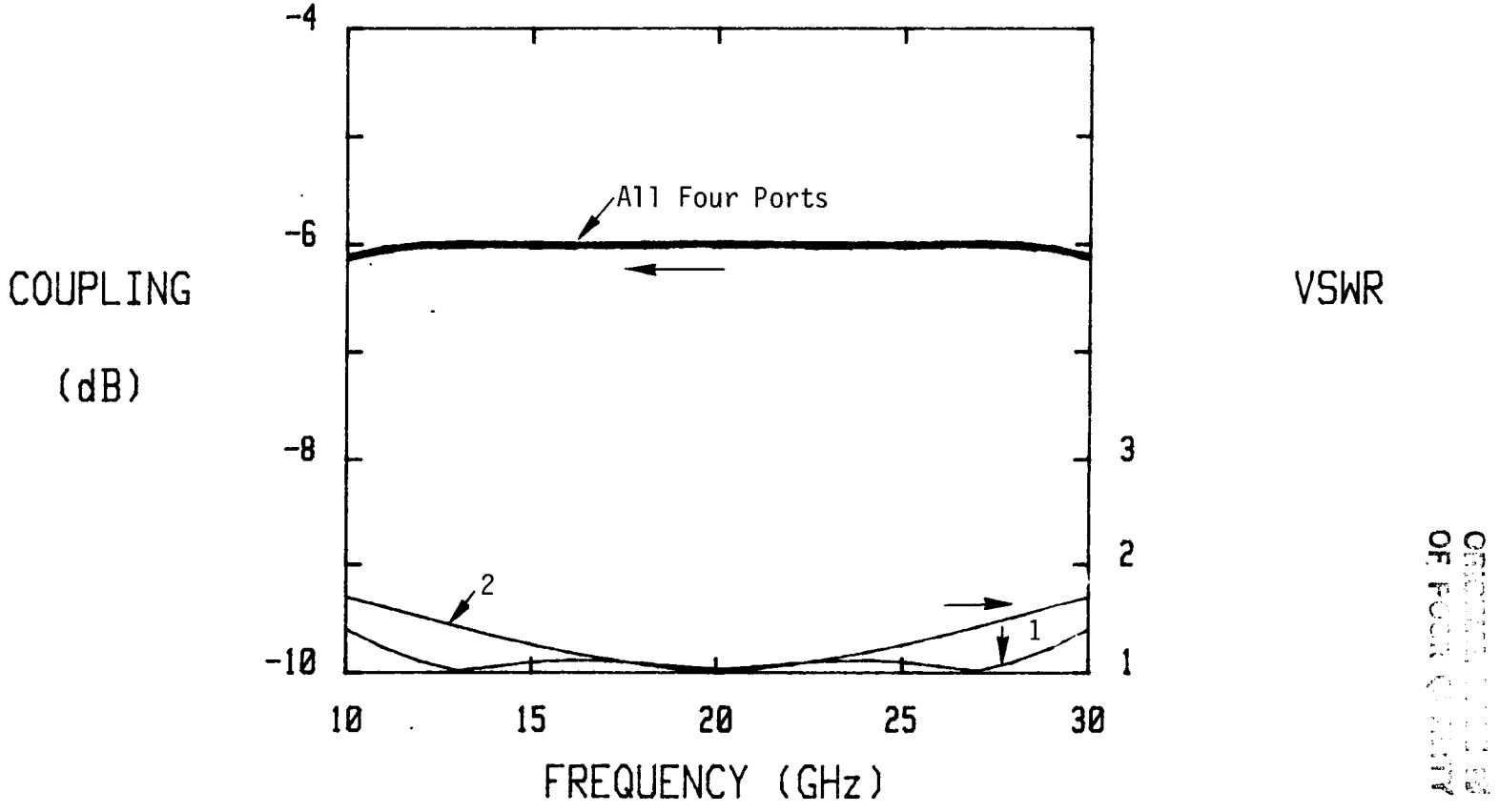


Figure 3 Power Coupling and VSWR Performance of the Traveling-Wave Divider

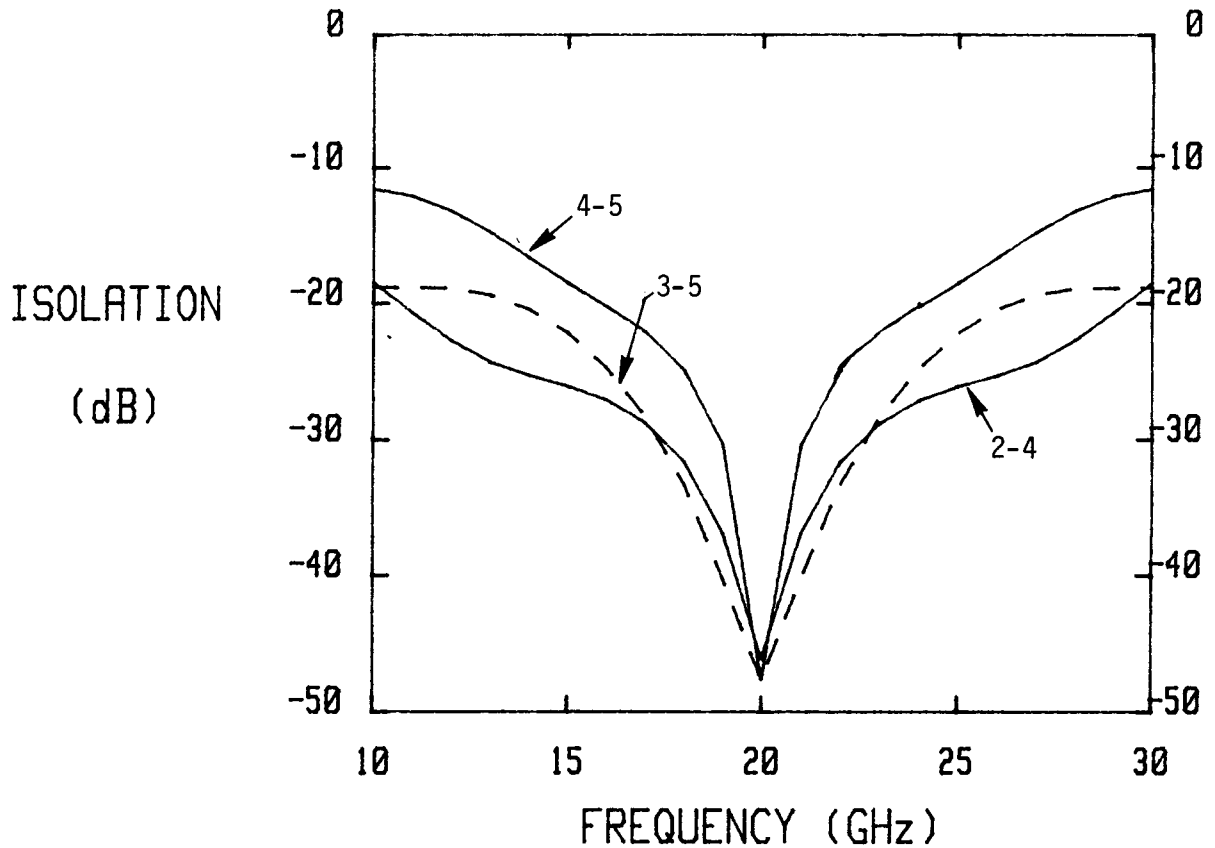
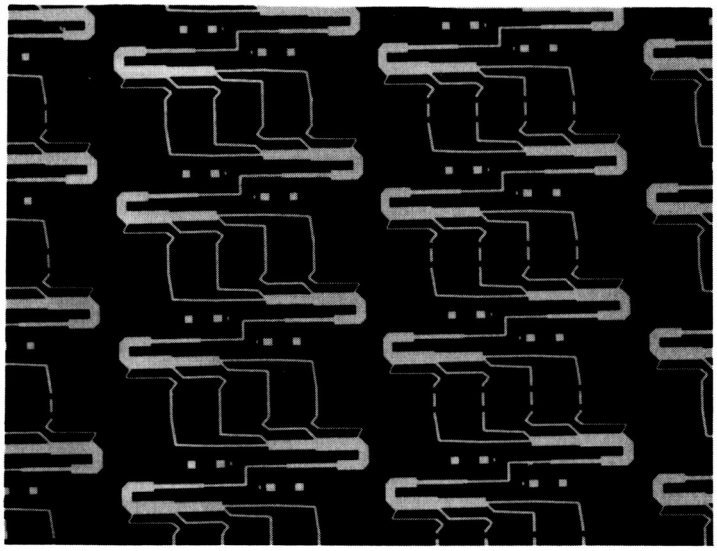
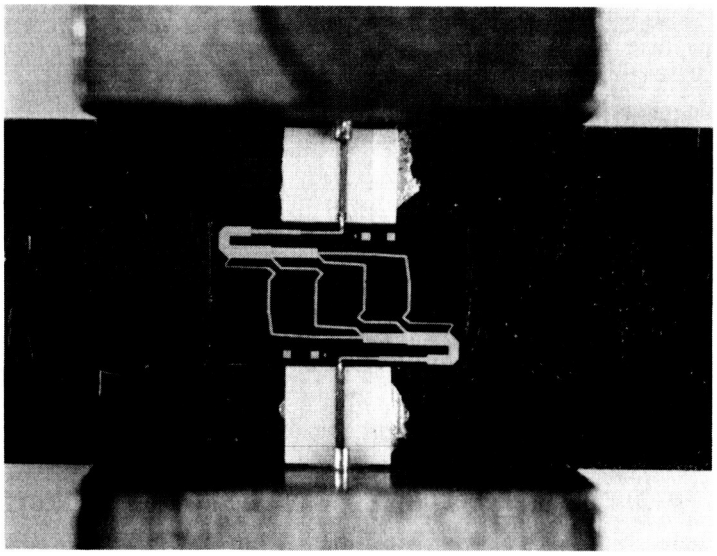


Figure 4 Isolation Characteristics of the Traveling-Wave Power Divider



(a)



(b)

Figure 5 Monolithic Four-Way Traveling-Wave Divider/Combiner
(a) Divider/Combiner in Slice Form
(b) Test Fixture

main divider/combiner sections and the two step transformers. The masks were subsequently modified by increasing the spacing to eliminate this problem.

Figure 6 shows a photograph of the revised divider/combiner in a "through" configuration. Except for reconfiguration of the second transformers, it is essentially the same as that described above. The second transformers are laid out so as to minimize the coupling between the input line and the main divider/combiner. With this revised design, the insertion loss dip seen at around 20 GHz for the old design disappeared.

Figure 7 shows the measured total insertion loss and input return loss of the divider/combiner connected back-to-back. Across the frequency range of 10 to 30 GHz, the total insertion loss is better than 1.2 dB with return loss better than 10 dB (2:1 VSWR). Figure 8 shows the isolation between the output ports. Better than 20 dB of isolation has been obtained across the 10 to 30 GHz band. Figures 9(a) and 9(b) show the measured performance within the 17 to 22 GHz band. The application of this state-of-the-art monolithic broadband power combiner in power combining of FET amplifiers is discussed in Section IV.

B. Distributed Amplifier

1. Amplifier Design

The distributed amplifier approach was utilized as early as 1948 by Ginzton, et al.,[4] as a means of extending the bandwidth of vacuum tubes. As applied to FETs, this approach couples the input and output circuits of a given number of active devices through input and output transmission lines, respectively. Figure 10 shows the classical interconnection of devices for a FET distributed amplifier. In the figure the capacitive reactances of the FET, C_g and C_d, have been incorporated into the shunt capacitive elements of the artificial transmission lines of characteristic impedance Z_{go} and Z_{do}, respectively.

From Figure 10 it can be seen (following Ginzton's analysis) that the gate-to-gate voltage gain is just

$$A_v = (g_m n/2)\sqrt{Z_{go} Z_{do}} \quad , \qquad (1)$$

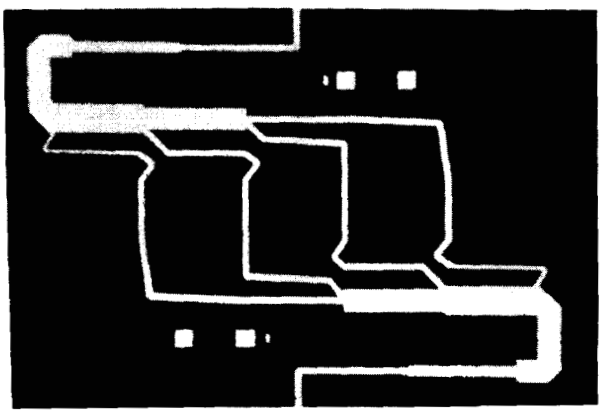


Figure 6 Revised Traveling-Wave Divider/Combiner in "Through" Configuration

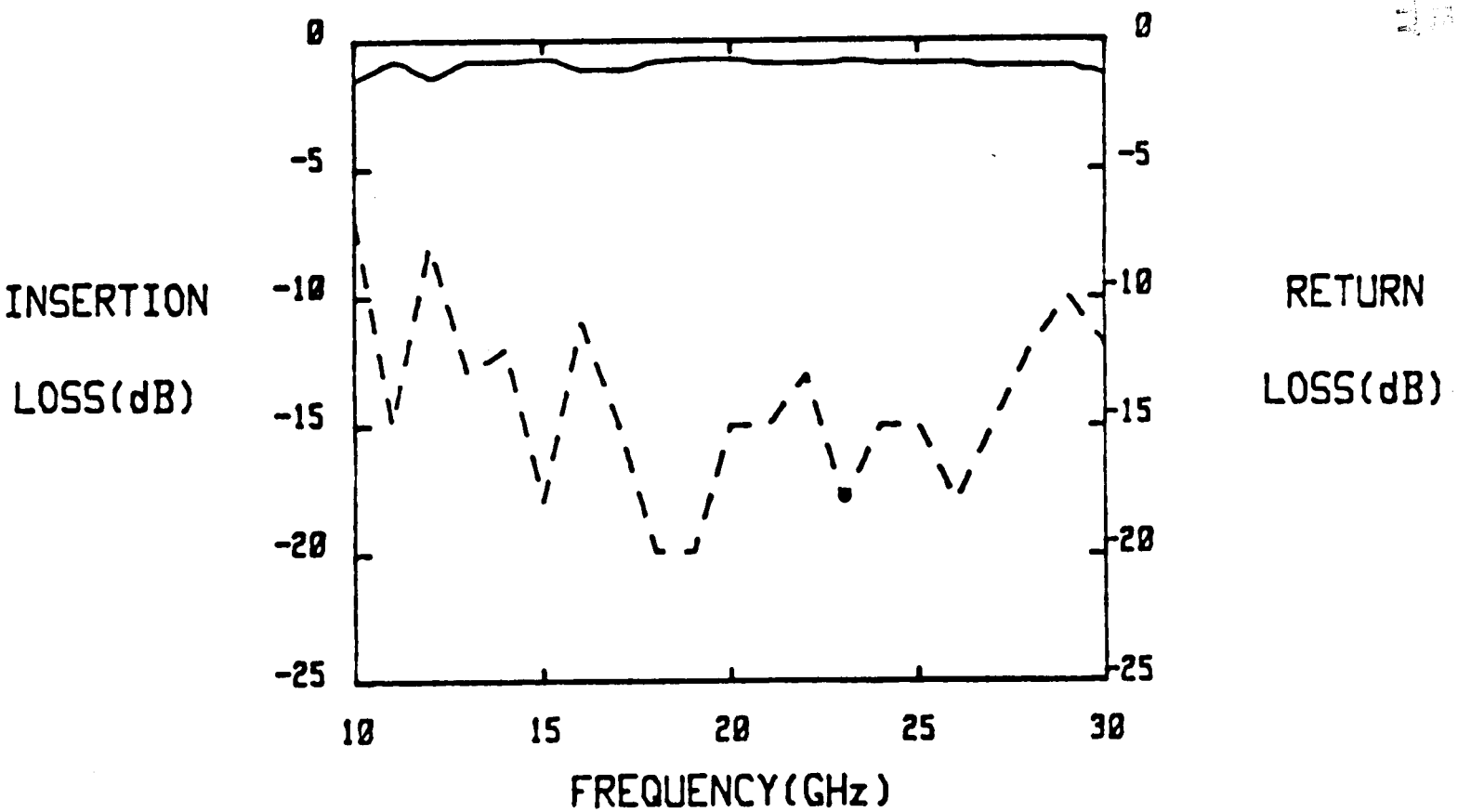


Figure 7 Insertion Loss and Input Return Loss of a Pair of Back-to-Back Connected, Monolithic, Four-Way Traveling Wave Divider/Combiners

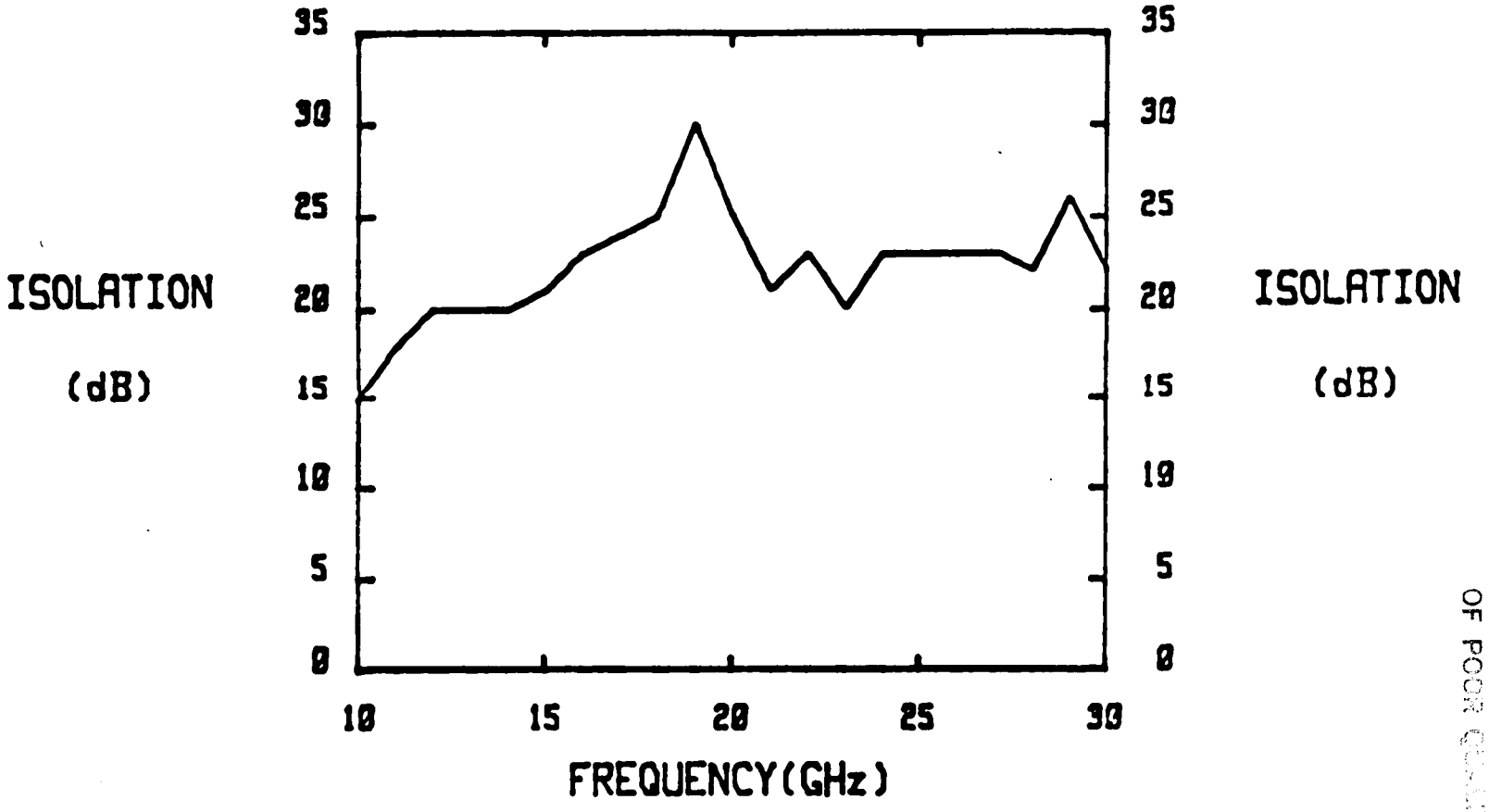
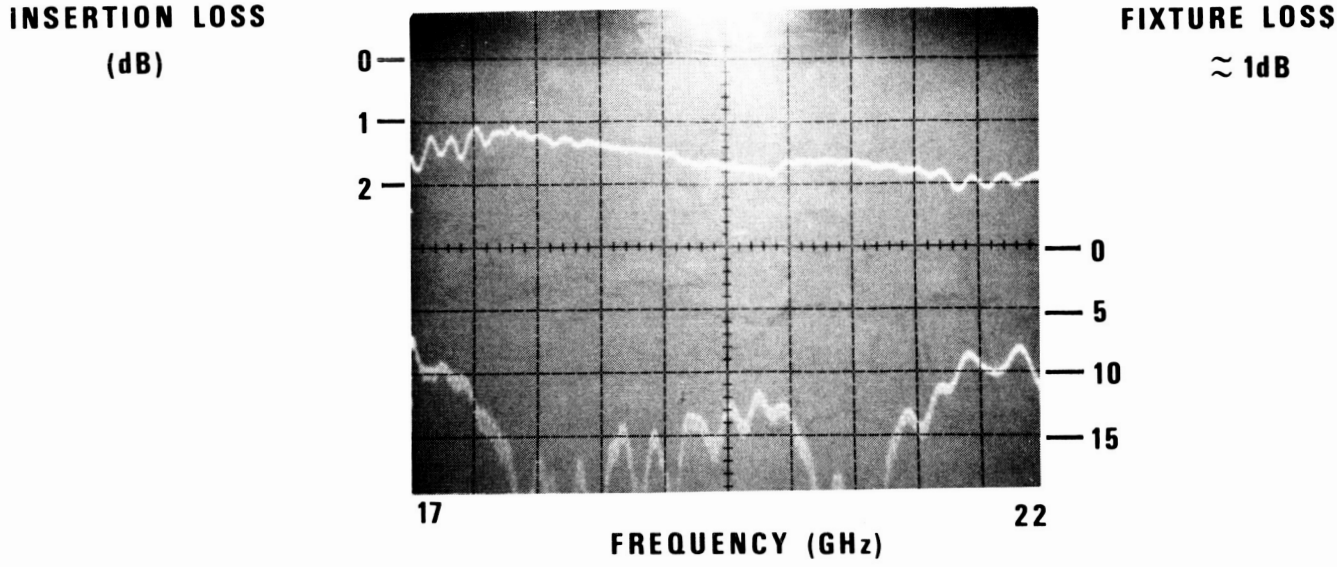
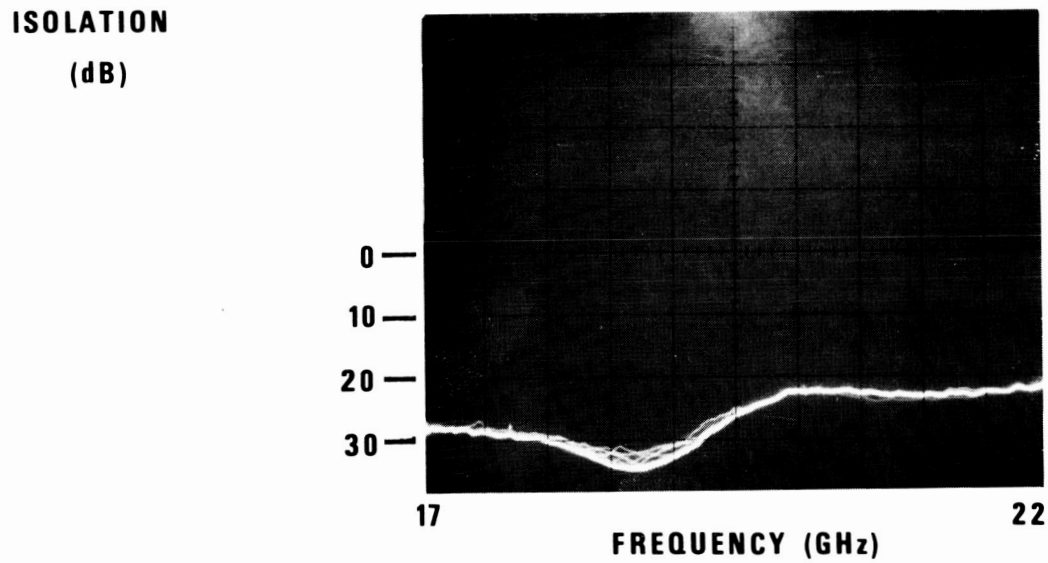


Figure 8 Output Port Isolation of a Four-Way Traveling Wave Divider/Combiner



(a) **INSERTION LOSS AND INPUT RETURN LOSS OF A BACK-TO-BACK CONNECTED MONOLITHIC TRAVELING-WAVE DIVIDER/COMBINER**



(b) **ISOLATION BETWEEN OUTPUT PORTS OF THE TRAVELING-WAVE DIVIDER (COMBINER)**

Figure 9 Performance of the Four-Way Divider/Combiner Across the 17 to 22 GHz Band

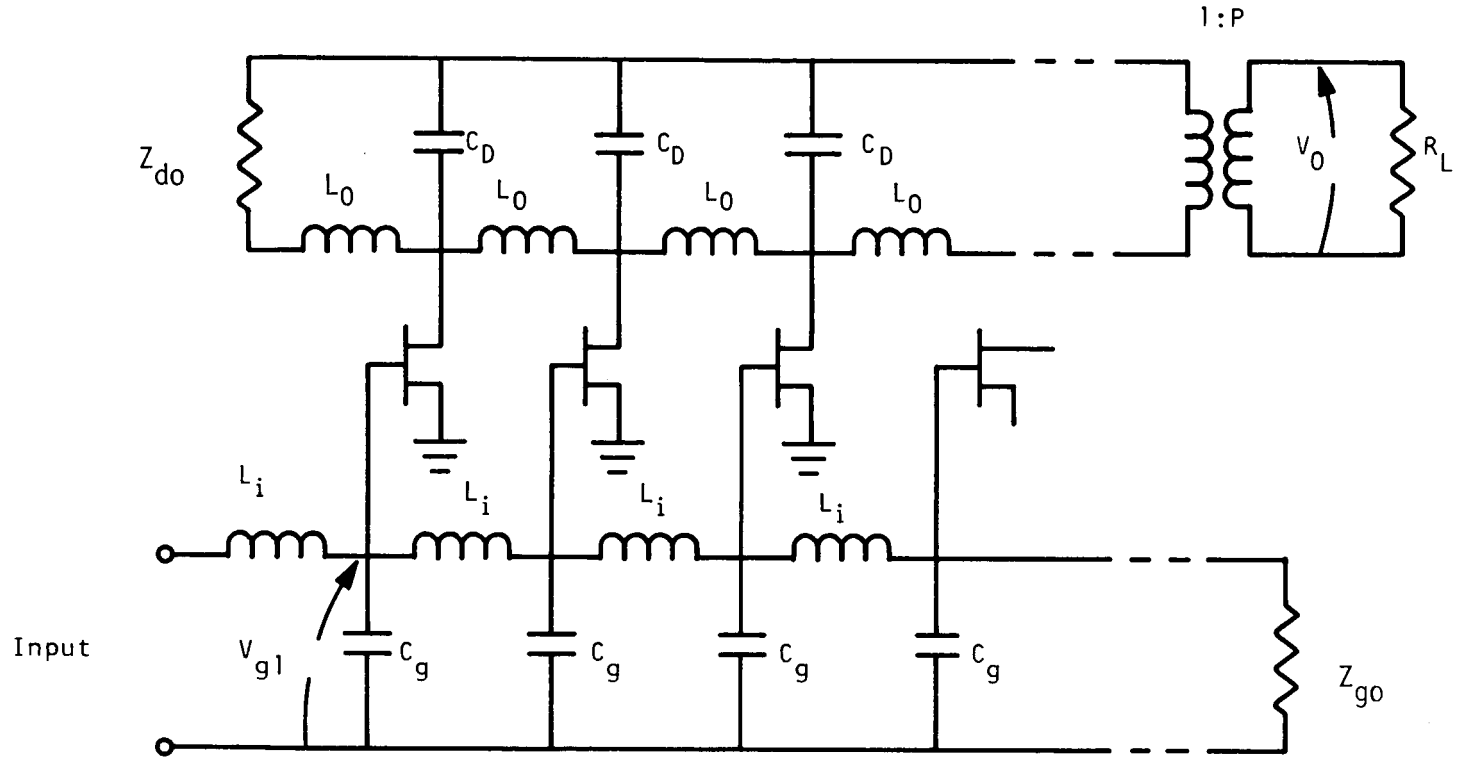


Figure 10 Distributed Amplifier

where n is the number of devices in the stage and g_m is the transconductance per device.

The real parts of the input and output impedances of the FET complicate the classical analysis of a distributed amplifier. The voltage gain of the lossy distributed amplifier is obtained by including the loss factor in the gain expression for the lossless case[5]:

$$A = \sum_{q=1}^{n} \frac{g_m \sqrt{Z_{go} Z_{do}}}{2} e^{-\alpha_g q_e - \alpha_d (n+1=q)} \quad . \qquad (2)$$

α_g and α_d, the gate and the drain attenuation coefficients, are given by

$$\alpha_g \approx (2\pi f\ C_g)^2\ R_g Z_{go}/2 \quad , \qquad [3(a)]$$

$$\alpha_d \approx Z_{do}/2R_d \quad . \qquad [3(b)]$$

Here f is operation frequency, R_g is the gate resistance, and R_d is the drain resistance. At 20 GHz attenuation coefficients for a 300 μm FET (see Figure 11) on a 50 Ω system are given by

$$\alpha_g = 0.61 \text{ napers/device} \quad ,$$
$$\alpha_d = 0.0625 \text{ napers/device} \quad .$$

Thus, significant losses are incurred as a result of dissipative loading by the gate and drain resistances of the FETs. The attenuation of the gate line is particularly severe and limits the maximum number of devices that can be connected.

To reduce the gate-line attenuation, a series capacitor[6] can be inserted between the FET gate and the transmission line as shown in Figure 12. The capacitor reduces the effective value of C_g of the gate line, resulting in a decreased α_g. This capacitor reduces the gain per device, but

R_g = 10 Ω
C_g = 0.4 pF
C_{dg} = 0.015 pF
G_m = 45 mmhos
R_d = 350 Ω
C_d = 0.07 pF

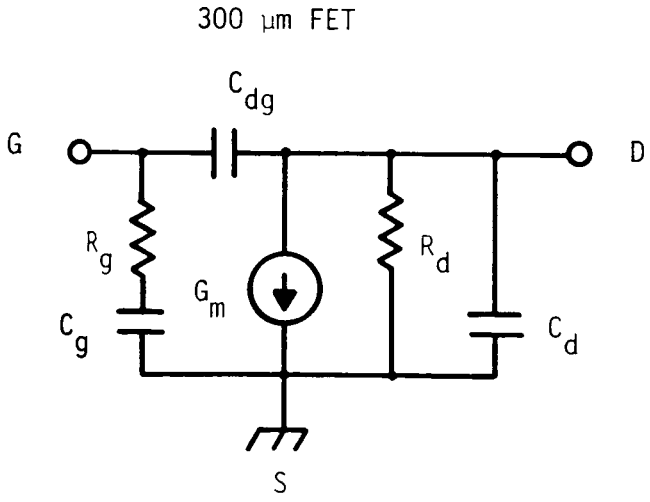


Figure 11 Equivalent Circuit of 300 μm FET Used for a Unit Cell of the Distributed Amplifier

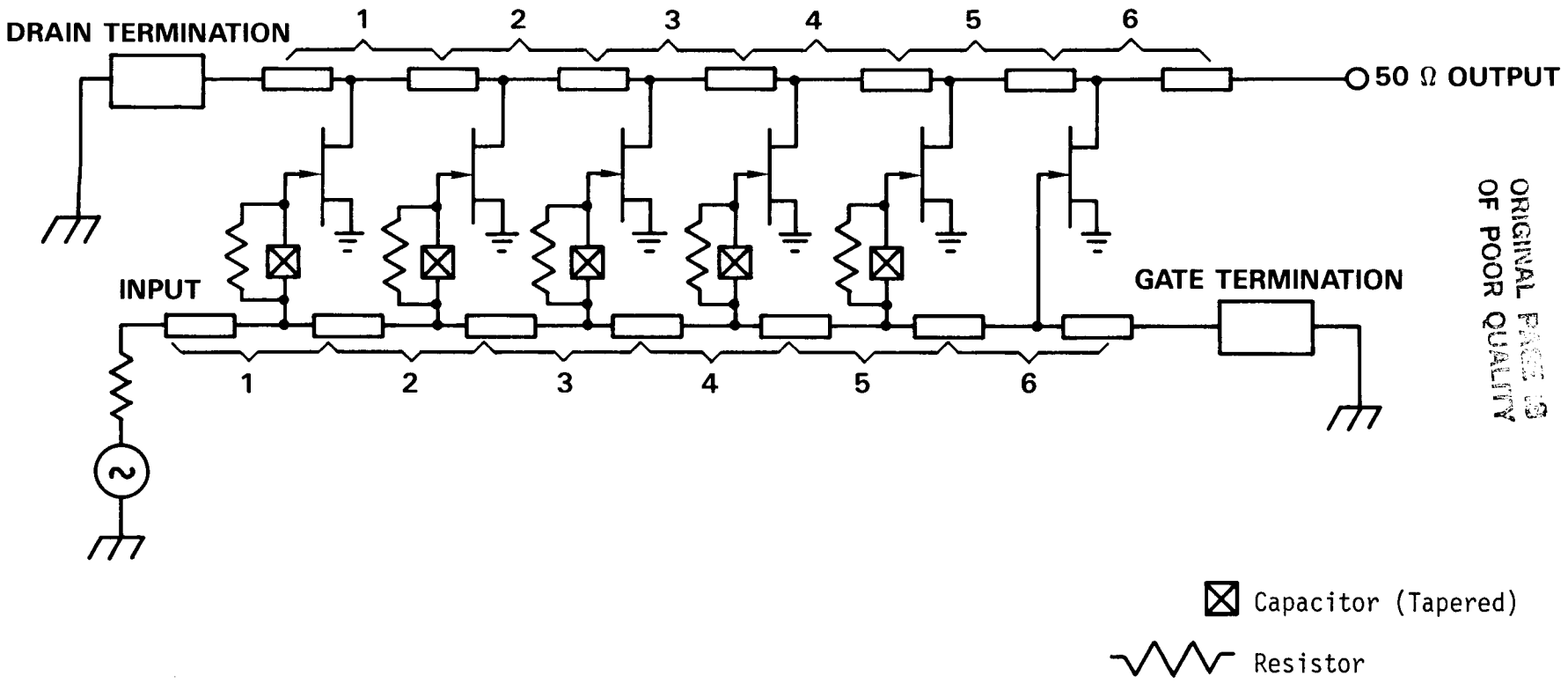


Figure 12 Circuit Diagram of a Distributed Power Amplifier with Tapered Capacitor

the overall amplifier gain does not decrease, because more devices can be connected. Moreover, this capacitor and the FET input capacitor form a voltage divider, allowing for an increased signal level along the gate line. This results in a significantly higher output power and efficiency for a distributed amplifier.

The loss reduction technique described above has been implemented in a 6 x 300 μm monolithic GaAs distributed amplifier design. To provide for a constant rf voltage across all the FET gates, the series capacitors are tapered. Figure 13 shows the voltage across the gates. It is clear that a fairly constant gate voltage can be maintained with this scheme, even though the input signal at the gate line attenuates significantly. The circuit components are optimized using CAD techniques.

Significant losses are also incurred at the drain line. For the uniform impedance line at the drain, only half the generated current flows into the load, and the other half flows into the reverse termination. To increase the current generation capability and efficiency of a distributed amplifier, the amount of current flowing in the reverse direction should be minimized. This can be achieved using the so-called tapered impedance scheme in the drain line. The tapering is done in such a way that the voltage amplitude of each section is maintained at a constant level, in spite of the fact that power is being added to the drain line continuously. Assuming an identical gate width for each section, it can be shown that the output impedance of the line will be Z_0/n, where Z_0 is the initial impedance.[4] The entire current of the output devices may thus be effectively used in the load without the necessity of half the current flowing in the load and half the current flowing in the reverse termination. Therefore, the tapered line increases the current generation capacity by a factor of two. the power generation capacity of every section is fully utilized, resulting in maximum output power and higher efficiency. The practical implementation of the precise impedance tapering requirement with $Z \sim 1/n$ is difficult to achieve because of the practical restriction of transmission line impedance levels. Instead, a linearly tapered line ranging from 75 to 50 Ω is designed.

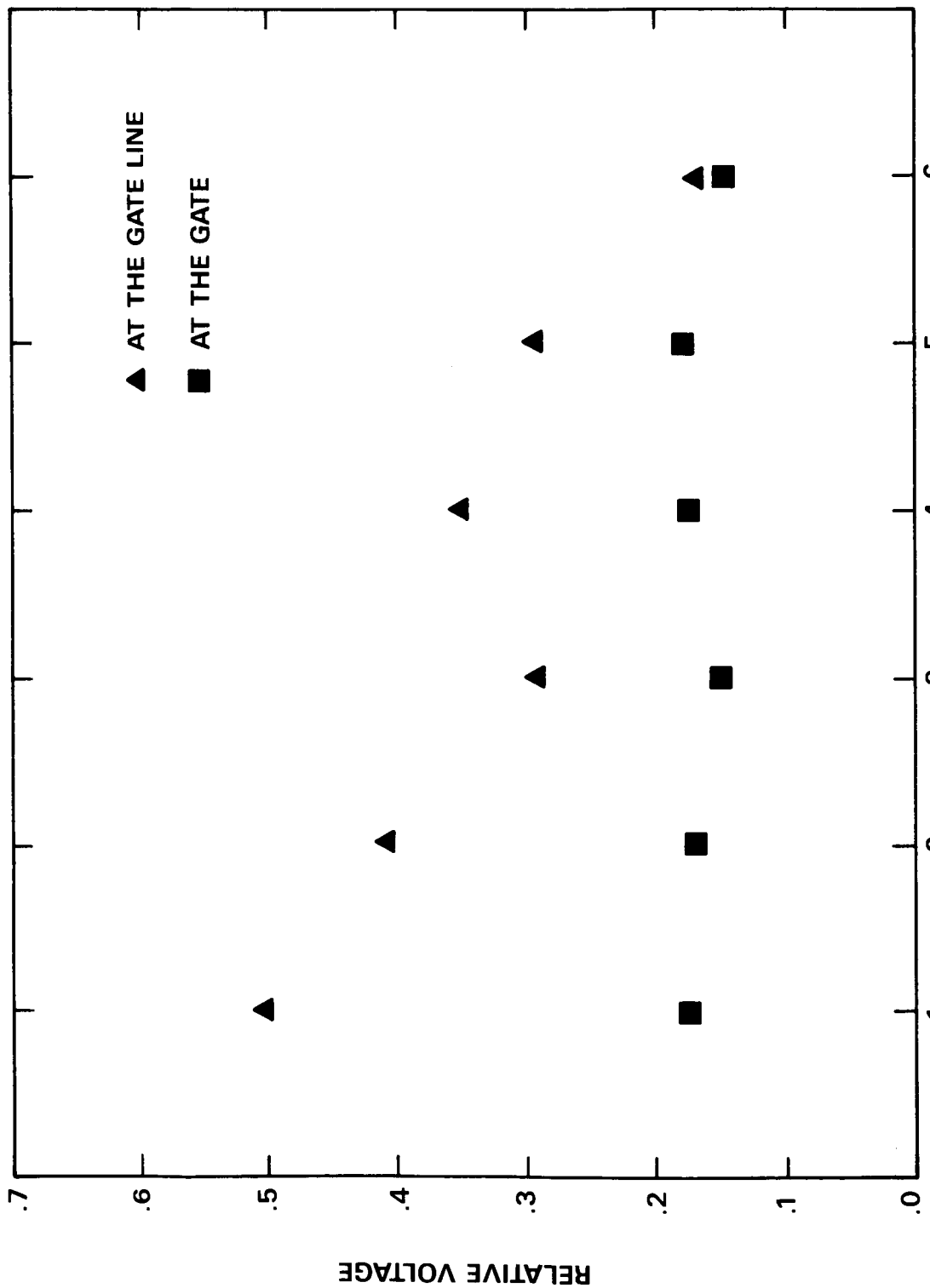


Figure 13 Voltage Distribution at the Gate and the Gate Line

At the termination ends of the drain and gate lines, reflectors are added instead of resistive absorption teminations. The terminations should be designed in such a way that they provide the proper phase to the reflected wave to have constructive interference for improving the amplifier gain and power. It was found that the reflectors must generate a phase angle to compensate the propagation phase delay of the incident wave through the amplifier.

The incident wave at the drain termination is the backward traveling-wave, which is phase mismatched to the input signal. Also, the wave reflected at the gate termination generates output that is also the backward traveling-wave. The power gain for the backward traveling-wave G_-, assuming lossless case, is given by[7]

$$G_- = \frac{(g_m n)^2 Z_{go} Z_{do}}{4} \left\{ \frac{\sin(\Delta\beta_- /2)}{\Delta\beta_- /2} \right\}^2 , \qquad (4)$$

where $\Delta\beta_-$ is the mismatching between the input and the backward waves.

To maximize the effects of the reflectors, the G_- at the operation frequency should be at or near the peak of the sine function variation. The amplifier propagation phase delay was adjusted to accomplish this. the voltage amplitude of the backward traveling-wave as a function of frequency is shown in Figure 14. It clearly shows that the backward wave is at its maximum at band center (~ 20 GHz).

The reflectors degrade the VSWR of the amplifier. Because of line attenuations, however, the VSWR degradations are minimal. With reflective terminations, the output power improves by 1.5 dB compared to the absorptive terminations.

2. Amplifier Fabrication and Microwave Performance

The starting material is grown by vapor phase epitaxy (VPE). The active layer doping is about 2.2 to 2.5 x $10^{17}/cm^3$, which is the optimum

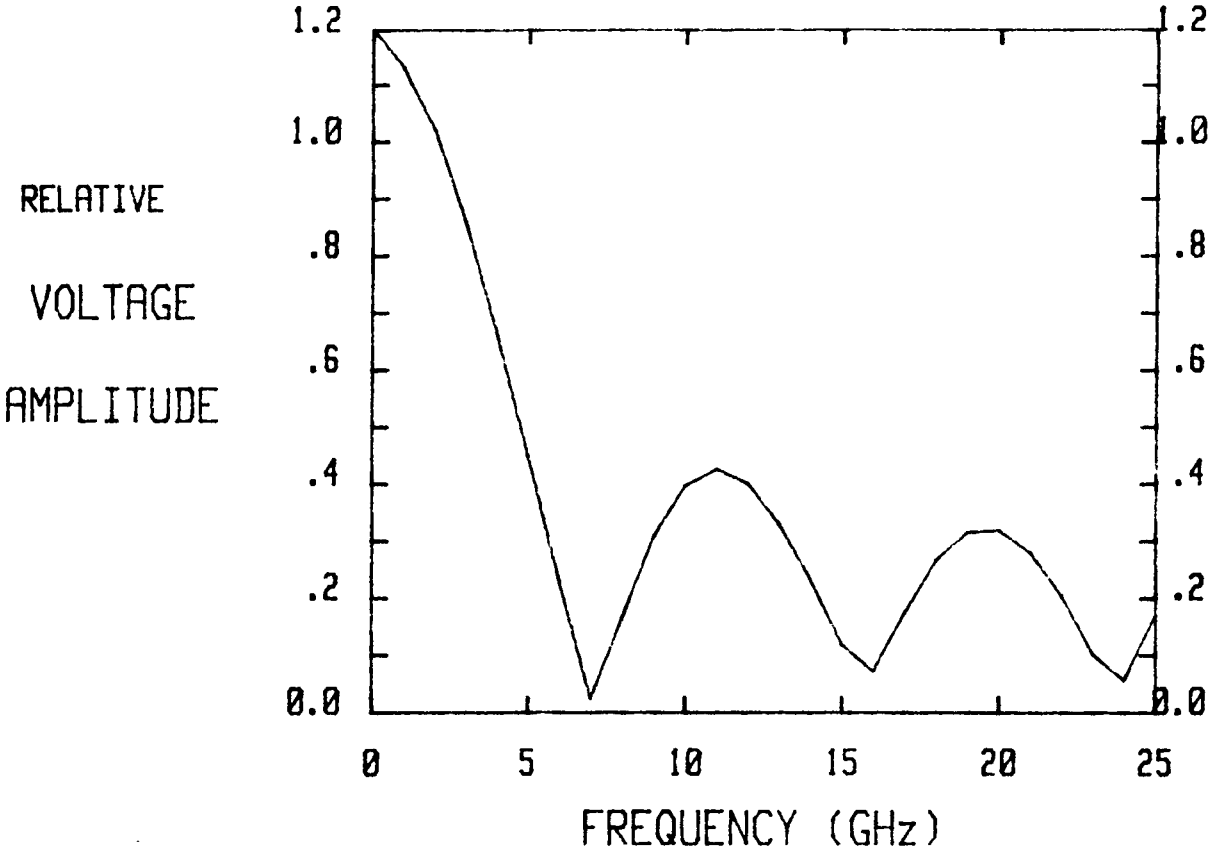


Figure 14 Voltage Amplitude of the Backward Traveling-Wave at the Drain Termination as a Function of Frequency

value for a K-band power FET. TI's standard monolithic circuit fabrication procedures are used. Following mesa isolation by wet etching, the AuGe/Ni/Au source-drain pattern is defined, then alloyed for two and a half minutes at 430°C. Next, 0.5 μm recessed gate stripes are defined in PMMA by e-beam machine. Then layers of 150 nm Ti/50 nm Pt/400 nm Au are evaporated and lifted-off.

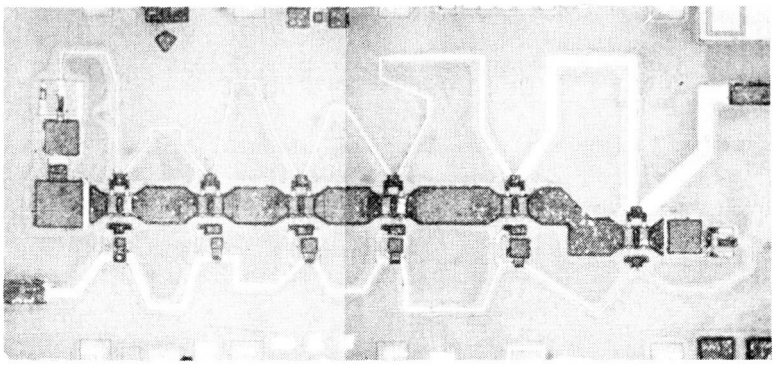
The first level of metal follows. In this level transmission lines, capacitor bottom plates, and FET electrodes are defined. Silicon nitride (400 nm) provides the dielectric for the capacitors. After evaporation of Ti/Au for the capacitor top plates, the inductors, FET electrodes, capacitor top plates, and air-bridges are plated up. The slice is then lapped down to 4 mils. Finally, vias are etched using reactive ion etching (RIE).

Figure 15 shows a photograph of the amplifier chip, which is 1.25 mm x 2.63 mm x 0.1 mm. Via holes for source groundings are provided between each of the 300 μm cells. Monolithic mesa resistors shunting the tapered MIM capacitors are used for gate bias. The reflectors are parallel combinations of resistors and capacitors, realized monolithically as shown in Figure 16. Mesa resistors and MIM capacitors are integrated.

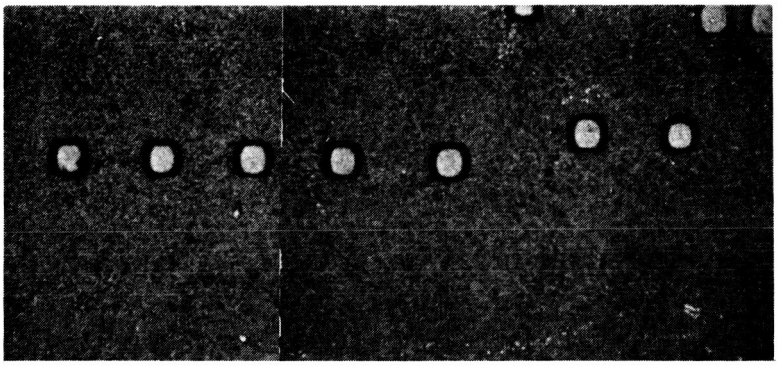
Several slices of this monolithic distributed amplifier have been processed and evaluated. A linear gain of 5 ± 1 dB has been obtained across the 2 to 22 GHz frequency range as shown in Figure 17. Under large signal operation and at a higher drain voltage (8 V), this amplifier has produced an output power of 0.5 W with at least 4 dB gain over the 2 to 21 GHz band. The power-added efficiency at 0.5 W output was 14%. We believe this is a state-of-the-art result for a GaAs distributed amplifier in terms of gain, bandwidth, output power, and efficiency.

3. Device Structure Optimization

In general, the parameters that will maximize the high-frequency gain also will make the device suitable or incorporation into the distributed amplifier designs. The most important factors for improved gain at high frequencies include minimum gate resistance, gate-source capacitance, source



(a)



(b)

Figure 15 Monolithic GaAs Traveling-Wave Amplifier.
(a) Front side, (b) back side.

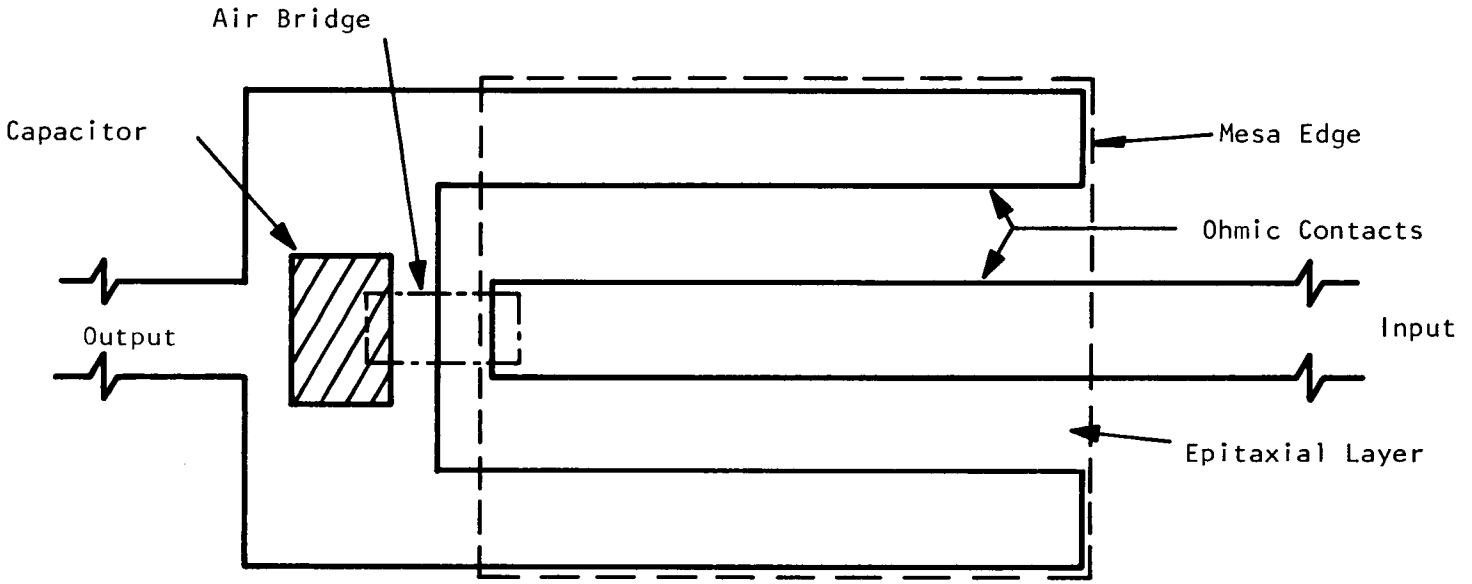


Figure 16 Monolithic Realization of Parallel Resistor and Capacitor

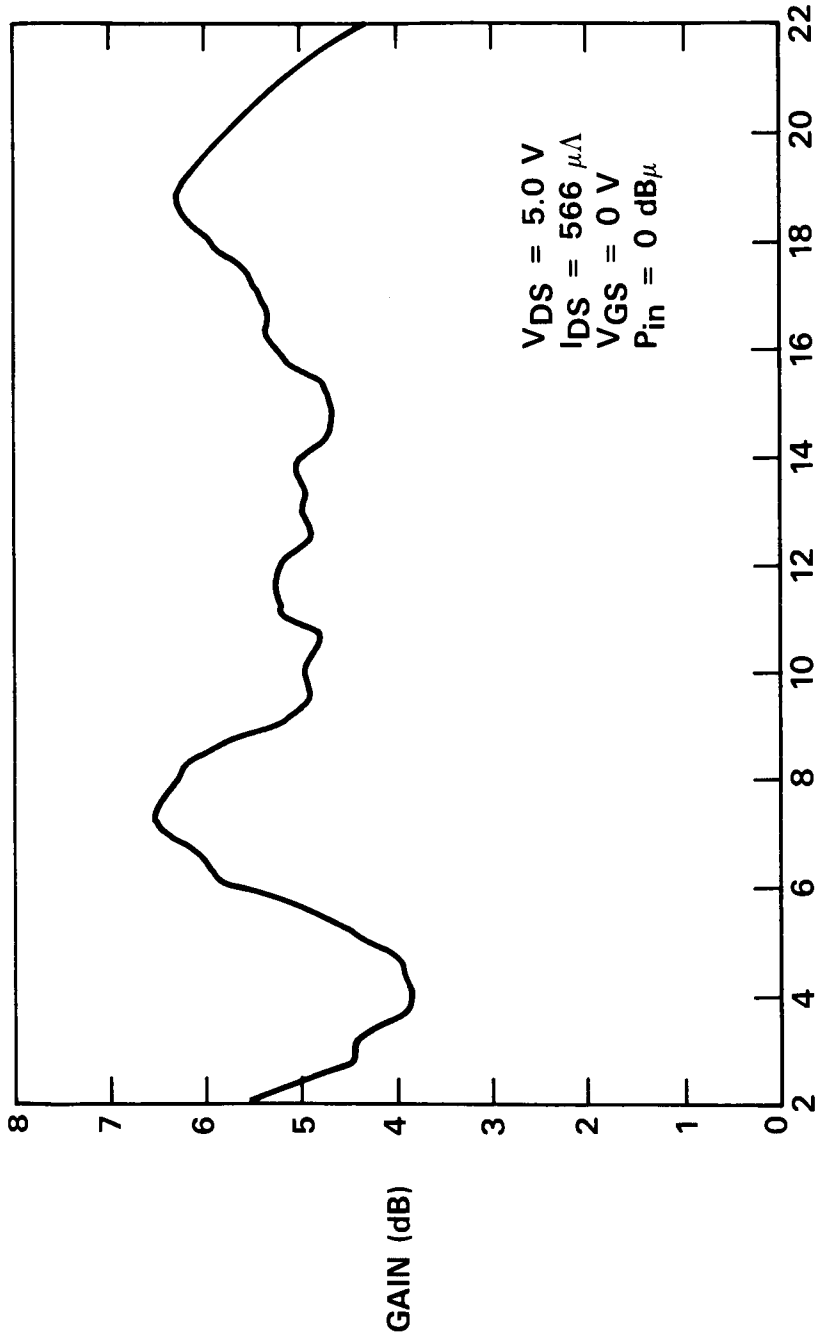


Figure 17 Performance of a Distributed Power Amplifier

resistance and inductance, and maximum device transconductance. In this subsection we show that, for the distributed amplifier design, because of losses (especially the gate transmission), the power gain will be proportional to $(g_m/C_{gs}^2)^2$ rather than $(g_m/C_{gs})^2$ as in a discrete device. Therefore, the gate-source capacitance, C_{gs}, is even more detrimental in the distributed amplifier than in a discrete device.

For a FET device, Mason's unilateral gain, G_u, is given by[8]

$$G_u \approx \frac{1}{2} \frac{g_m^2}{\omega^2 C_{gs}^2} \cdot \frac{R_{ds}}{R_{in}} \propto \left(\frac{g_m}{C_{gs}}\right)^2 , \tag{5}$$

where R_{in} is the input resistance and R_{ds} the output resistance. For high gain, g_m/C_{gs} should be maximized. The carrier profile dependent g_m/C_{gs} has been studied by several authors.[9-11] In a simple depletion layer approximation, g_m/C_{gs} is unaffected by the carrier profile, but is inversely proportional to the gate length.[9] The effects of doping profiles on g_m/C_{gs} have been reported in the literature.[10,11] It has been shown that with a special graded-channel profile, the quantity g_m/C_{gs} can be improved.

The dependence of gain G on g_m and C_{gs} for a distributed amplifier can be derived using Equation (2) in Section III.B.1. Neglecting the drain loss, the equation becomes

$$\begin{aligned} G &\approx \left[\sum_{q=1}^{N} \frac{g_m \sqrt{|Z_d Z_g|}}{2} e^{-\alpha_g q} \right]^2 \\ &= \left[\frac{g_m}{2} \sqrt{|Z_d Z_g|}\; e^{-\alpha_g} \frac{1 - e^{-\alpha_g N}}{1 - e^{-\alpha_g}} \right]^2 \\ &= \left[\frac{g_m}{2} \sqrt{|Z_d Z_g|}\; \frac{1 - e^{-\alpha_g N}}{\alpha_g} \right]^2 . \end{aligned} \tag{6}$$

The gain given in Equation (6) decreases as frequency increases. The gain at a low frequency is given by

$$G_q = \frac{|g_m \sqrt{|Z_d Z_g|}\, N|^2}{2} \tag{7}$$

The number of sections N is determined by the desired bandwidth for a given gain variation, say 3 dB;

$$\frac{1 - e^{-\alpha_g N}}{\alpha_g} = N/2 \ . \tag{8}$$

From Equation (8)

$$\alpha_g N = \text{Constant} = K \tag{9}$$

or

$$N = K/\alpha_g = K/\omega^2 C_{gs}{}^2 Z_g \ . \tag{10}$$

Combining Equations (6) and (10), the gain G_q is given by

$$G_q \approx \left| \frac{g_m}{2} \sqrt{|Z_d Z_g|} \cdot \frac{K}{\omega^2 C_{gs}{}^2 Z_g} \right|^2$$

$$= \left[\frac{g_m K}{8\pi^2 f^2 C_{gs}{}^2} \cdot \left| \frac{Z_d}{Z_g} \right| \right]^2 \tag{11}$$

$$\propto (g_m/C_{gs}{}^2)^2 \ .$$

Here, f is the cut-off frequency. Thus, the gain of a distributed amplifier is proportional to $(g_m/C_{gs}{}^2)^2$.

The gain of a conventional FET is proportional to $(g_m/C_{gs})^2$, while for a distributed amplifier structure the gain is proportional to $(g_m/C_{gs}{}^2)^2$. Due to the squared C_{gs} term for the distributed amplifier, it is

even more important to reduce the gate-to-source capacitance (C_{gs}) for an improved gain. The ultimate output power is limited by the breakdown voltage. An attempt was made to reduce the C_{gs} and improve the breakdown voltage by using an active layer with a lower doping ($1.7 \times 10^{17}/cm^3$, instead of the usual doping of $2.3 \times 10^{17}/cm^3$). The lower doping will reduce the gate-to-source capacitance while increasing the breakdown voltage. A slice with this doping has been processed and evaluated, and an output power of up to 0.5 W with 4 dB gain was obtained at 20 GHz. This is as good as the result for the best slice processed so far.

Another approach aimed at reducing the gate-to-source capacitance is to use an n^- gate buffer layer ($1 \times 10^{17}/cm^3$), followed by an n active layer ($5 \times 10^{17}/cm^3$), and the usual buffer layer (see Figure 18). To reduce the parasitic source and drain contact resistances, an n^+ contact layer was grown on top of the n^- gate buffer. The n^- gate buffer should reduce C_{gs} and also should increase the breakdown voltage significantly. A slice with this material structure was grown by MBE and has been successfully processed. Microwave measurement results showed that a significantly higher output power can be obtained. An output power as high as 700 mW was obtained with 2.5 dB gain at 19 GHz. This is the highest output power ever achieved for the distributed amplifier. This improvement in output power was attributed to the higher breakdown voltage and the lower gate-to-source capacitance of this structure. Due to the change of the device parameters, the impedance levels for the amplifier circuit might not be optimal. Further improvement in gain is expected with a slight modification of the circuit. For this purpose, a discrete device having this special doping profile will be characterized in terms of S-parameters and equivalent circuit model. This will determine the minor redesign of the distributed amplifier for increased gain.

C. Three-Stage, 2.5 W Amplifier

At the time of the original proposal it was not certain that the simple monolithic three-stage cascaded common-source amplifier approach would be successful at the high frequency and high power level necessary to meet the program goals. Consequently, this approach was just one of several investigated. Recent results have been very promising, however, and it appears that this approach is most likely to meet the program goals. In

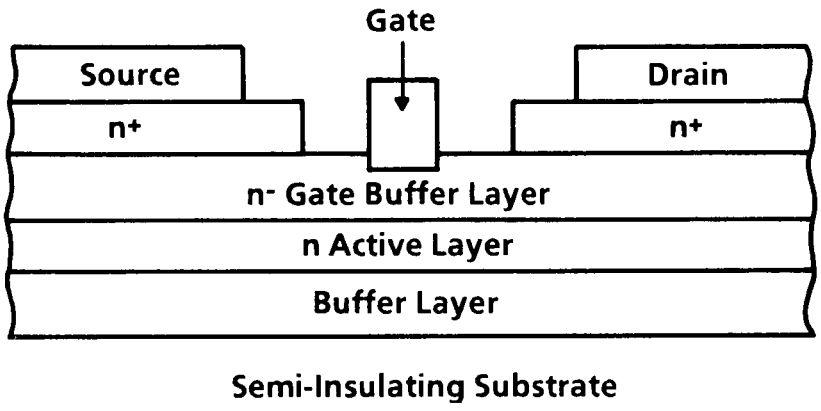


Figure 18 n^+ Ledge, Two Active Layer Channel Structure

addition, the cascaded common-source design is much simpler in concept and more compact in realization than the other approaches.

The circuit topology and predicted gain-frequency response of the three-stage amplifier are shown in Figure 19. This is the same topology given in the original proposal. The lumped inductors shown in the figure have been replaced by high-impedance transmission lines using the Super-Compact circuit design routine. The FET gate widths of the three stages are 1.2 mm, 2.4 mm, and 6.0 mm. Recent experimental data continue to support the proposal assumption that output powers of ~ 0.5 W/mm gate width are reasonable at the power level and frequency of interest. The chip layout is considerably different from that shown in Figure 29 of TI's proposal, however. Figure 20 shows the digitized photomask design data obtained from a plotter for all the mask levels. The chip size is a very compact 3.3 mm x 2.0 mm x 0.1 mm, less than half the area of the proposal design.

Figure 21 is a photograph of a slice after completion of front-side processing, showing the actual implementation of the plot in Figure 20. The dark areas are plated gold. All the inductors are formed from 25 μm wide transmission lines. The small input and output capacitances are realized by the capacitance to the bottom of the chip of the large pads on the input and output (1.1 pF/mm^2). The larger interstage capacitances are realized by MIM capacitors. Figure 19 does not show the two interstage blocking capacitors, which are 5 pF MIM capacitors (140 pF/mm^2 for 4000 Å silicon nitride dielectric). Therefore, between the FETs of stages 1 and 2 and stages 2 and 3 are a shunt capacitor (2.3 pF or 5.0 pF) and a series capacitor (5.0 pF). Figure 22 is an SEM photograph illustrating the connection of such a series/shunt capacitor pair to the rest of the circuit. The input transmission line enters from the left and is connected to the shunt capacitor top plate by an air bridge. The bottom plate is grounded by a via (not shown) to the large pad at the bottom of the photograph. The shunt capacitor is connected by another air bridge to the top plate of the series capacitor. The bottom plate of the series capacitor is contacted by a transmission line which exits on the right side of the photograph.

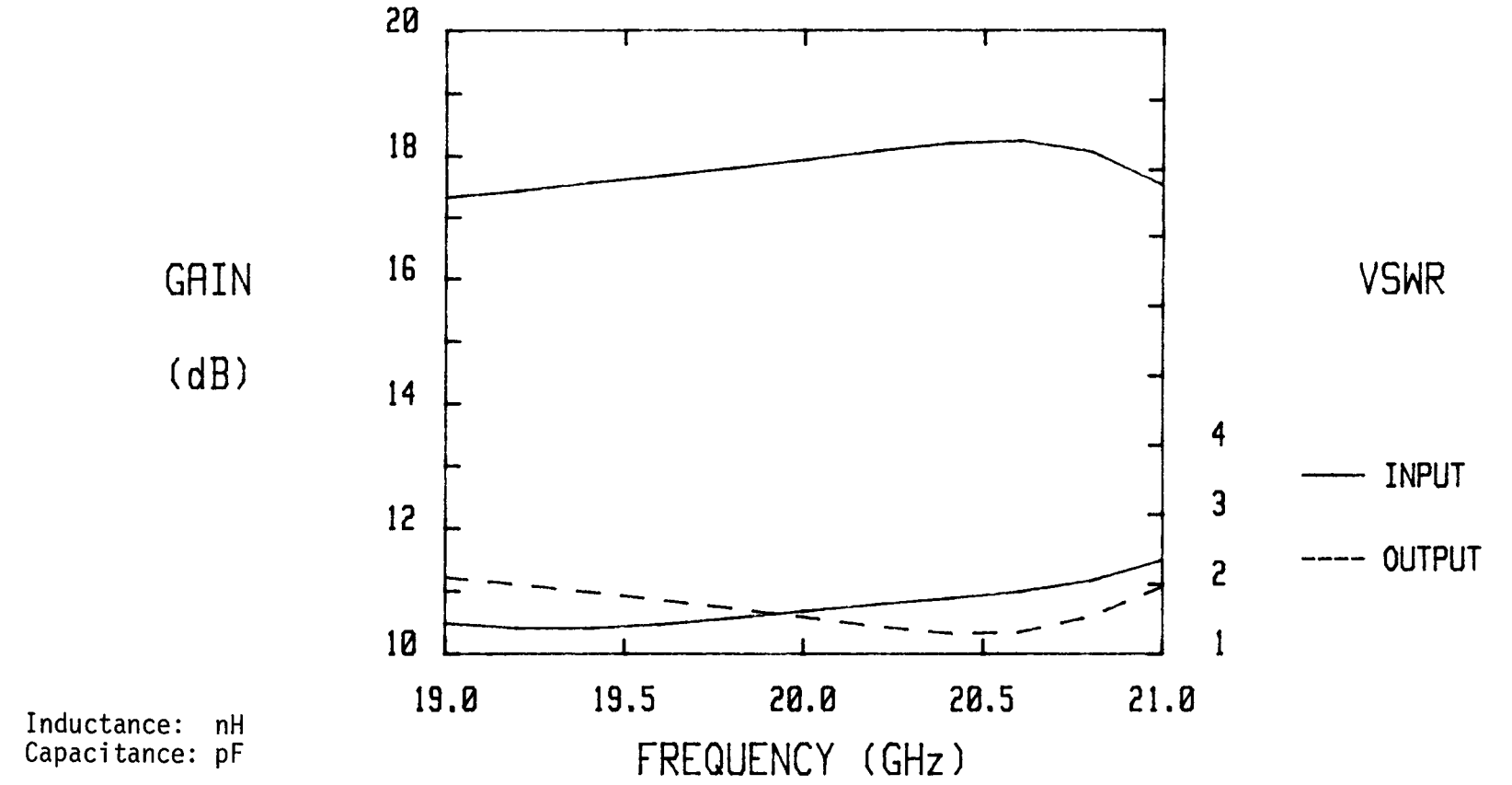


Figure 19 Circuit Topology and Gain-Frequency Response of a Three-Stage (1.2 mm - 2.4 mm - 6.0 mm), 2.5 W Monolithic Amplifier Module

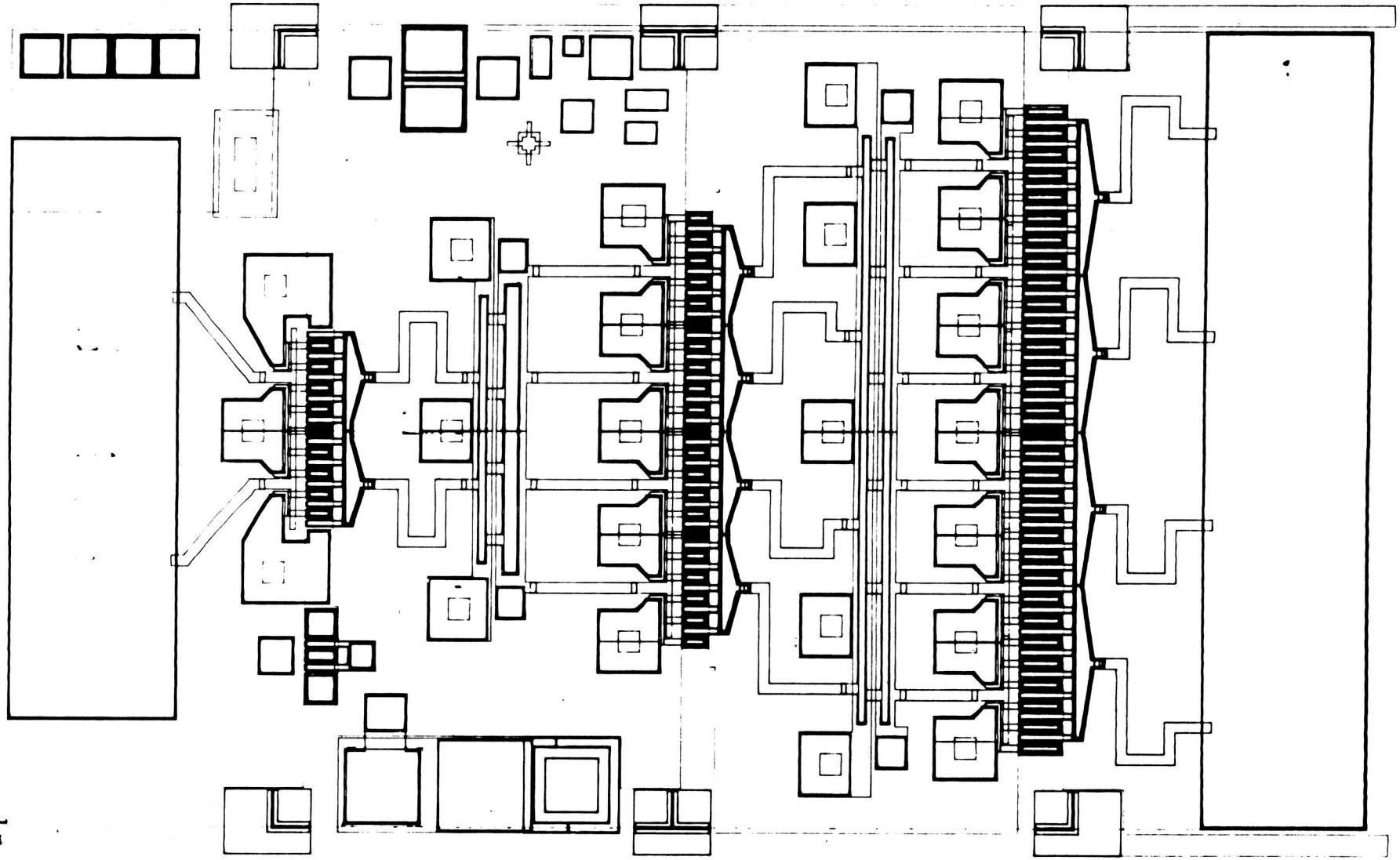


Figure 20 Digitized Photomask Design for 2.5 W, 20 GHz, Three-Stage Monolithic Amplifier Module

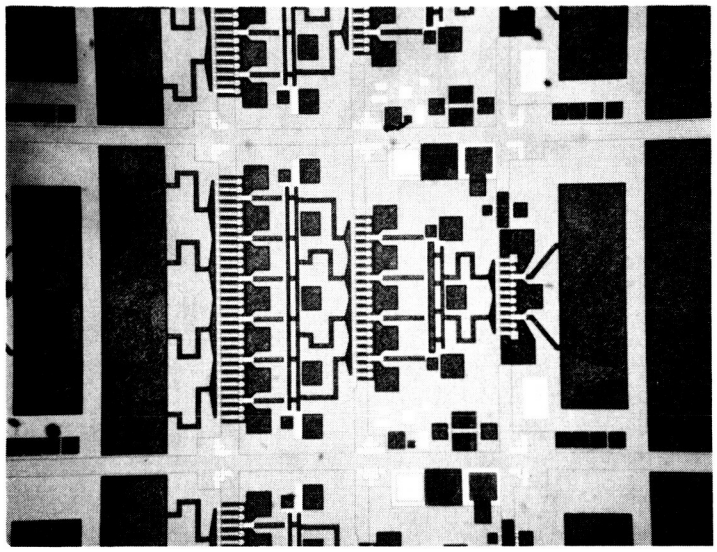


Figure 21 A Portion of a Three-Stage 2.5 W Amplifier Slice Following Completion of Front Side Processing

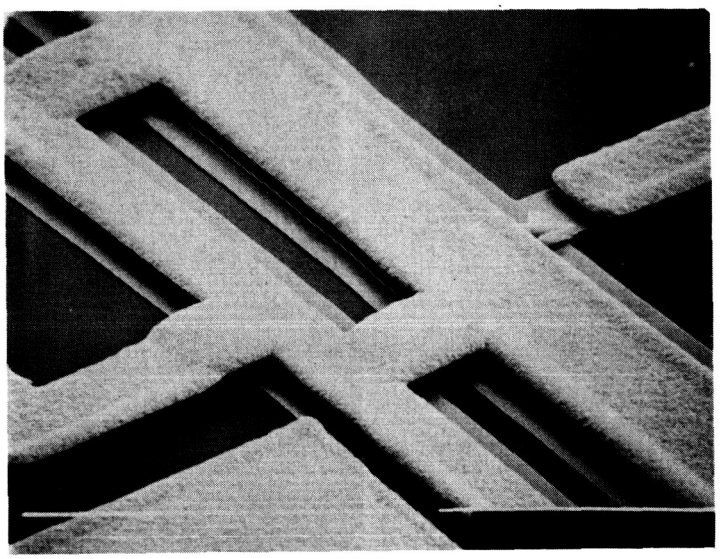


Figure 22 SEM Photograph of a Series/Shunt Capacitor Pair Connected to Input and Output Transmission Lines

The FETs must be designed for the highest possible gain for successful operation at 20 GHz. The FET geometry must be compact to minimize phase shift across the device. It must also have low source lead inductance to minimize gain degradation. For this reason the source overlay structure sketched in Figure 23 was chosen. The sources are connected by air bridges over the gate bus bars to the large pads, which are grounded by vias to the back of the chip. There are three such vias to the 1.2 mm device, five for the 2.4 mm device, and seven for the 6 mm device. The sketch in Figure 23 is of the 1.2 mm device. Figure 24(a) is an SEM photograph of one of the 1.2 mm devices on a completed amplifier showing the realization of the overlay geometry. The signal enters from the left and exits to the right. Figure 24(b) shows the details of the air bridge connection. The use of reactive ion etching (RIE) for vias is critical for this application because the via should be as close as possible to the active area, and contact must be made to a 150 μm wide pad through 100 μm GaAs. Recently, it has been shown that a 1.2 mm gate width GaAs FET with overlay geometry can have up to 0.5 W output power at 30 GHz.[12] This verifies the usefulness of the geometry at high frequencies.

Other FET design parameters used are a gate length of 0.5 μm and an active layer doping level of ~ 2.5×10^{17} cm^{-3}. With 0.5 μm gates it is desirable to keep the gate finger width less than ~ 75 μm to reduce gain degradation due to signal attenuation and phase shift along the gate fingers.[13] The FETs in the first two stages therefore used a 60 μm finger width, but that was not possible for the last stage FET. A 60 μm gate finger width would have resulted in a FET that was too large from end to end when enough fingers were included for 6 mm total gate width. The gate-gate spacing cannot be reduced much without excessive drain resistance and temperature rise during operation. The compromise values chosen for the 6 mm FET are 100 μm finger width, 20 μm gate-gate spacing across the drain, and an FET physical length of ~ 2 mm.

Reducing the gate-gate spacing across the drain has the favorable result of reducing the gate-drain feedback capacitance (C_{dg}), which increases gain. The gate bus bar was placed 25 μm away from the active area, instead of the 13 μm mentioned in the proposal, to further reduce C_{dg}.

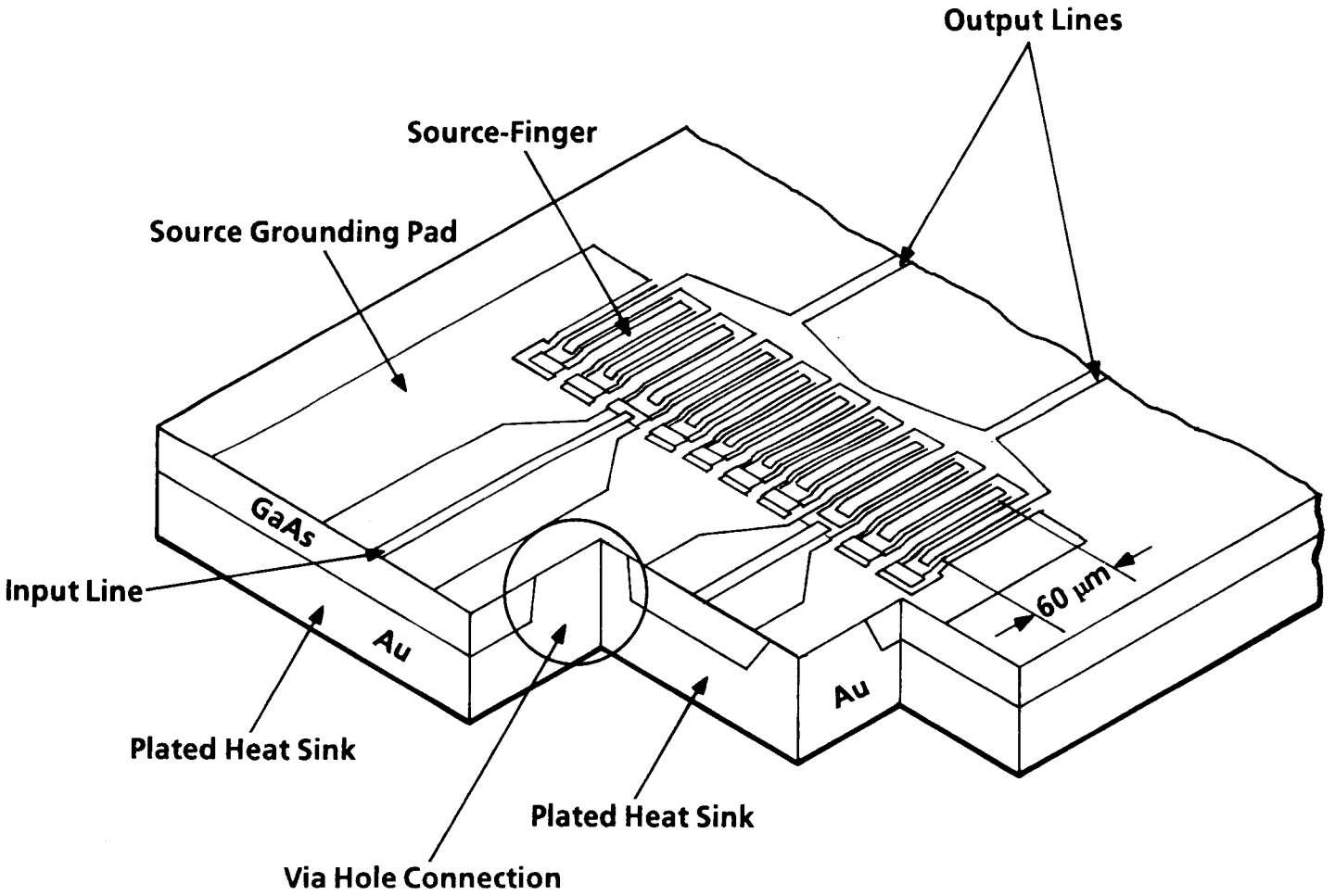
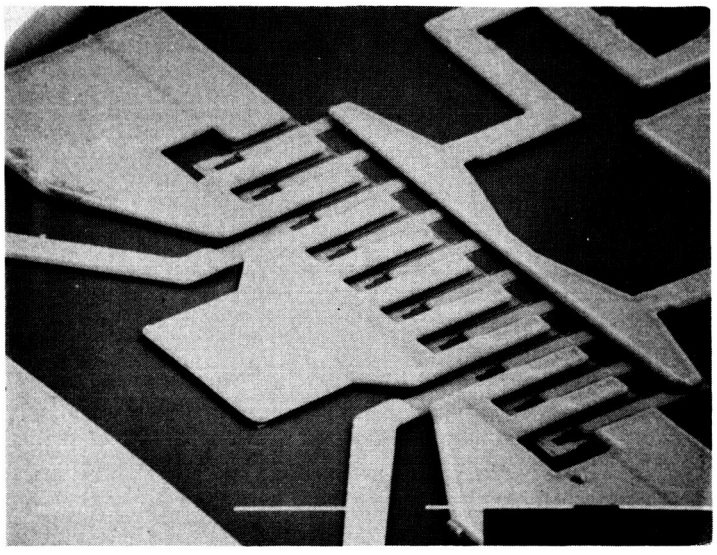
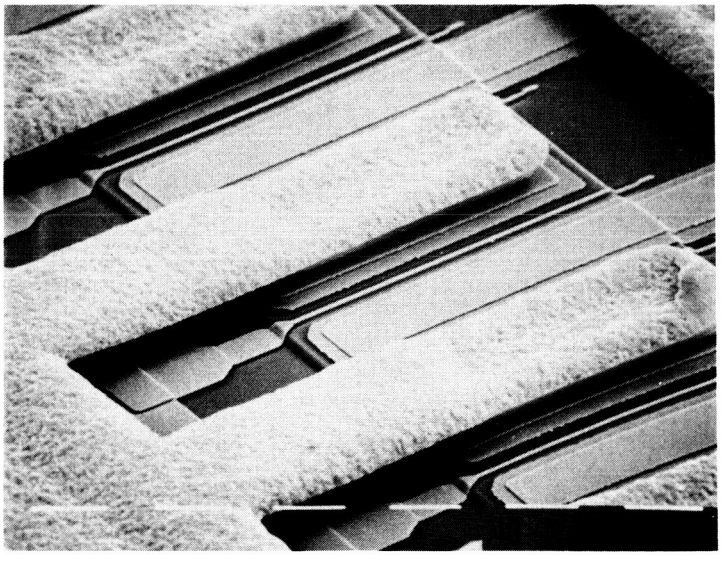


Figure 23 Sketch of Source Overlay Structure with Via Grounding



(a)



(b)

Figure 24 SEM Photographs of 1200 μm Gate Width FET on Monolithic 20 GHz Amplifier

Except for a few minor improvements, the device fabrication process is the same as described in the original proposal. The AuGe/Ni ohmic contact metal has been replaced by AuGe/Ni/Au. The resulting contacts are smoother with sharper edges, which increases yield and reliability. The alignment marks are also more visible to the e-beam machine. All gates are defined by e-beam lithography and are 0.15 μm Ti/0.05 μm Pt/0.4 μm Au with an intended gate length of 0.5 μm. In the proposal it was stated that careful monitoring of yield due to shorted capacitors would be necessary if large MIM capacitors were employed on the circuit. Although there are none in the present design, we are considering the addition of on-chip bias circuitry, which would include several large (10 to 20 pF) bypass capacitors, for future design iterations. Since the proposal was written, the shorted capacitor problem has been eliminated by adding a mask step to the capacitor fabrication process. The yield of 30 pF MIM capacitors has risen from 90-95% to ~ 99% and is no longer a potential problem. The new process is already incorporated into the 2.5 W amplifier mask set. None of the other fabrication processes has been changed since the beginning of the program.

Amplifiers have been fabricated on active layers produced by several different techniques. The first lot completed had two slices with VPE active layers and one with the active layer produced by ion implantation directly into the substrate. The performance of devices from these three slices was similar; amplifiers produced 1.1 to 1.3 W output power with 7.5 to 8 dB gain at 17 GHz. The 1200 μm (first stage) and 300 μm (test) FETs were sawed from several amplifiers and tested at 15 GHz, where we have a large data base. Gain was 1 to 2 dB lower than expected. Yield of good three-stage amplifiers was 3.6% to 13%, which results in ~ 20 good chips from a 2 inch slice. This is a good yield for such a large total gate width at the beginning of a program. Most of the bad chips had FETs that would not pinch off due to broken gates.

Following completion of this first lot, two lots containing five slices were stopped in process when the overlay metal would not lift off completely. It was concluded that the lift-off was made more difficult by the inclusion of a Cr layer as an RIE via etch stop. The metal could be lifted off the FETs, but could not be lifted off between some of the transmission lines. The problem was alleviated by depositing the transmission lines separately

from the pads and not using Cr. This was possible because the transmission lines are defined by a separate photomask, and only the pads that are contacted by vias require the Cr layer.

Following completion of the first three slices described above, an n^+ contact layer was added to improve FET performance (as first suggested in the proposal). The devices were fabricated with the n^+ ledge channel structure (or "double recess channel structure") shown in Figure 25. It has been shown[14] that devices with this structure have the highest resistance to instantaneous burnout and the highest long-term reliability. In our laboratory we have found that the n^+ ledge structure also significantly improves discrete device microwave performance over that of conventional recessed gate devices.[15]

The n^+ ledge fabrication process involves one more step than the conventional process. Following ohmic contact fabrication, the first (or wide) recess pattern is defined by electron beam lithography. The slice is then etched through the n^+ layer and down into the active layer until the correct current is reached. The resist is then removed, and the standard gate pattern is defined in a new resist layer. The second (or gate) recess is then etched until the final current is reached and the gate metal is evaporated and lifted off as with conventional devices.

The performance improvement is much better understood now than at the time of the proposal; it is attributed to two factors:

(1) The reduced parasitic resistance of the source-gate and drain-gate regions permits a shallower gate recess and lower active layer doping level than is optimum for a deivce without the n^+ layer. Measurements at S- and X-bands have shown that the optimum current before gate recess is 700 mA/mm gate width for conventional channel structures and ~ 600 mA/mm gate width after the first (wide) recess for n^+ ledge channel structures. This reduction, along with the lower doping level, reduces the gate-to-drain feedback capacitance (C_{dg}), which is one of the most important factors in determining gain.

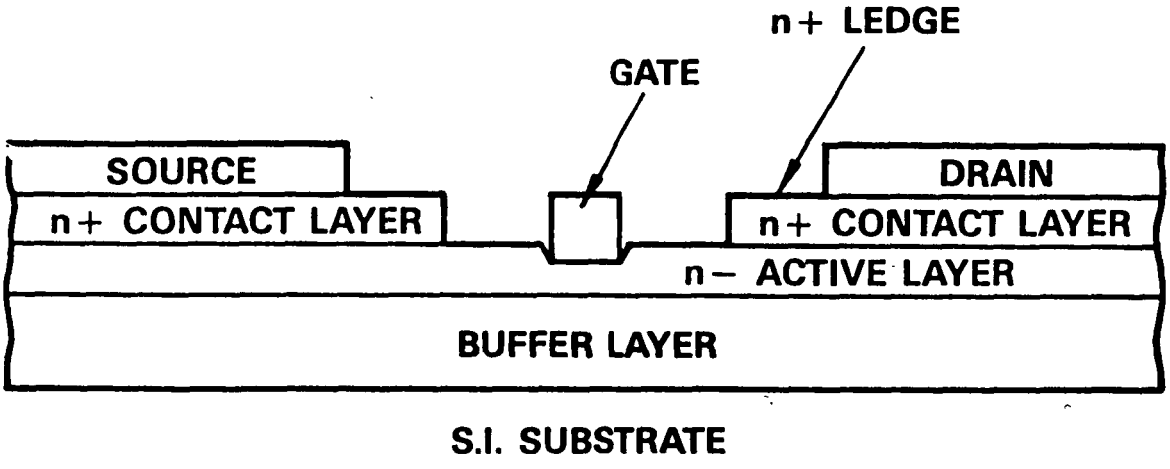


Figure 25 n^+ Ledge Channel Structure

(2) The shallower gate recess and lower active layer doping level increase the gate breakdown voltage, which increases the drain voltage at which output power saturates. Higher maximum output power and higher efficiency at a given drain voltage result. It is breakdown of the gate Schottky barrier that limits device efficiency.[16] This is especially important on the present program because the very small gate length and accompanying higher active layer doping level both tend to reduce gate breakdown voltage.

Three slices have now been completed with the n^+ ledge channel structure. The epitaxial layers of two were grown by vapor phase epitaxy (VPE) and the other by molecular beam epitaxy (MBE).

An amplifier from the first VPE slice had 1.6 W output power with 9 dB gain at 17 GHz, a significant improvement over the previous high of 1.25 W from a conventional slice. There was considerable variation in performance, which is thought to be the result of variations across the slice in the alignment of the gate to the wide recess. This has been solved by shifting gate definition from E-Beam 1 in the Central Research Laboratories to the newer and more accurate E-Beam 14 in the Equipment Group GaAs Pilot Line. The first few slices have completed gate definition on E-Beam 14, and both alignment accuracy and gate length uniformity are much better. These slices will be completed in the near future. Some slices from E-Beam 1 have had gates as large as 0.7 μm, but 0.5 μm is routinely achieved with E-beam 14.

An amplifier from the MBE slice was even better: 2 W was measured at 17 GHz with 12 dB gain and 20% efficiency. This is in spite of a 0.7 μm gate length and a poor match between the second and third stages, as evidenced by the fact that the first two stages alone produced 1.6 W with 9 dB gain at 17 GHz with 26% power-added efficiency (last stage sawed off). This latter result is extremely good for a 2.4 mm gate width output FET--as good as the best discrete devices we have measured in our laboratory. It is not yet known if the MBE slices are intrinsically better than the VPE slices, since n^+ ledge VPE discrete devices have had very good microwave performance on

other programs. Results from all the completed slices are summarized in Table 2.

One problem that was encountered with the three most recent slices is low amplifier yield (only ~ 0 to 3 chips per wafer). This same problem was also encountered on other monolithic amplifier programs in our laboratory and was traced back to a change in e-beam resist several months ago. The new resist is attacked slightly during gate recess etch, leaving small particles in the channels (averages ~ 1 to 5 per 6 mm gate width device). This causes a broken gate following metal evaporation and an FET that will not pinch off. Changing to another e-beam resist seems to have solved the problem.

All the three-stage amplifiers tested to date have operated below the design band. It is thought that this results partially because the effective transmission line length is longer than expected, especially between the second and third stages, due to the distributed nature of the long, narrow capacitors. The use of 0.5 μm gates as in the original design will also improve the impedance match. We are currently measuring individual stages and pairs of stages to obtain the data necessary to redesign the matching components to maximize performance in the 19 to 21 GHz band.

The basic design and the fabrication process have been demonstrated, and good amplifiers have been produced from slices having several different types of active layers. Yields have ranged up to 13%, which is good for the present stage of development. Several small processing changes have been made to improve yield. The best devices have had the n^+ ledge FET channel structure, and the results have been very impressive. It is thought that with some modification of the matching circuits and reduction of the gate length to 0.5 μm, all the program goals will be met or exceeded.

D. Four-Stage, 0.6 W Amplifier Module

Figure 26 shows the circuit topology for the four-stage cascaded amplifier design of Figure 1. The calculated gain-frequency response is also shown in this figure. A gain in excess of 20 dB can be obtained across the design bandwidth with good input/output VSWRs. The circuit layout is similar to that of the four-stage module of NASA Contract No. NAS3-22886 (Figure 27).

Table 2
2.5 W, Three-Stage Amplifier Slices Completed During the First Year of Contract No. NAS3-23781

Slice Number	n ($\times 10^{17}$ cm^{-3})	Gate Length (μm)	300 μm FET	1200 μm FET	Amplifier Performance			Active Layer
			Gain at 15 GHz (dB)	Power at 15 GHz (dB)	Gain (dB)	Power (W)	Frequency (GHz)	
83E1-68	2.6	0.51	8.3	0.72	8.0	1.26	17	VPE
82H1-136(63)	2.3	0.55	8.5	0.71	7.7	1.17	17	Ion Implant
82G2-98-4	3.1	0.69	9.0	0.69	7.5	1.12	17	VPE
83E1-114	2.5	0.70	7.9-10	0.74	9.0	1.58	17	VPE
	(n^+/n)							
MBE-500	2.8	0.70	10.6	0.95	12.0	2.0	17	MBE
	(n^+/n)							
84E1-3	2.6	0.68	11.4	0.71	-	-	-	VPE
	(n^+/n)							

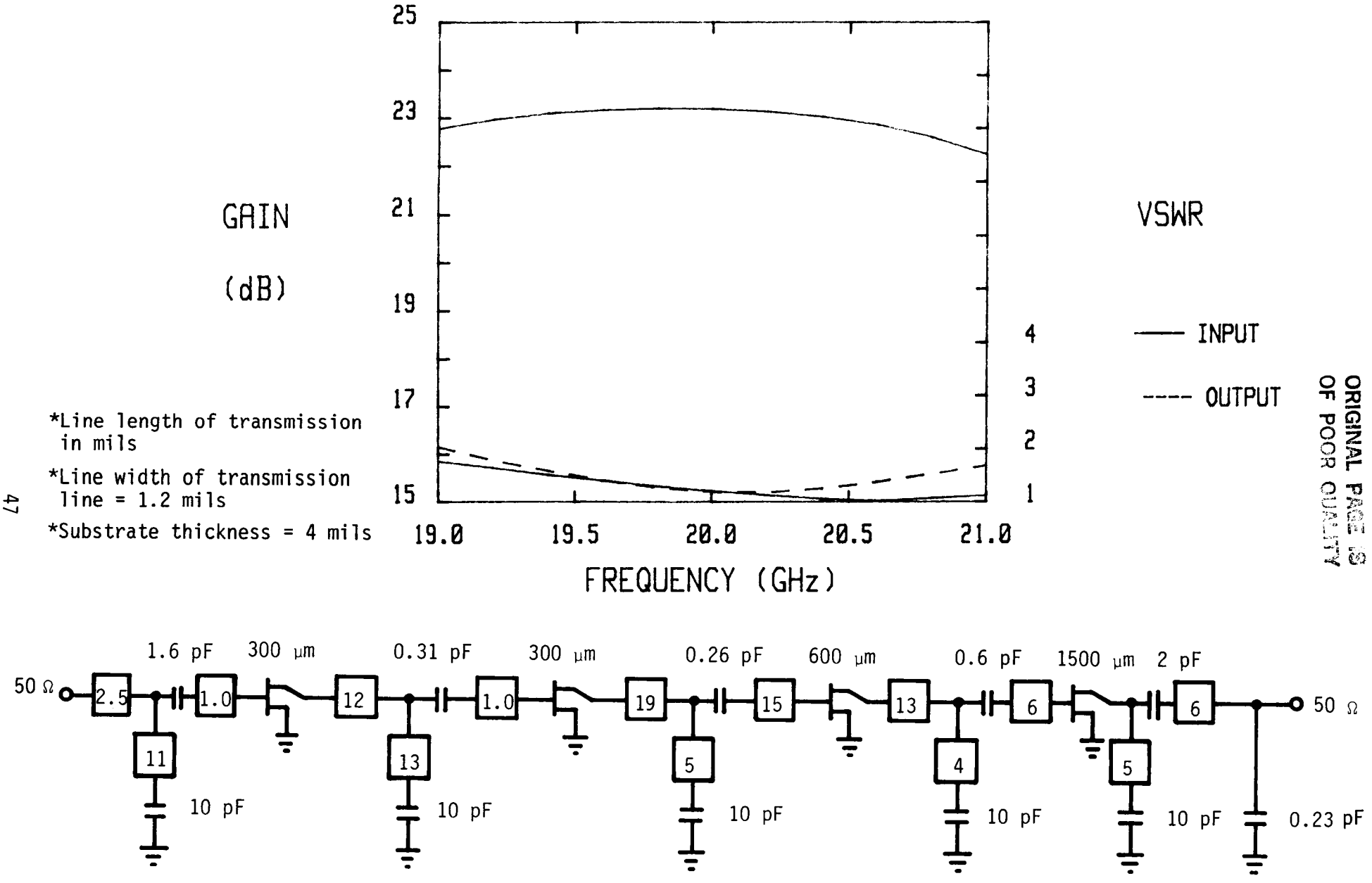


Figure 26 Circuit Topology and Gain-Frequency Response of a Four-Stage (0.3 mm - 0.3 mm - 0.6 mm - 1.5 mm) Monolithic Amplifier Module

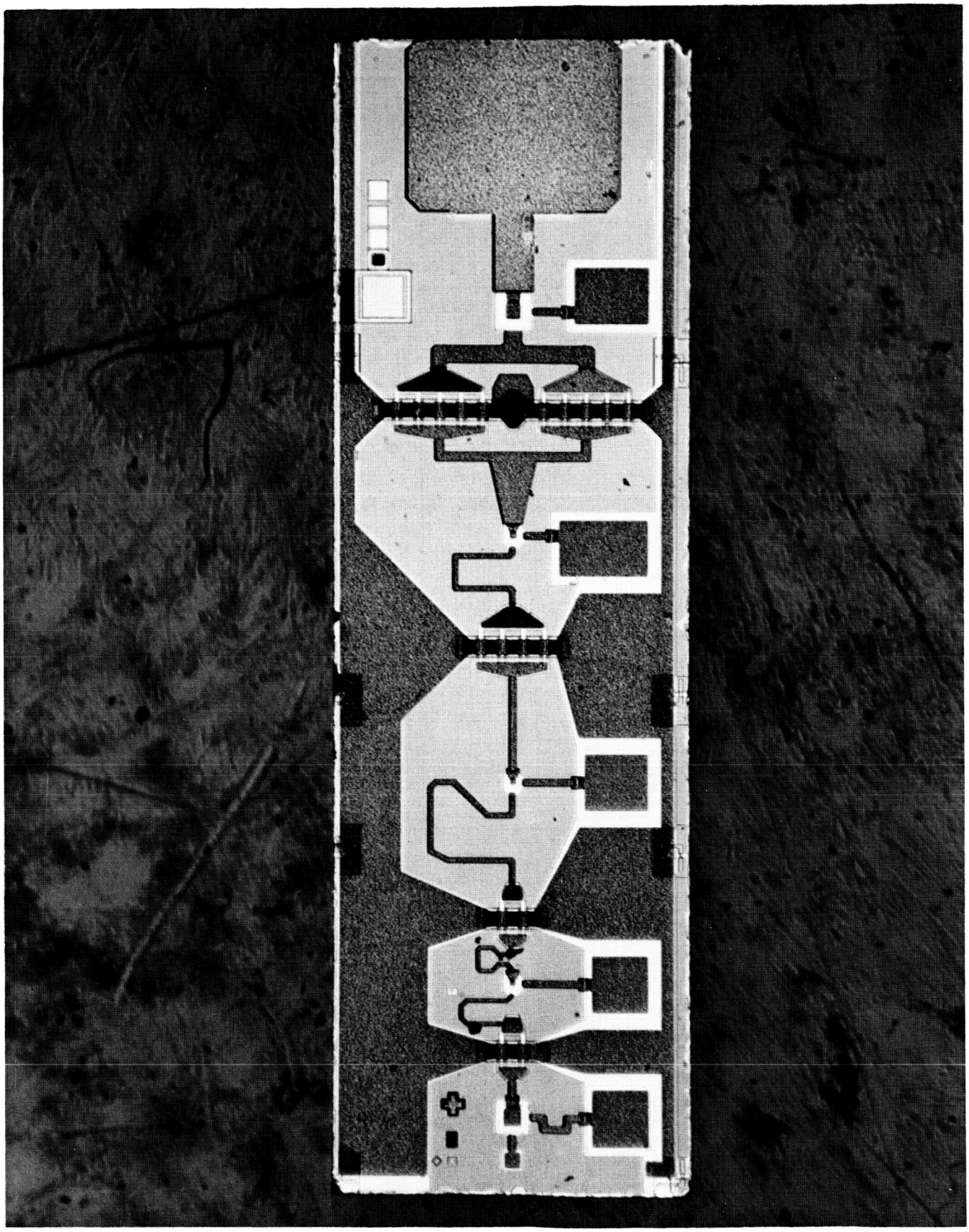


Figure 27 K-Band Monolithic Power Amplifier

Figure 28 shows the gain-frequency response of the first three stages (with the fourth stage scribed off) of the module shown in Figure 27 with some of the series high-impedance transmission lines shortened for higher frequency operation. THe line lengths of the amplifier of Figure 27 will be modified so that the center frequency of operation can be moved to the 19 to 21 GHz range. This task will be carried out during the second year of this program. In addition, a new design with a totally integrated bias network will be initiated so that four amplifiers on a single chip can readily be power combined using the combiners described in Section III.A.

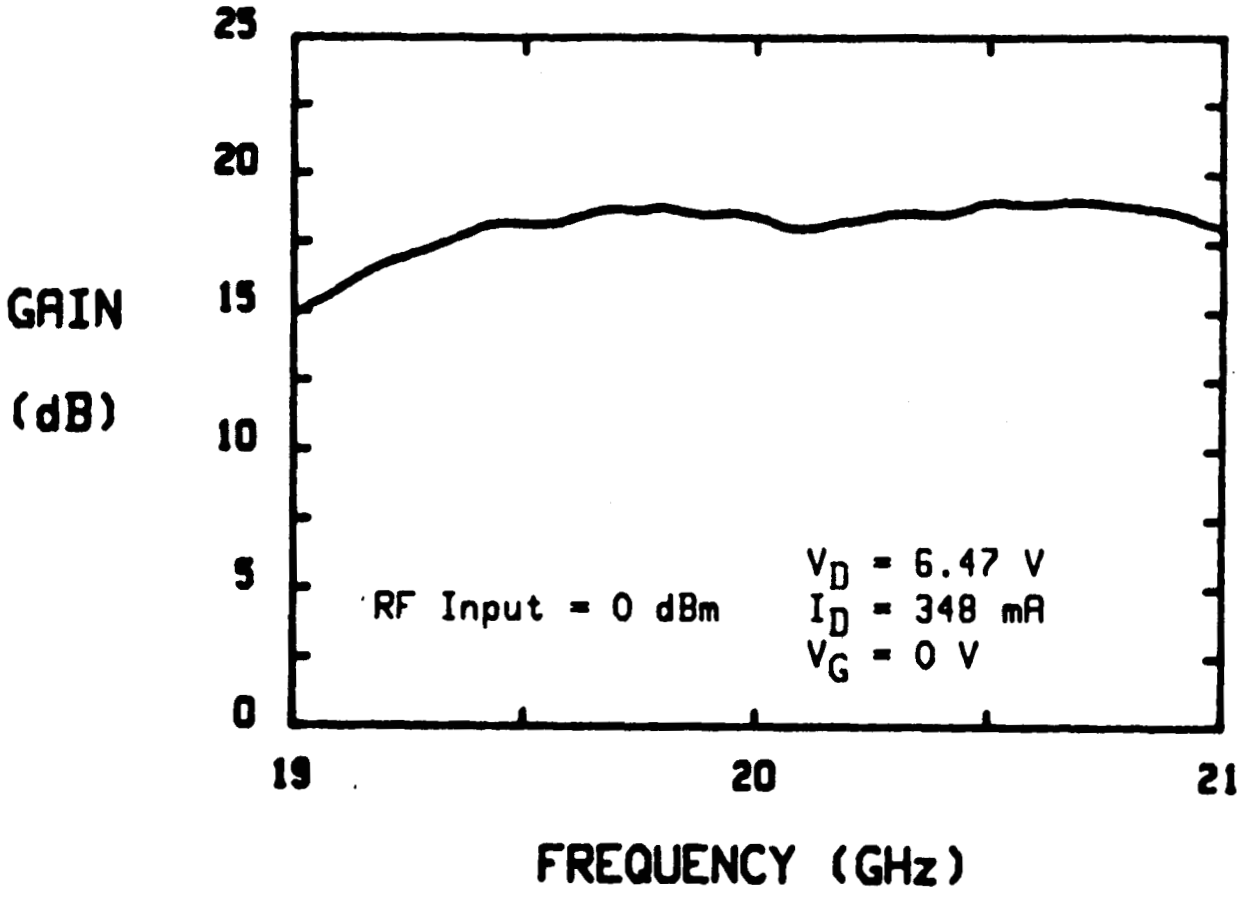


Figure 28 Gain-Frequency Response of a Three-Stage (Modified) Monolithic Amplifier

SECTION IV
MONOLITHIC POWER AMPLIFIER MODULE

The three-stage amplifier design approach discussed in Section III.C uses GaAs FETs with sufficient gate widths to generate the required output power. No circuit-level power combining will be required for such an approach. For both the 0.6 W conventional and distributed amplifiers, power combining will be required. These amplifier configurations are shown in Figure 29. To reduce chip size and maximize the amplifier efficiency, it is possible that for the approach shown in Figure 29(a), only two cascaded (0.6 mm to 1.5 mm) amplifier stages need be used for each of the four component amplifiers within the traveling-wave power divider/combiner. An additional single-ended one- or two-stage amplifier with an output power of ~ 24 dBm (0.25 W) can be used as a driver amplifier to drive the four-way combiner output stage. The exact configuration will be decided based on further trade-off analysis during the early stage of the next report period.

Interconnected traveling-wave divider/combiner and amplifier chips are shown in Figure 30 for the four-stage amplifier and in Figure 31 for the distributed amplifier modules. Further monolithic integration of the bias networks will eliminate the bond wire crossovers for the combiner shown in Figure 30. For the distributed amplifier combiner of Figure 31, the gate and drain biases can simply be injected from the 50 Ω input/output. Figure 32 shows the small-signal gain-frequency response of the distributed amplifier/combiner. Gains on the order of 3 to 5 dB can be obtained from 8 to 20 GHz. At a large-signal measurement frequency of 18 GHz, an output power of 2 W with 2.5 dB gain was obtained. Further optimization the device structure will result in a substantial gain improvement for this combiner.

The comparison and trade-off analysis of the amplifier design approaches described above are shown in Table 3. Analysis in terms of output power, gain, efficiency, bandwidth, and chip size is shown. From Table 3 it is seen that the optimum approach seems to be in favor of the three-stage direct-cascaded amplifier configuration. The only uncertainty in this approach is the ability to match the impedance (particularly the interstage between the second and third stages) efficiently at 21 GHz. With the proper distributed

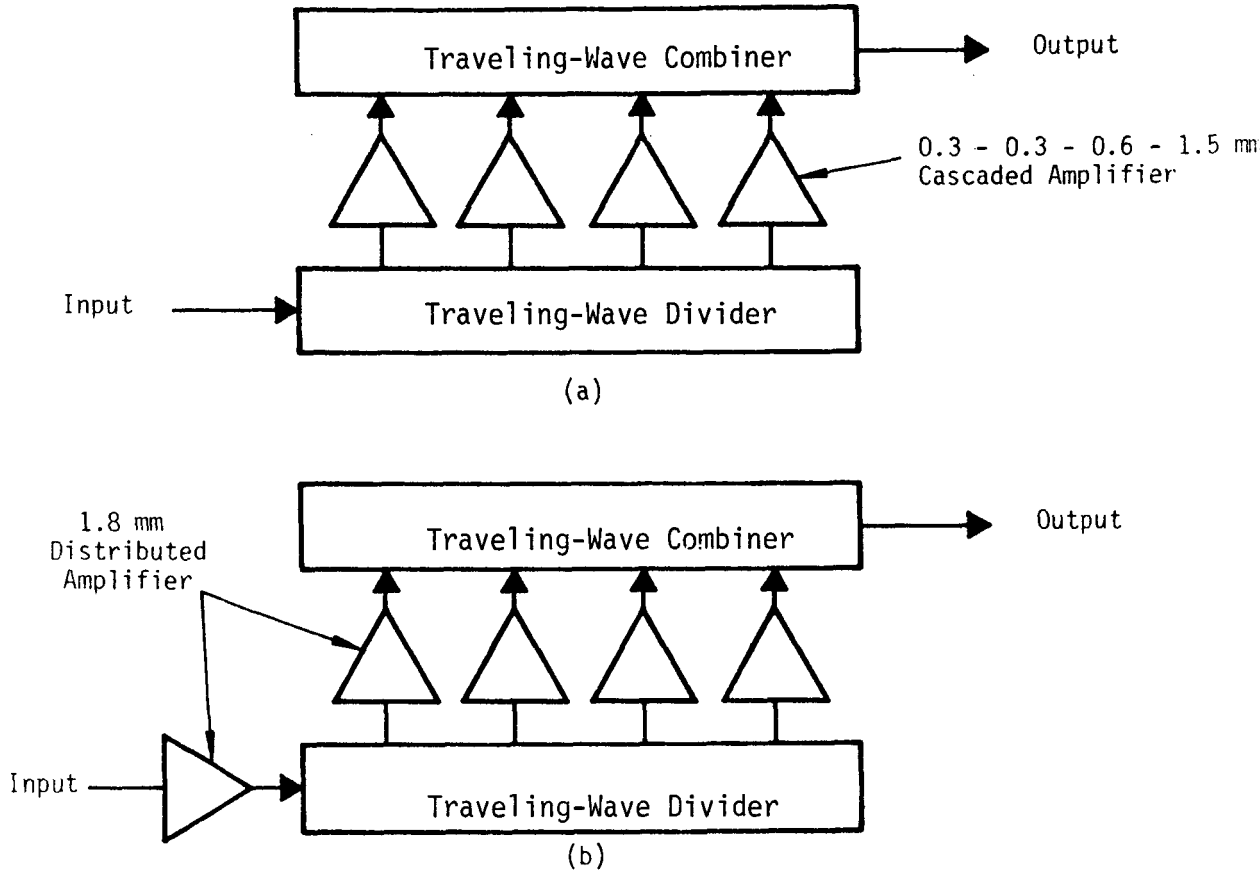


Figure 29 Amplifier Configurations (a) Cascaded Amplifiers with Traveling-Wave Power Divider/Combiner, (b) Distributed Amplifier with Traveling-Wave Divider/Combiner

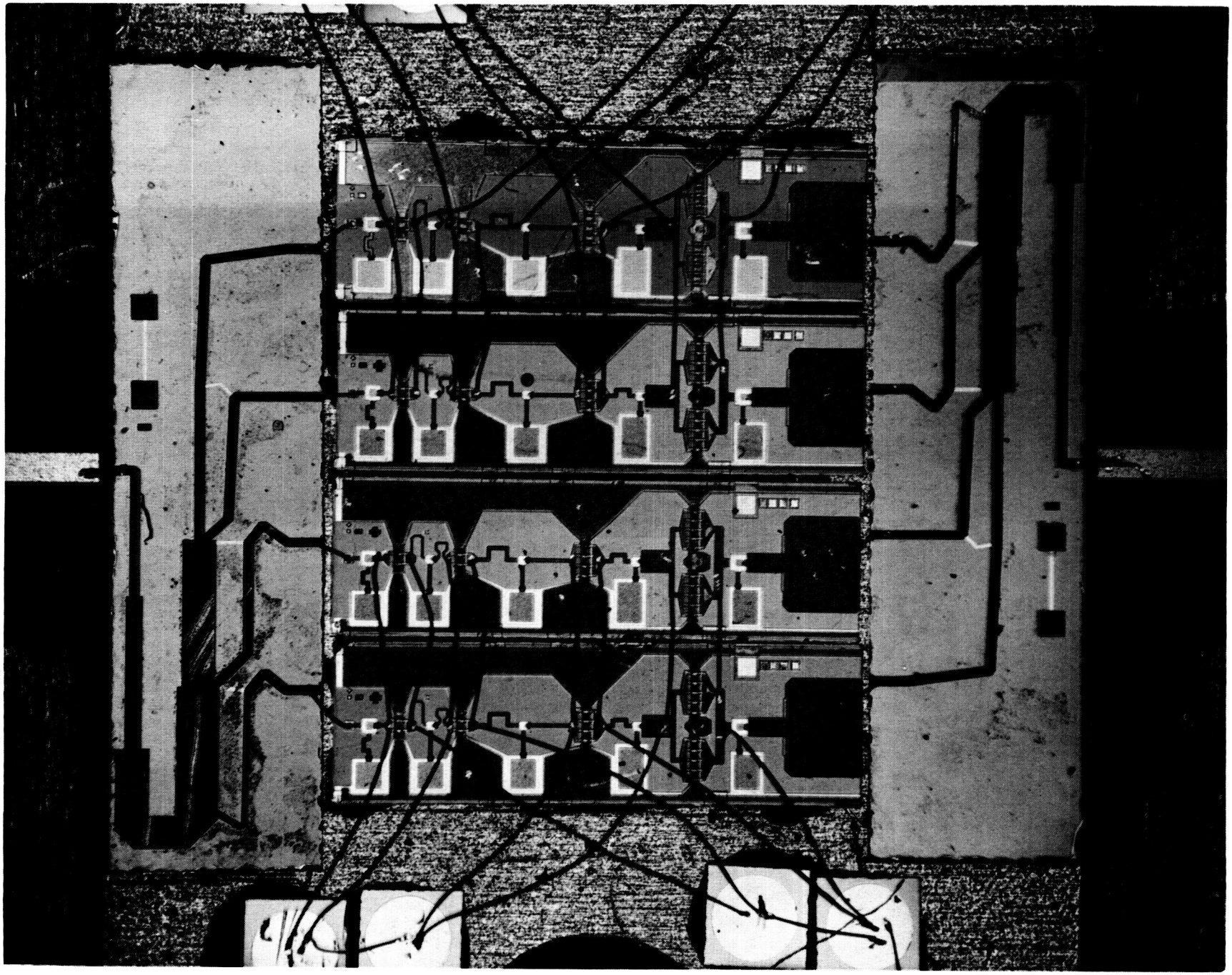
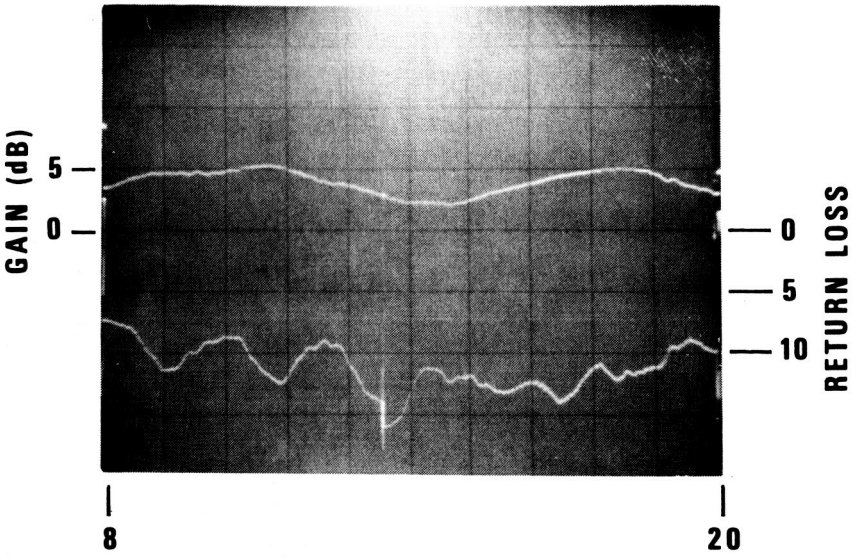


Figure 30 Four-Stage Amplifier with Four-Way Traveling-Wave Power Combiner

Figure 31 Traveling Wave Amplifier with Four-Way Combining



AT 18GHz, OUTPUT POWER=2 WATTS WITH 2.5 dB GAIN

V_d=8.75V

I_d=1.14A

V_g=1.9V

Figure 32 Performance of a Four-Way Combined Monolithic Distributed Amplifier

Table 3
Comparison of Amplifier Design Approaches

Approach	Output Power	Gain	Efficiency	Bandwidth	Chip Size
Three-Stage (Direct)	High	Medium	High	Narrow	Small
Traveling-Wave (With Combiner)	Medium	Low	Low	Ultrawide	Large
Four-Stage (With Combiner)	Medium	High	Medium	Moderate	Medium

nature of the matching circuitry taken into consideration during the next design iteration, it is believed that this approach will be feasible for meeting the goals of this program.

SECITON V
SUMMARY

Achievements in this program for the first 12 month period are summarized as follows:

- Completed development of the monolithic four-way traveling-wave divider/combiner.
  - 1.2 dB insertion loss for a pair of back-to-back connected divider/combiners.
  - Isolation between output ports better than 20 dB. VSWRs better than 2:1.
  - 20 GHz bandwidth (10 to 30 GHz).

- A distributed amplifier using 6 x 300 μm FETs has achieved the state-of-the-art results of 0.5 W output power over the 2 to 21 GHz frequency range with an average gain of 4 dB and 14% power-added efficiency.

- A four-way monolithically combined traveling-wave amplifier has achieved an output power of 2 W.

- An output power of 2 W with 12 dB gain and 20% power-added efficiency has been achieved for the three-stage amplifier. The linear gain was 14 dB at 1 W output (17 GHz).

- A two-stage (1.2 mm to 2.4 mm) amplifier has achieved an output power of 1.6 W with 9 dB gain and 26% power-added efficiency at 16 GHz. The linear gain was 11 dB at 1 W output.

SECTION VI
PLANS

Plans for the next 12 months of the program are summarized below.

- Continue to process and optimize the FET channel parameters for the distributed amplifier using the low-high doping profile.

- Continue to process and evaluate the three-stage amplifier module using the n^+ ledge channel structure.

- Optimize the FET performance for 20 GHz operation.

- Use E-Beam 14 for gate definition to achieve improved gate length control and alignment accuracy.

- Revise the interstage matching network design of the three-stage amplifier with more accurate accounting for the distributed nature of the matching network for improved performance in the 19 to 21 GHz frequency range.

- Complete the mask design for the four-stage 0.6 W module.

- Continue testing of interconnected power combiner and amplifier modules.

- Select the best approach for the final amplifier module.

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