INTERNATIONAL SOLAR-TERRESTRIAL PROGRAM
DATA PROCESSING CONSORTIUM

Purchase Order No. H-78750B

Final Report
UAH Research Report No. 530

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September 3, 1986

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Introduction.

The University of Alabama in Huntsville (UAH) effort for the common design of a Data Proccessing Unit (DPU) for use on the 'International Solar Terrestrial Physics Program (ISTP) began sometime in December 1985 with meetings at Goddard Space Flight Center among all the principals including University of Alabama in Huntsville, University of California, San Diego, University of California, Berkley, University of Washington, and Goddard Space Flight Center. This meeting defined the requirements that such a system should have to accomodate the needs of five instruments in the ISTP program . Appendix 1 combines together these requirements that at this time, we feel the instruments can accomodate. Briefly, the initial design effort covered under this purchase order has allowed us to: 1) investigate the 32016 Prototype board with the tiny development system; 2) acquire the P-CAD development system which allows for automated circuit drawing and circuit board layout, 3) to put down our initial design of the processing unit Mother Data Processing Unit; 4) to begin to establish coordination among all members of the DPU Consortium that can be accomodated over the SPAN network (Space Physics Analysis Network). Most elements of the DPU Consortium now can be addressed on the SPAN network in a routine manner. Appendix 2 gives their SPAN network addresses.

In the interval since this effort began, several new facts have changed the direction of the DPU design. Most importantly, is the fact that the entire ISTP program now looks as if it may be delayed by up to two years. This consideration and the established schedule for the 32016 design at Sandia Laboratories implies that the entire proccessing scheme will be based totally around 32016 processors. Secondly, we now have acquired an operating FORTH language operating system for the 32016 base microproccessor systems with targeted cost compiler. This UNIFORTH system operates and allows one to develop microprocessor code on an IBM PC, cross-compile to the 32016, and then execute code in the 32016. With this capability, we feel that the FORTH operating system is the best to pursue for language and operating systems. It is also probable that there will be a second source FORTH operating system for the 32016 provided by LMI of California.

MAIN PROCESSING UNIT

In the following sections we describe our present conception of the data processing scheme including Main Processing Units (MPU) and Satellite Processing Units (SPU) which will acquire the data for the instruments presently planned in the ISTP Project.

The MPU will be organized into 5 boards and a power supply. The five boards are as follows: 1) Processor Board, 2) Memory Board, 3) Peripheral Interface Board, 4) Spacecraft Interface

Board, and 5) Accumulator Board. The SPU will be organized into 3 boards and a power supply. Three boards are as follows: 1) Processor Board, 2) Peripheral Interface Board, and 3) Accumulator Board.

The MPU's processor board will contain a 32C016 16-bit microprocessor with associated Timing Control Unit and Floating Point Processor. This three chip set computer will provide the processing power required for the in-flight data reduction. The board will contain a minimum of ROM and RAM to execute the FORTH kernel and application software. Circuitry will be included to interface with the rest of the system as well as an RS-232 link for ground testing. A watchdog timer is required to reset the system if a single point radiation failure interrupts processing.

The MPU's memory board will contain a 256k-byte mass memory for burst data storage. This memory will utilize 32 64k-bit chips and associated decoding logic. The processor board will reduce this large amount of data to meet the telemetry constaints of the down link. The MPU's peripheral interface board will provide the necessary interfaces to the SPU and the High Voltage Supplies in the system. The SPU interface will be a Manchester encoded bi-directional data link for command initiation and data recovery. The HV supply interface will be a three wire data transmission scheme utilizing a data path, a gated clock and an data enable.

The MPU's spacecraft interface board will provide the necessary interface to the satellite for data transmission to the ground, and data reception of satellite position and ground commands. Since this interface has not been determined, a full card slot has been dedicated for use.

The MPU's accumulator board provides the data recovery from the particle detectors in the system. The board will comprise 82C54 counter/timers which contain three 16-bit accumulator channels. Associated circuitry will control the accumulation interval and enable data to the processor.

The SPU will use the same boards as the MPU except some part will be removed. The SPU's processor will not require the memory interface and high level of subsystem decoding as required in the MPU. The rest of the SPU is anticitated to be identical to the MPU.

Software

The system software for the 32C016 processor boards will use the FORTH programming language. The software will be written on an IBM compatible computer and can down loaded to the MPU or SPU RAM for testing before the final code is cross-compiler to ROM for flight. FORTH was chosen because of its ease of programming and debug, personnel experience, and its close control of processor functions. Since the units provide a terminal ground link, test code can be downloaded during ground testing and deleted for flight for optimum use of processor memory.

Present and Future Work

The MPU will be modeled after telemetry units in use on sounding rocket programs. The new processor board is in the could be built and tested in a following design phase and a wire-wrapped prototype could be built. A similar design board utilizing the 32C016 processor will be built and flight tested on a sounding rocket in 1QFY87. Design of the spacecraft interface board is awaiting definition of the interface or design of the spacecraft subsystem.

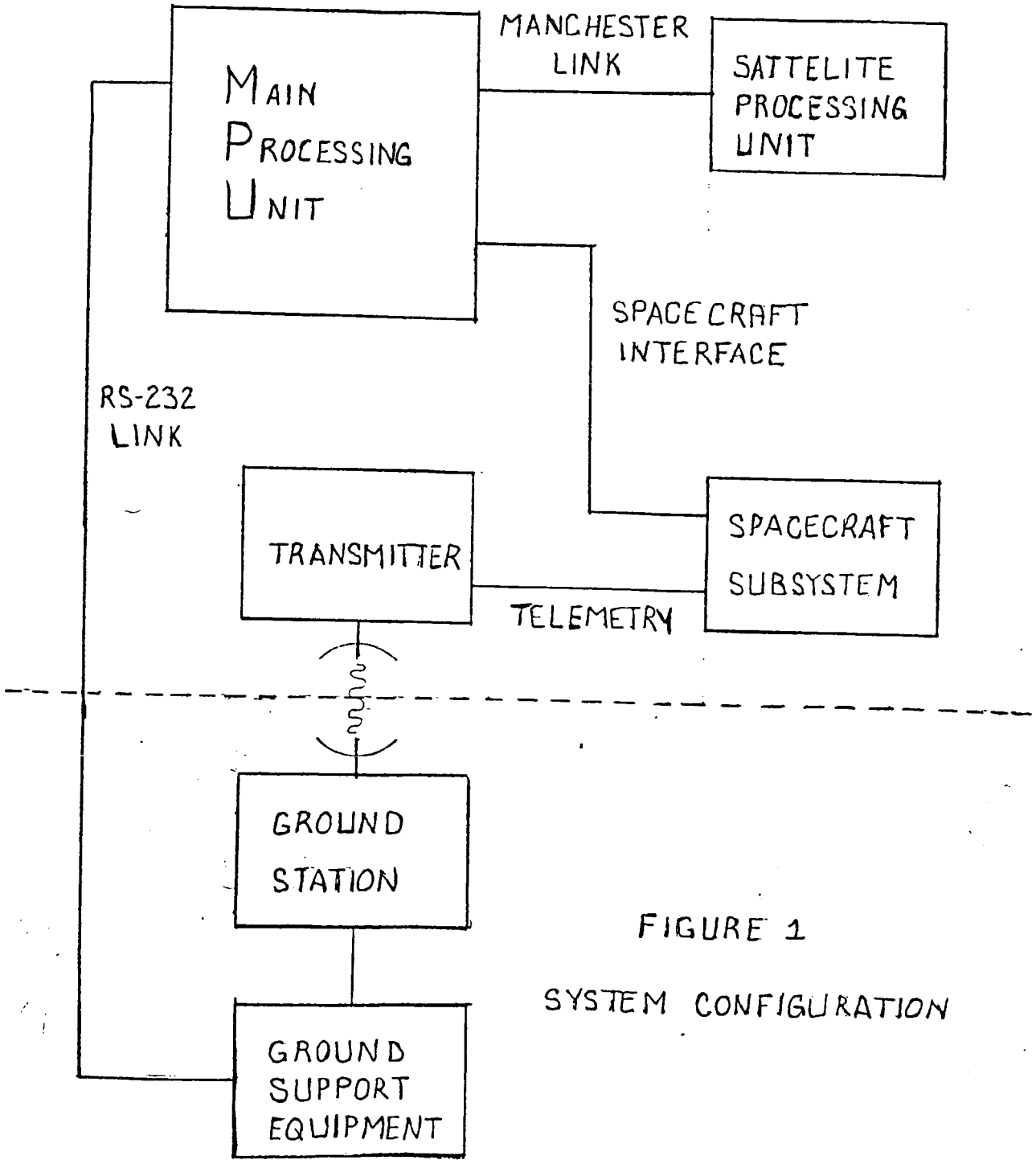
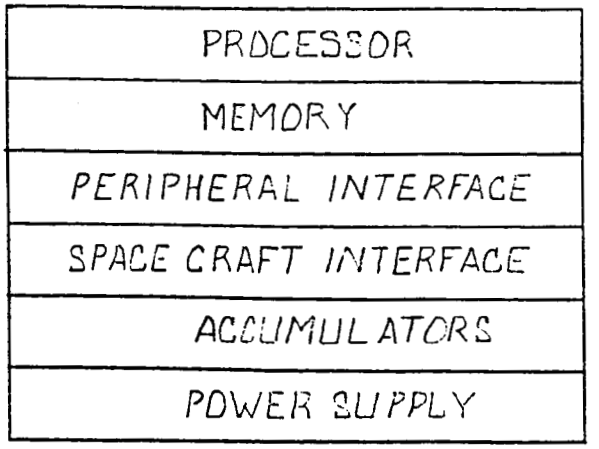
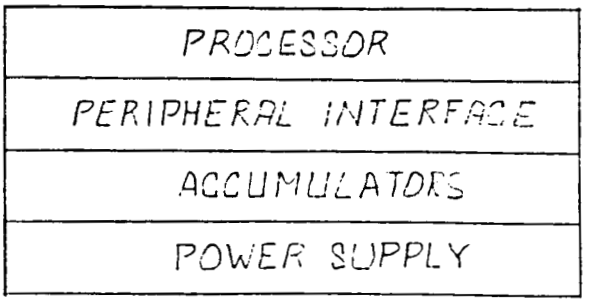


FIGURE 1

SYSTEM CONFIGURATION



MAIN
PROCESSING UNIT



SATELLITE
PROCESSING UNIT

FIGURE 2
UNIT CONFIGURATION

Appendix 1 : Requirements for
Common DPU's

Design vs Fabrication Phases

Design will be shared amongst UCB, UCSD, and UAH.. Fabrication will take place at UCSD, layout at UCB..

Budgetary Management Guidelines

Note, in the following matrix, that money can flow along vertical lines without such penalties as double overhead charges, etc., and that startup occurs along horizontal lines, ie: Wind gets funded before Polar and Equator.. Partly this is because U Wash doesn't charge overhead on subcontracts, and because a contract at one branch of the U Cal can pay costs incurred at another branch without subcontracting it..

	U Cal, U Wash	GSFC
Wind	Lin	Ogilvie
Polar/Equator	Parks, McIlwain	Scudder

For the design phase it is up to each (vertical) funding family to balance their costs internally, so that money does not have to pass back and forth horizontally.. There is one exception to this separation, and that is that UCB will provide to UCSD a 10 K$ budget to enable UCSD to monitor the initial design and participate as much as it can..

During the fabrication phase, each participant will have to break the budget he presents to the project into two parts: one that he spends for his purposes alone, and the other which is his share of the the common microprocessor effort.. Microprocessor features that are not part of the common design must be provided and paid for by the individual.. If fabricated at UCSD, the individual will be billed separately..

Management

At the scientific level, the highest authority will be a council of the PI's and Co-I's.. For day to day tracking of details, There will be a Manager for the design phase and another for the fabrication phase.. Dave Curtis was nominated for the design phase, and Roy Torbert for the fabrication phase..

Communications

Use the SPAN network, with CAD/CAM utilities..

Technical Features

It was proposed that the main and peripheral processors have the same board sizes and backplane bus..

It was suggested that the backplane bus should be based on the IBM PC or PC/AT bus or a subset thereof..

Intercommunications should be via serial lines with several priority lines..

The box that houses the microprocessor should not be included in the common design, as different experiments will use different numbers of boards.. However, the boxes are constrained by the choice of board size, and so the mechanical interface that the box has to meet will be called out..

Technical Requirements

	Lin	Ogilvie	Parks	Hydra	Efields
Configuration					
Main	1	1	1	1	1
Daughters	2	?	2	1	1
Stepdaughters					3
Number of serial interfaces					
on main board	2	1	2	1	4
Count accumulators (16 bit)					
Main	16	16	0	24	?
Daughter	48	16	48	24	8
Daughter	48		48		
D/A Controllers (HV/Discr.)	0	4	0		?
Main				1/2	
Daughter				1/2	
Digital Lines for Device Control		4			8*n
Main	8		0	8	
Daughter	8		8	8	
Daughter	8		8		
>64 kbit external memory	y	y	y	y	y
Spacecraft Interface	y	y	y	y	y
Ground Support Equipment	y	y	y	y	y

Spacecraft Simulator	y	y	y	y	y
RS232 Interface	y	y	y	y	y
Power Converter	y	y	y	y	y
power allocation	12 W	?	10 W	8 W	13-15W
Digital Timing Lines	~2	8I, 8O	~2	8	?
Analog sampling	8x8bits	-	nx8bits	nx8bits	?
Memory, main processor					
error-corrected RAM	16K	16K	16K	16K	16K+8K
ROM	32K	32K	16K	32K	32K
Memory, peripheral processor					
error-corrected RAM	8K		8K	8K	
ROM	8K		8K	8K	

The processor board includes
- CPU
- Clock oscillator
- Timing functions with 82C54 registers
- ECCRAM and ROM
- Reset line
- Watchdog timer
- RS232
- Digital control bits
- Serial interfaces

Common Fabrication Budget

6 styles of boards. 1 prototype, 1 flight unit apiece..

	4 expmts	5 expmts
Layout	100 K$	100 K$
Assembly (3 people x 3 years)	470 K$	580 K$
Outside help for peak loading	100 K$	120 K$
PC board procurement	50 K$	65 K$
Parts	800 K$	1000 K$
Quality Control Subcontract	100 K$	100 K$
Supplies	80 K$	100 K$
GSE boards	20 K$	25 K$
Management (0.25 man-year during layout) (1 man-year during fab)	110 K$	120 K$
	1830 K$	2210 K$
Average Cost per Share	460 K$	440 K$

Appendix 2 : SPAN Addresses

UCSD : CASS::CEM (McIlwain)
CASS::Fillius

UAH : OPTICS::TORBERT
::BODET
::SISK

GSFC : LEPVAX::U2JDS (Scudder)
::USKWO (Ogilvie)

UCB : STAR::"DWC%SSL@BERKELEY.EDU" (Dave Curtis)

UWASH : (still undefined)