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Pulse Code Modulation (PCM) Encoder Handbook for Aydin Vector MMP-600 Series System

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Scientific and Technical Information Branch

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for
AYDIN VECTOR MMP-600 SERIES SYSTEM

Stephen F. Currier and Wayne R. Powell

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INTRODUCTION

The information required to effectively and reliably use the Aydin Vector Division MMP-600 series pulse encoder system is presented in this document. The system capabilities and limitations are defined and required interfacing information is provided. Assimilation of this information by instrumentation systems designers prior to the conceptual definition of mission instrumentation systems will increase the probability that this encoder system can satisfy mission requirements.

Due to the system's small size, low power consumption and programmable flexibility, a broad range of telemetry data transmission requirements can be satisfied by this encoder system. Frequently recurring mission data transmission requirements are accommodated in short response times by stocking a library of standardized input expansion modules at NASA Wallops Flight Facility. By drawing from this library, a mission unique encoder system can be assembled.

The modules are procured as commercial grade sub-assemblies. Component and systems level functional tests are performed by the manufacturer. The systems are screened at mounting plate temperature extremes of -35 degrees Centigrade and +85 degrees Centigrade. A "standard" encoder component composition programmed for a typical output format is employed for systems level tests.

When the mission's data requirements are defined, the necessary parts are issued from the NASA Wallops Flight Facility library of PCM components. The modules are assembled into the required configuration and programmed for the desired output format. Functional and vibration testing is then performed in that configuration.

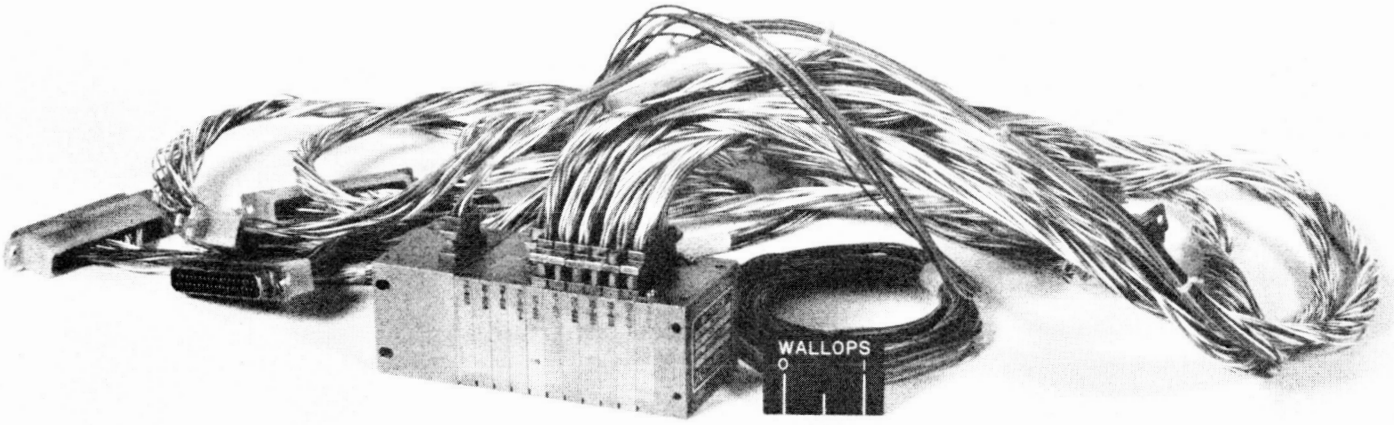


Figure 1a.-Typical MMP-600 microminiature PCM encoder system shown with interface connectors.

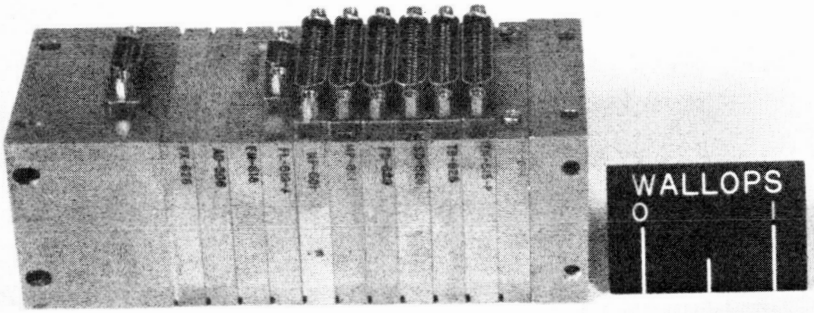


Figure 1b.-Typical PCM stack.

GENERAL DESCRIPTION

The PCM encoder system (Figures 1a and 1b) has flown on more than 50 sounding rockets without an in-flight anomaly. An exploded view of a typical stack is shown in Figure 2 and the general block diagram of the system is shown in Figure 3. Combinations of analog and digital data inputs are accepted by this system which consists of standard plug-in modules from two groups:

Group I

One each of the modules listed below are required in every system.

PX-628 Power Supply.-This module is a synchronous isolated power supply which also includes the basic oscillator for the system. Eight bit rates are programmable at this module of 6.25, 12.5, 25, 50, 100, 200, 400, 800 kilobits per second. An external clock input exists at the power supply module. Bit rates of up to one megabits per second are attainable using this 0 to +10 volt input.

PR-614 Processor.-This module contains the processor control circuit. The PR-614 functions as a microprocessor executing the software program entered into the 256 x 8 erasable programmable read-only memory (EPROM) and controls the timing and operation of the entire system.

FM-618 Formatter.-The FM-618 receives all of the digital data, which is supplied by the AD-606 and all of the digital multiplexers except the serial digital module. The FM-618 then performs parallel to serial conversion as necessary and merges the digital data with synchronization words.

TM-615P Timer.-This module receives the serial output from the formatter module. The timer then converts this data into the desired PCM codes Bi-Ø-L, NRZ-L, Bi-Ø-M, Bi-Ø-S, NRZ-M, NRZ-S. Test point outputs, such as bit clock, word clock, and frame synchronization pulses, are also provided by the timer. A 2X bit clock is available at the timer module. This 2X bit clock is the only system output that is not low power TTL compatible; it is a 0 to +10 volt output and can be used as an input to the external clock input at the power supply module to run multiple MMP-600 systems synchronously. Programmable parameters at the timer module are number of bits per word (8, 9 or 10 bits selectable), odd or no parity select, sample settling time, and output code.

EP-612 End Plate.-This module contains the removable EPROM and terminates the stack.

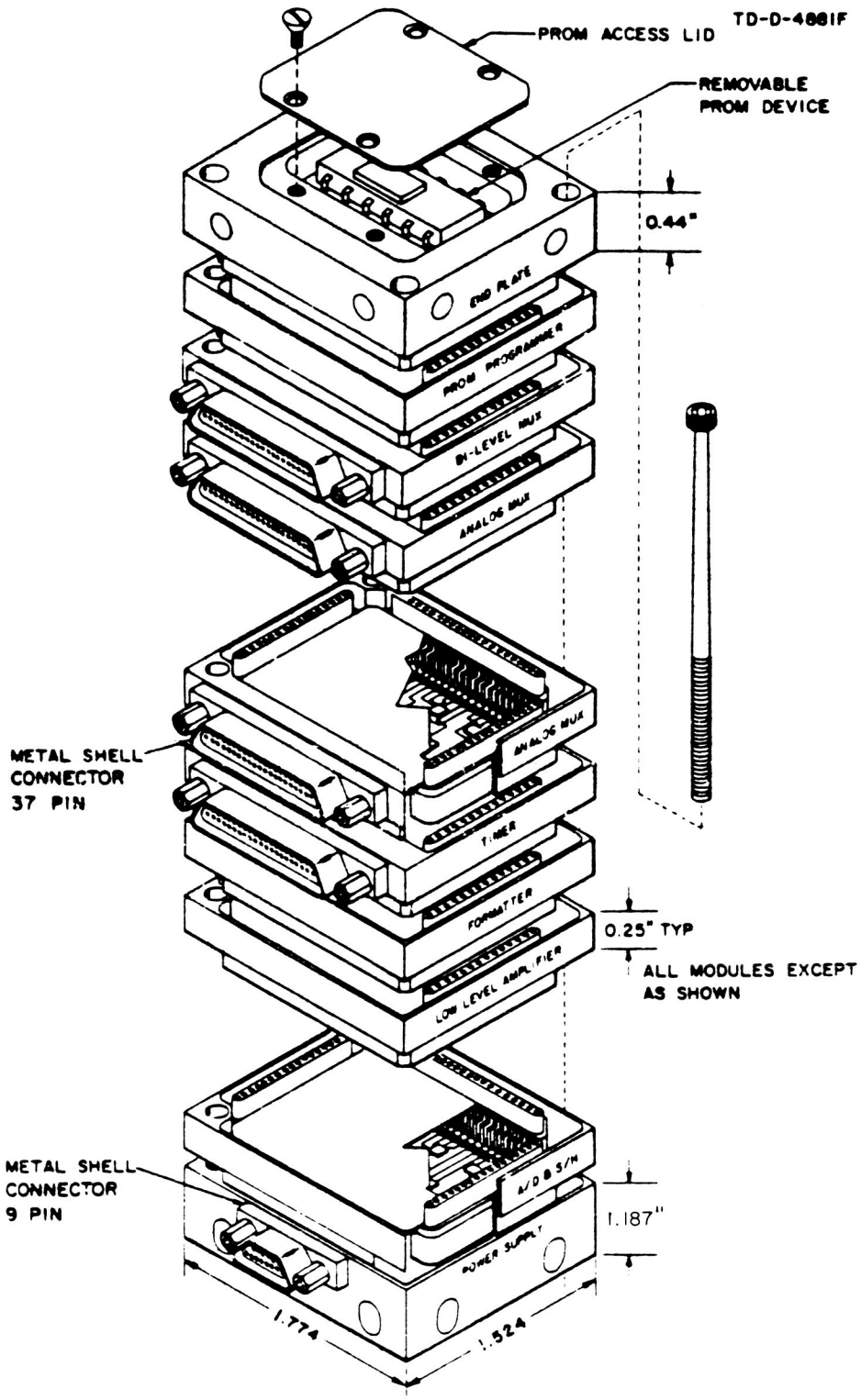


Figure 2.-Exploded view of PCM encoder system

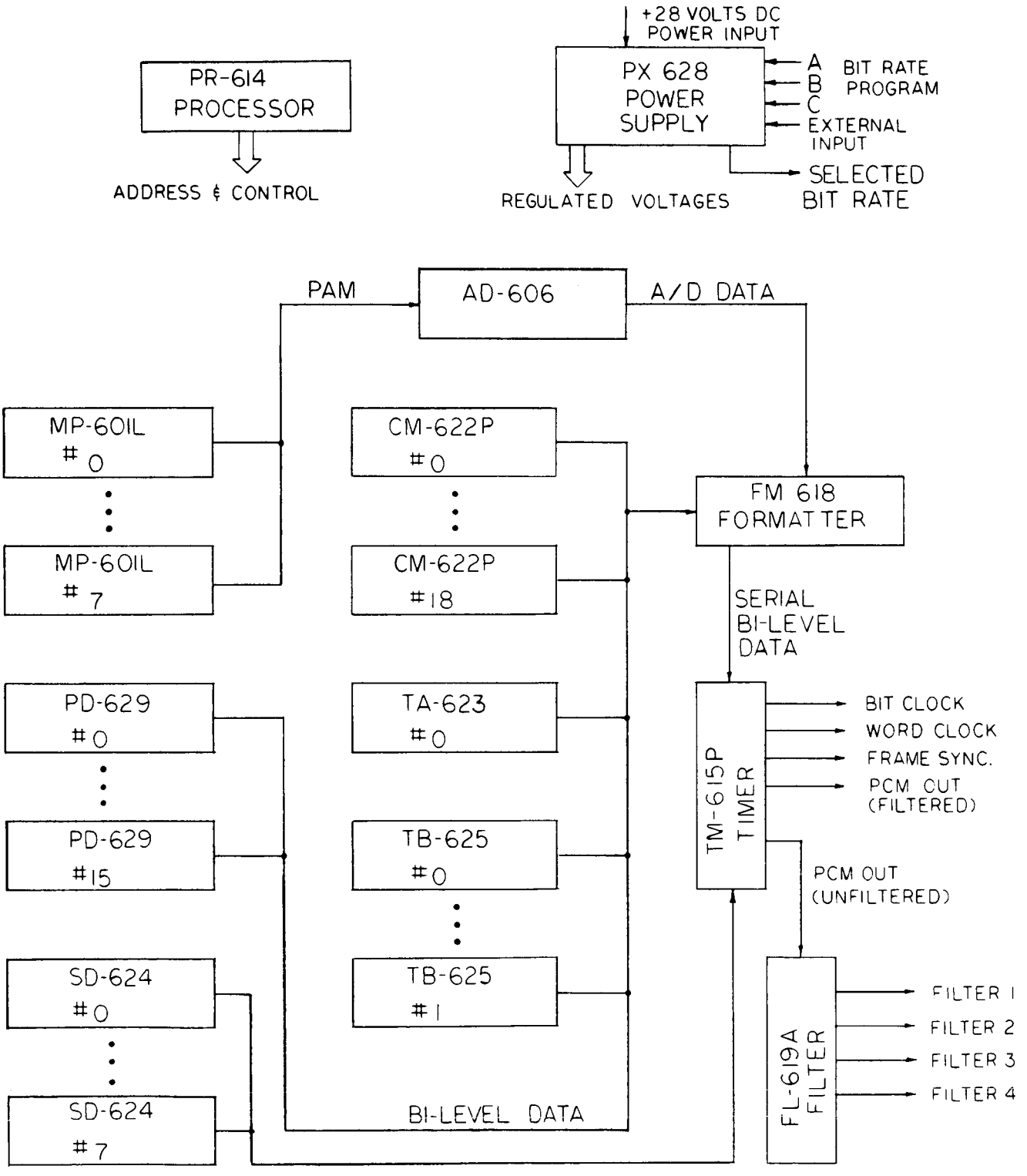


Figure 3.-General block diagram of system

Group II

Use of each module in this group is optional. Variable quantities of each module can be used depending on the data input requirements.

AD-606 Sample and Hold and Analog to Digital Converter (ADC).-This module is required only when analog data inputs are present. This module accepts inputs from the analog multiplexers and digitizes each sample into 10 bits of resolution. Only one is required per system.

MP-601L 32-Channel High Level Analog Multiplexer.-This module accepts 32 analog inputs from 0 to +5 volts. Eight is the maximum number of MP-601L modules per system.

PD-629 30-Input Bi-Level Multiplexer with Two Enables.-This module accepts up to three parallel digital channels with each word containing 8, 9 or 10 bits. Sixteen is the maximum number of PD-629 modules per system.

SD-624 Serial Digital Data Multiplexer.-This module accepts up to eight serial digital inputs with word lengths of 8, 9 or 10 bits. Four is the maximum number of SD-624 modules per system.

CM-622P Dual Counter/Accumulator.-This module counts pulses. Each CM-622P includes two counter/accumulators. Nineteen is the maximum number of counter modules per system.

TA-623 Time Event Monitor with Alternating Registers.-This module accepts two event pulse inputs and is used to determine the relative time of occurrence of events. The alternating registers reduce the rate at which this module must be read out. One is the maximum number of TA-623 modules per system.

TB-625 Time Event Monitor and Timing Buffers.-This module accepts two event pulse inputs and is used to determine the relative time of occurrence of events. The timing buffers provide counter outputs of word number per frame and minor frame number. Two is the maximum number of TB-625 modules per system.

FL-619A Quad Filters.-This module provides four lowpass premodulation filters to filter the serial output. The amplitude of the voltage output is adjustable with a potentiometer on this module.

Refer to specific sections of each module for a complete description. The information here is intended only as introductory material.

TABLE 1. EPROM PROGRAMMING CODES* FOR SELECTING DATA CHANNELS

Module Name	Address Line A7	A6	A5	A4	A3	A2	A1	A0	Channels per Module	Maximum No. of Modules per System
MP-601L	M	M	M	C	C	C	C	C	32	8
PD-629	O	O	M	M	M	M	C	C	3	16
SD-624	O	O	M	M	X	C	C	C	8	4
CM-622P	O	O	M	M	M	M	M	C	2	19
TA-623	(See Table 15)								2	1
TB-625	(See Table 15)								2	2

M = Module select bit
C = Channel select bit
O = Must program a "0"
X = Don't care

*These programming codes are to be used in the EPROM program.

MULTIPLEXING CONTROL

The multiplexing sequence is determined by means of an eight-bit parallel address, A0 - A7, generated by the processor module and bused internally to all multiplexer modules. The most significant bit (MSB) is represented by A7 and A0 represents the least significant bit (LSB) of the address lines. The higher order address lines select a multiplexer module and the lower order address lines select a single channel within that module. In the system program written into the EPROM, each multiplexer module is assigned a unique address. Since all multiplexer modules of the same type are interchangeable, each module must be programmed with a unique address. This is accomplished by grounding appropriate programming pins on the external connector of the multiplexer modules. A module is enabled when the address at the module agrees with the state of the address lines, which update at the word rate. The EPROM programming codes required for each multiplexer module are listed in Table 1, and the operation of the MP601L analog multiplexer is illustrated in Figure 4.

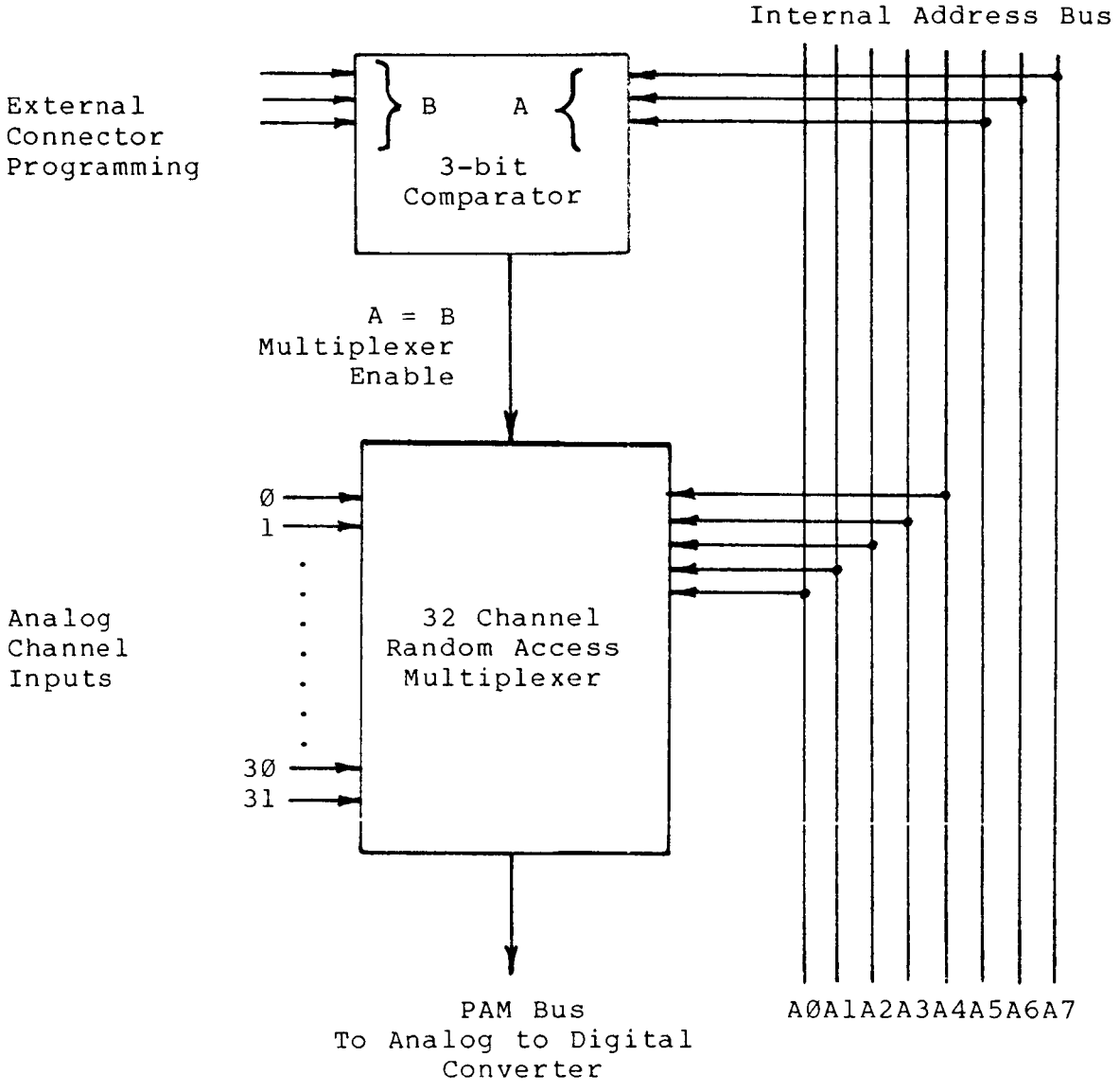


Figure 4.-MP-601L analog multiplexer block diagram

The address line functions of the individual multiplexers are listed below:

MP-601L	A0 - A4 channel select; A5 - A7 module select
SD-624	A0 - A3 channel select; A4 - A5 module select; A6 = 0, A7 = 0
PD-629	A0 - A1 channel select; A2 - A5 module select; A6 = 0, A7 = 0
CM-622P	A0 channel select; A1 - A5 module select; A6 = 0, A7 = 0.
TA-623	See specific module section
TB-625	See specific module section

EPROM CONTROL AND DATA FORMAT

The user written system program residing in the 9702A ultraviolet 256 x 8 EPROM is responsible for several system format characteristics:

- The system program sets the sampling rate of all analog and digital inputs. Variable sampling rates are achieved by using subcommutation and supercommutation within the data sampling format.
- The bit pattern and the number of frame synchronization words appearing in the format are under EPROM control.
- The location of each measurement (input channel), synchronization words and the subframe identification within the data format are under EPROM control. The subframe identification word must precede the first subcommutated data word.
- Major and minor frame lengths are under EPROM control. Allowing three percent to five percent of the 256 EPROM address locations for synchronization of words, a major frame length of 247 words is possible (without subcommutation in the format). When subcommutation is used, maximum minor frame length is governed by the following equation:

$$L = 256 - 2F - \Sigma Qn\ (n + 2) \qquad (1)$$

where

L = Maximum minor frame length

F = Number of frame synchronization words in one minor frame (include subframe identification counter word)

Qn = Number of subframes that are n words in depth

n = Subframe depth (number of words in subcommutation)

Minor frame length is limited only by equation (1). Subcommutation is possible to a subframe depth of 32 in the following increments: 2, 4, 8, 16, 32. Non-binary subframe depths (such as 5, 10, and 20) can also be provided. A sample format is displayed in Figure 5, and an explanation of the frame lengths (equation (1)) follows.

Format Length

Applying equation (1) to the sample format given in Figure 5, we obtain the following equality:

$$L = 256 - \underset{\text{sync. words}}{8} - [\ \underset{\text{words 11\&12}}{2(2+2)} + \underset{\text{words 14\&15}}{2(4+2)} + \underset{\text{words 17\&23}}{2(8+2)}\ ]$$

$$L = 208$$

This result states there are 208 unused address locations within the EPROM. It is possible to address 208 additional channels either at the mainframe rate or supercommutated. Using subcommutation will diminish the number 208 according to equation (1).

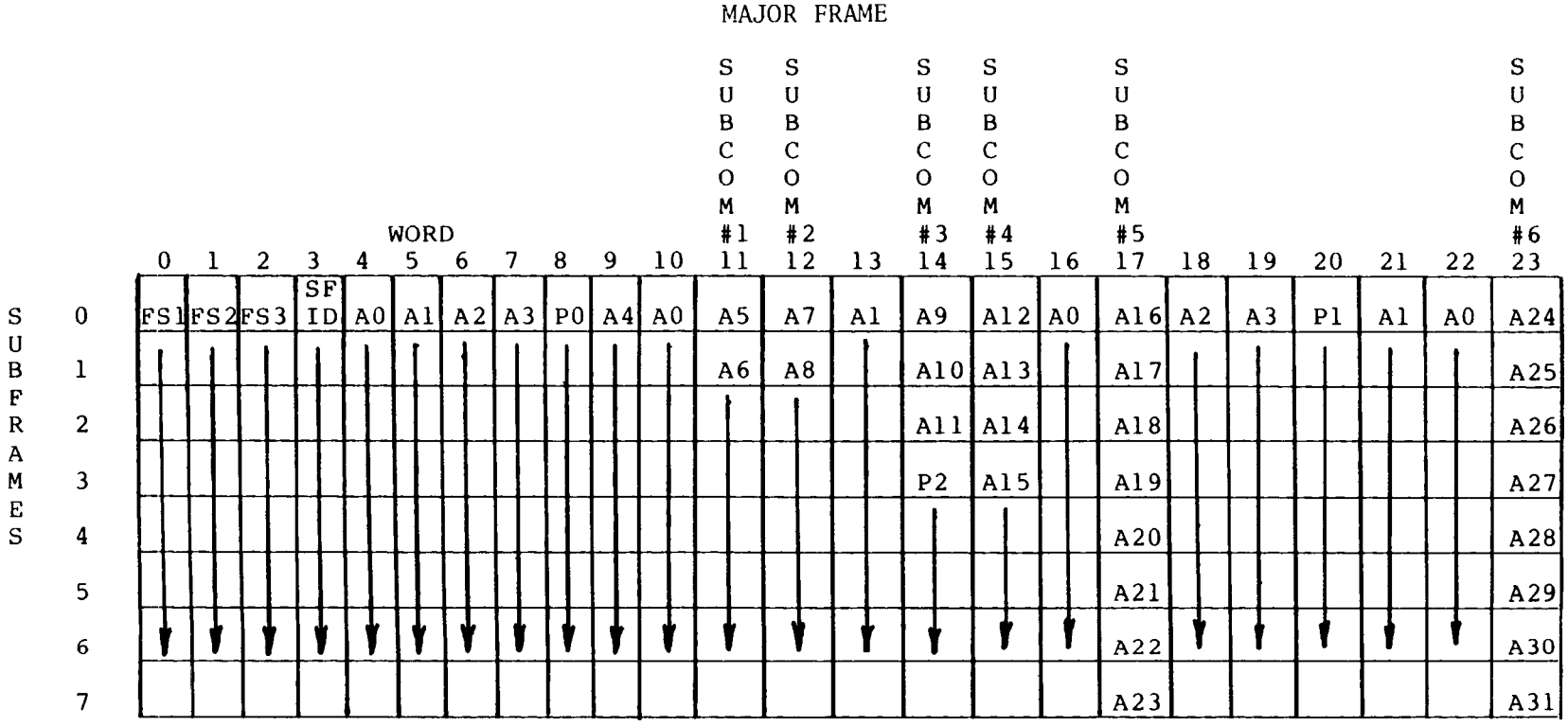
SYSTEM SPECIFICATIONS

Bit Rate Stability

The crystal clock in the PX-628 power supply provides ± 0.02 percent error maximum. The bit rate stability for systems employing an external clock follows the stability of the external clock used.

Frame Synchronization

The number, bit pattern and location within the format of the frame synchronization words are all under EPROM control and can be programmed as desired. When subcommutation is used, a subframe identification counter word is used to determine the minor frame count. Typically, three to five percent of the format should be



Subframes = Minor Frames (0-7)
FS1, FS2, FS3 = Frame Synchronization Words
SFID = Subframe Identification Counter Word
An = Analog Data Channels, Pn = Parallel Digital Data Channels

Bit Rate = 200 Kilobits/Second, Word Rate = 20 Kilowords/Second, (10 bits per word)
A0 = Supercommutated Data Channel 3333.44 samples per second
A1 = Supercommutated Data Channel 2500.08 samples per second
A2, A3 = Supercommutated Data Channels 1666.72 samples per second
A4, P0, P1 = Data Channels at Mainframe Rate 833.36 samples per second
A5 through A8 = Subcommutated Data Channels 416.68 samples per second
P2, A9 through A15 = Subcommutated Data Channels 208.34 samples per second
A16 through A31 = Subcommutated Data Channels 104.17 samples per second

Figure 5.-Sample data format

synchronization words. The subframe identification counter word must precede the first subcommutated data word.

PCM Output Formats

Bi-Ø-L, Bi-Ø-M, Bi-Ø-S, NRZ-L, NRZ-M, NRZ-S are selectable at the timer module. (See Figure 10 for further explanation and description of these codes.)

Unfiltered PCM Output Level

The unfiltered PCM output is COS-MOS and low power TTL compatible. Logic "0" falls in the range 0 to +0.1 volt dc. Logic "1" falls in the range +5.0 to ±0.5 volt dc. The output impedance is one kilohm maximum.

Premodulation Filter

The premodulation filter is a linear phase low pass filter. The final roll-off slope is -36 dB per octave past the -3 dB point of the filter. A single premodulation filter is available in some TM-615P timer modules. A low pass filter with 280 KHz fco is used for systems using Bi-Ø-L outputs with a bit rate of 200 kilobits per second. The output is 2.0 volt peak-to-peak centered about 0.0 volt. A second TM-615P module has a low pass filter with 560 KHz fco. This filter is used with systems employing a Bi-Ø-L output at a rate of 400 kilobits per second. The output of this second filter is 4.0 volt peak-to-peak centered about 0.0 volt. The formulas for selecting a premodulation filter are:

0.7 x bit rate = fco for systems using NRZ-L output
1.4 x bit rate = fco for systems using Bi-Ø-L output.

Additional Premodulation Filters

Four additional filters are available at the FL-619A quad filter module. Low pass filters with -3 dB corner frequencies of 8.8, 11.5, 17.5, 23, 35, 46, 70, 92, 140, 280, 560, and 1120 KHz. Four filters are available per module. The proper module part number must be used to get the desired characteristic. The output voltage level is adjustable from 0.1 volt peak-to-peak through 10.0 volts peak-to-peak centered about 0.0 volt. (See the section on the FL-619A quad filter module for additional information.)

Word Structure

Word length is fixed such that all words are the same length within a single system. The transmitted bit sequence for analog and counter data is MSB first and LSB last. The AD-606 Sample and Hold and Analog to Digital Converter Module is a 10-bit analog to digital converter. Using word lengths less than 10 bits causes the LSB's to be truncated.

Resolution

The number of bits per word is determined by the resolution programmed at the timer module connector. Eight, nine, or ten binary bits are selectable. Other multiplexer modules that must be programmed for word length are the CM-622P Dual Counter/Accumulator and the SD-624 Serial Digital Data Multiplexer.

Linearity

The ADC's deviation from a best straight line is $\pm\frac{1}{2}$ LSB maximum.

Analog Accuracy

The worst case for analog accuracy occurs when a high number of analog modules are incorporated into a system (eight analog modules maximum), the bit rate is very fast (800 kilobits per second maximum using internal clock), and a short word length is used (eight bits per word minimum). The accuracy becomes a capacitive decay problem when approaching worst case conditions. Assuming 15 picofarad bus capacitance per module, eight bits per word and a high source impedance of 5000 ohms and a high bit rate of 800 kilobits per second, the analog error is 0.35 percent $\pm\frac{1}{2}$ LSB (the percentage refers to full-scale input of +5 volts). The analog error associated with a "typical" system is less than 0.01 percent $\pm\frac{1}{2}$ LSB. These numbers assume a system with eight bits per word, an 800 kilobits per second bit rate, a source impedance of 1000 ohms and five analog modules in the stack. For maintaining accuracy, it is recommended to use a source impedance of less than 100 ohms. For more information, refer to the MP-601L section.

Analog to Digital Conversion

The conversion process is accomplished using the method of successive approximations. Digitization is performed at a fixed rate of approximately 1.6 MHz which is generated by an internal clock. For more information refer to the AD-606 module section.

ELECTRICAL SPECIFICATIONS

Power Input

The power input is +28 volts ±4 volts dc. An input voltage in excess of +37 volts will cause permanent damage.

Reverse Polarity Protection

A continuous supply of -32 volts dc applied to the power input pin will not cause permanent damage to the system. There will be no current flow because of a reverse biased input protection diode.

System Grounding

The signal, power and chassis grounds in the system are all mutually isolated. For most applications it is recommended to bring each of these system ground points to a single common reference.

Current Drain

The current drain depends on the exact system configuration. The typical range is from 200 to 500 mA.

Fault Protection

With all outputs shorted to signal ground, no permanent damage to the system will result.

Data Channel Inputs

All data channel inputs are CMOS and low power TTL compatible.

Analog channels are single ended and accept 0 to +5 volt dc inputs. The analog inputs can range between -35 volts to +35 volts dc on all channels without permanent damage to the module. It is recommended that no more than 20 inputs per module be subjected to the voltage extremes simultaneously.

Bi-level parallel channels accept -35 volts to +2.0 volts dc inputs to provide a logic "0" output and +3.5 volts to +35 volts dc inputs to provide a logic "1" output. Voltages outside this range will cause permanent damage to the module.

Serial digital channels accept -1.5 to +0.9 volt dc to provide a logic "0" and +3.15 to +6.5 volts dc to provide a logic "1" output. The serial digital inputs can tolerate voltages of -1.5 volts to +6.5 volts without causing permanent damage to the module.

Input pulses to be counted shall be 0 to +5.0 volts dc for a minimum duration of 500 nanoseconds. For input pulses to be counted with an amplitude less than a full +5.0 volts, the pulse duration shall be a minimum of 1000 nanoseconds. There is a single pole lowpass filter at the counter input to limit false counts due to noise. The RC time constant is 0.5 microsecond. The inputs to pulses to be counted are CMOS or low power TTL compatible. (Typically, CMOS or TTL is less than 0 to +5.0 volts.) Voltages applied to the inputs outside the range -0.5 to +5.5 volts dc will cause permanent damage to the counter module.

Time event pulse inputs, used to measure relative time between pulses, shall be 0 to +5.0 volts nominal and be of duration one microsecond minimum to insure triggering of the module. Voltages applied to the inputs outside the range -0.3 to +36 volts will cause permanent damage to the time event modules.

Program Inputs

Several programmable parameters are associated with this system. The programming inputs on each of the programmable modules use a positive logic system. Programming is accomplished by grounding appropriate pins on the external connectors of these modules or by use of a logic interface. An ungrounded programming pin will be interpreted as a logic "1". All pull-up voltages are referenced to signal ground.

Programming inputs on the:

(1) PX-628 are pulled up to 10 volts through 10 kilohm resistors,

(2) TM-615P are pulled up to 10 volts through 30 kilohm resistors,

(3) MP-601 are pulled up to 10 volts through 10 kilohm resistors,

(4) PD-629 are pulled up to 10 volts through 30 kilohm resistors,

(5) CM-622P are pulled up to 10 volts through 20 kilohm resistors for the address lines and through 50 kilohm resistors for the word length program inputs,

(6) SD-624 are pulled up to 10 volts through 20 kilohm resistors for the address lines and the word length programming inputs are pulled up to 5 volts through 20 kilohm resistors,

(7) TA-623 are pulled up to 10 volts through 30 kilohm resistors, and

(8) TB-625 are pulled up to 10 volts through 30 kilohm resistors.

The specifications given above are limits to the system and a reliable interface design will fall well within the tolerances listed above. For additional input interfacing information, see the specific module sections.

MECHANICAL SPECIFICATIONS

Size

The overall size of a 32-channel high level analog PCM system is 1.52" x 1.77" x 2.38" not including the mating connectors. Refer to Figure 2 for individual module dimensions.

Finish

The finish is nickel plate.

Weight

Power supply PX-628, 50 grams (1.76 oz.) maximum. All other modules, 25 grams (0.88 oz.) maximum.

Connectors

A connector with insulated wire leads is provided with each module having an external connector. The connectors are Cannon Microminiature MDM series. The model numbers used with this system are MDM-9P, MDM-15P and MDM-37P. Screwlock assemblies are also provided to secure the connectors to the PCM stack.

Mounting

The system can be mounted in any one of two planes, connectors facing upward or sideways. The mounting screws are #4-40 socket head screws and are supplied with each system. Due to varying EPROM dimensions, clearance in the end plate should be checked.

Stacking

The stacking screws are #2-56 pan head screws supplied uncut and then custom cut to satisfy the stack length of the specific systems. For stacks containing eight or more modules, a spacer pallet or shim tape should be used. For detailed instructions on building up a stack, refer to the section covering system configuration and testing.

ENVIRONMENTAL SPECIFICATIONS

Operating Temperature

The operating temperature will be between -35 degrees Centigrade and +85 degrees Centigrade.

Storage Temperature

The storage temperature will be between -54 degrees Centigrade and +100 degrees Centigrade.

Humidity

The tolerable range is 0 to 95 percent relative humidity.

Altitude

Unlimited.

Shock

Tolerable shock is 100 G peak half sine wave for 11 milliseconds in each of the three major axes.

Acceleration

Tolerable acceleration is 100 G steady state for one minute in each of the three major axes.

Random Vibration

Tolerable vibration is 29.3 G rms at 20 to 2,000 Hz.

Electromagnetic Interference

The electromagnetic interference tolerance complies with MIL-STD-461A and 462.

DETAILED DESCRIPTION OF THE PCM ENCODER SYSTEM

Group I and II Modules

The Group I modules consist of the following:

PX-628	Power Supply	P/N 17028000-501	
TM-615P	Timer	P/N 17015001-515	280 KHz premod. filter
		P/N 17015001-516	560 KHz premod. filter
		P/N 17015001-519	No premod. filter
PR-614	Processor	P/N 17014003-501	
EP-612	End Plate	(Part of PR-614)	
FM-618	Formatter	P/N 17018000-519	

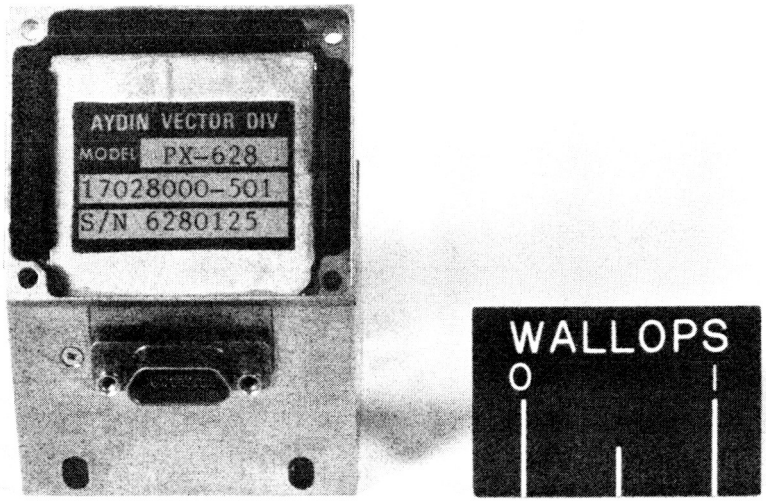


Figure 6.-Power supply module PX-628

PX-628 Power Supply

The power supply module (Figure 6) accepts +28 volts dc as nominal power input and supplies the entire system with the regulated voltages required. The basic system oscillator is also included in the power supply module. Three programming pins located at the external connector of this module allow for the selection of one of eight system bit rates. Programming is accomplished by grounding appropriate pins or by means of a logic interface. An open programming pin is interpreted as a logic "1". The programming pins are pulled up to +10.0 volts through 10 kilohm resistors. The bit rates selectable are 800, 400, 200, 100, 50, 25, 12.5 and 6.25 kilobits per second. Also provided at the external connector of the power supply module are seven bit clock outputs. The frequencies available are 1600, 800, 400, 200, 100, 50 and 25 kilobits per second. These bit clock outputs are 0 to +5.0 volts pulse trains and are CMOS or low power TTL compatible.

The power supply also allows for the use of an external clock. This capability will allow system bit rate to reach 1.0 megabit per second. When an external clock is used, the PX-628 should be programmed to the closest comparable bit rate. If transitions supplied by the external clock should fail, the system will revert to the internal clock selected by the program at the external connector. When an external clock is not used, it is recommended that the external clock input pin be grounded to reduce chances of noise being introduced into the system. For best performance the external clock should be between 1.6 and 3.2 MHz. The external clock must be

referenced to signal ground. The duty cycle of the external clock must be 50 percent ±2 percent. If the external clock input pulses are too narrow, the transitions may not be detected. The symmetry of the bi-phase outputs is dependent on the duty cycle of the 2X bit clock which is the same as the external clock when program A, B, and C are grounded.

When using the system, it is important to heat sink the power supply and the entire stack. The current drain depends on the exact configuration of the system but is typically in the range 250 to 500 mA maximum.

PX-628 Specifications

Power Input.-Nominal input of +28 volts ±4 volts dc is accepted by the power supply module.

Reverse Polarity Protection.-A continuous supply of -32 volts dc applied to the power input pin will not cause permanent damage to the system.

System Grounding.-The signal, power and chassis grounds are all mutually isolated. For most systems it is desirable to use a common reference for all of the system grounds.

Maximum Current Drain.-500 mA maximum.

Bit Rate Stability.-The internal system clock will have a stability of ±0.02 percent. The stability when using an external clock will follow the stability of the external clock used. For definition of this specification refer to IRIG document number IRIG 106-77, sections 4.3.1 and 4.3.2.

External Clock Input.-The external clock input is a 0 to +10.0 volt input. This input will not operate on a 0 to +5.0 volt input. The 2X bit clock output on the TM-615P module is a 0 to +10.0 volt output and can be used to run multiple systems synchronously using the external clock input.

PX-628 Programming.-"0" = grounded pin, "1" = open pin.

TABLE 2. BIT RATE PROGRAMMING CODES

Program A Pin 15	Program B Pin 14	Program C Pin 13	Bit Rate Kbit/sec
0	0	0	800
1	0	0	400
0	1	0	200
1	1	0	100
0	0	1	50
1	0	1	25
0	1	1	12.5
1	1	1	6.25

External Clock Frequencies.-The application of external clock frequencies which are outside the below recommendations will not damage the power supply module. However, degradation of analog accuracy and/or bit rate stability may occur. This is a 0 to +10.0 volt input and will not operate on 0 to +5.0 volts.

TABLE 3. EXTERNAL CLOCK FREQUENCIES

	Bit Rate Program							
Prog A	0	1	0	1	0	1	0	1
Prog B	0	0	1	1	0	0	1	1
Prog C	0	0	0	0	1	1	1	1
Word Length	External Clock Frequencies (In MHz)							
8 Bits/Word	1.2 to 2.0	1.2 to 3.2	→					
9 Bits/Word	1.4 to 2.0	1.4 to 3.2	→					
10 Bits/Word	1.6 to 2.0	1.6 to 3.2	→					
Resulting bit rate expressed as fraction of external clock	1/2	1/4	1/8	1/16	1/32	1/64	1/128	1/256

PX-628 Test Outputs.-Bit rate clocks are available at the external connector of the power supply module. The outputs are CMOS or low power TTL compatible and operate at 0 to +5.0 volts dc.

TABLE 4. POWER SUPPLY TEST OUTPUTS

Output	Pin No.	Output IC Type
25 Kbit/s Clock	7	RCA 4050
50 Kbit/s Clock	3	RCA 4050
100 Kbit/s Clock	4	RCA 4050
200 Kbit/s Clock	6	RCA 4050
400 Kbit/s Clock	5	RCA 4050
800 Kbit/s Clock	1	RCA 4050
1600 Kbit/s Clock	2	RCA 4050

PR-614 Processor

The processor module (Figure 7) contains the control circuit. The PR-614 executes the software program entered into the EPROM and controls the timing and operation of the entire system. There is no external connector on this module. For a detailed description of this module, refer to the section on processor control.

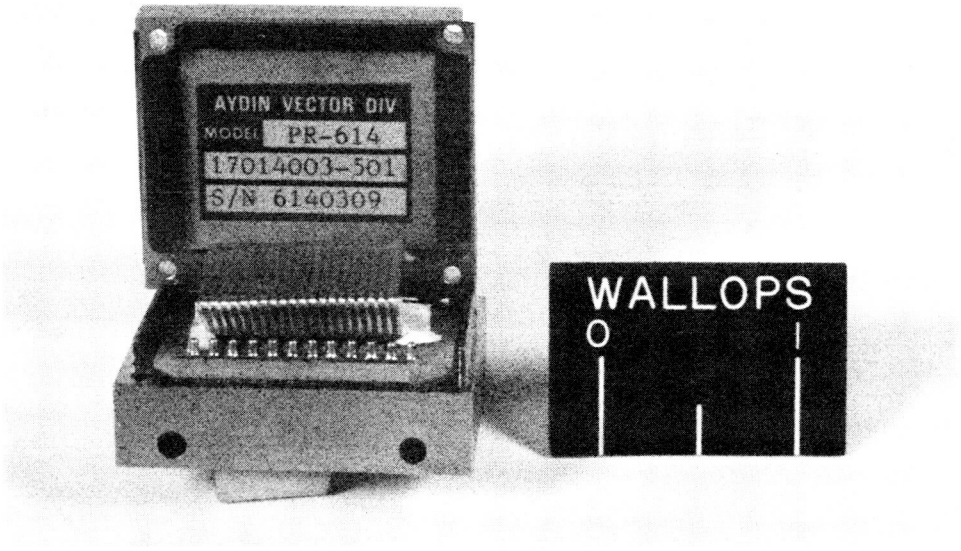


Figure 7.-Processor and end plate modules (PR-614 and EP-612)

EP-612 End Plate

The end plate (Figure 7) terminates the stack on the end opposite the power supply and contains the 9702A EPROM. Four screws secure the EPROM access lid. One EPROM is supplied with each system and is not soldered into its socket. The EPROM can be removed for programming and reprogramming. There is no external connector on this module.

TM-615P Timer

Several system functions must be selected at the timer module (Figure 8). The programming is accomplished by grounding appropriate pins on the modules external connector. A logic interface can also be used to control the state of the programming pins. A positive logic system is used and an ungrounded programming pin will be

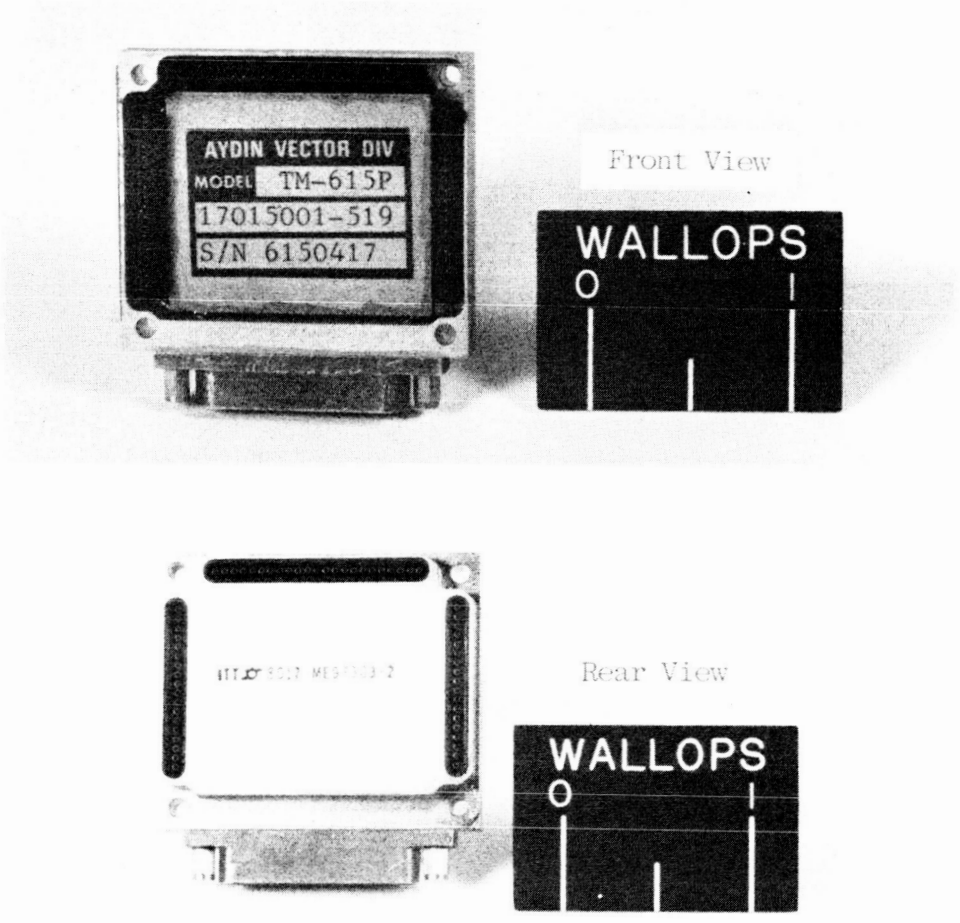


Figure 8.-TM-615P timer

interpreted as a logic "1". The programming inputs are pulled up to 10 volts through 30 kilohm resistors. The programmable parameters are number of bits per word, sample settling time, parity select and output code. The number of bits per word selectable are 8, 9, or 10 bits per word. All words within the system will be the same length. The counter module and the serial digital data module also require word length programming if used. The sample settling time is programmable for the analog channels. (See Table 9 for more information.) The parity option provides odd or no parity. The use of the odd parity option is not recommended above bit rates of 100 kilobit per second. The two fixed output codes available are Bi-Φ-L and NRZ-L. The output codes selectable by programming are Bi-Φ-M, Bi-Φ-S, NRZ-M and NRZ-S. (For more information on the output codes, see Figure 9.)

Some timer modules contain a single premodulation filter. This is a low pass linear phase filter with a roll-off of -36dB per octave minimum past the -3dB corner frequency. To use the premod filter, connect the desired coded output (pin 1, 2, 4, 6 or 20) to the filter input (pin 7). The filtered PCM serial bit stream will then be available at the filter output (pin 8). The recommended -3dB fco points are:

0.7 x bit rate = -3dB point for NRZ coding
1.4 x bit rate = -3dB point for Bi-Φ coding

Timer module, P/N 17015001-515, contains a premod filter with the -3dB point at 280 KHz. The output is two volts peak-to-peak centered about 0.0 volt. Timer module, P/N 17015001-516, contains a premod filter with the -3dB point at 560 KHz. The output of this filter is four volts peak-to-peak centered about 0.0 volt. The output impedance of these premod filters is less than 10 ohms. Timer modules, P/N 17015001-519, do not contain premod filters.

Other outputs are also available at the timer's external connector. These additional outputs are a normal and inverted 2X bit clock, a normal and inverted bit clock, word clock, minor and major frame sync and the invert of the programmed coded output. The 2X bit clock outputs are 0 to +10.0 volt outputs and can be used to run additional MMP-600 systems synchronously using the external clock input. A general description of system timing relationships is shown in Figure 10.

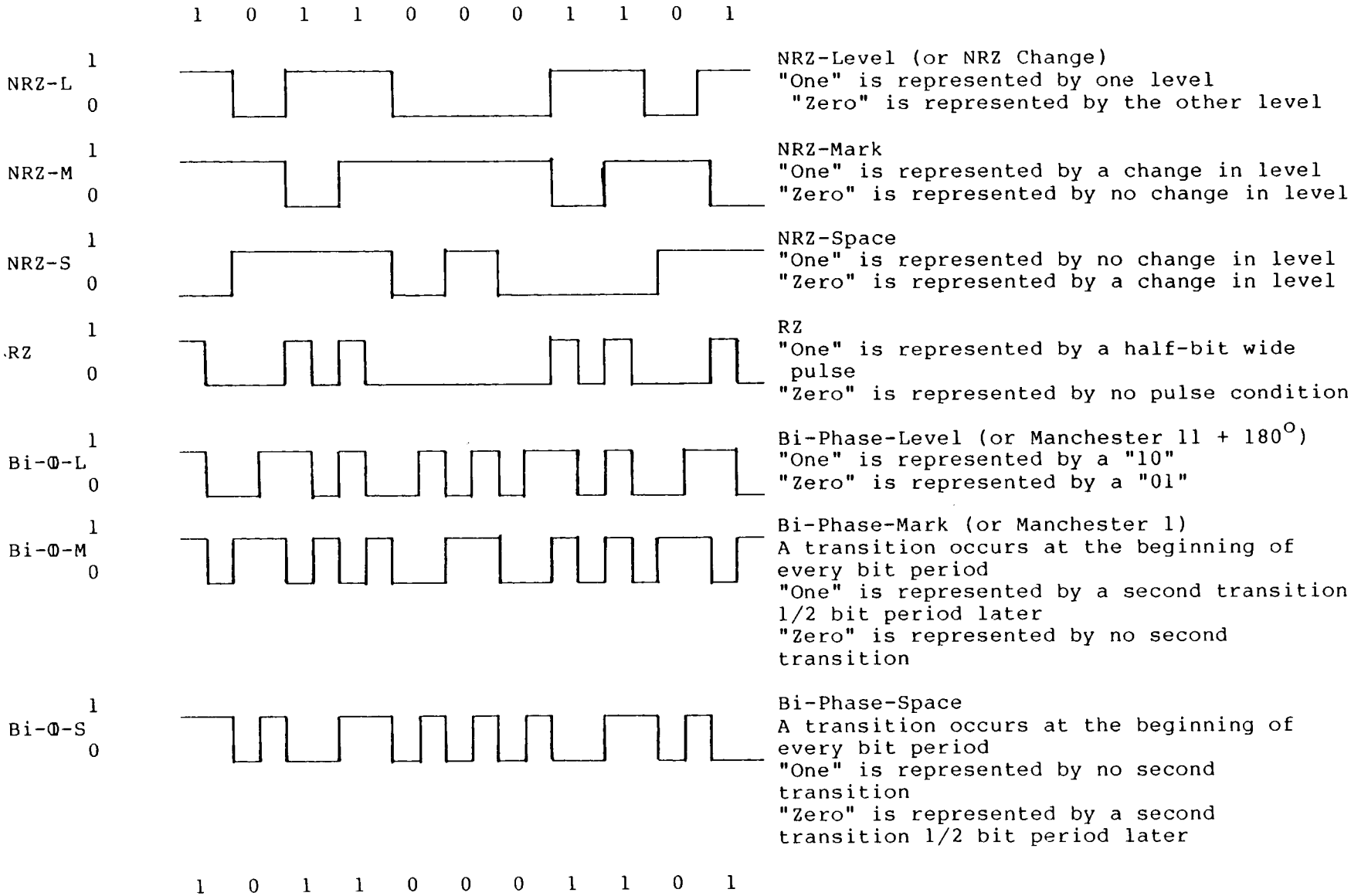
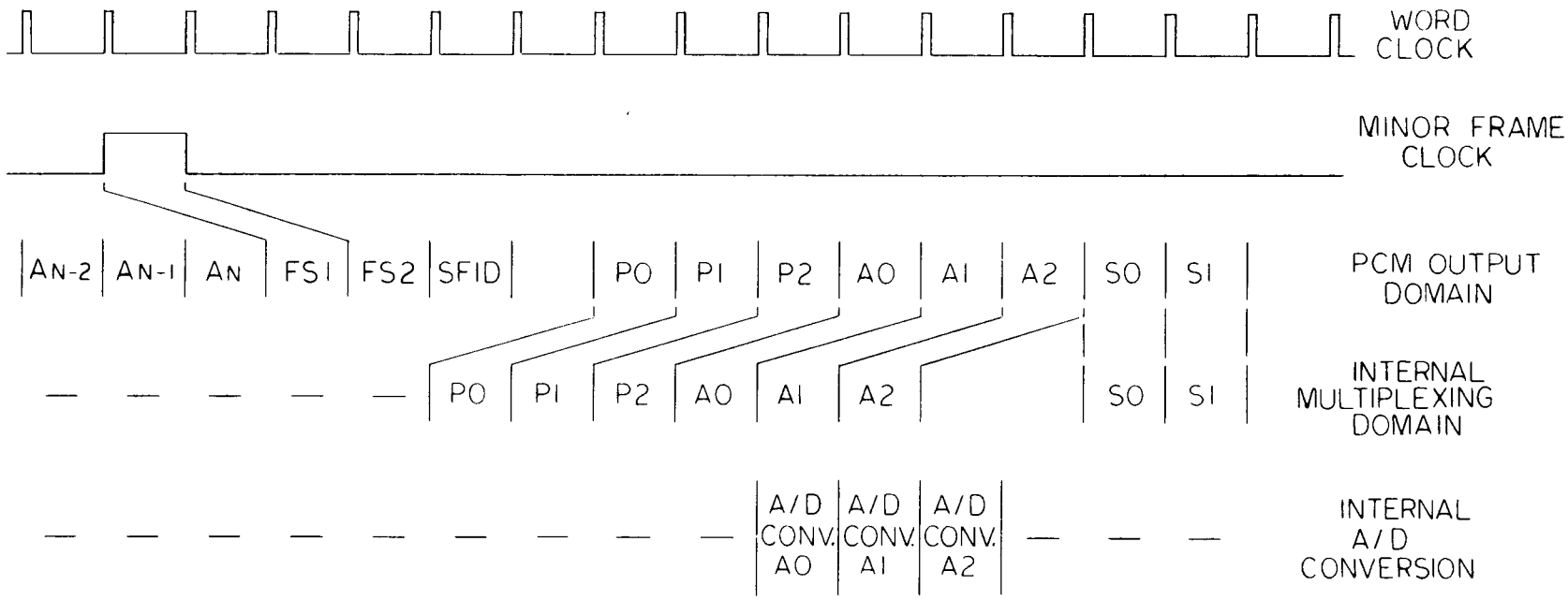


Figure 9.-PCM waveforms



AN = ANALOG WORD, NUMBER N
FS = FRAME SYNCHRONIZATION WORD
SFID = SUBFRAME IDENTIFICATION COUNTER WORD
P = PARALLEL DIGITAL DATA WORD
S = SERIAL DIGITAL DATA WORD

Figure 10.-System timing diagram

TABLE 5. TM-615P INPUTS

Description	Pin Number(s)	Input to IC Type
Bi-Ø/NRZ select	3	RCA 4030 & 4081
Premod filter input	7	RCA 4049
Word length programming pins	12,13,14,15	RCA 4029
Sample duration programming pins	16,17,18	RCA 4063
Mark/space select	22	RCA 4030

TABLE 6. TM-615P OUTPUTS

Description	Pin Number(s)	Output from IC Type
NRZ-L output	1	RCA 4049
Bi-Ø-L output	2	RCA 4049
NRZ-L primary output	4	RCA 4050
Major frame sync	5	RCA 4050
Bi-Ø-L primary output	6	RCA 4050
Premod filter output	8	CF 2515
Inverted 2X bit clock	9 (0 to +10.0 V)	RCA 4041
2X bit clock	10 (0 to +10.0 V)	RCA 4041
Bi-Ø/NRZ, mark/space coded output	20	RCA 4049
Inverted Bi-Ø/NRZ mark/space coded output	21	RCA 4049
Inverted bit clock	23	RCA 4049
Minor frame sync	24	RCA 4050
Word clock	25	RCA 4050
Bit clock	26	RCA 4050

All outputs except the 2X bit clocks are CMOS or low power TTL compatible and operate within the 0.0 to +5.0 volt dc range.

TABLE 7. BITS PER WORD TM-615P PROGRAMMING CODES

	Programming Pins			
Bits/Word	B4 (pin 14)	B3 (pin 12)	B2 (pin 13)	B1 (pin 15)
8	0	1	1	1
9	1	0	0	0
10	1	0	0	1

TABLE 8. PARITY SELECT TM-615P PROGRAMMING CODES

Parity Select	Pin Number 11
Odd parity*	1
No parity	0

*The use of the odd parity option is not recommended above bit rates of 100 kilobit per second.

These programming codes are to be used at the external connector of the module. "0" = grounded pin; "1" = open programming pin.

The sample duration feature allows for maximum sample settling time. It is very important to insure against an overlap in the analog sampling and digitization periods within the analog to digital converter. Significant error would result if this overlap were allowed to occur. The recommended sample duration times follow:

Bits/Word	Sample Width
8	$2\frac{1}{2}$ bits
9	$3\frac{1}{2}$ bits
10	$3\frac{1}{2}$ bits

TABLE 9. SAMPLE DURATION PROGRAMMING CODES

Sample Duration	Programming Pins S3 (pin 17)	S2 (pin 16)	S1 (pin 18)
1½ bits	0	0	1
2½ bits	0	1	0
3½ bits	0	1	1
4½ bits	1	0	0
5½ bits	1	0	1

TABLE 10. CODED OUTPUT PROGRAMMING CODES

Coded Output	Bi-Φ/NRZ Select (pin 3)	Mark/Space Select (pin 22)
Bi-Φ-M	0	0
Bi-Φ-S	0	1
NRZ-M	1	0
NRZ-S	1	1

The TM-615P is the only module that has an output other than 0 to +5.0 volts dc CMOS or low power TTL compatible. The 2X bit clock and the inverted 2X bit clock found on pins 9 and 10 of the external connector of this module are 0 to +10.0 volts dc outputs. These 2X bit clock outputs are of limited drive capability and should not be used into less than 1000 ohms.

Formatter FM-618

The formatter module (Figure 11) merges digitized data with frame synchronization words and performs parallel to serial conversion as necessary. The output of the formatter module is sent to the timer module. The formatter must be located directly under the quad filter module if the quad filter module, FL-619A, is used in the system. The formatter module has a recess in the side of the module wall to enable the user to access the adjustment potentiometer on the quad filter module. No external connector exists on the formatter module.

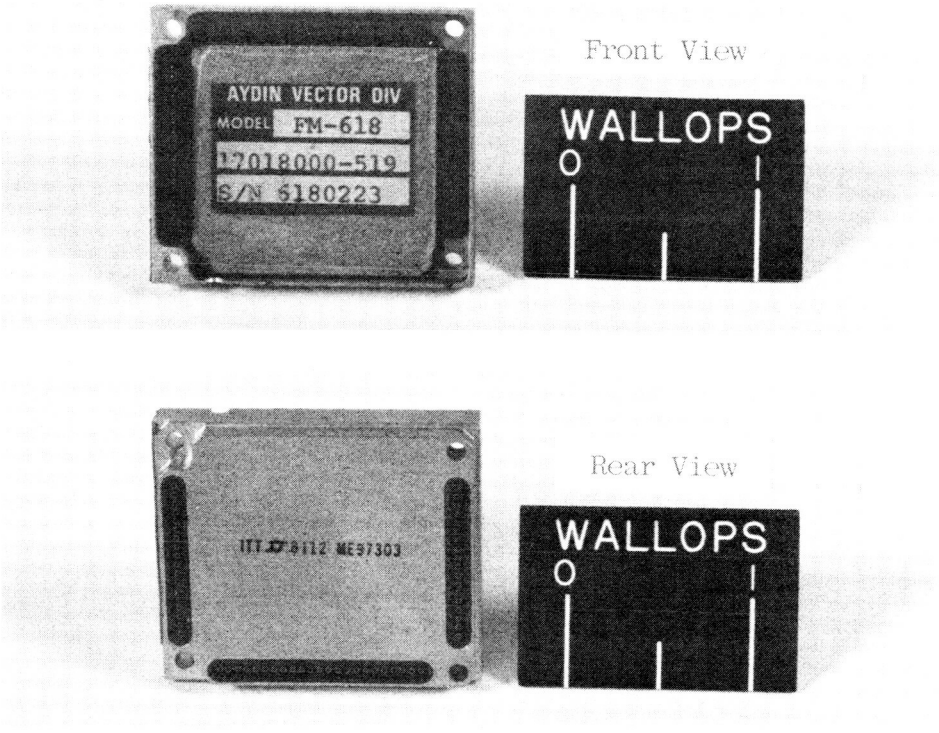


Figure 11.-Formatter FM-618

The Group II modules consist of the following:

AD-606	Sample and Hold Amplifier and Analog to Digital Converter	P/N 17006003-501
MP-601L	32 Channel High Level Analog Multiplexer	P/N 17001004-510
PD-629	30 Input Parallel Digital Data Multiplexer with two enables	P/N 17029000-501
SD-624	Serial Digital Data Multiplexer with eight inputs	P/N 17024003-501
CM-622P	Dual Counter/Accumulator	P/N 17022003-503
TA-623	Time Event Monitor with Alternating Registers	P/N 17023000-501
TB-625	Time Event Monitor with Timing Buffers	P/N 17025000-501
FL-619A	Quad Filter Module with Adjustable Output	P/N 17019001-515 (1120, 280, 70, 17.5)KHz fco P/N 17019001-516 (560, 140, 35, 8.8)KHz fco

Group II modules are input multiplexers with the exception of the analog to digital converter, which must be included in systems using analog input channels and the quad filter module, which contains four premodulation filters. Group II modules can be used in variable combinations to satisfy system requirements.

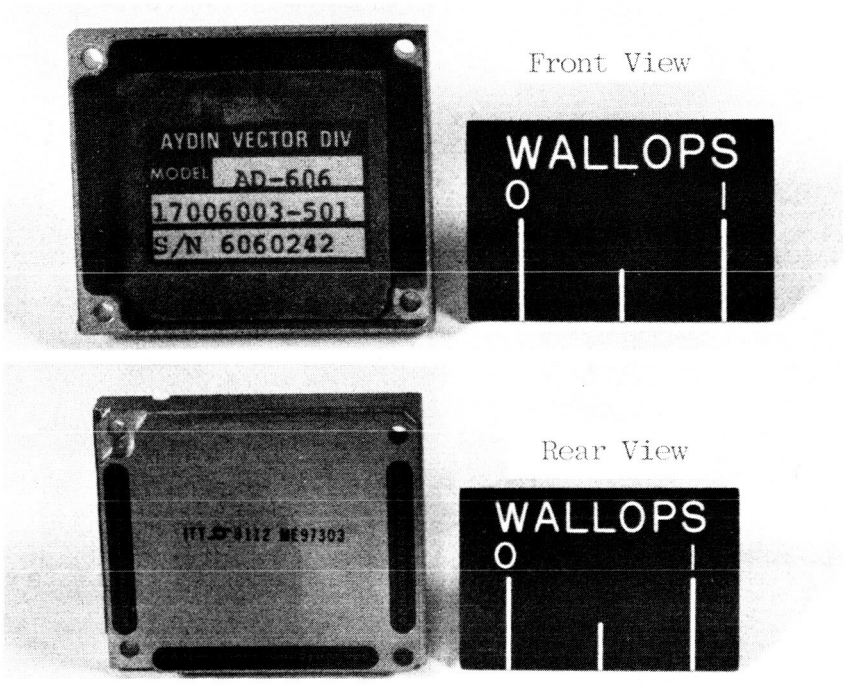


Figure 12.-Sample and hold amplifier and analog to digital converter, AD-606.

AD-606 Sample and Hold Amplifier and Analog to Digital Converter

The AD-606 module (Figure 12) includes a sample and hold amplifier which performs several functions. The sample amplifier provides a high input impedance to the PAM bus (greater than 10 megaohms). The hold amplifier provides a narrow aperture time which minimizes error in ground data processing. Channel-to-channel crosstalk is minimized through the use of a sampling capacitor which has a very low dielectric absorption characteristic. Lastly, the hold amplifier provides a low output impedance to the analog to digital conversion circuit.

The settling time for the hold amplifier is programmable at the timer module for $1\frac{1}{2}$, $2\frac{1}{2}$, $3\frac{1}{2}$, $4\frac{1}{2}$, and $5\frac{1}{2}$ bit periods. This flexibility is provided to gain maximum data settling time and to insure that the hold amplifier settling period and the digitization period do not overlap. Digitization takes place during the first

portion of the following word period, during which the data is being held at a stable level.

The analog to digital converter digitizes each analog signal into a ten-bit binary number by method of successive approximations. The current switching technique employed by this A/D method is suited to high speed conversions. Digitization is performed at a fixed rate of approximately 1.6 MHz, generated by an internal clock. This internal clock is synchronized with the power supply inverter to prevent inverter noise from entering into the data at the latching of the hold amplifier.

The AD-606 does not have an external connector and therefore no programming can be done at this module. Programming at the timer module controls the hold amplifier settling time and recommended settling times follow in tabular form. (Refer to Figure 13 for a graphical representation of the A/D conversion timing.)

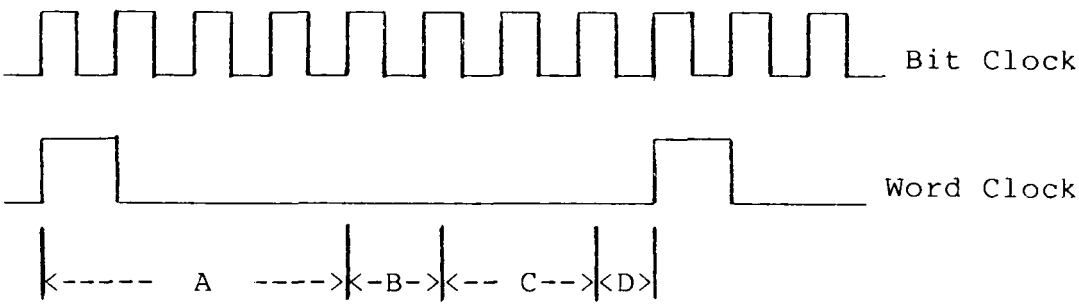


Figure 13.-AD-606 timing diagram

In Figure 13, above, the two functions that take place in time period A are: channel N data multiplexer settling and digitization of channel (N - 1) data. Time period A is a fixed duration of 5.0 microseconds. Time period B is used to allow switch noise settling time. At the leading edge of this period, the analog switch (Figure 14) completes the circuit to the hold amplifier. Time period B must be no less than one microsecond. Time period A and D are constant, therefore, time period B is residual of the word time minus time periods A, C, and D. Time period C allows for channel N data to settle in the hold amplifier. This time period is of programmable duration. See TM-615 timer module section for programming instructions. Time period D is used to allow switch noise settling time. At the leading edge of this period, the analog switch breaks the circuit to the hold amplifier and the hold

amplifier is then latched on channel N data. Time period D is a fixed length of one half bit period.

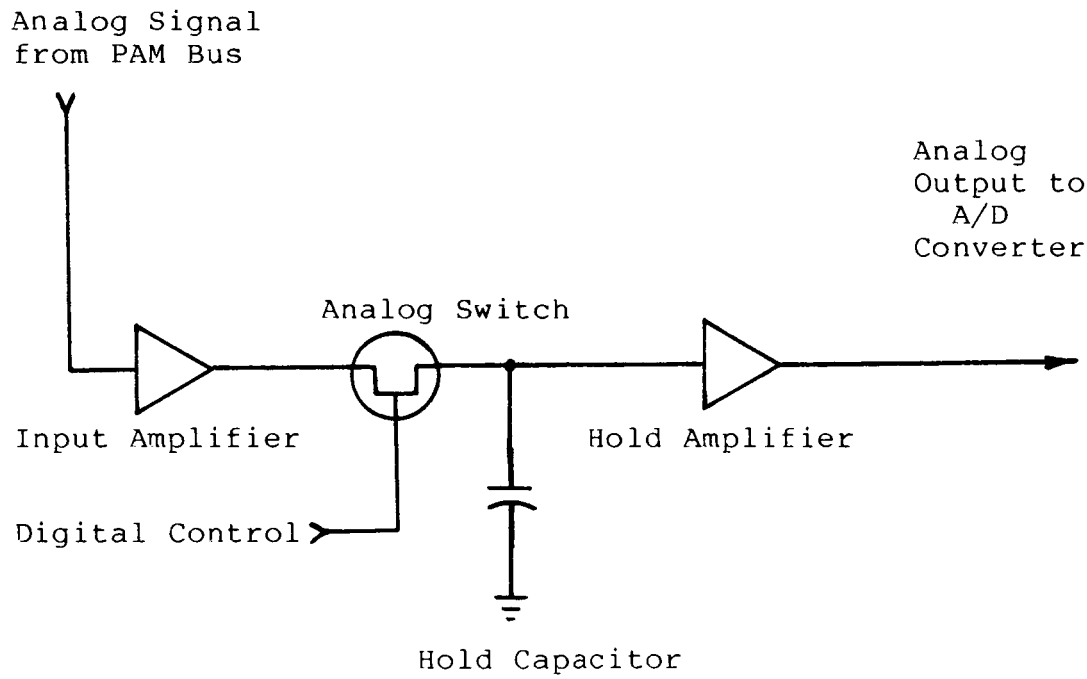


Figure 14.-Typical sample and hold amplifier circuit

AD-606 Specifications

Accuracy.-The accuracy of the analog to digital conversion process is $\pm\frac{1}{2}$ of the LSB.

Conversion Method.-The conversion process is by method of successive approximations.

Number of Bits.-Ten.

Ideal Bit Weight.-Ideal bit weight (IBW) equals full scale input (+5.0 volts)/1000 equals 5 millivolts/bit.

Coding.-The coding of the A/D module is offset binary as follows:

Input	Binary Output	Decimal Equivalent
+5 volts full scale	1111110100	1012
+0 volt zero scale	0000001100	12

Sample Settling Time.-This parameter is programmable at the external connector of the timer module, TM-615P. The selectable sample periods are $1\frac{1}{2}$, $2\frac{1}{2}$, $3\frac{1}{2}$, $4\frac{1}{2}$ and $5\frac{1}{2}$ bit periods. The recommended sample settling times are as follows:

Bits/Word	Sample Width
8	$2\frac{1}{2}$ bits
9	$3\frac{1}{2}$ bits
10	$4\frac{1}{2}$ bits

Elaboration of A/D Conversion Timing.-As an example system, let the following data describe the system of interest:

Word Length: 8 bits/word Bit Rate: 800 Kbit/sec

1 bit period = 1.25 microseconds
1 word period = 10 microseconds

By referring to Figure 13:

Period A = 5.0 microseconds

Period B = 1.0 microsecond

Period C = 2.5 x 1.25 microseconds = 3.125 microseconds
(2.5 bit periods = sample width selected, 1.25 microseconds = 1 bit period)

Period D = 0.625 microsecond ($\frac{1}{2}$ bit period)

Adding A + B + C + D = 9.75 microseconds. By selecting a sample duration time of $2\frac{1}{2}$ bits, the crucial periods within the sample and hold and A/D processes do not overlap. The word period being 10 microseconds in length is left with 0.25 microsecond as a cushion in this worst case example.

MP-601L 32-Channel High Level Analog Multiplexer

The addressing capability of the MP-601L (Figure 15) allows for a maximum of eight analog modules in a single system. This provides 256 analog input channels per system maximum. However, the EPROM size allows for only 240 input channels maximum. The number and selection of active analog channels are determined by the program entered into the EPROM. Programming pins 18, 19 and 36 located on this modules' external connector are used to give each analog module a unique address. (See Table 11 for a detailed address programming.)

Programming is accomplished by grounding appropriate pins or by means of a logic interface. A positive logic system is used and an ungrounded pin will be interpreted as a logic "1". Programming pins are pulled up to +10.0 volts through 10 kilohm resistors.

Input voltage range is 0.0 to +5.0 volts dc (Figure 16). However, each analog multiplexer can withstand overvoltages of ±35 volts dc on every analog input channel. (Over 20 overvoltaged channels per multiplexer are not recommended.)

The word length selections are 8, 9 or 10 bits of resolution. (For 10 bit words, the resolution is one part in 1000.) The word length is programmable at the timer module. For word length programming instructions, refer to the TM-615P section of this report. Systems with word lengths less than 10 bits truncate the LSB's of the 10-bit digitized word from the analog-to-digital converter to meet the required word length. All words in the system will be the same length.

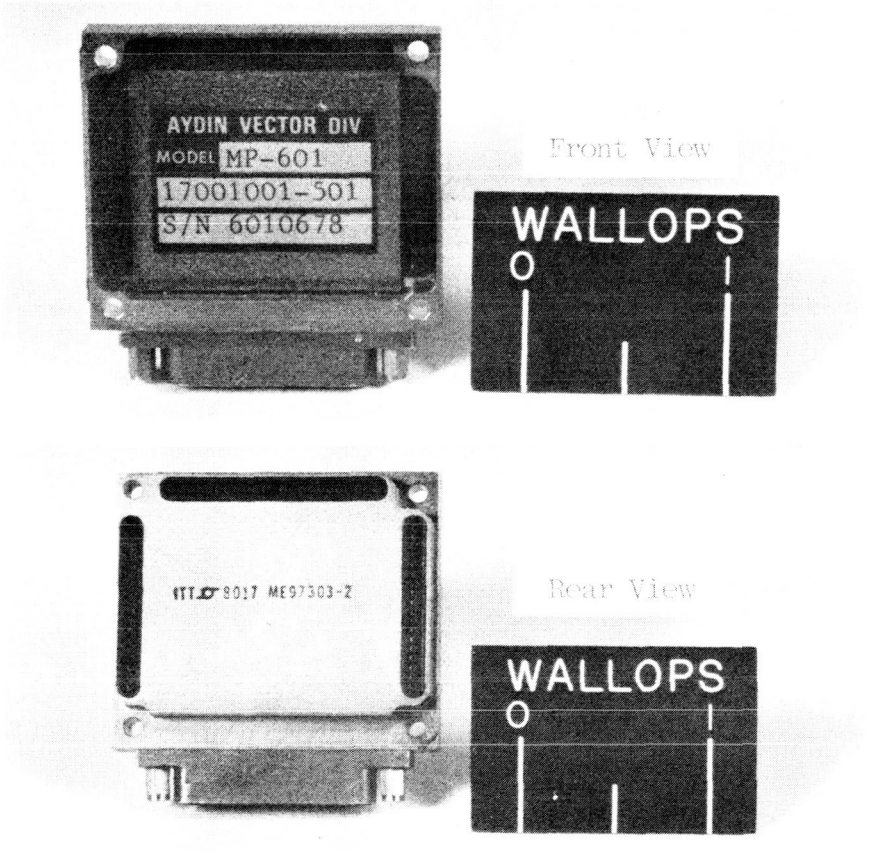


Figure 15.-MP-601L 32-channel high level analog multiplexer

TABLE 11. MP-601L ANALOG MULTIPLEXER CHANNEL PROGRAMMING

Channel No.	Pin No.	A7	A6	A5	A4	A3	A2	A1	A0
0	20	M	M	M	0	0	0	0	0
1	1	M	M	M	0	0	0	0	1
2	2	M	M	M	0	0	0	1	0
3	21	M	M	M	0	0	0	1	1
4	3	M	M	M	0	0	1	0	0
5	22	M	M	M	0	0	1	0	1
6	4	M	M	M	0	0	1	1	0
7	23	M	M	M	0	0	1	1	1
8	24	M	M	M	0	1	0	0	0
9	5	M	M	M	0	1	0	0	1
10	6	M	M	M	0	1	0	1	0
11	25	M	M	M	0	1	0	1	1
12	7	M	M	M	0	1	1	0	0
13	26	M	M	M	0	1	1	0	1
14	8	M	M	M	0	1	1	1	0
15	27	M	M	M	0	1	1	1	1
16	28	M	M	M	1	0	0	0	0
17	9	M	M	M	1	0	0	0	1
18	10	M	M	M	1	0	0	1	0
19	29	M	M	M	1	0	0	1	1
20	11	M	M	M	1	0	1	0	0
21	30	M	M	M	1	0	1	0	1
22	12	M	M	M	1	0	1	1	0
23	31	M	M	M	1	0	1	1	1
24	32	M	M	M	1	1	0	0	0
25	13	M	M	M	1	1	0	0	1
26	14	M	M	M	1	1	0	1	0
27	33	M	M	M	1	1	0	1	1
28	15	M	M	M	1	1	1	0	0
29	34	M	M	M	1	1	1	0	1
30	16	M	M	M	1	1	1	1	0
31	35	M	M	M	1	1	1	1	1

Table 11. (continued)

Address lines A5 - A7 are used to select specific MP-601L modules. Address lines A4 - A0 are used to select specific channels within an analog multiplexer. These programming codes are to be used in the EPROM program.

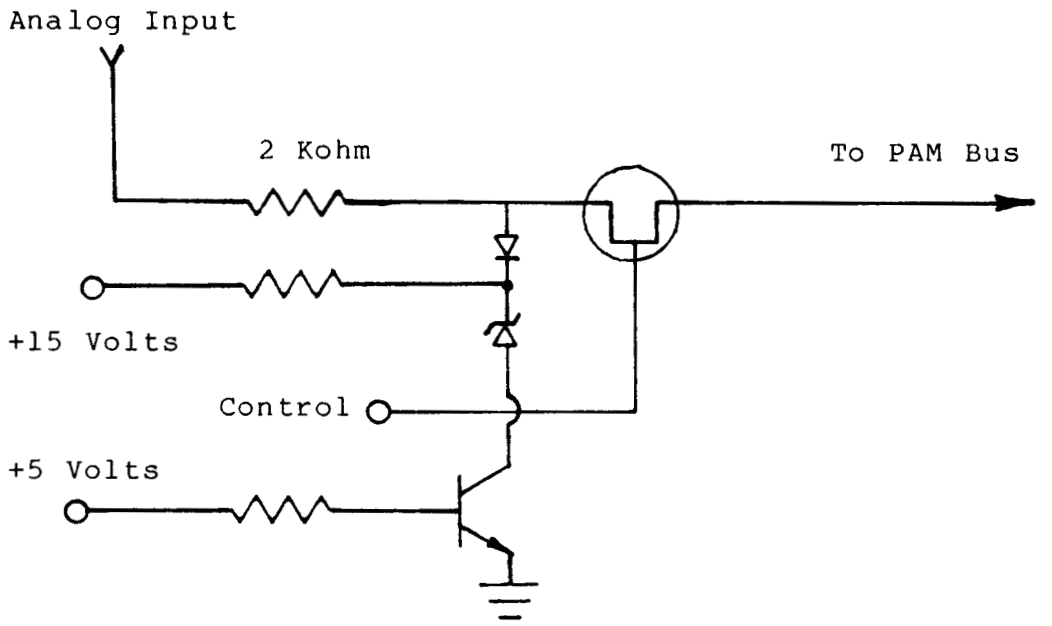


Figure 16.-Typical analog input circuit

The accuracy of the analog system is a function of the source impedance, the number of analog modules in the system, the system bit rate and the number of bits per word. It is therefore recommended to use source impedances of less than 100 ohms to maintain accuracy commensurate with the resolution provided by the number of bits per word. A set of curves follows with conditions exaggerated beyond those found in a typical system to illustrate the effects of source impedance, the number of modules per system, the system bit rate, and the number of bits per word. The system crosstalk error is directly proportional to source impedances, the number of analog modules in the system, and the bit rate. The crosstalk error is inversely proportional to the number of bits per word. The error is due to the time constant of the PAM bus caused by undesirable capacitance.

MP-601L Specifications

Input Voltage.-The input voltage range is 0.0 to +5.0 volts dc. The analog modules can tolerate ±35 volts dc on all analog inputs without causing permanent damage to the module. (It is recommended no more than 20 inputs per multiplexer be over-voltaged simultaneously.)

Coding.-Offset binary coding is used. See the AD-606 section for definition of coding used.

Word Length.-Word lengths of 8, 9 or 10 bits are selectable at the timer module external connector. All words within one system are of equal length.

Input Impedance.-The input impedance will be 10 megaohm with the power on and one megaohm with the power off.

Switch Type.-The switch type used is MOS-FET.

Backcurrent.-The maximum backcurrent will be 500 nA during sampling and non-sampling periods.

Channel-to-Channel Offset.-±5.0 millivolts maximum.

Crosstalk.-For the worst case due to system parameters and configuration is 0.35 percent of full scale maximum. A typical system will have less than 0.1 percent of full scale maximum crosstalk error. (Refer to Figures 17 through 19 to determine the percent error.)

PD-629 30-Input Parallel Digital Data Multiplexer

Each PD-629 module (Figure 20) accepts three parallel digital words of up to ten bits each. Sixteen PD-629 modules can be included in a single system giving a total parallel digital capability of 48 channels (480 bits). The number of active parallel digital channels is determined by the program in the EPROM. The module addresses are assigned by programming pins on the external connector. The programming is accomplished by grounding appropriate pins or by using a logic interface to determine the state of the programming pins. A positive logic system is used. An ungrounded programming pin will be interpreted as a logic "1". Programming pins are pulled up to +10.0 volts through 30 kilohm resistors.

Two of the input channels have an enable pulse associated with them. The enable pulses PDWO and PDW1 are used to signal external circuits that parallel data is

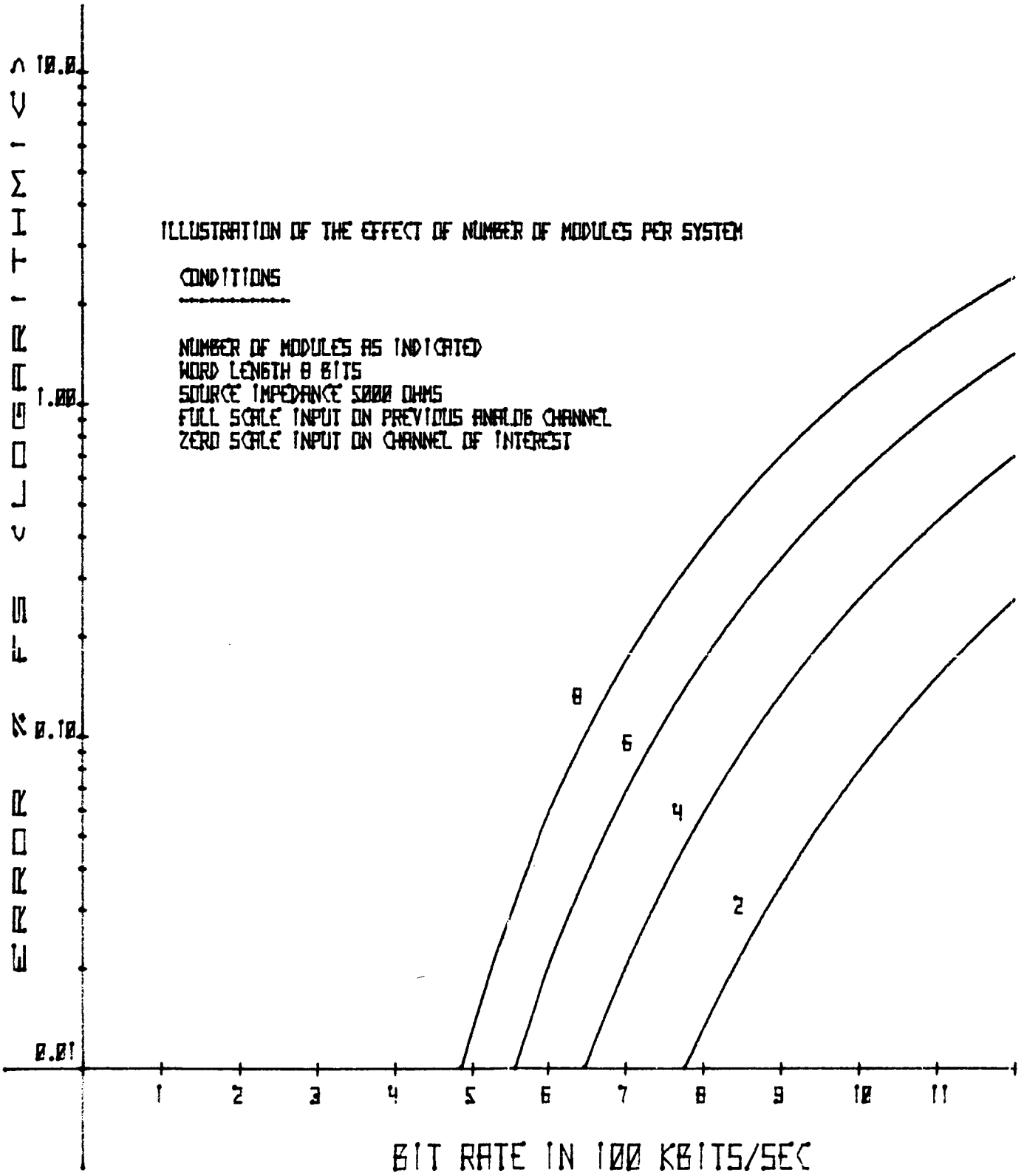


Figure 17.-Analog crosstalk error

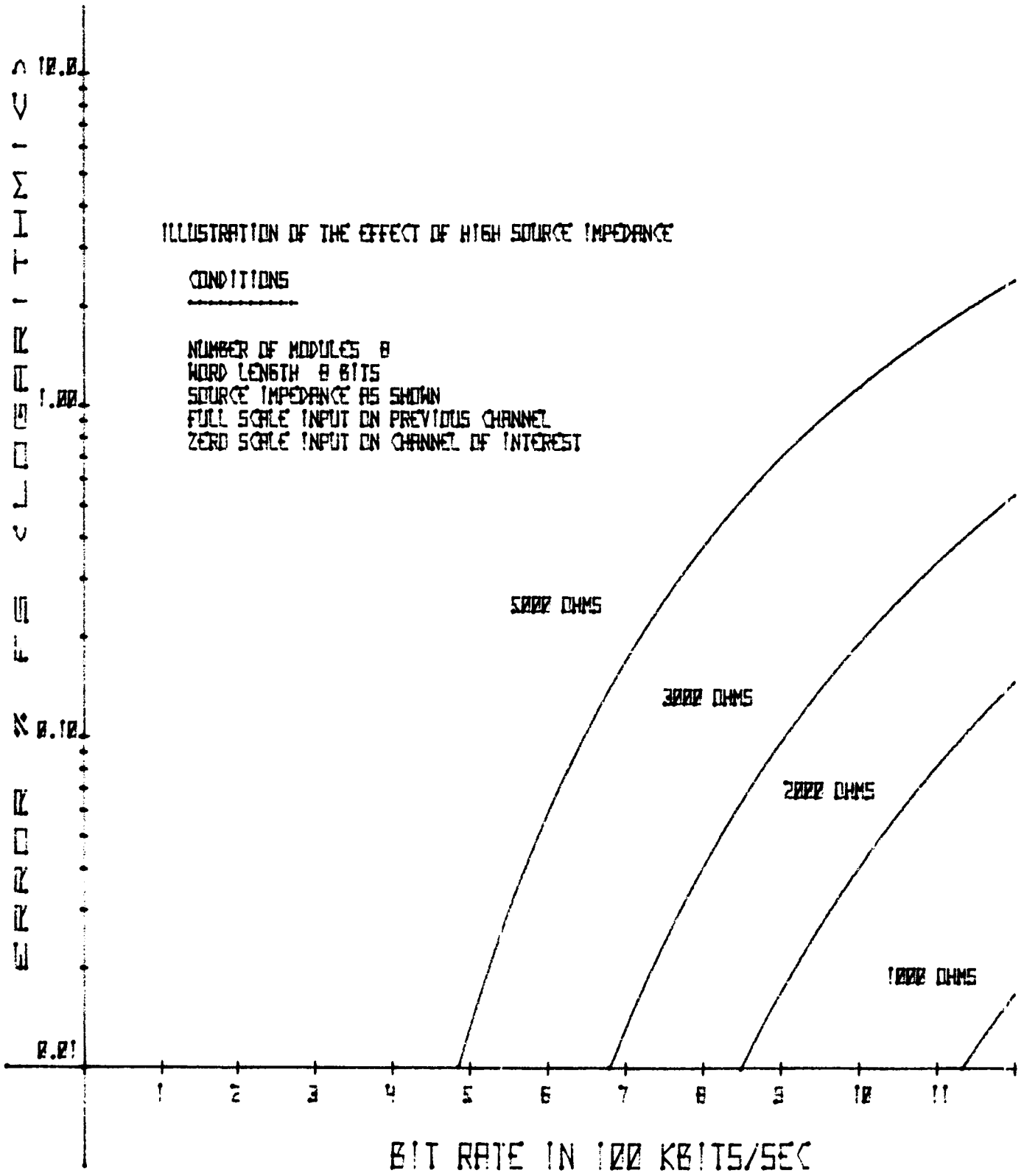


Figure 18.-Analog crosstalk error

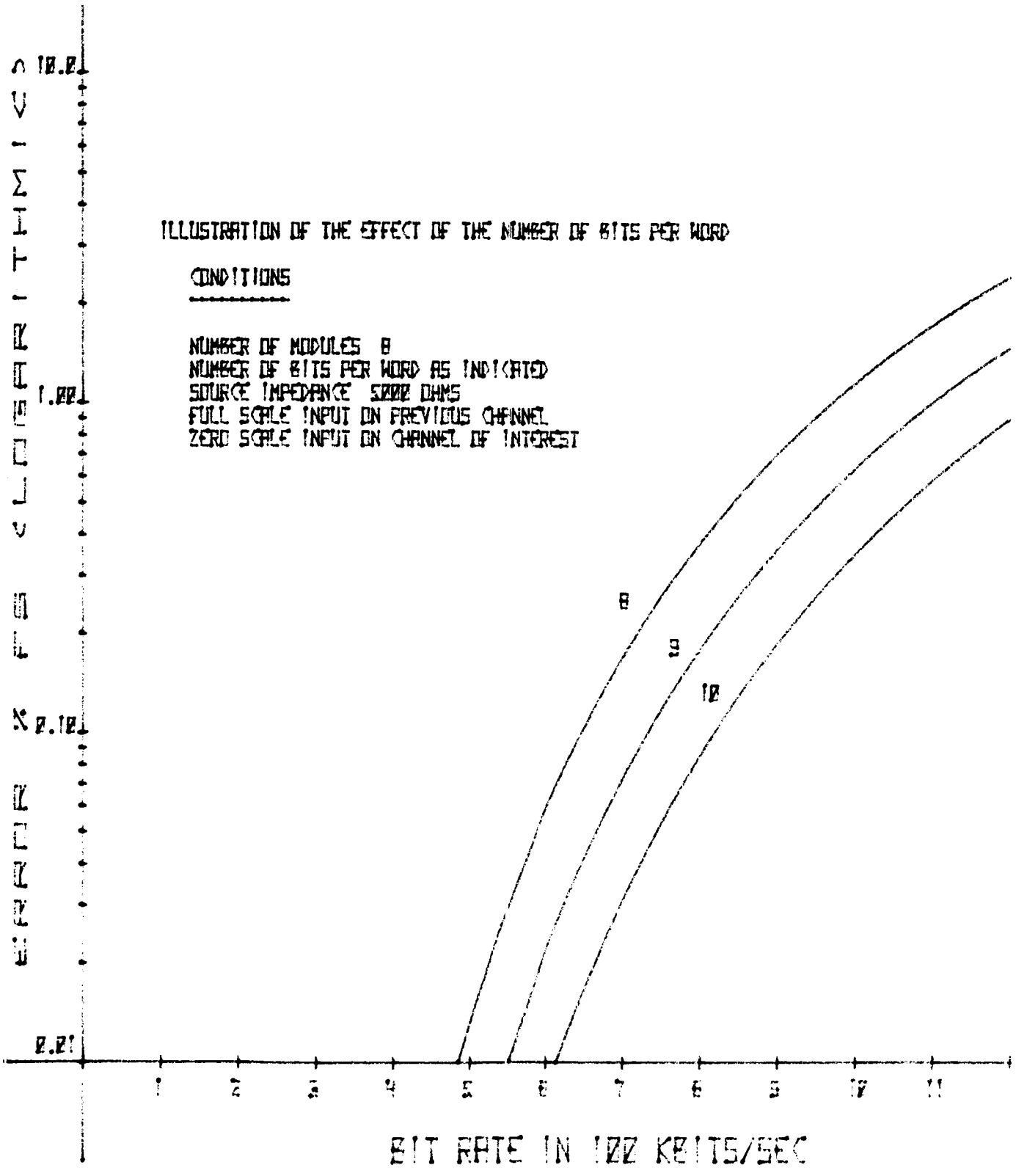


Figure 19.-Analog crosstalk error

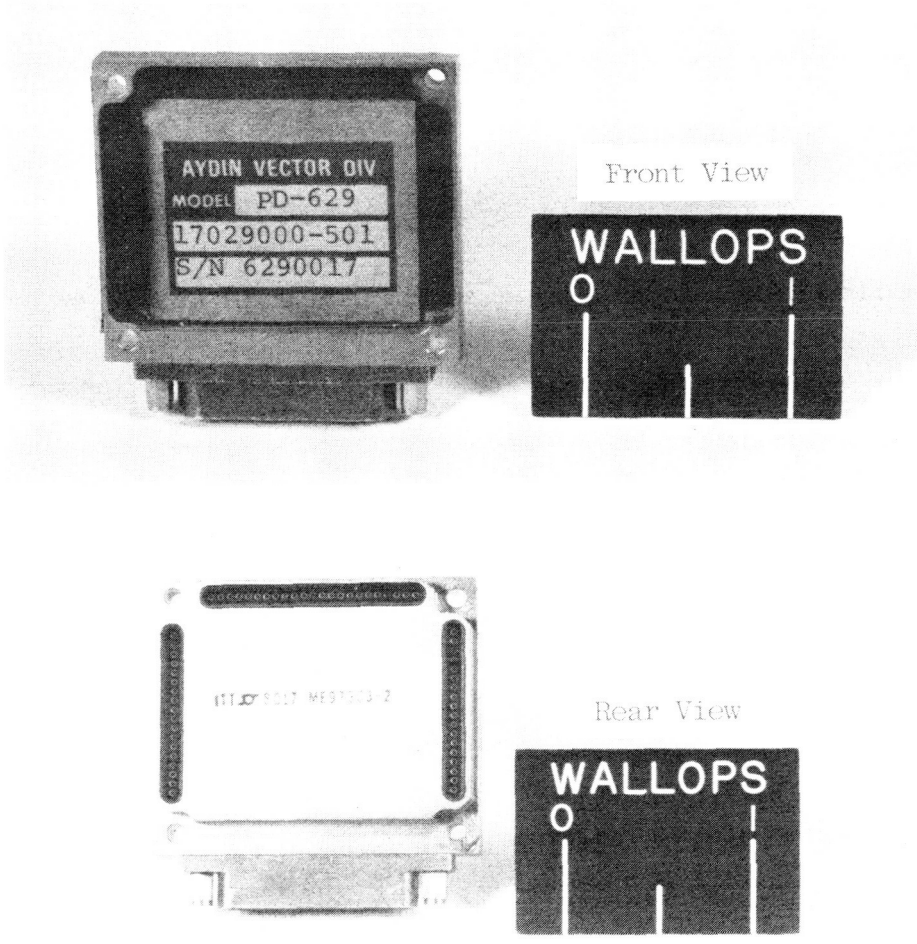


Figure 20.-PD-629 30-Input parallel digital data multiplexer

acceptable at that time. This feature allows for synchronous parallel data transfer; however, data may be entered independent of the enable pulses. See Figure 21 for a timing diagram of the enable pulses.

All bits of a given parallel word are strobed in simultaneously assuring time correlation. The parallel digital module is useful in monitoring any conditions which have only two states; i.e., on or off, yes or no. Up to ten monitors can be incorporated into one data channel using this technique. The parallel digital module is also useful in providing a computer interface.

For 8-bit systems, parallel input bits 8 and 9 are truncated. For 9-bit systems, parallel input bit 9 is truncated. Parallel input bit 0 is the first bit transmitted (FBT) and parallel input bit 9 is the last bit transmitted (LBT).

(The timing diagram, below, depicts the worst case conditions of an 8-bit word and 800 kilobit per second. Decoding spikes may be present on the two enable lines. Therefore, it is recommended that the enables be used in conjunction with the word clock and to trigger interface circuitry with the trailing edge of the gated enable. With increasing word lengths and decreasing bit rates, the data set-up time increases.)

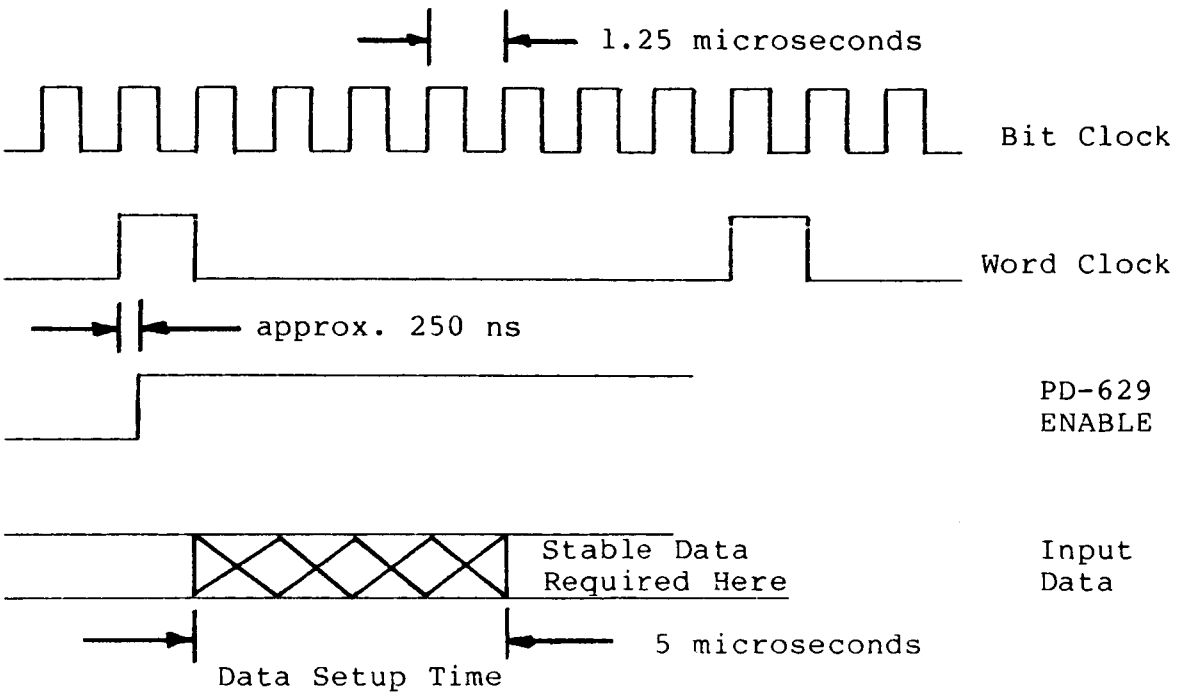


Figure 21.-PD-629 timing diagram

PD-629 Specifications

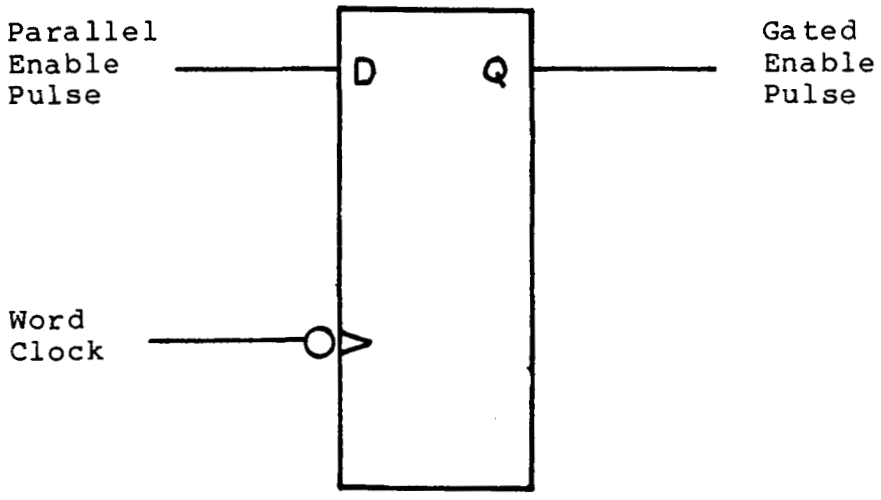
Input Voltage.-Input voltage at -35.0 to +2.0 volts dc is recognized as a logic "0" and +3.0 to +35 volts dc is recognized as a logic "1". An open circuit will be recognized as a logic "0". Voltages outside this range will cause permanent damage to the module.

Input Impedance.-The input impedance to the PD-629 module will be 10 kilohms minimum.

Enable Outputs.-The enable outputs are from RCA 4050's.

The above specifications are boundary conditions and interface circuits should not be designed at the above limits but, rather, designed well within the above tolerances for reliable operation of the system.

The interface circuit that is recommended when the parallel enable pulses are used is depicted in Figure 22. This circuit will suppress any spurious voltage spikes.



CD-4Ø13

Figure 22.-Parallel enable interface circuit

TABLE 12. PD-629 CHANNEL PROGRAMMING CODES

Channel No.	Pin Nos.	A7	A6	A5	A4	A3	A2	A1	A0
0	2,22,5,25,8 28,11,31,14,34	0	0	M	M	M	M	0	0
1	20,3,23,6,26, 9,29,12,32,15	0	0	M	M	M	M	0	1
2	1,21,4,24,7, 27,10,30,13,33	0	0	M	M	M	M	1	0

These programming codes are to be used in the EPROM program. A7 is the MSB and A0 is the LSB. A7 and A6 must always be programmed with a zero when accessing the parallel digital data multiplexers. A5 through A2 are used to address a specific PD-629 module. A1 and A0 are used to select a specific channel within the desired channel within that module.

SD-624 Serial Digital Data Multiplexer

The SD-624 module (Figure 23) accepts eight serial digital input channels. Up to four SD-624 modules can be used in a single system. This gives a maximum of 32 serial digital data channels per system. The duration of each channel sample, the location within the output format, the rate of channel sampling and the number of active channels are all under EPROM program control. Each SD-624 must be assigned a unique module address. The module addresses are assigned by grounding appropriate programming pins in the modules external connector. An open programming pin is interpreted as a logic "1". The module address and word length programming pins are pulled up to +10.0 and +5.0 volts, respectively, through 20 kilohm resistors. For programming codes, see Table 13.

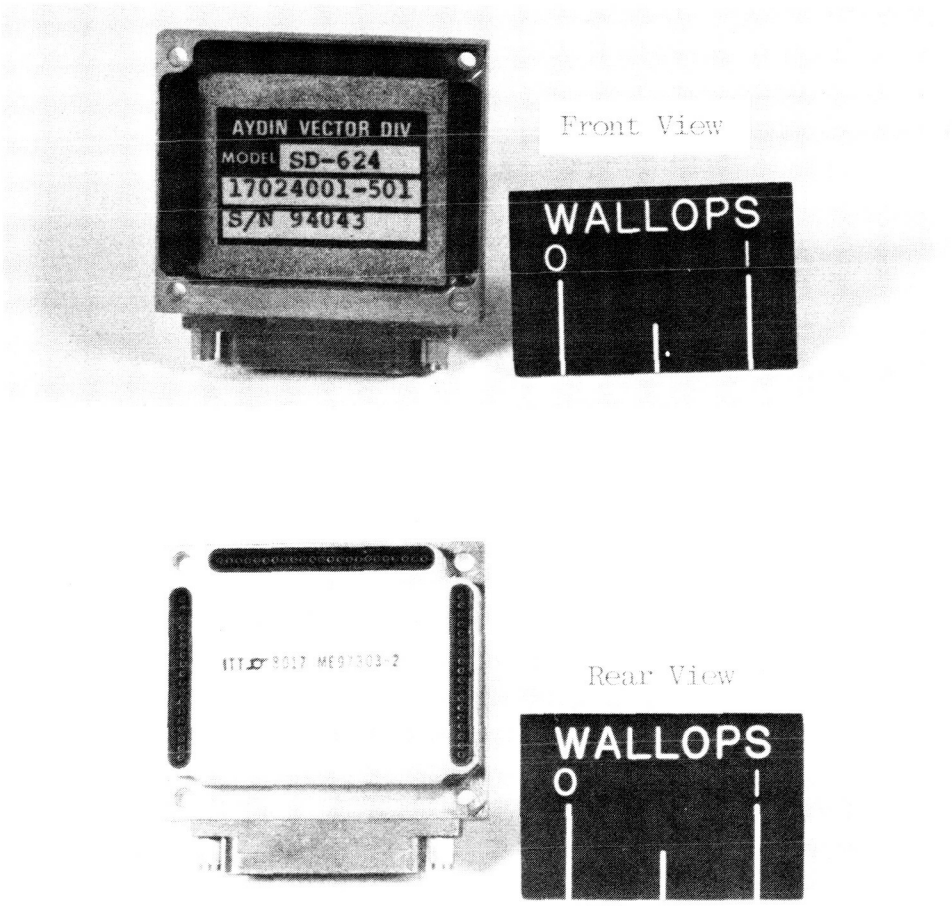


Figure 23.-SD-624 serial digital data multiplexer

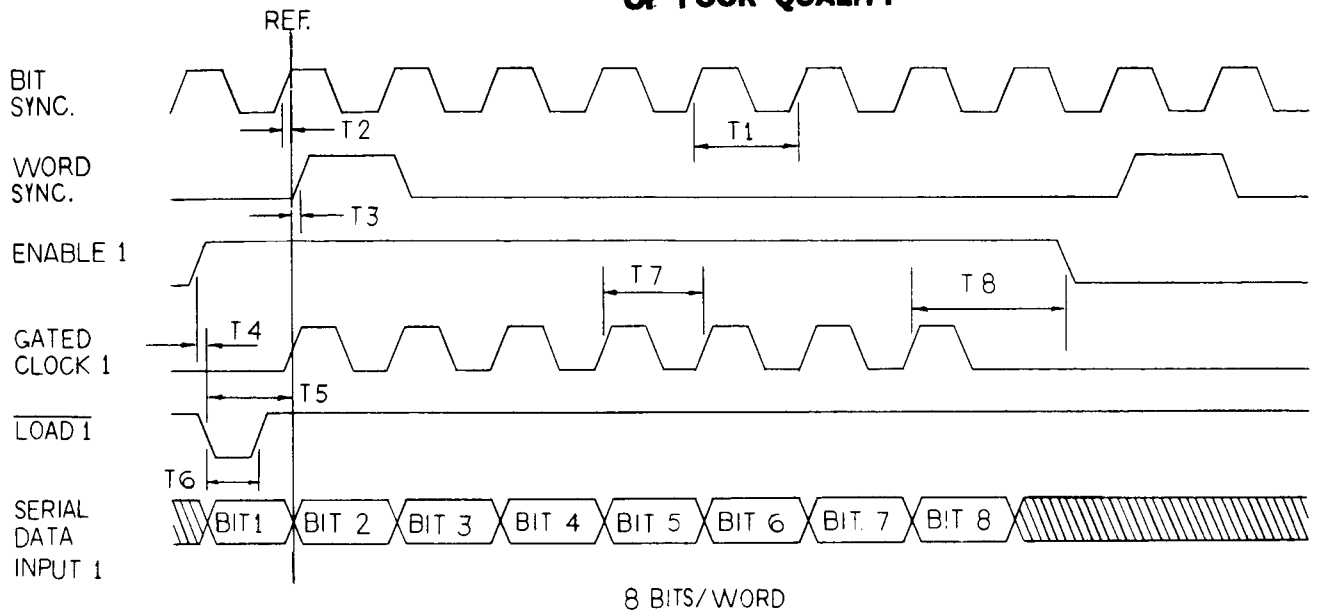
TABLE 13. SD-624 SERIAL DIGITAL DATA MULTIPLEXER CHANNEL PROGRAMMING

Input Channel	Pin No.	A7	A6	A5	A4	A3	A2	A1	A0
0	27	0	0	M	M	X	0	0	0
1	8	0	0	M	M	X	0	0	1
2	26	0	0	M	M	X	0	1	0
3	7	0	0	M	M	X	0	1	1
4	1	0	0	M	M	X	1	0	0
5	20	0	0	M	M	X	1	0	1
6	2	0	0	M	M	X	1	1	0
7	21	0	0	M	M	X	1	1	1

These programming codes are for use in the EPROM program. The "M" denotes address lines reserved for module address programming and the "X" denotes a don't care condition. Address lines A7 and A6 must be programmed with zero when addressing any SD-624 module. A7 represents the MSB and A0 represents the LSB.

The SD-624 is capable of sampling the same input channel in consecutive contiguous words of the PCM output format to accommodate serial digital words of length greater than 10 bits. There is no limit to the number of consecutive words that can be taken of a single serial input channel. The resultant word length will be an integer times the number of bits per word. The word length must be programmed at the external connector of this module if it is less than 10 bits per word. For programming codes, see Table 14.

Associated with each serial digital input are three handshaking signals to aid in data transfer. These signals are 0 to +5.0 volt dc signals and include a gated clock, an enable pulse and an inverted load pulse. The inverted load pulse can be used directly with many common CMOS or low power TTL parallel load serial output shift registers. Upon receiving the inverted load pulse, the MSB must appear at the output of the shift register. The gated clock can then be used directly to shift out the remaining bits. The serial input data must be clocked with the positive going leading edge of the gated clock starting with the first bit of the gated clock. For timing information of these handshaking signals, see Figure 24.

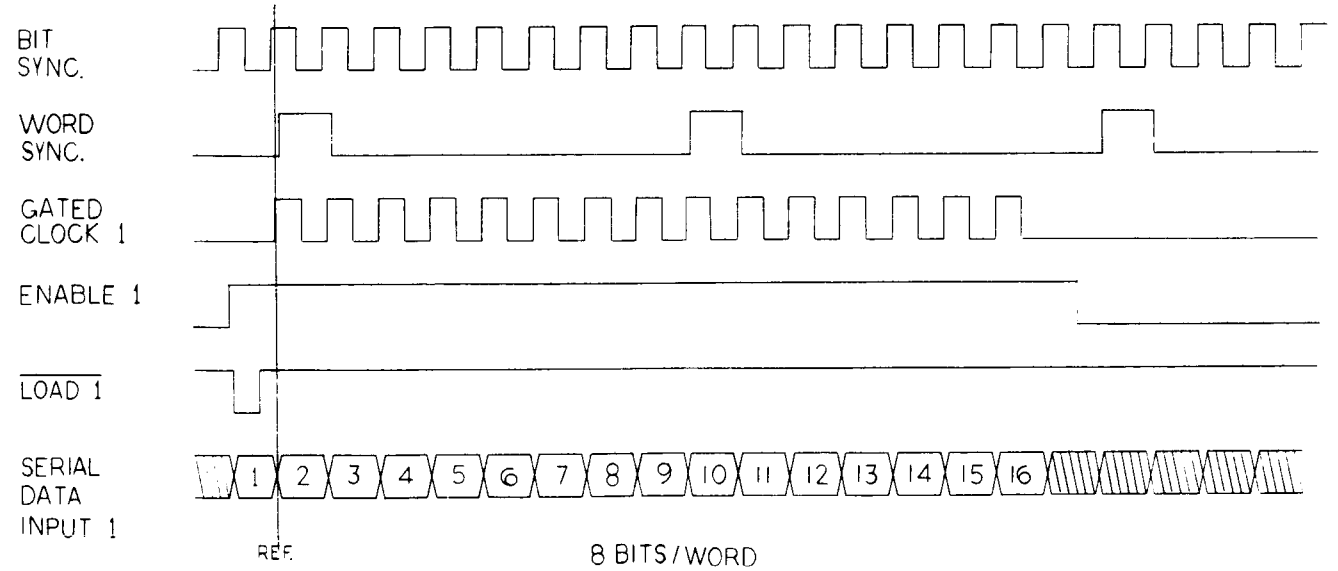


8 BITS/WORD
SINGLE SERIAL DATA WORD

SYMBOL	TYP. (NS.)
T1, T7	1/BIT RATE
T2	70
T3	185
T4	30
T5	0.83 • T1
T6	0.45 • T1
T8	1.5 • T1

NOTES:

1. //// = DON'T CARE.
2. ON THE LEADING EDGE OF THE FIRST GATED CLOCK WHEN ENABLE IS VALID, THE FIRST SERIAL DATA BIT IS CLOCKED IN THE SD-624.
3. THIS SAME EDGE OF THE GATED CLOCK CAN BE USED TO UPDATE THE SOURCE OF SERIAL INPUT DATA.
4. ENABLE 1, GATED CLOCK 1, AND LOAD 1 ARE SD-624 OUTPUTS FOR ONE CHANNEL.



8 BITS/WORD
2 CONTIGUOUS DATA WORDS

Figure 24.-SD-624 timing diagram

TABLE 14. SD-624 WORD LENGTH PROGRAMMING

Word Length	Program A Pin 9	Program B Pin 11
8 bits	0	1
9 bits	1	0
10 bits	0	0

These programming codes are to be used at the external connector of this module. A "0" represents a grounded programming pin and a "1" represents an open programming pin. The word length program must be the same as the word length programmed on the TM-615P, timer module. This program does not necessarily have to match the number of bits in the actual data word, which may be less than the word length of the PCM system.

SD-624 Specifications

Input Voltage.-0 to +0.9 volt dc is recognized as a logic "0". +3.15 to +5.0 volts dc is recognized as a logic "1". The serial digital module can tolerate voltages of -1.5 to +6.5 volts dc without being permanently damaged.

Bit Alignment.-The first bit shifted into the PCM system will be the first bit transmitted.

Output Voltage.-The interface signals, gated clock, enable and inverted load are 0 to +5.0 volt dc signals.

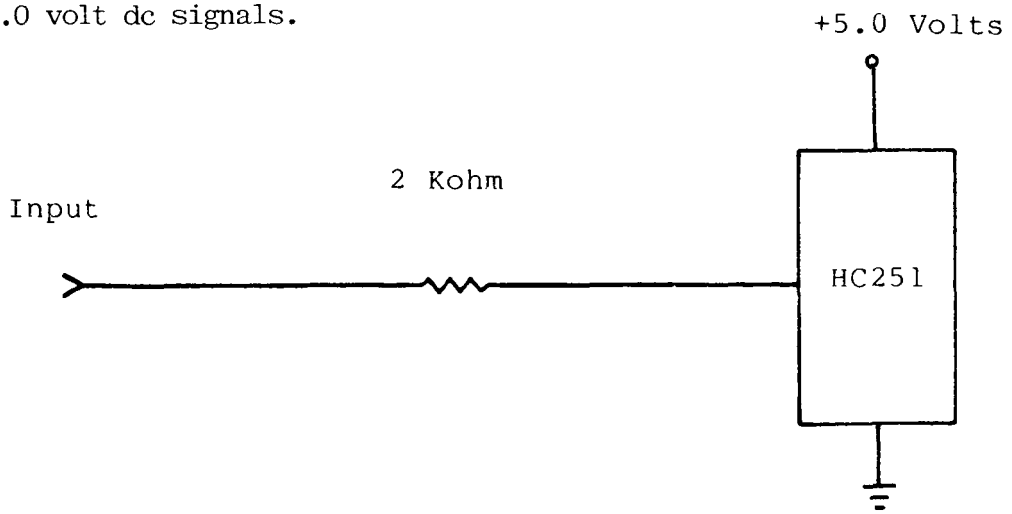


Figure 25.-Typical input circuit to the SD-624

TABLE 15. SD-624 OUTPUTS

Description	Pin Numbers	Output Device
Enable Pulses	36,35,17,16,34, 15,33,14	RCA HC240
Gated Clocks	25,6,24,5,23,4 22,3	RCA HC240
Inverted Load Pulses	31,13,30,12,37 18,32,19	RCA HC244

All outputs from the SD-624 are CMOS or low-power TTL compatible. The outputs are 0 to +5.0 volt dc signals nominal.

CM-622P Dual Counter/Accumulator

The CM-622P module (Figure 26) counts pulses. Each CM-622P contains two 10-bit counter/accumulators. Nineteen counter modules may be used per system for a maximum of 38 individual counter inputs. The actual number of active channels is determined by the program entered in EPROM. Each counter module must be assigned a unique address. This is done by grounding appropriate pins found in the external connector. Open programming pins will be interpreted as a logic "1". Module address programming pins are pulled up to +10 volts through 20 kilohm resistors. For programming codes, see Table 16.

The counter module may be operated in one of two counter modes--dual counter (two separate inputs) and single counter mode (one counter input). In the dual counter mode each counter will output an 8, 9 or 10 bit word and in the single counter mode, the counter module will output a 16, 18 or 20 bit count. When using the single counter mode, data should be entered into counter 0 input and counter 1 should be programmed in the EPROM to read out before counter 0. In the single counter mode, counter 1 input and reset lines have no effect. Counter 1 contains the MSB. If the system word length is greater than 8 bits per word, then the word length must be programmed at the external connector of the counter module. Word length programming is accomplished by grounding appropriate pins at the external connector. See Table 17 for programming codes. An open programming pin is interpreted as a logic "1". Word length programming pins are pulled up to +10 volts through 50 kilohm resistors.

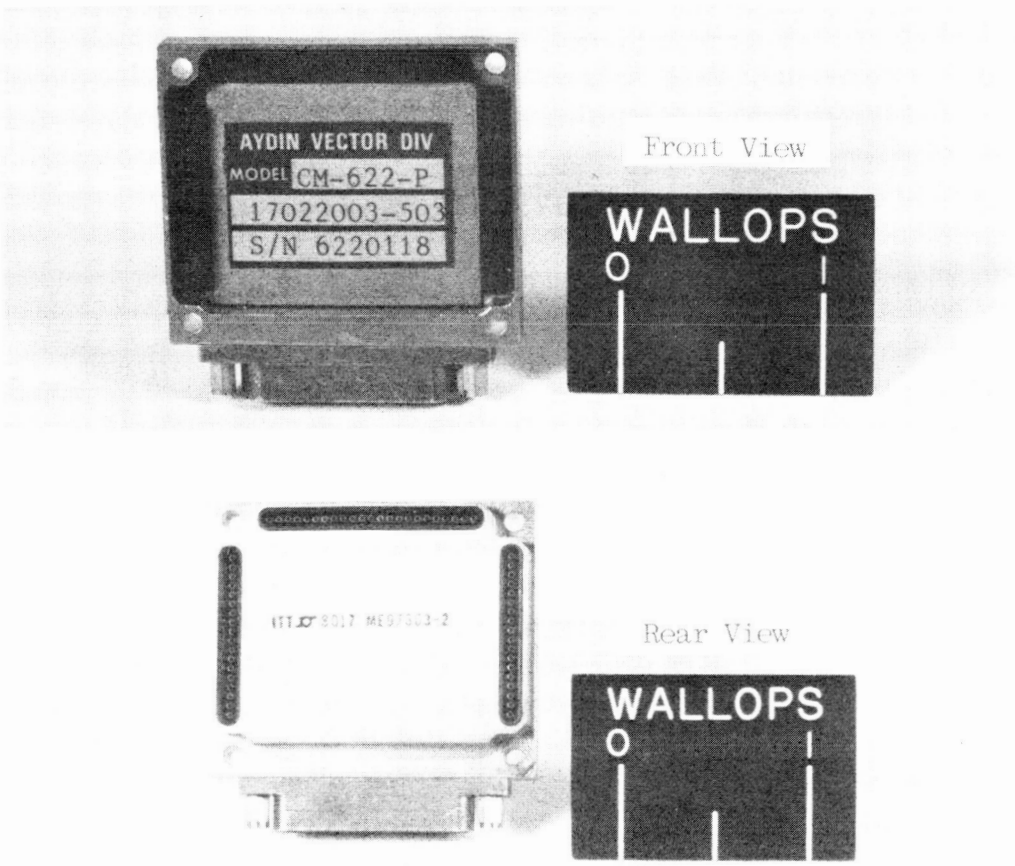


Figure 26.-CM-622P dual counter/accumulator

TABLE 16. CM-622 COUNTER/ACCUMULATOR ADDRESS PROGRAMMING CODES

Channel	Pin No.	A7	A6	A5	A4	A3	A2	A1	A0
0	4	0	0	M	M	M	M	M	0
1	5	0	0	M	M	M	M	M	1

These programming codes are to be used in the EPROM program. A7 is the MSB and A0 is the LSB. When addressing any counter module, A7 and A6 must be programmed with a zero. A5 through A1 are used to select a specific counter module. A0 is used to select a channel within the counter module.

TABLE 17. CM-622P WORD LENGTH PROGRAMMING CODES

Word Length	Program A Pin 6	Program B Pin 11
8 bits	1	1
9 bits	0	1
10 bits	0	0

The word length programming codes are to be used for programming the pins on the external connector of the module. A zero represents a grounded programming pin and a "1" represents an open pin. The word length program must be the same as the word length programmed on the TM-615P timer module. This program does not necessarily have to match the number of bits in the actual data word, which may be less than the word length of the PCM system.

When the word length decreases from 10 bits per word, the MSB's are truncated from the counters to comply with the selected system word length.

There are three reset modes that the counter module can be operated in:

(1) Automatic Clear -- The counter is automatically reset to zero after each time its contents are read out.

(2) External Clear -- The counter continues to totalize until an external reset pulse is applied.

(3) Overflow -- The counter continues to totalize until it clears itself by overflowing upon reaching the maximum count.

Each counter may be operated independently in reset modes. For more information, see Table 18.

The interval at which the contents of the counters are transferred into the PCM output format is under EPROM control. Any individual counter channel is inhibited for a short period of time to prevent it from changing state during transfer of its contents into the PCM output format. This dead period prevents an erroneous count readout. For timing information, see Figure 27.

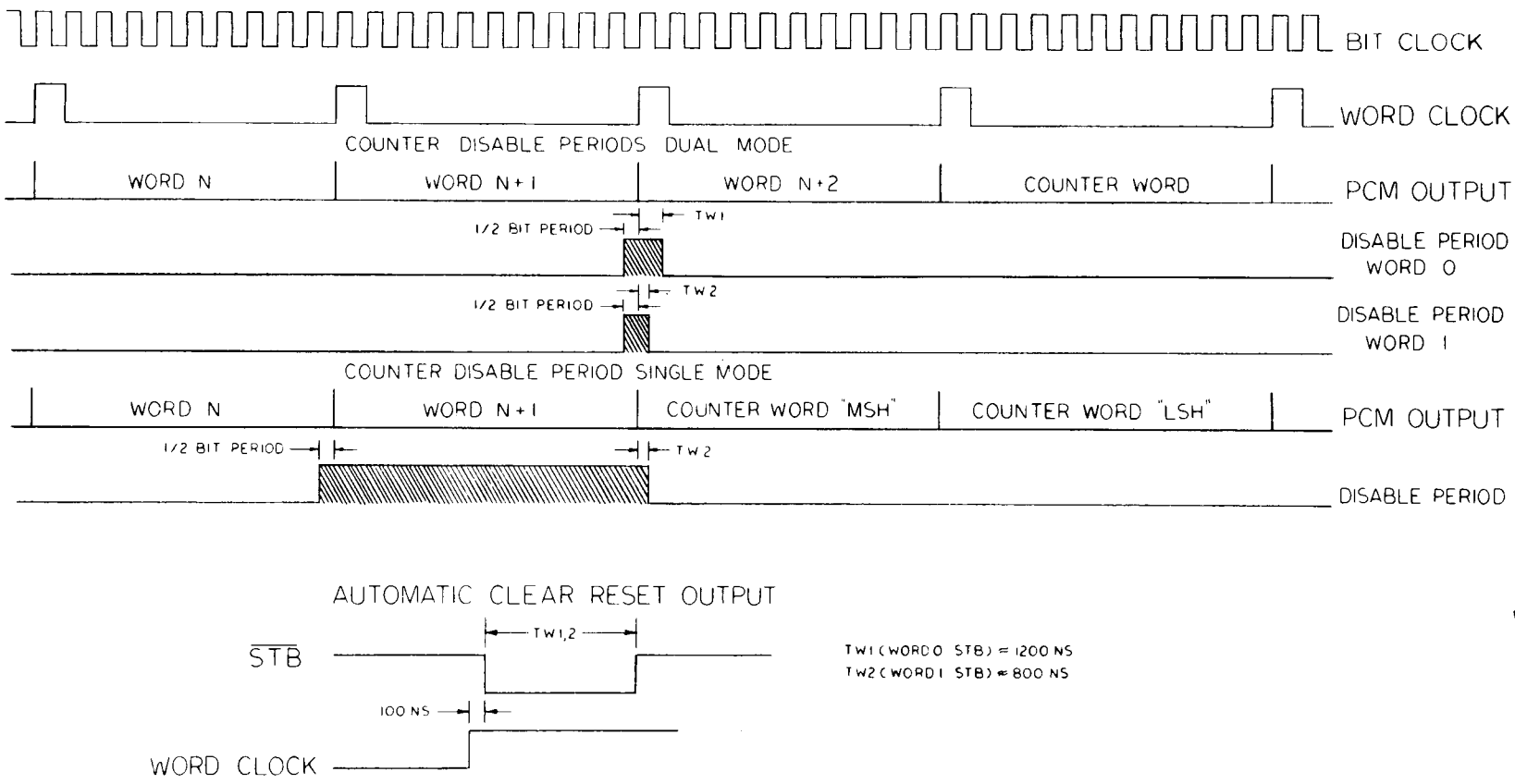


Figure 27.-CM-622P timing program

TABLE 18. CM-622P RESET MODE PROGRAMMING CODES

Counter 0 Input Pin 7	Counter 1 Input Pin 12	Pin 15	Mode
Jump to pin 9	Jump to pin 10	1	Automatic
Positive External Pulse	Positive External Pulse	0	External
Negative External Pulse	Negative External Pulse	1	External
0	0	0	Overflow
1	1	1	Overflow

These programming codes are to be used at the external connector of the counter modules. Pin 16, not shown, is used to select single or dual counter operation. Grounding pin 16 will select single counter operation (one counter input) and leaving pin 16 open will select dual counter operation (two counter inputs per module). In single counter mode, data is input to counter 0 (pin 4). Counter 1 contains the MSB and is programmed in the EPROM program to read out before counter 0. In single counter mode, counter 1 input and reset lines have no effect. Pin 15, shown above, selects between a positive or negative external reset pulse. The negative reset pulse should be 0.0 volts nominal during reset conditions and +5.0 volts during totalize conditions. See the specifications for more information concerning the external reset pulses. The program at pins 7, 12 and 15 should match to select the overflow mode.

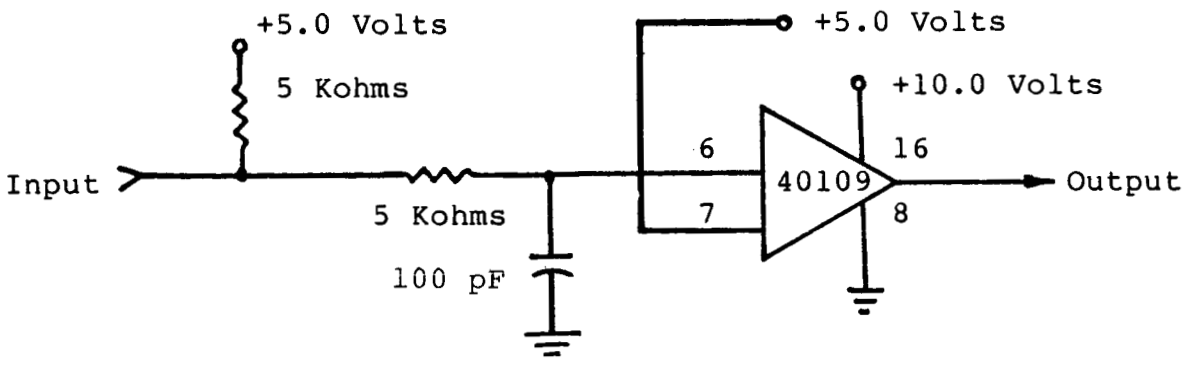


Figure 28.-Typical counter input circuit

CM-622P Specifications

Counter Input Voltage.-0 to +5.0 volts nominal. CMOS or TTL compatible. For a full 0 to +5.0 volt pulse, the minimum pulse width recognizable is 500 nanoseconds. For a pulse input of less than 0 to +5.0 volts, the minimum pulse duration is 1000 nanoseconds (typical CMOS or low power TTL is less than 0 to +5.0 volts). Voltages outside the range -0.5 to +5.5 volts dc will cause permanent damage to the module.

Pulse Pair Resolution.-1 Hz up to 1 MHz nominal. Also dependent upon input voltage amplitudes given above.

External Reset Input Voltage.-The positive external reset input must be a 0 to +5.0 volt pulse nominal. The interface must operate into a 10 kilohm input impedance and the pulse duration must be one microsecond minimum. The negative external reset pulse should be 0.0 volt to reset the counter and +5.0 volts during the totalize period.

The above specifications are boundary conditions and reliable interface design will fall well within these limits.

TABLE 19. CM-622P INPUTS

Description	Pin Number(s)	Input to IC Type
Program A1 - A5	3,17,18,13,14	RCA 4063 & 4030
Counter 0, 1 Inputs	4,5	RCA 40109
Word Length Program A & B	6,11	RCA 4049
Counter 0, 1 Reset Inputs	7,12	RCA 40109
Compliment Reset	15	RCA 4030
Counter Mode Control	16	RCA 4019

TABLE 20. CM-622P OUTPUTS

Description	Pin Number(s)	Output from IC Type
Counter 0, 1 Internal Reset Output	9,10	RCA 4049

TA-623 Time Event Monitor with Alternating Registers

The function of the time event module (Figure 29) is to allow the user to determine the elapsed time between the occurrence of two events (pulses). This is accomplished by determining the position in the major frame at which the user's pulses occur. There is a binary counter accumulator in the module which is reset to zero at the beginning of the major frame. The input to this counter is the word clock. The binary count is incremented by one at the beginning of each word. The parallel output of the counter is latched into a storage register by the leading edge of each input pulse. The contents of the latched register can be read out as often as required in the format. The readout is nondestructive. However, since a new word number is stored in the latched register by each input pulse, data will be lost if the register is not read out between input pulses.

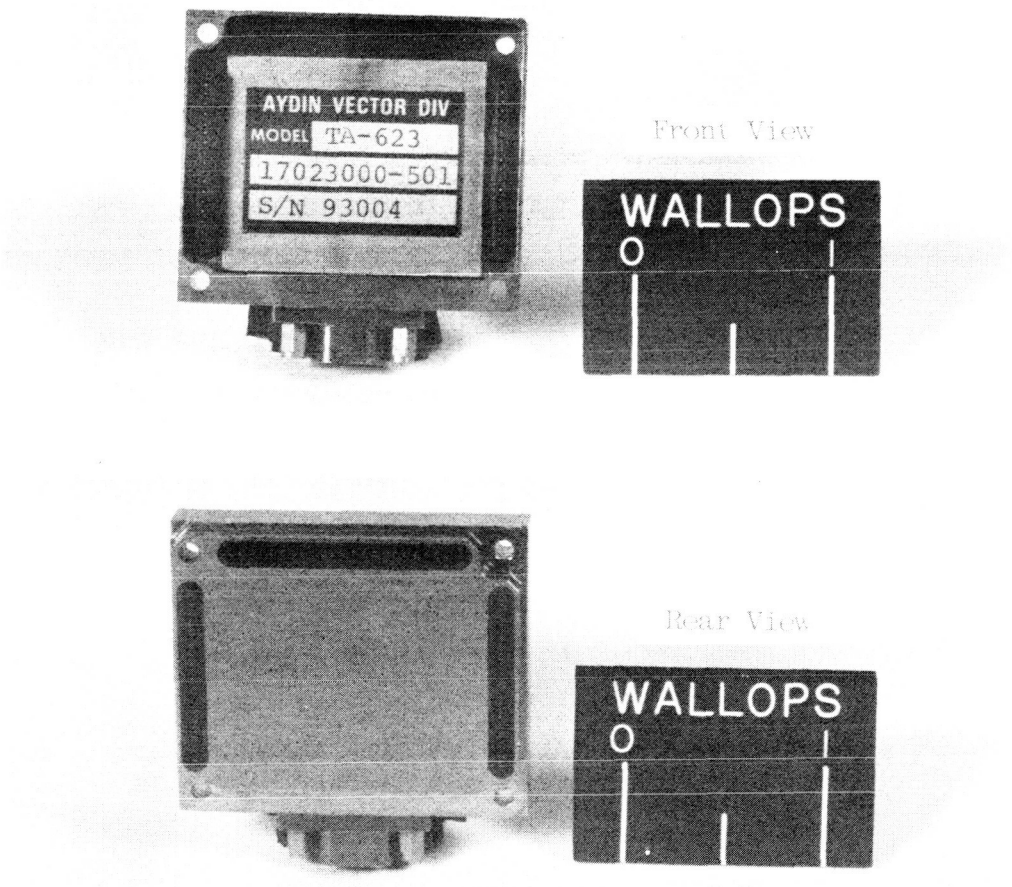


Figure 29.-TA-623 time event monitor with alternating registers

Obviously, the resolution to which the elapsed time between two input pulses can be determined is two word periods. Also, the following ambiguity exists. The only way to determine if a new pulse has occurred is to monitor the word number which is read out each time for a change. When it changes, a new pulse input has occurred. Should a new pulse input occur in the same word period as the previous pulse, the latter will not be detected since the new word count stored in the latch will be the same as the old value.

CAREFUL CONSIDERATION MUST BE EXERCISED IN THE SELECTION OF SYSTEM PARAMETERS SUCH AS BIT RATE, WORD SIZE, NUMBER OF WORDS IN THE MAJOR FRAME, READOUT RATE, AND INPUT PULSE LENGTH TO OBTAIN USEFUL DATA FROM A TIME EVENT MODULE.

The bit rate and word size control the maximum elapsed time resolution obtainable. Increasing the number of words in the major frame diminishes the probability that the ambiguity will occur. If the readout rate is inadequate, the output data will not be correct.

For certain types of data, as depicted in Figure 30, the required readout rate may be reduced significantly by storing the word numbers in which alternate pulses occur in alternate registers. The registers are then read out independently--this is the reason that the TA-623 has two different types of time event monitors with two separate inputs. The input associated with the alternating registers is interface connector pin no. 1, and the word numbers at the time of occurrence of alternate pulses on that input are stored in alternate registers numbers 2 and 3. For asynchronous pulse inputs, the register in which the first pulse is stored is indeterminate. This complicates, but does not inhibit, data reduction.

The input associated with interface connector pin no. 6 is the normal type of time event monitor described initially. It has only one storage register no. 1 in which the word number at the time of the event input pulse is latched.

Figure 30.-TA-623 alternating register application

The design of the alternating registers is suited to the data input in Figure 30. When pulse pairs occur on the data input and then are followed by a comparatively long delay before another pulse pair occurs, the alternating registers can be used advantageously. The time event information is stored in two storage registers alternately. For pulse groups of more than two pulses per group, the alternating registers will no longer be of advantage. The output data must be predictable as indicated in Figure 30 to utilize the advantage of the alternating registers.

For the non-alternating input, the time event channel must be programmed to be sampled at a rate greater than the highest pulse pair resolution of the actual data. The alternating registers can be used as in the previous example to read out that particular channel at a lower rate. In this way, more of the output format is reserved for other data channels.

The binary counter accumulator, which counts the word number in the major frame, is 12 bits long; therefore, it can accommodate a major frame length of 4095 words. When the number of words in the major frame exceeds the maximum binary value of the system word, the word number data stored in the 12-bit storage register must be read out in two contiguous system words. The word number is read out LSB first. When a two-word readout is necessary, the most significant bits are located in the second word with some duplication. For a detailed description of the readout configuration and technique, see Tables 26 and 27 in the TB-625 section.

The contents of the storage registers are multiplexed and entered into the PCM output format under EPROM program control. Only one TA-623 is permitted per system. Important information concerning the input and output time domains are given in Figure 31.

In Figure 31, an important point to note in the system timing is the offset that exists between the internal system domain and the PCM output domain. The two domains are skewed by two word periods. Further, the word per major frame counter is reset to zero at the leading edge of the major frame pulse.

The event pulse shown will load number 6 into the storage register within the time event monitor modules. The time event channel may be read out anywhere in the output format. The sampling rate of the time event channel should be greater than the highest frequency component in the actual data.

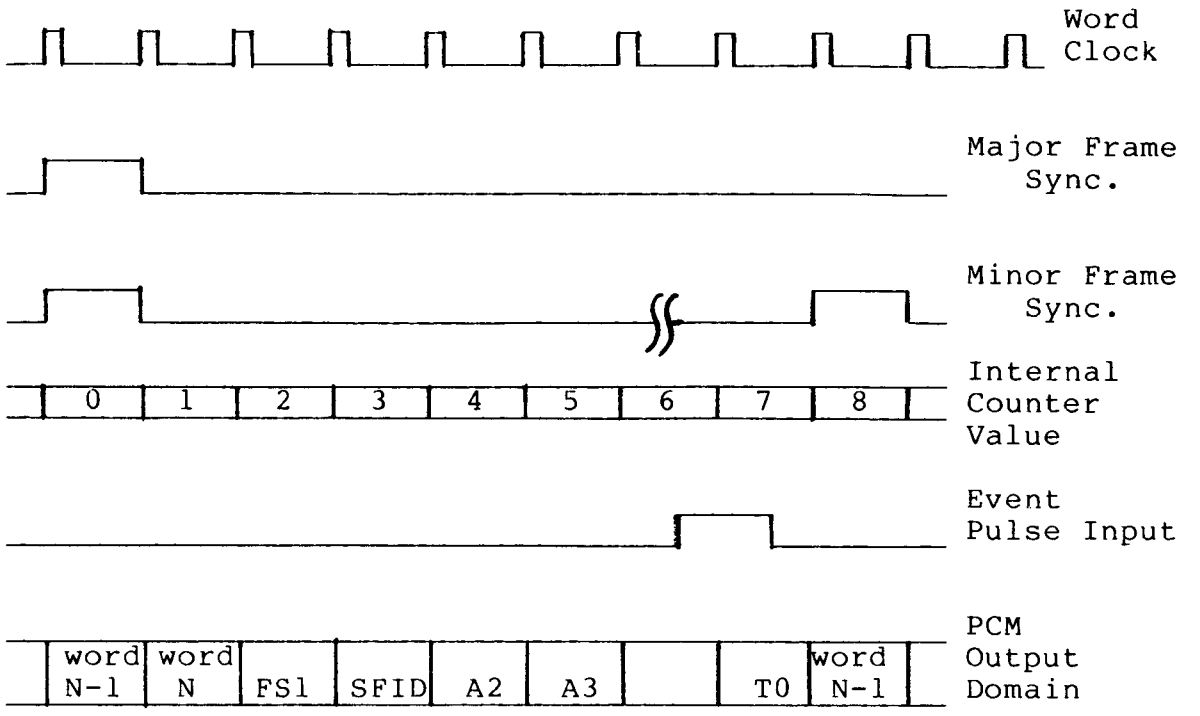


Figure 31.-Time event timing diagram

Since event pulses are asynchronous with the PCM timing, the word count is latched into each register by the first bit clock pulse that occurs immediately after the appropriate event pulse. Specific EPROM codes are dedicated to select each register within the module. The contents of each register is entered into the PCM output format at the coincidence of the assigned address and the internally generated "Load Command" pulse. The leading edge of the event pulse is used for information storage and the trailing edge has no effect.

Four synchronization signals utilized in this module are buffered and made available to the user as a convenience. Their use is not required to properly interface with the TA-623.

TA-623 Specifications

Input Voltage.-The event pulse inputs are CMOS or low power TTL compatible and are 0 to +5.0 volts nominal. Voltages outside the range -0.3 to +36 volts dc will cause permanent damage to the module.

Pulse Duration.- The pulse input must be of duration one microsecond minimum.

These specifications are boundary conditions and reliable interface design will fall well within these limits.

TABLE 21. TA-623 INPUTS

Description	Pin Number(s)	Input to IC Type
Event 0, 1 Inputs	6,1	LM 339
A3 Programming	8	RCA 4063

TABLE 22. TA-623 OUTPUTS

Description	Pin Number(s)	Output from IC Type
Major Frame Sync.	3	RCA 4050
Minor Frame Sync.	2	RCA 4050
Word Clock	5	RCA 4050
Bit Clock	4	RCA 4050
2X Bit Clock	7	RCA 4050

TB-625 Time Event Monitor with Timing Buffers

The TB-625 (Figure 32) is a second type of time event monitor used for determination of the relative time of occurrence of events. This module functions in exactly the same manner as the non-alternating input of the TA-623 time event monitor. The TB-625 has two separate event pulse inputs. Two TB-625 modules are permitted per system for a capability of four time event channels from TB-625 modules. Selecting between TB-625 modules is done by an address assignment made at the external connector of the module. The address programming pin is pulled up to +10 volts through a 30 kilohm resistor. Programming is accomplished by grounding the appropriate pin at the external connector. An open programming pin will be interpreted as a logic "1". For module programming codes, see Tables 23 through 25.

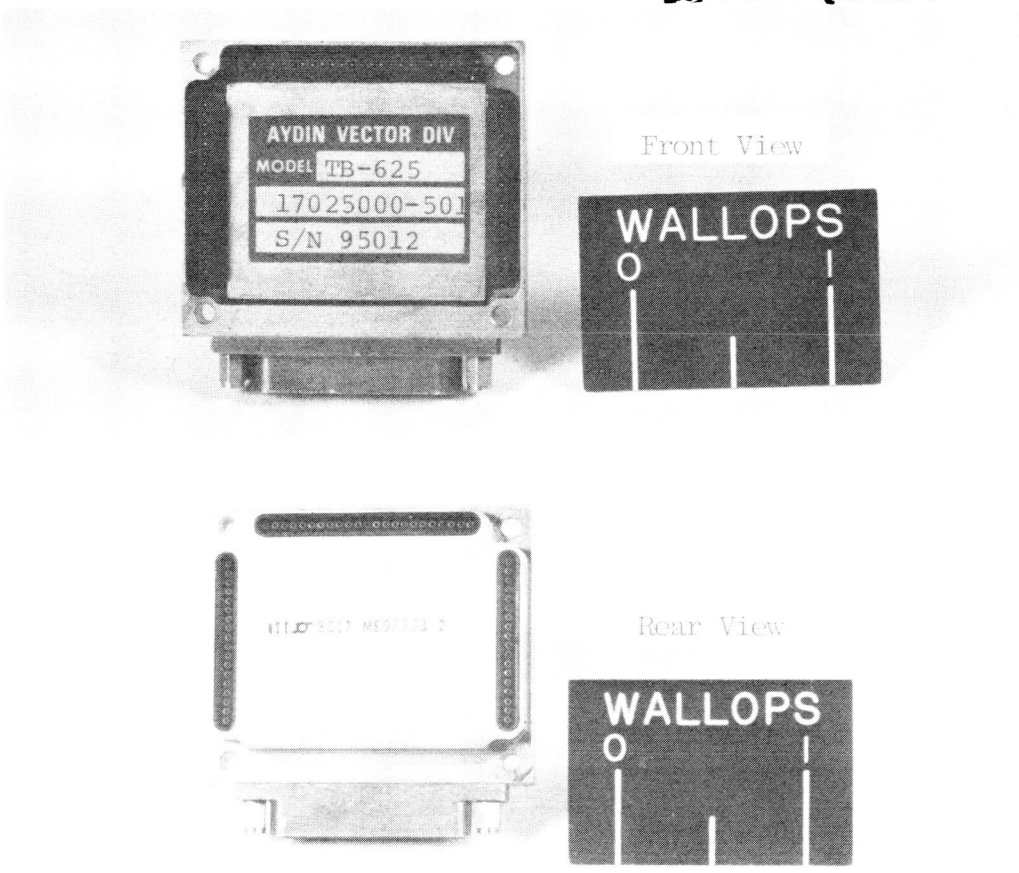


Figure 32.-TB-625 time event monitor with timing buffers

Another feature provided by the TB-625 is a set of internal binary counters which provide the "X" and "Y" positions in the format at any time. The outputs of these two counters are buffered and available on the external interface connect to permit external devices to be synchronized with the PCM major frame format. The output from one of the counters provide the word number in the frame and is reset to zero by the minor frame pulse. The output from the other counter is the minor frame number and is reset by the major frame. The word/frame counter has eight stages and counts from 0 to 255. The minor frame counter has five stages and counts from 0 to 31. (See Figure 31 for timing references.)

As with the non-alternating input of TA-623, the TB-625 has a single twelve-stage binary counter used to count major frame words from 0 to 4095. Associated with each of the inputs is a single 12-bit register into which the word number from the 12-bit word counter is latched. Again the number of active channels within this module, the readout rate and position within the PCM format are under EPROM format control.

TABLE 23. TA-623 and TB-625 PROGRAMMING CODES

Module	Register	Word	A7	A6	A5	A4	A3	A2	A1	A0	Hex. Code	Module No.
TA-623	1	1	1	1	0	1	1	0	0	0	D8	1
		2	1	1	0	1	1	0	0	1	D9	
	2	1	1	1	0	1	1	0	1	0	DA	
		2	1	1	0	1	1	0	1	1	DB	
	3	1	1	1	0	1	1	1	0	0	DC	
		2	1	1	0	1	1	1	0	1	DD	
TB-625	1	1	1	1	0	0	1	0	0	0	C8	1
		2	1	1	0	0	1	0	0	1	C9	
	2	1	1	1	0	0	1	0	1	0	CA	
		2	1	1	0	0	1	0	1	1	CB	
	1	1	1	1	0	0	0	0	0	0	C0	2
		2	1	1	0	0	0	0	0	1	C1	
	2	1	1	1	0	0	0	0	1	0	C2	
		2	1	1	0	0	0	0	1	1	C3	

The above codes are to be used in the EPROM program. A7 represents the MSB and A0 is the LSB. When using TA-623 and/or TB-625 modules in a system, program A7 = 1, A6 = 1, and A5 = 0. A4 programming determines whether the TA-623 or the TB-625 module is addressed. A3 applies only to the TB-625 module and is used for module number selection. Since only one address line is allocated for module selection, only two TB-625 modules can be used per system. A1 and A2 programming determines which data register, No. 1, No. 2 (or No. 3 in the TA-623) is selected for readout. A0 programming determines which word is read out. See Table 24 for more information concerning word selection. When using a time event module in a system, the program for the MP-601L Analog Multiplexer A7 = 1, A6 = 1 and A5 = 0 CANNOT be used.

TABLE 24. TA-623 and TB-625 PROGRAMMING CONDITIONS

Bits per Word	Condition	Use From Table 15
10	MFL <= 2^{10}	Word 1
	MFL > 2^{10}	Word 1 & 2
9	MFL <= 2^{9}	Word 1
	MFL > 2^{9}	Word 1 & 2
8	MFL <= 2^{8}	Word 1
	MFL > 2^{8}	Word 1 & 2

The conditions listed in the above table are used to determine the EPROM program necessary to recover correct data from the time event modules. MFL equals the major frame length measured by the number of words. Words 1 and 2 are taken from Table 23 and different programming codes are required to read out each word. Recall that the storage registers consist of twelve stages. It follows that the maximum count of these registers cannot be read out in one 8, 9, or 10 bit word. This is why the programming of word 2 is sometimes necessary. The condition for only word one to be read out of each register is, if MFL is less than or equal to 2^n, where n equals the number of bits per word. If MFL is greater than 2^n, then word 1 and 2 must be read out of each register. The program for readout of word 1 and 2 must occur in consecutive EPROM locations. For information concerning the word organization, see Table 25.

TABLE 25. TA-623 and TB-625 WORD ORGANIZING

	A0 = "0" Word 1										A0 = "1" Word 2									
Bit	1	2	3	4	5	6	7	8	9	10	1	2	3	4	5	6	7	8	9	10
Word Organizing	2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7	2^8	2^9										
	2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7	2^8	2^9	2^8	2^9	2^{10}	2^{11}	1	0	1	0	1	0

The word organization described above depicts the PCM output. Bit 1 is the first bit transmitted and bit 10 is the last bit transmitted. In this organization, the LSB of the counter value is the first bit transmitted. When programming both words 1 and 2 for readout is necessary, word 2 will have alternating ones and zeros in bits 5 through 10.

Since event pulses are asynchronous with the PCM timing, the word count is latched into each register by the first bit clock pulse that occurs immediately after the appropriate event pulse. Specific EPROM codes are dedicated to select each register within this module. The contents of each register is entered into the PCM output format at the coincidence of the assigned address and the "load command" pulse internally generated within the system. The leading edge of the event pulse is used for information storage and the trailing edge has no effect. The resolution of the reduced data will then be equivalent to two word periods of the system. The sampling rate chosen for time event channels must be greater than the greatest frequency component of the actual data being measured.

TB-625 Specifications

Input Voltage.-The event pulse inputs are CMOS or low power TTL compatible and are 0 to +5.0 volts nominal. Voltages outside the range -0.3 to +36 volts dc will cause permanent damage to the module.

Pulse Duration.-The pulse input must be of duration one microsecond minimum.

These specifications are boundary conditions and reliable interface design will fall well within these limits.

TABLE 26. TA-623 INPUTS

Description	Pin Number(s)	Input to IC Type
Event 0, 1 Inputs	20,1	LM 339
A3 Programming	37	RCA 4063

TABLE 27. TB-625 OUTPUTS

Description	Pin Number(s)	Output from IC Type
Major Frame Sync.	3	RCA 4050
Minor Frame Sync.	2	RCA 4050
Word Clock	5	RCA 4050
Bit Clock	4	RCA 4050
2X Bit Clock	7	RCA 4050
Minor Frame Number	6,16,17,18,36	RCA 4050
Word per Frame	7,8,9,10,11 12,14,15	RCA 4050

FL-619A Adjustable Output Quad Filter

This module (Figure 33) contains four linear phase lowpass filters. The FL-619A modules are provided with upper -3 dB points of (1120, 560, 280, 140, 92, 70, 46, 35, 23, 17.5, 11.5, and 8.8) KHz. Wallops Flight Facility supplies modules with four of the above -3 dB frequencies per module. The most common code used by Wallops Flight Facility is Bi-Ø-L. A filter for Bi-Ø-L code is selected by the formula:

1.4 x bit rate = Upper -3 dB fco.

A filter for NRZ-L, the other common code output by the system, is selected by the formula:

0.7 x bit rate = Upper -3 dB fco.

The appropriate unfiltered PCM output from the timer module (TM-615P), is connected to pin no. 6 of the FL-619A. This input is fed to all four active filter inputs

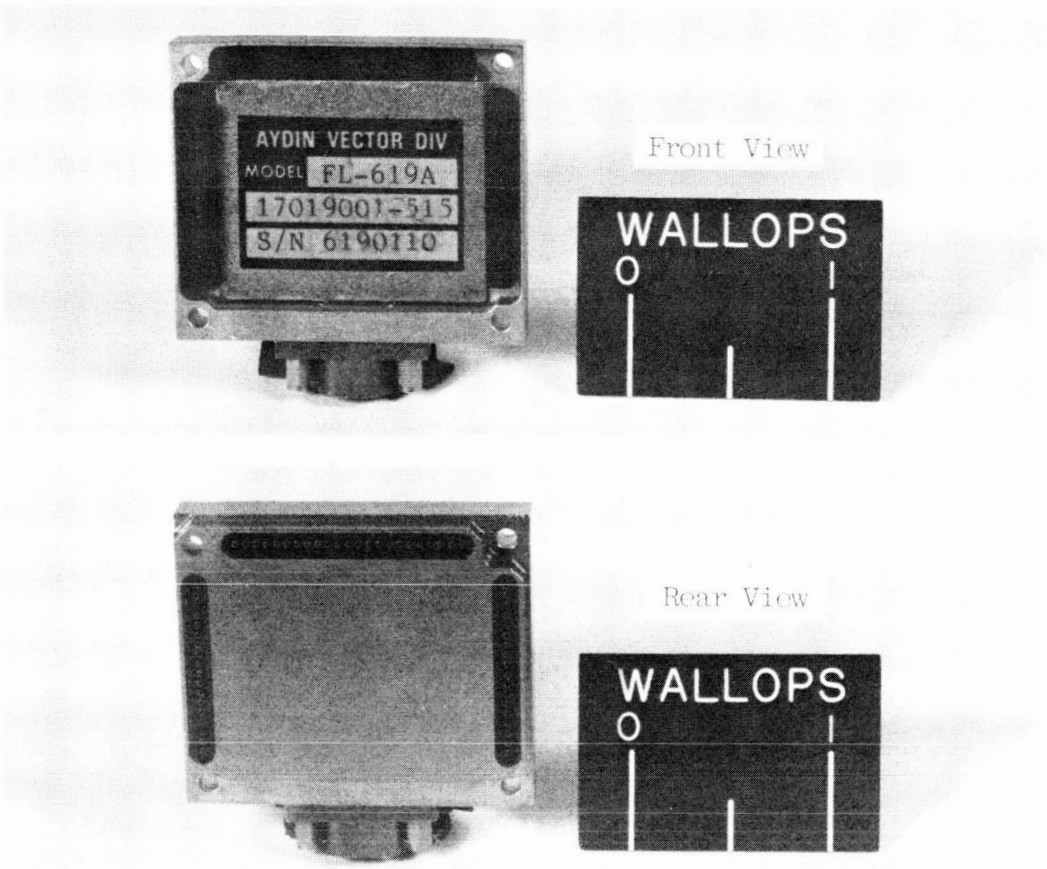


Figure 33.-FL-619A adjustable output quad filter

in parallel in the quad filter module. The pin from the desired filters output, filter no. 1-4, is then connected back to pin no. 1 of the FL-619A. This is the input to an adjustable gain amplifier. The filters bipoler low impedance output is on pin no. 2. The output voltage gain is adjustable using the potentiometer contained in the FL-619A. Access to the potentiometer is achieved through a slot on the formatter module. The FL-619A must be located directly above the FM-618 formatter module to allow adjustments.

FL-619A Specifications

Input Voltage Range.-0 to +5.0 volts nominal input from the TM-615P timer module.
Input Impedance.-10 kilohms minimum.
Output Impedance.-Less than 10 ohms.
Output Voltage Range.-Adjustable ±0.1 to ±5.0 volts centered about 0.0 volt.
Roll-Off Slope.-The roll-off slope past the -3 dB point is 36 dB/Octave.

TABLE 28. QUAD FILTER MODULES

Part Number	Low Pass Filters (Cut-off point in KHz) 1	2	3	4
17019001-501	1120	560	280	70
17019001-502	92	46	23	11.5
17019001-508	1120	560	280	140
17019001-509	70	35	17.5	8.8
17019001-515	1120	280	70	17.5
17019001-516	560	140	35	8.8

PROCESSOR CONTROL AND PROGRAMMING

The processor module executes the program entered into the 256 x 8 EPROM to accomplish the following functional capabilities. Multiple subframes with subcommutation rates up to 1/32 of the minor frame rate are possible. The rate of supercommutation is unlimited by the processor; however, supercommutation is limited by the size of the EPROM. Lastly, frame and subframe synchronization words may be located in any position of the format in any bit pattern. It is required to have a subframe identification counter word precede any subcommutated word.

One memory location of the 256 x 8 EPROM is required for each minor frame word, independent of the number of minor frames per major frame. Approximately a 7,000 word major frame is possible due to this technique. The format size is limited by the size of the EPROM. The maximum number of input channels is near 240, depending on the format configuration. Ten bits of bi-level parallel inputs are considered one data channel for a ten-bit system. A machine cycle of the processor is carried out within one PCM word period. The machine cycle is divided into seven clock periods, T0 - T6. The special instruction codes, recognized by the processor and used to program the system, can be used as input data channel addresses provided these channels are subcommutated. This is possible because -- after the T2 clock period -- the instruction decoder is ineffective.

Figure 34 illustrates the block diagram of the processor module. There is no external connector on the processor module.

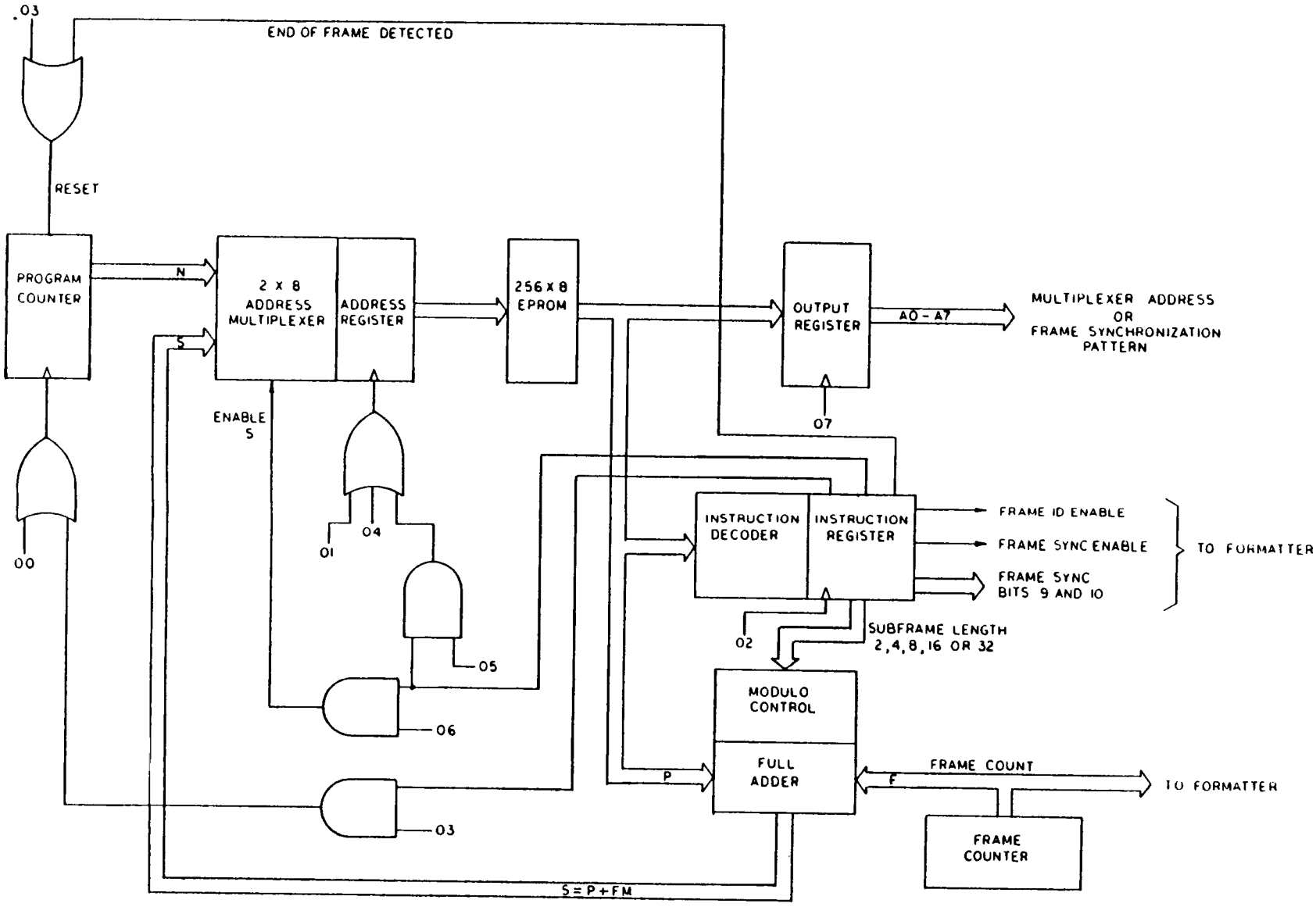


Figure 34.-Processor block diagram

PR-614 Processor Control Sequence

The following discussion covers the seven machine cycles, T0 through T6, required by the processor to execute the program that is stored in the EPROM. The machine code is given for each machine cycle for each type of code that the processor may encounter followed by a comment explaining the machine code.

T0: PC <-- N; Program Counter updates to N.

T1: AR <-- N; Address Register is loaded with N.

T2: IR <-- (N); Instruction Register is loaded with the contents of N.

Now the instruction decoder interrogates the contents of N.

Contents of N is not an Instruction.-Nothing important happens until T6.

T6: OR <-- Data; Output Register is loaded with Data Channel Address.

Contents of N is an Instruction.-T3: PC <-- N+1; Program Counter is updated to N+1.

T4: AR <--N+1; Address Register is loaded with N+1.

Subcommutated Data Instruction Detected:

T5: AR <--(N+1) + (FC); Address Register is loaded with the sum of the contents of N+1 and the Frame Counter.

T6: OR <-- (AR); Output Register is loaded with the subcommutated channel address.

(N+1) is the initial memory address for that subframe. This instruction contains indirect address information.

Frame ID Word Instruction Detected:

PCM Output <-- Status of the Frame Counter.

A command is issued to the formatter module to transfer the status of the frame counter to the PCM output.

(N+1), the contents of register N+1, contains the subframe counter reset information. This information is used to reset the frame counter as appropriate. (N+1) is composed of the following:

The three MSB's are ones and the five LSB's are a binary representation of the number of minor frames per major frame.

Frame Sync Word Detected:

This instruction is used three to five percent of major frame words but can be used as often as desired and carry any information desired. (N+1) is the eight MSB's of the frame sync word. For 10 bit systems, the two LSB's are included as the two LSB's of the frame sync word instruction.

```
T6:    OR <-- (N+1); Output Register is loaded with the
                     contents of (N+1). (Eight MSB's of
                     Frame Sync Word.) Then a command is
                     sent to the formatter module to transfer
                     the complete frame sync word to the PCM
                     output.
```

End of Frame Instruction Detected:

This instruction is the exception to the rule stated in the paragraph headed "Contents of N is an Instruction."

```
T3:    PC  <-- 0; Program Counter resets to Zero.
```

The contents of memory location 0 in the EPROM are the eight MSB's of the frame sync word. For nine and ten bit systems the two LSB's of the end of frame instruction are the LSB's of the frame sync word. This instruction marks the end of the major frame and outputs the first frame sync word.

Refer to Figure 34 for a block diagram of the processor module. See Table 29 for the EPROM instruction codes.

Programming Equipment

The 9702A EPROM can be programmed using any one of the commercially available EPROM programmers on the market today.

Instruction Codes

Instruction codes are unique eight bit codes. The four most significant bits are all ones. The next four bits determine the particular instruction code and contain other pertinent information. See Table 29, EPROM Instruction Codes, for further information.

TABLE 29. EPROM INSTRUCTION CODES

Instruction	A7	A6	A5	A4	A3	A2	A1	A0	HEX.	Comments
End of Frame	1	1	1	1	1	1	1	1	FF	Bits A1, A0 are stored for insertion into bit 9 and 10 position of first frame sync word for 9 and 10 bit systems.
	1	1	1	1	1	1	1	0	FE	
	1	1	1	1	1	1	0	1	FD	
	1	1	1	1	1	1	0	0	FC	
Frame Sync. Word	1	1	1	1	1	0	1	1	FB	Bits A1, A0 are stored for insertion into bit 9 and 10 position of first frame sync word for 9 and 10 bit systems.
	1	1	1	1	1	0	1	0	FA	
	1	1	1	1	1	0	0	1	F9	
	1	1	1	1	1	0	0	0	F8	
Frame ID Word	1	1	1	1	0	1	1	1	F7	
									F6	RESERVED Do Not Use
									F5	RESERVED Do Not Use
Subcommutated Data Word	1	1	1	1	0	1	0	0	F4	32 Deep Subframe
	1	1	1	1	0	0	1	1	F3	16 Deep Subframe
	1	1	1	1	0	0	1	0	F2	8 Deep Subframe
	1	1	1	1	0	0	0	1	F1	4 Deep Subframe
	1	1	1	1	0	0	0	0	F0	2 Deep Subframe

The above codes must be used only for instruction. Any analog multiplexer enabled by 111XXXXX code must not use these fourteen codes if the multiplexer is a prime frame multiplexer. If the multiplexer is a subcommutated multiplexer, it is permissible to use these codes.

Programming the System

°Obtain the PCM format drawing. An example format drawing is given in Figure 5.

°Choose the multiplexer types and quantities of each to satisfy mission requirements.

°Assign multiplexer enable addresses from the available codes. Refer to the specific module section or the Quick Programming Code Section and Table 29 to insure selecting allowable codes.

°Assign the input channels to be used on each multiplexer.

°Convert the binary codes of the input channels to hexadecimal codes.

°Convert the frame synchronization word patterns to hexadecimal and subframe ID instruction word if subcommutation is to be used.

°Convert instructions necessary for the format configuration to hexadecimal.

°The entire format must be programmed through the end of frame instruction before assigning the indirect addresses. Generate the indirect addresses for the subcommutated data if subcommutation is used. The indirect addresses follow the subcommutated data word instructions in consecutive EPROM memory locations. The indirect addresses may then be assigned to the blank EPROM memory locations.

A sample payload configuration is included in a latter section. Refer to that section for exemplary information. Refer to the Programming Codes Quick Reference Section for programming codes and external connector pin output lists.

Programming Exceptions and Examples

For subframe depths other than binary multiples, the instruction for 32 deep subframe is programmed. The 14 codes listed in Table 29 must be used for instruction only. Any analog multiplexer enabled by 111XXXXX code must be a subcommutated multiplexer. The instruction register, which recognizes EPROM instruction codes, is ineffective after machine cycle T2. Therefore, this group of codes can be used as a subcommutated multiplexer address or a system instruction.

End of Frame and Frame Sync. Programming Example

Documentation below steps through a typical EPROM program starting with the End of Frame Instruction and proceeding through the Subframe ID Instruction. Examples are given for EPROM address locations, address contents and PCM output. The end of

frame instruction is started at a chosen location in the EPROM assumed to be at the end of the program. The following EPROM location used will be address 00, the beginning of the program.

EPROM Address: 10100001 (binary) A1 (hexadecimal)

EPROM Contents: 111111 10 (binary) FF (hexadecimal)

Comment: End of Frame Instruction programmed in memory location A1 of the EPROM. The two LSB's of the instruction code are used as the LSB's required for 9 and 10 bit words below.

EPROM Address: 00000000 (binary) 00 (hexadecimal)

EPROM Contents: 11101101 (binary) ED (hexadecimal)

Comment: Frame Sync Word programmed in memory location 00 of the EPROM. This is not an instruction, but, a programmed word. The LSB's for 9 and 10 bit words are taken from the LSB's of the preceding instruction (above).

PCM Output:
11101101 10 (10 bit word)
11101101 1 (9 bit word)
11101101 (8 bit word)

EPROM Address: 00000001 (binary) 01 (hexadecimal)

EPROM Contents: 111110 10 (binary) F8 (hexadecimal)

Comment: Frame Sync Instruction programmed in memory location 01 of the EPROM. The two LSB's of the instruction code are used as the LSB's required for 9 and 10 bit words below.

EPROM Address: 00000010 (binary) 02 (hexadecimal)

EPROM Contents: 10001000 (binary) 88 (hexadecimal)

Comment: Frame Sync Word programmed in memory location 00 of the EPROM. This is not an instruction, but, a programmed word. The LSB's for 9 and 10 bit words are taken from the LSB's of the preceding instruction (above).

PCM Output:
10001000 10 (10 bit word)
10001000 1 (9 bit word)
10001000 (8 bit word)

EPROM Address:	00000011 (binary)	03	(hexadecimal)
EPROM Contents:	11110111 (binary)	F7	(hexadecimal)
Comment:	Subframe ID Instruction programmed in memory location 03 of the EPROM. The following EPROM address location will contain a data word used in resetting the frame count.		
EPROM Address:	00000100 (binary)	04	(hexadecimal)
EPROM Contents:	11111111 (binary)	FF	(hexadecimal)
Comment:	Frame counter reset word programmed in memory location 04 of the EPROM. This particular reset word indicates a major frame containing 32 subframes.		

Frame ID Word Instruction Programming Example

Two examples of Frame ID Word Instruction Programming are given below:

Example 1

EPROM Address:	00000011 (binary)	03	(hexadecimal)
EPROM Contents:	11110111 (binary)	F7	(hexadecimal)
Comment:	Frame ID Word Instruction programmed at EPROM memory location 03.		
EPROM Address:	00000100 (binary)	04	(hexadecimal)
EPROM Contents:	11100111 (binary)	E7	(hexadecimal)
Comment:	This subframe counter reset word, which follows the frame ID word instruction in consecutive EPROM memory locations, describes an 8 deep subframe length.		

Example 2

EPROM Address:	00000011 (binary)	03	(hexadecimal)
EPROM Contents:	11110111 (binary)	F7	(hexadecimal)
Comment:	Frame ID Word Instruction programmed at memory location 03 in the EPROM.		
EPROM Address:	00000100 (binary)	04	(hexadecimal)
EPROM Contents:	11110011 (binary)	F3	(hexadecimal)
Comment:	This subframe counter reset word, which follows the frame ID word instruction in consecutive EPROM memory locations, describes a 20 deep subframe length.		

The first example shows the programming necessary for a subframe count of eight, a binary length. The second example shows the programming necessary for using a subframe count of other than the binary steps 32, 16, 8, 4, or 2. The second example uses an arbitrary subframe count of 20. When using a subframe count of other than the binary steps listed above, use the subcommutated data word instruction for a 32 deep subframe. The subframe counter reset word, which follows the frame ID word instruction in consecutive EPROM memory locations, is described by: 3 MSB's are all ones and the 5 LSB's are a binary representation of the number of subframes per major frame. Refer to Processor Control Sequence for further information.

SYSTEM CONFIGURATION AND TESTING

This section provides information concerning the testing which is performed on the encoder systems, the documentation required to configure and necessary information for assembling a system.

Testing

All hardware is subjected to the following three levels of testing prior to its use on an actual mission:

- °Component, system and thermal testing by the vendor.
- °Systems level acceptance testing by Wallops Flight Facility.
- °Mission specific systems functional and environmental testing.

The vendor performs a functional test on a module basis in a microprocessor controlled test set. All applicable inputs and outputs are exercised and responses are limit checked. Following the module level checks, the module's are integrated in a typical system configuration and all parameters are functionally checked again to assure module compatibility. At this point, the system is checked for proper operation over the temperature range from -35 degrees Centigrade to +85 degrees Centigrade.

Wallops Flight Facility will perform systems level functional acceptance tests on the modules to two typical configurations. All features will be performance limit checked prior to incorporating a module into the existing library of PCM components. Figure 35 shows the hardware used for testing the PCM systems.

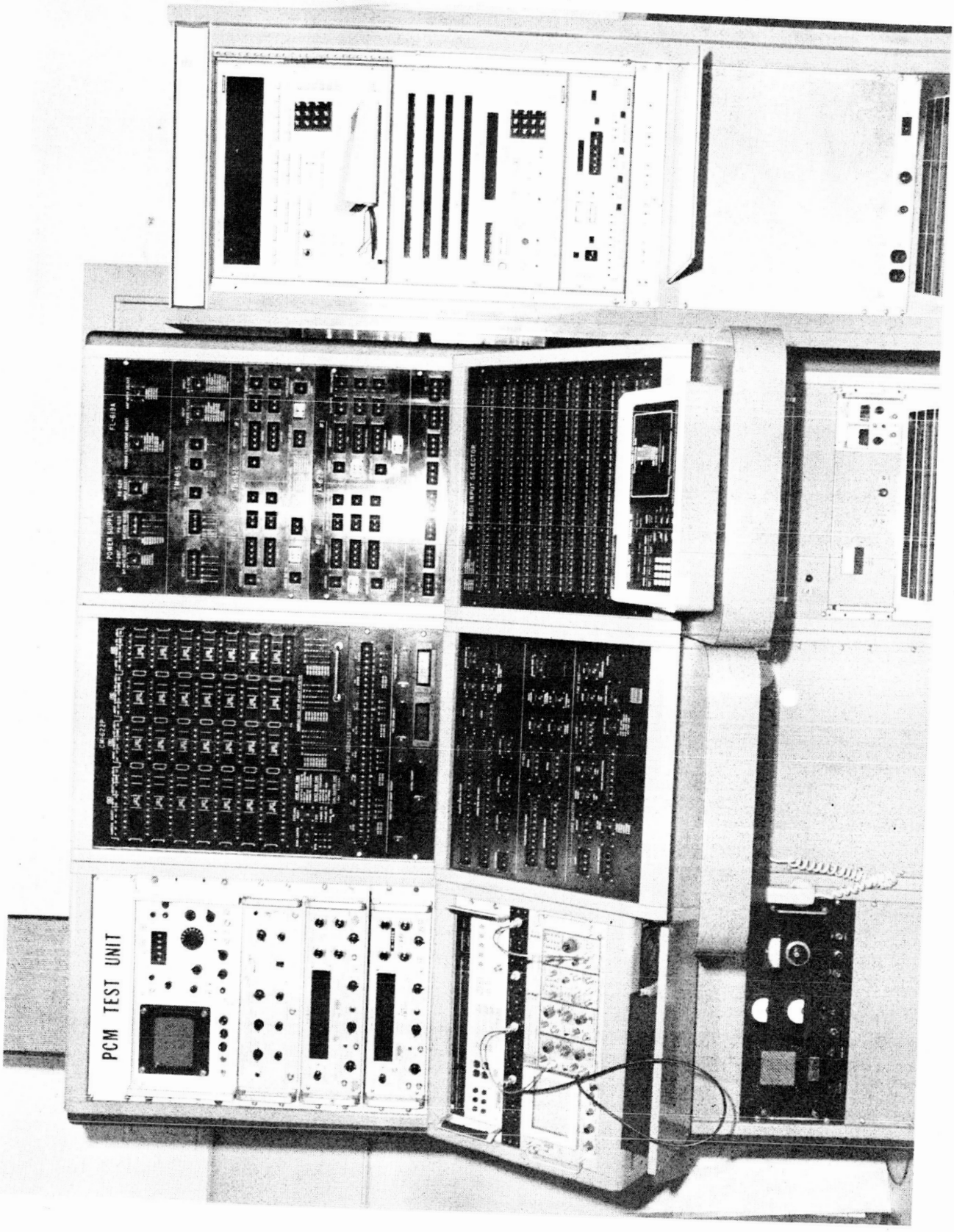


Figure 35.-Wallops Flight Facility PCM input simulator

Once a mission's requirements are defined, the required modules are selected from the library of components and assembled into a system. The EPROM is programmed for the mission format and all mission inputs are simulated while all required outputs are functionally checked and calibrated. Next, the PCM system is integrated into the payload and compatibility tests and calibrations are performed. The entire payload is then environmentally tested and the PCM system performance is monitored. Assuming no anomalies are observed, the PCM system's flight worthiness has been established.

Documentation

Necessary documentation for assembling an encoder system consists of the 9702A EPROM program, a drawing of the PCM output format, a listing of each data channel with word-frame-interval information, all outputs of the system that will be used, information specifying operational modes and hardwire addresses, the exact stacking configuration and information necessary to program the PCM decommutation system. By following the Sample Payload Configuration (presented in a following section), all of the required information will be included in the instrumentation engineers documentation package.

Configuration

CAUTION: EXTREME CARE SHOULD BE EXERCISED IN THE HANDLING OF THESE MODULES SINCE THE MATING CONNECTORS CAN BE DAMAGED IF THE CONNECTORS ARE NOT MATED PROPERLY.

WHEN CONNECTING THE MATING CONNECTORS, THE MATE SHOULD BE INSERTED WITH BOTH CONNECTORS PARALLEL AT ALL TIMES. THE RETAINING SCREWS SHOULD BE TIGHTENED ALTERNATELY ALWAYS KEEPING THE CONNECTORS PARALLEL.

CAUTION SHOULD ALSO BE EXERCISED WHILE ASSEMBLING OR DISASSEMBLING A STACK OF MODULES. THE MODULES MUST BE MAINTAINED IN A PARALLEL ORIENTATION DURING THE STACKING AND UNSTACKING PROCESS TO PREVENT FRACTURING OF THE MATING CONNECTORS.

The power supply, PX-628, must be located at the bottom of the stack. The power supply and the entire stack should be heat-sinked during operation. Next, the sample and hold amplifier and analog to digital converter, AD-606, should be located adjacent to the power supply if any analog multiplexers are to be used in the system. If no analog multiplexers are required, the AD-606 is not required. The formatter,

FM-618, should come next. If the AD-606 is not used, the FM-618 should be adjacent to the power supply. If the quad filter module, FL-619A is used, it must be located directly above the FM-618. This allows adjustment of the potentiometer in the quad filter through a slot in the formatter module. If adjustment is not required, the FL-619A can be located anywhere below the PR-614 and above the FM-618 and AD-606 combination. The timer module, TM-615P, must be above the FM-618 and the AD-606 modules. The processor, PR-614, must be located next to the end plate, EP-612, which is the top end of the stack. The analog and digital multiplexers should be located between the TM-615P and the FM-618. The multiplexers may be arranged in any desired stacking order. However, the stack should be tested in the same stack configuration in which it will be flown. Also, the multiplexer input assignments should be the same for testing and flight.

NASA Goddard Space Flight Center
Wallops Flight Facility
Wallops Island, Virginia 23337

December 1985

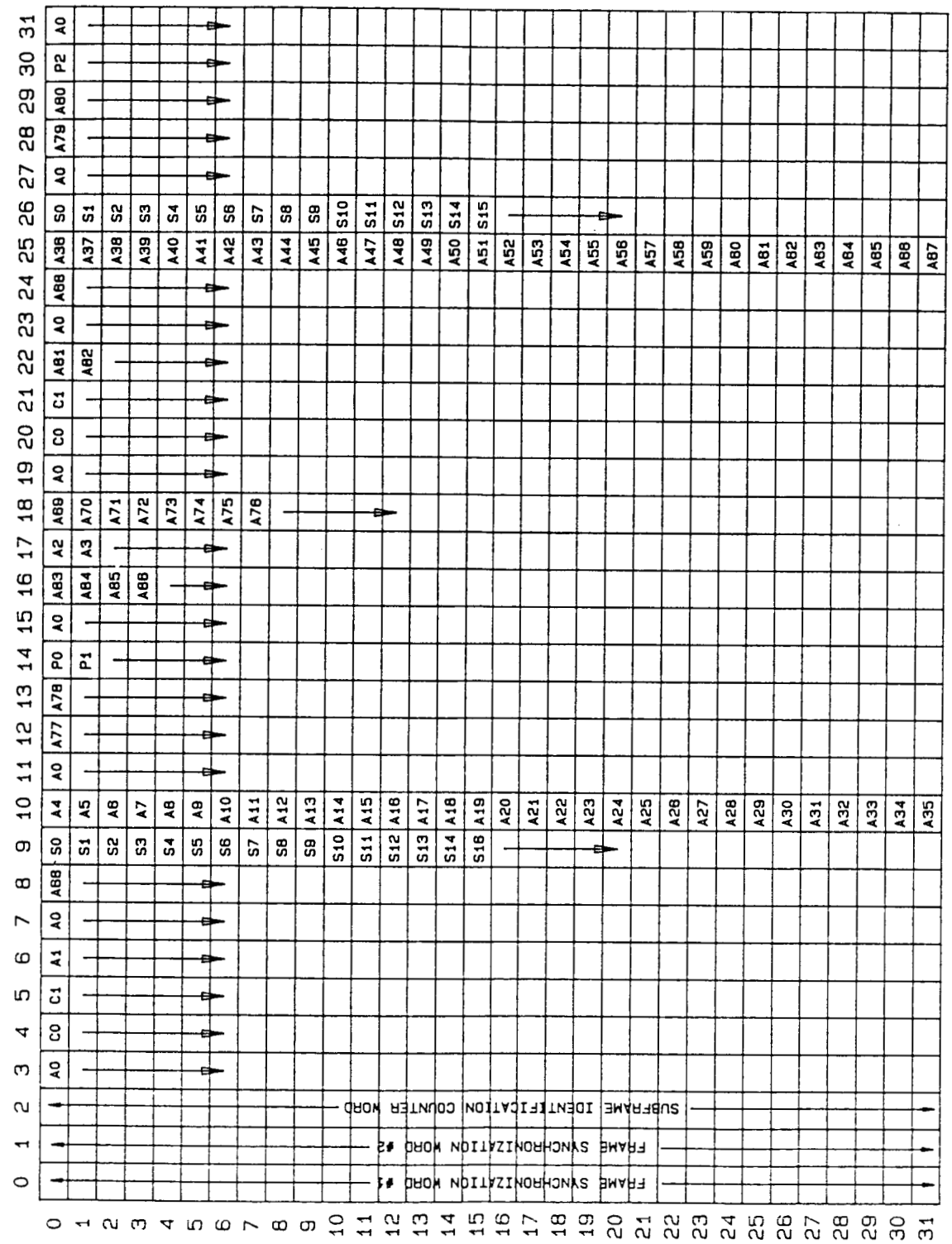
APPENDIX A. DOCUMENTATION FOR SAMPLE SYSTEM

PAYLOAD NUMBER SAMPLE

ELECTRICAL CONFIGURATION FOR WALLOPS STANDARD
MMP-600 PULSE CODE MODULATION ENCODER SYSTEM

INSTRUMENTATION ENGINEER: Stephen F. Currier

DATE 5/27/85



FRSYNC #1: 1110110111 ; FRSYNC #2: 1000100000
Bit Rate: 200 KB/S; 10 Bits/Word; 32 Words/Frame

PCM OUTPUT DATA FORMAT

Measurement	Data	User	Samples/Sec
S0	TEST	SFC	78.124
S1	TEST	SFC	78.124
S2	TEST	SFC	78.124
S3	TEST	SFC	78.124
S4	TEST	SFC	78.124
S5	TEST	SFC	78.124
S6	TEST	SFC	78.124
S7	TEST	SFC	78.124
S8	TEST	SFC	78.124
S9	TEST	SFC	78.124
S10	TEST	SFC	78.124
S11	TEST	SFC	78.124
S12	TEST	SFC	78.124
S13	TEST	SFC	78.124
S14	TEST	SFC	78.124
S15	TEST	SFC	78.124
C0	TEST	SFC	1249.98
C1	TEST	SFC	1249.98
P0	TEST	SFC	312.496
P1	TEST	SFC	312.496
P2	TEST	SFC	624.992
A0	TEST	SFC	4999.94
A1	TEST	SFC	624.99
A2	TEST	SFC	312.496
A3	TEST	SFC	312.496
A4	TEST	SFC	19.531
A5	TEST	SFC	19.531
A6	TEST	SFC	19.531
A7	TEST	SFC	19.531
A8	TEST	SFC	19.531
A9	TEST	SFC	19.531
A10	TEST	SFC	19.531
A11	TEST	SFC	19.531
A12	TEST	SFC	19.531
A13	TEST	SFC	19.531
A14	TEST	SFC	19.531
A15	TEST	SFC	19.531
A16	TEST	SFC	19.531
A17	TEST	SFC	19.531
A18	TEST	SFC	19.531
A19	TEST	SFC	19.531
A20	TEST	SFC	19.531
A21	TEST	SFC	19.531
A22	TEST	SFC	19.531
A23	TEST	SFC	19.531
A24	TEST	SFC	19.531
A25	TEST	SFC	19.531
A26	TEST	SFC	19.531
A27	TEST	SFC	19.531
A28	TEST	SFC	19.531
A29	TEST	SFC	19.531
A30	TEST	SFC	19.531
A31	TEST	SFC	19.531

Measurement	Data	User	Samples/Sec
A32	TEST	SFC	19.531
A33	TEST	SFC	19.531
A34	TEST	SFC	19.531
A35	TEST	SFC	19.531
A36	TEST	SFC	19.531
A37	TEST	SFC	19.531
A38	TEST	SFC	19.531
A39	TEST	SFC	19.531
A40	TEST	SFC	19.531
A41	TEST	SFC	19.531
A42	TEST	SFC	19.531
A43	TEST	SFC	19.531
A44	TEST	SFC	19.531
A45	TEST	SFC	19.531
A46	TEST	SFC	19.531
A47	TEST	SFC	19.531
A48	TEST	SFC	19.531
A49	TEST	SFC	19.531
A50	TEST	SFC	19.531
A51	TEST	SFC	19.531
A52	TEST	SFC	19.531
A53	TEST	SFC	19.531
A54	TEST	SFC	19.531
A55	TEST	SFC	19.531
A56	TEST	SFC	19.531
A57	TEST	SFC	19.531
A58	TEST	SFC	19.531
A59	TEST	SFC	19.531
A60	TEST	SFC	19.531
A61	TEST	SFC	19.531
A62	TEST	SFC	19.531
A63	TEST	SFC	19.531
A64	TEST	SFC	19.531
A65	TEST	SFC	19.531
A66	TEST	SFC	19.531
A67	TEST	SFC	19.531
A68	TEST	SFC	1249.98
A69	TEST	SFC	78.124
A70	TEST	SFC	78.124
A71	TEST	SFC	78.124
A72	TEST	SFC	78.124
A73	TEST	SFC	78.124
A74	TEST	SFC	78.124
A75	TEST	SFC	78.124
A76	TEST	SFC	78.124
A77	TEST	SFC	624.99
A78	TEST	SFC	624.99
A79	TEST	SFC	624.99
A80	TEST	SFC	624.99
A81	TEST	SFC	312.5
A82	TEST	SFC	312.5
A83	TEST	SFC	312.5
A84	TEST	SFC	156.25

EPROM PROGRAM

ADDRESS	DATA	COMMENT	ADDRESS	DATA	COMMENT
00	ED	FRAME SYNC #1	33	46	DATA A6
01	F8	FRAME SYNC INSTR.	34	47	DATA A7
02	88	FRAME SYNC #2	35	48	DATA A8
03	F7	SFID INSTR.	36	49	DATA A9
04	FF	SFID COUNT RESET	37	4A	DATA A10
05	40	DATA A0	38	4B	DATA A11
06	00	DATA C0	39	4C	DATA A12
07	01	DATA C1	3A	4D	DATA A13
08	41	DATA A1	3B	4E	DATA A14
09	40	DATA A0	3C	4F	DATA A15
0A	C5	DATA A68	3D	50	DATA A16
0B	F3	SUBCOM 16 INSTR.	3E	51	DATA A17
0C	53	INDIRECT ADDRESS	3F	52	DATA A18
0D	F4	SUBCOM 32 INSTR.	40	53	DATA A19
0E	31	INDIRECT ADDRESS	41	54	DATA A20
0F	40	DATA A0	42	55	DATA A21
10	CC	DATA A77	43	56	DATA A22
11	CD	DATA A78	44	57	DATA A23
12	F1	SUBCOM 4 INSTR.	45	58	DATA A24
13	65	INDIRECT ADDRESS	46	59	DATA A25
14	40	DATA A0	47	5A	DATA A26
15	F1	SUBCOM 4 INSTR.	48	5B	DATA A27
16	97	INDIRECT ADDRESS	49	5C	DATA A28
17	F0	SUBCOM 2 INSTR.	4A	5D	DATA A29
18	A1	INDIRECT ADDRESS	4B	5E	DATA A30
19	F2	SUBCOM 8 INSTR.	4C	5F	DATA A31
1A	8D	INDIRECT ADDRESS	4D	80	DATA A32
1B	40	DATA A0	4E	81	DATA A33
1C	00	DATA C0	4F	82	DATA A34
1D	01	DATA C1	50	83	DATA A35
1E	F0	SUBCOM 2 INSTR.	51		BLANK
1F	9D	INDIRECT ADDRESS	52		BLANK
20	40	DATA A0	53	10	DATA S0
21	C5	DATA A68	54	11	DATA S1
22	F4	SUBCOM 32 INSTR.	55	12	DATA S2
23	6B	INDIRECT ADDRESS	56	13	DATA S3
24	F3	SUBCOM 16 INSTR.	57	14	DATA S4
25	53	INDIRECT ADDRESS	58	15	DATA S5
26	40	DATA A0	59	16	DATA S6
27	CE	DATA A79	5A	17	DATA S7
28	CF	DATA A80	5B	20	DATA S8
29	31	DATA P2	5C	21	DATA S9
2A	40	DATA A0	5D	22	DATA S10
2B	FF	END OF FRAME INSTR	5E	23	DATA S11
2C		BLANK	5F	24	DATA S12
2D		BLANK	60	25	DATA S13
2E		BLANK	61	26	DATA S14
2F		BLANK	62	27	DATA S15
30		BLANK	63		BLANK
31	44	DATA A4	64		BLANK
32	45	DATA A5	65	30	DATA P0

EPROM PROGRAM PAGE 2

ADDRESS	DATA	COMMENT	
66	31	DATA	P1
67		BLANK	
68		BLANK	
69		BLANK	
6A		BLANK	
6B	84	DATA	A36
6C	85	DATA	A37
6D	86	DATA	A38
6E	87	DATA	A39
6F	88	DATA	A40
70	89	DATA	A41
71	8A	DATA	A42
72	8B	DATA	A43
73	8C	DATA	A44
74	8D	DATA	A45
75	8E	DATA	A46
76	8F	DATA	A47
77	A0	DATA	A48
78	A1	DATA	A49
79	A2	DATA	A50
7A	A3	DATA	A51
7B	A4	DATA	A52
7C	A5	DATA	A53
7D	A6	DATA	A54
7E	A7	DATA	A55
7F	A8	DATA	A56
80	A9	DATA	A57
81	AA	DATA	A58
82	AB	DATA	A59
83	AC	DATA	A60
84	AD	DATA	A61
85	AE	DATA	A62
86	AF	DATA	A63
87	C0	DATA	A64
88	C1	DATA	A65
89	C2	DATA	A66
8A	C3	DATA	A67
8B		BLANK	
8C		BLANK	
8D	C5	DATA	A69
8E	C6	DATA	A70
8F	C7	DATA	A71
90	C8	DATA	A72
91	C9	DATA	A73
92	CA	DATA	A74
93	CB	DATA	A75
94	CC	DATA	A76
95		BLANK	
96		BLANK	
97	D3	DATA	A83
98	D4	DATA	A84

ADDRESS	DATA	COMMENT	
99	D5	DATA	A85
9A	D3	DATA	A83
9B		BLANK	
9C		BLANK	
9D	D1	DATA	A81
9E	D2	DATA	A82
9F		BLANK	
A0		BLANK	
A1	42	DATA	A2
A2	43	DATA	A3
A3		BLANK TO	
A4		END OF	
A5		EPROM...	
A6			
A7			
A8			
A9			
AA			
AB			
AC			
AD			
AE			
AF			
B0			
B1			
B2			
B3			
B4			
B5			
B6			
B7			
B8			
B9			
BA			
BB			
BC			
BD			
BE			
BF			
C0			
C1			
C2			
C3			
C4			
C5			
C6			
C7			
C8			
C9			
CA			
CB			

EPROM PROGRAM PAGE 3

ADDRESS	DATA	COMMENT	ADDRESS	DATA	COMMENT
CC	____		FF	____	
CD	____				
CE	____				
CF	____				
D0	____				
D1	____				
D2	____				
D3	____				
D4	____				
D5	____				
D6	____				
D7	____				
D8	____				
D9	____				
DA	____				
DB	____				
DC	____				
DD	____				
DE	____				
DF	____				
E0	____				
E1	____				
E2	____				
E3	____				
E4	____				
E5	____				
E6	____				
E7	____				
E8	____				
E9	____				
EA	____				
EB	____				
EC	____				
ED	____				
EE	____				
EF	____				
F0	____				
F1	____				
F2	____				
F3	____				
F4	____				
F5	____				
F6	____				
F7	____				
F8	____				
F9	____				
FA	____				
FB	____				
FC	____				
FD	____				
FE	____				

ENCODER PARTS LIST

HEX. ADDRESS	MODEL NUMBER	PART NO.	SERIAL NO.	INPUTS USED
	PX-628	17028000-501	001	
	FM-618	17018000-519	002	
	TM-615P	17015001-519	003	
	PR-614	17014003-501	004	
	FL-619A	17019001-515	005	
	AD-606	17006003-501	006	
00 - 01	#0 CM-622P	17022003-503	007	C0 - C1
10 - 17	#0 SD-624	17024001-501	008	S0 - S7
20 - 27	#1 SD-624	17024001-501	009	S8 - S15
30 - 32	#0 PD-629	17029000-501	010	P0 - P2
40 - 5F	#0 MP-601L	17001004-510	011	A0 - A31
80 - 9F	#1 MP-601L	17001004-510	012	A32 - A64
C0 - D5	#2 MP-601L	17001004-510	013	A65 - A85

STACK CONFIGURATION

CONNECTOR NO.	MODULE MODEL NO.	HARDWIRE ADDRESS
	EP-612	
	PR-614	
P123	TM-615P	
P124	#0 SD-624	A5=0 A4=1
P125	#1 SD-624	A5=1 A4=0
P126	#0 PD-629	A5=1 A4=1 A3=0 A2=0
P127	#0 CM-622P	A5=0 A4=0 A3=0 A2=0 A1=0
P128	#0 MP-601L	A7=0 A6=1 A5=0
P129	#1 MP-601L	A7=1 A6=0 A5=0
P130	#2 MP-601L	A7=1 A6=1 A5=0
	XXX	
	XXX	
	XXX	
P131	FL-619A	USE FILTER #2 280KHZ FCO
	FM-618	
	AD-606	
P132	PX-628	A=0 B=1 C=0

MP-601L ANALOG MULTIPLEXER NUMBER: 0

SERIAL NUMBER: 011

MODULE ADDRESS

A7 0 A6 1 A5 0

ASSOCIATED INPUTS: A0 - A31

MP-601L ANALOG MULTIPLEXER NUMBER: 1

SERIAL NUMBER: 012

MODULE ADDRESS

A7 1 A6 0 A5 0

ASSOCIATED INPUTS: A32 - A64

MP-601L ANALOG MULTIPLEXER NUMBER: 2

SERIAL NUMBER: 013

MODULE ADDRESS

A7 1 A6 1 A5 0

ASSOCIATED INPUTS: A64 - A86

MP-601L ANALOG MULTIPLEXER NUMBER: _____

SERIAL NUMBER: _____

MODULE ADDRESS

A7_____ A6_____ A5_____

ASSOCIATED INPUTS: _____

PD-629 PARALLEL DIGITAL DATA MULTIPLEXER NUMBER: 0

SERIAL NUMBER: 010

MODULE ADDRESS

A5 1 A4 1 A3 0 A2 0

CHECK THE BITS BEING USED IN RESPECTIVE WORDS.

WORD NUMBER	BIT NUMBER									
	1	2	3	4	5	6	7	8	9	10
1	X	X	X	X	X	X	X	X	X	X
2	X	X	X	X	X	X	X	X	X	X
3	X	X	X	X	X					

BIT 1 IS LSB AND BIT 10 IS MSB.

SD-624 SERIAL DIGITAL DATA MULTIPLEXER NUMBER: 0

SERIAL NUMBER: 008

MODULE ADDRESS

A5 0 A4 1

INPUT NUMBER	DATA
INPUT 0	S0
INPUT 1	S1
INPUT 2	S2
INPUT 3	S3
INPUT 4	S4
INPUT 5	S5
INPUT 6	S6
INPUT 7	S7

Is the SD-624 being read out in two consecutive words?

YES _____ NO X

If YES, how many bits are to be shifted out in a series?

_____ BITS

C-2

SD-624 SERIAL DIGITAL DATA MULTIPLEXER NUMBER: 1

SERIAL NUMBER: 009

MODULE ADDRESS

A5 1 A4 0

INPUT NUMBER	DATA
INPUT 0	S8
INPUT 1	S9
INPUT 2	S10
INPUT 3	S11
INPUT 4	S12
INPUT 5	S13
INPUT 6	S14
INPUT 7	S15

Is the SD-624 being read out in two consecutive words?

YES _____ NO X

If YES, how many bits are to be shifted out in a series?

_____ BITS

CM-622P DUAL COUNTER/ACCUMULATOR NUMBER: 0

SERIAL NUMBER: 007

MODULE ADDRESS

A5 0 A4 0 A3 0 A2 0 A1 0

WORD LENGTH

A 0 B 0

Bits/Word	Word Length Code A	B
8	1	1
9	0	1
10	0	0

COUNTER MODE: DUAL X CASCADE

RESET MODE COUNTER 0: #2

RESET MODE COUNTER 1: #2

1. EXTERNAL RESET PULSE
2. RESET ON READ
3. OVERFLOW
4. OVERFLOW COMPLIMENT
5. EXTERNAL RESET PULSE COMPLIMENT

INPUT	DATA
COUNTER 0	C0
COUNTER 1	C1

TA-623 TIME EVENT MONITOR WITH ALTERNATING REGISTERS

SERIAL NUMBER: _____

MODULE ADDRESS

A3_____ ("1" NOMINAL)

INPUT	DATA
EVENT 0	_____
EVENT 1	_____

TB-625 TIME EVENT MONITOR AND TIMING BUFFERS NUMBER:_____

SERIAL NUMBER: _____

MODULE ADDRESS

A3_____

INPUT	DATA
EVENT 0	_____
EVENT 1	_____

GROUP I MODULE OUTPUTS REQUIRED FOR THE MISSION.
(INSTRUMENTATION ENGINEER CHECK ONLY THOSE REQUIRED)

POWER SUPPLY PX-628

25 KBIT CLOCK _____ CRYSTAL OSCILLATOR ±0.02% STABILITY

50 KBIT CLOCK _____ CRYSTAL OSCILLATOR ±0.02% STABILITY

100 KBIT CLOCK _____ CRYSTAL OSCILLATOR ±0.02% STABILITY

200 KBIT CLOCK __X__ CRYSTAL OSCILLATOR ±0.02% STABILITY

400 KBIT CLOCK _____ CRYSTAL OSCILLATOR ±0.02% STABILITY

800 KBIT CLOCK _____ CRYSTAL OSCILLATOR ±0.02% STABILITY

1600 KBIT CLOCK _____ CRYSTAL OSCILLATOR ±0.02% STABILITY

PX-628 output are CMOS operated at +5.0 volts. The simulator unit buffers them with TTL logic operated on +5.0 volts.

TIMER TM-615P

OUTPUT	PIN NO.	REQUIRED
NRZ-L	1	
Bi-Ø-L	2	
NRZ-L PRIMARY	4	
MAJOR FRAME	5	X
Bi-Ø-L	6	X
PREMOD FILTER	8	
INVERTED 2X BIT CLOCK	9	
2X BIT CLOCK	10	
Bi-Ø/NRZ OUTPUT	20	
INVERTED Bi-Ø/NRZ OUTPUT	21	
BIT CLOCK	23	
MINOR FRAME SYNC.	24	

TIMER TM-615P

OUTPUT	PIN NO.	REQUIRED
WORD CLOCK	25	X
BIT CLOCK	26	X

All TM-615P outputs are CMOS operated on +5.0 volts. The simulator buffers all outputs above with TTL logic operated on +5.0 volts.

PD-629 PARALLEL DIGITAL DATA MULTIPLEXER NUMBER: 0

CHECK OUTPUTS REQUIRED FOR THE MISSION.

WORD 0 ENABLE X

WORD 1 ENABLE

SD-624 SERIAL DIGITAL DATA MULTIPLEXER NUMBER: 0

CHECK OUTPUTS REQUIRED FOR THE MISSION.

ENABLE 0	X	INVERTED LOAD 0	X	GATED BIT CLOCK 0	X
ENABLE 1	X	INVERTED LOAD 1	X	GATED BIT CLOCK 1	X
ENABLE 2	X	INVERTED LOAD 2	X	GATED BIT CLOCK 2	X
ENABLE 3	X	INVERTED LOAD 3	X	GATED BIT CLOCK 3	X
ENABLE 4	X	INVERTED LOAD 4	X	GATED BIT CLOCK 4	X
ENABLE 5	X	INVERTED LOAD 5	X	GATED BIT CLOCK 5	X
ENABLE 6	X	INVERTED LOAD 6	X	GATED BIT CLOCK 6	X
ENABLE 7	X	INVERTED LOAD 7	X	GATED BIT CLOCK 7	X

SD-624 SERIAL DIGITAL DATA MULTIPLEXER NUMBER: 1

CHECK OUTPUTS REQUIRED FOR THE MISSION.

ENABLE 0	X	INVERTED LOAD 0	X	GATED BIT CLOCK 0	X
ENABLE 1	X	INVERTED LOAD 1	X	GATED BIT CLOCK 1	X
ENABLE 2	X	INVERTED LOAD 2	X	GATED BIT CLOCK 2	X
ENABLE 3	X	INVERTED LOAD 3	X	GATED BIT CLOCK 3	X
ENABLE 4	X	INVERTED LOAD 4	X	GATED BIT CLOCK 4	X
ENABLE 5	X	INVERTED LOAD 5	X	GATED BIT CLOCK 5	X
ENABLE 6	X	INVERTED LOAD 6	X	GATED BIT CLOCK 6	X
ENABLE 7	X	INVERTED LOAD 7	X	GATED BIT CLOCK 7	X

SYSTEM PROGRAMMING PARAMETERS

POWER SUPPLY PX-628 SERIAL NO. 001

BIT RATE: 200 KBIT/SEC

INTERNAL: YES EXTERNAL: _____

SYSTEM BIT RATE: A 0 B 1 C 0

TIMER TM-615P SERIAL NO. 003

SELECT BI-Ø (0)_____ or NRZ (1)_____

SELECT Mark (0)_____ or Space (1)_____

Connect the bit synthesizer to the output which will be used for flight. If premod filter is to be used, select the proper input.

PARITY ODD (0)_____ or NONE (1) X

TOTAL BITS/WORD B4 1 B3 0 B2 0 B1 1

SAMPLE DURATION S3 0 S2 1 S1 1

Bits/Word Codes

Bits/Word	B4	B3	B2	B1
8	0	1	1	1
9	1	0	0	0
10	1	0	0	1

Sample Duration Codes

Duration	S3	S2	S1
1 1/2 Bits	0	0	1
2 1/2 Bits	0	1	0
3 1/2 Bits	0	1	1
4 1/2 Bits	1	0	0
5 1/2 Bits	1	0	1

INFORMATION REQUIRED TO SYNCHRONIZE AND DECOMMUTATE DATA FOR THE ENCODER SYSTEM

BIT SYNCHRONIZER

BIT RATE: 200 KBIT/SEC

OUTPUT CODE: Bi-Φ-L

INVERTED: _____ NORMAL: X

FRAME SYNCHRONIZER

FRAME SYNC PATTERN

1 1 1 0 1 1 0 1 1 1 1 0 0 0 1 0 0 0 0 0 _ _ _ _ _ _ _ _ _ _ _ _

FBT LBT

PATTERN LENGTH 20 BITS.

STRATEGY _____ _____BIT WINDOW

ACCEPT ANY ERRORS PER FRAME? YES ____ NO X

VERIFY 1 PATTERN(S) TO PROCEED FROM VERIFY TO LOCK.

NUMBER OF BITS/FRAME 320 INCLUDING FRAME SYNC WORDS.

MSBF X LSBF _____

WORD LENGTH 10 BITS.

NUMBER OF DATA WORDS/FRAME 30 EXCLUDING FRAME SYNC WORDS.

SUBFRAME SYNCHRONIZER

ARE THERE ANY SUBFRAMES? YES X NO _____

IS SUBFRAME IDENTIFICATION COUNTER USED? YES X NO _____

DOES SUBFRAME ID COUNTER COUNT UP OR DOWN? UP X DOWN _____

SUBFRAME LENGTH 32 WORDS.

NUMBER OF BIT ERRORS ACCEPTED IN PATTERN? 1

BIT NUMBER OF MSB OF SUBFRAME IDENTIFICATION COUNTER? 4

SUBFRAME SYNCHRONIZER (CONTINUED)

IDENTIFICATION COUNTER LENGTH 5 BITS.

MSBF IDENTIFICATION COUNT BIT ALIGNMENT? YES X NO _____

INITIAL IDENTIFICATION COUNT? 0

WORD SELECTOR

NUMBER OF BITS/WORD? 10

MSBF X OR LSBF _____

IS PARITY USED? YES _____ NO X

APPENDIX B. PROGRAMMING CODES QUICK REFERENCE AND EXTERNAL CONNECTOR PIN OUTPUT LIST

RECOMMENDED FRAME
SYNCHRONIZATION PATTERNS

NUMBER OF BITS									
7	101	100	0						
8	101	110	00						
9	101	110	000						
10	110	111	000	0					
11	101	101	110	00					
12	110	101	100	000					
13	111	010	110	000	0				
14	111	001	101	000	00				
15	111	011	001	010	000				
16	111	010	111	001	000	0			
17	111	100	110	101	000	00			
18	111	100	110	101	000	000			
19	111	110	011	001	010	000	0		
20	111	011	011	110	001	000	00		
21	111	011	101	001	011	000	000		
22	111	100	110	110	101	000	000	0	
23	111	101	011	100	110	100	000	00	
24	111	110	101	111	001	100	100	000	
25	111	110	010	110	111	000	100	000	0
26	111	110	100	110	101	100	010	000	00
27	111	110	101	101	001	100	110	000	000
28	111	101	011	110	010	110	011	000	000	0
29	111	101	011	110	011	001	101	000	000	00
30	111	110	101	111	001	100	110	100	000	000

TABLE 19

PROGRAMMING CODES QUICK REFERENCE

EPROM Instruction Codes to be used in the EPROM program.

Instruction	A7	A6	A5	A4	A3	A2	A1	AØ	HEX.	Comments
End of Frame	1	1	1	1	1	1	1	1	FF	Bits A1, AØ are stored for insertion into bit 9 and 1Ø position of first frame sync word for 9 and 1Ø bit systems
	1	1	1	1	1	1	1	Ø	FE	
	1	1	1	1	1	1	Ø	1	FD	
	1	1	1	1	1	1	Ø	Ø	FC	
Frame Sync. Word	1	1	1	1	1	Ø	1	1	FB	Bits A1, AØ are stored for insertion into bit 9 and 1Ø position of first frame sync word for 9 and 1Ø bit systems
	1	1	1	1	1	Ø	1	Ø	FA	
	1	1	1	1	1	Ø	Ø	1	F9	
	1	1	1	1	1	Ø	Ø	Ø	F8	
Frame ID Word	1	1	1	1	Ø	1	1	1	F7	
									F6	Reserved Do Not Use
									F5	Reserved Do Not Use
Subcommutated Data Word	1	1	1	1	Ø	1	Ø	Ø	F4	32 Deep Subframe
	1	1	1	1	Ø	Ø	1	1	F3	16 Deep Subframe
	1	1	1	1	Ø	Ø	1	Ø	F2	8 Deep Subframe
	1	1	1	1	Ø	Ø	Ø	1	F1	4 Deep Subframe
	1	1	1	1	Ø	Ø	Ø	Ø	FØ	2 Deep Subframe

Program A Pin 15	Program B Pin 14	Program C Pin 13	Bit Rate Kbit/sec
Ø	Ø	Ø	8ØØ
1	Ø	Ø	4ØØ
Ø	1	Ø	2ØØ
1	1	Ø	1ØØ
Ø	Ø	1	5Ø
1	Ø	1	25
Ø	1	1	12.5
1	1	1	6.25

Power Supply PX-628 Bit Rate Programming Codes - These programming codes are to be used at the modules external connector. "Ø"=Grounded Pin, "1"=Open Pin.

Power Supply PX-628 External Clock Frequencies

		Bit Rate Program							
Word Length	Prog A	0	1	0	1	0	1	0	1
	Prog B	0	0	1	1	0	0	1	1
	Prog C	0	0	0	0	1	1	1	1
		External Clock Frequencies (In MHz)							
8 Bits/Word		1.2 to 2.0	1.2 to 3.2	→	→	→	→	→	→
9 Bits/Word		1.4 to 2.0	1.4 to 3.2	→	→	→	→	→	→
10 Bits/Word		1.6 to 2.0	1.6 to 3.2	→	→	→	→	→	→
Resulting bit rate expressed as fraction of external clock.		1/2	1/4	1/8	1/16	1/32	1/64	1/128	1/256

TM-615P Programming Codes - These programming codes are to be used at the external connector of the module.
"0" = Grounded Pin "1" = Open Programming Pin

TM-615P Bits per Word Programming Codes

	Programming Pins			
Bits/Word	B4 (Pin 14)	B3 (Pin 12)	B2 (Pin 13)	B1 (Pin 15)
8	0	1	1	1
9	1	0	0	0
10	1	0	0	1

TM-615P Parity Select Programming Codes

Parity Select	Pin Number 11
Odd Parity	1
No Parity	0

RECOMMENDED SAMPLE DURATIONS

Bits/Word	Sample Width
8	2 1/2 Bits
9	3 1/2 Bits
10	3 1/2 Bits

TM-615P Sample Duration Programming Codes

	Programming Pins		
Sample Duration	S3 (Pin 17)	S2 (Pin 16)	S1 (Pin 18)
1 1/2 Bits	0	0	1
2 1/2 Bits	0	1	0
3 1/2 Bits	0	1	1
4 1/2 Bits	1	0	0
5 1/2 Bits	1	0	1

TM-615P Coded Output Programming Codes

Coded Output	Bi-Ø/NRZ Select (Pin 3)	Mark/Space Select (Pin 22)
Bi-Ø-M	0	0
Bi-Ø-S	0	1
NRZ-M	1	0
NRZ-S	1	1

EPROM Programming Codes for Selecting Data Channels
These programming codes are to be used in the EPROM program.

MODULE NAME	ADDRESS LINE A7	A6	A5	A4	A3	A2	A1	A0	CHANNELS PER MODULE	MAXIMUM NO. OF MODULES PER SYSTEM
MP-601	M	M	M	C	C	C	C	C	32	8
PD-629	0	0	M	M	M	M	C	C	3	16
SD-624	0	0	M	M	X	C	C	C	8	4
CM-622P	0	0	M	M	M	M	M	C	2	19
TA-623	SEE TABLE 13								2	1
TB-625	SEE TABLE 13								2	2

M = Module select bit
C = Channel select
0 = Must program a "0"
X = Don't Care

SD-624 Serial Digital Data Multiplexer Channel Programming -
These codes are to be used in the EPROM program.

Input Channel	Pin No.	A7	A6	A5	A4	A3	A2	A1	A0
0	27	0	0	M	M	X	0	0	0
1	8	0	0	M	M	X	0	0	1
2	26	0	0	M	M	X	0	1	0
3	7	0	0	M	M	X	0	1	1
4	1	0	0	M	M	X	1	0	0
5	20	0	0	M	M	X	1	0	1
6	2	0	0	M	M	X	1	1	0
7	21	0	0	M	M	X	1	1	1

X = Don't Care; M = Address lines used for module selection.

SD-624 Word Length Programming - These programming codes are to be used at the external connector of the module. "0"= Grounded programming pin, "1"= Open programming pin.

Word Length	Program A Pin 9	Program B Pin 11
8 Bits	0	1
9 Bits	1	0
10 Bits	0	0

PD-629 Channel Programming Codes - These codes are to be used in the EPROM program.

Channel No.	Pin Numbers	A7	A6	A5	A4	A3	A2	A1	A0
0	2,22,5,25,8, 28,11,31,14,34	0	0	M	M	M	M	0	0
1	20,3,23,6,26, 9,29,12,32,15	0	0	M	M	M	M	0	1
2	1,21,4,24,7, 27,10,30,13,33	0	0	M	M	M	M	1	1

M = Address lines used for module selection.

CM-622 Counter/Accumulator Address Programming Codes - These codes are to be used in the EPROM program.

Channel	Pin No.	A7	A6	A5	A4	A3	A2	A1	A0
0	4	0	0	M	M	M	M	M	0
1	5	0	0	M	M	M	M	M	1

M= Address lines used for module

CM-622P Word Length Programming Codes - These codes are to be used at the external connector of the module. "0"= Grounded programming pin, "1" Open programming pin.

Word Length	Program A Pin 6	Program B Pin 11
8 Bits	1	1
9 Bits	0	1
10 Bits	0	0

CM-622P Reset Mode Programming Codes - These codes are to be used at the external connector of the module. "0"= Grounded programming pin, "1"= Open programming pin.

Counter 0 Input Pin 7	Counter 1 Input Pin 12	Pin 15	Mode
Jump to Pin 9	Jump to Pin 10	1	Automatic
Positive External Pulse	Positive External Pulse	0	External
Negative External Pulse	Negative External Pulse	1	External
0	0	0	Overflow
1	1	1	Overflow

TA-623 and TB-625 Programming Codes - These codes are to be used in the EPROM program.

Module	Register	Word	A7	A6	A5	A4	A3	A2	A1	A0	Hex. Code	Module No.
TA-623	1	1	1	1	0	1	1	0	0	0	D8	1
		2	1	1	0	1	1	0	0	1	D9	
	2	1	1	1	0	1	1	0	1	0	DA	
		2	1	1	0	1	1	0	1	1	DB	
	3	1	1	1	0	1	1	1	0	0	DC	
		2	1	1	0	1	1	1	0	1	DD	
TB-625	1	1	1	1	0	0	1	0	0	0	C8	1
		2	1	1	0	0	1	0	0	1	C9	
	2	1	1	1	0	0	1	0	1	0	CA	
		2	1	1	0	0	1	0	1	1	CB	
	1	1	1	1	0	0	0	0	0	0	C0	2
		2	1	1	0	0	0	0	0	1	C1	
	2	1	1	1	0	0	0	0	1	0	C2	
		2	1	1	0	0	0	0	1	1	C3	

MP-601L Analog Multiplexer Channel Programming - These codes are to be used in the EPROM program.

Channel No.	Pin No.	A7	A6	A5	A4	A3	A2	A1	A0
0	20	M	M	M	0	0	0	0	0
1	1	M	M	M	0	0	0	0	1
2	2	M	M	M	0	0	0	1	0
3	21	M	M	M	0	0	0	1	1
4	3	M	M	M	0	0	1	0	0
5	22	M	M	M	0	0	1	0	1
6	4	M	M	M	0	0	1	1	0
7	23	M	M	M	0	0	1	1	1
8	24	M	M	M	0	1	0	0	0
9	5	M	M	M	0	1	0	0	1
10	6	M	M	M	0	1	0	1	0
11	25	M	M	M	0	1	0	1	1
12	7	M	M	M	0	1	1	0	0
13	26	M	M	M	0	1	1	0	1
14	8	M	M	M	0	1	1	1	0
15	27	M	M	M	0	1	1	1	1
16	28	M	M	M	1	0	0	0	0
17	9	M	M	M	1	0	0	0	1
18	10	M	M	M	1	0	0	1	0
19	29	M	M	M	1	0	0	1	1
20	11	M	M	M	1	0	1	0	0
21	30	M	M	M	1	0	1	0	1
22	12	M	M	M	1	0	1	1	0
23	31	M	M	M	1	0	1	1	1
24	32	M	M	M	1	1	0	0	0
25	13	M	M	M	1	1	0	0	1
26	14	M	M	M	1	1	0	1	0
27	33	M	M	M	1	1	0	1	1
28	15	M	M	M	1	1	1	0	0
29	34	M	M	M	1	1	1	0	1
30	16	M	M	M	1	1	1	1	0
31	35	M	M	M	1	1	1	1	1

M = Address lines used for module selection.

PX-628 Power Supply External Pin Connections

1. 800 Kbit/sec Clock Output
2. 1600 Kbit/sec Clock Output
3. 50 Kbit/sec Clock Output
4. 100 Kbit/sec Clock Output
5. 400 Kbit/sec Clock Output
6. 200 Kbit/sec Clock Output
7. 25 Kbit/sec Clock Output
8. GROUND
9. Chassis Ground
10. External Clock Input
11. +28 Volt DC Power Input
12. Power Ground
13. Bit Rate Program C
14. Bit Rate Program B
15. Bit Rate Program A

Table 20.

TM-615P Timer External Pin Connections

1. NRZ-L Output from 4049
2. Bi-Ø-L Output from 4049
3. Bi-Ø/NRZ Select
4. NRZ-L Primary Output from 4050
5. Major Frame Sync Output from 4050
6. Bi-Ø-L Primary Output from 4050
7. Premodulation Filter Input to 4049
8. Premodulation Filter Output from CF 2515
9. Inverted 2X Bit Clock (0 to +10 Volt) from 4041
10. 2X Bit Clock Output (0 to +10 Volt) from 4041
11. Parity Enable Select
12. B3 Program Bits per Word Select
13. B2 Program Bits per Word Select
14. B4 Program Bits per Word Select
15. Bl Program Bits per Word Select
16. S2 Program Sample Duration Select
17. S3 Program Sample Duration Select
18. Sl Program Sample Duration Select
19. Digital Ground
20. Bi-Ø/NRZ Mark or Space Coded Output from 4049
21. Inverted Coded Output from 4049
22. Mark/Space Select
23. Inverted Bit Clock Output from 4049
24. Minor Frame Sync Output from 4050
25. Word Clock Output from 4050
26. Bit Clock Output from 4050
27. No Connection
28. No Connection
29. No Connection
30. No Connection
31. No Connection
32. No Connection
33. No Connection
34. No Connection
35. No Connection
36. No Connection
37. No Connection

Table 21.

MP-601L 32 Channel High Level Analog Multiplexer
External Pin Connections

1.	Analog Channel A1	20.	Analog Channel A0
2.	Analog Channel A2	21.	Analog Channel A3
3.	Analog Channel A4	22.	Analog Channel A5
4.	Analog Channel A6	23.	Analog Channel A7
5.	Analog Channel A9	24.	Analog Channel A8
6.	Analog Channel A10	25.	Analog Channel A11
7.	Analog Channel A12	26.	Analog Channel A13
8.	Analog Channel A14	27.	Analog Channel A15
9.	Analog Channel A17	28.	Analog Channel A16
10.	Analog Channel A18	29.	Analog Channel A19
11.	Analog Channel A20	30.	Analog Channel A21
12.	Analog Channel A22	31.	Analog Channel A23
13.	Analog Channel A25	32.	Analog Channel A24
14.	Analog Channel A26	33.	Analog Channel A27
15.	Analog Channel A28	34.	Analog Channel A29
16.	Analog Channel A30	35.	Analog Channel A31
17.	Analog Ground	36.	Program A5
18.	Program A6	37.	No Connection
19.	Program A7		

Table 22.

PD-629 30 Input Parallel Digital Data Multiplexer
External Pin Connections

1. Word 2 Bit 0
2. Word 0 Bit 0
3. Word 1 Bit 1
4. Word 2 Bit 2
5. Word 0 Bit 2
6. Word 1 Bit 3
7. Word 2 Bit 4
8. Word 0 Bit 4
9. Word 1 Bit 5
10. Word 2 Bit 6
11. Word 0 Bit 6
12. Word 1 Bit 7
13. Word 2 Bit 8
14. Word 0 Bit 8
15. Word 1 Bit 9
16. Program A3
17. Program A2
18. Word 0 Enable
19. GROUND
20. Word 1 Bit 0
21. Word 2 Bit 1
22. Word 0 Bit 1
23. Word 1 Bit 2
24. Word 2 Bit 3
25. Word 0 Bit 3
26. Word 1 Bit 4
27. Word 2 Bit 5
28. Word 0 Bit 5
29. Word 1 Bit 6
30. Word 2 Bit 7
31. Word 0 Bit 7
32. Word 1 Bit 8
33. Word 2 Bit 9
34. Word 0 Bit 9
35. Word 1 Enable
36. Program A5
37. Program A4

Bit 9 is the MSB and bit 0 is the LSB in the parallel words listed above. Pins 16, 17, 36 and 37 are used to assign an address to each PD-629 module.

Table 23.

SD-624 Serial Digital Data Multiplexer
External Pin Connections

1. Input S4	20. Input S5
2. Input S6	21. Input S7
3. Gated Clock 7	22. Gated Clock 6
4. Gated Clock 5	23. Gated Clock 4
5. Gated Clock 3	24. Gated Clock 2
6. Gated Clock 1	25. Gated Clock 0
7. Input S3	26. Input S2
8. Input S1	27. Input S0
9. Word Length Program A	28. Module Select Program A4
10. GROUND	29. Module Select Program A5
11. Word Length Program B	30. Inverted Load 2
12. Inverted Load 3	31. Inverted Load 0
13. Inverted Load 1	32. Inverted Load 6
14. Enable 7	33. Enable 6
15. Enable 5	34. Enable 4
16. Enable 3	35. Enable 1
17. Enable 2	36. Enable 0
18. Inverted Load 5	37. Inverted Load 4
19. Inverted Load 7	

Table 24.

CM-622P Dual Counter/Accumulator External Pin Connections

1. No Connection
2. No Connection
3. Program A1
4. Counter 0 Input
5. Counter 1 Input
6. Word Length Program A
7. Counter 0 Reset Input
8. No Connection
9. Counter 0 Internal Reset Output
10. Counter 1 Internal Reset Output
11. Word Length Program B
12. Counter 1 Reset Input
13. Program A4
14. Program A5
15. Compliment Reset
16. Counter Mode Control
17. Program A2
18. Program A3
19. Digital Ground
20. No Connection
21. No Connection
22. No Connection
23. No Connection
24. No Connection
25. No Connection
26. No Connection
27. No Connection
28. No Connection
29. No Connection
30. No Connection
31. No Connection
32. No Connection
33. No Connection
34. No Connection
35. No Connection
36. No Connection
37. No Connection

Pins numbers 3, 13, 14, 17 and 18 are used to assign an address to each counter module. Word length must be programmed at pin numbers 6 and 11.

Table 25.

TA-623 External Pin Connections

1. Event 1 Input (Alternating Registers)
2. Minor Frame Sync. Output
3. Major Frame Sync. Output
4. Bit Clock Output
5. Word Clock Output
6. Event 0 Input
7. 2X Bit Clock Output
8. A3 Programming Pin
9. GROUND

The A3 programming Pin is used for module selection of the TB-625 Time Event monitor, so this programming pin will always be left open or programmed for a logic "1". For more information concerning the channel addressing codes, see tables 15 through 17.

Table 26.

External Pin Connections

1. Event 0 Input
2. Minor Frame Sync. Output
3. Major Frame Sync. Output
4. Bit Clock Output
5. Word Clock Output
6. Minor Frame Counter Output (Bit 2^4)
7. Word per Frame Counter Output (Bit 2^1)
8. Word per Frame Counter Output (Bit 2^4)
9. Word per Frame Counter Output (Bit 2^5)
10. Word per Frame Counter Output (Bit 2^3)
11. Word per Frame Counter Output (Bit 2^0)
12. Word per Frame Counter Output (Bit 2^2)
13. 2X Bit Clock Output
14. Word per Frame Counter Output (Bit 2^6)
15. Word per Frame Counter Output (Bit 2^7)
16. Minor Frame Counter Output (Bit 2^0)
17. Minor Frame Counter Output (Bit 2^1)
18. Minor Frame Counter Output (Bit 2^3)
19. GROUND
20. Event 0 Input
21. No Connection
22. No Connection
23. No Connection
24. No Connection
25. No Connection
26. No Connection
27. No Connection
28. No Connection
29. No Connection
30. No Connection
31. No Connection
32. No Connection
33. No Connection
34. No Connection
35. No Connection
36. Minor Frame Counter Output (Bit 2^2)
37. A3 Programming Pin

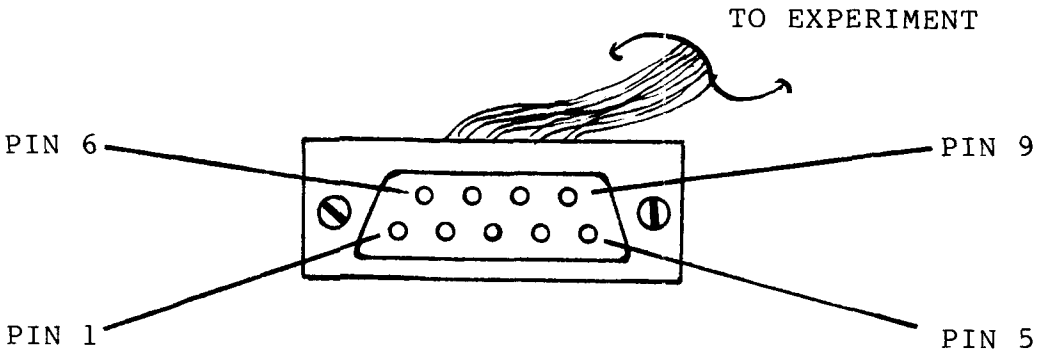
Table 27.

FL-619A Quad Filter External Pin Connections

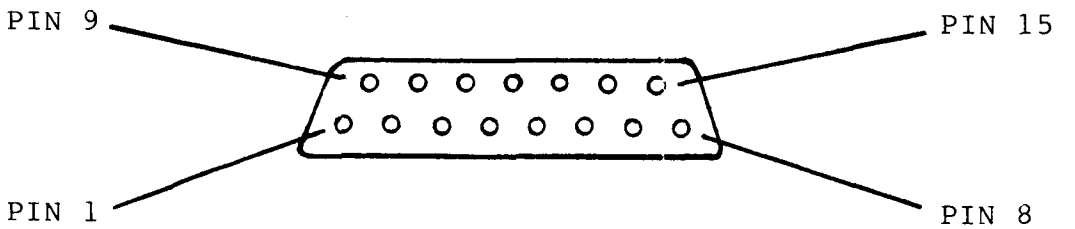
1. Input to Output Amplifier (Signal Conditioner Input)
2. Filtered Adjustable Output (Conditioned Output)
3. GROUND
4. Filter #3 Output
5. Filter #1 Output
6. Input to Filters (PCM From Timer Module TM-615P)
7. No Connection
8. Filter #4 Output
9. Filter #2 Output

The appropriate filter output can be connected to pin 1 for adjustable voltage amplitude output. The final filtered output is output on pin 2. This output can be used to directly modulate a transmitter.

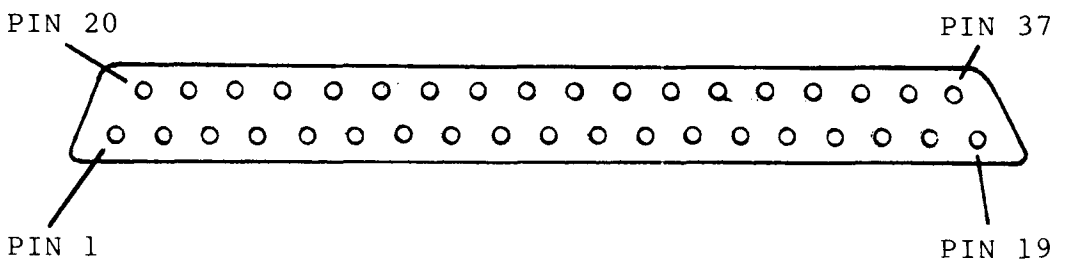
Table 28.



ITT CANNON MDM-9S SOCKET CONNECTOR



ITT CANNON MDM-15S SOCKET CONNECTOR



ITT CANNON MDM-37S SOCKET CONNECTOR

EXTERNAL CONNECTORS MATING SOCKETS VIEW LOOKING INTO THE MATING SURFACE OF THE SOCKET CONNECTORS.

Figure 32.

ABSTRACT

This document describes the hardware and software characteristics of a time division multiplex system. The system is used to sample analog and digital data. The data is merged with synchronization information to produce a serial pulse coded modulation (PCM) bit stream.

Information presented herein is required by users to design compatible interfaces and assure effective utilization of this encoder system.

GSFC/Wallops Flight Facility has flown approximately 50 of these systems, through 1984, on sounding rockets with no inflight failures. Aydin Vector manufactures all of the components for these systems.

GLOSSARY OF TERMS

For the purpose of discussion, some terms must be defined. These definitions may not be universally agreed upon but should suffice for the purpose of communicating the required information.

BIT. A bit is the smallest unit of information used in this system. It consists of an on or off condition, effectively, yes or no.

FRAME. A frame begins with the frame synchronization pattern and continues up to, but not including, the next frame synchronization pattern.

MAINFRAME RATE. One sample per minor frame in a subcommutated format is a mainframe sampling rate and one sample in a major frame if subcommutation is not used is also a mainframe sampling rate.

MAJOR FRAME. A major frame is made up of multiple minor frames in a subcommutated format. One complete sampling history is contained in one major frame.

MINOR FRAME. Minor frames appear when subcommutation is used. A minor frame begins with the frame synchronization pattern and continues up to, but not including, the next frame synchronization pattern. In effect, a minor frame is equal to a frame in length and is present only when subcommutation is used. Minor frames are sometimes referred to as subframes.

SUBCOMMUTATED DATA. This is data sampled at a rate less than the mainframe sampling rate. A subcommutated data channel is not sampled in every minor frame.

SUPERCOMMUTATED DATA. This is data that is sampled at a rate greater than the mainframe rate. Supercommutated data is sampled more than one time per minor frame in a subcommutated format and is sampled more than one time per frame if subcommutation is not used.

WORD. A word contains 8, 9 or 10 bits of data. The value of the word experesses the value of a single channel of data. The system uses the binary number system so the maximum value of an 8-bit word is 256 and so on.

For a graphical representation of these terms, refer to Figure 5, Sample Data Format.

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