A Comparison of Methods for DPLL Loop Filter Design

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Four design methodologies for loop filters for a class of digital phase-locked loops (DPLLs) are presented. The first design maps an optimum analog filter into the digital domain; the second approach designs a filter that minimizes in discrete time a weighted combination of the variance of the phase error due to noise and the sum square of the deterministic phase error component; the third method uses Kalman filter estimation theory to design a filter composed of a least squares fading memory estimator and a predictor. The last design relies on classical control theory, including rules for the design of compensators. Linear analysis is used throughout the article to compare different designs, and includes stability, steady state performance and transient behavior of the loops. Design methodology is not critical when the loop update rate can be made high relative to loop bandwidth, as the performance approaches that of continuous time. For low update rates, however, the minimization method is significantly superior to the other methods.

I. Introduction

For many years phase-locked loops have been a cornerstone in phase coherent communication systems. Analog implementations dominated the scenario until the late sixties. Then, as a result of rapid advances in the field of microelectronics, digital systems offering a myriad of advantages began to replace their analog counterparts. The trend now is to implement and design phase-locked loops digitally.

Researchers in the field have explored several avenues for the implementation and design of digital phase-locked loops (DPLLs). An excellent survey of theoretical and experimental work accomplished in this area up to 1981 is presented by Lindsey and Chie (Ref. 1). The study, however, is not mature yet. The bulk of the research has concentrated on different ways to mechanize the loop phase detector, but very little effort has been spent in the design of loop filters. The typical design implements simply the discrete version of loop filters that have been widely used in analog phase-locked loops (APLLs) (Refs. 2, 3, 4, 5). This approach has a drawback, because the design process does not take into account the computational delays inherently present in any sampled-data system. These delays cause wider loop bandwidths than calculated from the continuous time equations, larger steady state phase errors for given loop bandwidths and dynamics, and reduced overall loop stability.

The classical control theory approach to improve performance would be to insert a compensator into the system. A variety of compensators have been proposed, with lead, lag, and lead/lag being the most commonly used. Nagrath and Gopal (Ref. 6) comment that lead/lag compensators are not

very useful when open loop transfer function poles are present on the imaginary axis if dealing with continuous time systems (on the unit circle for digital systems). This occurs with DPLLs, and tuned (second order) compensators are required for substanial improvements. The usefulness of this approach is, however, questionable. With a similar effort, one may employ more refined techniques and even obtain superior loop filters optimum in some sense.

This lack of design methodology for loop filters has led to the recent works on the methods compared in this article. Here, we present a systematic comparison of several loop filters that have been proposed for a class of DPLLs wherein each sample of the phase detector output represents the average phase error since the previous sample. We evaluate four different methodologies for the design of such filters. These are as follows:

(1) Impulse Invariance Transformation

(2) Minimization Method

(3) Estimation-Prediction

(4) Classical Control Theory Approach

Throughout the article, linear models for the PLLs are used, and the analysis is based on Z-transform theory due to the discrete nature of the loop component building blocks.

The performance of each loop is measured in terms of gain margin for stability, steady state phase error for unmodeled dynamics, and transient distortion (sum of the squares of the deterministic phase errors at the sampling instants). These criteria are typical in linear system analysis to assess the "quality" of a control system. For example, in case of DPLL, the closed-loop gain of the linearized model depends directly on the received signal power level. Thus to maintain the loop stability under power level variations, it is desirable to have high gain margin for stability.

In order to establish a fair basis of comparison, a convenient parameter (common to all the loops) must first be chosen. Then, the behavior of the different loops can be measured against this parameter. We find it convenient to use the one-sided loop noise bandwidth as the common element, because the bandwidth appears explicitly in expressions that characterize the variance of the phase estimation error, regarded by communication systems engineers as one of the most important measures of PLL performance.

The organization of the article is as follows. In Section II, the basic DPLL configuration studied here is defined. In Section III, the four methodologies for determining loop parameters are summarized. In Section IV, transfer functions resulting from the four methods are presented and compared. Loop stability, transient and steady state responses are compared in Section V. Finally, some general conclusions are drawn.

II. Basic DPLL Configuration

Several ideas have been suggested for the implementation of a DPLL, usually based on the mechanization of the phase detector. A notable example is the loop that attempts to track the zero crossings of the incoming signal; consequently, the sampling intervals are nonuniform (Ref. 1). In this article, however, uniform sampling is assumed. The main components of the general DPLL considered here are depicted in Fig. 1. The integrate-and-dump circuit integrates the phase detector output over T s, henceforth called the loop update time. The result is applied to the loop filter $F(z)$, which is typically implemented in software, to produce the control signal. This signal drives a hardware numerically controlled oscillator (NCO), whose output frequency is proportional to the control signal. The output phase of the NCO is fed back to become the reference phase input to the phase detector, to close the loop.

The input signal in Fig. 1 is $A\cos(wt + \theta) + n(t)$ where $n(t)$ is white noise with one-sided power spectral density N_0 W/Hz. The output of the sampler is $A\phi_k + n_k$ where ϕ_k is the average phase error over the last sampling period, and n_k is a white noise sample with variance $\sigma_n^2 = N_0/2T$. An equivalent linearized model of the DPLL considered here is illustrated in Fig. 2. The generic transfer function $KN_g(z)$ takes into account the mathematical representation of the NCO, the mechanization of the phase detector and a normalized computational delay g. This normalized transport lag is the fraction of loop update time interval from the time that each phase measurement is made until the NCO input is updated. The effects of the phase detector integrate-and-dump filter, the transport lag g, and the NCO are derived elsewhere (Refs. 7, 8) and can be included in a single transfer function $N_g(z)$ given below.

$$N_g(z) = \frac{T[(1-g)^2 z^2 + (1 + 2g - 2g^2) z + g^2]}{2z^2 (z-1)} \quad (1)$$

The DPLL implementation is facilitated when $g = 1$ corresponding to maximum possible delay. For this important example, Eq. (1) reduces to

$$N_1(z) = \frac{T(z+1)}{2(z-1)} \frac{1}{z^2} \quad (2)$$

This can be recognized as the cascade of two computational delays and the discrete version of the integral operation using the trapezoidal rule.

III. Design of Loop Filters

In this section we provide a synopsis of the underlying principles behind each methodology. Further details may be found in the references.

A. Impulse Invariance Transformation (IIT)

The first design (Ref. 7) involves the impulse invariance transformation (Ref. 9) of an optimum analog filter into a digital filter. Under this transformation, perfect integrators are approximated by

$$\frac{1}{s} \sim \frac{Tz}{z-1} \tag{3}$$

Other transformations such as the backward difference and the right-side rectangular rule also indicate Eq. (3) as their equivalent sampled-data transformation. In this manner, the equivalent sampled-data loop filter parameters can be conveniently expressed in terms of the corresponding analog loop filter parameters such as bandwidth and damping ratio.

An immediate advantage of this approach is that the theory of continuous time loops is very mature, and a wealth of useful knowledge has been accumulated. This information in many instances can be applied directly to the resultant digital loops. As one would expect, the continuous and discrete time theories are very close when the loop update rate is very high compared to loop bandwidth.

B. Minimization (MIN)

The minimization method (Ref. 10) applies optimal control theory concepts so as to arrive at a set of optimum digital filters for various input dynamics. The input to the loop is assumed to be the sum of a phase signal and white noise, the two being independent of each other. If σ represents the closed loop rms phase jitter due to additive white noise and if the sum square of the deterministic phase error is represented by D^2, the design criterion is to minimize

$$E = \sigma^2 + \lambda D^2 \tag{4}$$

where λ is a Lagrange multiplier. The design procedure is carried out as follows: For given input phase dynamics, fixed update rate and $N_g(z)$, find a causal filter $F(z)$ that minimizes E in Eq. (4). The overall loop transfer function can be obtained as a function of λ. Then, for any desired loop noise bandwidth, the multiplier λ can be obtained.

An analogous optimum design procedure using Wiener filtering theory was presented by Jaffe and Rechtin (Ref. 11), leading to the loop filters that found widespread use in APLLs. The same standard optimization technique was utilized later by Gupta (Ref. 12) to design a digital-analog loop.

C. Estimation-Prediction (E-P)

The third method (Ref. 13) borrows estimation theory concepts and is particularly attractive to Kalman filter users. The idea is illustrated in Fig. 3. Assume that the normalization is $A = 1$. Since $N_g(z)$ is known and realizable in hardware, it can also be implemented in software. This is done, and the same value of $\hat{\theta}_k$ which is subtracted in the phase detector is added back to the phase detector output in software, generating $\theta_k + n_k$ at the input to $S(z)$. On the basis of this signal, the digital filter $S(z)$ predicts the frequency correction signal for the NCO and its equivalent software realization. The filter transfer function $S(z)$ is assumed to be of the following type

$$S(z) = \frac{C(z)\,D(z)}{z^N N_g(z)} \tag{5}$$

where N is the number of transport lags, $C(z)$ is an estimator and $D(z)$ is a predictor. The design procedure is divided into five different steps. The first step is to select a model for the received phase that includes known dynamics plus process and measurement noise. The second step is to specify $N_g(z)$. The next step is the selection of an estimator. For this example, a least squares fading memory estimator was selected. The estimator obtains a state estimate (phase, frequency and acceleration) applying an exponentially decaying weight to past data and ignoring the pure delay. The fourth step is to compensate for the delay by designing an appropriate predictor. The predictor uses the state estimate to predict the phase N delays ahead. The last step checks for loop realizability and stability.

D. Classical Control Theory Approach (CCT)

The fourth approach is a heuristic method (Ref. 8). Here, classical control theory concepts are applied, including rules for the design of compensators. The idea is to select a realizable transfer function of the form

$$F(z) = \frac{A(z)}{B(z)} \frac{z^2}{C(z)} \tag{6}$$

The quadratic term in z cancels the transport lags, and $A(z)$, $B(z)$ and $C(z)$ are polynomials in z such that $F(z)$ is a realizable filter transfer function. Based on repeated trials and errors, convenient locations of the roots of these polynomials are selected. This is done via root locus analysis.

Basically, the goal is to produce an overall stable loop with reasonable transient and steady state performance, using well-known rules for the construction of root locus plots. The selec-

tion of the pole and zero locations of the filter is informal and requires some design experience.

IV. Loop Filter Transfer Functions

In this section we present a collection of results obtained with each of the design procedures outlined in the previous sections. For the sake of completeness, we provide their corresponding filter transfer functions. For space limitations, detailed derivations are omitted.

A. Impulse Invariance Transformation (IIT)

The sampled-data filter has the form (Ref. 7)

$$F(z) = G_1 + \frac{G_2}{1 - z^{-1}} + \frac{G_3}{(1 - z^{-1})^2} \tag{7}$$

where

$$\left.\begin{aligned} G_1 &= rd/AKT \\ G_2 &= rd^2/AKT \\ G_3 &= krd^3/AKT \\ d &= \frac{4B_A T}{r}\left(\frac{r-k}{r-k+1}\right) \end{aligned}\right\} \tag{8}$$

In Eq. (8), the coefficients are those employed in continuous time loop filters. The parameter r is typically 2 or 4, and is equal to $4\zeta^2$ where ζ is the damping ratio. The parameter k is a type 3 loop gain component ($k = 0$ for type 2 loop), with typical values ranging from 1/4 to 1/2. The coefficient B_A is the noise bandwidth of the underlying analog loop. The parameters A and K are those appearing in Fig. 2.

B. Minimization (MIN)

For a type 2 system the loop filter is given by (Ref. 9)

$$F(z) = \frac{2}{KT} \times \frac{(h_0 z - h_1)z^2}{\{4az^2 + (8a + 4b)z + (5a + 3b + c - d)\}(z - 1)} \tag{9}$$

The coefficients a, b, c, and d satisfy the identity

$$az^3 + bz^2 + cz + d = (z + 1)(\bar{a}z^2 + \bar{b}z + \bar{c}) \tag{10}$$

where $\bar{a}, \bar{b}$, and $\bar{c}$ satisfy the following set of equations

$$\left.\begin{aligned} \bar{a}\bar{c} &= 1 \\ \bar{a}\bar{b} + \bar{b}\bar{c} &= -4 \\ \bar{a}^2 + \bar{b}^2 + \bar{c}^2 &= 6 + r \\ r &= \frac{\lambda T}{\bar{N}_0} \\ \bar{N}_0 &= N_0/A^2 \end{aligned}\right\} \tag{11}$$

where N_0 = one-sided spectral density of input noise. The previous set of equations produces cancellation of a zero at $z = -1$ by a pole at $z = -1$. Imperfect cancellation can cause instability problems; therefore, a slight modification to the previous equations is used where the factor $(z + 1)$ in Eq. (10) is replaced by $(z + q)$. The value of q may be in the range of 0.9 to 0.999.

The type 3 loop filter has the form

$$F(z) = \frac{2}{KT} \times \frac{\{\tilde{C}z^2 + (\tilde{B} - 2\tilde{C})z + (\tilde{A} + \tilde{C} - \tilde{B})\}z^2}{(z - 1)^2\{16az^2 + 16(3a + b)z + [16(6a + 3b + c) - \tilde{C}]\}} \tag{12}$$

The various filter coefficients are given in terms of a set of four nonlinear simultaneous equations that will not be reproduced here. The set of equations again produces a pole-zero cancellation at $z = -1$, that demands a slight modification. The reader may refer to Ref. 10 for a simple method to obtain the values of these coefficients.

C. Estimator-Predictor (E-P)

The loop filter is given by (Ref. 13)

$$F(z) = \frac{S(z)}{1 - N_g(z)S(z)} \tag{13}$$

with $S(z)$ as indicated in Eq. (5). For a type 2 loop with a fading memory filter with estimator decay factor $\alpha, 0 < \alpha < 1$, the loop filter transfer function is given by

$$F(z) = \frac{(az - b)z^2}{c[z^2 + (1 + b)z + b](z - 1)} \tag{14}$$

where

$$\left.\begin{aligned} a &= 3 - 4\alpha \\ b &= 2(1-\alpha) \\ c &= T/2 \end{aligned}\right\} \quad (15)$$

The fading memory type 3 loop is

$$F(z) = \frac{(az^2 + bz + c)\,z^2}{d(z^2 + ez + c)\,(z-1)^2} \quad (16)$$

where

$$\left.\begin{aligned} a &= 6 - 9\alpha \\ b &= 9\alpha - 8 \\ c &= 3(1-\alpha) \\ d &= T/2 \\ e &= 4 - 3\alpha \end{aligned}\right\} \quad (17)$$

Special attention must be paid in the implementation of $S(z)$, because a pole-zero cancellation at $z = -1$ occurs as in the minimization method.

D. Classical Control Theory (CCT)

The last design procedure assumes a normalized computational delay $g = 1/2$ in Eq. (1), while the other three methods assume $g = 1$. This, however, complicates the loop implementation. For a type 2 loop, the filter used in Ref. 8 is

$$F(z) = \frac{(z - z_1)\,z^2}{(z - P_1)(z - P_2)(z-1)} \quad (18)$$

where

$$P_1 = -0.173$$

$$P_2 = -0.999$$

$$z_1 = 0.960$$

For a type 3 loop,

$$F(z) = \frac{(z - z_1)(z - z_2)\,z^2}{(z - P_1)(z - P_2)(z-1)^2} \quad (19)$$

where

$$P_1 = -0.173$$

$$P_2 = -0.999$$

$$z_1 = z_2 = 0.960$$

It is noted that these parameters were chosen for a specific application, in which the product of the one-sided loop noise bandwidth B_L times T is in the neighborhood of 0.15. No design rules are given for other $B_L T$.

V. Performance Comparisons

An indication of the relative merits of the individual configurations can be acquired using standard techniques of linear control systems. In this section, we employ three common criteria: (1) computation of stability gain margin, (2) calculation of steady state errors, and (3) calculation of transient distortion, defined as the sum of the squared phase estimation errors at the sampling instants. The output in all cases is graphical. In the design of PLLs, it is customary to treat the one-sided noise bandwidth as the independent variable and characterize loop behavior as a function of this parameter. We find it convenient to use, instead, noise bandwidth normalized (multiplied) by the loop update time.

In computing the results, it should be noted that Ref. 10 used symbols B_L and B for unnormalized and normalized two-sided loop bandwidth respectively, whereas we use them in the more conventional way to denote one-sided loop bandwidth. For the CCT approach, the results illustrated for the design example (Ref. 8) assume an update time $T = 1$ s.

A. Stability and Gain Margin

It is well known that second order, type 2 APLLs are unconditionally stable, and that third order, type 3 APLLs are unstable for low loop gains, but stable otherwise (Refs. 2, 3, 4, 5). Digital PLLs, however, are only conditionally stable. Type 2 DPLLs are unstable for high loop gains, and type 3 DPLLs are unstable for both, low and high loop gains. To differentiate these two extreme cases in computing gain margins, we use the terms "lower" and "upper" gain margin, respectively.

In Fig. 4 we examine the stability of the various configurations for a type 2 loop. The CCT loop is somewhat superior because it assumes a normalized computational delay $g = 1/2$. The other three loops assume $g = 1$ and have performances that differ among themselves by 2 dB at most, with the MIN method being the best.

In Fig. 5 we plot the lower gain margin for type 3 loops. It is important to emphasize that the CCT loop was designed with fixed compensation, not depending on desired $B_L T$. With this compensation, it cannot attain normalized bandwidths smaller than 0.06, because the loop becomes unstable. Any redesign for lower $B_L T$ would change both upper and lower gain margins. Upper gain margins for type 3 loops are depicted in Fig. 6. The MIN method is slightly better than the IIT and E-P methods in upper gain margin, and slightly worse in lower gain margin.

B. Steady State Performance

For both APLLs and DPLLs, the steady state phase error due to step acceleration and jerk is approximately proportional to the inverse of second and third power of the bandwidth for types 2 and 3 loops, respectively. It is convenient then, to define the phase error coefficients C_2 for type 2 loops and C_3 for type 3 loops. The use of these coefficients is advantageous because they exhibit slower variations with bandwidth than steady state errors. Thus, the steady state phase errors are related to bandwidth and phase error coefficients in the following way:

Type n:

$$\phi_{ss} = \theta^{(n)} \left(\frac{C_n}{B_L} \right)^n \tag{20}$$

where $\theta^{(n)}$ denotes the nth highest nonzero derivative of the input phase.

Figure 7 concentrates on type 2 loops. Notice from Eq. (20) that a smaller phase error coefficient implies a smaller steady state phase error. The MIN method is uniformly better than all of the other methods for all $B_L T$. For normalized bandwidths smaller than 0.02, both the IIT and MIN filter are superior to the E-P method and produce essentially the same results. This is because the E-P method used a fading memory filter, which has more damping than the IIT filter with $r = 2$. For larger bandwidths, the MIN filter is better. The poorest performance is provided by the CCT filter.

Figure 8 presents similar results and conclusions for type 3 loops. Again, the MIN method is best for all $B_L T$.

The importance of these results is that there are cases when significant performance improvements can be realized using the MIN method. Suppose T cannot be reduced, due to implementation limitations. In such situations using the MIN method of design, for a specified maximum steady state phase error, a smaller value of loop noise bandwidth is obtained compared to that achievable from other design methods.

For example, for the type 3 loop, using Fig. 8, $C_3/B_L T$ is approximately 6.7 at $B_L T = 0.2$ for the MIN method and at $B_L T = 0.3$ for the IIT and E-P methods. Thus a 1.8 dB (factor of 1.5) higher loop SNR can be achieved for the same lag error using the MIN method. In some cases, for very wide bandwidths, only the MIN method is satisfactory.

C. Transient Performance

The integral square error or transient distortion is defined here as the sum of the squares of the deterministic phase error components at the loop update instants. The summation runs from zero to infinity. The integral square error is plotted in Figs. 9 and 10 for type 2 and 3 loops. In the former case we applied a unit phase ramp, computed the square error and normalized (divided by T^2) the result. Type 3 loops assumed a unit frequency ramp, and the result was normalized by T^4. The MIN loop is the best in both cases, as it should be due to the optimization procedure. The CCT loop is the worst for type 2 (except for large normalized bandwidths), and the E-P loop is the worst for type 3 loops. In this last case, the gap between the MIN and the E-P loops is several orders of magnitude. This is probably due to selecting fading memory filters for the E-P case.

VI. Conclusions

Four classes of digital filters have been presented that have been proposed recently for a class of DPLLs wherein each sample of the phase detector output represents the average phase error since the previous sample. Whereas the filters in the first class are the mapped versions of the corresponding optimum analog filter, the filters in the second class are derived using optimal control theory. A suboptimal version of fading memory Kalman filter/predictor results in filters of class 3, while filters of the last class are designed on the basis of classical control theory.

On the basis of the results depicted in Figs. 4–10 we conclude that the filter obtained using the minimization method is the best in all regards, except in low gain margin for type 3 loops, where it is the worst. Since its lower gain margin is adequate, it is normally the best choice.

When the system is not update rate limited, so that $B_L T$ is small, the Impulse Invariance or continuous time analogy is very good. In fact, the Impulse Invariance and minimization filter performances converge to the same values for all the criteria. This agrees with intuition, because in the limit as the normalized bandwidth goes to zero, the Impulse Invari-

ance filter converges to a continuous time filter whose transfer function is derived using the same optimization technique that is employed by the minimization filter.

The specific E-P loops considered here use fading memory filters with a damping greater than that of IIT loops with $r = 2$. Therefore, they do not have as good a performance as the IIT and MIN loops even for small $B_L T$.

The loops derived from classical control theory were designed only for a limited range of $B_L T$. They perform reasonably well there. Their main disadvantage is lack of an overall design method, resulting in loops with performance depending on the designer's skill, experience and intuition.

The main instance in which it is important to use the minimization method over the IIT method is when $B_L T$ is not small. This occurs when the update rate has a maximum, due to implementation restrictions. Performance is then significantly better for the minimization method than for all other methods studied. In some cases, only the minimization method results in a usable design.

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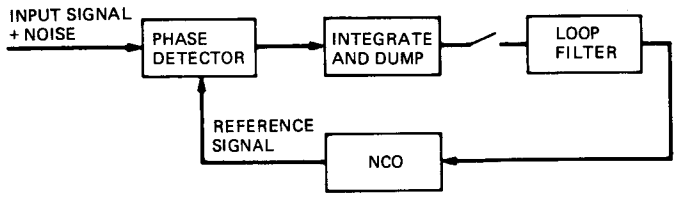

Fig. 1. Digital phase-locked loop

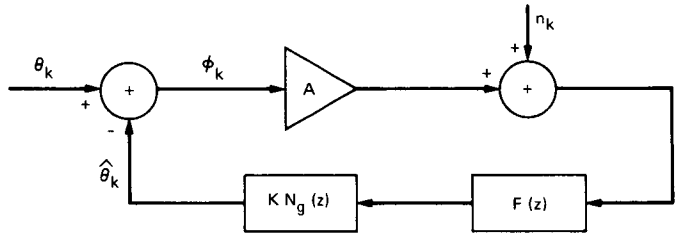

Fig. 2. Linear baseband sampled data loop model

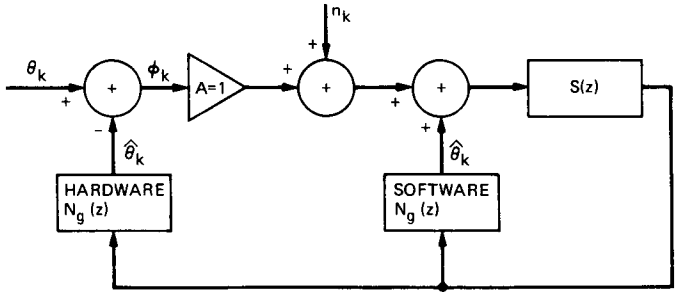

Fig. 3. DPLL with estimator-predictor

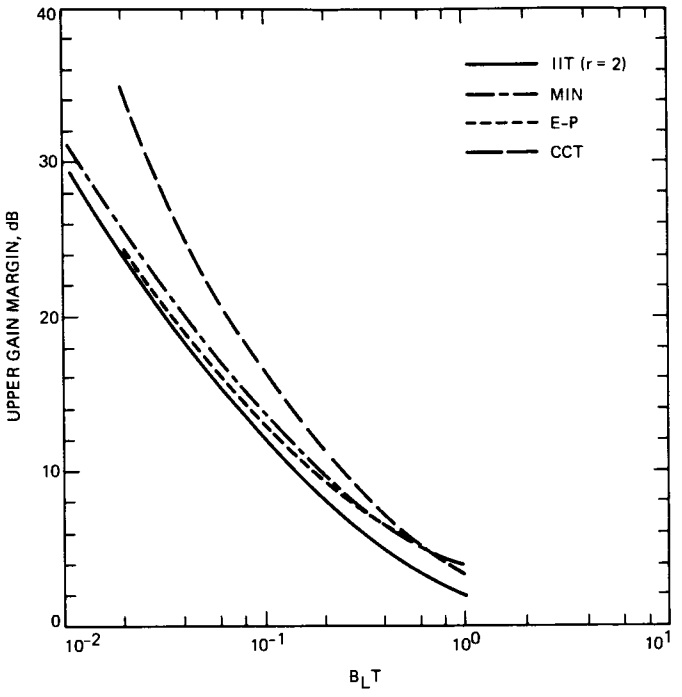

Fig. 4. Upper gain margin for type 2 DPLL

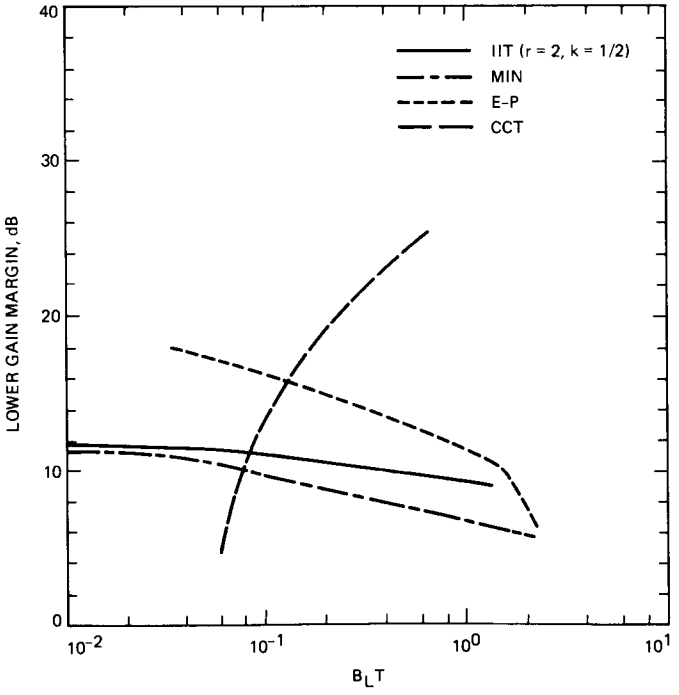

Fig. 5. Lower gain margin for type 3 DPLL

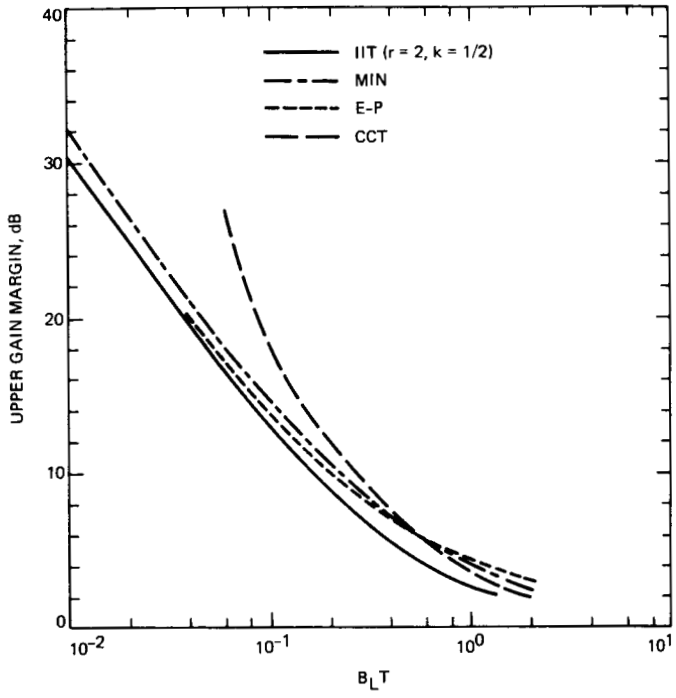

Fig. 6. Upper gain margin for type 3 DPLL

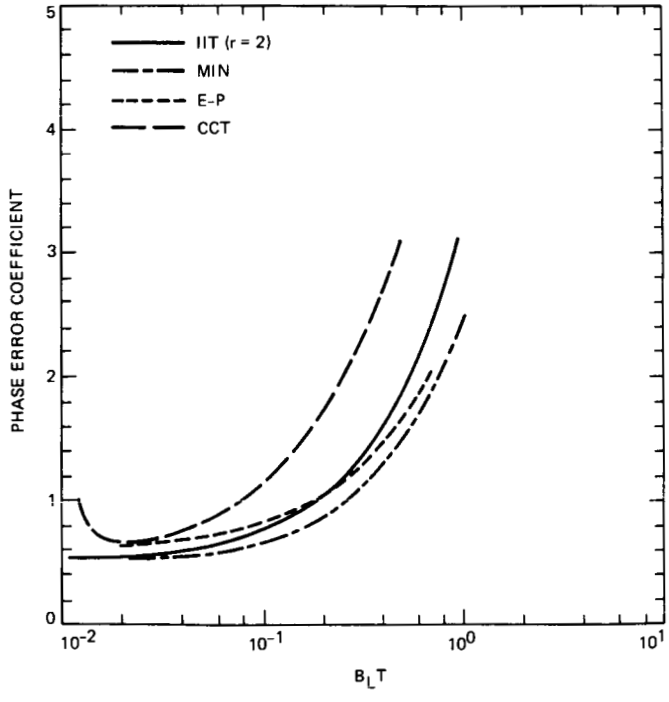

Fig. 7. Steady state phase error performance of type 2 DPLL

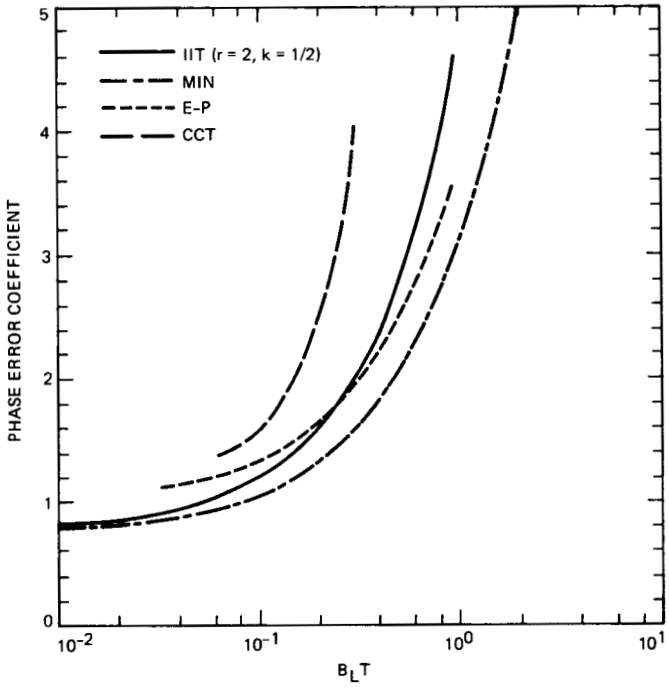

Fig. 8. Steady state phase error performance of type 3 DPLL

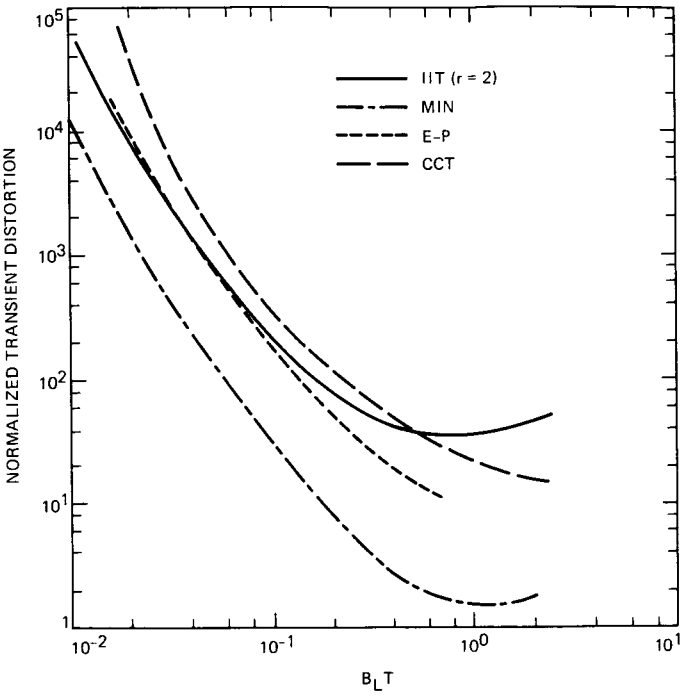

Fig. 9. Transient response of type 2 DPLL

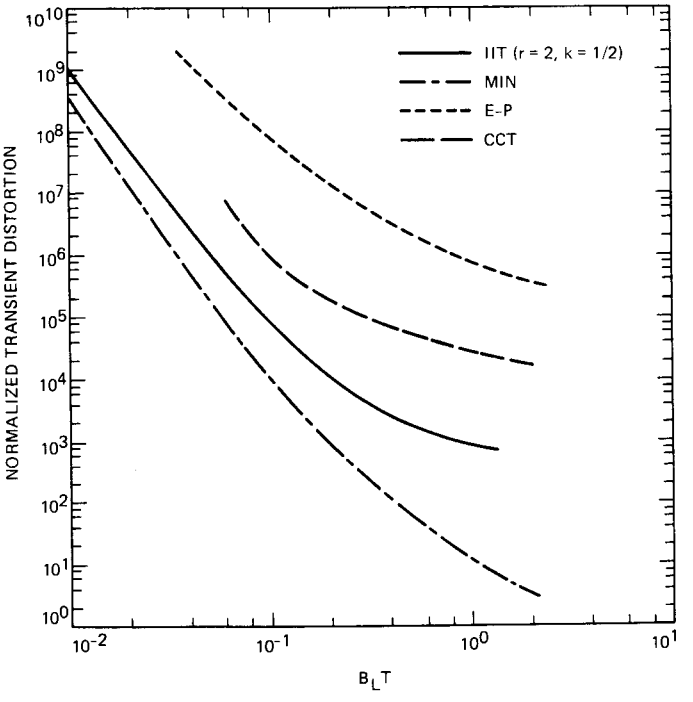

Fig. 10. Transient response of type 3 DPLL