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INVERSION LAYER MOS SOLAR CELLS

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ABSTRACT

Inversion layer MOS solar cells have been fabricated. The fabrication technique and problems are discussed. A plan for modeling IL cells is presented. Future work in this area is addressed.

ACKNOWLEDGEMENTS

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INTRODUCTION

Conventional silicon solar cells using diffused p-n junctions exhibit conversion efficiencies ($\sim$ 10.5% for 10 ohm-cm cells) which are far below the theoretical values of efficiencies (18-22%) (1). This may be due to a variety of causes. The first reason is that p-n junction cells have high space charge layer recombination which make the I-V characteristics different from those of an ideal junction, and the second reason is that very shallow p-n junctions are hard to control.

Inversion-layer IL/MIS solar cells have become a promising alternative to conventional diffused junction cells. MIS inversion-layer cells use two related techniques which are inversion layers formed in p-silicon and minority carrier MIS tunnel diodes. The advantage of using these techniques is that the processing is of low temperature and the diffusion-induced crystal damage inherent in diffused p-n junction cells can be avoided. Besides, the electric field on the silicon surface is in a direction to aid in the collection of minority carriers generated by short wavelength light. It avoids the "dead layer" found at the surface of many p-n junction cells. Therefore, the ultraviolet response has been shown to be much better than for diffused cells. Hence, the IL cell remains a viable alternative to diffused cells and further development is warranted.

OBJECTIVES

The main object of this work is (1) to fabricate IL/MOS solar cells, (2) to develop a simple, inexpsensive, low-temperature process for fabricating high-efficiency IL cells, and (3) to develop theoretical models for the cells.

PRINCIPLES OF OPERATION OF IL/MIS SOLAR CELLS

The basic structure of an IL/MIS cell is shown in figure 1. It consists of a sintered aluminum back contact on a p-Si substrate, a photolithographically defined Al MIS front contact in the form of a grating, and a thick oxide/antireflection coating. The main function of the oxide in an IL cell is to invert the surface of the p-Si substrate and to induce an ideal n^+/p junction. This is achieved through the action of positive charges trapped in the oxide during fabrication. The principal charge in thermal oxides is the surface state charge, Q_{ss}, which is considered to be associated with excess silicon atoms close to the SiO_2-Si interface. The value of Q_{ss} is highest on <111> oriented substrates and can be varied over a wide range by heat treatment in dry oxygen.

The minority carriers, which are electrons in this case and are generated in the bulk of the p-Si, are collected vertically and then flow along the inversion layer to the MIS contact and removed from the cell via the aluminum grid as shown in figure 2. In order to get higher minority carrier collection efficiency, the MIS contacts have to be very closely spaced, typically of the order of the diffusion length of the minority carriers (50 - 120 micrometers).

IL/MIS CELL DESIGN AND FABRICATION

For an IL cell, the substrate must be p-type. To get strong inversion using only fixed positive interface charge, the wafer should be in the <111> orientation and be lightly doped. A higher open circuit voltage can be obtained using a more heavily doped substrate. At the same time, it will be more difficult to get the inversion layer and will reduce the short-circuit current because of lower electron lifetime. Based on this consideration, the doping levels in the ranges of 10^{15} cm^{-3} to 10^{16} cm^{-3} yield the best results (2).

Wafer thickness is also important. A cell with a BSF region whose thickness is less than one diffusion length operates best. However, a cell fabricated on thicker wafer will absorb more light. The thickness of a single crystal silicon cell is normally in the range of 50 micrometers to 500 micrometers.

The basic IL cell requires a thick oxide layer on the front surface. It can be grown thermally by oxidizing the surface of the wafer. This process is reliable and produces good SiO_2-Si interfaces with reasonable levels of positive interface charges. One of the drawbacks of this process is that it requires high temperature.

Other types of oxide can be used to get higher oxide charge densities. Chemical vapor deposition (CVD) of SiO_2 is a promising alternative. CVD oxides appear to have a high value of positive interface charges. It

is a fast, low-temperature (as low as 250°C) process producing uniform, reproducible oxide layers. The disadvantages of CVD oxides are: (1) it tends to be leaky, and (2) it is somewhat difficult in depositing SiO_2 uniformly around aluminum grid lines.

Once the internal structure is complete, contact to the inversion layer must be made. For diffused IL cells, a window in the oxide is opened and n^+ diffusion is made to contact with the inversion layer.

The most promising alternative is the MIS contact. Thin oxide layers can be grown in the contact windows by a variety of low-temperature processes such as sputtering. Aluminum is deposited over the thin oxide to complete the MIS contact.

The process of evaporation and photolithography is the process most often used for metallization. Aluminum is deposited over the entire wafer surface by electron beam evaporation in a vacuum. The grid pattern is defined in photoresist using an optical mask and the excess metal is lifted off, leaving the pattern which has been designed.

Most metal used on silicon must be sintered after deposition to obtain good ohmic contacts. During this process, any layers between the metal and silicon are brought into intimate contact. For this reason, sintering after MIS contact formation should be avoided.

In summary, the procedure for fabrication is described as follows:

(1) On <111> p-type silicon, substrates of approximately 1000A of SiO_2 are grown thermally.

(2) Aluminum is next deposited on the back surace and sintered.

(3) MIS grid is then defined photolithographically using a first mask and a thin oxide layer grown in this region by sputtering.

(4) A thickness of one micrometer of aluminum is deposited on the front surface. The excess metal is lifted off, leaving the pattern designed.

To have the highest possible efficiency from a solar cell, its structure must be optimized. It is not straightforward to optimize a cell, however, the main reason is that the device parameters are not interdependent, and there exist complex relationships between structural parameters and cell operation.

In desiging the contact grid for the induced junction solar cell, the sheet resistance of the inversion layer must be taken into account. Since this layer is shallow and has a relatively low equilibrium carrier concentration, it will demonstrate a high sheet resistance. Therefore, the contact grid must be close to every point on the front surface to reduce the lateral series resistance in the inversion layer. On the other hand, the front contact grid must cover only a small fraction of the cell area in order to maximize the area exposed to the light. It is obvious that grid design becomes critical to efficient cell operation. To optimize the tradeoff between grid shading and high sheet resistance in the inversion layer, the grid finger spacing must be carefully chosen.

EXPERIMENTAL RESULTS

Results are presented here for three cells. They were fabricated using the process described in the previous section.

The I-V characteristics under simulated AMO are shown in figure 3 (cell #1), figure 4 (cell #2), and figure 5 (cell #3). The area of each cell is 4.1 cm^2. The short circuit currents are 2.4 mA and 1.22 mA for cell #1 and cell #2, respectively. The open-circuit voltage is 0.1645V for cell #1, while the value for V_{OC} for cell #2 is 0.1558V. For cell #3, we have obtained 0.4655V for its open-circuit voltage and 0.02 mA for its short-circuit current. For cell #1 and cell #2, no oxide was sputtered between the metal and semiconductor for MIS diodes. For cell #3, a very thin oxide layer was sputtered as the thin interfacial region for the MIS grid. For cell #1 and cell #2, the short-circuit currents are quite lower than we expected. The values of V_{OC} for these two cells, however, are not far from those values for a Schottky diode. For cell #3, the open circuit voltage is quite reasonable, but the short-circuit current is far too low. It might be due to (1) the thin interfacial oxide is still too thick and (2) the thermal oxide has become too thin at the edge of aluminum to strongly invert the surface, and thus, the inversion layer in the active areas is isolated from the MIS contacts. Because of the first reason, a minority carrier tunneling diode might not be realized. Because of the second reason, only a small amount of lateral collection occurred, resulting in the low value for I_{SC}.

To reduce cracking and separation between an inversion layer and an MIS contact, we plan to use a second mask to define the grid photolithographically. To determine the optimum thickness of the thin silicon dioxide for an MIS grid, we are going to vary the sputtering time.

MODELING OF IL CELLS

In order to fully understand the operation of an inversion layer cell and to obtain higher conversion efficiency, detailed analysis and modeling of this cell are needed. So far, however, only limited modelings of these devices have been published (3,4,5).

We plan to develop a computer program for modeling induced-inversion-layer MOS solar cells. A theoretical analysis of the current-voltage characteristics of these devices will be pursued. The overall objective of the work is to identify and to characterize various mechanisms which tend to limit the conversion efficiency of these IMOS devices. This will be accomplished through a solution of the fundamental device equations including the effects of the $Si-SiO_2$ interface charges and traps. An external generation rate due to the full spectrum solar irradiance will be included too. Doping and field dependent mobility and nonuniform doping profiles in the substrate will also be taken into account. Moreover, the effects of radiation damage and the effects of the sheet resistivity in the induced n^+ region will be studied.

CONCLUSION AND RECOMMENDATION

Objectives (1) and (2) were partially achieved. Objective (3) has not been achieved due to short period of time (10 weeks plus two additional weeks). In fact, all of these tasks are long-term projects. They need a much longer time to accomplish. It is a good start. Continuous effort should be made to obtain more productive results.

IL/MOS solar cells have been fabricated. It has been demonstrated that they can be fabricated using low-temperature processing. The short-circuit currents of the cells fabricated in this laboratory are still far too low. The effort of improving this situation is now under way. As mentioned earlier, we plan to use a second mask to define grid photolithography. For future study, the following items are recommended:

(1) Analyze dark I-V and C-V characteristics of the cells to obtain information on the mechanisms of barrier formation and current transportation.

(2) Perform further optimization of the grid structure for increasing the efficiency.

(3) Control the thin layer of oxide in an MIS contact more accurately.

(4) Fabricate IL/MOS cell using CVD SiO_2 instead of thermal oxide.

(5) Fabricate IL/MIS cells using other transparent dielectrics which are responsible for inducing an inversion layer at the silicon surface, such as TiO_x. SiO, and Ta_xO_x and above all CVD nitride (6).

(6) Study IL cells under high concentration.

(7) Determine the characteristics of the inversion layer cell under the influence of ionizing radiation for space application.

(8) Study the problems of cascading the cells.

(9) Investigate the IL solar cell array.

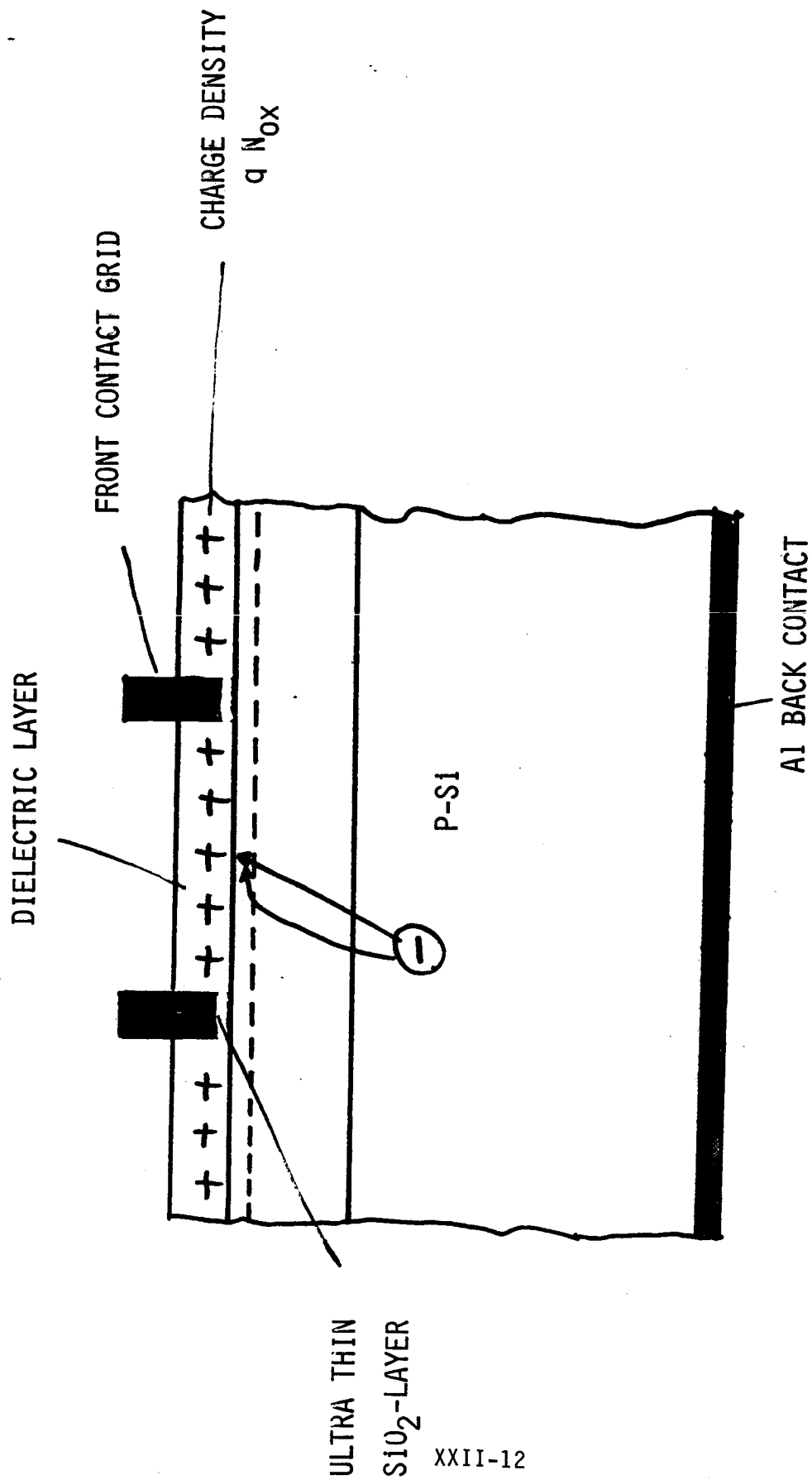(10) Study other surface effect solar cells such as accumulation layer cells.

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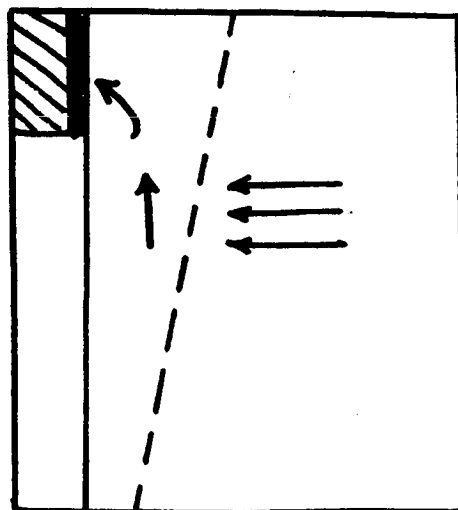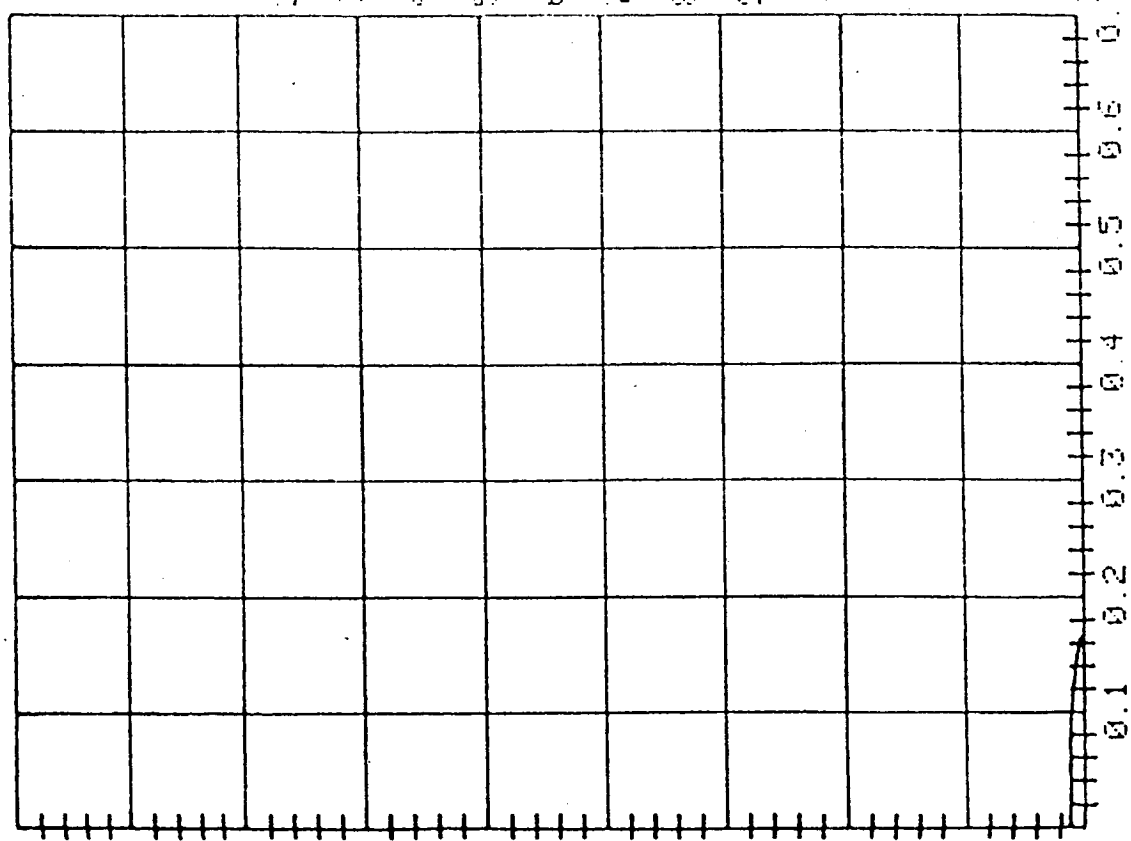Figure 1. Schematic Cross Section of an MIS/IL Solar Cell

XXII-12

Figure 2. Schematic Diagram of the Electron Current Flow in an MIS Inversion Layer Solar Cell

SPECTROLAB

MODEL # ____
SERIAL # 4N
DATE ____

1 CELL AREA (SQ MM)
330

2 # OF CELLS IN PARALLEL
1

3 # OF CELLS IN SERIES
1

4 AMBIENT TEMP (DEG C)
25

5 STANDARD TEMP (DEG C)
28

6 I TEMP COR(UA/SQ CM/DEG C)
20

7 V TEMP CORR UV/DEG C/CELL)
-2000

8 AMB CAL CURRENT (0.1'S MA)
506

9 TEST VOLTAGE (0.01'S V)
1

10 MIN I(TEST) (0.01'S A)
1

I(TEST) =   2220 UA
ISC =   2400 UA
VOC =   164500 UV
185 UW
MAX POWER = 102000 UV

AMP.
.18
.16
.14
.12
.10
.08
.06
.04
.02
0

0.1 0.2 0.3 0.4 0.5 0.6 0.7 VOLTS

Figure 3. I-V Characteristics for Cell #1
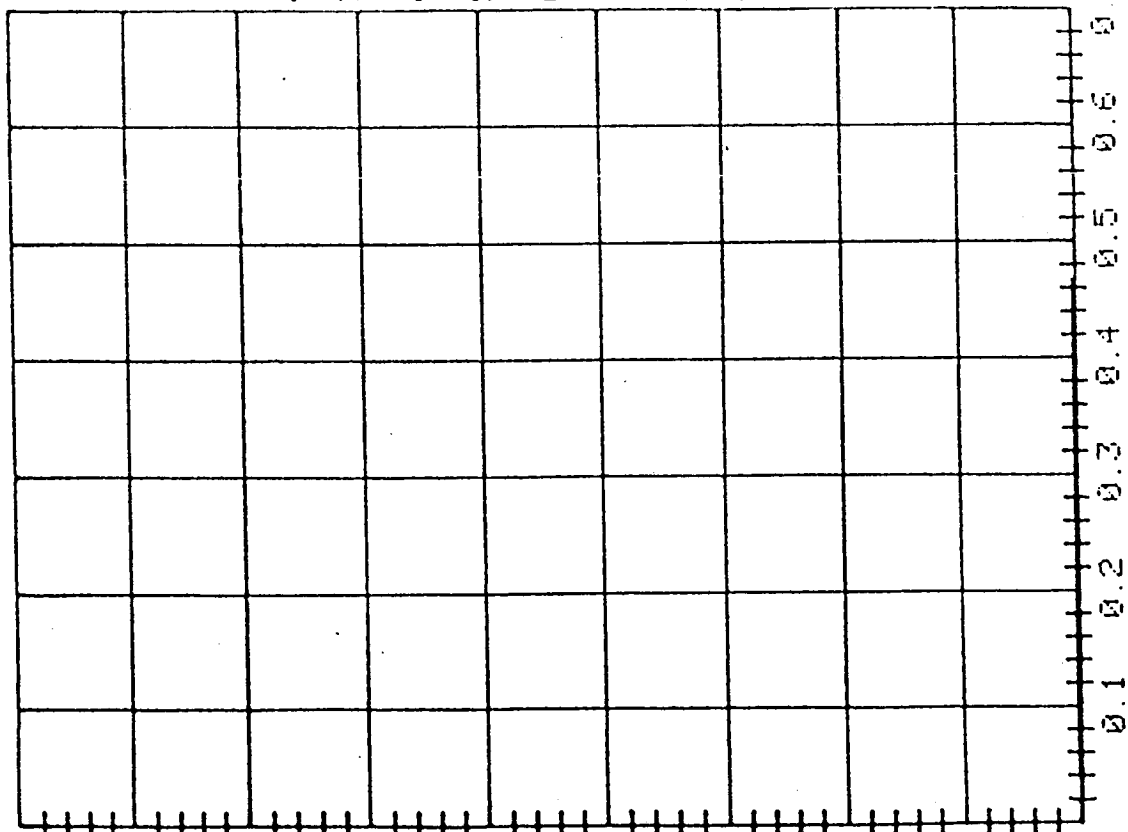
S P E C T R O L A B

MODEL # 4D
SERIAL #
DATE

1 CELL AREA (SQ MM)
  380
2 # OF CELLS IN PARALLEL
  1
3 # OF CELLS IN SERIES
  1
4 AMBIENT TEMP (DEG C)
  25
5 STANDARD TEMP (DEG C)
  28
6 I TEMP COR(UA/SQ CM/DEG C)
  28
7 U TEMP COR(UU/DEG C/CELL)
  -2000
8 AMP CAL CURRENT (0.1'S MA)
  506
9 TEST VOLTAGE (0.01'S U)
  1
10 MIN I(TEST) (0.01'S A)
  1

  I(TEST) =   1020 UA
  ISC =   1220 UA
  VOC =   155000 UU
  MAX POWER   54 UW
          @   88100 UU

Figure 4.   I-V Characteristics for Cell #2

Figure 5. I-V Characteristics for Cell #3

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