NASA CR-179546

20 GHz Power GaAs FET Development

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One Space Park
Redondo Beach, CA 90278

SEPTEMBER 1986

FINAL REPORT

Contract No. NAS3-22503

Prepared for

National Aeronautics and Space Administration
Lewis Research Center
Cleveland, OH 44135

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1. INTRODUCTION

This report covers the work performed by both TRW and Raytheon on the 20 GHz Power GaAs FET Development program, Contract No. NAS3-22503, sponsored by the National Aeronautics and Space Administration, Lewis Research Center, Cleveland, Ohio, during the period from December 1982 to April 1986.

The objective of this program was to develop Ku-band power GaAs FETs meeting the following specifications, and to design and develop an amplifier module using these devices.

(1) 1 Watt Power FET	Bandwidth:	19.7 to 21.2 GHz
	Output power:	1 Watt min
	Associated gain:	5 dB min
	Efficiency:	20 percent min
(2) 2 Watt Power FET	Bandwidth:	20.2 to 21.2 GHz
	Output power:	2 Watt min
	Associated gain:	4 dB min
	Efficiency:	18 percent min

As a result of the previous development of the 20 GHz 8.3 W GaAs FET POC Amplifier under this contract (Cf. Report No. CR 168240), it became obvious that the GaAs FET devices had to be improved to provide high-power handling capability with increased gain, bandwidth, and improved efficiency.

As a minimum, the following tasks should be investigated to improve the device:

- Modify the two-cell device used for the original POC amplifier into a single-cell device and compare it with the original
- Reduce overall chip size to reduce parasitics
- Combine VIA holes and air bridge techniques to achieve lower parasitic interconnects
- Increase device source periphery to 2 mm
- Increase gate thickness using plating techniques to reduce gate resistance
- Reduce gate length using novel photolithographic method and E-beam technology.

ACKNOWLEDGEMENT

The authors would like to thank Dr. P. White, principal investigator of the power FET development program at Raytheon, and Dr. M.C. Tasi, his successor, for their many contributions to the programs. They would also like to thank R. Healy and B. Liles of Raytheon Company, SMDO, and Dr. B. Hewitt for their contributions.

2. GaAs POWER FET DEVELOPMENT

During the course of this program, two new devices, the S102 and S204, were developed. Activities included device design; doping profile determination; airbridge technology; tee-gate technology; dc, thermal, and RF characterization.

2.1 DEVICE DESIGN

At the start of the program, an existing device (S900) had recorded state-of-the-art RF performance of 0.8 Watt output power, 4 dB gain, and 20 percent power-added efficiency at 20 GHz. The device used standard Raytheon via-hole structures. These devices were made with a 0.5-μm gate length and 100-μm finger width. The total gate periphery was 1.6 mm. Gates were originally defined by photolithography, which gave relatively poor yield. The performance was not impressive over the 19.7 to 21.2 GHz frequency band.

It was initially believed that the potential disadvantages of this conventional structure were the large chip size caused by the via-hole under each source pad and a relatively high gate resistance because of the device width. Two new device designs were consequently made for this program. Both employed 2 mm total gate width to supply the required output using 0.5 W/mm as a goal. One structure incorporated twenty 100-μm wide unit gates in the usual comb pattern. However, it was made more compact than the existing S900 1.6 mm gate width device using smaller source pads with airbridge connections. In this design, the air bridges do not obscure the active channel areas, thus allowing full visual inspection. Plated through via-holes provide connections from the grounding pads to a plated integral heatsink on the underside of the chip. Average gate-to-gate spacing is 20-μm and the maximum dimension of the active area is only 0.5 mm, which is approximately $\lambda/9$ at 20 GHz. This single-cell device eliminates the necessity of wire-bond interconnections, but it provided with two-gate and drain bonding pads. These are made as small as possible, consistent with wire bonding capability, to minimize parasitic input and output capacitances. A diagram of this S102 comb structure is shown in Figure 2-1.

The second device used a novel "ladder" structure in which 16 gate units are each fed at the mid point as well as at both ends from a series of gate buses lying parallel to the gates. The effective unit gate width is

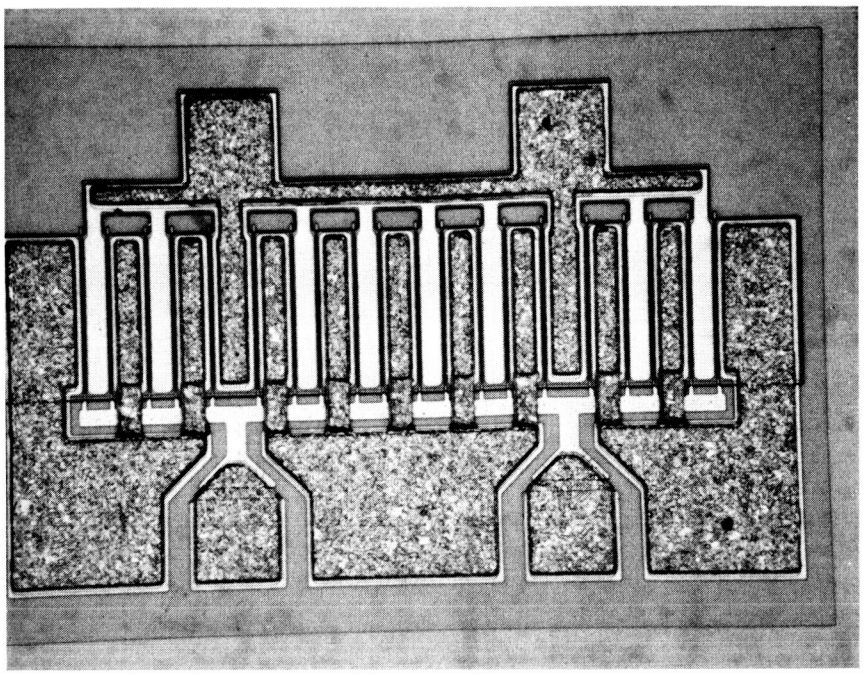


Figure 2-1. Device configuration of S102 "comb" type

therefore reduced this way to 31-μm, giving a factor of 3 reduction in parasitic gate resistance compared with the conventional structures. This device used similar air bridge source interconnections and via-hole grounding schemes as described above. A diagram of the device structure is given in Figure 2-2. The disadvantage of this structure is its greater complexity and larger active area. The maximum active dimension is 0.83 mm or $\lambda/6$ at 20 GHz. The parasitic gate pad capacitance is also increased because of the complex gate feeds. In addition, the mask set contained a drop-in test pattern for in-process monitoring of contact resistance, isolation, and dc characteristics. It included test transistors without passivation for post-process SEM examination of gate length, and a FAT FET for carrier density and mobility profiling.

Figure 2-3 shows the drawing of an S204 device which is basically, a single-cell device that incorporates two S102 devices. It was assumed that a S204 device would yield 2 Watts output power.

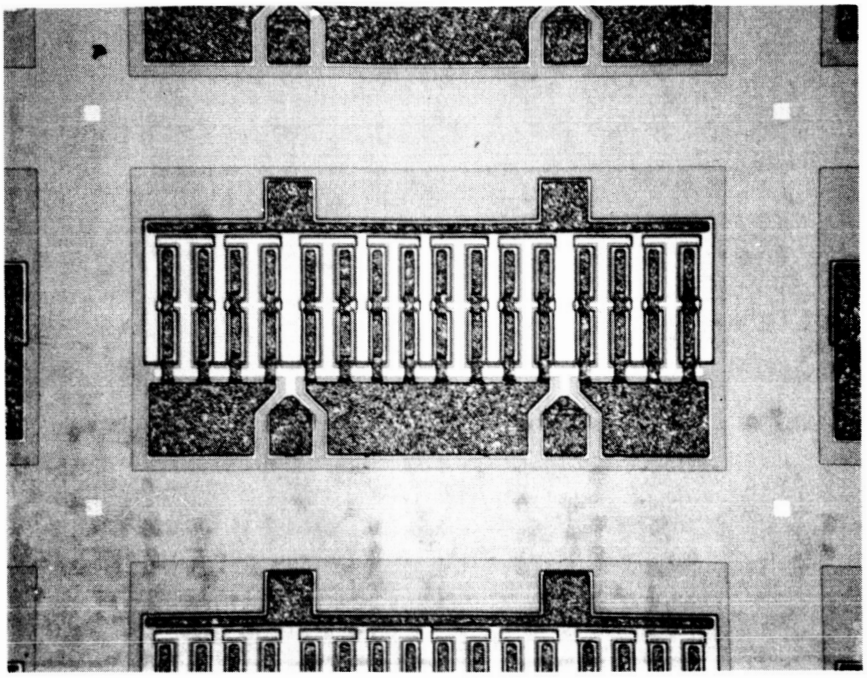


Figure 2-2. Device configuration of S102 ladder type

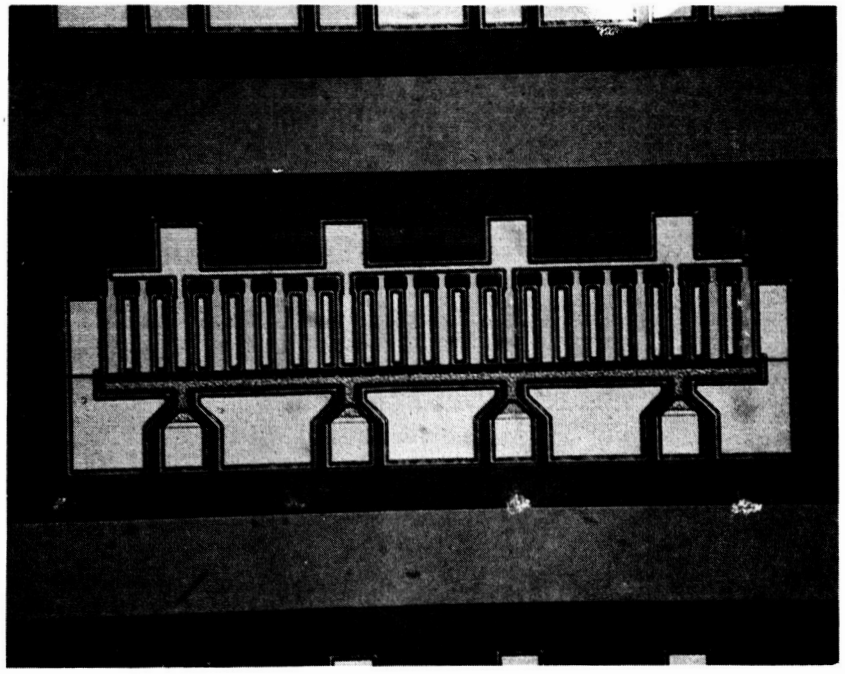


Figure 2-3. Device configuration of S204 "comb" type

2.2 MATERIALS FABRICATION

A typical doping profile for GaAs FET devices consists of buffer, active, and contact layers. The buffer layer is deposited directly on the

semi-insulating substrate by vapor phase epitaxy and serves to isolate the active layer from the deleterious effects of deep level traps located in the substrate. The substrates used for these programs were fabricated from outside vendors who had mutual cooperation with SMDO through other development programs. Previously, it was found that substrate effects are crucial to the device performance. Two methods, Deep Level Transient Spectroscopy (DLTS) and Secondary Ion Mass Spectroscopy (SIMS) were adopted to detect impurities in the material.

The active layer is grown on top of the buffer layer. The required doping level was experimentally determined to be around 2E17 e-/cc. The N+ layer on top of the active layer is to facilitate ohmic contact to the device. This doping level was determined to be higher than 1E18 e-/cc. Figure 2-4 shows the standard doping profile of a power FET.

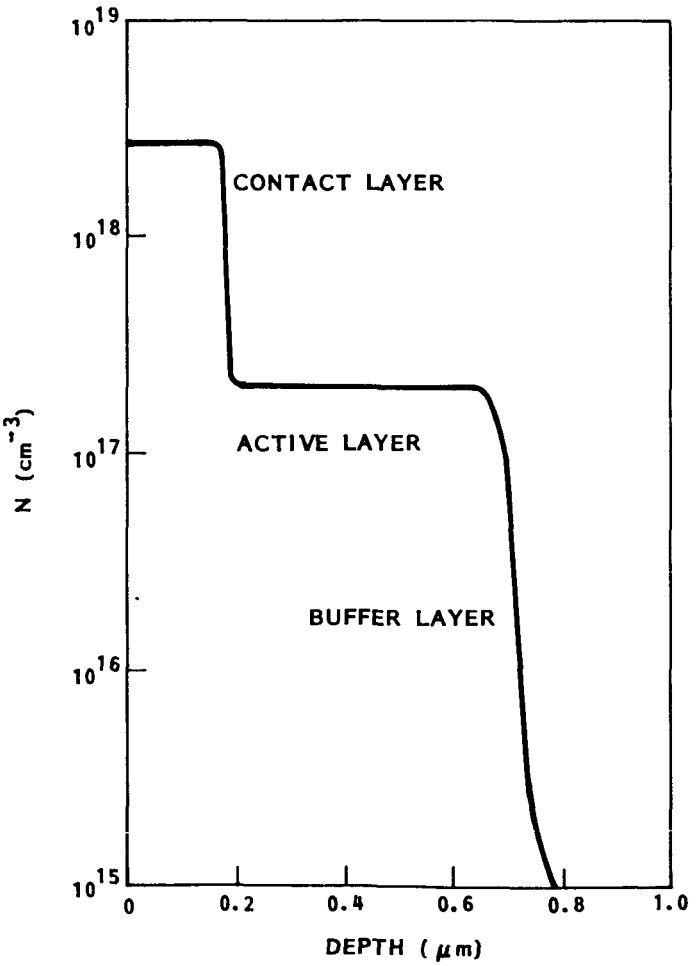


Figure 2-4. Power FET doping profile

2.3 WAFER PROCESSING

The wafer processing sequence is shown in Figure 2-5. During the course of this program, the sequence remained unchanged with the exception that air-bridge and tee-gate technology have been developed. Eight masks are used in standard wafer processing: Mesa I, Mesa II, source-drain, gate, passivation, final metal, Via-hole, and grid. Mesa etching is used to isolate each cell of the device. A gold-germanium nickel metallization provides ohmic contacts. The gate mask is used to define the gate formation. E-beam writing has since replaced photolithography. This method significantly improves gate yield. Silox passivation protects the device from surface charge migration. The final front side metallization (gold) serves to enhance reliability by reducing the current density in the metal which subsequently reduces electromigration. Via-holes connect the source pads to the backside metal. After backside processing, wafers are diced into chips.

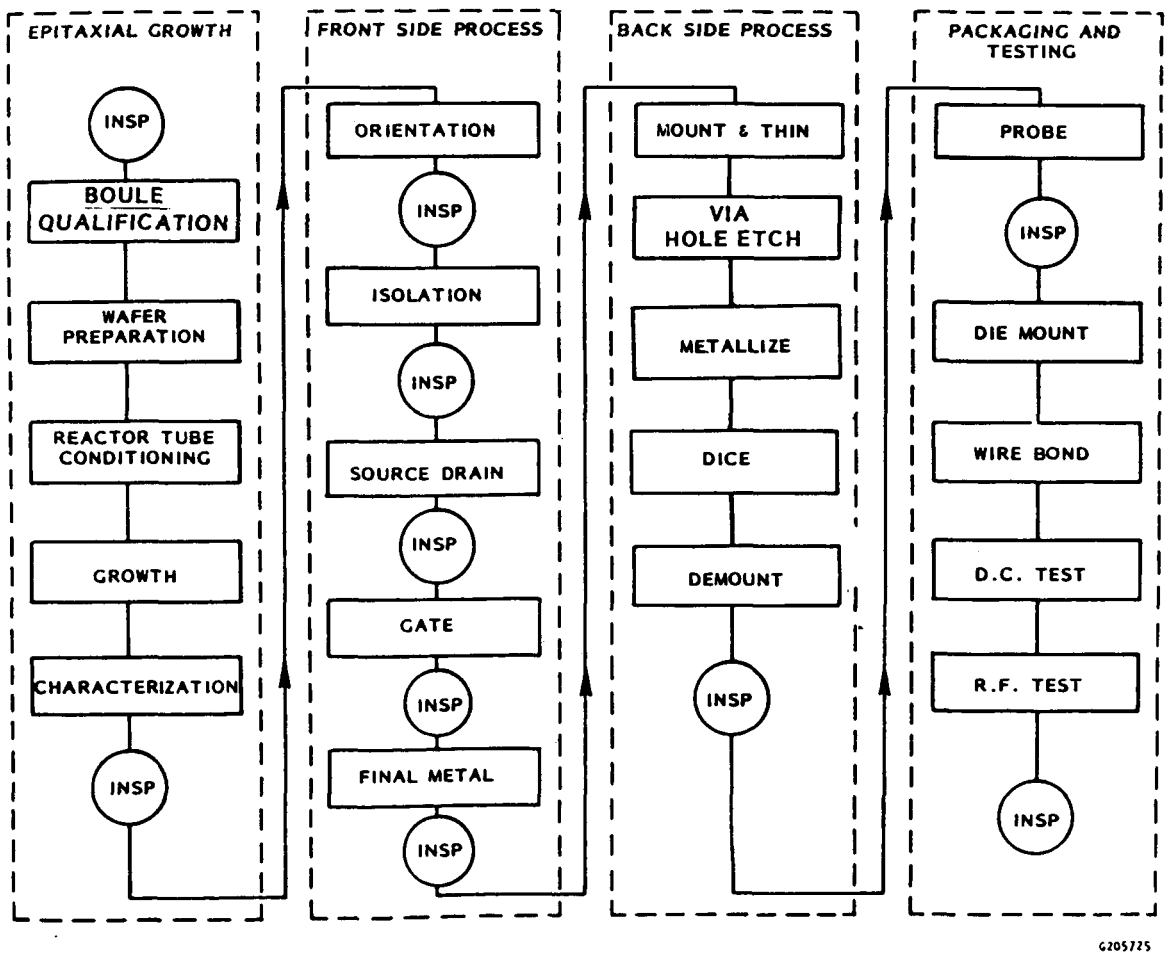


Figure 2-5. GaAs FET process-assembly flowchart

2.3.1 Air-Bridge Technology

In standard processing, each source finger is connected to the backside through a via-hole. S102 and S204 devices designed for this program developed an air-bridge technology to connect each source finger to source pads which in turn are connected to the backside through the via-holes at each end. The air bridge process consists of the following four basic steps:

1) Deposition of layer I, a thick layer of positive photoresist, typically 2.5 to 3 μm form a smooth arch on the bridge.

2) Deposition of layer II, a mask which defines the bridge pattern.

3) Gold plating to form the bridge to about 3 μm thick.

4) Liftoff to remove the unwanted gold areas and two resist layers.

Figure 2-6 shows micrographs of experimental air bridges on wafer 16I18A.

Figure 2-6. SEM photograph of air bridges crossing gate bus on experimental wafer 16I18A

2.3.2 Tee-Gate Technology

Figure 2-7 schematically shows a novel process for tee-gate fabrication which was initially investigated. In this process, the top of the gate is

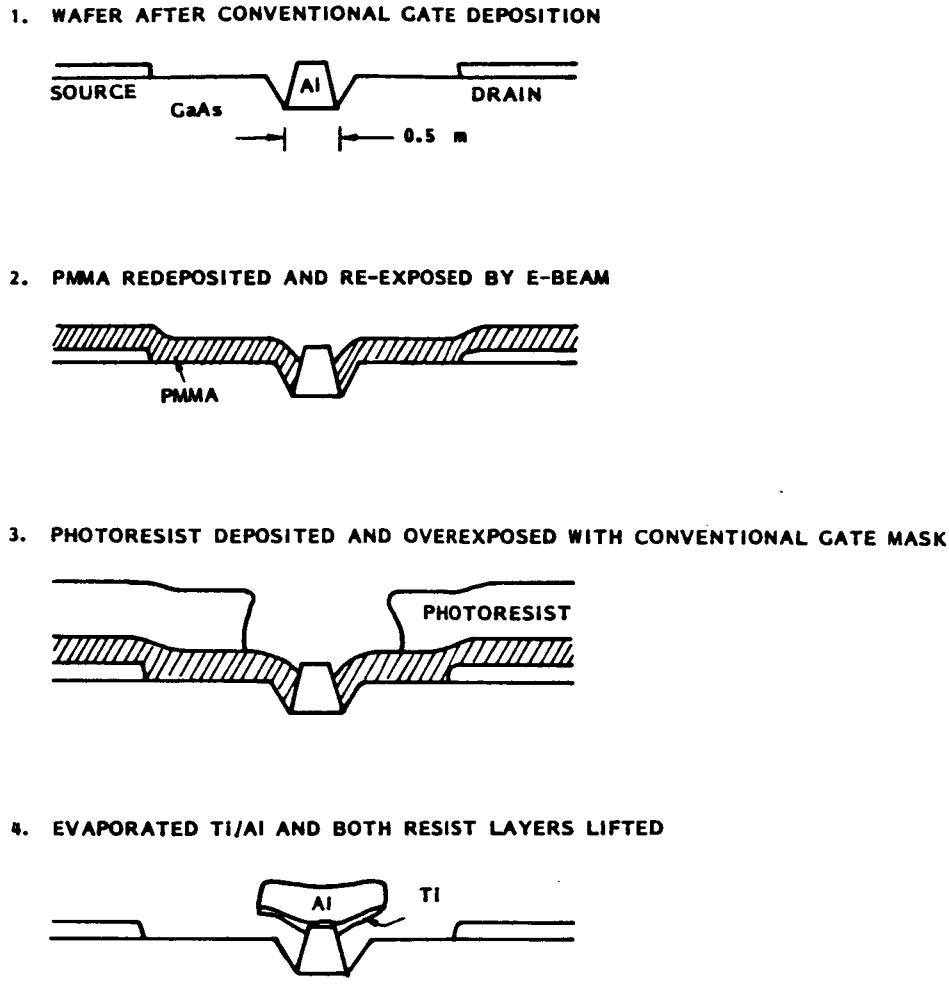


Figure 2-7. Schematic of Tee-gate technology - Method 1

deposited in a separate evaporation. Some of the advantages of this process over single-evaporation techniques are listed below:

1) Compatible with deep recessed channels, i.e., the problems of "closing off" the 0.5 μm opening during evaporation would be avoided.

2) Ability to evaluate the gate length, diode characteristics, etc. before committing to a tee section.

3) Capability of comparing tee sections with conventional gates on the same wafer.

4) Applicable to Al gates or plated structures which would require Ti/Pt/Au or similar metallization.

This process is feasible because of the precise realignment capability

of the E-beam system. The most likely foreseen problem was adhesion between the second and first metal layers; however, an unexpected difficulty arose.

Realignment, Step 2, was successfully accomplished on test wafers as shown in the SEM photograph of a cleaved cross section in Figure 2-8. Tests to produce a wide (1.5 μm) opening in Shipley 1350J photoresist deposited over PMMA were also successful (including the undercut profile to aid lift-off induced by a chlorobenzene soak). However, when the exposure was made over a 0.5 μm gate opening already positioned in the PMMA, only a broad shallow depression was formed in the photoresist--even though pad areas were properly cleared. A cross sectional SEM photograph of the result is shown in Figure 2-8b. The same problem arose when the original test piece containing an actual 0.5 μm gate was aligned. The problem is believed to to be the result of scattered UV light by the submicron feature beneath the photoresist layer into the area otherwise shadowed by the mask.

The original approach has therefore been abondoned and a more conventional single-evaporation process using a 2-level resist has been investigated. Since it appears impossible to expose the photoresist when the gate strip is present, the method being attempted is to first define the photoresist opening followed by E-beam writing. The process as envisaged is sketched in Figure 2-9.

The formation of the latest tee-gate structures is summarized as follows:

- Standard wafer processing technology is used through gate trenching of the epi active layer.
- The gate metals used are titanium, platinum, and gold layers. They are deposited to a thickness of 0.3 μm forming the base of the tee structure. Standard "liftoff" process is used to remove unwanted metal leaving 0.5 μm gates.
- Using photolithography, a grid pattern is defined on the wafer connecting all the devices. A thin layer of gold is deposited and "liftoff" is used to remove unwanted metal. This step provides electrical connections between all devices for electroplating the "tee" tops on the gates.
- The gates are then rewritten using E-beam lithography for accurate alignment over the existing gates.

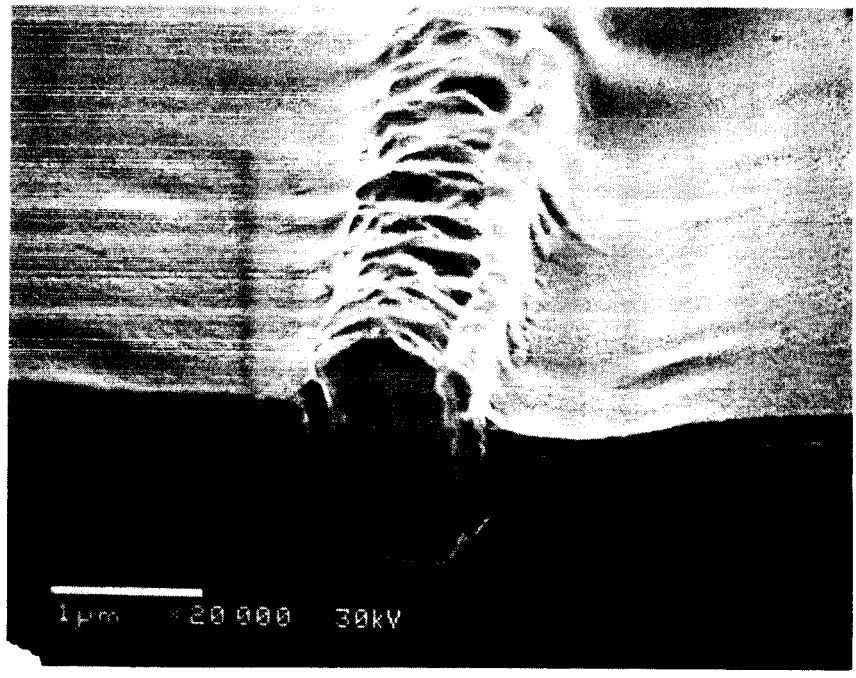
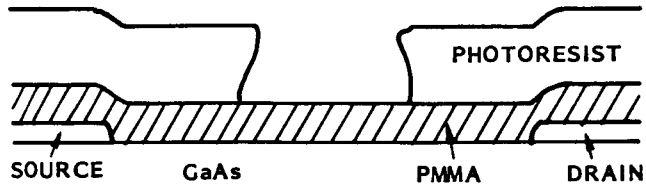
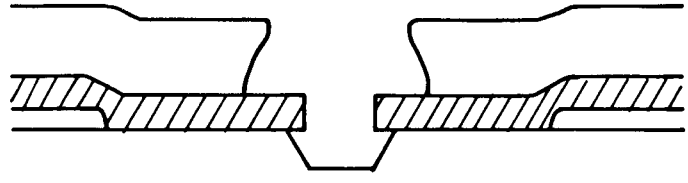


Figure 2-8. Cross sectional SEM photographs of Tee-gate technology experimental wafers

1. WAFER COATED WITH PMMA AND PHOTORESIST OPENING DEFINED IN PHOTORESIST



2. 0.5 μm OPENING DEFINED IN PMMA BY E-BEAM AND GATE RECESS ETCHED



3. ALUMINUM DEPOSITED AND LIFTED

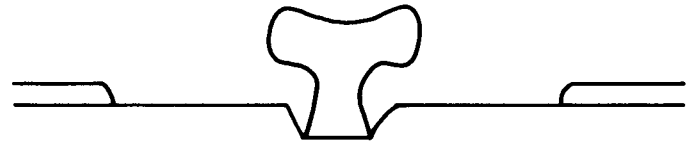


Figure 2-9. Schematic of Tee-gate technology - Method II

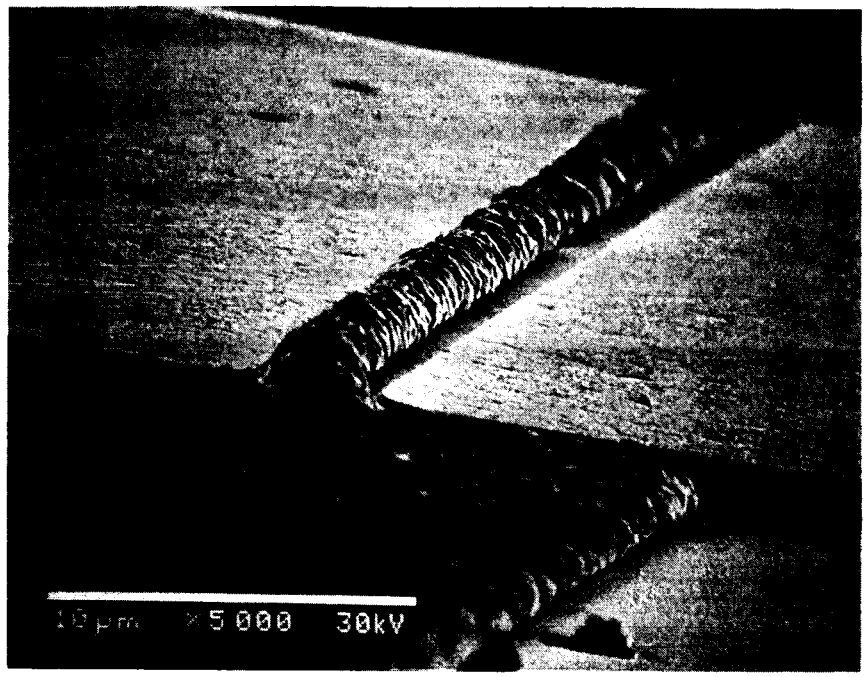
- The area to be plated is calculated and gold is electroplated using a current density of 3 mA/cm until the final metal "spills" over the top of the resist to a length of 2 μm. This forms the tee top. The resist is removed using "liftoff."
- Standard wafer processing is used to complete the wafer.

Figure 2-10 shows SEM photographs of plated tee-section Ti/Pt/Au gates.

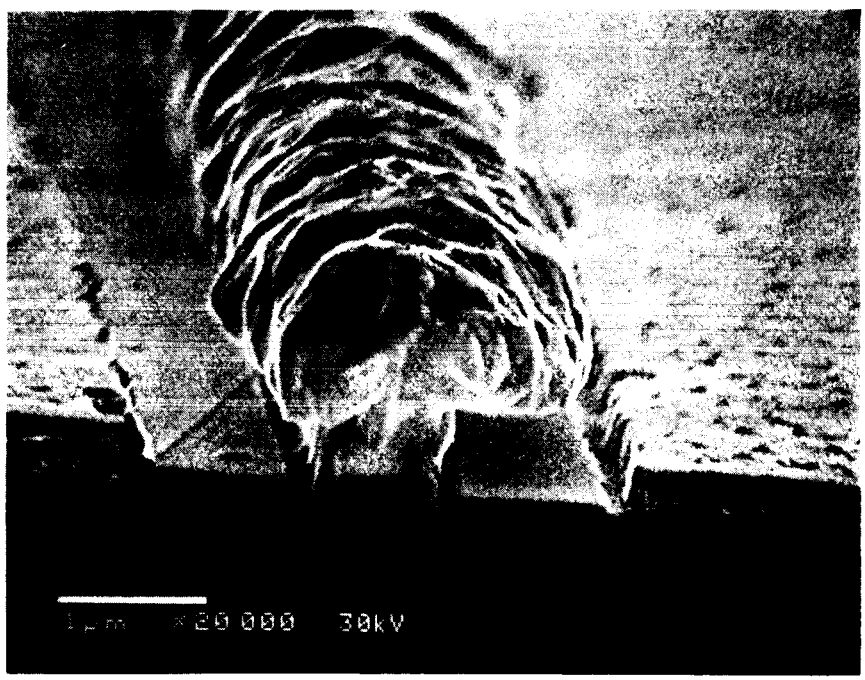
2.4 DC CHARACTERIZATION

Chips are probed individually after dicing for the following parameters: I_{DSS}, G_M, V_p, V_F, V_{RB}.

I_{DSS} is the saturated current between drain and source. This value is measured at 4 V between the drain and source terminal. Dice are sorted according to their I_{DSS} currents per cell. Typically, the higher current



(A) ANGLE VIEW OF COMPLETE GATE AND PLATED GATE-PAD



(B) CLEANED CROSS SECTION SHOWING RECESS

Figure 2-10. SEM photographs of plated Tee-section Ti/Pt/Au gates

devices give higher RF output power. A derived current range was established for high power output with good efficiency from device performance feedback. This current range was 250 mA to 330 mA per mm.

The transconductance, G_M, is measured from the slope of the transfer characteristic between V_{GS} = 0 and V_{GS} = 1 V with V_{DS} = 4 V. A higher G_M generally gives higher small signal gain, but it does not necessarily imply that more output power can be obtained. Performance data also showed that higher small signal gain is not necessarily related to higher device efficiency. However, these parameters are useful in sorting dice, and facilitates internal matching once a matching network has been designed.

The pinchoff voltage, V_p, is the gate bias at which the drain current has been reduced to 10 percent of I_{DSS}. Devices that do not "pinch off" usually indicate soft active-layer buffer-layer interface or nonuniformity in the material; they are rejected from probing.

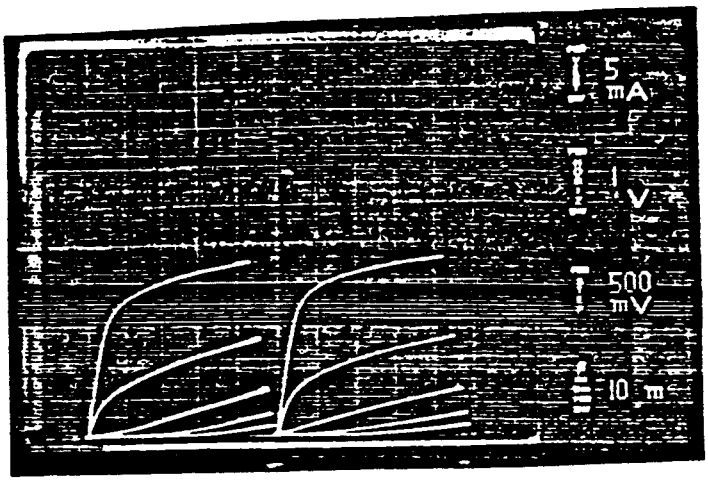
The forward voltage, V_f, is defined as the two terminal voltage between gate and drain which creates a forward current of 5 mA per cell. The forward voltage generally ranges between 0.6 and 1 V; typically not a limiting parameter to the RF performance.

The reverse breakdown voltage, V_{rb}, is defined as the two-terminal voltage between gate and drain which sets off a reverse breakdown current of 5 mA per cell. Normally, a higher reverse breakdown voltage is desired because it will result in a reduction in reverse dc gate current during operation. It was observed that dc data did not always predict RF performance. It was found, however, that sorting dice according to similar values of the dc parameters described above greatly improves the RF yield and predictability of devices once the proper dc values have been established.

Other dc parameters such as gate resistance, R_g, open channel resistance, R_o, contact resistance, R_c, and parasitic resistance, R_p, can be characterized from the test pattern. Table 2-1 shows the single 100 μm gate width test pattern transistors on Wafer 17K82A, which were characterized in detail. Figure 2-11 shows curve tracer photographs of the characteristics for a test pattern near the center of Wafer 19H7A. Note that the open channel current to I_{DSS} ratio is greater than 2, which may indicate a high buffer acceptor trap density not ideal for good RF performance. Figure 2-12 shows photographs of the two device types and test pattern taken immediately after gate definition.

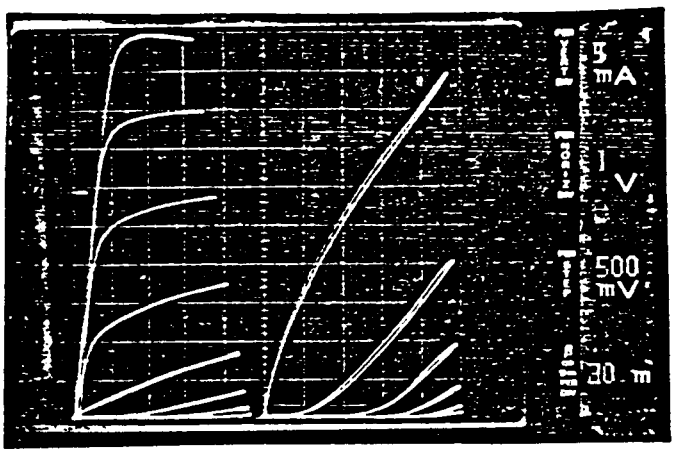
Table 2-1. DC characterization data on 178K82A test pattern

PARAMETER (PER 100 μm GATE WIDTH)	VALUE
I_{DSS}	39 mA
MAXIMUM OPEN CHANNEL CURRENT - I_m	50 mA
KNEE VOLTAGE - V_k	0.9 V
LOW FIELD PINCHOFF VOLTAGE - V_p	3.4 V
GATE BARRIER HEIGHT - V_b	0.64 V
GATE IDEALITY FACTOR - n	1.38
TOTAL PARASITIC SOURCE AND DRAIN RESISTANCE - R_S+R_D	10Ω
CONTACT RESISTANCE (SOURCE AND DRAIN) - R_c	3.3Ω
TOTAL PARASITIC CHANNEL RESISTANCE - $R_{ps}+R_{pd}$	3.4Ω
OPEN CHANNEL RESISTANCE - R_o	5.9Ω
MEASURED (EXTRINSIC) TRANSCONDUCTANCE AT V_{DS} = 4, G'_m	12 mS
INTRINSIC TRANSCONDUCTANCE - G_m	12.8 mS
GATE RESISTANCE - R_g	18Ω
GATE BREAKDOWN VOLTAGE AT 1 mA - V_{gdb}	14 V



DARK LIGHT

Drain Characteristics to I_{dss}

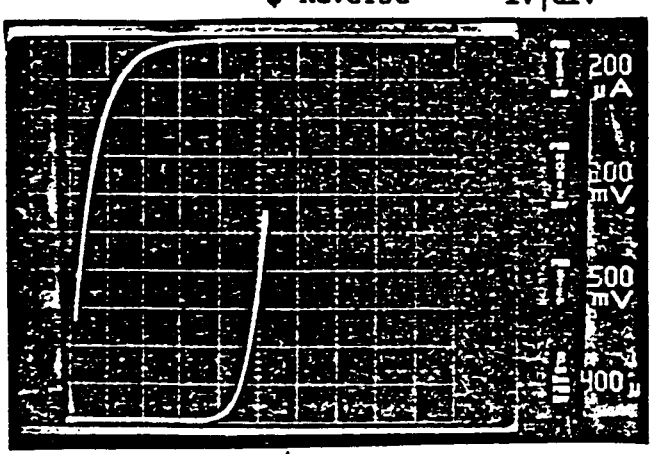


+1.55 V ↑ Forward Offset

↑ 1mA|div

Drain Characteristics to Open Channel and Details of Pinch-Off in Dark.

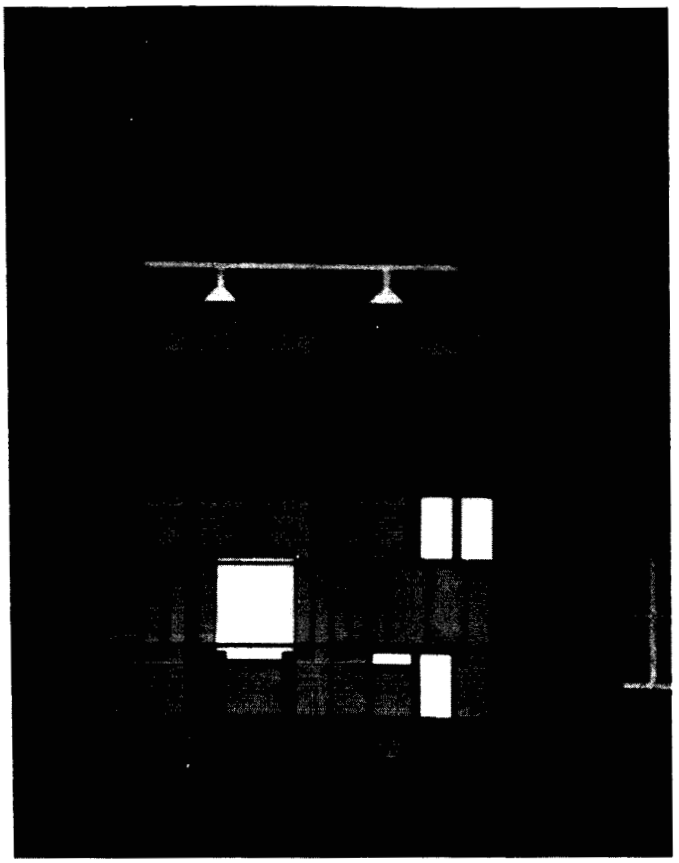
↓ Reverse 1V|div



↑Forward 0.2V|Div

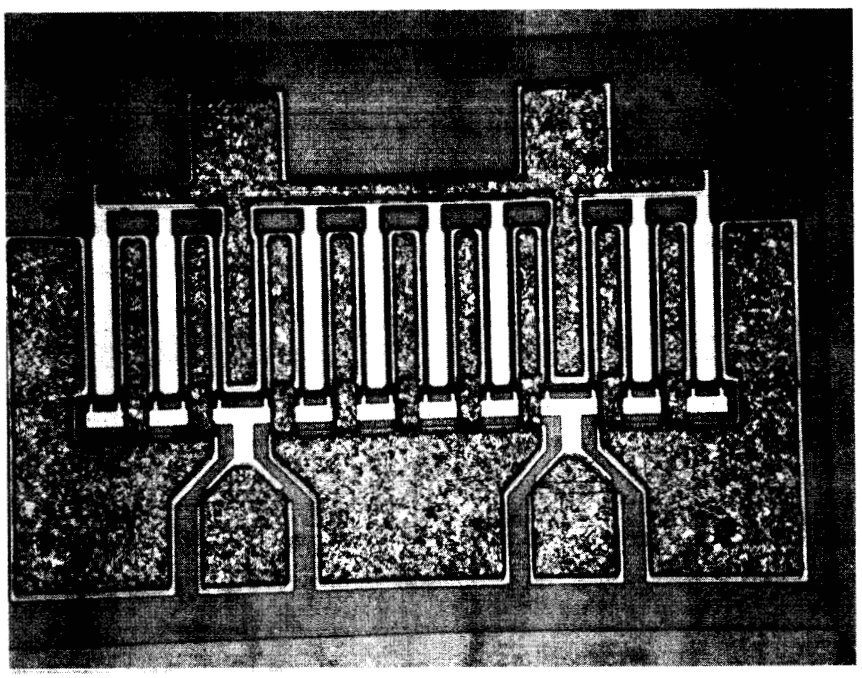
Gate Diode Characteristics

Figure 2-11. DC characteristics of 100-μm test pattern transistor on wafer 17H7A after gate definition



CONVENTIONAL DEVICE

TEST PATTERN



LADDER TYPE DEVICE

Figure 2-12. Photographs of S102 type devices on wafer 17H7A after gate definition

2.5 THERMAL CHARACTERIZATION

The thermal property of a FET is generally characterized by the thermal impedance, θ, which is defined as

$$\theta = \frac{(T_c - T_o)}{P_{dis}}$$

where T_c is the channel temperature, T_o the baseplate temperature, and P_{dis} the dissipated power. Different gate peripheries of the FETs are usually characterized by the normalized thermal impedance $\bar{\theta}$, which is defined as

$$\bar{\theta} = \theta W$$

where W is the total gate periphery of the FET under test. The dimension of the normalized thermal impedance is °Cmm/Watt.

Two methods of measurement on the thermal impedance are performed at SMDO. The liquid crystal measurement technique and the electrical measurement technique. These two measurement methods are described briefly below.

Figure 2-13 shows a setup of the liquid crystal measurement. Because liquid crystal is Electrically nonconductive, it does not short out the FET. The long molecules become randomly oriented and the liquid becomes optically inactive above a particular temperature. The thermal impedance can be obtained when the dissipated power is known at the transition temperature. This method is useful and accurate in determining the peak value of the thermal impedance. The electrical method employs the characteristic that unbiased forward gate voltage is inversely proportional to the channel temperature at a fixed gate-source forward current. This measurement is carried out with a Sage Die Attachment Evaluator (DAE 220A). Logic circuit in the instrument generates microsecond pulses with 50 Hz repetition rate. The pulse width is much shorter than the thermal time constant to avoid junction cooling. The heating period is much longer than the current pulse width to ensure that the average and peak heating powers are essentially the same. This method determines the average channel temperature instead of the peak.

Sample devices from Wafer 16I18A have been thermally characterized using the liquid crystal technique. The mean values of the normalized thermal impedance for the conventional and ladder-type devices are 95.6 and

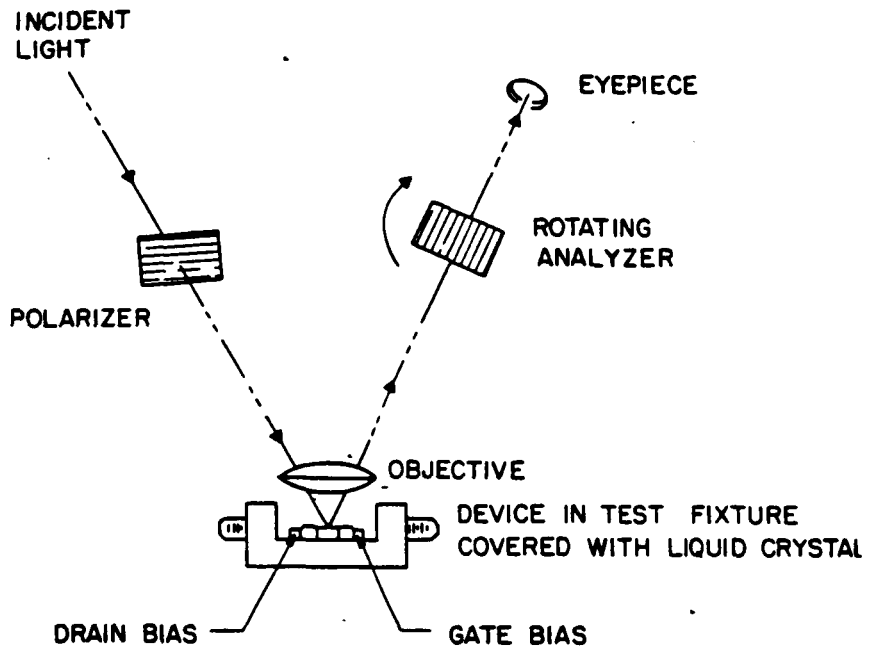


Figure 2-13. Test setup of liquid crystal measurement

64.1°C mm/W, respectively. Table 2-2 gives data of this measurement. Table 2-3 shows thermal characterization data of sample devices from 17H7A using the pulsed electrical method. The mean values of the normalized thermal impedance for the conventional and ladder type devices are 55 and 33.8°C mm/W, respectively. Both data show that the thermal resistance of the C-type device is a factor 1.6 higher than the ladder structure, a consequence of its closer packed geometry. Values of thermal impedance measured by the liquid crystal method, however, are almost twice as high compared with those measured by the electrical pulse method. It was found that the transition temperature of the liquid crystal used is dependent on the film thickness, so that the thermal impedance measured by the electrical method is considered more accurate.

Table 2-4 shows the thermal resistance evaluation of 204 devices. In this case, the values of thermal resistance measured from the electrical method are higher than those measured from the liquid crystal method. This may account for the disappointing performance of the S204 devices.

Table 2-2. Thermal resistance of 102 type devices from wafer 16I18A

TYPE AND NO.	R_{th} (°C/W)
C 1	61.9
C 2	41.7
C 3	39.8
	MEAN = 47.8
L 1	43.5
L 2	30.3
L 3	28.4
	MEAN = 34.1

Table 2-3. Thermal characterization data pulsed electrical method using DAE 220

DEVICE NO.	THERMAL RESISTANCE AT APPROX. 80°C T_{TH} (°CW^{-1})	NORMALIZED VALUE R_{TH} Z °$CmmW^{-1}$
17H7A C 5	26.0	52.0
C 7	28.5	57.0
	MEAN 27.3	MEAN 55.0
17H7A L 2	16.0	32.0
L 4	18.3	36.6
L 5	16.3	32.6
	MEAN 16.9	MEAN 33.8
RPK 9030 DEVICE (Z = 1.6 mm)	23.3	37.3

Table 2-4. Thermal resistance evaluation of 204 devices

	SAGE DAE					LIQUID CRYSTAL (T_{CH} = 81.3°C)				
DEVICE NO.	S/D CONNECT	V_{DS}	I_{ds}	R_{th} (°C/W)	R_nZ (°Cmm/W)	S/D CONNECT	V_{DS}	I_{ds} (A)	R_{th} (°C/W)	$R_{th}Z$ (°Cmm/W)
15J3B #3							1.61	1.47	23.9	95.6
15J3B #4	NORMAL	2.0	1.96	32.0	128.0		1.63	1.57	21.8	87.2
15I58B #3	NORMAL	1.5	1.82	26.4	106.0		1.45	1.58	24.4	97.6
15J5B #3	NORMAL	2.0	2.3	56.0	204.0					
	REVERSE	2.0	2.2	67.8	271.0					
17E42B #1 (102 DEVICE)	NORMAL	2.0	0.73	26.1	52.2		3.97	3.99	35.3	70.6
	REVERSE	2.0	0.70	28.2	56.4					

2.6 RF CHARACTERIZATION

S-parameter measurements over 2 to 18 GHz were performed on two C-type and one L-type S102 devices from wafer 17H90A, selected because they have dc parameters similar to the best performing chips from this wafer. The chips, assembled on 50-ohm carriers using the same ribbon bond configuration as the RF tested units were measured on the HP ANA and calibrated using microstrip calibration pieces to a reference plane at the bond wires. The two C-type devices gave essentially identical data. The C- and L-type data were, however, significantly different. Tables 2-5 and 2-6 give the raw data for both device types. It is clear that while S11 and S22 are similar for the two designs, |S21| is typically 2 dB lower over the whole frequency range for the ladder type device. The |S21| data is reproduced graphically in Figure 2-14.

Figures 26-15 and 2-16 show typical RF performance of S102 devices from Wafer 17H6B at 20 GHz and 19 to 22 GHz. At 20 GHz, it shows a comb-type device which gives 1 Watt with 5 dB gain and 19 percent efficiency at 1 dB compression. Over the required bandwidth, the performance was achieved with 1 Watt and 4.5 dB associated 1 dB compressed gain at band center. Because the ladder-type devices did not perform as well as the comb type (gain was typically 1 dB lower, although saturated power output was essentially the same) the structure was abandoned early into the program. Table 2-7 shows a summary of RF data on 17H6B devices.

Table 2-5. Measured S-parameters over 2 to 18 GHz on C-type S102 devices from wafer 17H90A

FREQUENCY (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
2000	0.84	-133	4.33	101	0.054	26	0.42	-163
2500	0.83	-143	3.52	94	0.054	23	0.43	-162
3000	0.83	-153	2.88	88	0.052	23	0.45	-165
3500	0.85	-158	2.40	85	0.052	20	0.47	-166
4000	0.86	-161	2.07	82	0.049	17	0.48	-165
4500	0.87	-162	1.91	76	0.047	18	0.49	-164
5000	0.88	-161	1.80	72	0.048	18	0.49	-161
5500	0.86	-162	1.68	71	0.047	14	0.49	-162
6000	0.84	-162	1.60	71	0.047	19	0.48	-161
6500	0.83	-166	1.48	71	0.049	17	0.49	-163
7000	0.84	-171	1.33	70	0.048	16	0.50	-165
7500	0.86	-174	1.20	66	0.048	15	0.52	-171
8000	0.89	-177	1.05	60	0.048	14	0.55	-172
8500	0.90	-177	0.93	52	0.049	13	0.57	-172
9000	0.91	-178	0.88	44	0.048	12	0.59	-172
9500	0.91	-177	0.90	39	0.046	13	0.60	-169
10000	0.89	-179	0.95	37	0.047	19	0.61	-166
10500	0.87	180	1.00	40	0.049	25	0.61	-164
11000	0.87	176	0.98	43	0.057	24	0.61	-163
11500	0.88	174	0.89	45	0.071	24	0.61	-163
12000	0.92	176	0.73	43	0.067	-8	0.60	-162
12500	0.93	177	0.63	37	0.049	-2	0.61	-164
13000	0.93	180	0.54	31	0.045	3	0.62	-163
13500	0.93	-177	0.53	22	0.039	7	0.62	-163
14000	0.93	-175	0.53	21	0.037	15	0.60	-169
14500	0.91	-174	0.62	24	0.035	22	0.63	-171
15000	0.90	-178	0.69	32	0.033	24	0.65	-172
15500	0.95	175	0.73	39	0.030	21	0.69	-175
16000	1.06	168	0.69	41	0.030	7	0.76	-176
16500	1.11	165	0.50	36	0.027	-6	0.80	-175
17000	1.03	167	0.35	22	0.025	-22	0.78	-173
17500	0.96	170	0.29	2	0.027	-36	0.80	-170
18000	0.92	173	0.30	-11	0.032	-39	0.79	-165
18500	0.89	174	0.41	-14	0.035	-35	0.74	-162

RPE(IN) = 0 CM
RPE(OUT) = 0 CM

Table 2-6. Measured S-parameters over 2 to 18 GHz on C-type S102 devices from wafer 17H90A

FREQUENCY (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
2000	0.86	-141	3.25	96	0.057	21	0.49	-166
2500	0.86	-150	2.60	89	0.056	19	0.50	-169
3000	0.87	-159	2.11	84	0.054	18	0.51	-172
3500	0.88	-163	1.75	81	0.053	15	0.54	-173
4000	0.89	-166	1.51	78	0.051	12	0.55	-173
4500	0.90	-166	1.38	72	0.049	13	0.56	-172
5000	0.90	-165	1.28	67	0.049	13	0.57	-169
5500	0.89	-166	1.21	65	0.047	10	0.58	-169
6000	0.88	-165	1.13	67	0.048	14	0.58	-163
6500	0.87	-168	1.05	67	0.049	12	0.58	-163
7000	0.87	-172	0.94	67	0.047	11	0.59	-169
7500	0.88	-174	0.84	64	0.047	11	0.61	-171
8000	0.91	-176	0.74	59	0.048	11	0.62	-171
8500	0.92	-178	0.67	50	0.049	9	0.63	-171
9000	0.92	-178	0.64	41	0.048	9	0.64	-172
9500	0.93	-179	0.67	36	0.047	9	0.65	-172
10000	0.90	178	0.69	32	0.046	12	0.65	-172
10500	0.89	177	0.73	33	0.048	18	0.66	-172
11000	0.90	173	0.72	36	0.055	20	0.68	-174
11500	0.91	172	0.65	38	0.078	16	0.68	-174
12000	0.94	175	0.51	38	0.061	-16	0.69	-170
12500	0.95	177	0.42	34	0.045	-9	0.71	-163
13000	0.95	-180	0.36	29	0.041	-3	0.71	-166
13500	0.94	-176	0.36	20	0.036	2	0.69	-161
14000	0.94	-174	0.37	20	0.033	11	0.64	-160
14500	0.93	-172	0.46	26	0.032	17	0.62	-163
15000	0.93	-176	0.52	32	0.032	17	0.82	-169
15500	0.97	176	0.56	37	0.031	11	0.67	-177
16000	1.10	168	0.55	34	0.032	-2	0.79	176
16500	1.14	163	0.39	27	0.028	-17	0.82	174
17000	1.04	165	0.26	15	0.025	-35	0.80	175
17500	0.96	168	0.19	-4	0.027	-52	0.82	177
18000	0.93	171	0.19	-17	0.029	-56	0.82	-177
18500	0.90	172	0.26	-22	0.031	-52	0.80	-170

RPE(IN) = 0 CM
RPE(OUT)= 0 CM

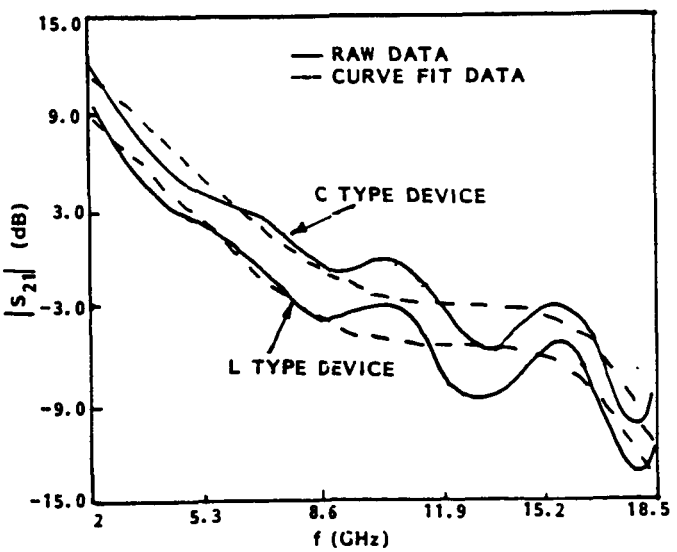


Figure 2-14. Comparison of |S21| for comb type and ladder type 102 devices

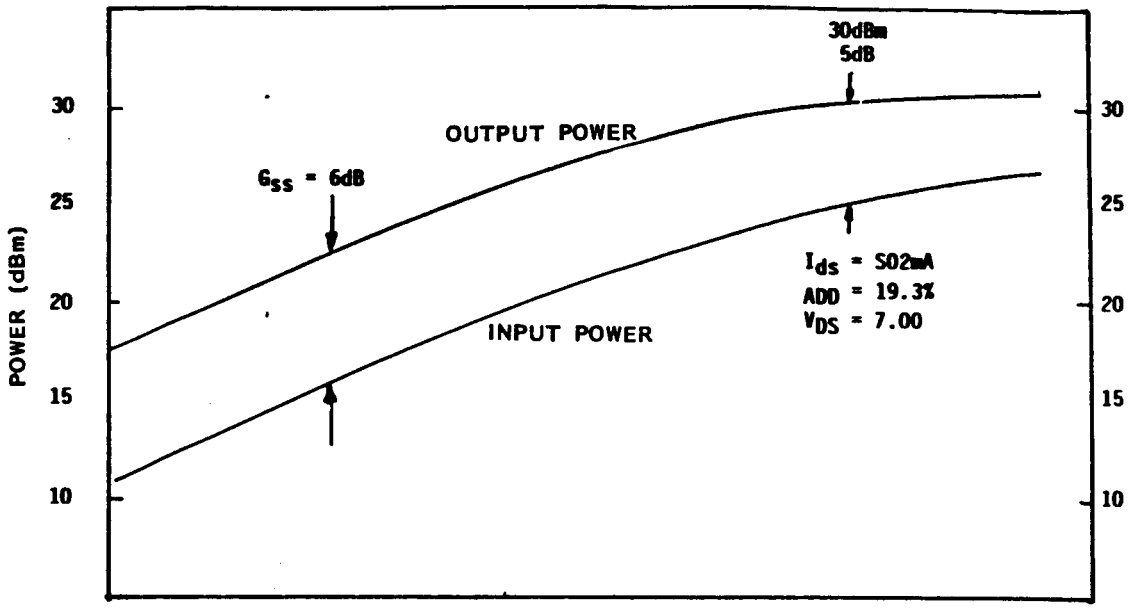


Figure 2-15. Performance of S102 device 17H6B #02 at 20 GHz

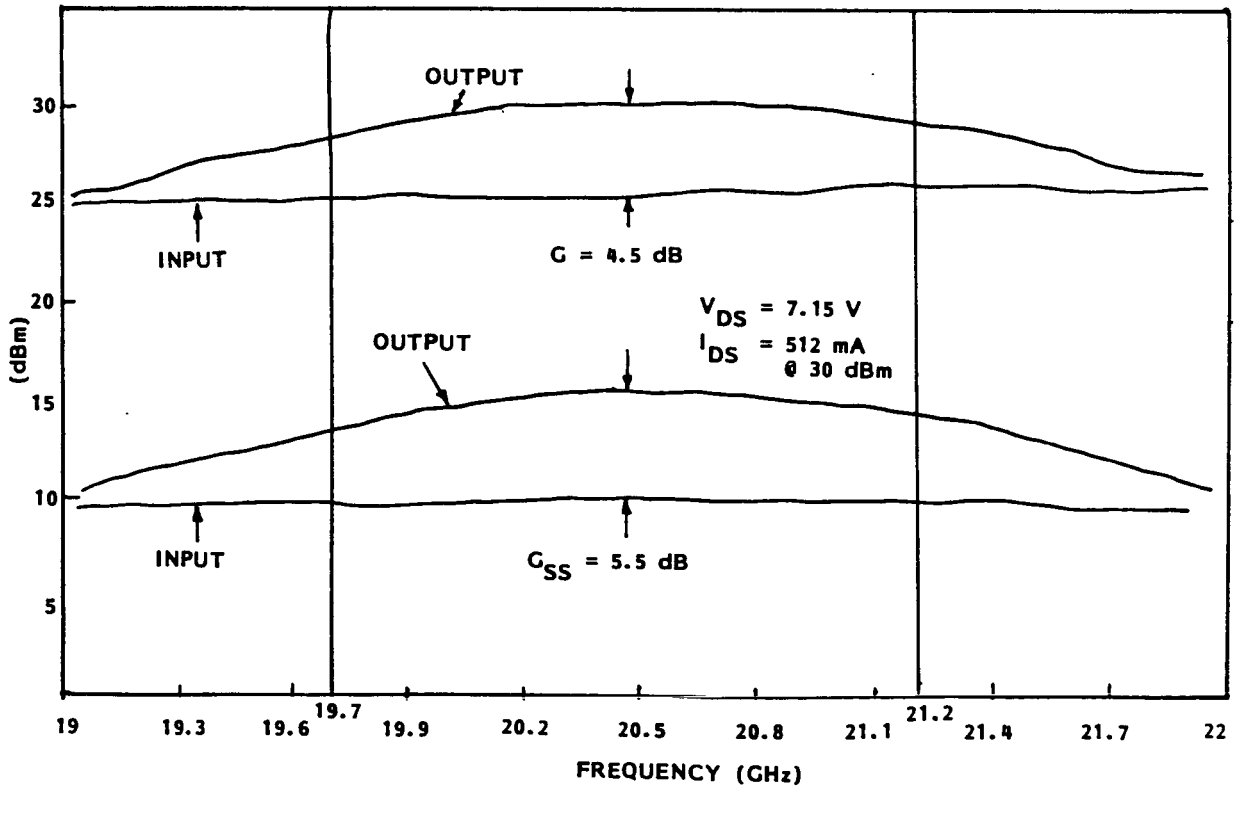


Figure 2-16. Bandwidth performance of device 17H6B #01

Table 2-7. Summary of RF data on 17H6B devices

DEVICE NO.	V_{DS}	V_{GS}	1-dB COMPRESSION AT f=20 GHz				NOTES
			I_{ds} (mA)	P_{OUT} (dBm)	G (dB)	η_{ADD} (5)	
C 1	7.34	-0.77	477	30.0	4.5	18.4	
C 2	7.07	-1.01	502	30.0	5.0	19.3	
C 3	7.18	-0.79	469	30.0	4.5	19.1	
C 4	6.73	-0.97	426	29.5	4.0	18.7	
L 2	7.11	-0.95	479	29.0	3.0	11.6	
L 3	7.04	-0.8	676	30.0	2.0	7.8	INPUT SUB-STRATE WRONG

Computer modeling was performed for the S204 device. S parameters over the 2 to 18 GHz range were measured and compared with data from the distributed model. Figure 2-17 shows plots of the magnitude of S21, where the measurements have remarkably similar characteristics. Table 2-8 shows data of RF characterization of 204 devices. The best output power obtained was 32.5 dBm with 3.3 dB gain and 16.9 percent efficiency.

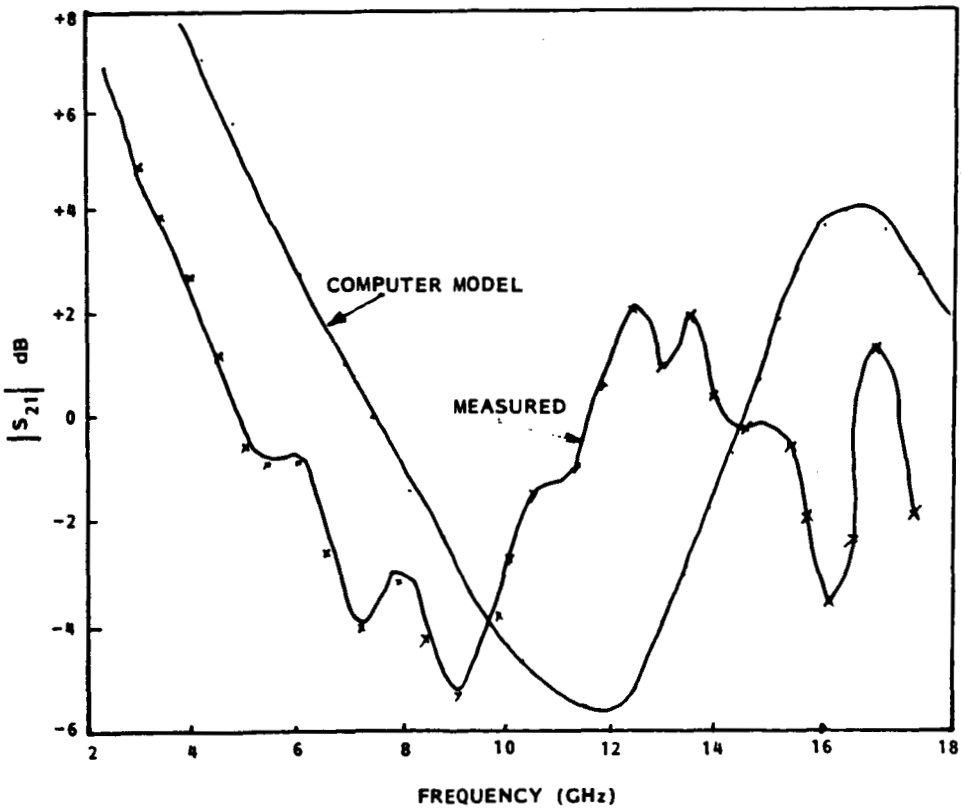


Figure 2-17. Comparison of modified and measured $^2S_{21}$) band for 204 device in "opposite-end" bonding configuration

Table 2-8. RF characterization of 204 devices

DEVICE NO..	DC DATA						1 dB COMPRESSION			
	I_{dss} (mA)	G_m (mS)	V_p @ I_{ds} (mA)	V_{GdB} @ 1 mA	V_{DS}	V_{GS}	P_o (dBm)	G (dB)	η_{ADD} (%)	P_{SAT} (dBm)
15I588#A1	1100	340	5 AT 100	7.0	7.5	-2.1	32.5	3.3	16.9	>32.8
15J1B#2	1200	300	4 AT 200	6.8	8.0	-1.5	32.5	3.0	15.2	32.5
15J2B#1	1500	300	7 AT 100	8.5	8.0	-2.6	32.0	3.0	11.0	>32.0
15J5B#2	1200	300	5 AT 50	12.0	8.6	-1.6	32.0	2.5	12.1	32.0
15J88A#1	1400	300	6 AT 30	8.8	8.0	-2.5	~32.0	2.0	<10.0	~32.0
17K82B#1	DEVICE BLEW WHILE TUNING				G_{SS} = 4 dB					

Two spike profile wafers (17B18A and 17H22B) were evaluated at 20 GHz, results are given in Table 2-9. Wafer 17H22B gave poor performance, probably because of its low transconductance. Wafer 17B18 behaved no better than the best flat profile wafers at 20 GHz. This limited experiment indicates that no advantages to spike profiles at K-band frequencies exist.

Table 2-9. RF evaluation of spike profile wafers

DEVICE NO.	DC DATA			1 dB COMPRESSION				
	I_{dss} (M)	g_m (mS)	V_{gdB} @ 1 mA	V_{DS}	V_{GS}	P_{OUT} (dBm)	G (dB)	η_{ADD} (%)
17H22B/3	640	110	14.5	8.3	-2.5	30.0	2.0	12.3
17B18B/2	560	160	12.0	9.2	-1.9	30.0	4.0	17.8
/3	610	180	13.2	8.1	-2.0	30.0	4.0	22.3
/4	500	200	14.0	9.4	-1.8	30.5	3.5	24.5

An experiment was conducted to combine two newly developed S246 devices paralleled on the 0.246 inch carrier and matched aiming at the 19.7 to 21.2 GHz band. The results for this 2.4 mm gate width combination are shown in Figure 2-18. The device gave 1 dB compressed performance of 31.5 dBm with 5.5 dB associated gain and 20.3 percent efficiency at band center.

The single cell S900 A1 Tee-gate devices from wafer 15N74B were RF characterized at 20 GHz with results similar results to those reported on the earlier wafer. The devices oscillated severely until the Silox passivation layer was etched away, after which they gave 5 to 6 dB small signal

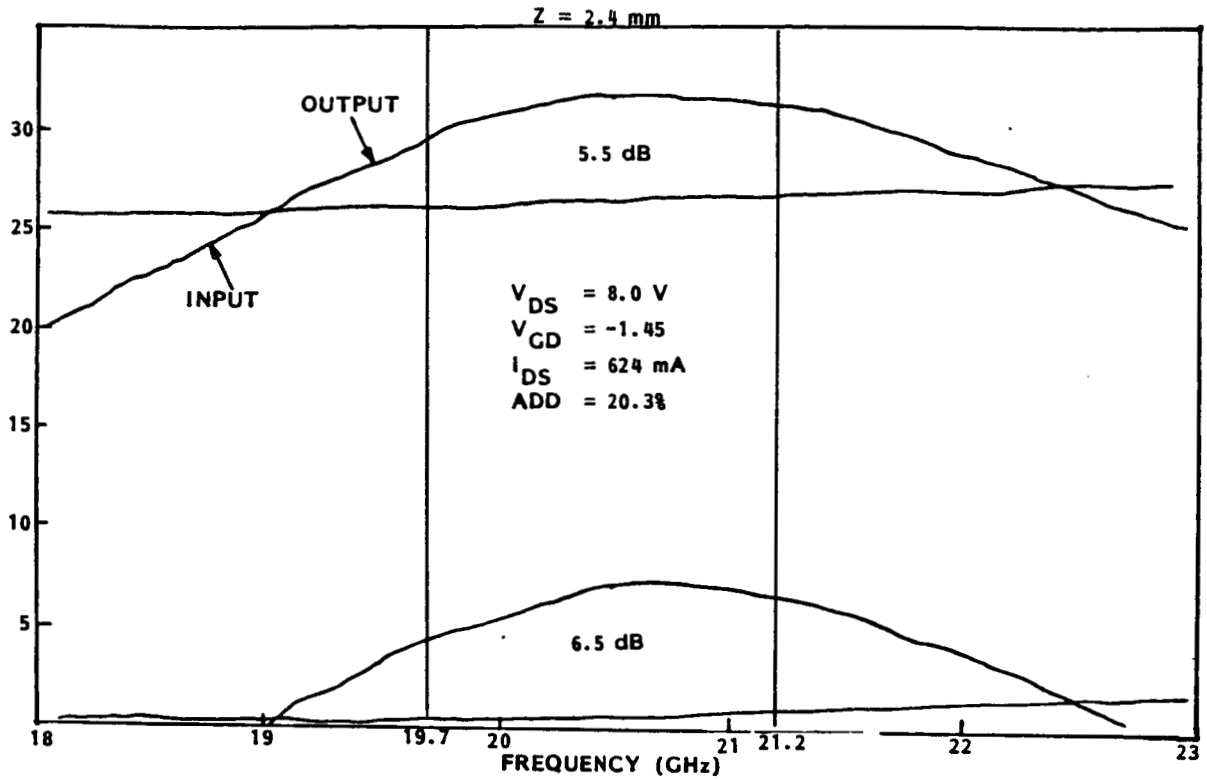


Figure 2-18. Performance of pair of 246 chips in parallel on 0.248" carrier

gain but poor saturated power performance. The devices burned out very easily when operated at high drive levels. Confirmation of this highly unsatisfactory performance led to the abandonment of this structure.

2.7 RF TEST DATA

From the RF characterization given in the last section, it was concluded that the devices developed for this program did not fully meet the original specifications. Since this is a development program, it is agreed that delivery of 20 carrier-matched 1 Watt devices and 10 carrier-matched 2 Watt devices would be on a best-effort basis at the conclusion of the program. Table 2-10 shows RF data of 20 carrier-matched 1 Watt devices at 20.4 GHz tested before shipment. The devices are the new RPK 2020, S202-100, developed from other similar programs. The output power was taken at 25 dB input power. It can be seen that the small signal gain of most of the devices exceed 6 dB. The efficiency would have to exceed 20 percent if the input power is driven more than 1 dB into compression. The typical RF performance of these devices is shown in Figure 2-19.

Table 2-10. Test data of twenty 1-Watt carrier matched devices at 20 GHz before shipment

DC PARAMETERS			RF PERFORMANCE AND BIAS CONDITIONS					
I_{DSS} AT V_{DS}=5 V (mA)	G_M (mS)	I_{DS} AT V_p=-5.5 V (mA)	V_{DS} (V)	V_{GS} (V)	I_{ps} (mA)	SMALL SIGNAL GAIN (dB)	OUTPUT POWER AT INPUT POWER = 25 dBm (dBm)	(%)
753	276	30	7.50	-0.82	609	6.7	30.5	17.5
744	276	31	7.50	-0.93	700	6.0	30.5	14.6
953	243	98	7.50	-1.01	763	5.8	30.1	12.2
741	272	30	7.50	-0.80	618	5.3	30.0	14.4
800	256	56	7.50	-1.00	636	6.0	30.1	15.0
710	271	32	7.50	-0.73	638	6.1	30.6	16.9
734	270	43	7.50	-0.88	600	6.3	30.6	18.8
940	232	100	7.50	-0.83	779	5.8	30.0	11.7
825	246	80	7.50	-0.95	704	6.0	30.0	13.1
851	254	63	7.50	-0.95	692	6.0	30.0	13.2
837	263	60	7.50	-1.05	637	6.2	30.0	14.3
891	249	67	7.50	-1.15	681	6.4	30.8	17.3
964	238	50	7.50	-0.95	786	6.6	30.7	14.6
925	219	92	7.50	-1.12	756	6.0	30.7	15.1
843	258	51	7.50	-1.07	645	6.3	30.5	16.8
795	287	37	7.50	-0.95	638	6.0	30.1	14.8
842	270	67	7.50	-0.91	681	5.5	30.0	13.4
954	248	90	7.50	-1.00	765	5.8	30.2	12.7
904	254	100	7.50	-0.97	740	6.0	30.6	15.0
808	261	58	7.50	-0.95	624	6.0	30.5	17.2

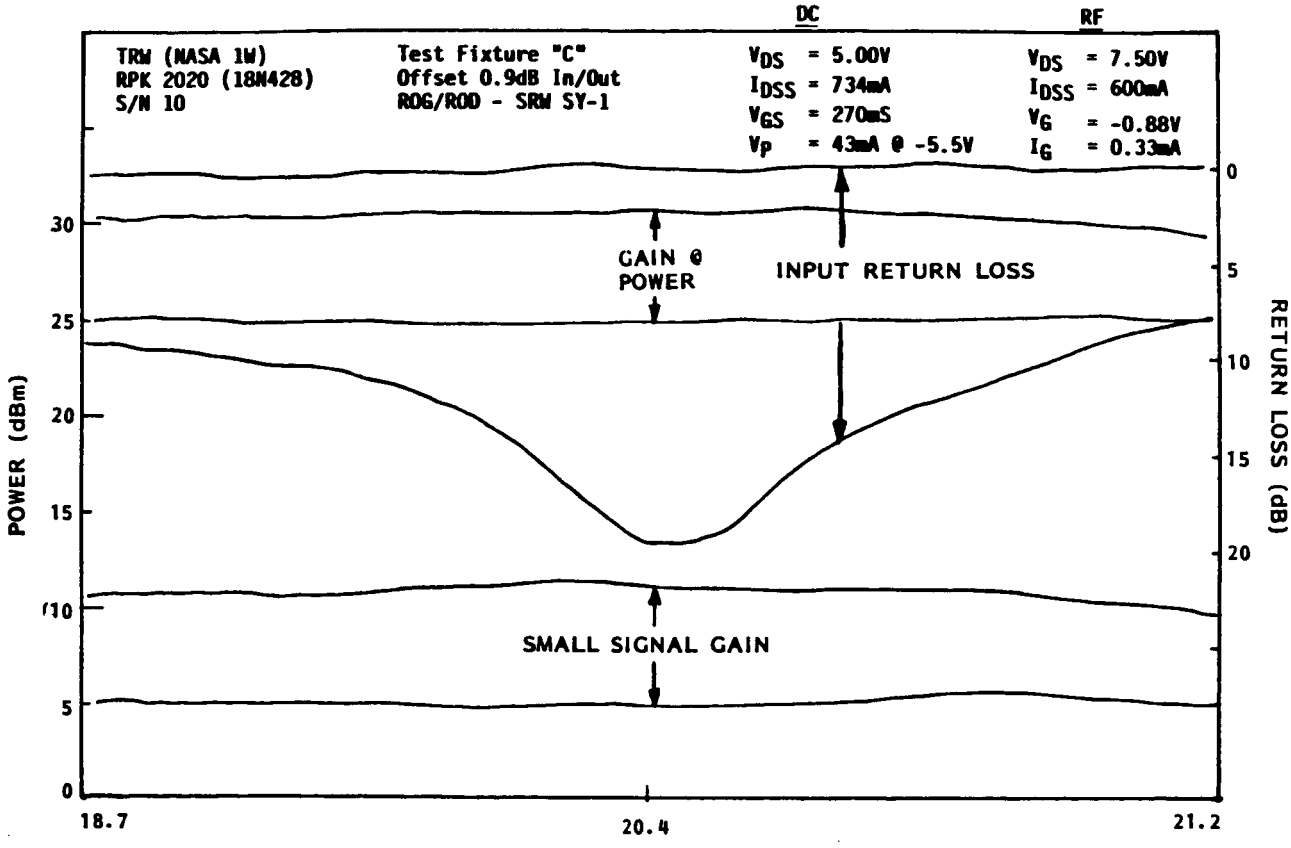


Figure 2-19. Typical RF performance of 20 shipped carrier-matched 1-W devices using S202-100

Figure 2-20 shows RF performance of S/N 04 carrier-matched 2 Watt device; ten of these devices have been shipped. These devices used the modified Wilkinson power divider/combiner (see Figure 2-21) to combine two S202-100 device chips.

2.8 CONCLUSIONS AND RECOMMENDATIONS

From the results of the original specifications for both the 1 Watt and 2 Watt devices, it is clear they are pushing the current state-of-the-art to its limit. Increasing the gate periphery by using either the via-hole or air-bridge structure may not improve output power, because it becomes more difficult to match the device. As the gate periphery is increased, there is also an increased chance of resonance in the device. Two side-by-side combined S102 devices performed better than one single S204 device, which suggests a single cell 204 device is suffering from resonance. One way to eliminate these oscillations is to separate the device into several cells

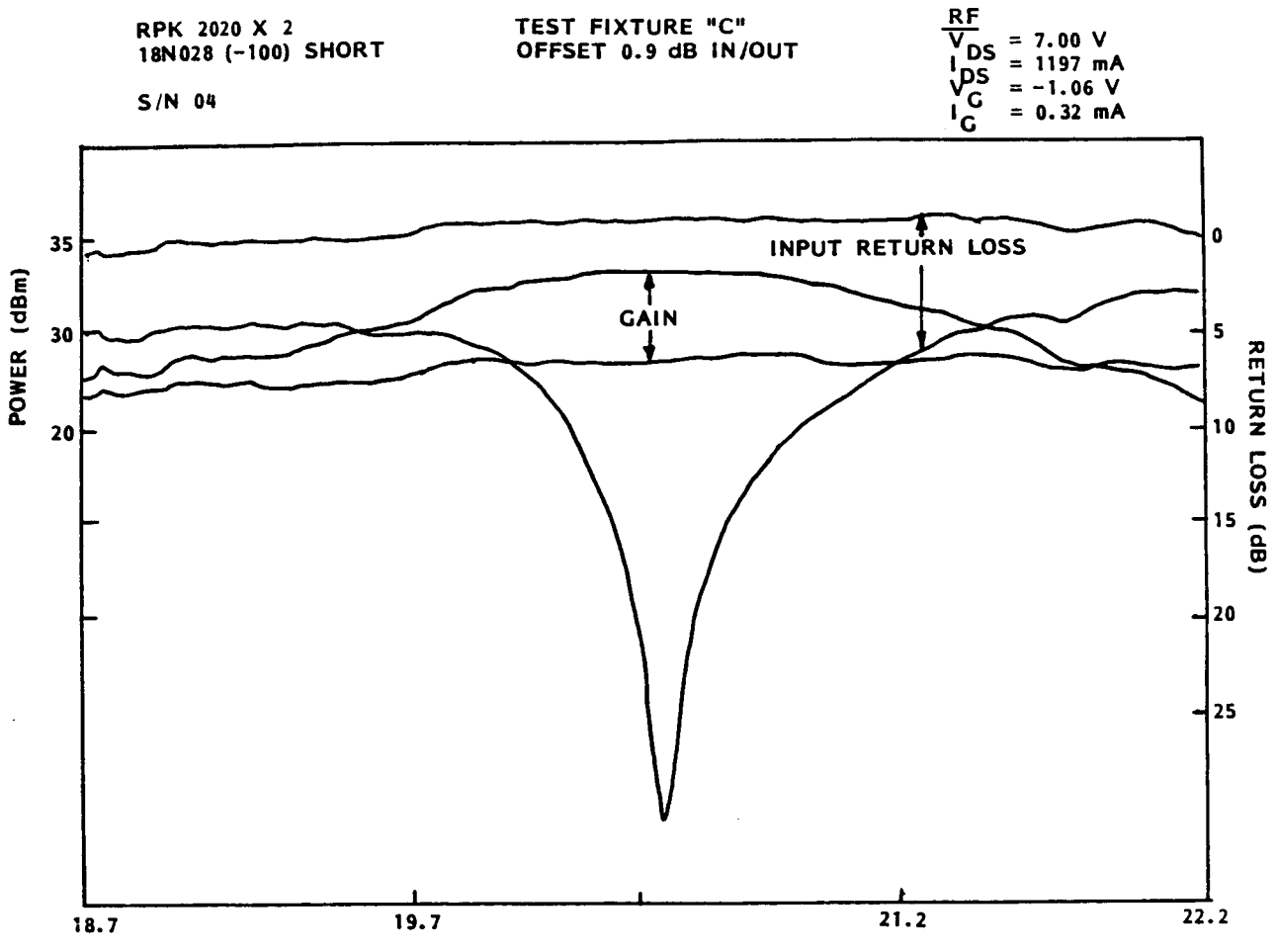
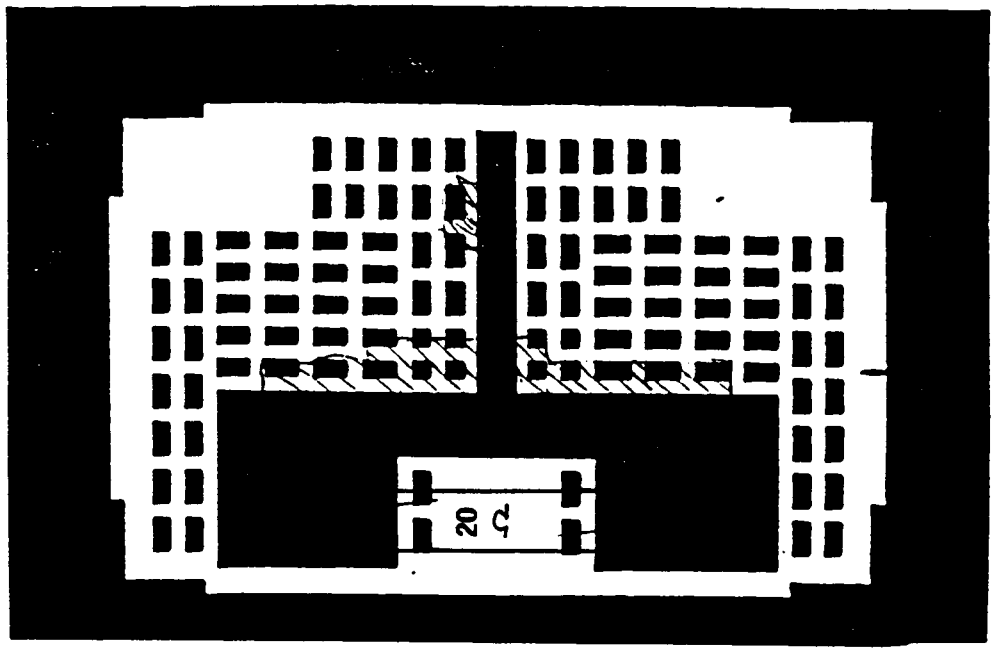


Figure 2-20. RF performance carrier-matched device S/N 04 using two combined S202-100 devices



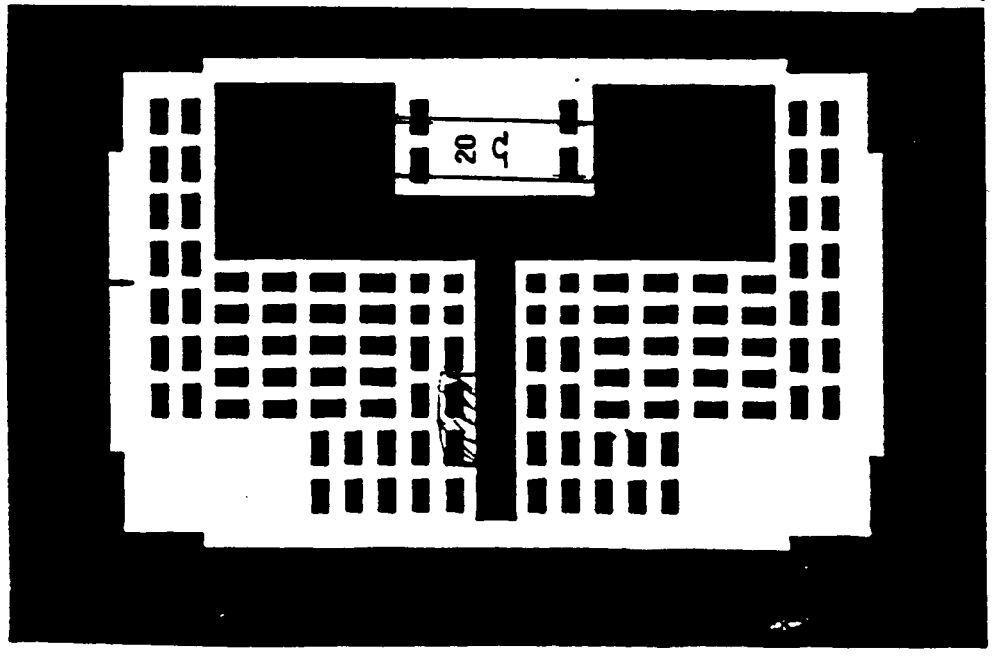


Figure 2-21. Matching pattern of shipped 2-W devices which use modified Wilkinson power divider/combiner

and isolate each one. This will create the same problem as the number of cells is increased.

Tee-gate devices which did not show significant improvement in RF performance, can be explained as follows: 1) It could increase the gate-drain capacitance, thus increasing the power feedback from output to input and may cause oscillation, and 2) the skin depth was reduced at high frequency. Reducing the dc gate resistance does not necessarily reduce the RF gate resistance.

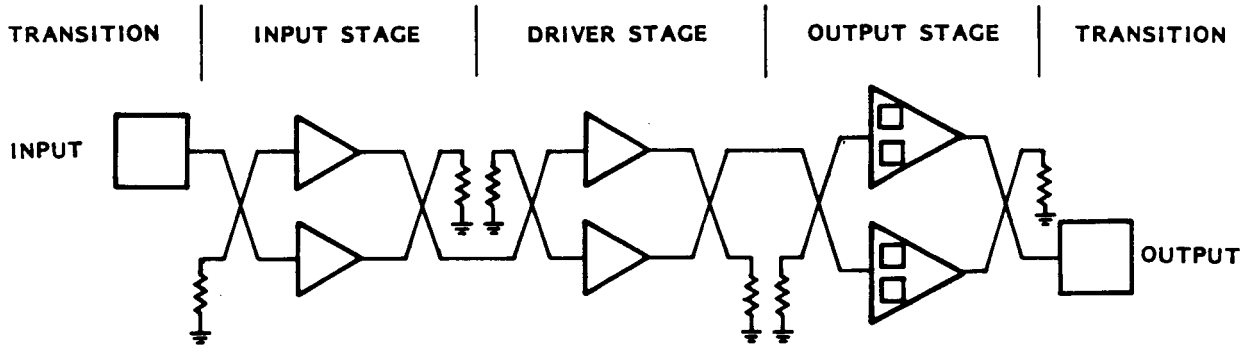
New approaches seem inevitable if performance goals become more ambitious. An improvement to the existing approach would be on-chip power combination where the chip is no longer a single FET but contains integrated FETs. These FETs are either cascaded or combined with internal matching circuits. This "super chip" will contain resistors and capacitors and may be considered an embryonic MMIC chip. Another approach worth considering is the dual-gate FET. It provides more gain in the low noise devices. Larger gain means higher efficiency for the power FET.

3. HIGH POWER AMPLIFIER DESIGN

The high power amplifier consists of three balanced stages cascaded to produce the required gain and output power. The input and driver stages consist of 2 GaAs devices mounted in a balanced configuration. The output stage consists of four 1-Watt devices mounted as balanced pairs. The details of the amplifier design are discussed in this section.

3.1 SYSTEM OVERVIEW

The overall block diagram and power/gain budget is presented in Figure 3-1. The RF signal is fed to the input stage through a waveguide to microstrip transition. The input 3 dB coupler splits the power to the two input FETs. The signal is then amplified and recombined in the input stage output 3 dB coupler. Building each stage with its own input and output coupler allows the stage to be assembled and tuned outside the main amplifier housing, which greatly facilitates stage matching. Also, the isolation provided by the couplers minimizes interstage matching when all the stages are cascaded together. Similarly, the signal is amplified in the driver and output stage and finally transitioned back into waveguide.



GAIN (dB)	-0.5	-0.3	4.5	-0.3	-0.3	4.0	-0.3	-0.3	3.5	-0.3	-0.5	
POWER (dBm)	24.3	24.3	24.0	28.5	28.2	27.9	31.9	31.6	31.3	34.8	34.5	34.0

Figure 3-1. Amplifier block diagram and power/gain budget

3.2 AMPLIFIER CIRCUIT COMPONENTS

3.2.1 Waveguide-to-Microstrip Transition

The waveguide-to-microstrip transition consists of a series of quarter wave sections of ridge waveguide which transform the WR-42 TE10 mode to the

microstrip quasi-TEM mode. Figure 3-2 shows the insertion loss of two transitions connected back-to-back. The total insertion loss is typically 1 dB. The return loss of the transition from 18 to 23 GHz is greater than 20 dB, as shown in Figure 3-3.

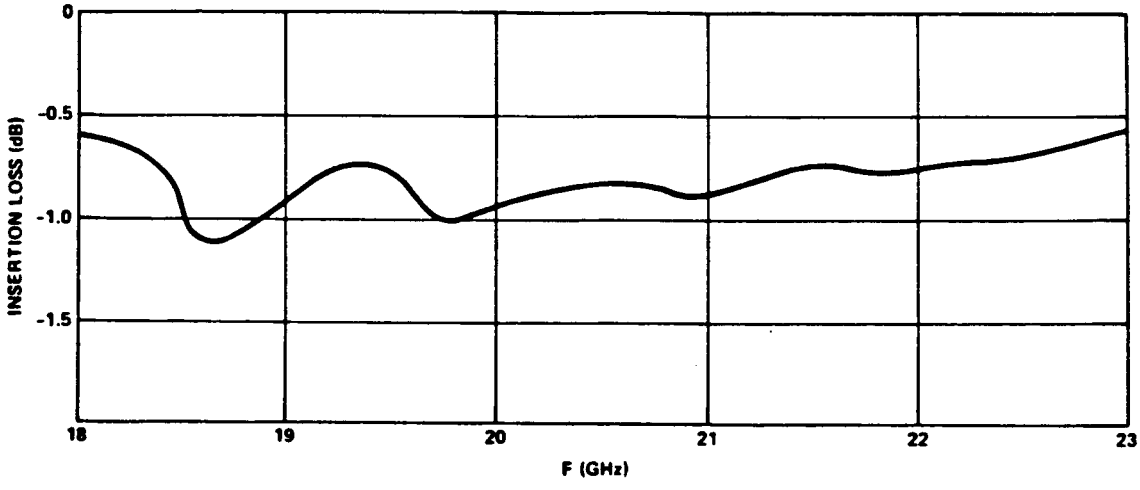


Figure 3-2. Insertion loss of two transitions connected back-to-back

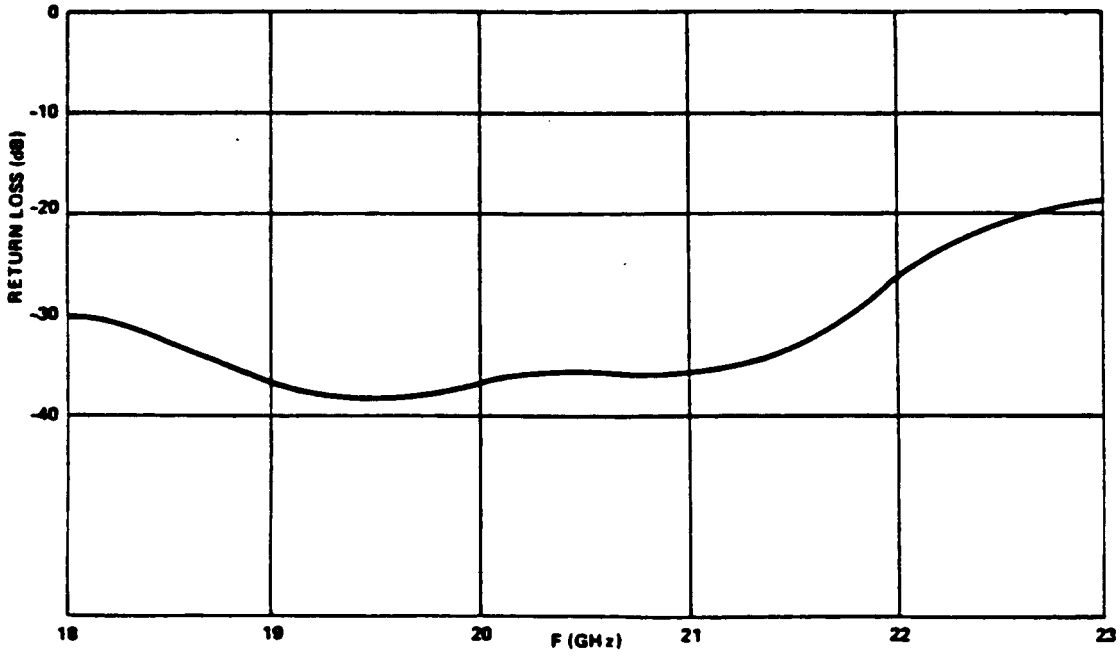


Figure 3-3. Return loss of waveguide-to-microstrip transition

3.3 3 dB COUPLER

The design of the 3 dB (Lange) coupler is based on the proximity coupling of two adjacent quarter-wavelength long microstrip lines. The coupled

microstrip lines may be analyzed in terms of two fundamental modes of propagation denoted even and odd. In the even mode, the current and voltages on the two strips are equal; in the odd mode, the current and voltages have opposite signs (see Figure 3-4). Any other pseudo-TEM propagation on the two strips can be expressed as a combination of these two modes. It can be seen from the figure that more of the even mode field lines are in the substrate than the odd mode field lines. Because of the nonuniform dielectric structure of microstrip, the odd and even modes have different phase velocities, and cause dispersion. The even, Z_{oe}, and odd, Z_{oo}, mode impedances required to achieve a desired power coupling ratio, C, are related by

$$C = 20 \log \frac{Zoe - Zoo}{Z_{oe} + Z_{oo}}$$

$$Z_0^2 = Zoe\ Zoo$$

Where Z_0 is the impedance to which the coupler ports are matched.

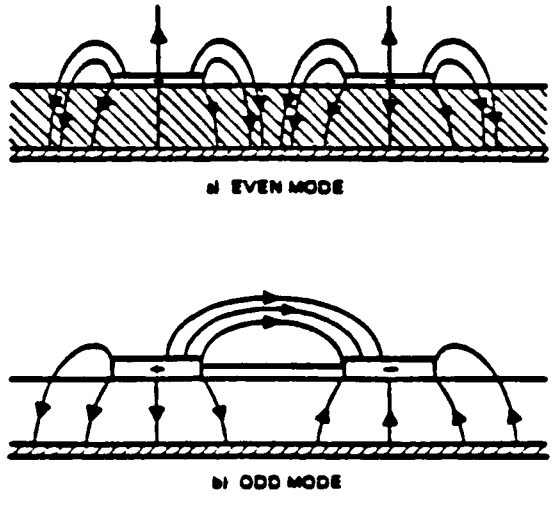


Figure 3-4. Electrical flux lines for two fundamental modes of two coupled microstrip lines

For a 3-dB coupler matched to 50 ohms, the even and odd mode impedance required is 120.7 and 20.7 ohms, respectively. The even impedance is determined primarily by the width dimension of the lines, whereas the odd mode impedance is a strong function of the proximity of the lines. In practice,

it is difficult to realize the low value of Z_{oo} required for 3 dB or tighter coupling using a single pair of edge-coupled transmission lines in microstrip.

There is a basic idea behind the interdigital coupler. For a given spacing between lines, a tighter coupling is derived with mutiple pairs of lines (alternately tied together at the ends) than is derived for a single pair (Figure 3-5).

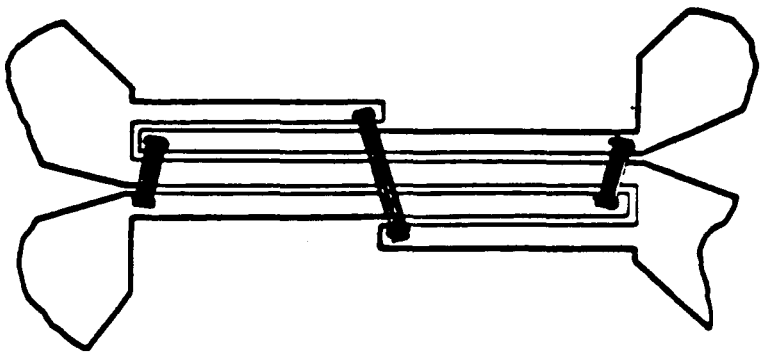


Figure 3-5. Layout and bonding of four-finger interdigitated coupler

The Lange couplers used for this amplifier are an improved version of those used at TRW in the past. The original couplers used wire to connect the fingers. These introduced significant inductance at the higher frequencies, which caused a poor phase relation and led to unacceptable passband ripple. The couplers used on this amplifier use air-bridge technology to minimize these problems. A low dielectric, polyimide insulating layer is used over the interdigitated fingers and a flat ribbon is used to electrically tie the fingers together. Typical performance data for these couplers is presented in Figure 3-6.

3.4 INPUT STAGE

3.4.1 Input Stage Design

The input stage consists of four RF substrates mounted on a common carrier. The first substrate is a Lange coupler. This splits the input energy and directs it to the two input FETs. The second substrate is the input matching substrate. This substrate provides the RF matching and dc voltage to the devices. A bypass capacitor is used on the RF line to

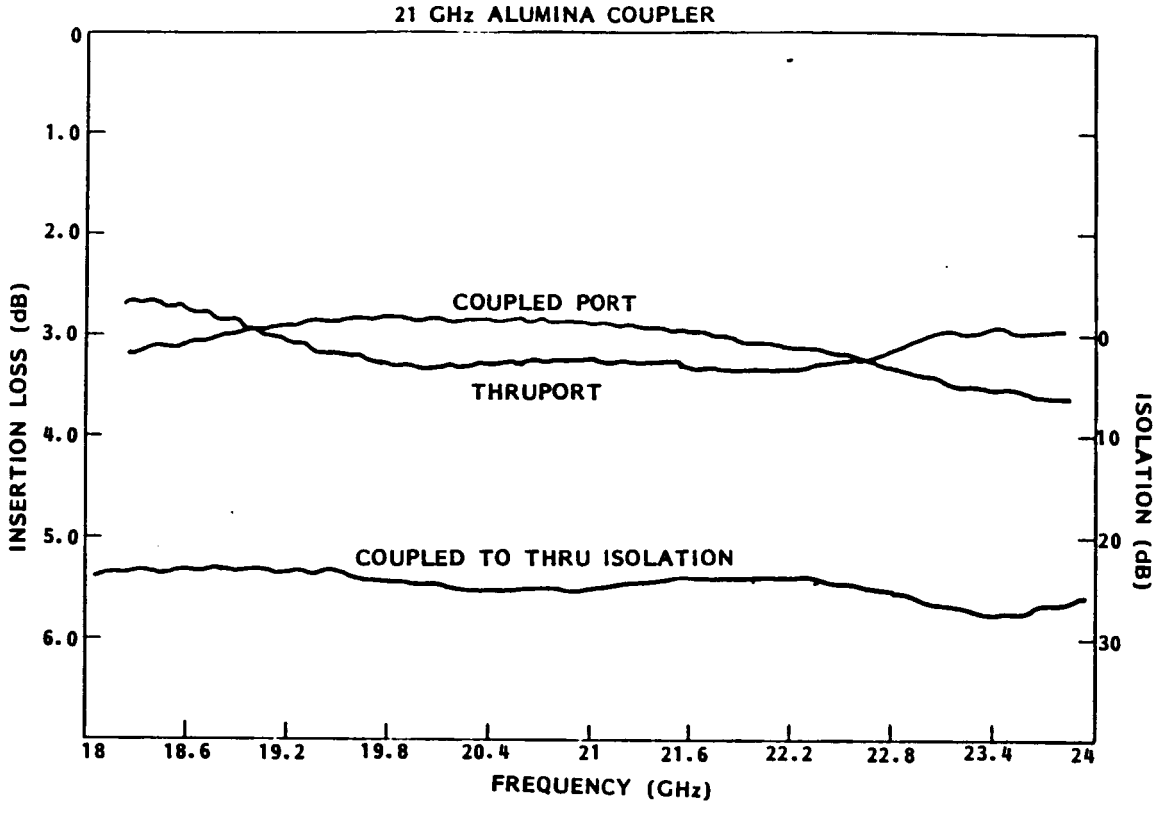


Figure 3-6. Measured performance of typical 18 to 24 GHz coupler

provide dc isolation. The devices are mounted to the carrier next to the input matching substrate and bonded to the substrate with gold wire. Following the FET devices is the output matching substrate. This serves to match the RF output and provide dc voltage similar to the input matching substrate. Finally, the output Lange coupler recombines the RF energy. The four substrates are connected electrically with gold ribbon.

3.4.2 Input Stage Performance

The input stage described above was built using two Raytheon half watt devices (R2012). The 1 dB compression point data is presented in Figure 3-7, and the gain vs. frequency data, in Figure 3.4-2. The small signal gain is flat at 4.5 dB from 19.5 to 21.1 GHz and the 1 dB compression point is +26.3 dBm. The input stage return loss over this frequency range is better than 15 dB, as shown in Figure 3-8.

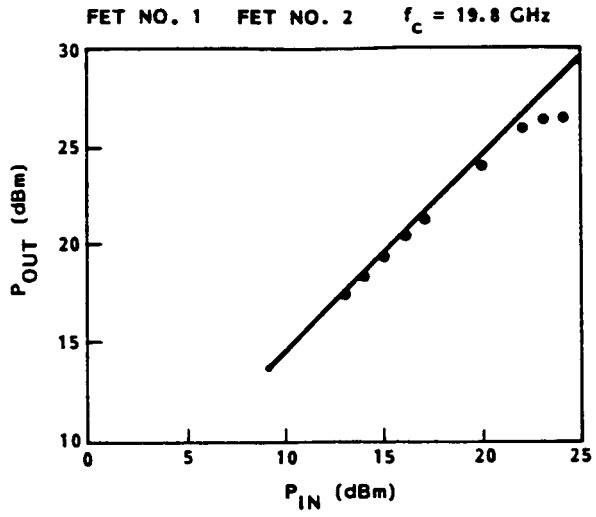


Figure 3-7. Raytheon 1/2 W balanced stage

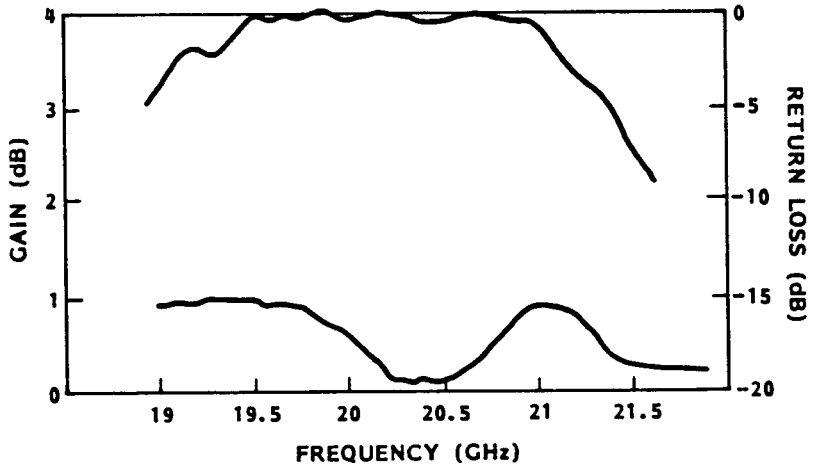


Figure 3-8. Raytheon 1/2 W balanced stage

3.5 DRIVER STAGE

3.5.1 Driver Stage Design

The driver stage design is identical to the design of that of the input stage with the exception of the input and output matching circuits. These matching circuits have been optimized for use with the Raytheon 1 Watt FET devices.

3.5.2 Input and Driver Stage Cascaded Performance

The input and driver stage were cascaded together and their performance measured. Figure 3-9 shows the small signal gain of the two stages, which

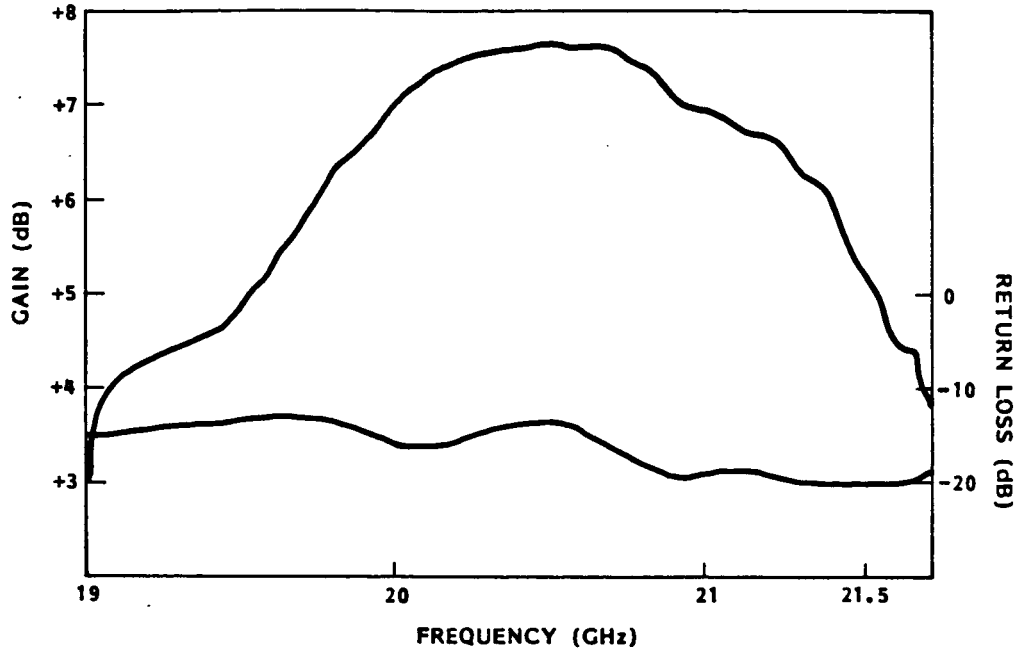


Figure 3-9. Cascaded 1/2 W and 1 W balanced stages

is 7.1 ±0.5 dB over a 1.2 GHz bandwidth centered at 20.5 GHz. The output power over this frequency band is +29 dBm, as shown in Figure 3-10. The input return loss (Figure 3-9) was better than 13 dB over the operating frequency range.

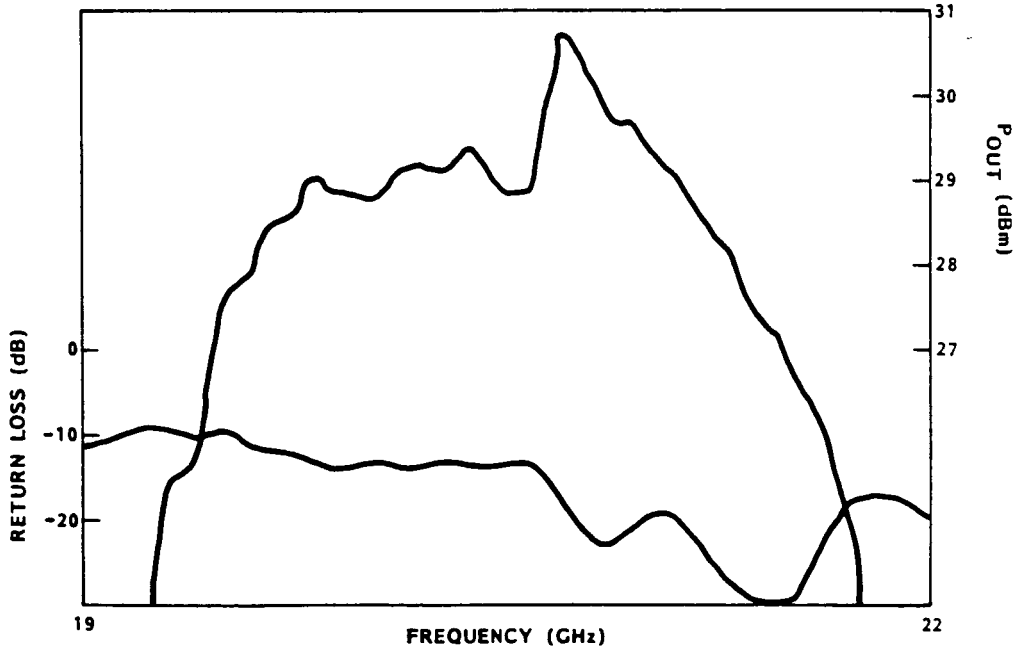


Figure 3-10. NASA 1/2 W and 1 W open loop (no ALC)

3.6 OUTPUT STAGE

3.6.1 Output Stage Design

The output stage consists of an input Lange coupler, an input/output matching circuit, and an output Lange coupler (as in the first two stages). However, the matching circuits are different because two 1 Watt devices are used in each balanced arm.

3.7 DC CIRCUITRY

One of the most important and often overlooked aspects of a power amplifier design using GaAs FET circuits is the dc circuitry considerations and the impact of proper dc biasing to maintain performance of these circuits over temperature.

FET devices undergo an inherent reduction in gain as the temperature of the device increases. In general, the gain and output power variations with temperature can be substantial. To control this change in gain and output power, regulators have been developed to maintain the amplifier performance over temperature. This is accomplished by constant current regulators that control the IDS through the FET devices.

In a FET, RF gain and output power changes with temperature can be attributed to the following changes in the active layer properties:

- Carrier-drift mobility decreases with temperature
- Peak-drift velocity decreases with temperature
- Pinchoff voltage increases with temperature, effictively reducing the transconductance.

The net result of these factors is a decrease in the drain current, causing simultaneous decreases in amplifier gain and output power, with an increase in temperature.

To stabilize gain and power over a temperature range, drain current has to be stabilized. This is accomplished by employing constant current regulators.

The bias regulators operate by sensing the amount of current drawn through a small series resistor in the drain bias supply. The voltage is amplified via the gain of PNP active bias regulator and fed to the JFET gate

to form a negative dc feedback loop. The large open loop gain of this combination and proper phase compensation result in a very stable bias regulator.

This type of current regulator (shown schematically in Figure 3-11) has been incorporated into numerous FET amplifier designs at TRW and has resulted in very stable amplifier design using GaAs FET devices.

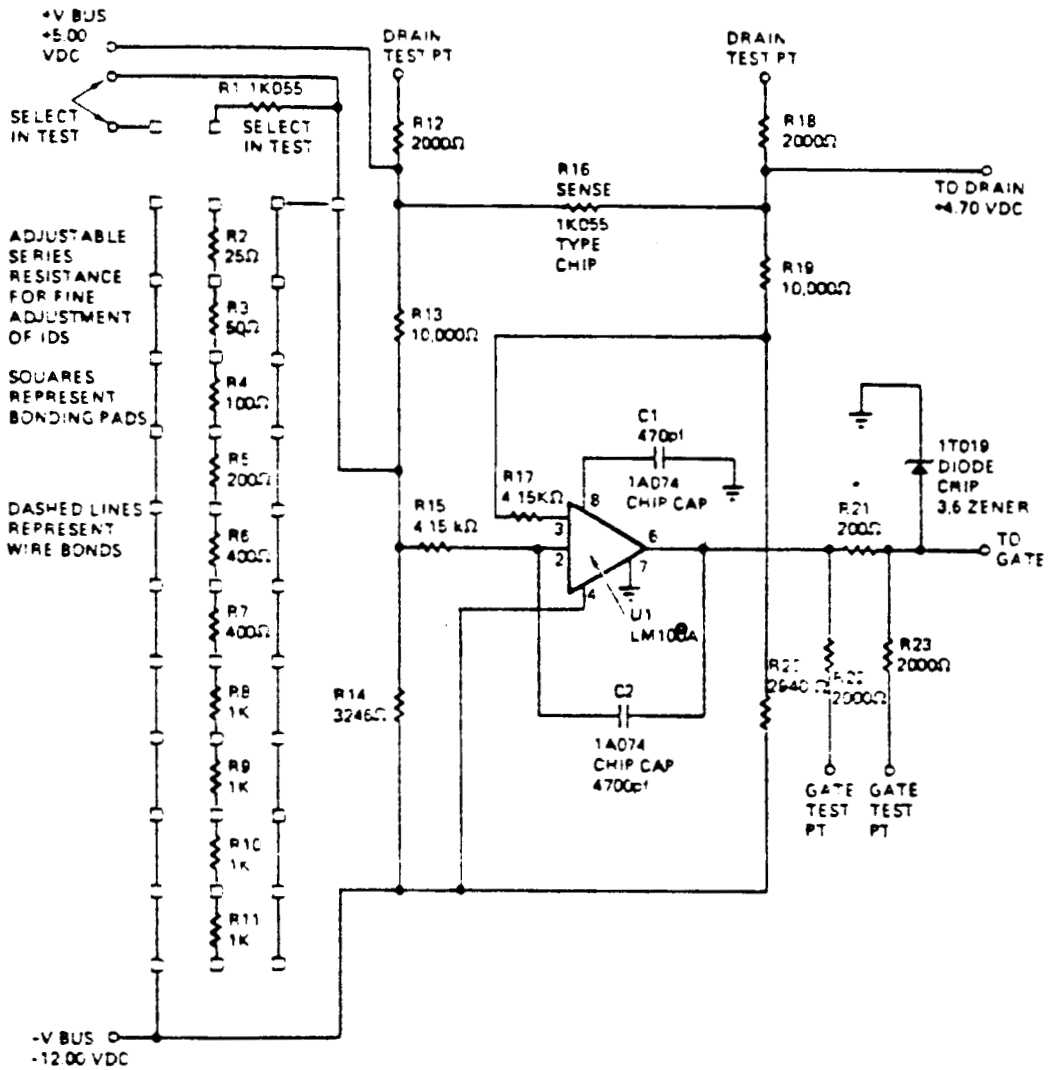


Figure 3-11. Current regulator schematic

4. MECHANICAL PACKAGING

4.1 AMPLIFIER PACKAGING

The amplifier is packaged in a machined aluminum housing which accommodates all the amplifier stages and current regulators. The advantages of using aluminum are its light weight and high thermal conductivity. The housing is plated with an electroless nickel base plating followed by a copper buffer layer to provide a compatible plating surface for the exterior gold layer of 100 inches. The housing has three machined out cavities: the main cavity accepts the three amplifier stages and the two waveguide-to-microstrip transitions; the two side cavities accept the current regulators. DC bias connections from the regulators are made using feedthrough connectors soldered into the housing. This provides isolation between the amplifier stages and current regulators. The transitions are machined pieces which are screwed onto the housing.

Three covers provide amplifier seals, one for the main cavity and two for the side cavities. Figures 4-1 and 4-2 are photographs of the assembled amplifier. The amplifier stages can be seen in Figure 4-1, and the current regulators can be seen in Figure 4-2.

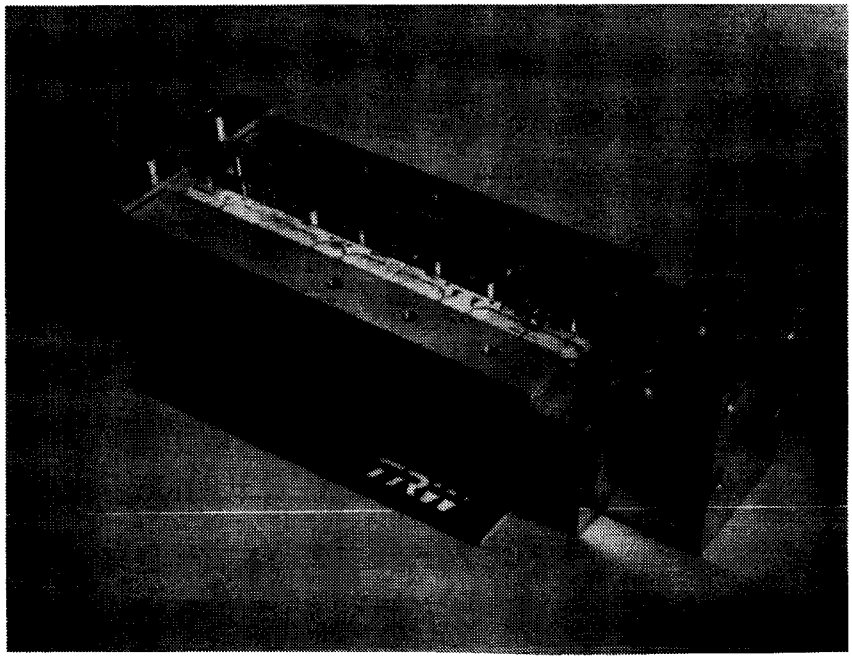
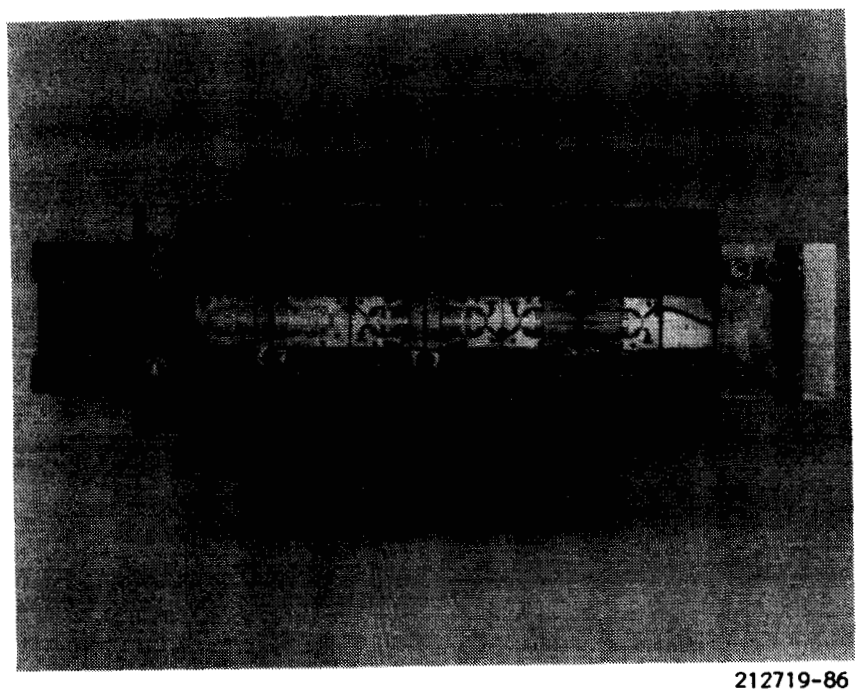


Figure 4-1. 20 GHz 2.5 W amplifier 212720-60



212719-86

Figure 4-2. 20 GHz 2.5 W amplifier

5. CONCLUSIONS AND RECOMMENDATIONS

As the report indicates, most processing steps used during the course of this program did not give concrete evidence of marked improvements in device performance. As often happens in device development, the process development phase could last for a long time without any improvement. Then, a significant improvement in device capabilities will occur within the whole industry due to the high competitive nature of this business. At the time this report was written, a number of companies, including Raytheon, had developed 1 Watt devices with impressive results. For example, Raytheon's 1 Watt devices have yielded 4.5 dB linear gain across a bandwidth of 19 to 22 GHz when operated in an amplifier. They also have a power added efficiency of 28 percent. Avantek recently completed the development of an 18 GHz, 1 Watt device providing 7.5 dB gain; Microwave Semiconductor Corporation (MSC) in Somerset, New Jersey, is making impressive advances in FET devices. Primarily, they are using processes similar to Raytheon and expect to have 20 GHz, 1 Watt capabilities shortly. In addition, Raytheon's S203-4 is a 4 mm periphery device. COMSAT is currently developing an MMIC device with a predicted performance of 4 Watt power output, 5 dB gain with 25 percent power added efficiency at 20 GHz.

Although many devices are becoming available, they are not being sold in quantity. Thus, though the technology has made significant advances, it is not yet mature. We do anticipate that the technology will advance enough whereby at least the 20 GHz, 1 Watt devices will be available in the near future.

At the same time, the power combining techniques have also been rapidly progressing. The most significant development in the power combining technology is the radial combining area. A 16-way radial combiner can be made almost as efficiently as an 8-way radial combiner. The additional insertion loss of a 16-way radial combiner is only 0.2 to 0.3 dB compared with an 8-way combiner at 20 GHz. In a recent experiment in which a 20 GHz, 10 Watt amplifier with 20 percent power added efficiency was designed (there was a choice of devices between a 1 Watt device with 30 percent efficiency and a 2 Watt device with 25 percent efficiency), the 1 Watt, 30 percent efficient device was determined to have a definite advantage.

In conclusion, the development of a 20 GHz amplifier with 20 dB gain, 20 percent efficiency and an output power of 30 to 40 Watts is definitely feasible, and we highly recommend the establishment of such a program.

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16. Abstract

This report describes the development of power FET operating in the 20 GHz frequency band. The major efforts include GaAs FET device development(both 1W and 2W devices), and the development of an amplifier module using these devices.

Power FET developments were carried out by Solid State Device Group of Special Microwave Device Operation, Raytheon Company, Northorough, Massachusetts. The amplifier module development was performed by TRW Defense and Space Systems Group, Redondo Beach, California.

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