THE SIR-C GROUND DATA SYSTEM: DIGITAL PROCESSOR, DATA PRODUCTS, INFORMATION FLOW

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The SIR-C instrument will collect both C-Band and L-Band data with each frequency band consisting of direct (HH or VV) and cross-polarized (HV or VH) data. Considering all possible combinations as many as eight different data channels will be available for any given target area. This data will be digitized and formatted on-board for direct downlink via the Tracking and Data Relay Satellite System (TDRSS), or it will be buffered through on-board high density digital recorders for storage or transmission when TDRSS is available. The data is received by the TDRSS ground station at White Sands and is nominally relayed via DOMSAT to the high data rate recording facility at GSFC (Figure 1). The tapes are then shipped to JPL for processing into imagery and eventual distribution to the SIR-C investigators.

I. IMAGE PROCESSING

All SIR-C raw data is to be processed digitally by the Advanced Digital SAR Processor (ADSP). This processor, designed and built by JPL, can perform SAR image correlation at real-time or near real-time throughput rates. The system configuration for SIR-C is shown in Figure 2. It centers around the ADSP which consists of four racks of VSLI circuit boards controlled by a VAX 11/785. The system also features a SIR-C custom input interface, two high density digital recorders for the input and output data, a scrolling display with a video cassette recorder (VCR) and a laser beam recorder (LBR) for quick-look image products.

The input interface contains the logic necessary to decode the sub-commutated header data in real-time, reformat the block floating point coded data into integer bytes, and perform data quality analyses such as BER checks, radar parameter change detection, or data drop-out detection. The decoded header data is transferred to the VAX controller for initialization of the autofocus and clutterlock algorithms. In addition, this data is used for determination of range line and reference function sizes as well as estimation of the geometric and radiometric correction parameters (e.g., antenna pattern, incidence angle, azimuth skew, slant range, etc.).

The correlation algorithm is essentially two one-dimensional matched filtering operations performed in the frequency domain (Figure 3). The reference functions are determined from the characteristics of the transmitted pulse for the range reference and from the Doppler characteristics of the echo data for the azimuth reference.

The ADSP can perform up to $6 \cdot 10^9$ complex operations per second. It is designed to process SAR raw data into imagery in strips rather than on a frame-by-frame basis as in SIR-B. It also has the capability to dynamically update the azimuth reference function during the processing to compensate for variations in the earth rotation rate or the shuttle attitude. However, the

ADSP has limited capability for updating the radiometric and geometric correction parameters. This may require, depending on the stability of the shuttle during a data take and the application of a specific data set, special processing to maintain the fidelity of the output product. For this purpose a special purpose processor (SPP) has been added to perform postprocessing operations on the image products. This system will interface with the ADSP output and will include an array processor, mass storage, a video display and a frame-type film recorder. Its primary function is to meet the special processing requirements of the SIR-C investigators on selected segments of image data.

II. DATA PRODUCTS

The SIR-C raw data set will consist of digitized echo data of two frequencies with each frequency containing one to four different polarizations. Contained in the raw data header are the radar parameters and shuttle parameters required for the processing. In addition, high precision postflight attitude and trajectory files will be available 2 to 3 months after the mission.

In the processor timeline, a period for data validation and sensor performance evaluation of approximately 1 month will be allotted. Following this period data will be processed in a quick-look mode to assess the quality and specific coverage of the data set. As a minimum for the survey processing, one image set (up to 4 channels) will be produced for each of the planned 50 investigator sites. This output will be recorded on HDDT and video cassettes (or film strips) of this imagery will be distributed to investigators over their test sites. The survey processing will not involve any special corrections for shuttle instability, or registration of multiple polarizations or frequencies and will require approximately 2 months. All imagery will consist of detected (real), 4-look pixels.

The third phase of the processing, requiring approximately 9 months per flight, will produce image products as per the primary investigation for each data take. The SIR-C processor is capable of allowing options such as: (1) complex data, 16-bit floating point; (2) single-look, double-look or 4-look data; (3) real data, 8-bit or 16-bit integer; (4) range compressed only data; (5) radiometrically uncompensated data; and (6) slant range deskewed data. However, discussions are on-going in an attempt to define a single image standard. The real-time output will be recorded on HDDT and film strips via the laser beam recorder. These film strips will be annotated with time and location each 10 seconds ($\approx$ 75 km) and an ancillary data record generated for each data take containing the full set of shuttle, processor and radar parameters including updates of time varying parameters each 10 seconds. The ancillary data record will be stored in the SPP and written to CCT for distribution to the investigators. This processor will interface to both the HDDR and the ADSP and serve an additional function as the SAR data catalog. In parallel with refinement of the standard image products as described above, this processor will produce a limited amount of special products as required by the investigators. For example, within this category are: (1) geocoded images (i.e., rotated to north and resampled to specified map projection); (2) radiometrically calibrated products in geophysical units (i.e., backscatter coefficient); (3) imagery corrected for foreshortening due to terrain

variations; and (4) pure phase imagery, phase difference between any two polarizations, or magnitude ratios between polarizations or frequencies. Depending on the amount of special processing, it is expected that this phase of the processing will last from 9 to 12 months, being completed approximately 15 months following the second mission.

III. DATA DISTRIBUTION

As previously described, the special purpose processor will also act as a data base management system for the SIR-C, and to a limited extent, the entire terrestrial SAR catalog. It will contain all of the fundamental and derived parameters for the SIR-C data set. This catalog will contain maps illustrating the SIR-C coverage as well as the capability to cross-reference target location with any of the SIR-C parameters to determine the extent of a particular type of coverage. In addition, coverage maps from SEASAT, SIR-A, and SIR-B will be available with algorithms to determine the extent of multisensor/multimission coverage.

This catalog will be accessible by modem to remote users for determination of processing status, coverage of a target area, or to communicate to the processing team a special processing or distribution request. It is also desired, depending on technological development, to provide the capability for on-line access of low resolution image data to remote users. This will depend primarily on the expected development of mass optical disk storage and high data rate modems and communication links.

The primary means of product distribution will be via mail in one or more of the following forms. The initial product will be a quick-look video cassette (or optical disk if practical) or film strip of the investigator's test area. This will be provided approximately 3 months postflight primarily for survey purposes. Associated with this will be a limited ancillary data set with periodic time and location updates. Note that the high precision ephemeris and attitude data will not be available in this time frame, therefore, the radiometric and geometric fidelity of the survey products may not meet final product requirements.

Based on the investigators' evaluation of the survey products and a priority schedule determined by the science team, production and distribution of the final products will begin 3 months postflight and will last for a period of approximately 1 year for each flight. This system will be designed to optimally meet the special needs of the investigators by having the capability to generate a variety of image products. The large volume of data associated with full resolution SAR imagery precludes electronic transfer of this imagery in the SIR-C time frame. However, the processor development plan will include - as a minimum - access to the SIR-C ancillary data set and potentially remote access to low resolution or compressed SIR-C imagery.

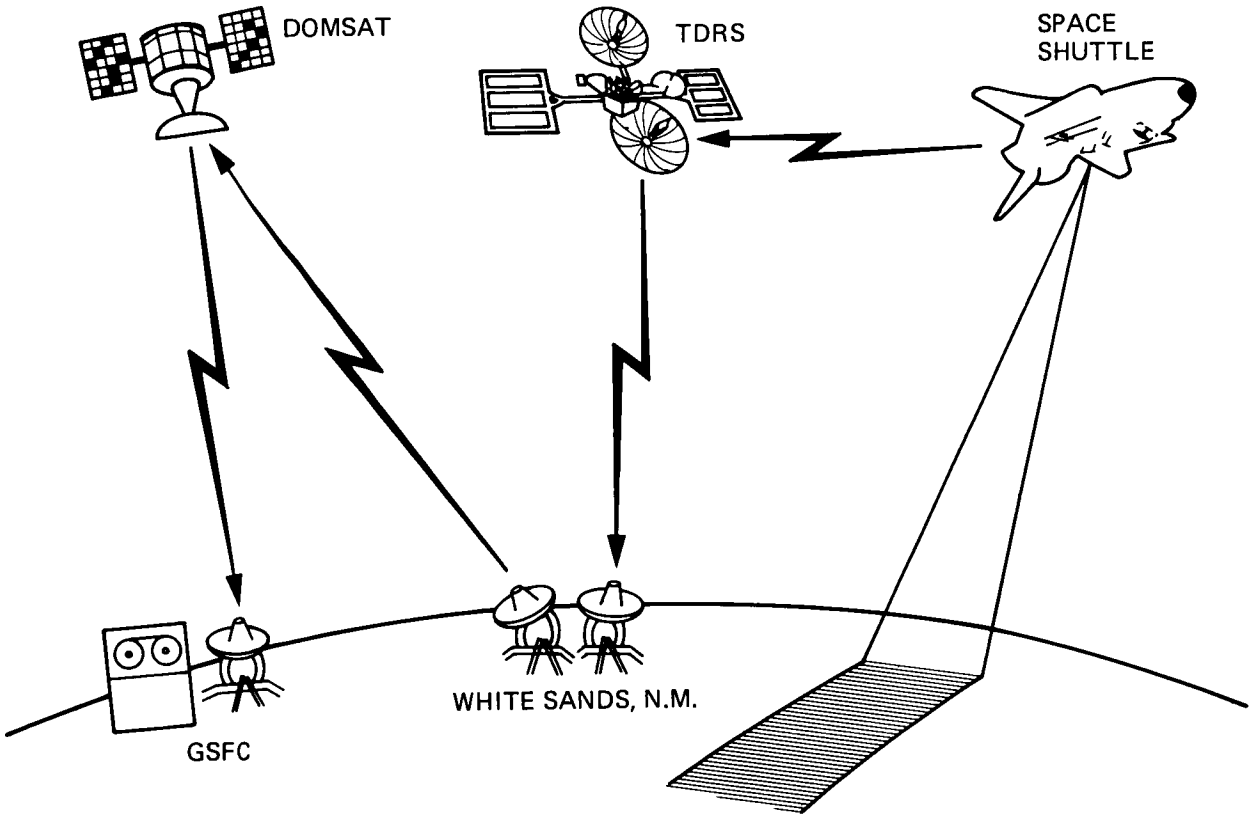

Figure 1. SIR-C data flow

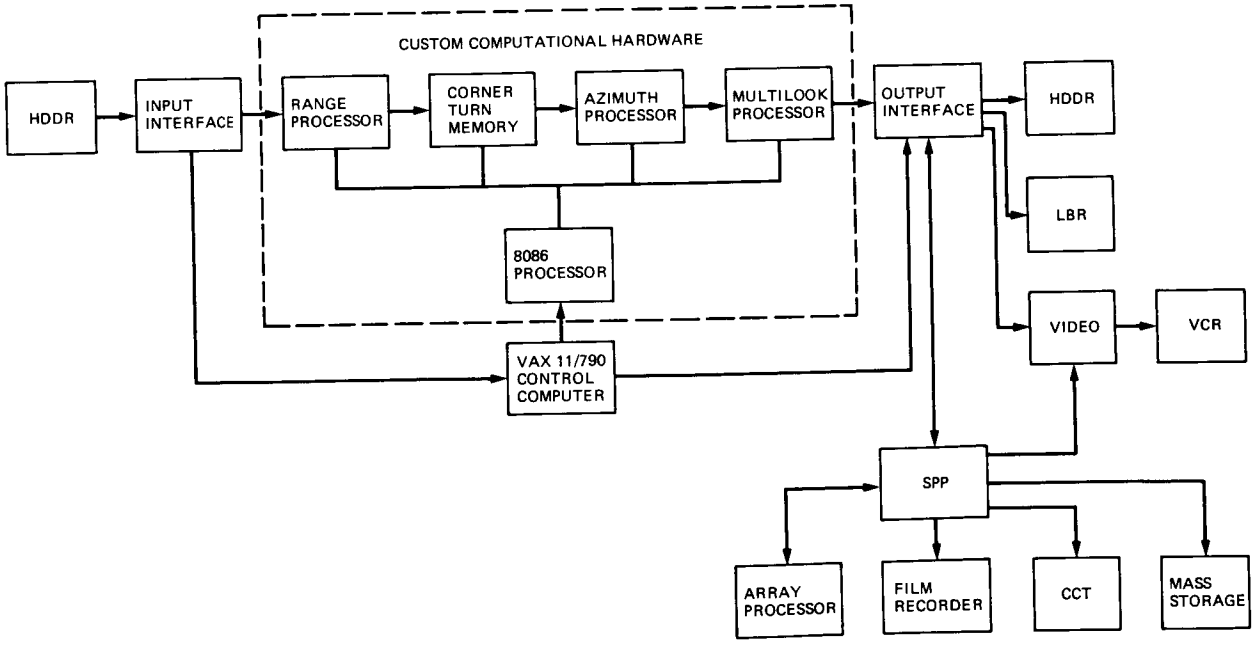

Figure 2. SIR-C processing system block diagram

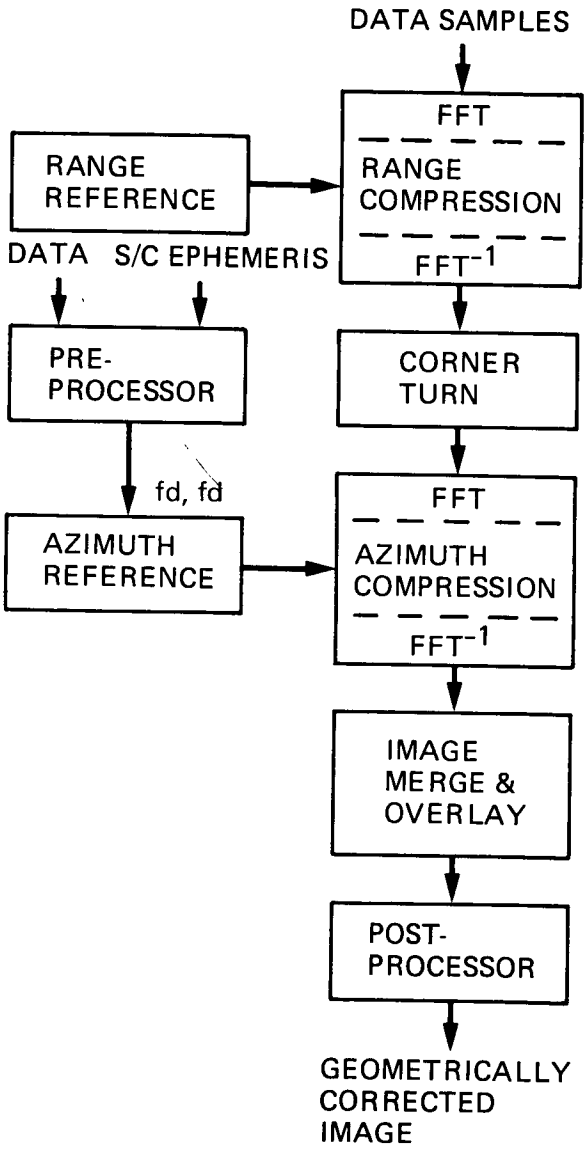

Figure 3. Functional block diagram of SAR processing algorithm

AN OPTIMUM SAR PROCESSOR

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I. INTRODUCTION

Recent experience has shown that synthetic aperture radar (SAR) processing costs can be prohibitively large when conventional computers and/or array processors are used. Special-purpose signal processors are unattractive because it is generally not cost effective to develop such devices for a single application. The problem is to find an architecture which is both optimized for SAR processing yet flexible enough to be used for a variety of systems and modes. This paper describes a flexible SAR processor which has been built, tested and shown to be a cost-effective solution to the problem.

II. ARCHITECTURAL APPROACH

SAR image formation requires a sequence of independent steps performed on complex data vectors. The optimum way to implement the sequence is as a pipeline interconnection of processing elements (PEs), each of which works on a vector and then passes it on (see Figure 1). As some PEs may be faster than others, it is often necessary to "fan out" the pipeline into parallel paths at various points.

The monumental task of scheduling data through many simultaneously active PEs is avoided by asynchronicity, achieved through double buffering the PEs (see Figure 2).

Each PE could be a general-purpose computer or array processor, and although this minimizes the need to develop new hardware, it can lead to excess equipment in proportion to the computational rate achieved. The optimum PE should implement only those functions needed at its stage in the pipeline. Because the processing operations are ultimately arithmetic, it might seem that a central processing unit (CPU) would be a good choice as a universal PE. The problem is that decomposing the functions to such a low level results in excessive numbers of buffers and data paths. A better approach is to escalate the functional complexity to the highest level which neither restricts flexibility nor results in redundant capabilities. For example, all SAR algorithms can be implemented with only seven high-speed functions:

1. Fast Fourier Transform - used for range and azimuth matched filtering
2. In-Plane Filter - filter samples along a data vector
3. Cross-Plane Filter - filters across data vectors
4. Reference Function Generator - stores and/or creates reference functions and applies them to the data

5. Corner-Turn Memory - allows data to be written by columns and read by rows, and vice versa

6. Automatic Focus - removes residual phase errors

7. Detector/Log Encoder - converts output samples to logarithmically encoded image pixels.

III. IMPLEMENTATION

If interconnecting the PEs required wiring backplanes and designing interfaces, the development of an optimum processor would be too expensive. This problem is solved by the implementation of Figure 3, which shows the processor as a wheel, with a matrix crossbar switch at the hub, the PEs as spokes, and a control and initialization bus at the rim.

The structure of Figure 3 implements the features of an optimum processor as follows:

1. Modularity - the processor is scaled to a specific requirement by "plugging in" only the precise combination of PEs needed.

2. Reconfigurability - the machine is reconfigured by reprogramming the crossbar switch, either before processing (to establish a base configuration) or during processing (to time multiplex PEs).

3. Control - The PEs are initialized and controlled by a combination of (a) instructions from the control microcomputer via the control bus and (b) operation codes and data tags contained in vector header words.

4. Test and Fault Isolation - the control computer can test each PE independently by inserting test patterns and comparing the results with prestored responses.

5. Graceful Degradation - spare PEs can be provided so that if an active PE fails, the spare can be switched in without loss in processing time. Even when spares are unavailable, it is often feasible to shift the load of a failed PE to another unit by time multiplexing, thus leaving the processor functionally operational but at a reduced throughput rate.

IV. CONCLUSION

The nature of SAR processing dictates a pipeline parallel interconnection of PEs. While any number of bus structures and PE types can be envisioned, the scheme above has already been developed and shown to be successful.

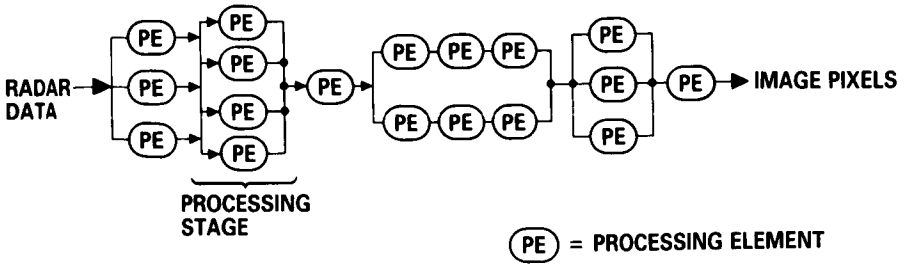

Figure 1. The optimum SAR processor is a pipeline/parallel interconnection of processing elements.

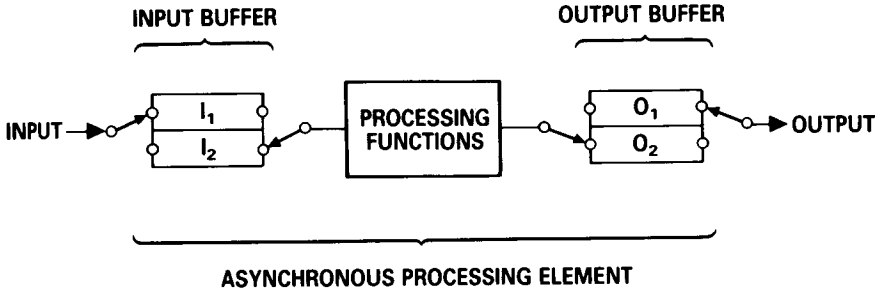

Figure 2. Asynchronicity requires PEs with input and output double buffers.

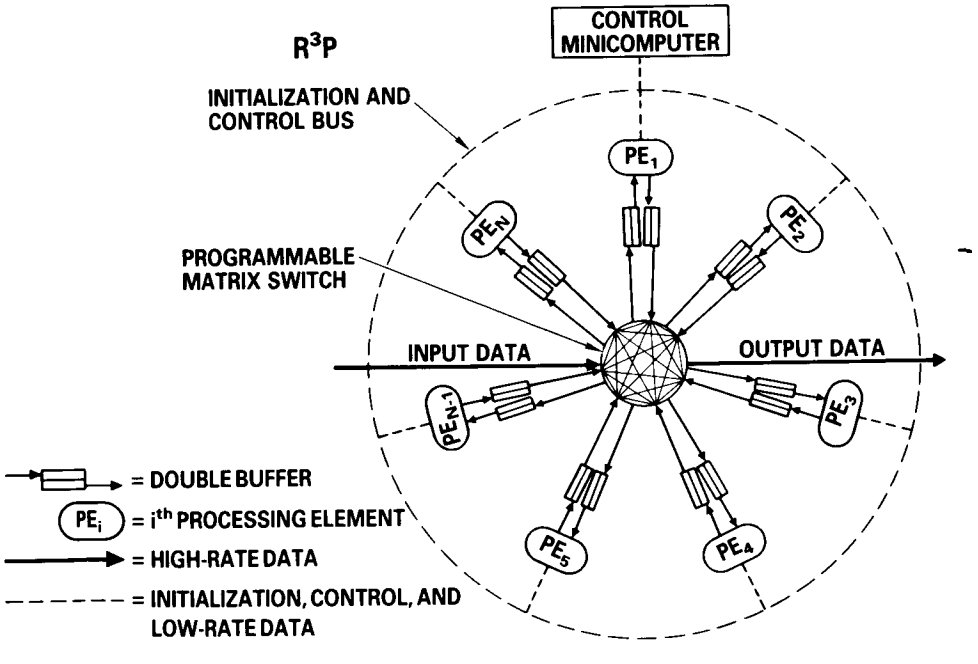

Figure 3. Processing elements and a crossbar switch are used to implement the optimum SAR processor.